ABSTRACT

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As CMOS technologies scale beyond sub-90nm process nodes, one of the major hurdles that the CMOS devices face is increasing manufacturing process parameter variations. This has resulted in device characteristics to be more sensitive to these process variations and thus increased the uncertainty in circuit performance parameters like delay and leakage power, leading to loss in parametric yield.

The Process Design Kit(PDK) which is an integral part of the design flow needs to enhance the communication across the design-manufacturing interface. This would aid in design for manufacturing, to handle the effect of process variations and result in robust, high performance design. The PDK needs to be variation aware in order to achieve this.

This thesis work provides a framework to study and incorporate the effects of random process variations, systematic layout dependent variations, for use with circuit extraction and simulation tools and thus make a PDK variation aware. Modeling the effects of random process variations on circuit performance parameters is done using Response Surface Methodology and Design of Experiments, Statistical Circuit Analysis is carried out with this information. For systematic layout dependent variations, compact model instance parameters due to Well Proximity Effects are extracted according to guidelines from Compact Model Council. An example illustrating the complete flow is presented along with the results from other sample circuits.

Circuit Extraction and Simulation in the presence of Random and Systematic Process Variations

by

Sunil Basavarajaiah

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APPROVED BY:

Dr. Paul Franzon

Dr. Doug Barlage

Dr. W.Rhett Davis
Chair of Advisory Committee

DEDICATION

To my family for their unconditional love and support.

BIOGRAPHY

Sunil Basavarajaiah was born on 1st October 1982 in Bangalore, India. He received his Bachelors degree in Electronics and Communication Engineering from M.S.Ramaiah Institute of Technology, Visvesvaraya Technological University in 2004. After undergraduate studies, he worked in Hical Magnetics Pvt Ltd for 8 months and then in WIPRO Technologies for 16 months. In Fall 2006, he began his graduate studies in the Electrical and Computer Engineering Department at North Carolina State University, NC. Since Spring 2007, he has been working in the Methodologies for User-friendly System-on-a-chip Experimentation (MUSE) group under the guidance of Prof. Rhett Davis.

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Chapter 1

Introduction

Today's chip design is facing several challenges due to increasing circuit complexity and decreasing feature size, currently in nano-meter scale. Apart from the challenges that directly arise as a result of feature scaling (e.g. increasing leakage power and interconnect delay, reliability issues), imperfections in the fabrication process for nano-scale feature sizes have recently become a major design hurdle, as they randomize the electrical properties of the components on the chip.

Worst case and best case SPICE models are used by the designers to verify the design at the extremes of process variations. In this case, the design can be overly pessimestic. From an IC design perspective, a shift in paradigm, from deterministic to probabilistic, is needed to handle the unpredictable nature of these fabrication variations. Also, the effects of systematic process varitions which can be modeled accurately needs to be taken into account during the design phase.

1.1 Motivation

Most Electronic Design Automation tools do not take into account the substantial electrical uncertainty in transistors due to manufacturing/process variabilty. As a result, static timing analysis tools needlessly overestimate operational delay in the circuits, and introduce significant pessimism into the operational frequency of a design. Also, other circuit performance parameters might also be overly estimated [4]. This highlights the need for accurate consideration of process variations and resulting parametric uncertainty in logic and circuit design. In Fig. 1.1, %-effect on sign off delay as a function of parametric

variation is predicted in shrinking devices [2].

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
Parameter uncertainty:%-effect (on signoff delay)	6%	8%	10%	11%	11%	12%	14%	15%	18%
Year of Production	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*		
Parameter uncertainty: %-effect (on signoff delay)	20%	20%	20%	22%	25%	26%	28%		

Figure 1.1: Parameter uncertainty and %effect on sign off delay [2]

1.1.1 Design For Manufacturability (DFM)

DFM largely centers on developing methodologies/technologies to improve yield by enhancing the communication across the design-manufacturing interface. The increase in yield in turn increases the overall profitability and return-on-investment of chip makers'. The manufacturability criteria of the chip needs to be considered during the design flow. The key challenges in the manufacturing and its effects is quantified as DFM Technology requirements in Figs. 1.2 and 1.3 [2]. It summarizes the percentage variability in V_{th}, critical dimensions and also circuit performance/total power/leakage power variability.

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
Normalized mask cost from public and IDM data	1.0	1.3	1.7	2.3	3.0	3.9	5.1	6.6	8.7
% V_{dd} variability: % variability seen in on-chip circuits	10%	10%	10%	10%	10%	10%	10%	10%	10%
% V_{th} variability: doping variability impact on V_{th}, (minimum size devices, memory)	31%	35%	40%	40%	40%	58%	58%	81%	81%
% V_{th} variability: includes all sources	33%	37%	42%	42%	42%	58%	58%	81%	81%
% V_{th} variability: typical size logic devices, all sources	16%	18%	20%	20%	20%	26%	26%	36%	36%
% CD variability	12%	12%	12%	12%	12%	12%	12%	12%	12%
% circuit performance variability circuit comprising gates and wires	46%	48%	49%	51%	60%	63%	63%	63%	63%
% circuit total power variability circuit comprising gates and wires	56%	57%	63%	68%	72%	76%	80%	84%	88%
% circuit leakage power variability circuit comprising gates and wires	124%	143%	186%	229%	255%	281%	287%	294%	331%

Figure 1.2: Design for Manufacturability Technology Requirements-Near-term Years [2]

To address DFM technology requirements, the DFM solutions described in Fig. 1.4 [2] will be needed. DFM solutions mentioned in Fig. 1.4 will have to directly address and tolerate various dimension of variability. Among these solutions, we are interested in

- Statistical analysis and optimization tools/flows.

Year of Production	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
Normalized mask cost from public and IDM data	11.4	14.9	19.6	25.6	33.6	44.2	57.7
% V_{dd} variability: % variability seen in on-chip circuits	10%	10%	10%	10%	10%	10%	10%
% V_{th} variability: doping variability impact on V_{th}, (minimum size devices, memory)	81%	81%	112%	112%	112%	112%	112%
% V_{th} variability: includes all sources	81%	81%	112%	112%	112%	112%	112%
% V_{th} variability: typical size logic devices, all sources	36%	36%	50%	50%	50%	50%	50%
% CD variability	12%	12%	12%	12%	12%	12%	12%
% circuit performance variability circuit comprising gates and wires	63%	65%	66%	69%	69%	71%	73%
% circuit total power variability circuit comprising gates and wires	92%	96%	102%	110%	121%	130%	140%
% circuit leakage power variability circuit comprising gates and wires	368%	381%	395%	360%	325%	477%	628%

Figure 1.3: Design for Manufacturability Technology Requirements-Long-term Years [2]

- Tools that consider both systematic and random yield loss.

1.1.2 Implications of Process Variation on Microprocessors & ASICs

As an example to illustrate the effect of process variation, the profit functions of Microprocessors and ASIC are given in Fig. 1.5 [17]. The operating frequency is a very important requirement for Microprocessors and ASIC. Across a wafer of microprocessors, some of the manufactured chips are able to operate at $b1$ while others may have to operate at $a1$, due to process variations. The chips at $a1$, although slower, can be still be sold at a lower profit i.e. they can be speed binned at a lower frequency. But in the case of ASICs, chips with clock period $>$ than $b2$ needs to be simply discarded.

1.2 Goal of this Work

The major objectives of this work is

- To provide a framework/methodology for statistical analysis using Response Surface Method (RSM) and Design of Experiments (DoE) to model the effects of Random Process Variations on circuit performance parameters.
- To understand the effect of systematic variations due to Well Proximity Effect.
- To provide examples that utilize the methodology and assess the impact of random and systematic variations.

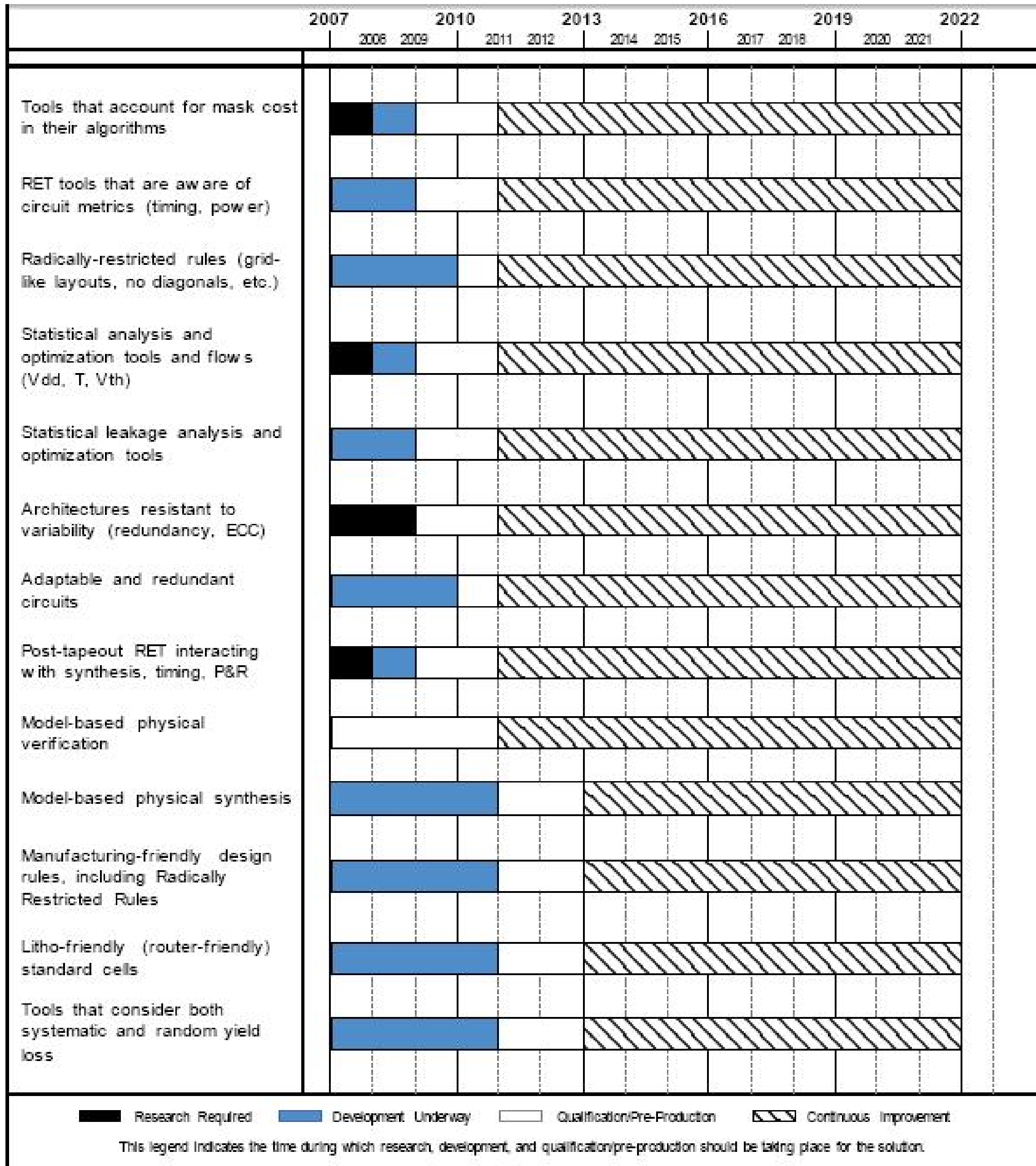

Figure 1.4: Design for Manufacturability Potential Solutions [2]

1.3 Thesis Organization

The thesis is organized as follows: Chapter 2 gives an overview of the kinds of process variations and methods to handle them. Chapter 3 explains the methodology used

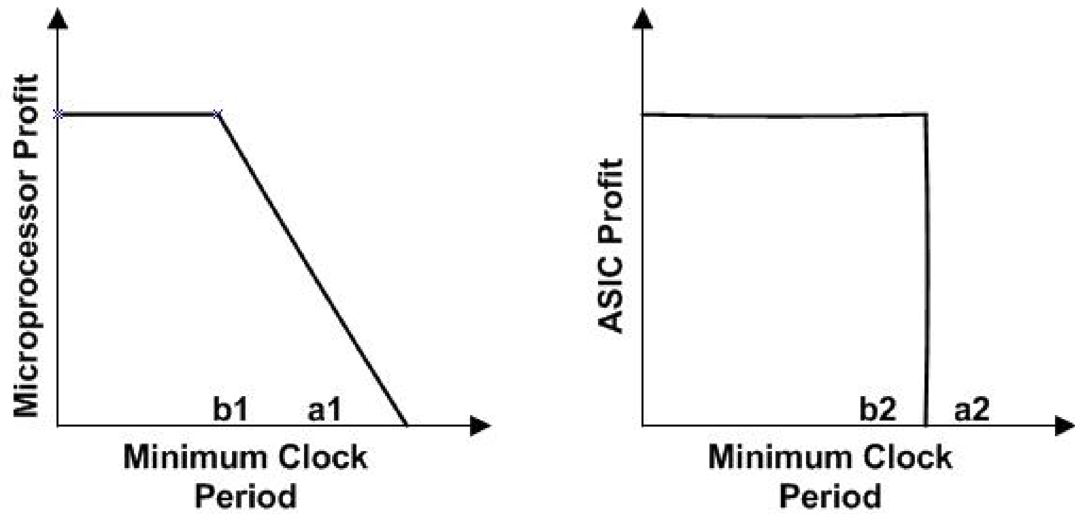

Figure 1.5: Microprocessors vs ASIC profit

in modeling of random process variations, including the Response Surface Methodology, Design of Experiments, Predictive Technology Models and Well Proximity Effect modeling and netlisting. Chapter 4 illustrates the entire design flow with the help of an example and the implementation details. Chapter 5 deals with some more examples and results. Finally, in Chapter 6, we conclude the thesis and point out future directions for research and enhancement.

Chapter 2

Overview

2.1 Process Variations

Semiconductor process variation occurs when process parameters deviate from their ideal, as-designed values. Due to these process variations, the electrical properties of the tranistors varies. As technology scales, the importance of understanding the effects of process variations on circuit performance is increasing further.

2.1.1 Sources of Variations

Process Variation can be classified into [18]

- Temporal Variations are time varying and change depending on circuit operating conditions like switching activity and temperature variation. Aging-induced variation has a negative impact on performance.
- Spatial Variation are fixed in time and depend on physical factors such as structural variation in the chip that is based on the circuit layout, neighboring environment, and process conditions.

Spatial Variation in turn can be classified into inter-die variations and intra-die variations. Inter-die variations are caused by lot-to-lot, wafer-to-wafer or across-wafer process variations. Intra-die variations occur between multiple devices on the same die. Intra-die variation can be further classified into random and systematic variations.

Random Variations

Random variations are caused by atomic-level differences between devices even though the devices may have identical layout geometry and environment. Some of examples for these variations are dopant profiles, film thickness variation, and line-edge roughness. Variation in the threshold voltage V_{th} is observed due to placement of random number of dopants in the channel during manufacturing steps of implant and annealing processes [18]. This phenomenon is called Random Dopant Fluctuation and is one of the variations that will be considered in this study. The other random variations considered are gate oxide thickness T_{ox} and channel length L_e.

Systematic Variations

Systematic Variations implies spatial correlation between devices. The electrical parameters of the device vary depending on the placement of a device relative to its neighbors. These variations have a well-understood relationship between design instances or layouts and the resulting electrical parameter values. They are predictable that can be modeled and the values are maintained across all corners/distributions. Some of the systematic layout dependent proximty effects are

- Well Proximity Effect
- Stress Proximity Effect
- Optical Proximity Effect
- CMP Proximity Effect

Well Proximity Effect is the systematic variation considered for this study and is explained in detail in Section 3.3.

2.1.2 From Process and Layout to Device I-V

Fig. 2.1 summarizes how process and layout affect the device behaviour. The manufacturing process involves many steps and technology like Lithography, Etching, Implantation, Annealing, Oxide Growth, Chemical Mechanical Polis (CMP) and so on. The layouts follow a style accordng to functionality specification. These are the variables where in variation might take place. The physical properties affected due these variations are -

Stress Field, Dopant field and 3D structure. These physical properties inturn affect the device parameters like mobility, threshold voltage, gate oxide thickness and critical dimensions of the transistor. The variation in device parameters has an affect on the electrical behaviour of the transistor like the drain current in linear and saturation regions, leakage current.

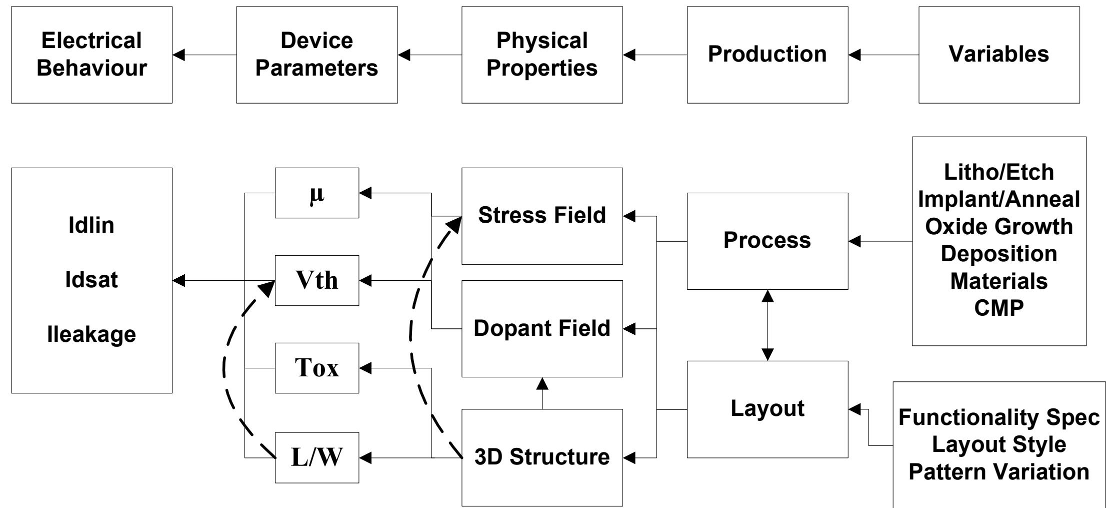

Figure 2.1: From Process and Layout to Device I-V [24]

2.2 Handling Process Variations

There are three classes of techniques proposed to ensure/enhance yield under variations while incurring minimal impact on design overhead [11]

- Statistical Design approach
  In this technique, a circuit performance parameter is modeled as statistical distribution and the circuit is designed to meet a constraint on yield with respect to a target value of the parameter.

- Post-Silicon compensation and correction
  In this technique, after manufacturing, if a shift in parameter is detected, it is compen-

sated/corrected by changing operating parameters such as supply voltage, frequency or body bias.

- Variation avoidance
  A given circuit is synthesized in such a way that the delay failures due to variations can be indentified in run time and avoided by adaptively switching to two cycle operation.

Given the broad levels of handling process variations, we are interested in pre-fabrication,design time technique of Statistical Design that could potentially reduce the effect of variations. Along with the statistical design approach, systematic layout dependent Well Proximity Effect (WPE) which leads to a fixed variation depending on that particular layout is also handled

2.2.1 Statistical Design vs Corner Case Design Methodology

In the conventional static analysis design flow, worst-case or best-case corner values of all the factors of variations is used in simulation. In actual chips, the likelihood of all factors being at the corner cases is very low. Therefore, it leads to conservative analysis and over-design as it analyzes using excessive margins for perfomance parameter variations [4].

As one of the DFM potential solutions, Statistical Analysis estimates circuit delay and other circuit performances parameters by considering the variations in these parameters statistically.

In a probabilistic design framework, all the varying circuit parameters are modeled as random variables. These random variables may or may not be correlated to each other. At the lowest level, variations happen in the geometries of interconnects (e.g., length, width) and of transistors (e.g., effective channel length,oxide thickness), transistor doping (as well as other possibilities). These low-level factors are modeled as random variables . Given the variations of these low-level factors, one could model the effects of variations at higher levels by finding the Probability Density Function (PDF) of performance metrics of a design such as its frequency and power, as these performance metrics are ultimately a function of the low-level factors.

Under process variations the circuit delay could be modeled as a random variable described as a function of those random variables representing the varying factors of the transistor . These variation-aware models will then be used within an optimization framework in the context of different design techniques.

Statistical Static Timing Analysis, as explained in the next section, considers delay as the circuit performance parameter to be estimated.

2.3 Statistical Static Timing Analysis (SSTA)

In order to analyze circuit delay more accurately considering the random variations, SSTA defines the random variations of the delay as random variables and calulates the probability density funtions (PDF) of circuit delay [19]. A circuit is expressed by a graph that represents the gates and interconnects as nodes. Traversing the graph, the PDF of the delay in each of the node is calculated using the statistical sum and max operations with the delay variations of the gates and interconnects as inputs. Let us consider two inverter gates connected in series and a NAND gate, in which two input signals converge at the output pin of a gate. The two basic operations in SSTA is explained using these two circuits. The delay variation due to variation in interconnects is not considered in this study and is ignored.

2.3.1 Basic SSTA operations

- **sum** [19] - The delay of the two inverters connected in series is calculated using the statistical sum operation. Let us denote the delay PDF of each of these inverters as f_1 and f_2. Then the delay PDF at end point f is calculated as the statistical sum of f_1 and f_2. The statistical sum is calculated using convolution integration. However, if f_1 and f_2 have normal distributions, a simple formula can be used. Consider f_1 and f_2 have normal distributions with average m_1, m_2 and 3 sigma standard deviations s_1, s_2 respectively. Then f has a normal distribution with average of $m_1 + m_2$ and $\sqrt{s_1^2 + s_2^2}$.

- **max()** - Statistical max operation is used to find the output delay of the multiple-input gate as in a NAND gate. If f_1 and f_2 are independent of each other, an accurate solution can be obtained and is calculated as the upper bound of statistical max of $d1$ and $d2$. Conversely, if f_1 and f_2 correlate with each other, it is difficult to obtain an accurate solution of the statistical max operation and only an approximation is possible.

2.3.2 Path-based and block-based SSTA

In path-based SSTA [19], the delay of each path or say critical path is calculated individually, traversing from the source to the sink of the path. The advantage of this method is that it accurately calculates the delay PDF of each path delay because it does not use statistical max operations to analyze sequential paths. In block-based SSTA, all paths are analyzed simultaneously by traversing the graph, with the delay of the entire circuit being calculated at the end of the traversal. To reduce the processing time of SSTA, it is recommended to perform SSTA on the critical paths detected by the conventional Static Timing Analysis tool.

2.4 PDK

Process Design Kits (PDKs) provide the data files that are needed to design chips for a given process technology, using a supported set of EDA tools. PDKs include such things as schematic symbols, Spice models, parameterized cells, a layout technology file, design rule check (DRC) and layout-versus-schematic (LVS) deck, Parasitic Extraction Deck, standard cell/pad library and associated characterization files, framework to perform statistical circuit analysis and so on.

Existing PDKs cannot be used in the classroom due to tight intellectual property (IP) controls on them. Also, only fragmented PDKs are available to universities and modification, redistribution of existing PDKs are prohibited. The FreePDK45 is an effort to address these issues and its information may be freely used, modified, and distributed under the open-source Apache License [21] .

The PDK must have the ability to take into account the variations and help in robust design. It needs to become variation aware for reasons we have discussed before and this thesis work is aimed in that direction.

Chapter 3

Methodology

3.1 Modeling of Random Variations

Modeling is a essential component of statistical analysis framework. The models need to capture the effect of process variation. One way of building such models is to describe the circuit performance parameters as functions of random variables that represent variations. For example, the circuit delay can be modeled as a random variable described as a function of those random variables representing the varying transistor geometries. Response Surface Methodolgy along with Design of Experiments is used to build these models. These variation aware models can be further used in optimization framework. The theory behind the modeling is explained in the following two sections.

3.1.1 Response Surface Methodology (RSM)

RSM can be defined as a collection of statistical and mathematical techniques useful for developing, improving, and optimizing processes. The most extensive use of RSM can be found in situations where several input variables influence some performance measure, called the response, in a way that is difficult or impossible to describe with a rigorous mathematical formulation. In these situations it might be possible to derive an expression for the performance measure based on the response values obtained from experiments at some particular combination of the input variables. The expression of the performance measure obtained through experiments is called response surface [23]

The complete circuit's performance parameters will be modeled in terms of per-

formance variables of simpler blocks constituting the circuit. Due to this the computational effort is greatly reduced because circuits consists normally of only a limited number of distinctly behaving primitives and only one representative of every such primitive needs to be analyzed.

For each of the above described 'primitive', the following quantities are defined and will be used for modeling the performance parameter of the entire circuit.

Factors - are processing conditions or input variables whose values can be controlled by the experimenter - at least for purposes of a test or an experiment/simulation. Presumably, if one of the factors changes then response variable varies. In this work, V_{th}, L_{eff} and T_{ox} will be taken as factors and its range of values, its variation from its nominal value will be considered.

Response-

$Y = \eta + \epsilon$

Y - is the response variable and is the observed value from the output of the simulation of the circuit. The response variables value is affected due to change in the levels of the factors. True value of the response is denoted by the variable η. The observed response is sum of the true response and Experimental error denoted by ϵ. If the model is an inadequate representation of the true response, then this error ϵ will also contain a non-random error called lack of fit error and is due to the absence of higher degree terms. This lack of fit error must be minimized. The response variable can be circuit performace parameter like delay, power and so on.

Response Function-

$\eta = \varphi\left((X_1, X_2, X_3, X_4 \ldots X_k)\right)$

The relation between the various factors and the response can be represented by a function which is called Response Function η

Response Surface The response function

$\eta = \varphi\left((X_1, X_2, X_3, X_4 \ldots X_k)\right)$

can be represented by a surface. With K factors, the response surface is a subset of (K+1) - dimensional Euclidean Space.

This is just an introduction to RSM and the actual steps involved in building these models is explained in great detail in Section 4.2 .

3.1.2 Design of Experiments (DoE)

To build the response surface and the model, we need to run the experiments at some values of the factors and the response obtained from this is used in building the model. The values of the factors are called the sampling points and are calculated using the thoery of Design of Experiments. The points chosen using the DoE theory ensures that the entire design space is covered and the best possible precision of the form of the response surface. Some of the widely used sampling methods are given below [20]. In this work, Full-factorial is used as it provides a uniform grid with user-specified density covering the input factors space. Also, other DoE can be experimented with.

- Nominal Design is the simplest one which uses nominal values of all the inputs factors.
- Center point design is similar to Nominal design but uses the midpoint values of all the input factors.
- Axial Design includes center points, and points at the minimum and maximum of each input factor while holding other inputs to their nominal values.
- Box-Wilson design includes the center point, axial points and corner points distributed around a n-dimensional sphere circumscribing the cuboid defined by the input minima and maxima of the factors.
- Box-Wilson (inscribed) modifies the Box-Wilson design by distributing axial and corner points on an n-dimensional sphere inscribed within the cuboid.
- Box-Wilson on a cube stretches the corner points to lie on the cuboid corners to achieve more complete coverage of the input factors space.
- Full-factorial design produces a uniform grid with user-specified density covering the input factors space.
- Latin hypercube sampling provides an orthogonal array that randomly samples the entire design space broken into r^n equal-probability regions (where r is the number of runs and n is the number of input variables.

3.2 Predictive Technology Models (PTM)

PTM provides accurate, customizable, and predictive model files for future transistor and interconnect technologies [1]. These predictive model files are compatible with standard circuit simulators, such as SPICE, and scalable with a wide range of process variations. With PTM, competitive circuit design and research can start even before the advanced semiconductor technology is fully developed. As an evolution of previous Berkeley Predictive Technology Model (BPTM), PTM provides the following novel features for robust design exploration toward the 10nm regime:

- Predictions of various transistor structures, such as bulk, FinFET (double-gate) and ultra-thin-body SOI, for sub-45nm technology nodes.
- New methodology of prediction, which is more physical, scalable, and continuous over technology generations.
- Predictive models for emerging variability and reliability issues, such as NBTI.

These PTM transistor models at 45nm technology node are used in this work. The source code to generate PTM models is available.

3.3 Well Proximity Effects (WPE)

In this section, we will discuss in depth about the origin of WPE, its physical understanding, modeling WPE as a function of layout, extraction of instance parameters and its inclusion in the PTM models

MOSFETs are formed during the front-end of fabrication process, which mainly consists of MOSFET wells, shallow trench isolation(STI), and MOSFET gate formations. During implants of the n-type transistors, the p-type transistors are covered by photoresist and vice-versa. As seen in Fig 3.1, when a transistor is located near the edge of the photoresist, the high-energy ions can scatter from the photoresist edge and introduce extra dopant atoms in the silicon near the well edge [13]. Due to this phenomenon, the threshold voltage of the transistor can vary depending on the location and shape of adjacent wells [14]. As the MOSFET gate approaches the well edge, the dopant concentration of the MOSFETS core area will increase, causing a increase in the threshold voltage [12].

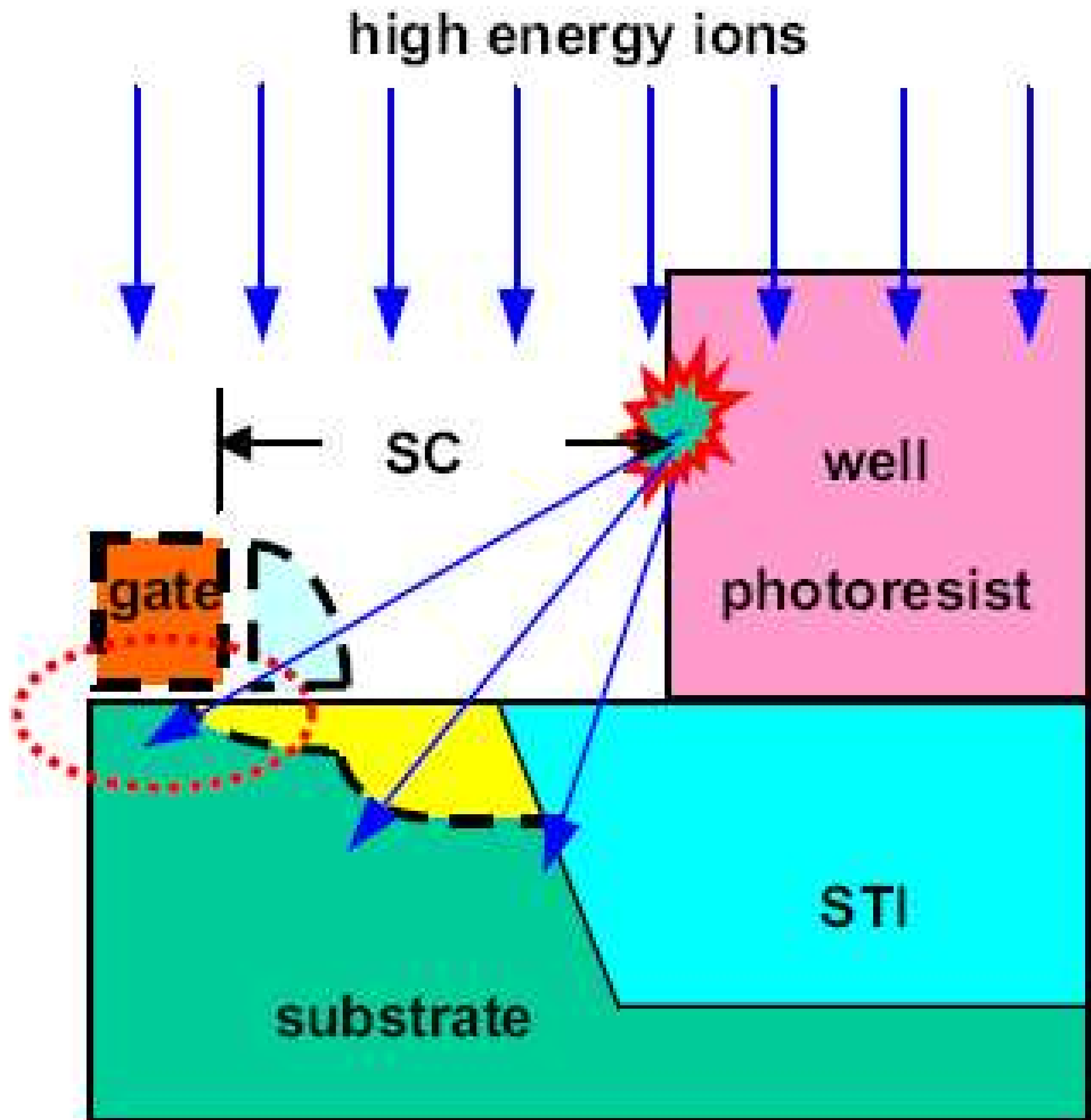

Figure 3.1: The origin of well edge proximity effect [12]

3.3.1 Netlisting and Modeling WPE

Let us assume some FETs placed at the same distance from the well edge. However, because of the shape and orientation of the FETs, each will receive a different dose and a different shift in threshold voltage. The total effect is thus calculated by averaging the dose

over the area of FET as

$$Z = \frac{1}{WL} \int\int f\left(d\left(x,y\right)\right) dx \cdot dy \tag{3.1}$$

where $f\left(d\right)$ is the modeling function that determines the additional dose due to a long edge as a function of the distance from the edge [6].

Edges that have a direct line of sight to a given FET is only considered to affect that FET as ions scattered by other edges will be stopped by any region of photoresist between the scattering edge and FET.

For the case of a FET near a single long well edge, the integral in Eqn 3.1 becomes a one-dimensional integral and for multiple well edges that effect the same device, it is assumed that the combined effect is simply the sum of separate effects.

If the well edge is not a single straight edge but contains a jog, then Eqn 3.2 is approximated by dividing the FET active area into and applying the formula twice.

$$Z = \frac{1}{WL} \sum_i W_i \int_{d_i}^{d_i+L} f\left(u\right) du \tag{3.2}$$

In a general case, there can be multiple scattering edges parallel to any or all four sides of the FET active area and the expression becomes

$$Z = \frac{1}{WL} \left(\sum_i W_i \int_{d_i}^{d_i+L} f\left(u\right) du + \sum_i L_i \int_{d_i}^{d_i+W} f\left(u\right) du \right) \tag{3.3}$$

The below set of functions are used to represent $f\left(d\right)$

$$f_A\left(d\right) = \frac{1}{d^2} \tag{3.4}$$

$$f_B\left(d\right) = d\, exp\left(-10d\right)$$

$$f_C\left(d\right) = d\, exp\left(-20d\right)$$

The new equations for threshold voltage, mobility and the body effect considering the well proximity effect can be described as

$$Vth0 = Vth0_{org} + KVTH0WE \cdot \left(SCA + WEB \cdot SCB + WEC \cdot SCC\right) \tag{3.5}$$

$$K2 = K2_{org} + K2WE \cdot \left(SCA + WEB \cdot SCB + WEC \cdot SCC\right) \tag{3.6}$$

$$\mu_{eff} = \mu_{eff,org} \cdot \left(1 + KU0WE \cdot \left(SCA + WEB \cdot SCB + WEC \cdot SCC\right)\right) \tag{3.7}$$

where in, $Vth0_{org}$, $K2_{org}$, $\mu_{eff,org}$ are the original values of threshold voltage, body effect and mobility respectively. $KVTH0WE$, $K2WE$ and $KU0WE$ are the curve

fitting parameters. SCA, SCB and SCC are instance parameters that represent the first/second/third distribution functions for scattered well dopants. For relatively large distances, the effect falls off roughly as the distance squared, as modeled by the SCA term. For technologies whose design rules do not allow well edges close to an active area, only SCA is needed and WEB and WEC may be set to zero else they need to be set to one [5].

The integral forms for the instance parameters are

$$\begin{aligned} SCA = & \frac{1}{W_{drawn} \cdot L_{drawn}} \cdot \sum_{i=1}^{n} \left(W_i \cdot \int_{SC_i}^{SC_i + L_{drawn}} f_A(u)\, du \right) + \\ & \sum_{i=n+1}^{n+m} \left(L_i \cdot \int_{SC_i}^{SC_i + W_{drawn}} f_A(u)\, du \right) + corners_A \\ f_A(u) = & \frac{SC_{ref}^2}{u^2} \end{aligned} \tag{3.8}$$

$$\begin{aligned} SCB = & \frac{1}{W_{drawn} \cdot L_{drawn}} \cdot \sum_{i=1}^{n} \left(W_i \cdot \int_{SC_i}^{SC_i + L_{drawn}} f_B(u)\, du \right) + \\ & \sum_{i=n+1}^{n+m} \left(L_i \cdot \int_{SC_i}^{SC_i + W_{drawn}} f_B(u)\, du \right) + corners_B \\ f_B(u) = & \frac{u}{SC_{ref}} exp\left(-10 \cdot \frac{u}{SC_{ref}} \right) \end{aligned} \tag{3.9}$$

$$\begin{aligned} SCC = & \frac{1}{W_{drawn} \cdot L_{drawn}} \cdot \sum_{i=1}^{n} \left(W_i \cdot \int_{SC_i}^{SC_i + L_{drawn}} f_C(u)\, du \right) + \\ & \sum_{i=n+1}^{n+m} \left(L_i \cdot \int_{SC_i}^{SC_i + W_{drawn}} f_C(u)\, du \right) + corners_C \\ f_C(u) = & \frac{u}{SC_{ref}} exp\left(-20 \cdot \frac{u}{SC_{ref}} \right) \end{aligned} \tag{3.10}$$

In the above equations, SC_{ref} is SC_{max}, the maximun search distance beyond which the WPE is not significant and thus not used in the calculation of instane parameters. These equations are derived from Eqn 3.2 by substituting the functions in Eqn 3.4. **n** is the number of projections of the well edge along the width of the devices for which SC (the distance between gate edge and well edge) is constant. **m** is the number of projections of the well edge along the length of the devices for which SC (the distance between gate edge and well edge) is constant and the count for this starts from n+1 and not 1.

The closed form solutions for the instance parameters obtained from sloving the integral forms are

$$SCA = \frac{1}{W_{drawn} \cdot L_{drawn}} SC_{ref}^2 \sum_{i=1}^{n} \left(W_i \left(\frac{1}{SC_i} - \frac{i}{SC_i + L_{drawn}} \right) \right) + SC_{ref}^2 \sum_{i=n+1}^{n+m} \left(L_i \left(\frac{1}{SC_i} - \frac{i}{SC_i + W_{drawn}} \right) \right) + corners_A \quad (3.11)$$

$$\begin{aligned} SCB = \frac{1}{W_{drawn} \cdot L_{drawn}} \cdot & \sum_{i=1}^{n} W_i \left(\frac{SC_i}{10} + \frac{SC_{ref}}{100} \right) exp\left(-10 \frac{SC_i}{SC_{ref}} \right) - \\ & \left(\frac{SC_i + L_{drawn}}{10} + \frac{SC_{ref}}{100} \right) exp\left(-10 \frac{SC_i + L_{drawn}}{SC_{ref}} \right) + \\ & \sum_{i=1}^{n} L_i \left(\frac{SC_i}{10} + \frac{SC_{ref}}{100} \right) exp\left(-10 \frac{SC_i}{SC_{ref}} \right) - \\ & \left(\frac{SC_i + W_{drawn}}{10} + \frac{SC_{ref}}{100} \right) exp\left(-10 \frac{SC_i + W_{drawn}}{SC_{ref}} \right) + \\ & corners_B \end{aligned}$$

$$\begin{aligned} SCC = \frac{1}{W_{drawn} \cdot L_{drawn}} \cdot & \sum_{i=1}^{n} W_i \left(\frac{SC_i}{20} + \frac{SC_{ref}}{400} \right) exp\left(-20 \frac{SC_i}{SC_{ref}} \right) - \\ & \left(\frac{SC_i + L_{drawn}}{20} + \frac{SC_{ref}}{400} \right) exp\left(-20 \frac{SC_i + L_{drawn}}{SC_{ref}} \right) + \\ & \sum_{i=1}^{n} L_i \left(\frac{SC_i}{20} + \frac{SC_{ref}}{400} \right) exp\left(-20 \frac{SC_i}{SC_{ref}} \right) - \\ & \left(\frac{SC_i + W_{drawn}}{20} + \frac{SC_{ref}}{400} \right) exp\left(-20 \frac{SC_i + W_{drawn}}{SC_{ref}} \right) + \\ & corners_C \end{aligned}$$

Let us understand the extracion of these instance parameters from the layout using a typical layout of the MOSFET as shown in Fig. 3.2 with an irregularly shaped well to cover all the aspects of the formula. For each FET in the layout, the LVS tool needs to identify all the well-edges that will affect that FET. The WPE drops off rapidly as the distance fron the edge to the device channel region increases. So a maximum search distance called S_{max} is used so that any edge outside of S_{max} is ignored during calculations. So for the given layout, only the following pairs of SC and W will be used - (SC1,W1) (SC5,L5) (SC3,W3) and (SC7,L7)

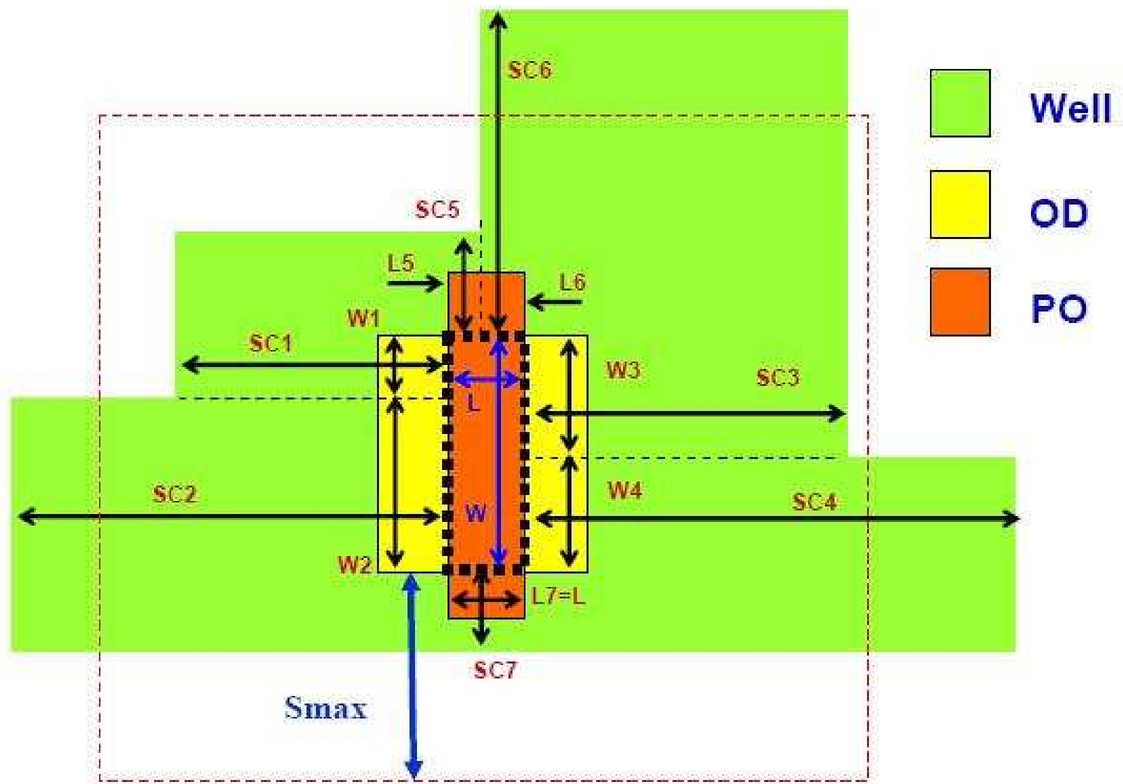

Figure 3.2: Typical MOSFET layout showing WPE parameters and maximum search distance [5]

3.3.2 Development of LVS rules

Measurement of SC_i, W_i and L_i is done by extending the Property Function of a transistor in the Calibre LVS rule deck. There are special commands in Calibre's Standard Verification Rule Format to obtain these measurements. Once these measurements are done, then computation of instance parameters SCA, SCB and SCC is done using Tcl Verification Format.

3.3.3 DELVTO and MULU0 instance parameters

Once the change in V_{th}, Body effect and Mobility is calculated using the instance parameters and fitting parameters, this information needs to be passed on the BSIM/PTM transistor models. For this purpose, new instance parameters DELVTO and MULU0 have been introduced in version 4.6 of BSIM models for V_{th} and mobility respectively. There

is no instance parameter for body effect. Therefore, unless a new transistor model-type is developed, variations in the body effect must be simulated by declaration of a new transistor model (for example, a .MODEL statement in SPICE).

Chapter 4

Design Flow

4.1 Introduction

The overall flow of modeling using RSM/DoE is given in Fig. 4.1. The steps involved is discussed in detail in the following sections.

4.2 Modeling

To perform the DOE and RSM, we will use the Taurus Workbench from Synopsys. On the NCSU Unity computer system, Taurus workbench is setup by the following command
% *add synopsys_tcad*
We need to start taurus workbench with -use_dfm option to use the RSM feature as follows.
% *twb -use_dfm* &
The first window that appears is called the Workspace [Fig. 4.2].
Create a new project by selecting **Project->New**. Projects are shown as columns. Each project has a library (a cell with the book icon) and a list of experiments. Each library also contains simulation components(Modules/Tools/Drivers) for reuse in other projects. An experiment consists of a Process Recipe, a Wafer Flow, and all the associated simulation data. Access to a given project is indicated by the book icon; if a pencil is on the book,you have write-access, otherwise, theproject is read-only. In the initial Workspace window you see three read-only projects: templates,standard and dfm_work.
(The project can be renamed by right-clicking on the library and Edit name)
Once you create a new project, you can copy experiments from the read-only libraries. To

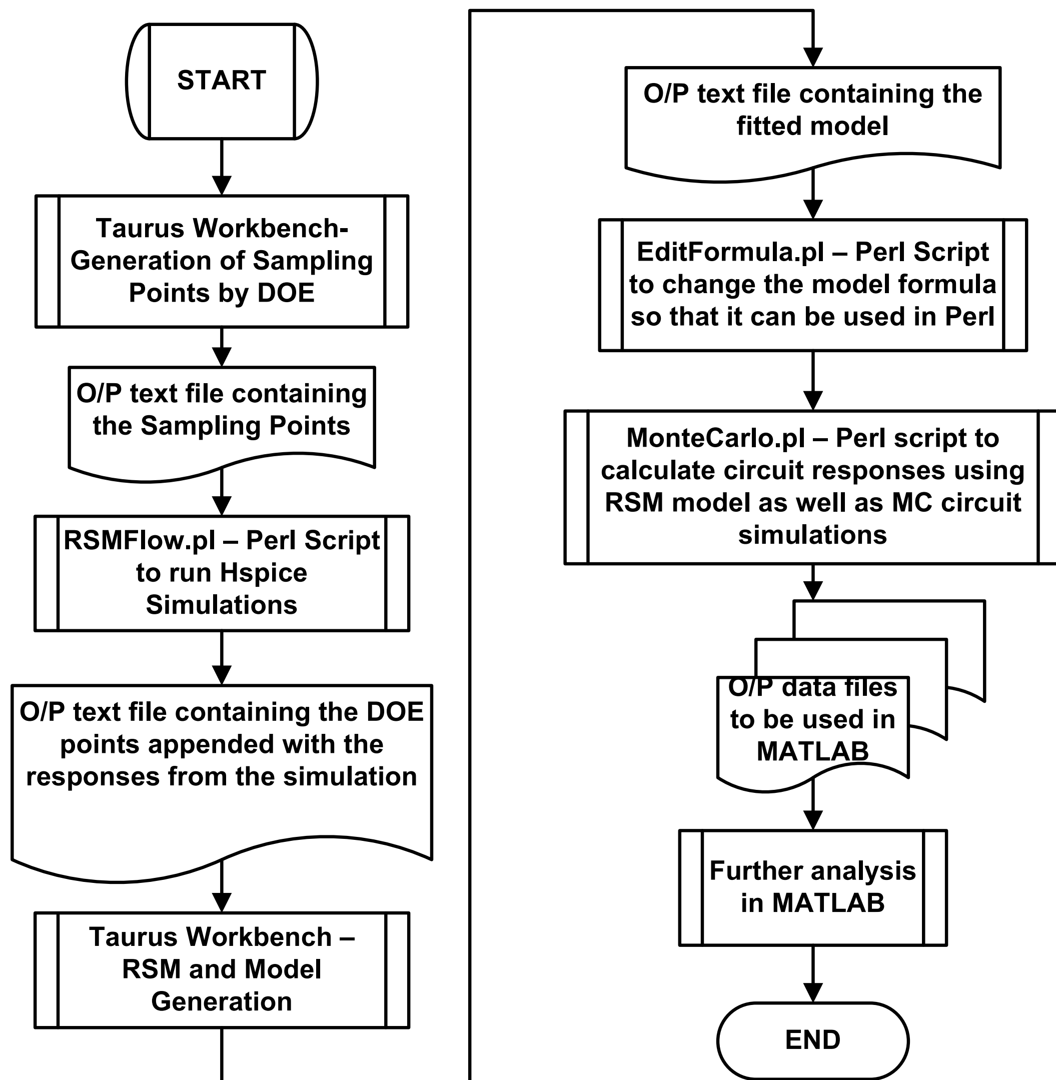

Figure 4.1: Over all flow for modeling using RSM/DoE

do this:

1. Select a cell with an experiment's name by clicking on it.

2. Drag and drop it into your project.

A warning notice offers a choice of Deep or Shallow copy. Do a Shallow copy of the library hspice_baseline from dfm_work project and rename it. We will be using this experiment as

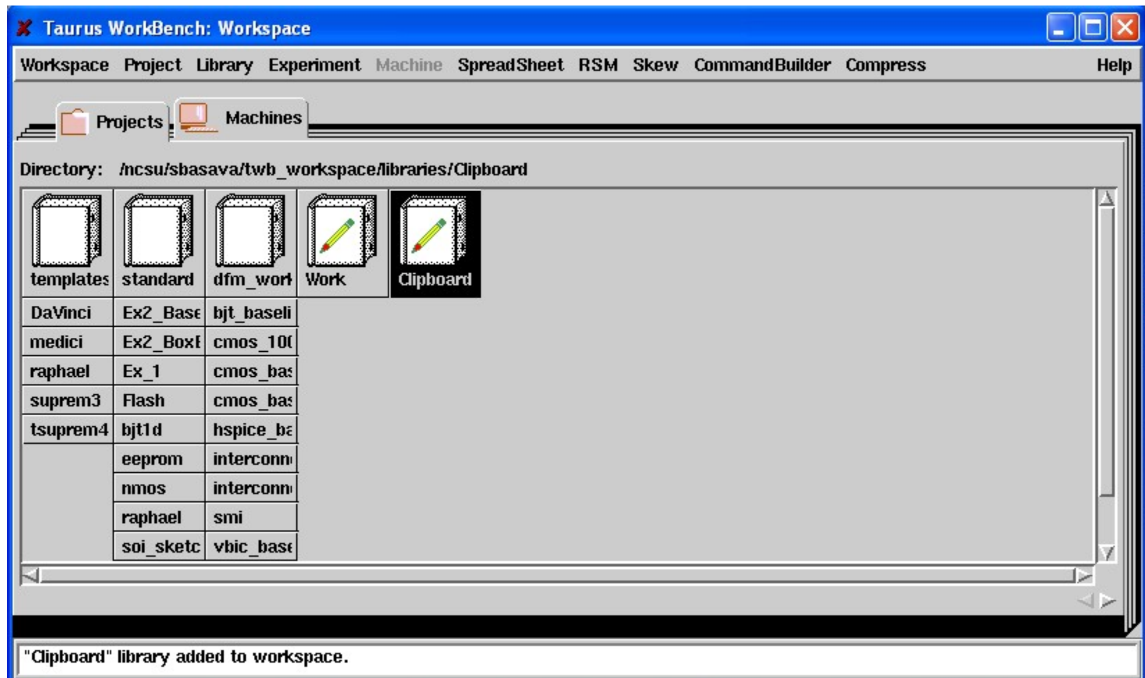

Figure 4.2: Workspace Window

our starting point and editing it to our requirements. To edit the newly created experiment **Expt1**, double-click the cell containing the experiment name. An experiment window opens, as shown in figure 4.3. To view the contents of a module "hspice_test", double-click the module object (hspice_test). A Module editor opens. We can delete the inbuilt Command "circuit" by selecting the particular cell and **Command->Cut**. Lets create a new command called "RSM" by **Command->New->Append**. You will get the following warning saying "Saving changes to this module means destroying already completered wafers. Do you want to destroy the modules wafers". Choose "Destroy".

Lets consider an example of a two stage, two input Standard Cell Inverter (INVX1). The setup allows us to analyze the effects of process variations considering each of the transistors in the circuit suffer different variations. The parameters that are currently supported whose variation effects can studied are L_{eff}, T_{ox} and V_{th}.

In this example, V_{th} is assumed to vary by +/-10% of the nominal value. So we need to carry out DoE for 4 parameters of V_{th} (one for each of the transistors). This is done by **Parameter->New->Append** and enter the corresponding values in each window as

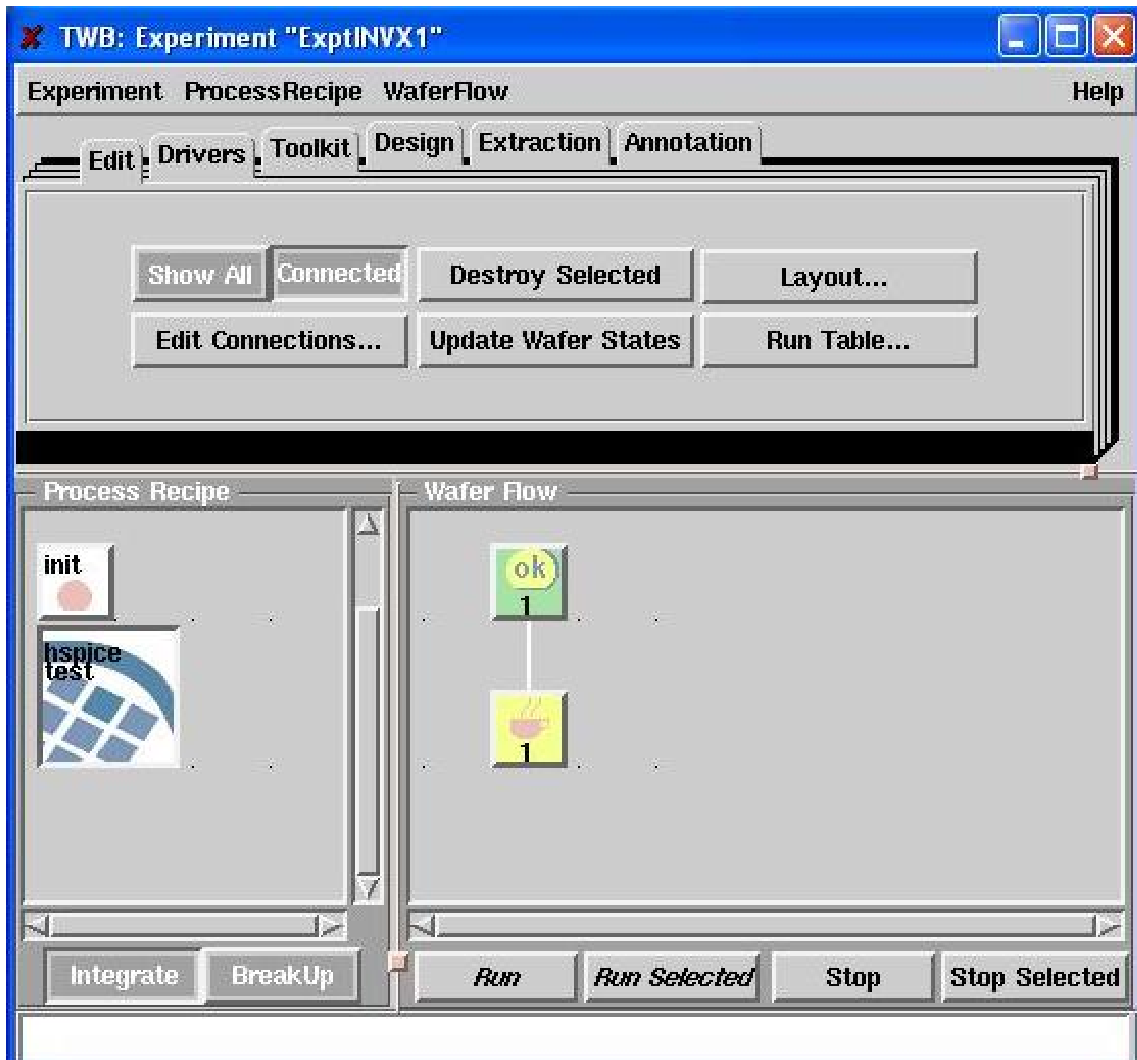

Figure 4.3: Experiment Window

shown in Fig.4.4

1. The parameter name (Vth1, Vth2,.. Leff1, Leff2.. and Tox1, Tox2,.. so on) and nominal value of the parameter (separated by an = sign).

2. The Parameter label, which is used to reference a parameter value (% followed by parameter name).

3. The Min/Max fields - values depending on the percentage of variations.

4. A Control checkbox to designate a control parameter (Check this so that this parameter can be accessed in DoE).

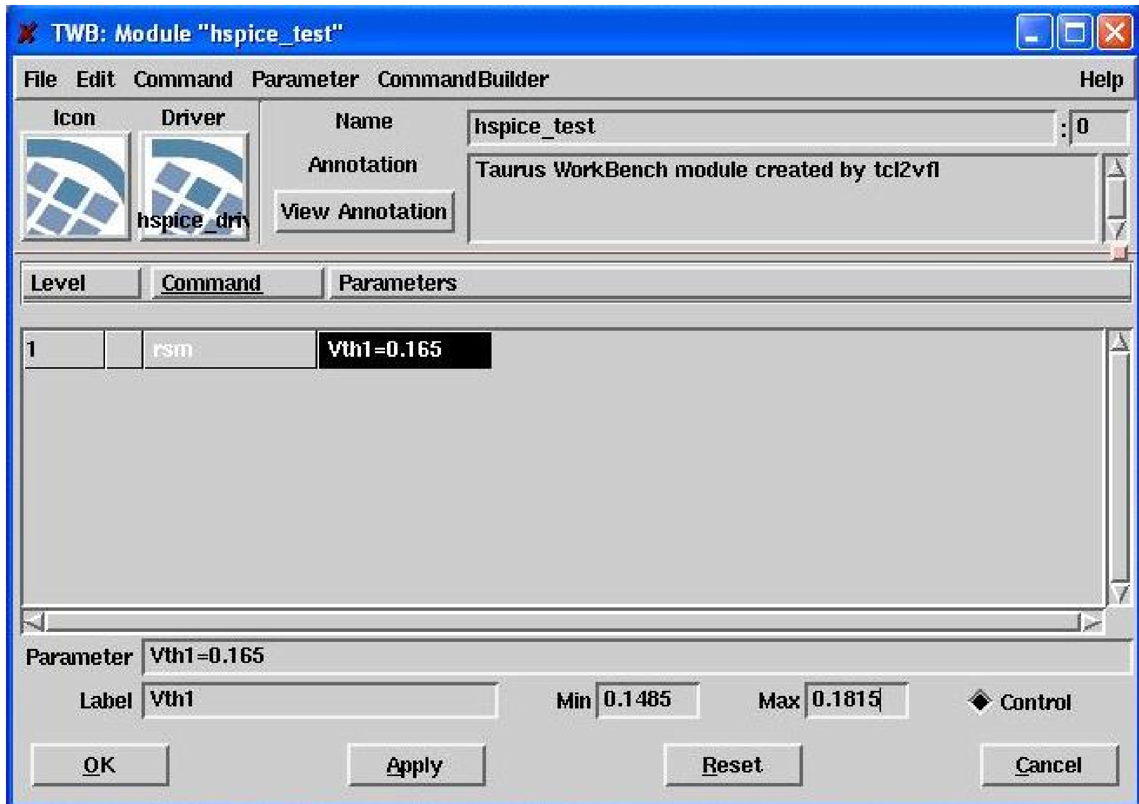

Figure 4.4: Module Parameter Window

We can similarly add other parameters Vth2-Vth4.

The variations, delays, other circuit perfomance parameters and results of statistical operations are modeled as Gaussian random variables. A definition of a Gaussian random variable and its probability density function (PDF) is given in Eqn. 4.1 and 4.2 respectively.

$$X = N\left(\mu, \sigma^2\right) \tag{4.1}$$

$$f\left(x; \sigma, \mu\right) = \frac{1}{\sigma\sqrt{2\Pi}} exp\left[-\frac{\left(x-\mu\right)^2}{2\sigma^2}\right] \tag{4.2}$$

Also, we need to add a parameter for response (for ex - delay, power). Multiple responses can also be entered. The min/max value can be 0/1 as it does not matter and do check the

control checkbox for this parameter also. Let's add three responses - tdelayLH, tdelayHL and tdelay.

In the Experiment window, click on the "Run Table..." under the "Edit" tab. The following window opens as in Fig.4.5 and the rest of the procedure is done from this window. To

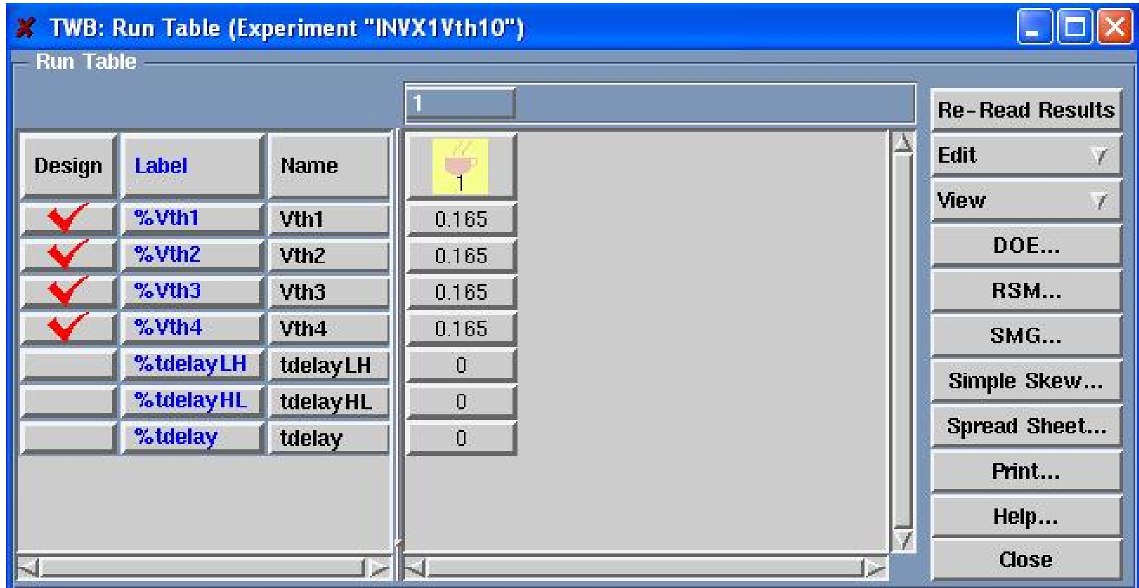

Figure 4.5: Run Table

perform DoE click on the "DOE..." tab and make sure you have ticked all the parameters required for DoE under the "Design" column as shown in Fig.4.5 (NOTE - Do not check the responses, tdelayLH and tdelayHL in this case). A new DoE window opens as shown in Fig.4.6 You can select the required DOE, change the levels and say "Build Design". You might get a warning regarding change in Build Method, proceed to say yes. Once the design is built, you will get a message "New Design has been built" and the sampling points generated from this DOE can be accessed by clicking on the "Spread Sheet..." in the Experiment window. Now check the responses also so that it gets reflected in the spread sheet as shown in Fig4.7. Save this file as .txt by **File->Save** The responses from the simulations using these values as inputs, will be appended to this spreadsheet and used to build the model.

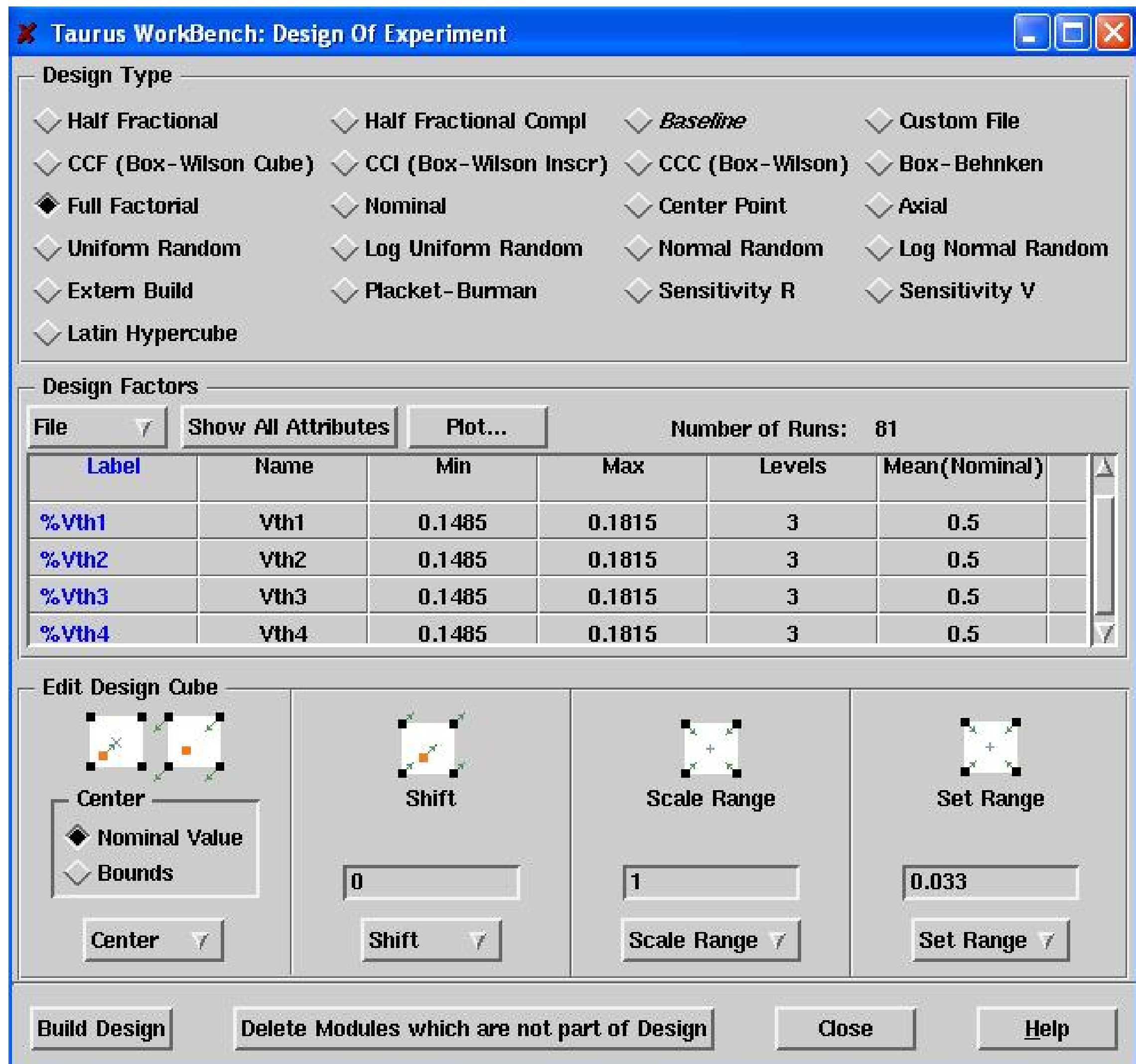

Figure 4.6: Design Of Experiment

4.2.1 RSMFlow.pl

A automation script, RSMFlow.pl is used to do the following

- To use each set of values in the DoE file as inputs to create different PTM models.
- Use these PTM models to simulate a netlist of a circuit using hspice.
- To capture the response of the circuit in every simulation run and to update the response of DoE spreadsheet so that it can be used to build the model

TWB: SpreadSheet0

File Rows Columns Statistics RSM Export Filter Options Skew Help

Spread Sheet

Experiment: INVX1Vth10 CellType: Name

SubWafer	%Vth1	%Vth2	%Vth3	%Vth4	%tdelayL	%tdelayH	%tdelay
SubWafer	%Vth1	%Vth2	%Vth3	%Vth4	%tdelayL	%tdelayH	%tdelay
#	Vth1	Vth2	Vth3	Vth4	tdelayLH	tdelayHL	tdelay
0	0.1485	0.1485	0.1485	0.1485	0	0	0
0	0.1815	0.1815	0.1815	0.1815	1	1	1
1.0	0.1485	0.1485	0.1485	0.1485	0	0	0
2.0	0.165	0.1485	0.1485	0.1485	0	0	0
3.0	0.1815	0.1485	0.1485	0.1485	0	0	0
4.0	0.1485	0.165	0.1485	0.1485	0	0	0
5.0	0.165	0.165	0.1485	0.1485	0	0	0
6.0	0.1815	0.165	0.1485	0.1485	0	0	0
7.0	0.1485	0.1815	0.1485	0.1485	0	0	0
8.0	0.165	0.1815	0.1485	0.1485	0	0	0
9.0	0.1815	0.1815	0.1485	0.1485	0	0	0
10.0	0.1485	0.1485	0.165	0.1485	0	0	0

Figure 4.7: Spreadsheet

To use the RSMFlow.pl script, the following must be present in the current working directory

- Automation script - RSMFlow.pl
- Netlist of the circuit - .sp file
- DOE file generated by Taurus Workbench - .txt file
- PTM directory - Create a directory by name “PTM” (should have the two files called NMOS_last PMOS_last) and a sub-directory called “doc”. With in this doc directory, the created PTM models are stored.

Makesure you do "add hspice" in the terminal window before you run RSMFlow.pl.
Usage of RSMFlow.pl
perl RSMFlow.pl -help
Will show the help for this flow as
NOTE: Makesure you do " add hspice " in the terminal window before you run RSMFlow.pl
To run this flow,the inputs needed are:

- The Hspice Netlist file (-netlist)
- The DoE File (-doe)
- The Design Factors can be Vth, Leff, Tox. If any of the factors is not used, its value must be zero,else should indicate the order it is present in the DOE spreadsheet
- The number of responses in the Experiment (-res)
- If the factors is assumed to vary by the same amount for all tranistors in the netlist then set (-multi) to 0, otherwise 1
- The Name of the output DoE file with the responses appended (-output)

Ex: " perl RSMFlow.pl -netlist INVX1.sp -doe INVX1DOE.txt -vth 1 -leff 0 -tox 0 -res 2 -multi 1 -output INVX1DOERes.txt

The following is a brief explanation of the inputs to the RSMFlow.pl and its working.

- The hspice netlist file which needs to be simulated is given as input using the -netlist option and the DOE file with -doe option. In this example, since only Vth is being used,value of option -vth is 1 and -leff,-tox are 0. If Vth and Tox were varied in this experiment and if Vth was entered first in the module window and then Tox, then the options would be -vth 1 -leff 0 -tox 1.
- The use of option -multi is as follows - If there is a need to experiment such that all the tranistors in the circuit suffer the same process variations, then we can set -multi to 0 else its value must be 1.
- A copy of the original netlist is modified by replacing NMOS_VTL by NMOS_VTL_0, next occurence of NMOS_VTL as NMOS_VTL_1 and so on. Similarly replacing

PMOS_VTL by PMOS_VTL_0, next occurence of PMOS_VTL as PMOS_VTL_1 and so on.

- Also, if the instance parameter K2 from the Systematic Variations effect (by using the netlist obtained from layout extraction using Well Proximity effects) is present in the netlist, then its value is stored to be used while generating the PTM models. K2 and its value is removed from the netlist.

- It creates a hspice.include file which is included in the hspice netlist and points to transistor models (depending on the number of transistors in the netlist) going to be used in simulations.

- The parameter values from the DOE file is used to generate transistor models. In this case, 4 PTM transistors models are generated and a hspice simulation is done. Another set of 4 PTM transistors models are generated and a hspice simulation is done. This is repeated N number of times depending on the sampling points in DOE. For each of the simulation, the response is got from the .mt0 files and updated in the output DOE file. The INVX1DOERes.txt is the resultant file with responses appended.

INVX1DOERes.txt needs to be opened from spreadsheet window by **File->Load**. Once this file is loaded, click on the "RSM..." from the spreadsheet and RSM window opens as in Fig.4.8. Delays - tdelayHL, tdelayLH and tdelay which are the response can selected and moved from Factors to Responses as shown. Also delete the control factor "SubWafer". This factor is present by default and if not removed, the models cannot be fitted properly. The overall strategy for RSM is shown in Fig. 4.9

The statistics of the factors and responses can be seen under the statistics tab. Orders for the models can bet set in the orders tab. You can choose the model type and assing all the factors the same order or assign the order individually. X-order refers to interaction order between factors. Then click on the "Fit Models". The model will be fitted and added under the "Polynomial Models". Select a model and click on the "Open" tab. The poynomial window opens (Fig. 4.10and the measure of fit for the model can be studied.

Taurus Workbench uses four statistics to measure the quality of an RSM model:

1. Residual RMS (Residual Root Mean Square Error)

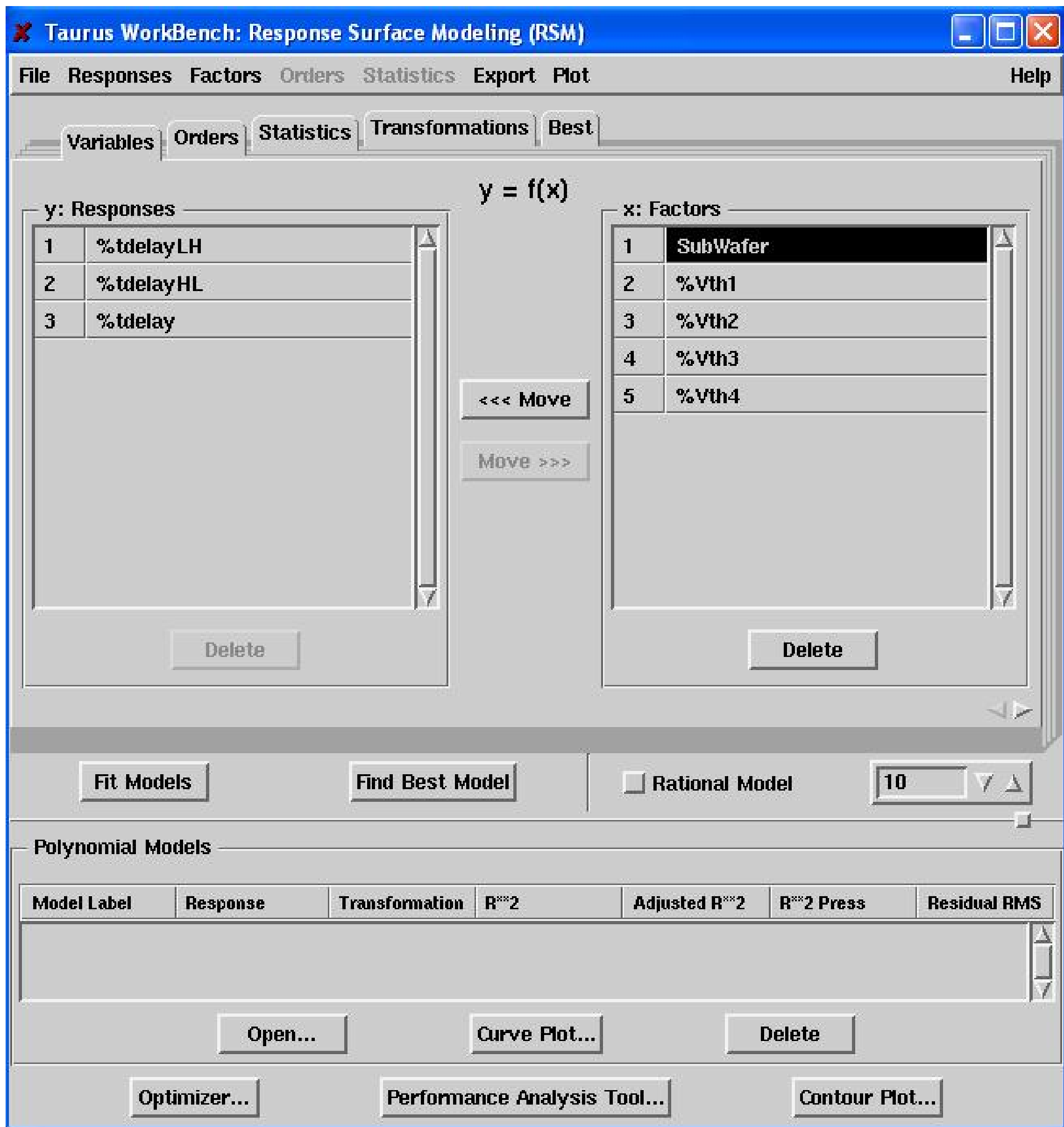

Figure 4.8: Response Surface Modeling

2. R^2 (multiple coefficient of determination or R-Square)

3. $\bar{R}^2$(adjusted multiple coefficient of determination or adjusted)

4. R^2_{press} (predictive residual sum of squares)

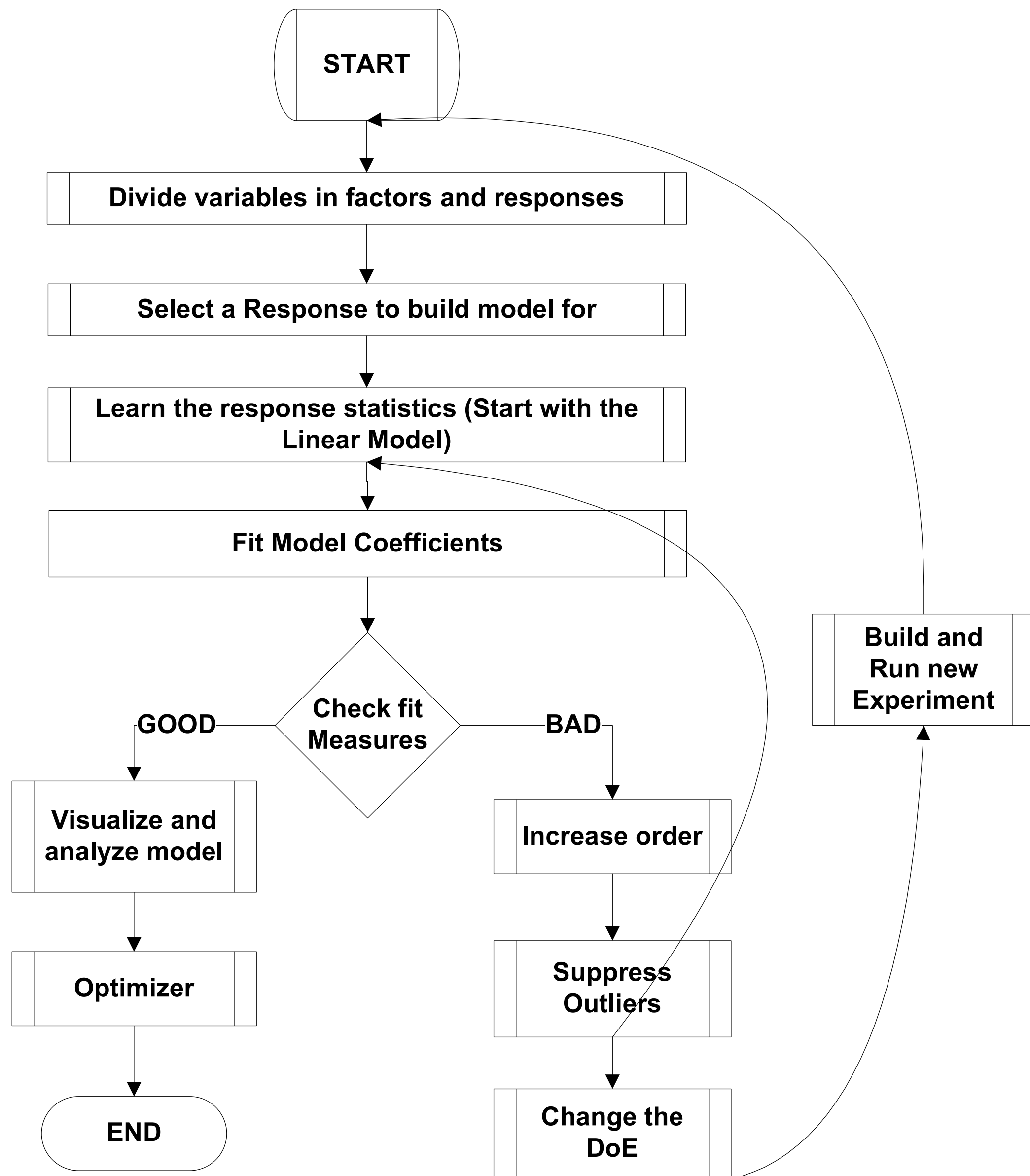

Figure 4.9: Overall Strategy for RSM

The better the model fits the data, the smaller the RRMS value becomes and R^2,$\bar{R}^2$ and R^2_{press} become closer to 1. Ideally, RRMS=0, R^2,$\bar{R}^2$ and R^2_{press} =1.

If the measures are not good, then we can increase the order, interaction order and build new models.Then the best model can be selected by clicking on "Find Best Model". The Best Model will be added under the "Polynomial Models".

Once the best model is found out, choose that model and again click on the "Open" tab. In the "Polynomial Model" window, under the "Polynom" tab, the model equation for the response in terms of the factors is present. This equation can be exported to a .txt file for use in Monte Carlo Flow by selecting **Export->Formula** and saving it as a .txt file. This is the model equation that will be used in getting the PDFs.

Delete all the models which are not required. Choose the best model and open the Perfomance Analysis Tool.

Increase the number of samples to say 1000 and click on "Sample Models". We will be able to see a set of plots including the distributions/histograms of the response and the factors.

Unfortunately, the workbench does not have the option to export the data values of the sampled responses using which further statistics could be found. It generates the values of factors according to a certain distribution, finds the response using the model built and shows the graph !!

To overcome this, another script called "MonteCarlo.pl" is used. It also has the ability to do hspice simulations and is used to verify if the model built is correct.

4.2.2 MonteCarlo.pl

The MonteCarlo.pl script was created to allow comparison of the RSM flow to a more traditional Monte Carlo flow for determination of a PDF. The script can launch a set of HSPICE simulations in the same way that RSMFlow.pl can, except that the sample points will be generated randomly. In addition, the script can be invoked to use the results of the RSMFlow.pl HSPICE simulations. This approach was used to verify that the PDFs generated by MonteCarlo.pl were close to the ones generated by Taurus workbench.

Usage of MonteCarlo.pl

perl MonteCarlo.pl -help

Will show the help for this flow as :

Makesure you do "add hspice" in the terminal window before you run RSMFlow.pl

To run this flow,the inputs needed are:

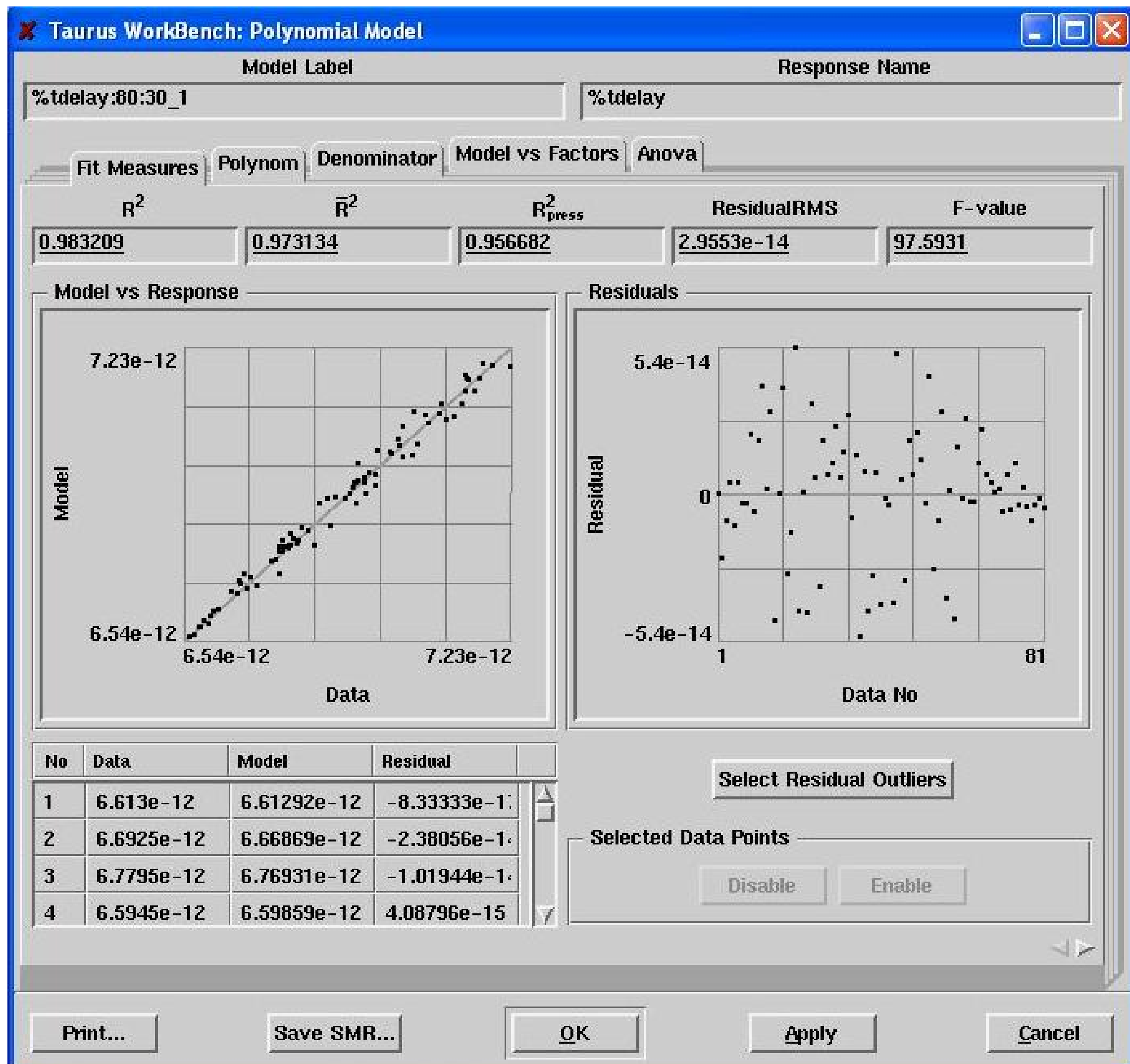

Figure 4.10: Model vs Response and Residual plots for tdelay

- The Netlist file (-netlist).
- The Design Factors can be Vth, Leff, Tox. If any of the factors is not used, its value must be zero.
- Number of runs (-runs)
- The -hspice option is used to indicate whether or not HSPICE runs should be performed. Setting this option to 1 indicates that the input parameters should be varied

randomly, and HSPICE should be invoked. Setting this option to 0 indicates that the results of previous HSPICE simulations should be used. Note that when this option is 1, the script can be used without the rest of the RSM flow, but when the option is 0, it can be used only after RSMFlow.pl has been executed.

Ex: " perl MonteCarlo.pl -netlist INVX1.sp -vth 1 -leff 0 -tox 0 -runs 10000 -hspice 1 "

The model obtained from the previous section which is saved in a .txt file needs to be modified such that it can be used in MonteCarlo.pl perl script. It involves replacement of [by (,] by) , ** by ând vth1, vth2 and so on to variables that MonteCarlo.pl script can recognize.

Usage of Editformula.pl

perl EditFormula.pl -help

Will show the help for this flow as :

perl EditFormula.pl -input INVX1Formula.txt -output INVX1FormulaEdited.txt

-input - file which has the model formula obtained from Taurus Workbench

-output - generated file which has the model formula edited

By using the -hspice 0 option, a set of random numbers is generated according to a guassion distribution of factor like Vth and these values are used in the model formula to calculate the response delay with out doing the hspice simulations of the circuit. If you need to verify the RSM model, it can be done my setting -hspice 1 option where in not only the response is calculated using the RSM model, hspice simulations is carried out similar to RSMFlow.pl and response calculated. Matlab data files are dumped in each case, which can be used calculate the further statistics like mean, variance, standard deviation and fit model to the data.

The results of the above example along with few others are given in section 5.1

4.3 Extraction and Netlisting with WPE

For extracting and netlisting with WPE, the procedure is exactly similar to doing Layout vs Schematic (LVS) check but with a LVS rule deck capable of calculating the instance parameters. That is because, during LVS the transistors are recognized and extracted to layout netlist which is compared to a schematic netlist. So the WPE instance

parameters are calculated for each of the transistors and are present in the layout netlist. The only thing to keep in mind that we need to Flat extraction and not hierarchical so that each of the transistors in extracted along with the corresponding instance parameters. If hierarchical option is used then .subcircuit definitions may be used for some of the gates/circuits and effect of WPE on each of the transistors cannot be studied. As an example, a simple inverter netlist obtained from layout during LVS would be

m0 Y A vdd vdd PMOS_VTL W=5e-07 L=5e-08

m1 Y A gnd gnd NMOS_VTL W=2.5e-07 L=5e-08

With WPE in effect the above netlist would be modified into

m0 Y A vdd vdd pmos_vtl l=0.05u w=0.5u delvto=-0.0249 mulu0= 1.151

m1 Y A gnd gnd nmos_vtl l=0.05u w=0.25u delvto=0.0113 mulu0= 1.069

Because there is no BSIM instance parameter for change in the body-effect coefficient, the change in this variable must currently be done in the transistor model parameters. This capability was added into the RSMFlow.pl but is not documented here.

Since we dont have any silicon data to find out the fitting parameters, $KVTH0WE$ and $KU0WE$ ($K2WE$ was not considered), they were estimated by considering the first order effect, SCA for standard cells. SCA was calculated for a subset of standard cells in the FreePDK standard cell library and the minimum value of SCA was 26.74, maximum value of SCA was 189.25 and the average value of SCA was 92.29. Average SCA value of 100 for standard cell were assumed to have 10% V_{th} and mobility variation and then values of $KVTH0WE$ and $KU0WE$ were chosen to make this match. Using these values of $KVTH0WE$ and $KU0WE$, variation due to any other value of SCA can be calculated. If we can obtain the values of the fitting parameters $KVTH0WE$ and $KU0WE$ either from silicon data or by extensive TCAD simulations, then these values can be changed in the LVS rule file and follow the same procedure as explained before as the calculation of instance parameters remains the same.

Chapter 5

Examples/Results

5.1 Introduction

In this chapter, we present some examples and results to validate the framework for modeling methodology. The effect of WPE on few of the standard cells in the FreePDK45 kit is also given.

5.2 Inverter Delay Modeling

Lets consider an example of a two stage two input Standard Cell Inverter (INVX1) which was used to explain the modeling methodology in the previous chapter. An input pulse with a rise and fall time of 10ps is applied and the stage delay of the first INVX1 stage at its output is monitored when load with an identical second stage. Delay values for rising(tdelayLH) and falling(tdelayHL) edge transitions at the output are obtained using transient analysis. The average delay (tdelay) is calculated as (tdelayLH + tdelayHL)/2.

The percentage variation in the INVX1 stage delay with respect to the nominal, with variations in process parameters considered, is presented in Table: 5.1 and 5.2. The relative deviation of any parameter x about its nominal value x_{nom} is calculated as $\Delta x = (x - x_{nom})/x_{nom}$. A variation of +10% in V_{th} results in decrease in tdelayHL by -2.45% and a decrease in tdelayLH by -5.97% with the average delay variation of -4.51%. Similarly, variation in delay values due to +/- 10%, +/- 5% variation in V_{th}, T_{ox} and L_{eff}, T_{ox} considered together is given. These two tables in a sense give the worst case delay variations considering process variations.

Table 5.1: Process Variation in tdelayHL and tdelayLH for INVX1. The nominal values of tdelayHL=5.7510e-12 and tdelayLH=8.0970e-12

Process Variation	tdelayHL			tdelayLH		
	V_{th}	T_{ox}	T_{ox},L_{eff}	V_{th}	T_{ox}	T_{ox},L_{eff}
-10%	-2.45%	-2.42%	-2.92%	-5.97%	-4.21%	-4.41%
-5%	-1.25%	-1.20%	-1.7%	-4.29%	-3.61%	-4.66%
+5%	1.30%	0.33%	1.32%	1.41%	-0.78%	1.95%
+10%	2.70%	2.57%	5.13%	3.20%	1.12%	5.95%

Table 5.2: Process Variation in tdelay for INVX1. The nominal value of tdelay=6.9240e-12

Process Variation	tdelay		
	V_{th}	T_{ox}	T_{ox},L_{eff}
-10%	-4.51%	-3.47%	-3.79%
-5%	-3.03%	-2.61%	-3.43%
+5%	1.36%	-0.32%	1.69%
+10%	2.99%	1.73%	5.61%

For a +/- 10% process variation in V_{th}, second order models are built for tdelayHL, tdelayLH and tdelay and the model statistics is given in Table: 5.3. The delay models have been tested for their validity to predict the response values. For all the delay models, the statistics are very good. Residual RMS is very low in the order of 10^{-14}. R^2 , $\bar{R}^2$, R^2_{press} are very close to 1 as required.

The model is verfied by performing 10000 Monte Carlo hspice simulations and comparing the actual simulation response with the model-predicted response. The correlation coefficient is >0.95 and shows that model accuracy is good.

Table 5.3: Model Statistics of INVX1 with +/- 10% variation in V_{th}

Statistics	tdelayHL	tdelayLH	tdelay
Residual RMS	3.81565e-15	5.78709e-14	2.95530e-14
R^2	0.999209	0.971604	0.983209
$\bar{R}^2$	0.999168	0.965581	0.973134
R^2_{press}	0.999113	0.958424	0.956682
F-Value	24011.9	161.308	97.5931
Critical F-value	2.46	1.84	1.59
Correlation coefficient	0.9985	0.9596	0.95

The Probability density functions of the delay is show in Fig: 5.1. The distribution obtained using Monte Carlo hspice simulation is overlaid with the distribution using the

RSM modeling approach. We observe a good match for all the distributions. The statistics for variations in V_{th}, obtained by analyzing the resulting distributions is presented in Table: 5.4.

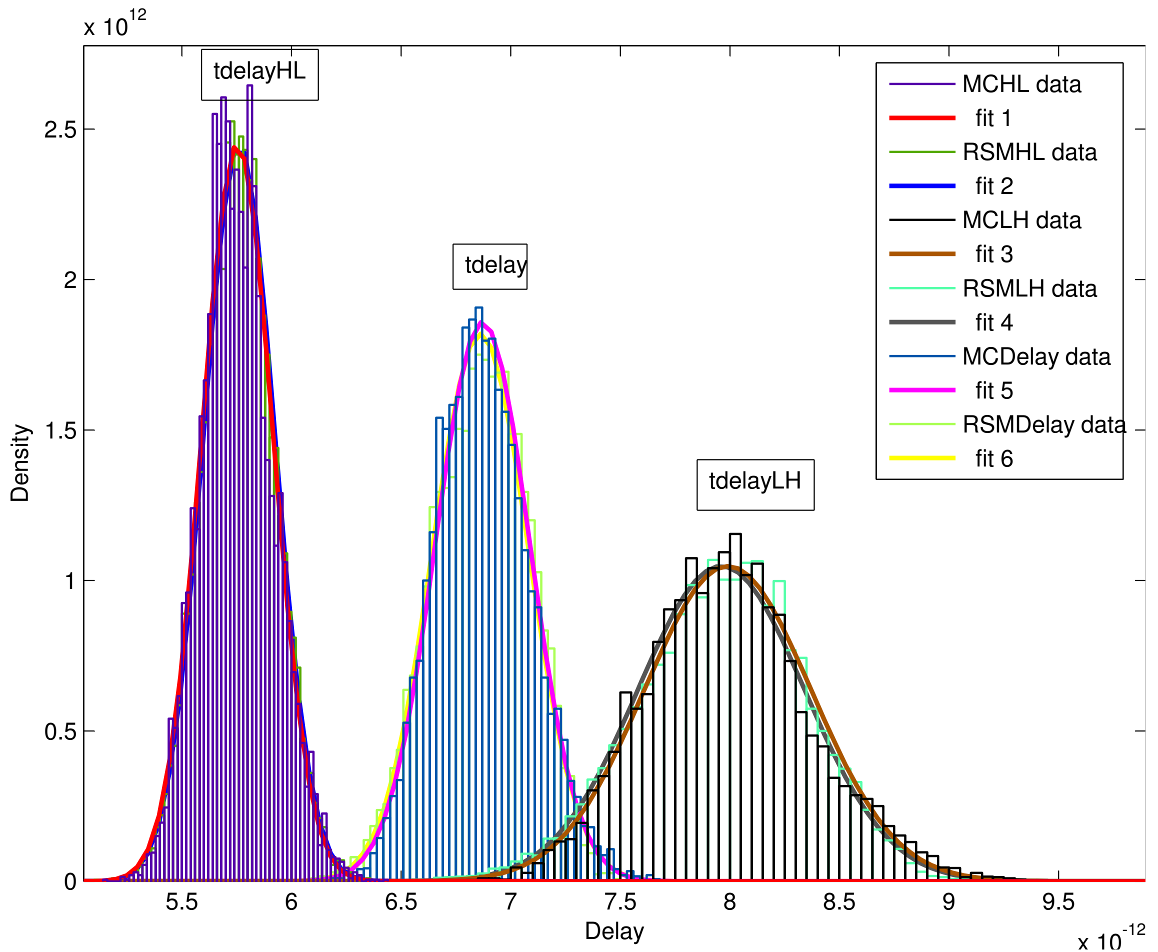

Figure 5.1: PDF of delays of INVX1 with +/- 10% variation in V_{th}

Table 5.4: Delay Statistics of INVX1 with +/- 10% variation in V_{th}

Statistics	RSM Model			Monte Carlo Simulation		
	tdelayHL	tdelayLH	tdelay	tdelayHL	tdelayLH	tdelay
Distribution Mean	5.7535e-12	7.9904e-12	6.8719e-12	5.7619e-12	7.9608e-12	6.8621e-12
Median	5.7450e-12	7.9790e-12	6.8610e-12	5.7610e-12	7.9760e-12	6.8700e-12
Std.Deviation	1.6283e-13	3.8090e-13	2.1463e-13	1.6295e-13	3.8085e-13	2.1925e-13
Variance	2.6513e-26	1.4509e-25	2.1463e-13	2.6553e-26	1.4505e-25	2.1925e-13

Similarly, the PDF of tdelay due to +/- 10% variation in T_{ox}, +/- 10% variation in L_{eff} and T_{ox} is show in Fig: 5.2 and Fig: 5.3 respectively.

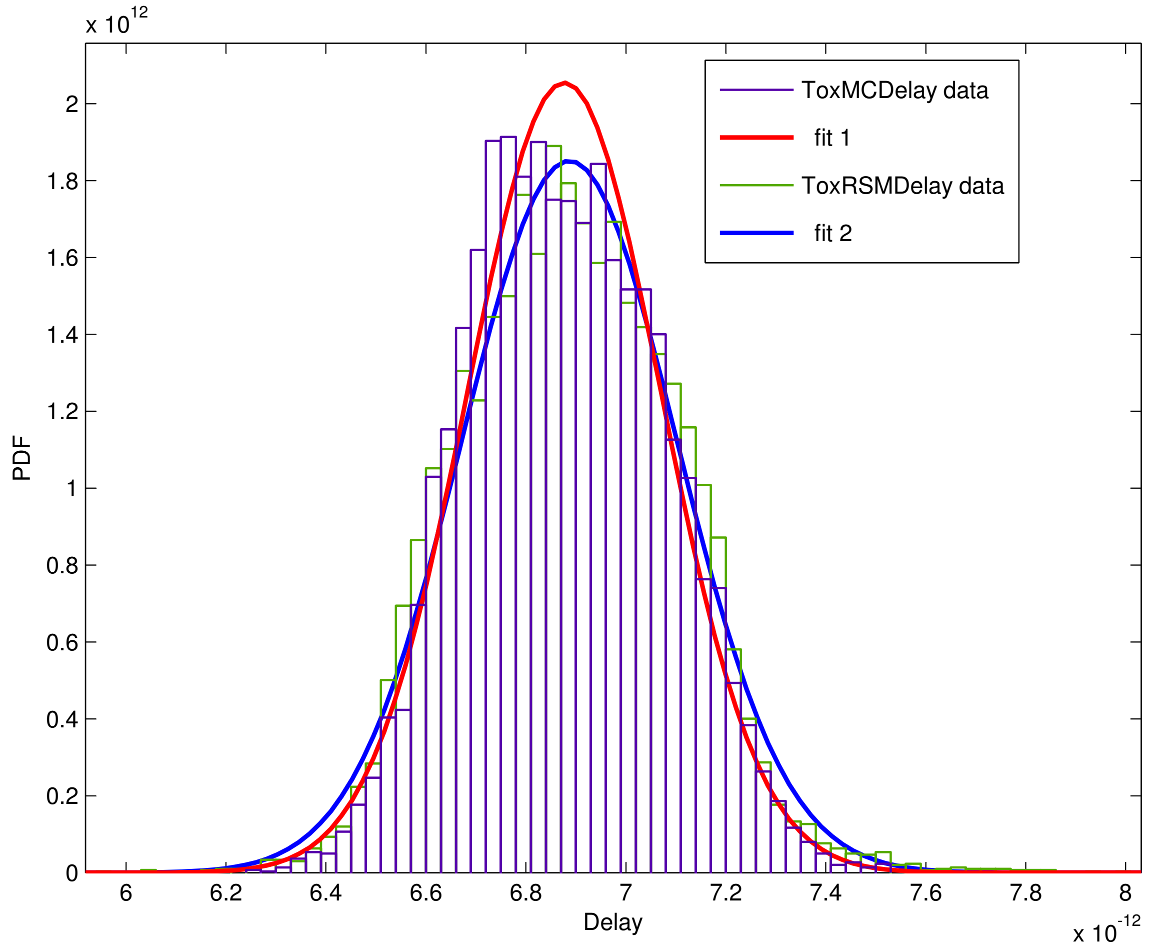

Figure 5.2: PDF of delay of INVX1 with +/- 10% variation in T_{ox}

5.2.1 Runtime Comparison

The runtime of RSM is compared with the traditional Monte Carlo simulations for 10000 runs and result is given in Table 5.5. RSM runtime is approximate as it depends on how fast modeling is done. RSM takes much less time as compared to MonteCarlo simulations.

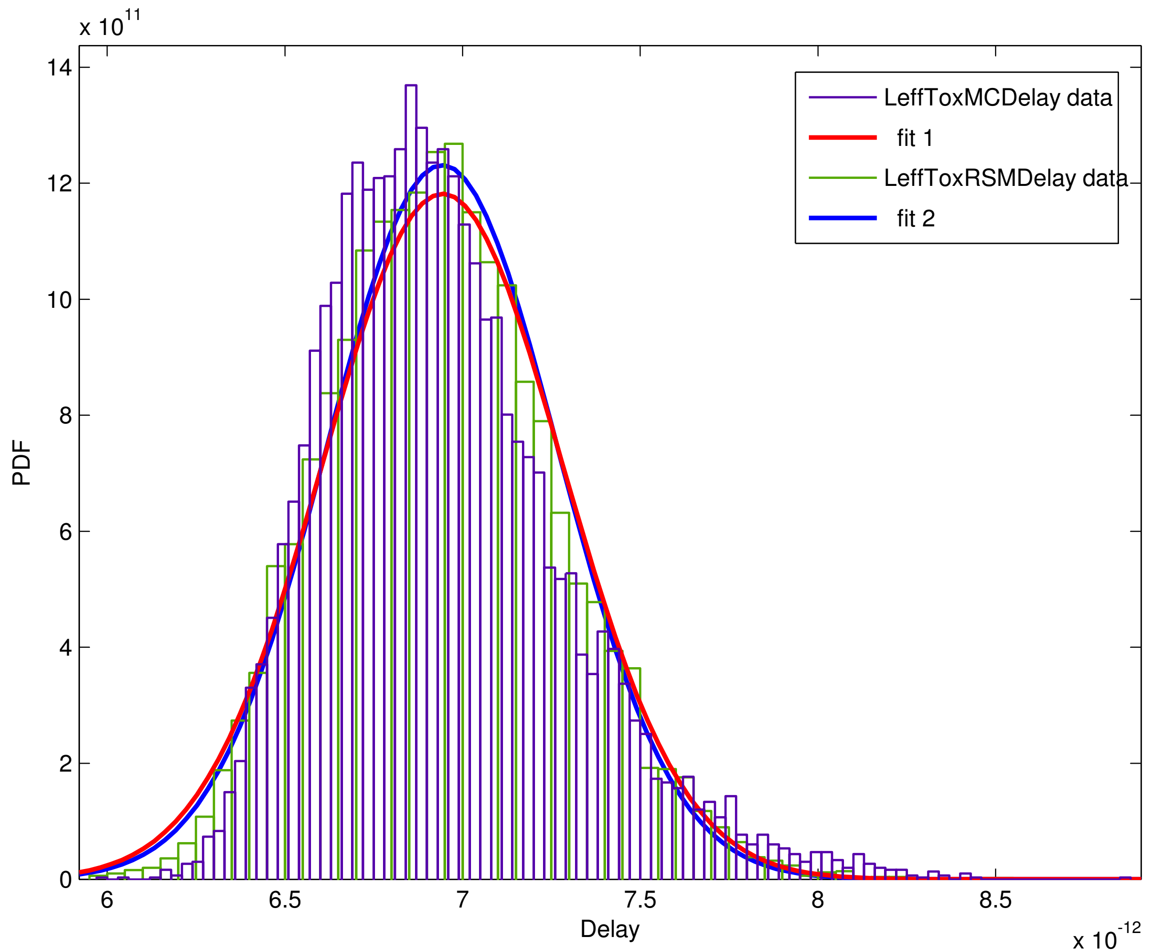

Figure 5.3: PDF of delay of INVX1 with +/- 10% variation in L_{eff} and T_{ox}

Table 5.5: Runtime Comparison

10000 Runs	MonteCarlo	RSM(approx)
INV	1Hr 3Mins	25Mins
NAND	1Hr 28Mins	35Mins

5.3 Chain of Inverters

A chain of 24 invereters is used as a representative circuit to characterize the delay of a digital logic circuit in statistical terms. This chain of inverters can be considered as one of the critical paths of a bigger circuit. The INVX1 gate has been used as the basic element which has been statistically characterized in the previous section. The delay PDFs

obtained in the previous section is used here to further carry out statistical analysis.

The nominal delay of the circuit is 201.7ps and the worst case corners considering +/- 10% variation in V_{th} is 211.6ps and 191.8ps respectively. Now let us calculate the delay of this circuit using the Path Based approach and using stastical sum. The mean of delay for a single stage of INV1 considering +/- 10% variation in V_{th} is 6.861ps and 3 sigma standard deviation is 0.65775ps (from Table: 5.4). So the path delay for 24 inverters is calculated to be 166.55ps. Comparing this value with worst case delay value of 211.6ps, there is differene of almost 20%. From this we can conclude that, using statistical approach and the models built, the overall circuit of which this circuit could be a part of can be clocked at a higher frequency.

5.4 SRAM Bit Cell

One of the parametric failures in a SRAM cell due to process variations [10] is Read Access Failures. During the read operation, the wordline is activated for a limited duration as determined by the cell access time. Read access failures occur if the contents of the cell cannot be read within this duration. In sense amplifier based memory architectures, the contents of a cell are read by sensing the voltage differential between bitlines. The read operation is successful if a precharged bitline discharges by a value large enough to trigger the sense amplifier within the wordline duration.

In this example, a SRAM cell [22] with a precondition circuit which takes care of precharging the bitlines is used to study effect of V_{th} variation on Read Access Failures. The V_{th} of transistors m1 and m2 in Fig. 5.4 is made to vary by +/-10% while the V_{th} of other transistors are kept constant at their nominal values. A zero is written to the cell and then a read is done. Transistors m1 and m2 correspond to pull-down device and access device respectively and are the only transistors that matter for read access time calculations. The Bit Lines (BLBOUT/BLOUT) nets are precharged to VDD through M3/M2 (BLBOUT) and M4/M5 (BLOUT) during read operation (WENB = 1) when CLK = 0. During the positive half of the clock cycle (CLK = 1) of read operation, the BL and BLB lines are tri-stated, so that the bit cells drive the bit lines. The read access delay is calculated as the delay of data transfer to the bit line. The read access time is modelled using the flow and the distribution of access time is shown in Fig 5.5. Table 5.6 summarizes the statistics.

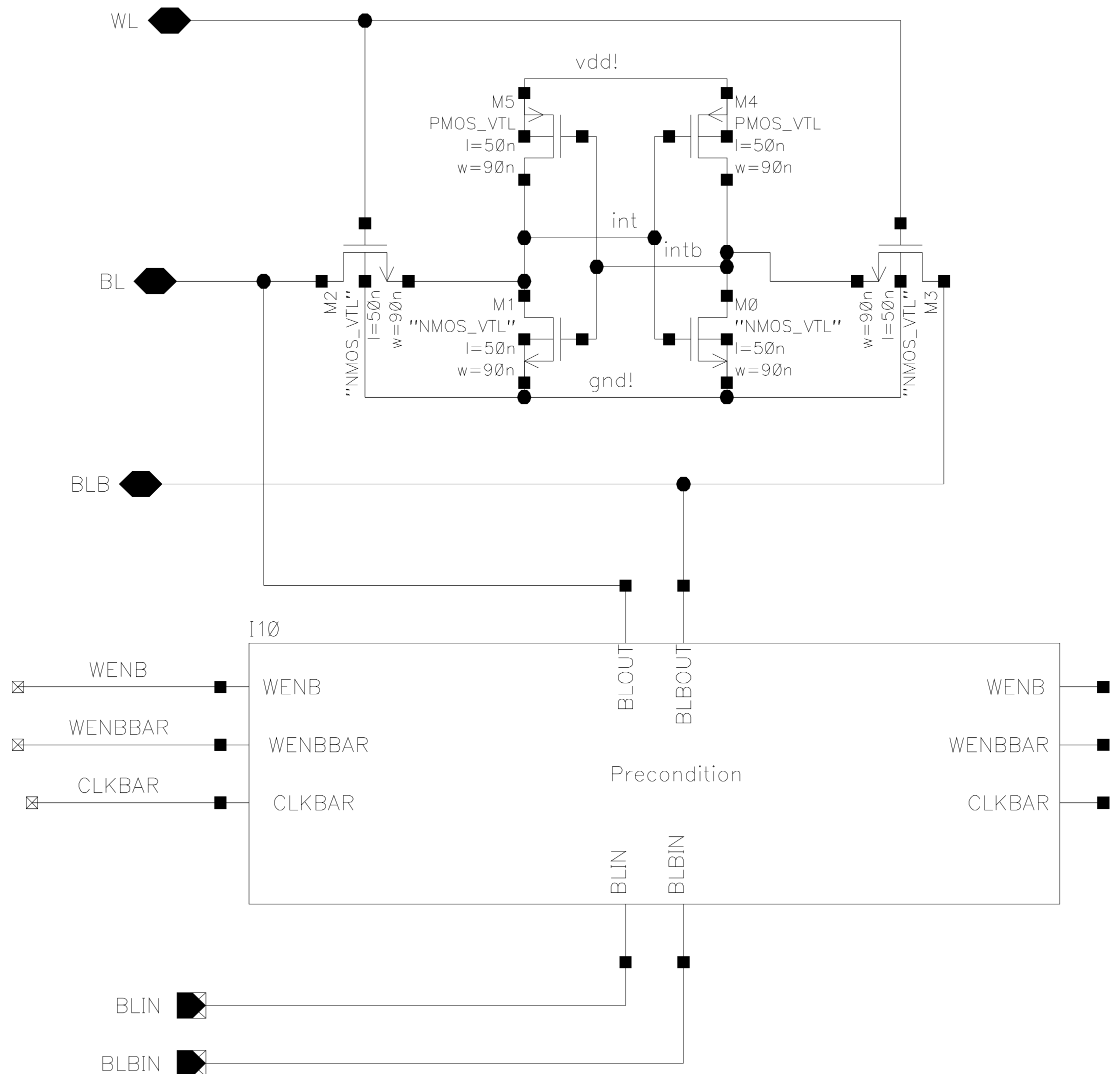

Figure 5.4: SRAM Bit Cell with Precondition Circuit

5.5 Effect of WPE on Standard Cells

To study the effect of WPE on standard cells, simulations were performed using the netlist obtained from the layout during LVS. The layout was extracted with DELVTO and MULU0 separately to see the individual effects of variation in V_{th} and mobility. Table 5.7 shows the WPE effect for standard cells shows 1 to 5% change in rise and fall time due

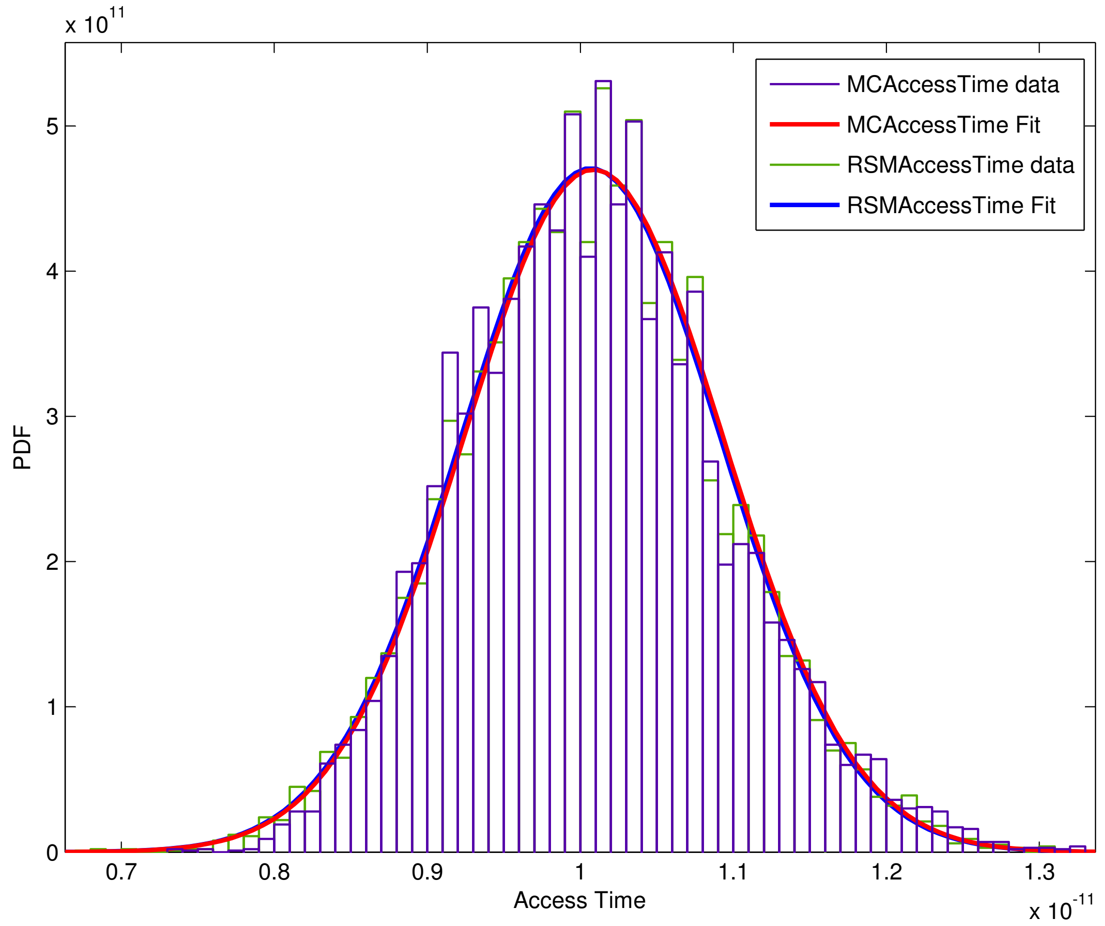

Figure 5.5: The distribution of access time from RSM and MC simulations

Table 5.6: Read Access Time Statistics of SRAM cell with +/- 10% variation in V_{th}

Statistics	RSM Model Access Time	Monte Carlo Simulation Access Time
Distribution Mean	1.01e-11	1.01e-11
Median	1.01e-11	1.01e-11
Variance	7.20e-25	7.18e-25
Standard Deviation	8.49e-13	8.47e-13

to DELVTO and 1 to 9% decrease due to MULU0.

Table 5.7: Standard cell circuit simulation with and without Well Proximity Effect

delay(ps)		No WPE	With WPE (DELVTO)		With WPE (MULU0)	
25C/1.1V		value	value	ratio	value	ratio
INVX1	tdelayHL	5.751	5.868	1.02	5.685	0.989
	tdelayLH	8.097	8.463	1.045	7.3730	0.911
INVX2	tdelayHL	4.869	4.978	1.022	4.809	0.988
	tdelayLH	6.418	6.622	1.032	6.1350	0.956
INVX4	tdelayHL	4.852	4.946	1.019	4.796	0.988
	tdelayLH	6.280	6.439	1.025	6.004	0.956
INVX8	tdelayHL	4.523	4.573	1.011	4.489	0.992
	tdelayLH	5.902	5.914	1.002	5.441	0.922
NAND2X1	tdelayHL	8.661	9.015	1.041	8.524	0.984
	tdelayLH	11.56	12.16	1.052	10.630	0.920
NAND3X1	tdelayHL	11.27	11.50	1.02	11.07	0.963
	tdelayLH	7.302	7.516	1.029	6.957	0.926
NOR2X1	tdelayHL	3.670	3.754	1.023	3.620	0.986
	tdelayLH	8.596	9.001	1.047	7.9510	0.925
NOR3X1	tdelayHL	4.491	4.5450	1.012	4.462	0.994
	tdelayLH	13.82	14.12	1.022	13.09	0.994
MUX2X1	tdelayHL	12.05	12.08	1.002	12.04	0.99
	tdelayLH	10.92	11.09	1.016	10.41	0.953

Chapter 6

Conclusions and Future Work

6.1 Conclusions

DFM is a must to handle process variations in the deep sub micron technologies. If random process variations is not taken into account during the design phase using statistical methods, then the design is going to be overly pessimistic. Also, effect of systematic process variations which can be modeled, needs to be considered. To understand the effects of process variations and to handle them, a framework is required. In this work, we have presented a framework to perform RSM/DoE to model the effects of Random Process Variations on circuit performance parameters. Perl scripts have been used to automate most of the steps involved. The complete flow is explained in detail using an example. The modeling methodology is verified for its accuracy and results presented. A two stage inverter is characterized thorougly and the result used in statistical timing analysis of chain of inverters. The methodology is applied to study the effect of V_{th} variations on read access time of 6T SRAM cell. To study the effect of WPE, LVS rule deck is extended to extract instance parameters based on layout. The effect of WPE on delay was calculated for few of the standard cells.

6.2 Future Work

Considering the work done in this thesis, future directions for for research and enhancement can be classified into those that

- Improve accuracy

- Involve the application of Statistical Analysis

For improving the accuracy, the following needs to be considered

- While considering a circuit for analysis, the wire delay was not taken into account. Variation in wire dimensions and its effects on the overall propogation delay of a signal needs to be handled [16].
- Effect of Stress and Strain as a systematic proximity effect.
- To do a full blown Statistical Analysis considering correlation.
- Tcad simulations to get the fitting parameters in WPE equations.
- CornerS_A_B_C calculation with support from SVRF to measure corner distances in WPE.
- Ability to handle Non-Gaussian Variation, Non-Linear Sensitivity of circuit perfomance parameter.
- To continue the optimization process - by gate sizing and dual-Vth assignment to vary circuit delay or leakage distribution. [11]
- Yield Optimization Process.
- Variation aware buffer insertion.

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