ABSTRACT

BAWA, GAURAV. Switched-Capacitor Filter Based Type-III Compensation for Voltage-Mode Control of Switched-Mode Buck Converters. (Under the direction of Dr. Alex Q. Huang).

In this dissertation, we propose a novel technique for the voltage-mode control of switched-mode fixed-frequency Buck Converters using Switched-Capacitor Filters (SCF). The salient features of the analog sampled-data Type-III filter embodiment (using SCF) is a monolithic solution, automatic scalability of the filter's transfer function w.r.t. the Buck Converter's switching frequency, and moderate on-chip area and power consumption. While the proposed technique is aimed to explore a new design-space, it was observed that it can potentially combine the performance benefits of the conventional all-analog (power efficiency) and all-digital implementations (integration and programmability) of the Type-III compensation.

In our prototype, the proposed Type-III SCF-based voltage-mode controller Integrated Circuit (IC) is implemented in Texas Instruments' 0.36-µm BCD (Bipolar-CMOS-DMOS) technology. The IC is configured to control the Buck Converter for two programmable switching frequencies of 500 KHz and 1 MHz. The IC consumes 1.1 mA of static current from a 3.3 V power supply, and has an active-area of ~ 0.65 mm^2. The theoretical foundations have been validated by performing closed-loop load transient response and open-loop frequency response experiments; while operating the controller IC in closed-loop configuration with a Buck converter power stage.

Switched-Capacitor Filter Based Type-III Compensation for Voltage-Mode Control of Switched-Mode Buck Converters

by
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DEDICATION

To my Parents

BIOGRAPHY

Gaurav Bawa was born in India in 1981. He received the B. Tech. in Electrical Engineering from Indian Institute of Technology (IIT), Delhi, in 2003. From 2003 – 2006, he was employed as a Design Engineer at STMicroelectronics, where he worked on the design and validation of Flash Memory and Analog-to-Digital Converters circuits. In Fall 2006, he started his graduate studies at the Department of Electrical and Computer Engineering at NC State University, Raleigh, NC. Here, he received M.S. (with Thesis) in 2008, and joined the Ph.D. program henceforth. His research interests include Analog/RF Integrated Circuit Design, Signal Processing and Device Physics.

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1. Introduction

1.1 Background and Prior-Art

Last decade has seen the emergence of highly compact, light and efficient portable devices which combine several functions into one. For example, a contemporary handheld cellular phone can serve as an audio/video recorder, a digital camera, a wireless internet browser and a jukebox, to mention a few. This has been made possible largely by the rapid shrinking of the MOS transistor dimensions that allow faster digital computing (Moore's Law) while occupying lesser area on an Integrated Circuit (IC). In contrast, the battery

Figure 1.1: Examples of state-of-the-art portable devices: iPad and iPhone [1].

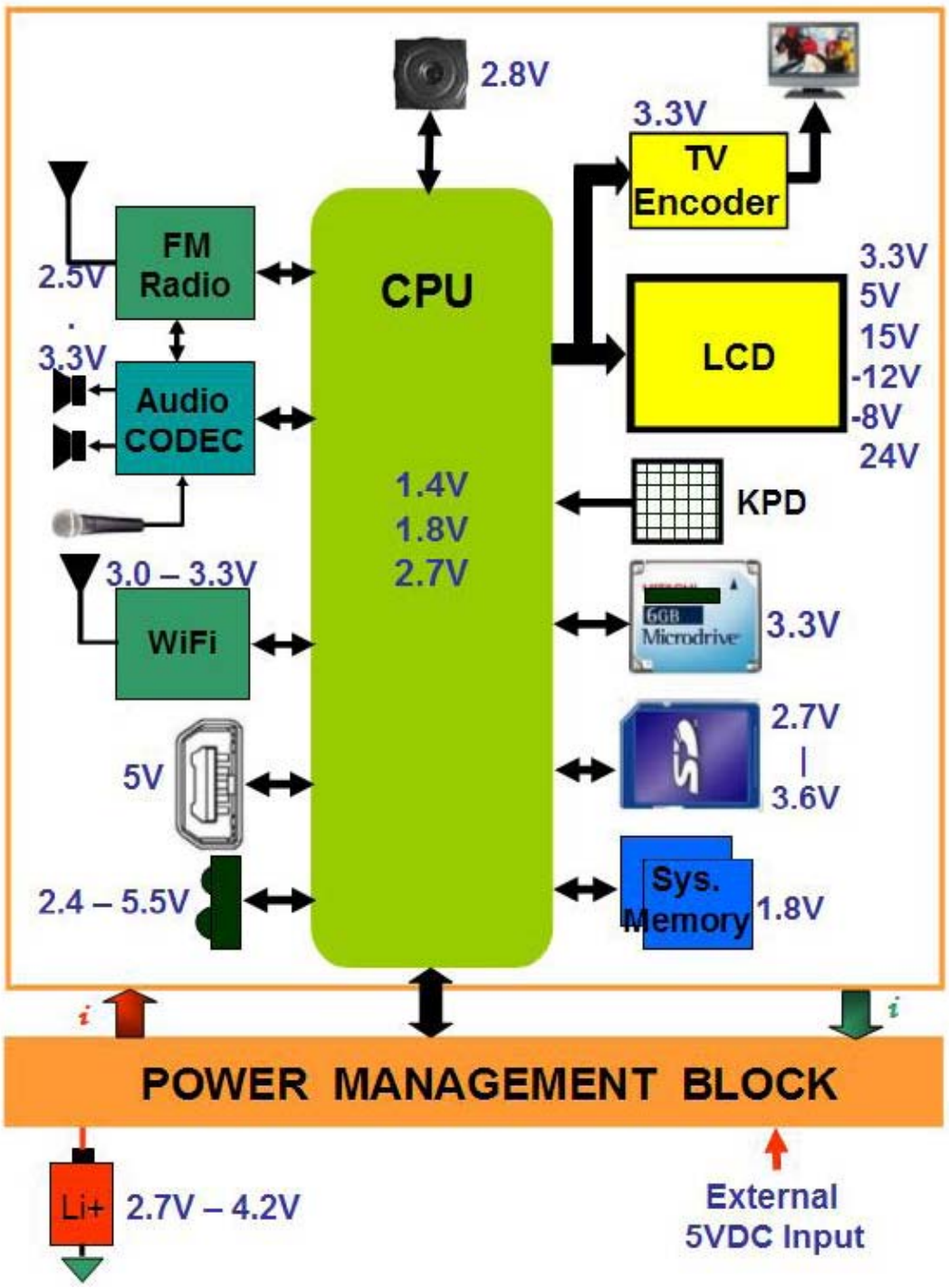


Figure 1.2: Diagram showing various functional blocks and their associated supply voltages in typical portable devices such as the ones shown in Fig. 1.1 [2].

technology needed to power the microprocessor and all the peripheral circuitry has not been able to keep up with the advancements in IC technology. With the battery size being a function of the system power requirements, it ends up occupying a larger portion of the total available size in the contemporary handheld devices, such as the ones shown in Fig. 1.1. This of-course is necessitated by the need to ensure a minimum user full-load user on-time before the battery recharging can take place. Thus, with the size (and weight) of the device at a premium, it is important that the system is designed to be highly area and power efficient, at the same time. These parameters are discussed in greater detail here:

1. Area Minimization: The best way to minimize the area is to try and implement as many circuit functions as integrated solutions, and minimize the off-chip components. In addition, since the ICs can be batch-fabricated, it results in a highly cost-effective solution with considerably lower price per die. However, since not all circuitry can be implemented on a single mammoth packaged IC, it is judicious to have various ICs and their respective packages segregated on the basis of their functionality. This also leads to greater design flexibility. As a result, a printed circuit board (PCB) solution that contains several packaged ICs, individually optimized for high performance and low cost is achievable.
2. Power Efficiency Maximization: To understand the power requirements, we can refer to Fig. 1.2, which gives a generalized block-diagram based overview of power management in portable devices. It can be seen that several positive/negative voltages need to be supplied to various circuit components from a single Li-Ion battery, which can provide an input DC voltage in the range 2.7 – 4.2 V. In addition, every circuit component has a

different current requirement. Hence, with braiding a single common power rail across the PCB not being an option, the efficient solution is point-of-load (POL) regulation. In POL, every voltage regulator is optimally designed for the given load voltage/current requirements and physically present right next to it.

Now, the CPU (Fig. 1.2) is the most power-hungry block in the entire architecture, with power amplifiers for audio/RF transmitters and LCD drivers being a distant second. The CPU is essentially a microcontroller core operating on a high-speed clock, which consumes several amperes of current at full-load (and about a tenth at light-load), and requires a low supply voltage of 1 – 1.8 V. Hence, a dedicated power converter which can efficiently step-down the battery voltage to the rated CPU voltage is *indispensable* in ensuring high overall system power efficiency. The design of such a regulator is indeed the focus of this research.

With the aforementioned area and power requirements in mind, a fully-integrated high-efficiency step-down voltage regulator would indeed be a plausible solution. This essentially gives us the following three options:

1. Linear Regulator

The schematic of a linear regulator is shown in Fig. 1.3. The output voltage (V_{OUT}), is regulated to a scaled version of the on-chip bandgap reference voltage (V_{REF}), by the resistors $R_{1,2}$ and the error amplifier in feedback:

$$V_{OUT} = V_{REF}\left(1 + \frac{R_1}{R_2}\right) \tag{1.1}$$

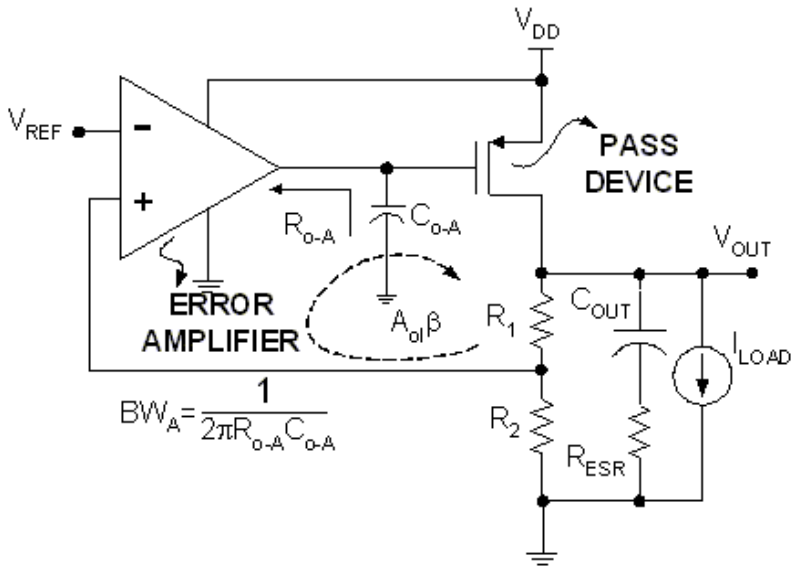


Figure 1.3: Circuit schematic of a linear regulator [3].

The linear regulator can be a fully-integrated solution (with the exception of load capacitor) but suffers from poor efficiency. The efficiency, assuming only the load current flows through the pass device, and zero current in the error amplifier, is given by:

$$\eta_{LIN} = \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT}}{V_{IN}} \tag{1.2}$$

For a given regulated V_{OUT} (= 1.5 V), the efficiency is maximum at lowest battery input voltage, V_{IN} (= V_{DD} = 2.7 V). Hence, the best case efficiency (= 55 %) is unacceptably low. It must be understood that even though this solution is fully-integrated and should result in lower area, the poor efficiency will result in a larger battery size (for a given user on-time). In addition, poor efficiency will also result in higher overall power dissipation for a given load power requirement, and can significantly heat up the device. Hence, power efficiency is the bottleneck to building a compact portable device.

2. Capacitive Charge-Pump Regulator

Fig. 1.4 shows the schematic of a step-down capacitive charge-pump based regulator in two different configurations. In a charge-pump, the flying capacitors C_1 and C_2 are

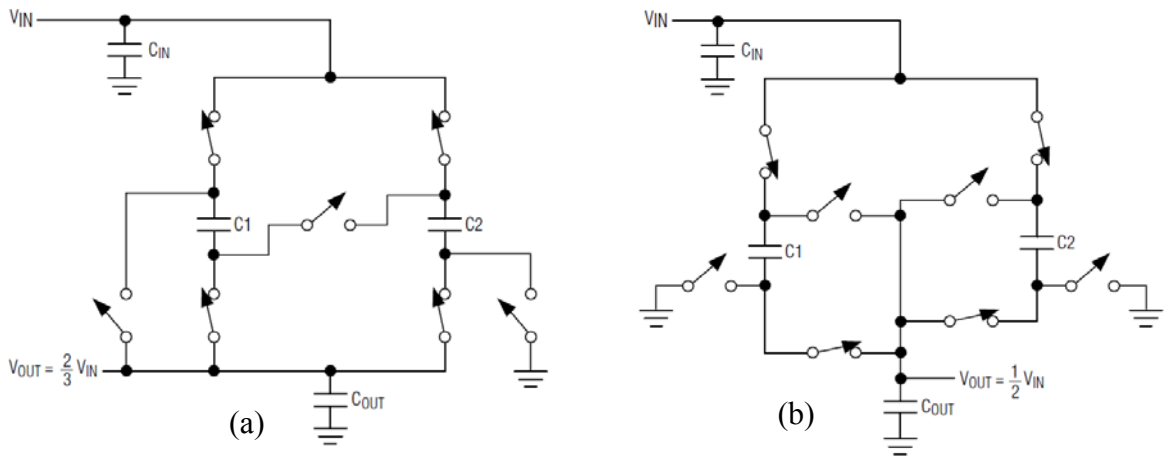


Figure 1.4: Circuit schematic of a step-down charge-pump regulator during C_1 and C_2 charging in (a) 3:2 and (b) 2:1 configuration. [4]

charged by V_{IN} in one phase, and share charge with C_{OUT} in the complementary phase. Based on the connection of the switches between the flying capacitors, the charge-pump can have various V_{IN} and V_{OUT} configurations (Fig. 1.4). Several operating modes are required in order to maintain high efficiency when the battery voltage (V_{IN}) changes for a given output voltage (V_{OUT}). With the exception of C_1, C_2, C_{IN} and C_{OUT}, the entire architecture can be fully-integrated. In addition, these capacitors can be made smaller by choosing a higher switching frequency, which decreases the output impedance of the converter. In [4], $C_{1,2} = 0.22$ µF, $C_{IN} = 1$ µF, $C_{OUT} = 4.7$ µF, for a switching frequency of 2 MHz and load current requirement of 50 mA. More than 85 % efficiency under steady-state conditions is ensured in various

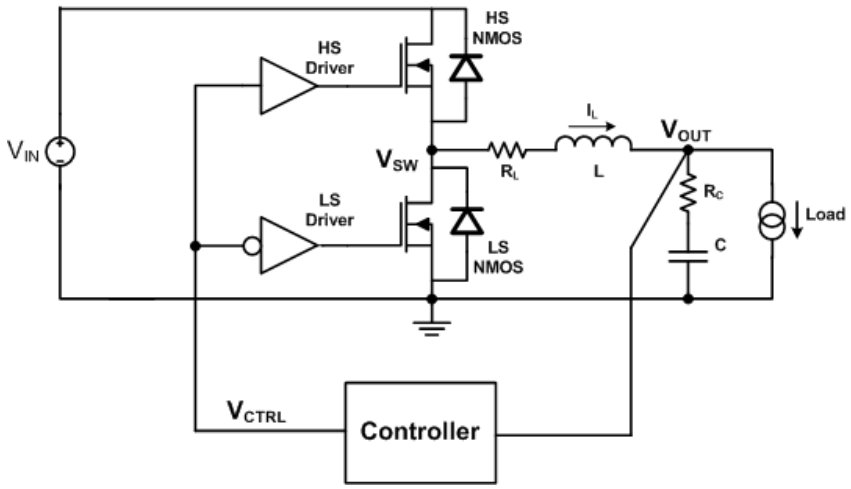


Figure 1.5: Circuit schematic of a switched-mode synchronous Buck Converter.

operating modes.

A fundamental limitation with the charge-pump (and the linear regulator as well) is the maximum current that can be supplied to the load [5]. This is limited by the input current drain, and hence high efficiencies can only be obtained for load currents up-to 200 mA. In addition, since a charge pump has discrete operating modes, it has poor regulation capability and efficiency around the points of mode transition.

3. Switch-mode Inductive Buck Regulator

Fig. 1.5 shows the circuit schematic of switch-mode Buck converter, with controller directly sensing the output voltage V_{OUT}, for regulation. Now, the High-Side (HS) and Low-Side (LS) NMOS are driven by complementary switches such that the switch-node V_{SW}, emulates a square wave with amplitude V_{IN} and duty cycle 'D' at any given switching frequency (f_{SW}). The duty cycle also corresponds to the time for which the inductor (L) is charged by switching the HS NMOS *On*. This square wave (at V_{SW}) when filtered by a low-

loss LC filter provides a stable output DC voltage V_{OUT}, to the load. It can be proved under steady-state conditions with V_{CTRL} (and hence V_{SW}) having a duty-cycle 'D' at a given f_{SW}, and assuming zero loss in switches and LC tank [6]:

$$V_{OUT} = D \times V_{IN} \tag{1.3}$$

Thus, with $0 < D < 1$, the output voltage is a scaled-down version of the input voltage. Now, the Buck converter can handle large output currents and it is indeed the preferred solution for powering the CPU (see Fig. 1.2) [5]. In state-of-the-art BCD technologies it is also possible to integrate the HS/LS NMOS and their corresponding Drivers on one die, while delivering full-load current of 3 A at an efficiency ~ 90 % [7]. This efficiency target is achieved at a nominal switching frequency of 1.1 MHz, at which it is not possible to integrate the LC filter. Higher switching frequencies (> 100 MHz) can be targeted to decrease the LC filter size for possible integration, but are generally not preferred due to the decrease in efficiency, as a result of increased frequency-dependent switching losses [6]. The main limitation exists in the switching device technology, which has a fundamental tradeoff between its on-resistance (conduction losses) and gate-capacitance (dynamic losses) minimization. In addition, the LS NMOS body-diode (see Fig. 1.5) reverse-recovery losses (during dead-time) also increase with higher currents and faster switching transients. Recently, many high-frequency Buck converters have been reported to be integrated designs [8]-[12]. Amongst these, the maximum reported load current is 300 mA for a corresponding efficiency of 83.2 % at f_{SW} = 233 MHz [10]. The authors have employed Surface-Mount Technology (SMT) air-core inductors mounted on-chip, while the output filter capacitor is integrated. In [11], when both L and C were integrated on-chip with f_{SW} = 170 MHz, an efficiency of only 77.9 % was

achieved for a 190 mA load. It must be understood that the current device technology presents fundamental barriers to the attainment of a high frequency (> 100 MHz) and high full-load current (> 1 A) switch-mode Buck converter with high power conversion efficiency (> 90 %).

With the LC filter integration not possible for the given load current requirements, our focus now shifts to the controller (Fig. 1.5). The controller is an essential component of the Buck converter design that ensures the regulation of output voltage even in the presence of noise, line/load transients and temperature variations. This is accomplished through negative feedback from the output voltage to control the duty cycle of the Buck converter. The following considerations are important in designing a controller for a Buck converter based CPU power supply:

i. DC Regulation: The steady-state regulation of the converter needs to be very tight for computing power applications (< 1 %). This is because it directly affects the performance and reliability of the digital circuitry. The DC regulation includes both the line and load regulation. This essentially means that the output DC voltage should not change by more that 1 % over the entire range of battery voltage and load current requirements (light/full load).

ii. Output Voltage Ripple: The ripple requirements for digital circuitry are much relaxed compared to that for sensitive analog designs. Hence, typically a ripple voltage of less than 5 % is considered acceptable. It must be understood that the output voltage ripple is determined by the output LC filter design for a given load current and switching

frequency. However, as discussed later, certain control strategies can also place minimum output voltage ripple requirements on the LC filter for voltage regulation.

iii. Stability Considerations: The converter should be stable under varying line/load conditions and LC filter values (determined by the worst case voltage/current ripple requirements). In addition, the controller must ensure that the converter is stable while transitioning from Continuous Conduction Mode (CCM) to Discontinuous Conduction Mode (DCM), and vice versa.

iv. Transient Response: The output voltage of the Buck converter should be able to recover quickly when a load step transient takes place. The closed-loop transient response is characterized by the voltage overshoot and settling time, and is a function of the load step magnitude and its di/dt. If the closed-loop stability is ensured with an under-damped 2^{nd} order response, the overshoot and settling time are inversely related. Typically, an over-/under-shoot < 10 % is an acceptable specification for CPU power supplies, which have di/dt ~ 1 A/μs. Note that we have only considered the effects of controller response on the transient performance, inside the control-loop bandwidth. In reality, the LC filter, PCB layout and IC packaging parasitic inductances also impact the transient response, by defining the high-frequency output impedance. To conduct a fair comparison, we will consider these effects to be the same for all types of compensation schemes.

v. Electro-Magnetic Interference (EMI) Considerations: EMI is an important concern for switching regulators especially due to the high strength of the current signal being commutated between HS and LS NMOS switches (Fig. 1.5). EMI thus needs to be controlled in order to meet the FCC regulations. Another serious concern is the possible

malfunction of the sensitive RF/analog circuitry present on the same board (see Fig. 1.2). There are two ways in which a controller can lead to poor EMI performance: Firstly, if the V_{CTRL} signal is jittery, it can fire the HS/LS commutation at non-uniform intervals or even lead to spurious switch activation. Secondly, if the frequency of the converter is not explicitly defined, it is prone to spreading over a range of values due to noise and temperature variations. In addition, it would not be possible to synchronize the converter with the system clock. Filtering of such effects can create havoc for the adjacent signal/power processing circuitry since its exact characteristics are unpredictable.

In addition to these requirements, the controller must have low enough power consumption such that the light-load efficiency is not significantly affected. In addition, a fully-integrated solution is preferred since it results in lower area. The aforementioned requirements are very much in-line with the overall power converter design requirements, and will not be discussed in more detail.

At this point, we can compare the available control schemes for voltage regulation. These can be categorized as either linear or non-linear control methods. Linear control schemes are based on the low-frequency linear small-signal response of the switching converter [6]. Such schemes use a fixed switching frequency (f_{SW}) for the converter using an on-chip clock oscillator (Fig. 1.6). The compensator morphs the input error signal ($V_{OUT} - V_{REF}$) based on its frequency response and generates V_{COMP}. The V_{COMP} signal must now be translated into appropriate duty cycle information for the converter. This is done by the asynchronous comparator comparing V_{COMP} with a linear ramp (sawtooth running at f_{SW}), to generate a Pulse-Width Modulated (PWM) signal, V_{PWM}. Since the switching converter's

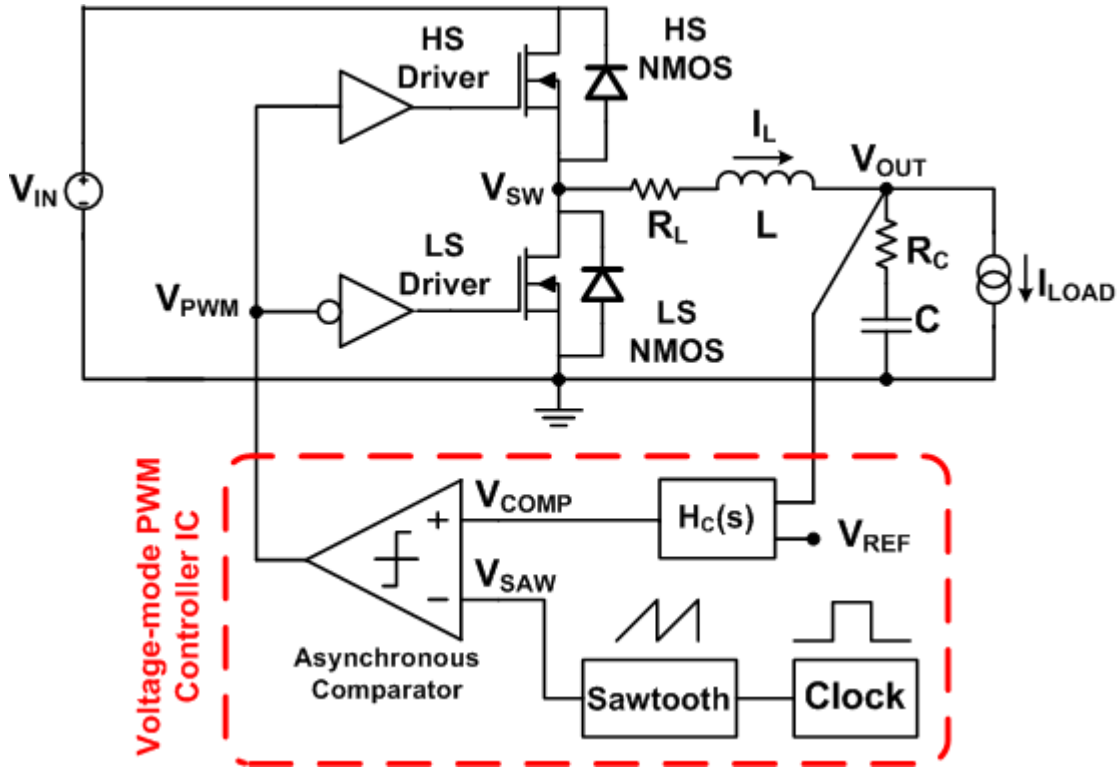


Figure 1.6: Circuit schematic of a linear PWM control based Buck Converter.

linearity is only valid for low-frequencies, it is the job of the compensator to ensure closed-loop stability with a low cutoff bandwidth $f_C \sim f_{SW}/10$. Thus, the transient response is limited by the switching frequency of the converter. Contemporary architectures employ $f_{SW} \sim 1 - 4$ MHz, which presents a reasonable tradeoff between size, efficiency and transient performance [5].

Basic non-linear control schemes monitor the output voltage ripple and can be based on either of the following two:

A. Hysteretic Control:

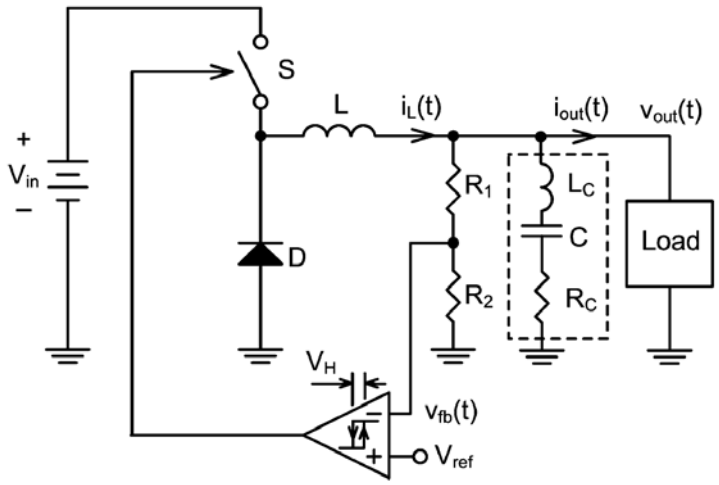


Figure 1.7: Circuit schematic of a hysteretic control based Buck Converter [13].

Fig. 1.7 shows the schematic of a hysteretic regulator. The asynchronous comparator (with hysteresis band V_H) compares the divided output voltage (V_{FB}) with the reference voltage V_{REF}, and turns the switch '*S*' *On* whenever $V_{FB} < V_{REF} - V_H/2$. The switch is turned *Off* when $V_{FB} > V_{REF} + V_H/2$. Thus, the output voltage is regulated to:

$$V_{OUT} = V_{REF}\left(1+\frac{R_1}{R_2}\right) \pm \Delta v \tag{1.4}$$

$$\Delta v_{\max} = \frac{V_H}{2} \times \left(1+\frac{R_1}{R_2}\right) \tag{1.5}$$

Hence, V_{OUT} is the sum of a DC component and an AC voltage ripple (Δv), and it maximum amplitude is given by Δv_{max}. The ripple magnitude (and hence large R_C) is clearly needed to be high for successful operation in a noisy environment. If V_H band is made smaller, the hysteretic converter is prone to jittery behavior. In addition, the steady-state switching frequency (f_{SW}) is a function of L, C, L_C, R_C, V_H and T_D. Here, T_D is the comparator delay,

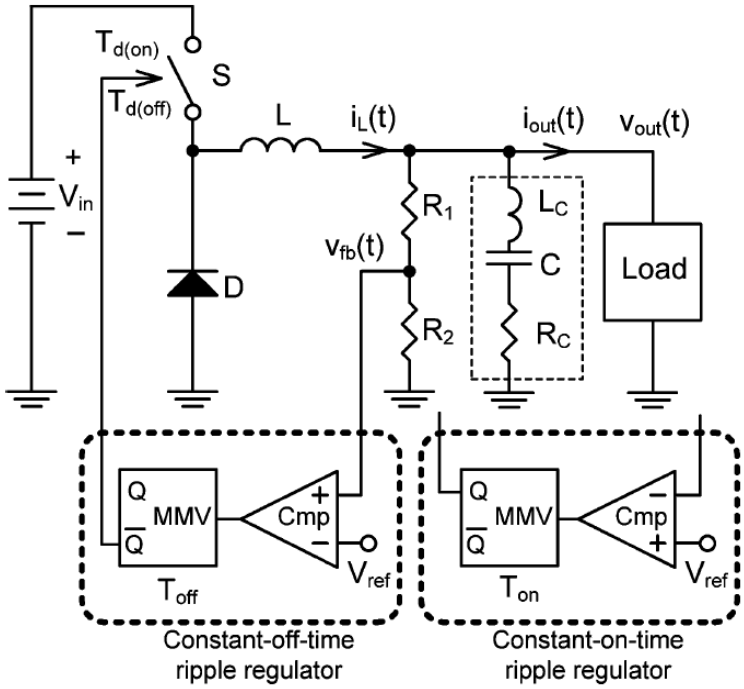


Figure 1.8: Circuit of constant-On/Off-time control based Buck Converter [13].

which is a highly non-linear function of temperature, process variations and input voltage slopes. Clearly, the switching frequency is poorly defined. The advantages of such a control are low power consumption, fully-integrated architecture, fast transient response (settles within 2 switching cycles [13]) and reduction in f_{SW} under DCM conditions (to ensure good light-load efficiency).

B. Constant-On-Time Control:

An improvement over the hysteretic regulator is the Constant-On-Time controller (Fig. 1.8). In this scheme, all the advantages of hysteretic regulator are inherited, while the problems of large f_{SW} spread, high noise sensitivity and poor DC regulation are improved upon. This is accomplished by generating a constant duty pulse whenever $V_{FB} < V_{REF}$. This

Table 1.1: Comparison of various Buck Converter control schemes

Performance Metric	***Fixed-Frequency***	***Hysteretic***	***Constant-On***
DC Regulation Accuracy	Good	Poor	Average
V_{OUT} Ripple Magnitude	Small	Large	Large
Stability Concerns	Stable with all *LC*	Large R_C	$R_C C > T_{ON}/2$
Transient Response	Average	Good	Good
EMI Regulation	Good	Poor	Average
Power Consumption	Analog – Moderate Digital – Very High	Low	Low
Monolithic Solution	Analog – No Digital – Yes	Yes	Yes

charges the inductor '*L*' for a given time (= T_{ON}), which can be programmed using a Monostable Multi-Vibrator (or one-shot). Thus, only the *Off* time is impacted by T_D and thus the frequency has lower spread than the hysteretic regulator. The comparator stills needs to monitor the V_{OUT} ripple and hence R_C cannot be made small. In addition, there is a stability concern in CCM which limits the minimum value of R_C to $T_{ON}/2C$ [13].

Table 1.1 compares the linear (fixed-frequency) control scheme with the two non-linear schemes (discussed above) on various controller performance metrics. Those cells have been highlighted in yellow in which the best performance is ensured by the control schemes under consideration. It can be seen that fixed-frequency (FF) control outperforms the non-linear schemes on DC regulation, output voltage ripple, stability across all LC (designed to meet ripple requirements) and EMI regulations. The biggest advantages of the non-linear schemes are their fast transient response and low power consumption. It must be understood that our target application is high-performance computing platforms, in which

DC regulation and voltage ripple are parameters which cannot be compromised. In addition, EMI is a serious concern since it is a high-current (> 1 A) switching converter that can impact the performance of nearby circuitry (Fig. 1.2).

To conclude, we have seen that a switch-mode Buck regulator is indeed a viable solution for high-current high-efficiency step-down power conversion for high-performance digital computing such as the CPU in portable applications. To save area, it is possible to integrate the switching devices and their associated drivers. However, the LC filter cannot be integrated in current technologies. On the controller front, the discussions in Table 1.1 lead us to conclude that fixed-frequency control is indeed the way forward. However, as can be seen in Table 1.1, ensuring a monolithic and power efficient solution for FF-control is not possible at the same time. This is indeed the topic of our next discussion and motivation for further research.

1.2 Research Motivation

In this section, we will first compare and contrast the analog vs. digital control schemes that are employed in PWM control based Buck converters. Our focus is thus on the $H_C(s)$ block in Fig. 1.6. In the analog implementation, Type-III compensation is used, especially in Buck converter designs that employ low-ESR Multi-Layer Ceramic Capacitors (MLCC) for small V_{OUT} ripple, low EMI and small footprint requirements [7]. This filter has the following transfer function corresponding to the circuit in Fig. 1.9.

$$H_C(s) = -\frac{1}{sR_2(C_2 + C_3)} \times \frac{(1 + sC_1(R_1 + R_2))(1 + sR_3C_3)}{(1 + sC_1R_1)(1 + sR_3(C_2 \,||\, C_3))} \tag{1.6}$$

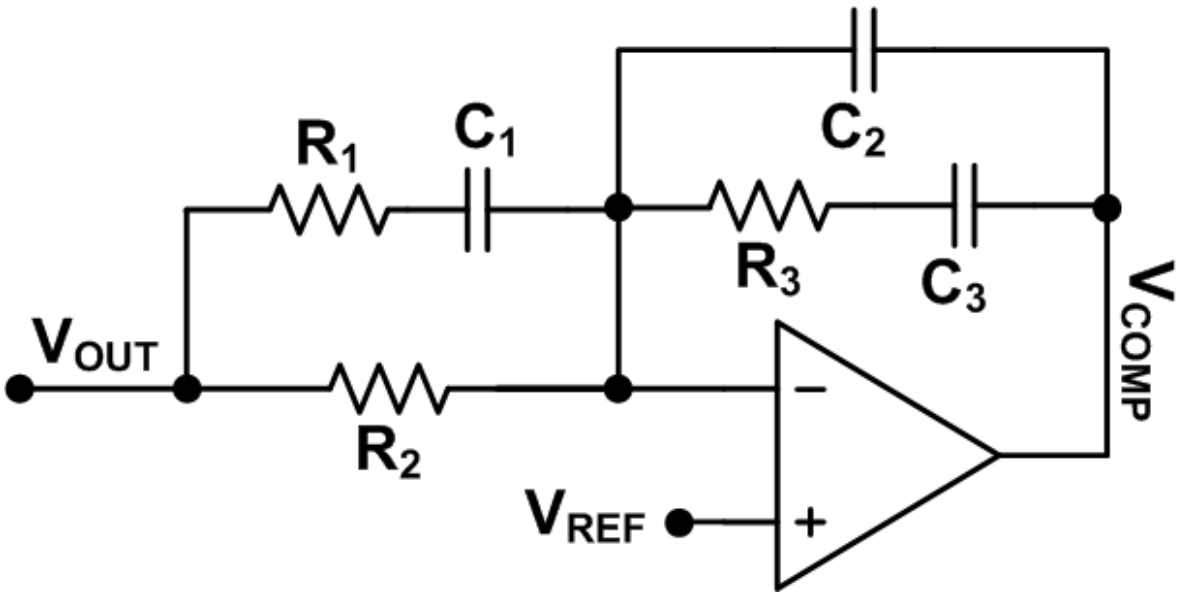


Figure 1.9: Type-III filter circuit used for analog compensation in Fig. 1.6.

Thus, a Type-III filter consists of an integrator for closed-loop DC regulation and two real zeroes for phase boost close to the LC filter double-pole. One pole is generally placed at the ESR zero frequency (given by $1/R_C C$ from Fig. 1.6) and another pole is placed at high frequency for attenuating the high-frequency switching harmonics. The Bode Plot of the Magnitude and Phase response of the filter is shown in Fig. 1.10, using asymptotic approximations. Now, we must consider the power requirements for amplifier used in Fig. 1.9. In order to successfully realize the filter transfer function, the amplifier Gain Band-Width (GBW) must be at-least 10 times higher than the filter Unity-Gain Bandwidth (UGB) given by f_{UGB} in Fig. 1.10. Now, for a Buck converter designed for f_{SW} = 1 MHz, typically f_{UGB} > 1 MHz and hence the amplifier's GBW, f_{GBW} > 10 MHz. In addition, the load capacitance to be driven by the amplifier is in the nF range [7]. These design requirements result in the amplifier burning > 1 mA of current in its output stage, just to push the non-

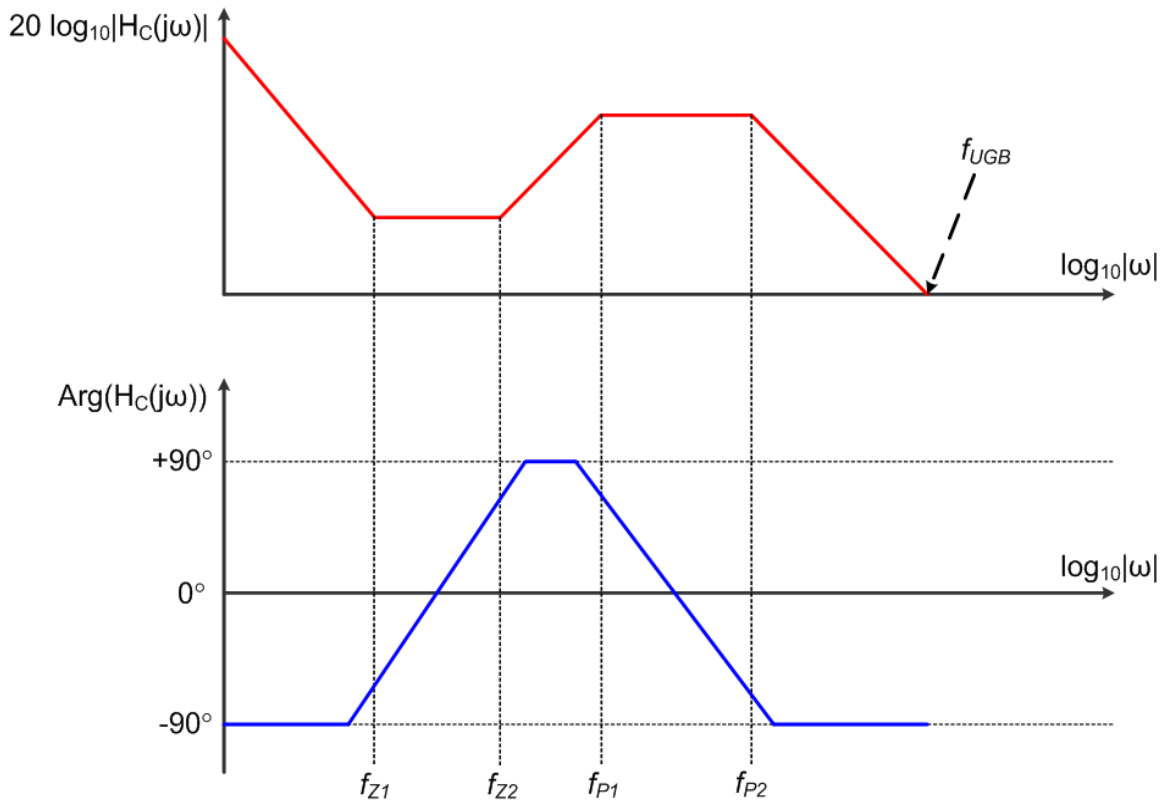


Figure 1.10: Frequency response of the Type-III filter circuit in Fig. 1.9.

dominant pole outside f_{GBW}. It must be understood that pushing higher switching frequencies would correspondingly result in an increased level of amplifier power dissipation. This level of power consumption is, however, acceptable even for ensuring high light-load efficiency in the current application. This is also made possible by the fact that many protection functions such as Over-current Protection (OCP) and Under-Voltage Lock-Out (UVLO) can be easily implemented by low-power analog circuitry. In [7], the total power consumed is ~ 2.2 mA for f_{SW} = 1.1 MHz Buck converter design. Another issue with this filter is that the capacitor values are too large to be integrated on-chip (in nF range). An example calculation for all

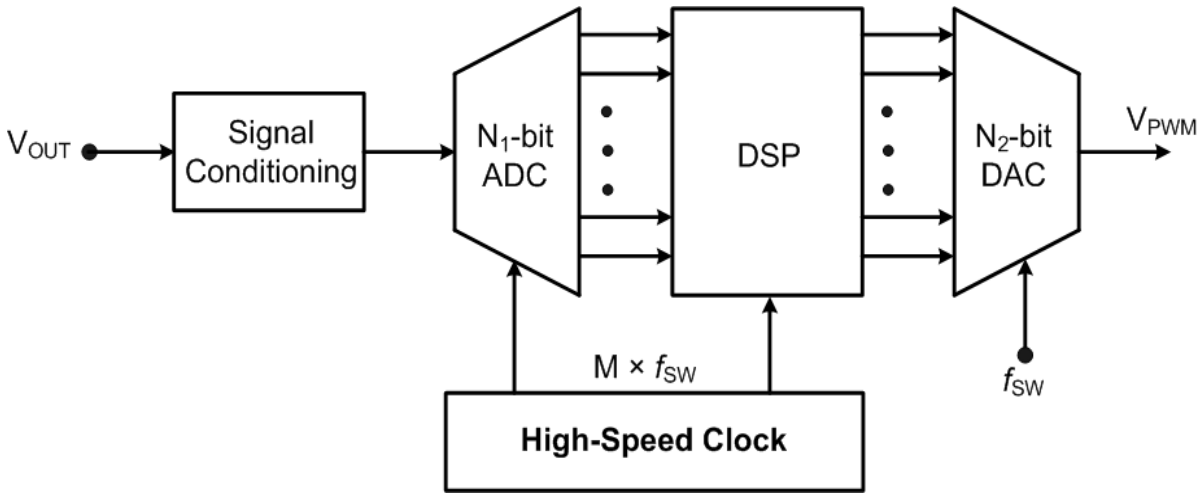


Figure 1.11: Block diagram showing the concept of Digital PWM control.

filter components for a 1 MHz Buck converter design is given later in Table 3.1 in Section 3.3. In addition, the RC time constants will vary ±40 % due to Process, Voltage and Temperature (PVT) variations, once they are implemented on-chip. These considerations rule out the possibility of a monolithic solution and result in a larger footprint and increased cost. Finally, the power supply designer can choose to operate the switching converter at a frequency of choice, based on area vs. power efficiency constraints in a given application. While the power-stage (excluding the LC filter) can remain the same, the filter components need to be redesigned and there exists no programmability.

To counter the aforementioned problems of the analog implementation of those of integration and programmability, there exists a Digital-PWM (DPWM) implementation. This is conceptually shown in Fig. 1.11. The output voltage is first conditioned, which includes calculation of the error signal ($V_{OUT} - V_{REF}$) and subsequent amplification. Thereafter, it is fed into a low-resolution high-speed Analog-to-Digital Converter (ADC), and it gives N_1-bit

digital output. This digital data is then processed by a Digital Signal Processing (DSP) circuitry, which implements the Type-III filter and the associated PWM functions. This digital output is then converted into an analog PWM signal every switching interval by a high-resolution Digital-to-Analog Converter (DAC).

The faster the DSP clock speed, higher is the temporal resolution of the controller and better the transient performance. Thus, in order to achieve a transient performance comparable to the analog counterpart, a very high speed clock is required and the analog front-end and digital circuitry ends up burning a lot of power. In addition, the DC regulation is largely a function of the DAC resolution, again making it a power intensive unit to meet the large SNR requirements. For a state-of-the-art DPWM based controller in [15], the power consumption for a 4-phase design is 40 mA (digital) and 8 mA (analog). This implies about 12 mA power consumption per phase. It is for this reason that DPWM controllers are more attractive for multiphase designs since a lot of digital monitoring and communication functions can be shared.

The DPWM scheme is fully-integrated on-chip and a highly programmable one. The user can configure the pole/zero placements, and even tune them based on the switching frequency. However, the large power consumption makes it unattractive for single-phase power conversion schemes, such as the one we are targeting for the CPU power supply design in portable devices.

Table 1.2 summarizes the comparison between the analog and digital filter implementations. It clearly motivates the need for a filter that can be fully-integrated, is programmable and dissipates moderate amount of power without significantly degrading the transient

Table 1.2: Comparison of linear PWM Buck Converter control schemes

Performance Metric	***Analog***	***Digital***
Area	High[$]	Moderate
Filter Variability	High[$]	Low
Degrees of Freedom	Low	High
Frequency Scalability	None	High
DC Regulation Accuracy	Good	Good[¥]
Transient Response	Average	Average[¥]
Power Consumption	Moderate	High[¥]
Monolithic Solution	No	Yes

[$] Assuming fully-integrated RC components for the Analog Filter.

[¥] Digital Filter requires much higher power to achieve a DC and transient performance comparable to the Analog Filter.

performance (choose all yellow boxes).

To achieve this goal, we have considered various integrated filter implementation schemes, and they can be mainly be categorized in the following ways:

1. Active-RC Filter

   The continuous-time Active-RC Filter (ARCF) uses resistors (R) and capacitors (C) to implement the filter transfer function. Typically, an active element (amplifier) is required to realize the signal amplification in the filter. In addition, the active element can be used for realizing high-Q filters, by emulating inductors or negative resistances on-chip via feedback mechanisms. The advantages of ARCF are very high linearity due to use of highly linear on-chip RC elements, low noise performance and as a result, a very high dynamic range. This is indeed true for the filter implementation as shown in Fig. 1.9. However, as discussed, this filter suffers from large on-chip variations requiring

extensive trimming for static process variations. For dynamic variations w.r.t. temperature and voltage shifts, typically on-line or off-line calibration is required which is hard to achieve in this case.

Another possibility is to implement resistors using MOS transistors operating in triode region, and controlling their resistance via their gate voltages. This approach opens up the possibility of calibration for dynamic variations, but the linearity (and hence dynamic range) is poor due to the large dependence of MOS resistance on the common-mode operating voltage.

2. G_m-C Filter

The ARCF concept can directly be extended to the G_m-C Filter (G_mCF) approach by implementing the resistors using on-chip transconductance (G_m) elements. The G_m block can be implemented either by directly using MOS transistors biased in saturation region, or using an MOS- or Bipolar-input based Operational Transconductance Amplifier (OTA), depending on the input/output impedance requirements. The G_mCF have the advantage over ARCF that they can be made scalable by using a control voltage or current. Thus, G_mCF can possibly be compensated for both static and dynamic process variations via closed-loop compensation. Such a principle is known as automatic tuning, and two methods of achieving the same are shown in Figs. 1.12 and 1.13.

Fig. 1.12 illustrates the indirect tuning mechanism for automatic tuning. Essentially, the main filter is *indirectly* tuned to achieve the desired frequency response, while an auxiliary circuit is being *directly* tuned via a closed-loop mechanism. It is important to understand that the various circuit elements in both the main filter and the auxiliary block

are closely matched on-chip. The auxiliary can either be a Voltage-Controlled Filter (VCF) (in Fig. 1.13a) or a Voltage-Controlled Oscillator (VCO) (in Fig. 1.13b) which is being tuned to an off-chip stable reference frequency (f_{REF}) via a control signal (V_{CTRL}). V_{CTRL} is typically a low-pass filtered version of the output of the Phase Detector and it closes the auxiliary tuning loop. If these filtering requirements necessitate large components and need to be placed off-chip, it defeats the purpose of this work.

The choice of f_{REF} is typically based on the characteristics of the VCF, and it should have high gain sensitivity w.r.t. the quantity being compared (phase or magnitude) for locking the loop. Now, V_{CTRL} contains harmonics (or spurs) of f_{REF} since no realistic low-pass filtering can ensure infinite attenuation. These harmonics can potentially impact the performance of the main filter, especially if it has high sensitivity at $N \times f_{REF}$. Thus, ideally, the main filter should have zero sensitivity at f_{REF} and its harmonics, while the VCF should be quite the opposite. Keeping our reference Type-III filter under consideration, ensuring the above by design is not an obvious or straightforward proposition.

Fig. 1.13 illustrates the direct tuning mechanism for automatic tuning. The tuning mechanism is similar to the VCF based tuning described above and a reference generator is still required. The advantage of this scheme is that the necessity for matching between the main filter and auxiliary circuit is completely eliminated, and hence better accuracy can be guaranteed. However, a replica filter is still required which is being tuned when the main filter is operational, and vice versa. This is done in order to prevent any interruptions in the signal processing. Thus, care must be taken to minimize switching

transients when the tuning circuit is being switched from one filter to the other. This makes the direct tuning mechanism rather unattractive, especially for the application under consideration, where closed-loop control (and stability) is required.

It must be understood that the automatic tuning mechanisms have their performance limitations in all the aforementioned schemes. In an example case, a G_mCF employing *indirect* automatic tuning will have the following drawbacks:

a. Limited linearity and linear scalability of the filter transfer function across PVT variations.
b. Issues related to automatic tuning to compensate for filter variability:
    i. An external, stable reference frequency generator is required leading to area and cost overhead.
    ii. Extra on-chip processing circuitry is required in addition to the main filter, leading to area and power overhead.
    iii. Filter accuracy is limited by imperfect device matching of elements present in the main filter and the auxiliary circuit. In addition, it is not simplistic to guarantee exactly the same operating conditions of the matched elements being tuned in the auxiliary; and the main filter.
    iv. The tuning circuit's non-idealities can lead to the performance degradation of the main filter. As a result, the design complexity of the main filter may increase. Another consequence could be the placement of tuning circuit's loop filter off-chip, which is highly undesirable.

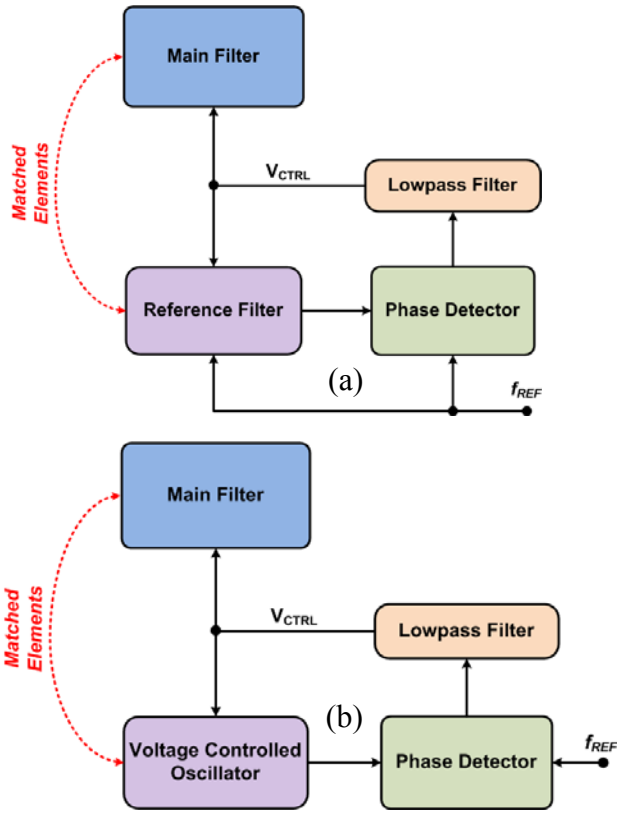


Figure 1.12: Indirect automatic tuning schemes using (a) VCF and (b) VCO.

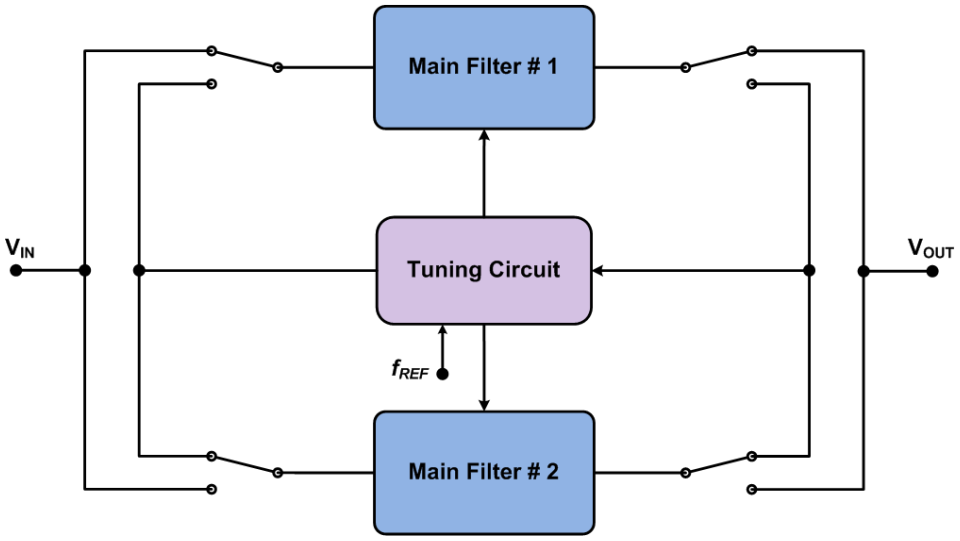


Figure 1.13: Direct automatic tuning scheme with no interruption in processing.

3. Switched-Capacitor Filter

Switched-Capacitor Filters (SCFs) are essentially sampled-data filters, and much like G_mCF, can be derived from their ARCF counterparts by replacing the resistors by an "equivalent" switching capacitor. It must be understood that the resistor approximation is only valid for frequencies much lower than the sampling rate of the SCF, and high frequency effects can introduce filter distortion. Thus, SCF is not the preferred solution for high frequency (> 10 MHz signal bandwidth) applications, since very high clock rates are required to ensure a given oversampling ratio for accurate filter realization. Now, since the filter is sampling the input signal, care needs to be taken to ensure that no aliasing distortion occurs in the filter. In addition, there can be inherent sampling delay in the SCF architecture, which is highly undesirable in a closed-loop control application. These effects make SCF the most difficult to synthesize out of the three aforementioned filters for the application under consideration.

However, the SCFs present an important benefit of very low on-chip variability (< 1 %), being highly tolerant w.r.t. both static and dynamic variations, completely eliminating the need for any trimming or tuning. The only requirement is the trimming of the sampling clock, which is generally ensured by default in most contemporary ICs, and hence is not truly a design overhead. The linearity of the filter is high if highly-linear capacitors are employed, while the dynamic range gets limited mainly by the thermal noise aliasing (inside the Nyquist Bandwidth) and charge injection/clock feedthrough effects.

Table 1.3: Comparison of various active filter topologies

Performance Metric	***ARCF***	***G_mCF***	***SCF***
Filter Variability	High	Moderate/High	Low
Compensation for variability	Extensive Trimming	Trimming/ Automatic Tuning	Clock Trimming
Linear Scalability	None	Low/Moderate	High
Noise	Low	Low/Moderate	High
Linearity	High	Low/Moderate	Moderate/High
Dynamic Range	High	Moderate	Moderate
Frequency Limits	High	Medium/High	Medium

To conclude, while there does not exist a perfect integrated filter topology, the SCF has the important advantages of being linearly scalable (with clock/sampling frequency), ensuring low on-chip variability w.r.t. PVT variations, without the need for any trimming or automatic tuning circuitry. In addition, SCF is well suited for medium-frequency and moderate dynamic range applications, such as the one under consideration. The summary and comparison matrix for all the aforementioned filters is described in Table 1.3.

1.3 Key Contributions

In this dissertation, we have made the following key contributions:

1. We have explored a novel paradigm involving the synthesis of sampled-data (discrete-time) integrated analog filter based Type-III compensation for voltage-mode control of fixed-frequency switched-mode Buck converters.

2. We have laid the theoretical foundations for the design of such a filter using a switched-capacitor filter embodiment. Potentially, the theory can be easily extended to other sampled-data (discrete-time) analog filter embodiments as well.
3. We designed an integrated circuit prototype of the filter and were able to validate the proposed theory via both time- and frequency-domain experiments.
4. In simulations, we observed that the analog (continuous-time) and the proposed (discrete-time) filters result in negligible difference in the closed-loop transient response, once designed to have near-similar open-loop frequency responses.
5. We have observed that the proposed filter can combine the benefits of conventional analog and digital Type-III filter implementations, and has the potential to outperform them in the future.
6. While the proposed filter is designed for a switched-mode Buck Converter employing linear PWM control, the fundamentals developed can be extended to other power converter topologies and control schemes as well.

1.4 Organization of the Dissertation

This dissertation has been organized as follows: In Chapter 2, we will discuss the basic Switched-Capacitor Filter (SCF) theory. In Chapter 3, the frequency response for the target filter will be evaluated for an example 1 MHz Buck converter design, using the conventional analog filter. In Chapter 4, the theoretical challenges concerning the SCF-based Type-III filter realization are discussed, and a fully-integrated frequency scalable architecture is arrived at. In Chapter 5, the design/implementation issues with the filter design are

addressed, for a target Texas Instruments' 0.36-μm BCD technology in the temperature range [-40, 125] °C. In Chapter 6, we discuss the issues related to the filter's clocking and interfacing circuitry for PWM control. In Chapter 7, we describe a unified simulation methodology for ascertaining the frequency response of the Type-III SCF and Buck converter in realistic SPICE simulations. We will also compare and discuss the closed-loop transient performance of the analog filter vs. the SCF based Buck converter. In Chapter 8, we present the measurements results from the fabricated integrated circuit prototype. Chapter 9 gives us the conclusions and future work.

Chapter 2

2. Basics of Switched-Capacitor Circuits

2.1 Simplest Switched-Capacitor Network

A basic switching capacitor circuit is shown in Fig. 2.1. The non-overlapping phase switches, Φ_1 and Φ_2, are derived from a Clock of time period 'T'. The capacitor C_1 is charged by the input voltage source V_{IN} during Φ_1, until $t = NT - \tau$. Here, 'τ' represents an infinitesimally small time period before the clock falling edge before which Φ_1 opens and C_1 stops charging. Again, at the clock edge at $t = NT$, Φ_2 closes and C_1 shares charge with C_2 until $t = NT + T/2 - \tau$. In the next half clock cycle, the capacitor C_1 again recharges back to V_{IN} at $t = NT + T - \tau$. Here, if we assume that V_{IN} has much smaller bandwidth compared to the clock frequency, and $C_2 >> C_1$, we can say:

$$Q_{C1}(t = NT - \tau) = Q_{C1}(t = NT + T - \tau) = C_1 V_{IN}$$

$$Q_{C1}(t = NT + \frac{T}{2} - \tau) = C_1 V_{OUT}$$

The average amount of charge that flows from the input source V_{IN} in one clock cycle (T) is given as:

$$\Delta Q_{AVG} = Q_{C1}(t = NT + T - \tau) - Q_{C1}(t = NT + \frac{T}{2} - \tau)$$

$$\Rightarrow \Delta Q_{AVG} = C_1 \times (V_{IN} - V_{OUT}) \qquad (2.1)$$

Thus, the average current flowing through the network is given as:

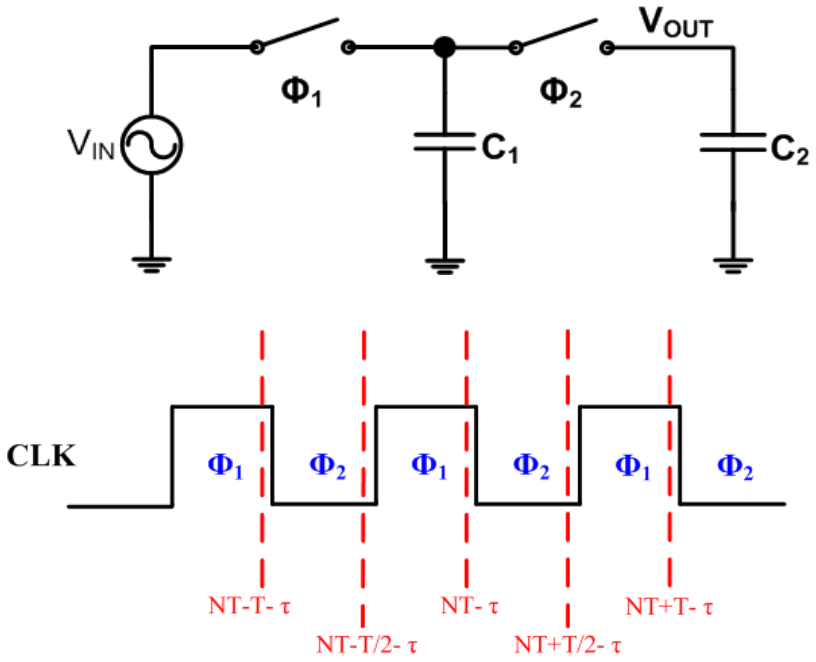


Figure 2.1: A basic switched-capacitor network with associated clock phases.

$$I_{AVG} = \frac{\Delta Q_{AVG}}{T} = \frac{C_1}{T} \times \left(V_{IN} - V_{OUT}\right) \tag{2.2}$$

We can thus write the equivalent network impedance at low frequency (since we have only calculated the average current):

$$Z_{EQ} = \frac{V_{IN} - V_{OUT}}{I_{AVG}} = \frac{T}{C_1} = \frac{1}{f_S C_1} = R_{EQ} \tag{2.3}$$

Hence, at frequencies much lower that the sampling frequency (f_S), a switching capacitor emulates a resistor, given by R_{EQ}. This is indeed the fundamental concept behind low-frequency architectures such as the charge-pumps for integrated power conversion [4]. In addition, by choosing a low f_S, it is possible to integrate on-chip resistors with very large

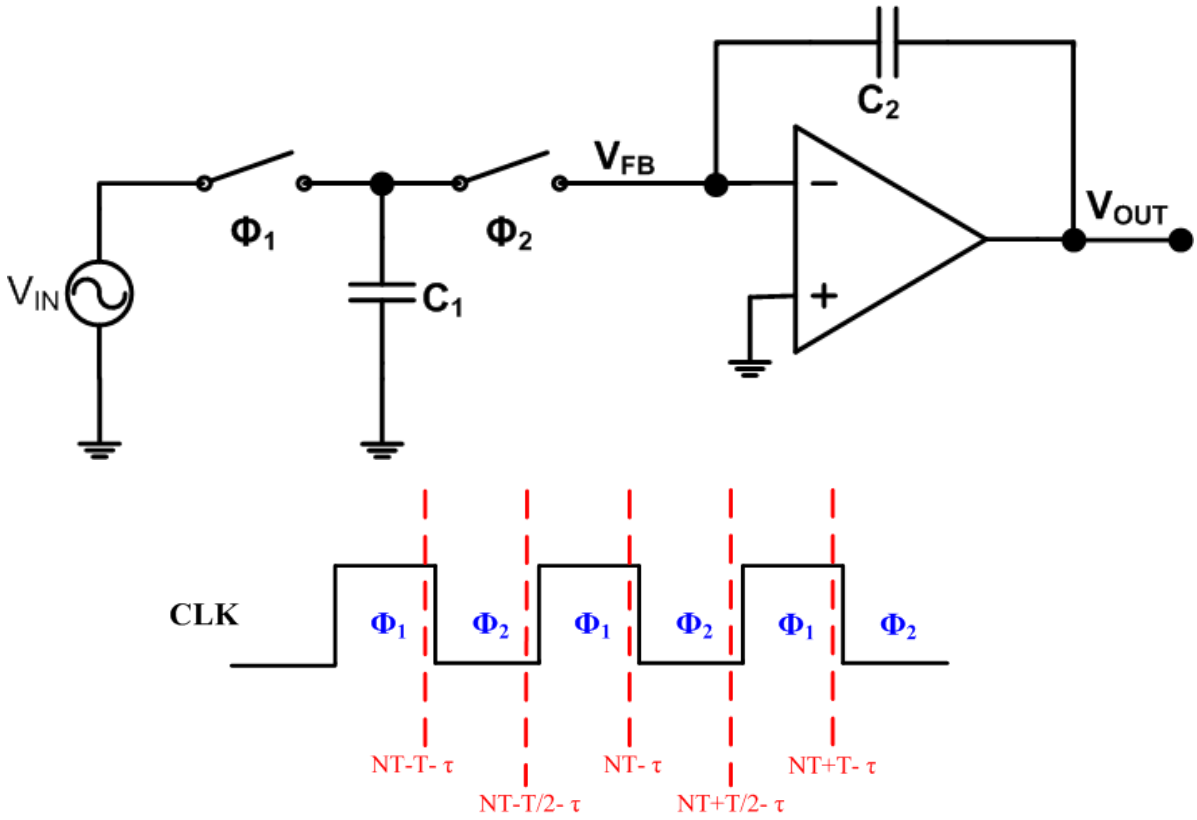


Figure 2.2: A basic switched-capacitor integrator with associated clock phases.

values (> 1 MΩ) using reasonable capacitance values (~ pF) [18].

2.2 Switched-Capacitor Time-Constant Properties

Now, if the voltage node V_{OUT} (Fig. 2.1) is connected to the feedback node of an amplifier (V_{FB}) with capacitive-feedback, we arrive at a basic inverting integrator (Fig. 2.2). This integrator is indeed the building block numerous filter realizations in the discrete-time domain [16], [18]. Assuming, low input signal frequency compared to f_{CLK}, and hence a large Over-Sampling Ratio ($OSR > 10$), we can assume that the switched-capacitor is indeed a resistor. Hence, the integrator time constant is given as:

$$\tau = R_{EQ}C_2 = \frac{1}{f_S} \times \frac{C_2}{C_1} = T \times \frac{C_2}{C_1} \tag{2.4}$$

Differentiating (2.4) we get,

$$\frac{\Delta\tau}{\tau} = \frac{\Delta T}{T} + \frac{\Delta C_2}{C_2} - \frac{\Delta C_1}{C_1} \tag{2.5}$$

From (2.4) and (2.5) we can arrive at two extremely significant results:

1. Frequency Scalability of Time-Constants

   From (2.4), it can be seen that the time constant is directly proportional to the sampling/clock period. This essentially means that if the filter clock is a derived version of the switching converter's clock, the realized filter would be a fundamentally frequency-scalable.

2. Low on-chip variability of Time-Constants

   From (2.5), it can seen that absolute variability of the time constant (τ) is a function of the absolute variability of the clock period (T) and relative mismatch of capacitors C_1 and C_2. Now, the clock frequency of a fixed-frequency control based switching converter is already trimmed to be highly accurate (< 1 %). In addition, while the absolute inaccuracies of capacitors ($\Delta C/C$) is large (~ 20 %) with Process/Temperature variations, the relative mismatches between capacitors can be made extremely small (< 1 %) [16]. The total inaccuracy of this time constant is significantly lower than that of a simple Active-RC integrator (~ 40 %), and thus a fully-integrated trimless filter design is possible.

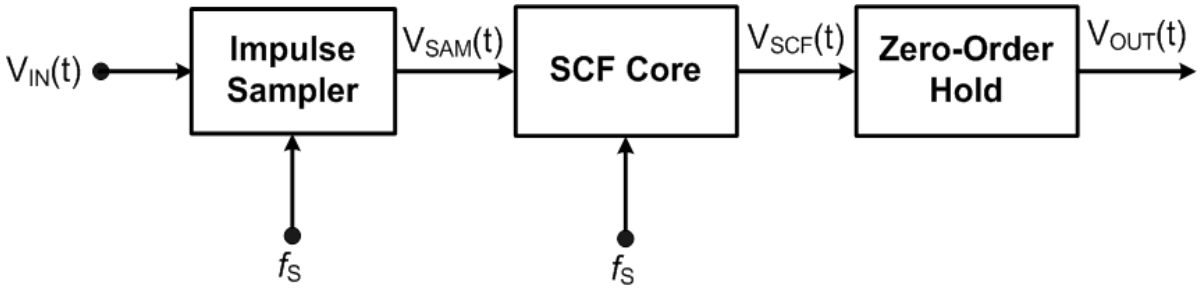


Figure 2.3: Block-diagram showing the signal processing concept in SCF.

As a conclusion, at the outset, it seems feasible to conceive fully-integrated, frequency-scalable switched-capacitor filter architecture. However, till now, we have only considered the low-frequency behavior of the switched-capacitor networks and it is not sufficient to understand the complete filter response at high-frequencies. These will be discussed in the following two sub-sections.

2.3 Switched-Capacitor Filter Theory

The Switched-Capacitor Filter (SCF) concept is shown in Fig. 2.3, in a constant-rate signal processing system. The analog input signal (V_{IN}) is sampled by an impulse train at a given sampling frequency (f_S) to generate a discrete-time signal V_{SAM}. This signal is then "morphed" by the impulse response of the SCF core to generate V_{SCF}. This signal, still in discrete-time domain, is converted back to continuous-time domain by a Zero-Order Hold (ZOH) function to generate the final staircase-resembling output signal, V_{OUT}.

Fig. 2.4 shows the frequency-domain representation of the signal processing that takes place in Fig. 2.3. The input signal is assumed to be band-limited with a bandwidth of f_B. The impulse sampler samples the input at a rate $f_S > f_B$, represented by a periodic impulse

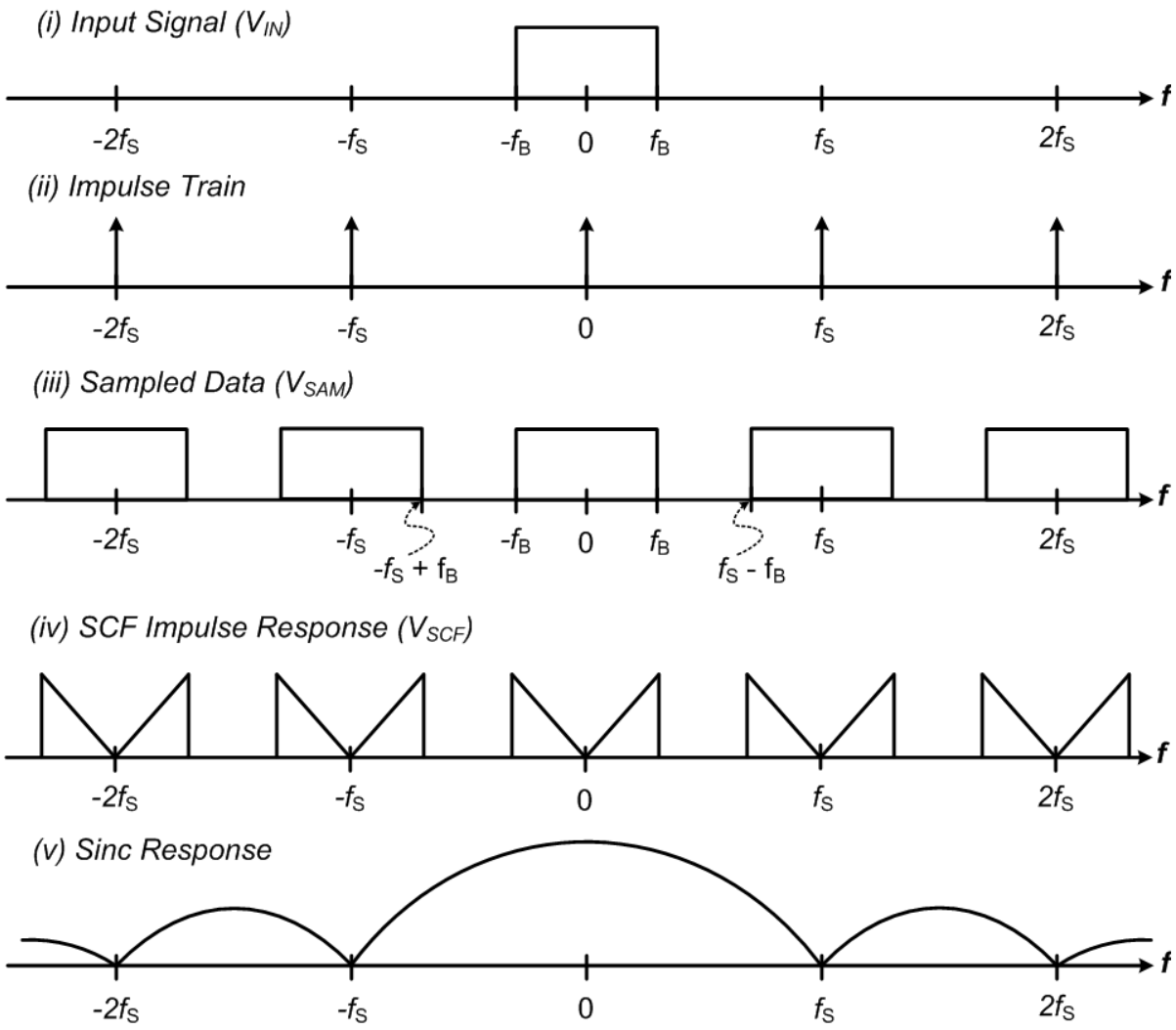


Figure 2.4: Frequency-domain representation of the signal processing in Fig. 2.3.

train. These impulses multiply with the input signal in time-domain and convolve in the frequency-domain to generate a periodic spectrum of sampled data (V_{SAM}) [16]. At this point, it is important to note that $f_S - f_B > f_B$, else the adjacent spectra would merge and lead to aliasing distortion. Once this distortion takes place, it is difficult to reconstruct the original signal using conventional schemes. In addition, any further signal processing on this data

would result in erroneous outputs. Hence, for a given f_S, the maximum allowable input signal bandwidth is $f_S/2$. This is also known as the *Nyquist Bandwidth*. Thereafter, the signal is processed by a discrete-time calculator (SCF Core Block in Fig. 2.3), which constructs new output samples based on the information contained in current/previous input/output signal samples. In Fig. 2.4, we have depicted a high-/band-pass SCF response. Finally, the ZOH essentially performs a time-domain convolution of V_{SCF} with a unit-step function at the same frequency, f_S. The frequency-response of the unit-step function is a sinc function, which has nulls at multiples of sampling frequency, f_S. Finally, the spectrum of V_{OUT} is a superposition of the V_{SCF} and sinc frequency response as shown in Fig. 2.4.

We will now briefly discuss the Anti-Aliasing Filter (AAF) design requirements based on the concept of Nyquist Bandwidth ($f_S/2$). From Fig. 2.4, we can conclude that an ideal AAF would limit the input signal (V_{IN}) to $f_B < f_S/2$, and any higher-frequency content would be rejected with infinite attenuation. Now, these are clearly impractical design specifications for the AAF, which can never be met. Instead, a more practical design specification for the AAF is that V_{IN} is limited within the Nyquist Bandwidth in such a way that the Signal-to-Noise Ratio (SNR) is > 40 dB. Here, noise refers to all unwanted signals that are present both in-band and out-of-band. In-band noise is dominated by the thermal and flicker noise present in MOS devices, while out-of-band noise is dominated by the high-frequency switching noise present on-chip. Finally, it must be understood that while the sinc function has a low-pass characteristic (notches at multiples of f_S), it cannot aid in meeting the AAF requirements for the SCF sampler. This is due to the fact that the input signal sampling has already taken place before the signal goes through the ZOH (see Fig. 2.3).

2.4 s-z Transformation Methods

In Section 2.2, we arrived at the Switched-Capacitor Integrator (SCI) time constant in Eq. (1.9), by the resistor approximation of a switched-capacitor. However, as we learnt in Section 2.3, the SCI's frequency response cannot be appropriately represented using the analog frequency variable '*s*' (see Fig. 2.4). This is essentially due to the fact that the input signal undergoes sampling and hence another variable '*z*' is introduced [16]. The two variables are related as follows:

$$z = e^{sT} = e^{\frac{s}{fs}} \tag{2.6}$$

Here, '*T*' is the sampling interval and f_S thus the sampling frequency. The mathematical derivation can simply be obtained from the Laplace Transform of the impulse sampling operation in time-domain [16]. In order to compute the frequency response, we replace the variable '*s*' by '$j\omega_d$', which is the discrete-time frequency variable. Hence,

$$z = e^{j\omega_d T} = e^{j2\pi T f_d} = e^{j2\pi\frac{f_d}{f_s}} = e^{j2\pi\frac{f_d + nf_s}{f_s}} \tag{2.7}$$

where, '*n*' is an integer. Eqn. (13) gives us a very important result. The discrete-time filter's frequency response would be periodic with f_S. This is indeed depicted in the traces (iii) and (iv) of Fig. 2.4.

At this point, we must discuss the possible ways for a Discrete-Time Filter (DTF) synthesis. One way to synthesize the DTF is from the Continuous-Time Filters (CTF). Traditionally, there has existed significant knowledge in the CTF theory, and it is intuitive to realize a DTF as a derivative of the same. For this, we must derive a mapping between the 's'

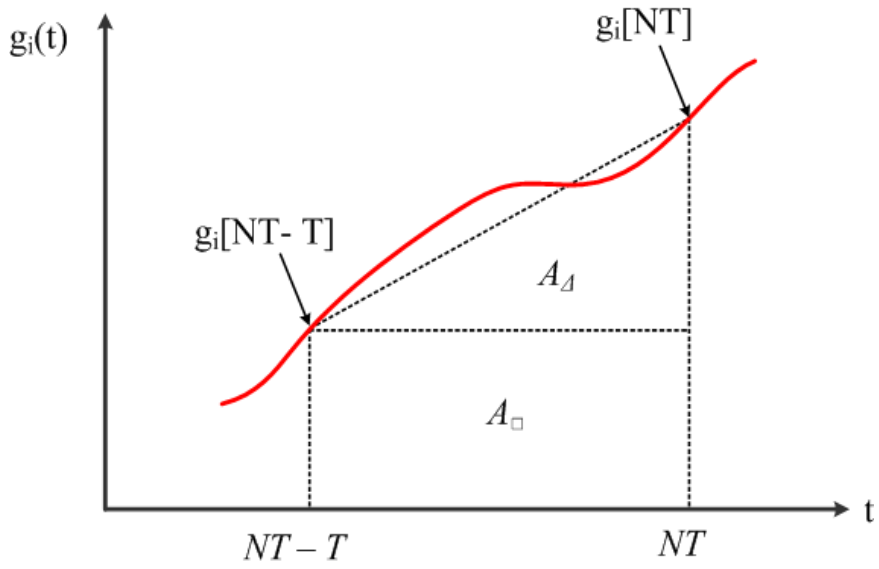


Figure 2.5: Figure showing the area under the curve using Trapezoidal Integration.

and 'z' planes. The only constraints that exist are that mapping function must be rational and it should ensure the stability criteria when transforming from one plane to the other [16].

In basic circuit theory, a CTF can be treated as a Linear Time-Invariant (LTI) system which can be represented by the following set of 1st order differential equations [19]:

$$\frac{dx_i(t)}{dt} = \sum_{j=1}^{N} a_j x_j(t) + \sum_{k=1}^{M} b_k w_k \qquad \forall\, i \in [1, N] \tag{2.8}$$

Here, 'x' is the state variable of the system of order 'N'. There are 'M' excitation sources in the system, and are represented by the scalar 'w'. For example, an LC tank excited by a single voltage source would have $N = 2$ and $M = 1$, and thus its response can be completely analyzed by two 1st order differential equations. Now, it is possible to write Eqn. (2.7) in a more simplistic form [16]:

$$\frac{dx_i(t)}{dt} = g_i(t) \tag{2.9}$$

Taking the definite integral of (2.8) in one sampling period from $NT - T$ to NT, we get,

$$x_i[NT] - x_i[NT - T] = \int_{NT-T}^{NT} g_i(t)dt \tag{2.10}$$

Now, the RHS can be evaluated using various numerical integration methods to calculate the area under the curve. We will consider the Trapezoidal Integration Method, which is one of the most accurate methods known for numerical computation. In this method, the curve is approximated by a straight line (Fig. 2.5) and hence the area is just a sum of the triangle and the rectangle and can be given by:

$$\int_{NT-T}^{NT} g_i(t)dt = \frac{T}{2}\left(g_i[NT] + g_i[NT - T]\right)$$

$$\therefore x_i[NT] - x_i[NT - T] = \frac{T}{2}\left(g_i[NT] + g_i[NT - T]\right) \tag{2.11}$$

Taking the z-transform of the above difference equation, we get,

$$\left(1 - z^{-1}\right)X_i(z) = \frac{T}{2}\left(1 + z^{-1}\right)G_i(z) \tag{2.12}$$

Now, taking the Laplace Transform of Eqn. (2.8) in the analog domain, we get,

$$s_a \times X_i(s_a) = G_i(s_a) \tag{2.13}$$

Thus, by comparing Eqns. (2.11) and (2.12), we can arrive at the following relation in the analog and discrete-time domain variables:

Table 2.1: Various s-z transformation methods

Integration Scheme	s-z Mapping
Forward Euler	$s_a = \frac{1}{T} \times \frac{1 - z^{-1}}{z^{-1}}$
Backward Euler	$s_a = \frac{1}{T} \times \left(1 - z^{-1}\right)$
Mid-point (Lossless Discrete Integration)	$s_a = \frac{1}{2T} \times \left(z - z^{-1}\right)$
Trapezoidal (Bi-Linear Transformation)	$s_a = \frac{2}{T} \times \frac{1 - z^{-1}}{1 + z^{-1}}$

$$s_a = \frac{2}{T} \times \frac{1 - z^{-1}}{1 + z^{-1}} \tag{2.14}$$

The above s-z mapping is also known as the Bi-Linear Transformation (BLT). Now, we can equate $s_a = j\omega_a$ and $z = exp(j\omega_d T)$ for a relation between analog and discrete-time frequencies:

$$j\omega_a = \frac{2}{T} \times \frac{1 - e^{-j\omega_d T}}{1 + e^{-j\omega_d T}} = \frac{2}{T} \times \frac{e^{+j\omega_d \frac{T}{2}} - e^{-j\omega_d \frac{T}{2}}}{e^{+j\omega_d \frac{T}{2}} + e^{-j\omega_d \frac{T}{2}}} = j\frac{2}{T} \times \tan\left(\frac{\omega_d T}{2}\right)$$

$$\therefore \omega_a = \frac{2}{T} \times \tan\left(\frac{\omega_d T}{2}\right) \tag{2.15}$$

The above equation has a very significant implication. It can be seen that all analog frequencies in the range (-∞, 0] can be mapped onto the unit circle of discrete-time

frequencies in the range (-π, 0]. Thus, theoretically speaking, it should be possible to realize any pole/zero with the frequency ranging from DC to $f_S/2$.

Another interesting result can be observed for low discrete-time frequencies and hence high-OSR. i.e. $\omega_d << 2/T$. In that case, $\omega_a \sim \omega_d$, and hence there is little difference between the analog and discrete-time frequency response. An intuitive explanation of the above phenomenon can be explained by Fig. 2.5. It can be seen that if the sampling period '*T*' is decreased for a given signal bandwidth (and hence increased *OSR*), the approximation would become more accurate. This low-frequency result is indeed valid for all the other s-z transformations as well (see Table 2.1). It is left as an exercise for the reader to conclude that the SCI circuit in Fig. 2.2 is an embodiment of the Forward-Euler s-z transformation scheme. With these fundamentals in mind, we can now proceed to designing an SCF for Type-III compensation.

Chapter 3

3. Specifications for the Type-III SCF Design

3.1 Small-signal Response of the Buck Converter

The basic linear PWM-based voltage-mode control of fixed-frequency Buck converters was discussed in Section 1.1 (see Fig. 1.6). For this, any perturbation of the duty cycle (Δd) of the switching converter is assumed to have a linear response to its output voltage (Δv_{OUT}). The linearity holds true for frequencies much lower than the switching frequency ($\sim f_{SW}/10$). Fig. 3.1 shows a simplified schematic of the Buck converter, with equal resistances assumed for High-Side (HS) and Low-side (LS) switches, given by R_{SW}.

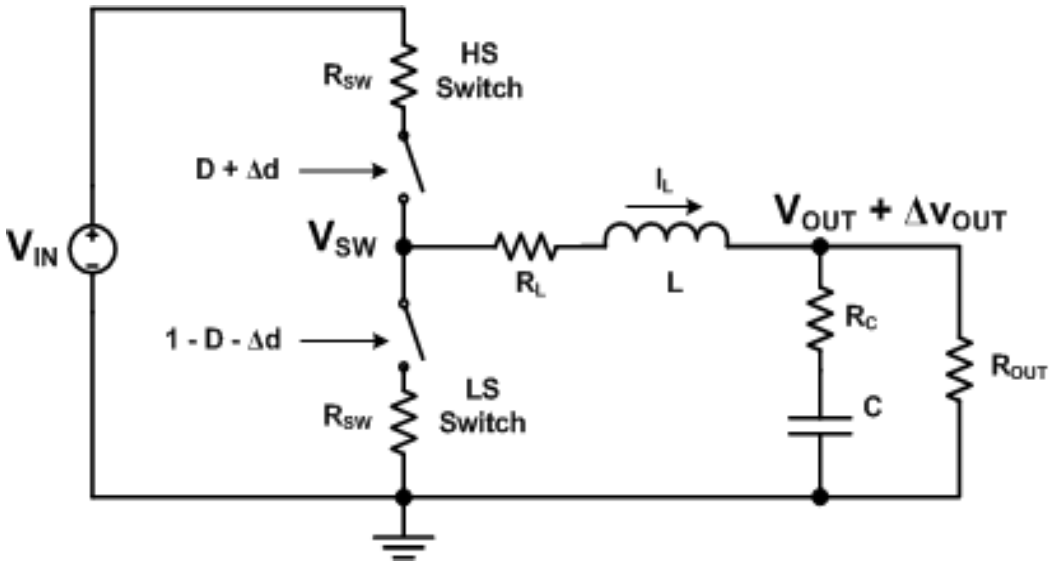


Figure 3.1: Simplified circuit schematic of a switch-mode Buck converter.

The open-loop response of this circuit is well studied, and is given in [6] as:

$$G_{vd}(s) = \frac{\Delta v_{OUT}}{\Delta d} = \left[V_{IN} + (1-2D) \times I_{OUT} R_{SW}\right] \times \frac{(1 + sR_C C)}{1 + \frac{2\zeta s}{\omega_N} + \frac{s^2}{{\omega_N}^2}}$$

$$\omega_N{}^2 = \frac{R_L + D^2 R_{SW} + R_{OUT}}{LC(R_C + R_{OUT})}$$

$$\frac{Q}{\omega_N} = \frac{1}{2\zeta\omega_N} = \frac{LC(R_C + R_{OUT})}{L + C\left[R_C R_{OUT} + (R_C + R_{OUT})(R_L + D^2 R_{SW})\right]}$$

Now, typically, $R_{OUT} >> R_L$, R_C, R_{SW}, to minimize conduction losses for any given load current requirement. Hence, we can simplify the above equations as:

$$\therefore G_{vd}(s) \approx V_{IN} \times \frac{(1 + sR_C C)}{1 + \frac{2\zeta s}{\omega_N} + \frac{s^2}{{\omega_N}^2}} \tag{3.1}$$

$$\omega_N{}^2 \approx \frac{R_{OUT}}{LC(R_C + R_{OUT})} = \frac{1}{LC} \tag{3.2}$$

$$\frac{Q}{\omega_N} \approx \frac{LCR_{OUT}}{L + R_{OUT} C\left[R_C + (R_L + D^2 R_{SW})\right]}$$

Now, substituting 'ω_N' from (23), we get,

$$\therefore Q = \frac{R_{OUT}\sqrt{LC}}{L + R_{OUT} C\left[R_C + (R_L + D^2 R_{SW})\right]} = \frac{\sqrt{LC}}{L/R_{OUT} + C\left[R_C + (R_L + D^2 R_{SW})\right]}$$

In practical converter designs, the following relation between the time constants holds:

$$\frac{L}{R_{OUT}} >> \left[R_C + (R_L + D^2 R_{SW})\right] \times C$$

This is also an indirect consequence of the aforementioned assumption on the various resistances in Fig. 3.1. Hence,

$$Q \approx R_{OUT} \times \sqrt{\frac{C}{L}} \tag{3.3}$$

At this point, we will analyze the Eqns. (3.1) – (3.3) in more detail. From (3.1), we learn that G_{vd} has a 2nd order response, which is intuitive because of the presence of *LC* tank. The natural frequency of oscillation is indeed governed by the *LC* (Eq. (3.2)). The quality factor (*Q*) is directly proportional to the load resistance (R_{OUT}) as seen in Eq. (3.3). This again is intuitive since a light-load condition would result is smallest loss in the *LC* resonant tank, and highest *Q*. Finally, it is important to note that there is a LHP zero present due to the load capacitor ESR, which can potentially result in a phase-boost.

Now, referring to Fig. 1.6, we can see that the compensator output (V_{COMP}) is fed to a comparator which generates the PWM signal containing the duty cycle information for the Buck Converter. Since the duty cycle, *D* lies from [0, 1], the modulator has attenuation equal to the height/amplitude of the sawtooth ramp waveform. Hence, the complete open-loop transfer function (excluding the compensator) is given by:

$$G_T(s) = M(s)G_{vd}(s) = \frac{V_{IN}}{|V_{SAW}|} \times \frac{(1 + sR_C C)}{1 + \frac{2\zeta s}{\omega_N} + \frac{s^2}{\omega_N{}^2}} = \frac{V_{IN}}{|V_{SAW}|} \times G(s) \tag{3.4}$$

Here, *M(s)* is the modulator gain given by $1/|V_{SAW}|$. For the compensator design, for now, we will consider $V_{IN} = |V_{SAW}|$ and hence $G_T(s) = G(s)$. As can be seen from Eq. (3.4), G(s) is largely a function of the various circuit parameters of the Buck converter.

3.2 LC Filter Design

As can be seen in the previous sub-section, the *LC* filter largely dictates the open-loop frequency response of the Buck converter. It must be understood that the primary function of this filter is to attenuate the high-frequency switching content on node V_{SW} and provide a low-ripple DC output voltage (Fig. 3.1). We will first focus on the inductor design. The inductor ripple at a given switching frequency f_{SW} is [6]:

$$\Delta i_L = \frac{1}{2 f_{SW} L} \times D(1-D) \times V_{IN} \tag{3.5}$$

where, '*D*' (= V_{OUT}/V_{IN}) is the steady-state duty cycle of the converter.

The inductor current ripple is generally chosen to be 10 – 20 % of the rated full-load current. The higher the chosen ripple, lower is the inductor value (hence size), but larger the RMS losses in the switches for a given load current. Other considerations include low R_L (for reduced losses) and that $I_L + \Delta i_L$ should have sufficient room below the inductor's saturation level.

Now we shall focus on the output capacitor design. Note that in Figs. 1.6 and 3.1, we have ignored the capacitor ESL. This is due to the fact that ceramic capacitors are chosen for low EMI and footprint requirements. Now, we assume that the inductor DC current flows through the load resistance, while the higher frequency ripple current flows through the output capacitor. While the capacitor integrates this ripple current, its ESR will directly reflect it on top of the output voltage. Hence, minimizing R_C is an important consideration while choosing the output capacitor. The total output voltage ripple is given by [6]:

$$\Delta v_{OUT} = \Delta v_{OUT,C} + \Delta v_{OUT,ESR}$$

Table 3.1: Power-Stage design for Buck Converter at f_{SW} = 1 MHz

Switching Frequency (f_{SW})	1 MHz
Input Voltage (V_{IN})	3.3 V
Output Voltage (V_{OUT})	1.0 V
Full-Load Current (I_{OUT})	1.5 A
Inductor (L/R_L)	1 μH/10 mΩ
Capacitor (C/R_C)	30 μF/5 mΩ
Double-Pole Frequency (f_{LC})	29 KHz
ESR Zero Frequency (f_{ESR})	1 MHz

$$\Rightarrow \Delta v_{OUT} = \frac{\Delta i_L}{8 f_{SW} C} + R_C \Delta i_L \tag{3.6}$$

We can thus calculate a range of realistic L, C and R_C values from the ripple requirements and the switching frequency from Eqns. (3.5) and (3.6).

3.3 Type-III Analog Compensator Design

We described the basic Type-III filter transfer function in Eq. (1.6) in Section 1.2. However, we first need to ascertain the open-loop Buck converter transfer function as given in Eqns. (3.1) – (3.4). For this, we can simply pick a reference design for our target application, such as the one in [7].

In [7], an output voltage (V_{OUT}) of 1.5 V is provided for a full-load current rating of 1.5 A (I_{OUT}) from an input voltage (V_{IN}) in the range 2.9 – 6 V. The Buck converter switches at a nominal frequency of f_{SW} = 1 MHz and has a fully-integrated driver and MOSFET design. At this point, we will consider a nominal input voltage of 3.3 V (V_{IN}), to ease our LC filter and hence the compensator design complexity. The LC filter design is done

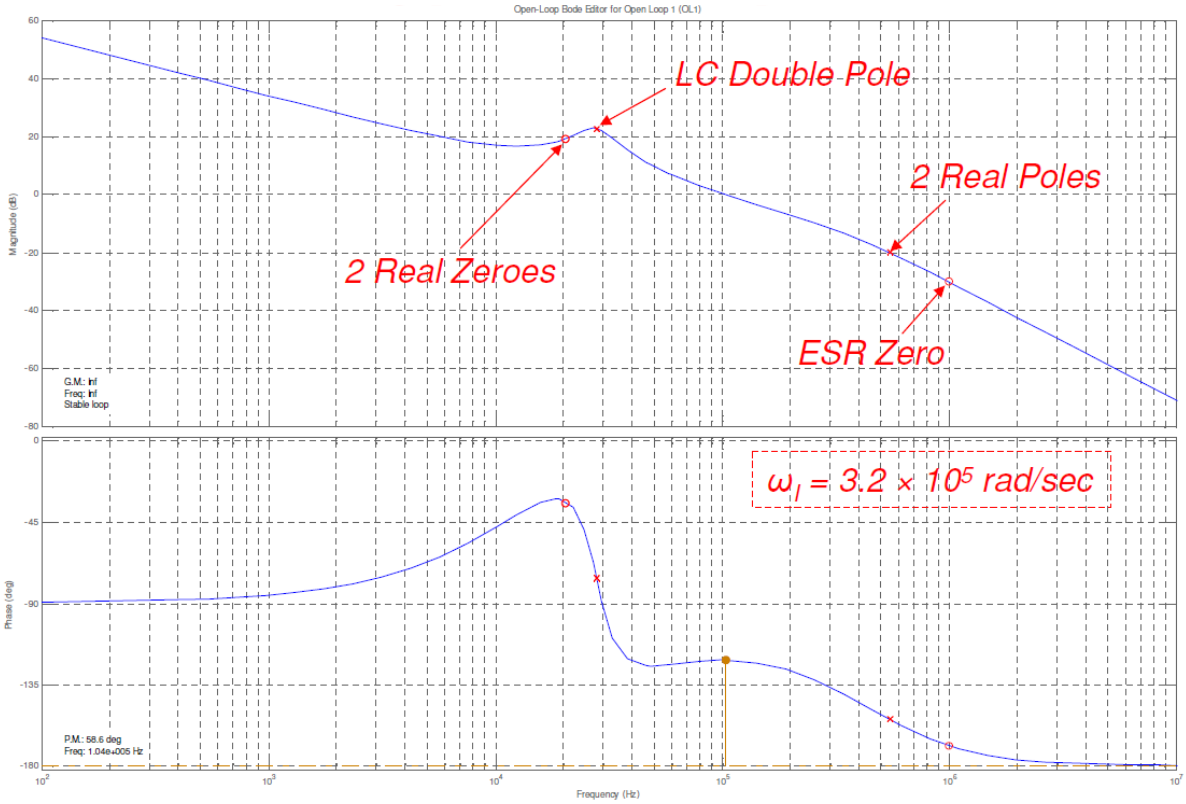


Figure 3.2: Snapshot of the sisotool showing complete open-loop response of Buck converter with Type-III compensation.

for 10 % current and < 1 % voltage ripple requirements, using Eqns. (3.5) and (3.6). Table 3.1 summarizes the power-stage design.

With the above information, it is possible to design a Type-III filter compensation for a closed-loop Unity-Gain Bandwidth (f_{UGB}) of $f_{SW}/10$ (~ 100 KHz). This can easily be done using the visual interface (sisotool) provided the MATLAB as a part of the Control Systems Toolbox [20]. It can be seen from Fig. 3.2 that a closed-loop bandwidth of 104 KHz is achieved with a phase margin of 58.6°. The LC double pole and ESR zero frequencies are indicated at the frequencies mentioned in Table 3.1. It can be seen that since ESR zero is

Table 3.2: Type-III analog filter components for specifications in Table 3.1

C_1	1.4 nF
C_2	400 pF
C_3	20 pF
R_1	111 Ω
R_2	5.6 KΩ
R_3	14 KΩ

present at a frequency 10 times higher than the closed-loop bandwidth, it has little contribution to the phase margin. In designs where the ESR zero is placed closed to loop bandwidth by employing electrolytic capacitors, Type-II filter (Integrator + one pole/zero pair) based compensation suffices.

Referring to Type-III transfer function in Eq. 1.6, the integrator bandwidth is 50 KHz; the two zeroes are placed at 20 KHz and the two poles at 550 KHz. Corresponding to these filter specifications, the components' values for the Type-III filter in Fig. 1.9 are shown in Table 3.2 for a switching frequency, f_{SW} = 1 MHz.

It is clear to see from Fig. 3.2 that various frequencies (or time constants) for the Type-III filter will scale linearly with f_{LC} to ensure stability. Now, as can be deduced from (3.6), f_{LC} scales linearly with f_{SW} to ensure the same V_{OUT} ripple magnitude, if the capacitor ESR (= R_C) can be neglected for ceramic output capacitors. This is indeed the motivation for designing a Type-III filter in which the various time-constants scale linearly with the switching time-period of the Buck converter. With the design specifications for the reference Type-III filter clear, we can now proceed to the SCF implementation of the same.

Chapter 4

4. Theoretical Considerations for the Type-III SCF Design

4.1 Proposed Strategy

From the discussion in Section 2.1 and 2.2, it is clear that the Type-III SCF cannot be realized simply by replacing resistors by Switched-Capacitor Networks (SCN) in the analog filter of Fig. 1.9. If say, the resistor R_1 was replaced by an SCN, at the instant of switch disconnection, the network would see infinite impedance looking into the left plate of C_1. Hence, no charge sharing (and information) transfer would be possible, rendering the circuit ineffective. This situation also holds true for the resistor R_3, and thus its replacement by an SCN is also not possible.

As a next step, we first "break" the Type-III filter of Fig. 1.9 into an equivalent circuit wherein all the resistors are connected between a driven node, and the feedback node of the amplifier. It must be noted that in Fig. 1.9, only the resistor R_2 satisfies this criterion. Thus, we arrive at the circuit configuration in Fig. 4.1. It must be hereby understood that this sequencing and partitioning of the Type-III transfer function is the most critical step in the synthesis of the proposed Type-III SCF prototype. Thus, we arrive at a cascade of three 1st order filters. The transfer function of this 3-stage filter circuit is given as:

$$H_C(s) = \frac{V_{COMP3}(s)}{V_{OUT}(s)} = H_{C1}(s) \times H_{C2}(s) \times H_{C3}(s) \tag{4.1}$$

The individual transfer functions are given as follows:

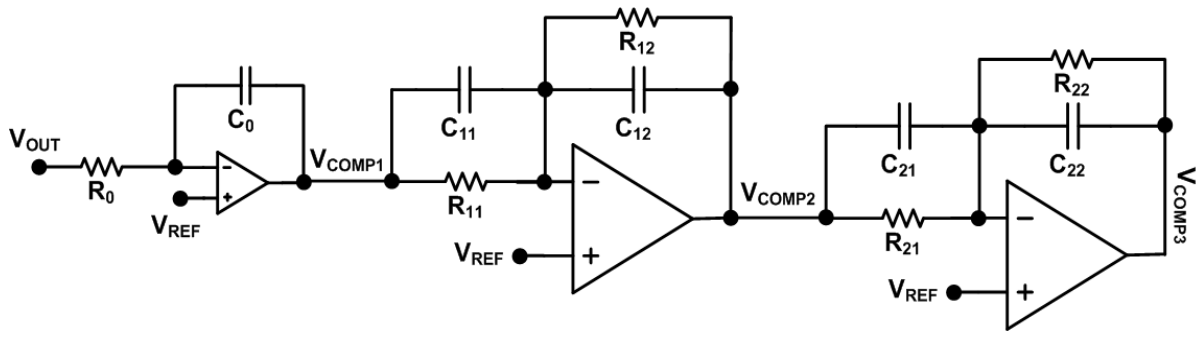


Figure 4.1: Circuit schematic emulating the Type-III filter in Fig. 1.9.

$$H_{C1}(s) = \frac{V_{COMP1}(s)}{V_{OUT}(s)} = -\frac{1}{sR_0C_0} = -\frac{1}{s\tau_0} \tag{4.2}$$

$$H_{C2}(s) = \frac{V_{COMP2}(s)}{V_{COMP1}(s)} = -\frac{R_{12}}{R_{11}} \times \frac{(1+sR_{11}C_{11})}{(1+sR_{12}C_{12})} = -\frac{R_{12}}{R_{11}} \times \frac{(1+s\tau_{11})}{(1+s\tau_{12})} \tag{4.3}$$

$$H_{C3}(s) = \frac{V_{COMP3}(s)}{V_{COMP2}(s)} = -\frac{R_{22}}{R_{21}} \times \frac{(1+sR_{21}C_{21})}{(1+sR_{22}C_{22})} = -\frac{R_{22}}{R_{21}} \times \frac{(1+s\tau_{21})}{(1+s\tau_{22})} \tag{4.4}$$

It can be seen that the 1st stage performs the integration function; while the latter two stages are 1st order high-pass filters. This filter can be used as a reference for any SCF derivatives that might arise out of the same. Based on the design requirements outlined in Section 3.3, the following relations hold:

$$\frac{1}{\tau_0} \times \frac{R_{12}}{R_{11}} \times \frac{R_{22}}{R_{21}} = 2\pi \times 50 \times 10^3 \, rad/s \tag{4.5}$$

$$\frac{1}{\tau_{11}} = \frac{1}{\tau_{21}} = 2\pi \times 20 \times 10^3 \, rad/s \tag{4.6}$$

$$\frac{1}{\tau_{12}} = \frac{1}{\tau_{22}} = 2\pi \times 550 \times 10^3 rad/s \tag{4.7}$$

Now, we can replace each of the resistors by SCNs, to achieve the aforementioned time constants given in Eqns. (4.5) – (4.7). In addition, we shall arrive at fully-integrated frequency-scalable filter architecture, based on the discussion in Section 2.2. However, before we do that, we need to understand the impact of the choice of sampling rate for the filter which is critical for the synthesis of this Type-III switched-capacitor filter.

4.2 Tradeoffs in choice of Sampling Frequency (f_S)

As we learnt in Section 2.4, by increasing the clock frequency (and hence the sampling rate) in an SCF, its *OSR* is increased for an input signal of fixed bandwidth. This has a direct benefit of the ease of the desired filter realization since the approximation becomes more accurate. In addition, as could be seen from Fig. 2.4 in Section 2.3, it would also ease-up the design requirements for the Anti-Aliasing Filter (AAF).

However, increasing f_{CLK} (and hence f_S) has its disadvantages as well. An expression for the switched-capacitor time constant (τ) was derived in Eq. (2.4) in Section 2.2. We shall rewrite it here for convenience:

$$\tau = R_{EQ}C_2 = \frac{1}{f_S} \times \frac{C_2}{C_1} = T \times \frac{C_2}{C_1}$$

It can be seen that increasing f_S would result in a larger capacitor spread (= C_2/C_1) and hence increased area. In addition, with a faster clock and higher capacitance to drive, the amplifier would need much higher bandwidth (and hence power) to fulfill its faster settling requirements [21]. In addition, the switches need to made larger for faster switching speeds.

This degrades accuracy and injects noise (clock feedthrough and charge injection) into the SCF. Finally, a faster clock would consume higher dynamic switching power and would require sophisticated circuitry for jitter control.

To conclude, a high-speed clock is clearly a power, area and noise penalty for the filter. However, if a low-frequency clock is chosen, the concerns regarding accurate filter transfer function realization and prevention of aliasing distortion need to be taken care of. We will try to tackle these issues in the next two sub-sections.

4.3 Bi-Linear Transformation (BLT)

In Section 2.4, we learnt the following relationship between the analog and discrete-time frequency domains when using the Bi-Linear s-z Transformation.

$$\omega_a = \frac{2}{T} \times \tan\left(\frac{\omega_d T}{2}\right) = 2 f_S \times \tan\left(\frac{\omega_d}{2 f_S}\right)$$

$$\Rightarrow f_a = \frac{1}{\pi T} \times \tan\left(\pi f_d T\right) = \frac{f_S}{\pi} \times \tan\left(\frac{\pi f_d}{f_S}\right) \qquad (4.8)$$

Now, we also learnt that it is possible to realize any pole/zero frequency using BLT (in the discrete domain) in the range $[0, f_S/2)$. Hence, it is clear by examining Eqns. (4.5) – (4.7) that the pole frequencies of 550 KHz given by (4.7) would be the limiting factor in choosing the sampling rate.

Now, it would seem reasonable to choose a sampling rate (f_S) of 2 MHz to realize this aforementioned pole frequency. Indeed this is the minimum realistic f_S that can be targeted, and should result in the most power and area efficient solution. However, with an OSR < 4

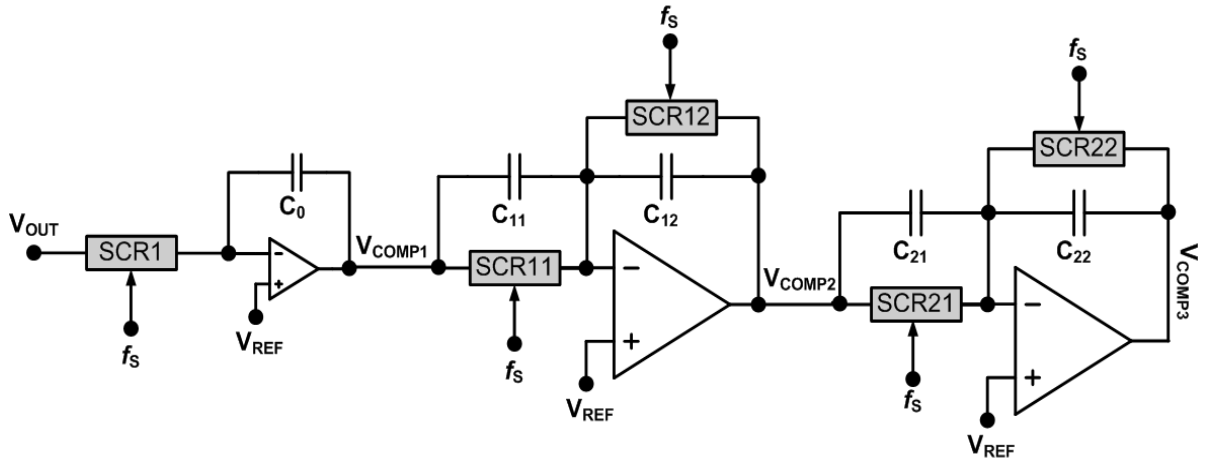


Figure 4.2: Switched-capacitor derivative of the analog filter shown in Fig. 4.1.

for the highest frequency pole, the reference analog filter frequency (f_a) would need to be pre-warped. As can be seen from Eq. (4.8), with f_d = 550 KHz and f_S = 2 MHz, the corresponding f_a = 745 KHz. It must be understood that the pole/zero frequencies in Eqns. (4.5) and (4.6) do not need any pre-warping since their OSR > 40. Finally, we must add that we have only chosen the sampling rate (f_S) which may or may not be equal to the clock frequency (f_{CLK}). This is because it is largely dependent on the circuit-level synthesis of every resistor (in Fig. 4.1) by a Switched-Capacitor Resistor (SCR), which will be discussed in detail in Chapter 5. We thus get an equivalent circuit as shown in Fig. 4.2.

4.4 Anti-Aliasing Analysis

In the preceding section, we chose a sampling frequency (f_S) for the SCF, which is effectively twice the switching frequency (f_{SW}) of the Buck converter. Now, the input to this filter is the output voltage of the Buck converter (V_{OUT} in Fig. 1.6). This voltage spectrum consists of baseband content (up-to the LC filter cutoff frequency) and high frequency

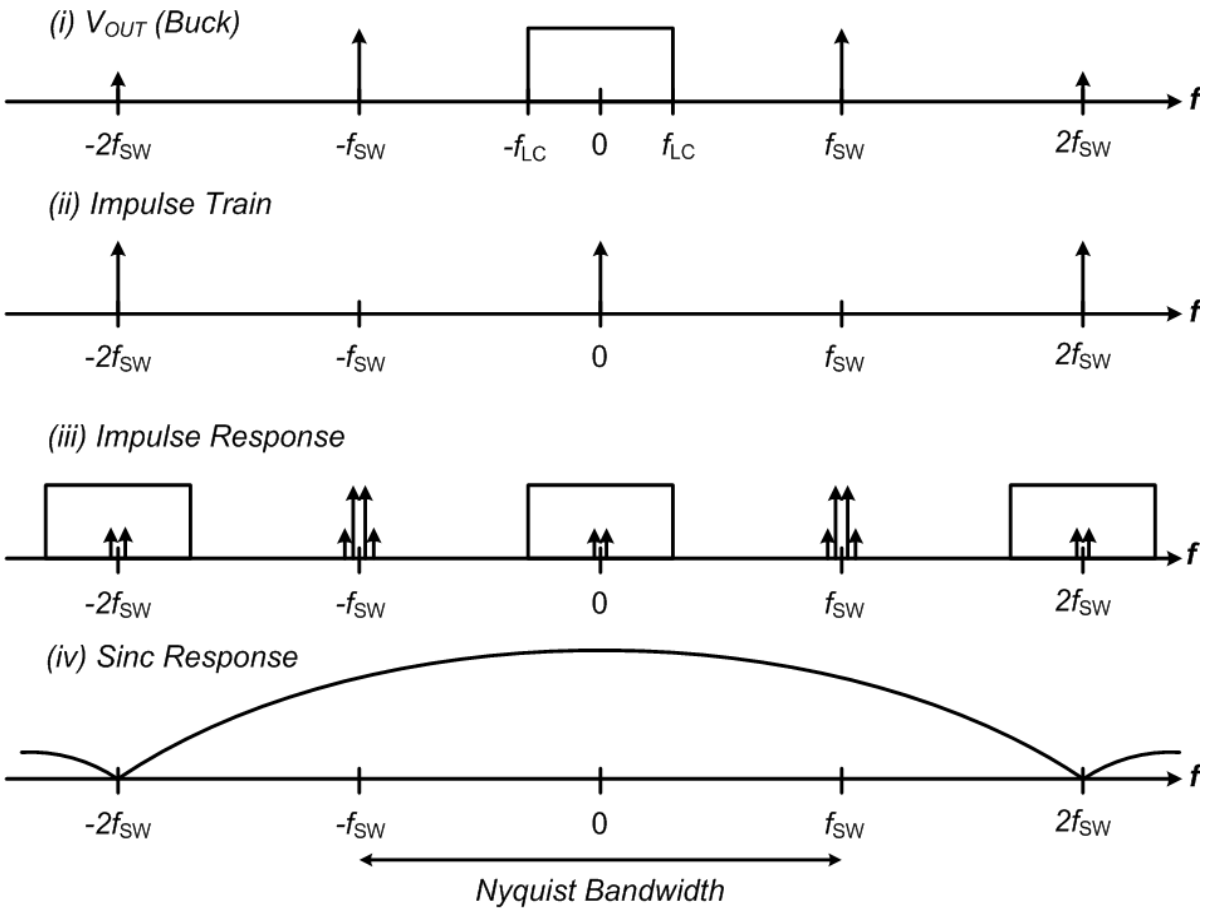


Figure 4.3: Spectral content due to sampling operation in the SCF of Fig. 4.2 without any pre-filtering and $f_S = 2 \times f_{SW}$.

switching harmonics. The strongest tone obviously exists at f_{SW}, and depends on the voltage ripple. The situation is aptly described in the frequency domain (excluding the SCF response) in Fig. 4.3.

With the worst-case ripple voltage of 5 %, we achieve a best case -26 dB SNR. Clearly, this does not meet the -40 dB SNR anti-aliasing requirements as discussed in Section 2.3. The ripple (and hence noise) power can be decreased by placing tighter requirements on

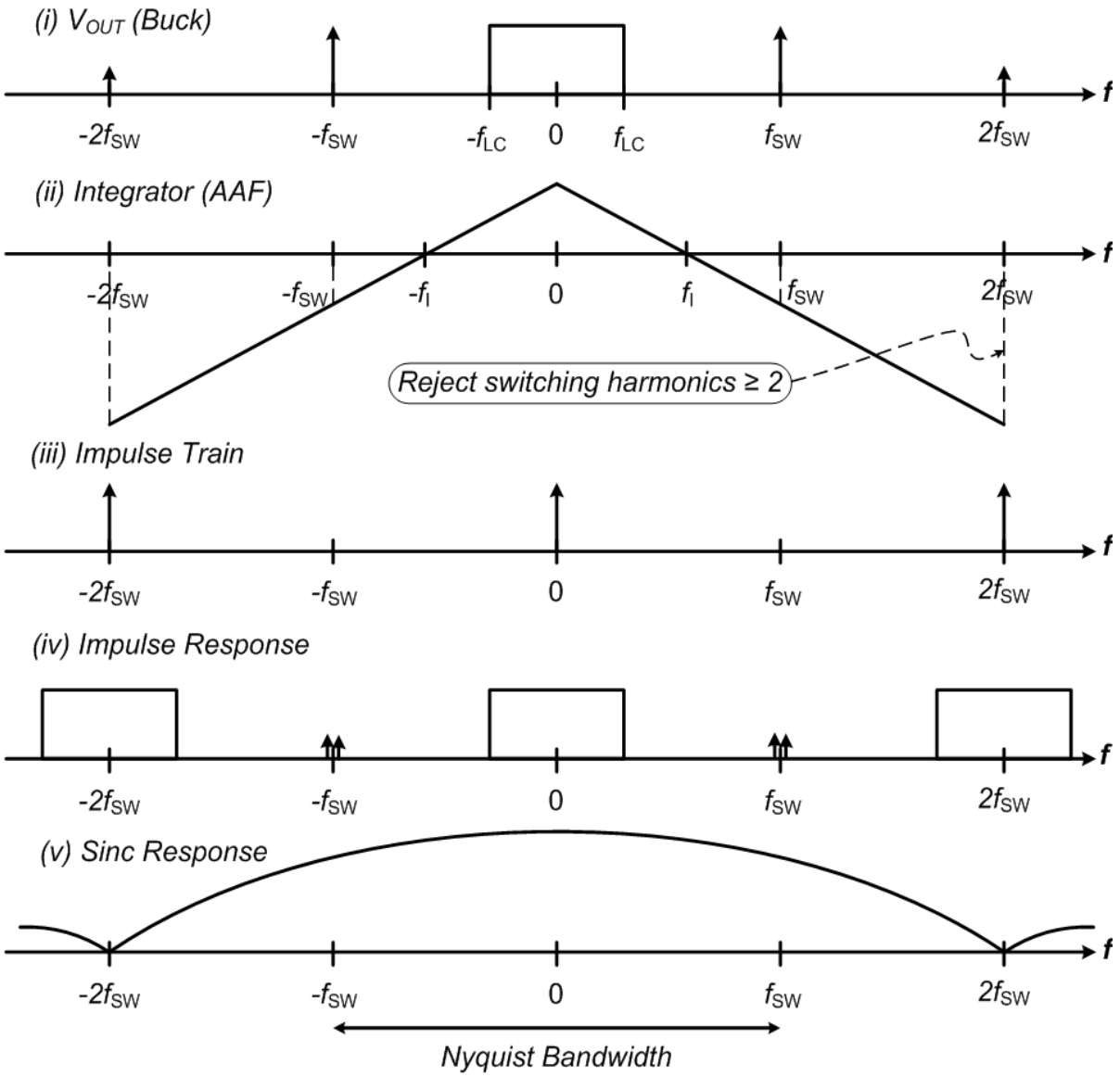


Figure 4.4: Spectral content due to sampling operation in the SCF of Fig. 4.2 with analog integrator as an AAF and $f_S = 2 \times f_{SW}$.

the LC filter design, such as low ESR, ESL and sufficiently low LC frequency. However, that would defeat the purpose of our current approach since we claimed in Section 1.1 that the linear PWM control is generally stable with all *LC* filter designs (keeping in mind only

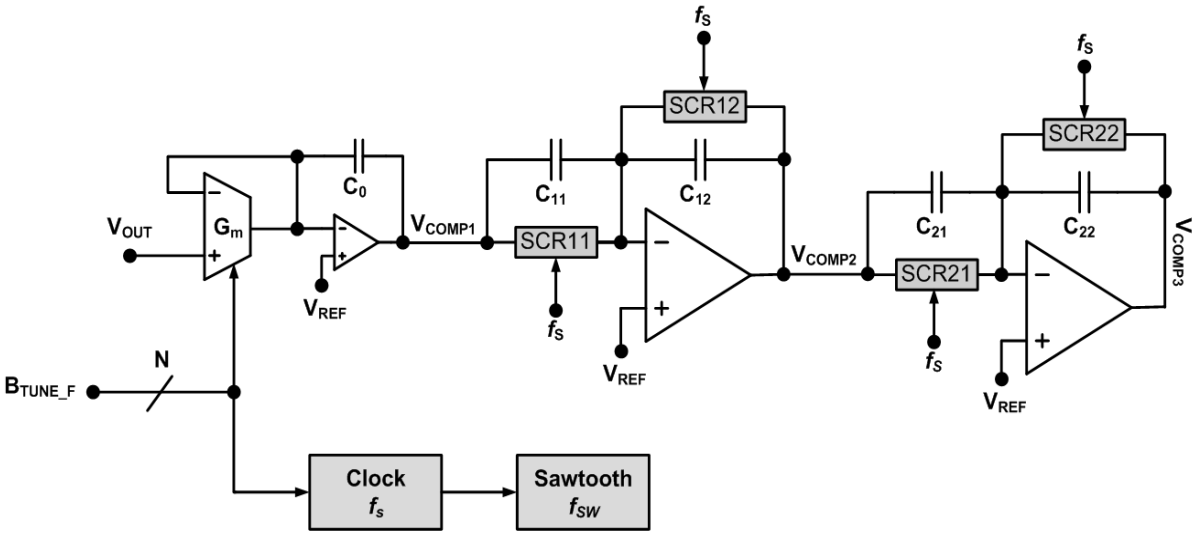


Figure 4.5: SCF architecture for *f*-scalability with integrator as an AAF.

the power-stage requirements). This was listed as a significant benefit compared to the non-linear control strategies (see Table 1.1), and thus cannot be compromised upon. Interestingly, while the closed-loop stability would improve with a larger output capacitor ESR in Type-III compensation by increasing the phase margin (see Fig. 3.2), it would increase the V_{OUT} ripple and disrupt the functioning of the SCF in Fig. 4.2. In order to make the filter requirements independent of the LC filter design, we can introduce some sort of analog pre-filtering (low-pass/notch) to attenuate the ripple magnitude. However, this pre-filter can potentially interfere with the desired Type-III filter response, and especially the phase response. It must be understood that any phase degradation can severely impact the stability of the switching converter.

An alternate solution to this problem would be to make the integrator stage a fully-analog design. If the integrator bandwidth ($1/2\pi\tau_1$) is placed at a maximum value of $f_{SW}/10$, it

would provide an additional -20 dB of attenuation to the switching and higher order harmonics, and would thus help meet the anti-aliasing requirements of the SCF stages that follow. This analysis is presented in Fig. 4.3.

The problem that arises out of this decision is regarding the implementation of the integrator. We would still require an integrator that shows low variability with Process, Voltage and Temperature (PVT) variations, and can be tuned with the switching frequency. Clearly, an Active-RC integrator is not an option. Hence, we propose a G_m-C integrator configuration that can be tuned using the same configuration bits as the Buck converter's clock, as shown in Fig. 4.5. These bits are user-programmed which are generally used to decide the operating frequency of the switching converter. The details of the G_m implementation for PVT insensitivity and linear scalability will be discussed in Chapter 5.

4.5 SCF Cascading Problem

The SCF architecture in Fig. 4.5 is a derivative of the analog Type-III filter in Fig. 4.1. It can be seen that there exists a continuous-time path from V_{OUT1} to V_{OUT3}, as a result of direct capacitive coupling. While this topology is perfectly valid in the continuous-time version, it is problematic in SCF. In low-pass SCF, it would result in low stop-band losses [22]. This effect is also known as "signal leakthrough" in SCF [23]. It was observed that in high-pass SCF, as is the current scenario, the impact of signal leakthrough is more severe, and results in aliasing distortion of the last-stage SCF response. We have verified this effect in two different simulators namely, Spectre-RF [24] and SWITCAP [25]. Although this effect is reported in [23], a suitable explanation was found lacking. Our explanation is as

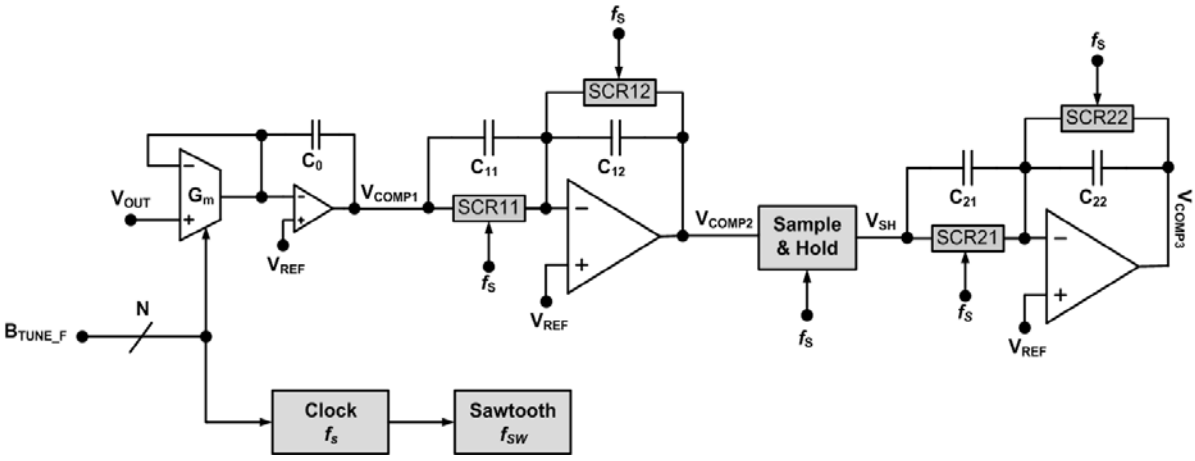


Figure 4.6: SCF architecture for eliminating the SCF cascading problem using SHA.

follows: When the 1st stage SCF produces a step output voltage V_{OUT2}, it is coupled and amplified by C_{21} and C_{22} to produce V_{OUT3}, since the 2nd stage SCF is a high-pass filter (HPF). Now, this high-frequency content on V_{OUT3} will simply distort the frequency response of this SCF due to aliasing. One way to reduce this effect is to reduce the high-frequency content on V_{OUT2}. This can be accomplished by reducing the UGB of the amplifier driving V_{OUT2} and by increasing the switch resistances of the SCNs in 1st stage SCF. However, this makes the frequency response highly dependent on the switch resistances, which can vary by more than an order of magnitude over Process, common-mode Voltage and Temperature (PVT) variations, and defeats the basic purpose of using an SCF.

An alternate strategy as listed in [22] and [23] is to "break" the continuous-time path between the two SCFs. This can be done by using a Sample-and-Hold Amplifier (SHA) circuit operating at the same sampling rate as the SCFs. Hence, we get the SCF architecture as shown in Fig. 4.6. The frequency response of an SHA operating at a sampling rate f_S

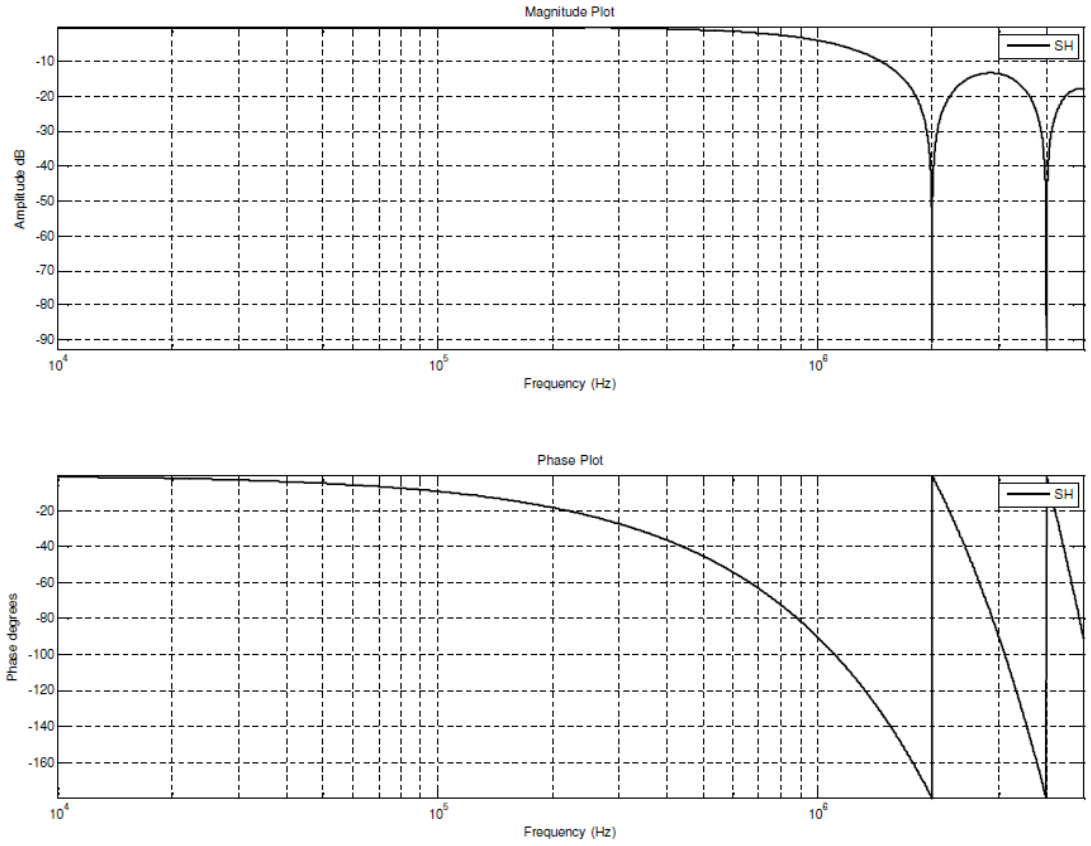


Figure 4.7: SHA magnitude and phase response for f_S = 2 MHz.

(=*1/T*) is given by:

$$H_{SHA}(j\omega_d) = Te^{\frac{-j\omega_d T}{2}} \frac{\sin\left(\frac{\omega_d T}{2}\right)}{\left(\frac{\omega_d T}{2}\right)} \tag{4.9}$$

The SHA response is represented using the MATLAB plot as shown in Fig. 4.7. It can be seen the SHA leads to magnitude degradation due to the sinc effect, with nulls at multiples of f_S. However, for f_S = 2 MHz, the magnitude degradation at the desired closed-loop

bandwidth, $f_C = f_{SW}/10 = f_S/20$ (~ 100 KHz) is negligible ~ -0.04 dB and only ~ -0.9 dB at 500 KHz. The SHA effect is more pronounced in terms of phase degradation. The phase-lag is essentially that of *T/2* in the discrete-time domain. It can be seen that the phase degrades by 9° at 100 KHz and by 45° at 500 KHz. This can severely impact both the phase and gain margin of the closed-loop response. The impact and workaround will be discussed in greater detail when we perform the complete SCF simulations in Chapter 7.

Chapter 5

5. Practical Considerations for the Type-III SCF Design

In this section, we will discuss the implementation details of the various blocks of the SCF architecture (Fig. 4.6) in Texas Instruments' (TI) 0.35-µm BCD process. Although this process offers various state-of-the-art actives/passives, we have only used the standard BiCMOS options for wider acceptability. All designs are characterized in the temperature range [-40, 125] °C, and temperature compensation has been employed, wherever necessary. Finally, based on the various design choices made keeping the power, area and speed tradeoffs in mind, we also show the gradual evolution of this Type-III SCF architecture.

5.1 G_m-C Integrator

The integrator front-end in the SCF architecture is a crucial block that helps implement both the Type-III filter and the AAF for the succeeding SCF stages. Hence, it has the following design requirements:

1. Linear Scalability: Since we are targeting frequency-scalable filter architecture, the linear scalability of the integrator bandwidth with the switching frequency is essential.
2. Process, Voltage and Temperature (PVT) Independence: For a fully-integrated design, the integrator should have little/no sensitivity to PVT variations.
3. Input Common-Mode Range (ICMR): The ICMR requirements are placed due to the soft-start function in the Buck converter, which is essential for a safe startup with controlled duty cycle (and hence inductor current). In soft-start, the soft-start signal (V_{SOFT}) is

ramped up-to V_{IN} in ~ 1 ms to allow the Buck converter to reach it steady-state operating point slowly. Now, the bandgap voltage generator (V_{BGAP}) provides a fixed on-chip reference voltage, while the soft-start ramp (V_{SOFT}) is provided externally. This ramp should bypass V_{BGAP} when $V_{SOFT} < V_{BGAP}$, while V_{BGAP} dominates otherwise, to provide V_{REF}. Thus, V_{REF} = Min (V_{SOFT}, V_{BGAP}). This operation can easily be achieved in the analog domain by using a 3-input buffer as shown in Fig. 5.1. Clearly, for both the G_m and its buffer stage, the minimum ICMR ranges between 0 and V_{BGAP}. In-fact, this requirement is true for all amplifiers in the signal chain.

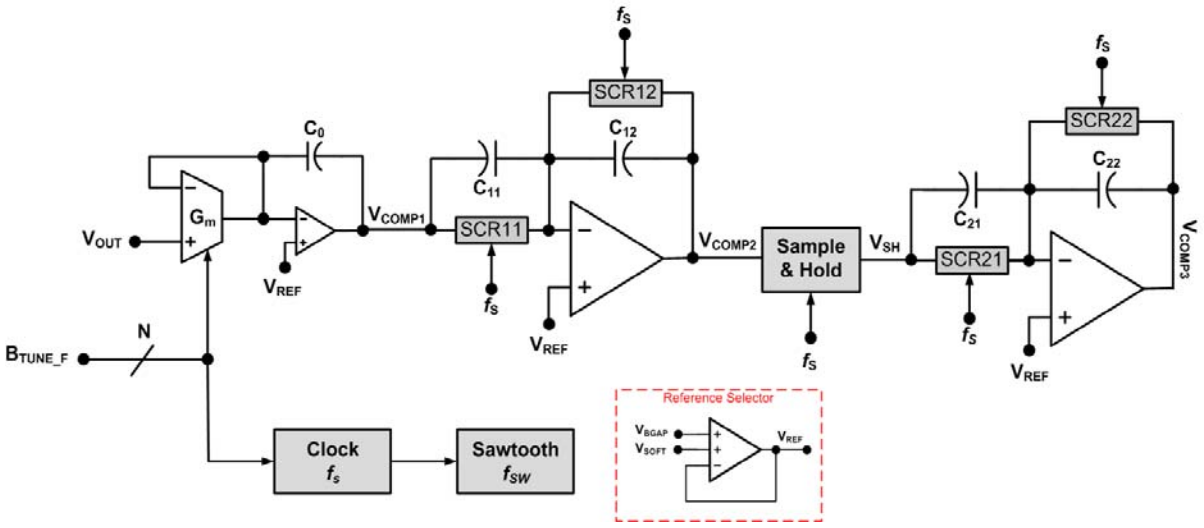


Figure 5.1: SCF architecture incorporating the reference voltage selector for soft-start of the converter.

4. Differential Linearity: This requirement is rather non-intuitive. The input signal to the filter in Fig. 5.1 is the output of the Buck Converter (V_{OUT} in Fig. 1.6). During soft-start

and line/load transients, the V_{OUT} voltage fluctuates above/below its steady state value, given by V_{REF}. This fluctuation is seen by the G_m-C integrator stage as a large input differential signal, and can be about 100 – 200 mV, if the closed-loop stability is ensured. Thus, in the worst-case, the integrator should ensure its large-signal linearity for *atleast* 200 mV of differential input signal across PVT variations.

With the design requirements firmly established, we proceed to Fig. 5.2 which shows the G_m-C filter schematic. The buffer amplifier is necessitated by the need to drive the succeeding SCF stage, and thus a fast transient response. It can be seen that V_{COMP1} has no DC feedback, but its operating point is set once the filter operates in closed-loop configuration with the Buck Converter. The G_m stage in feedback ensures that the common-mode voltage on V_{FB1} doesn't drift, which directly impacts the closed-loop

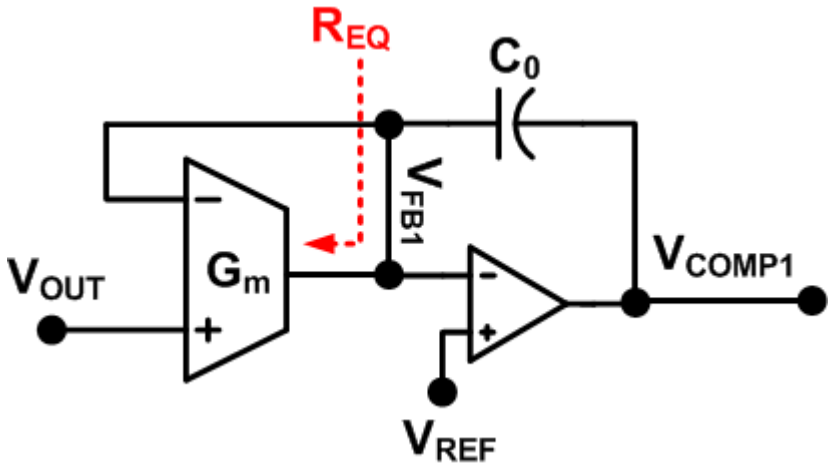


Figure 5.2: G_m-C integrator stage with buffer schematic.

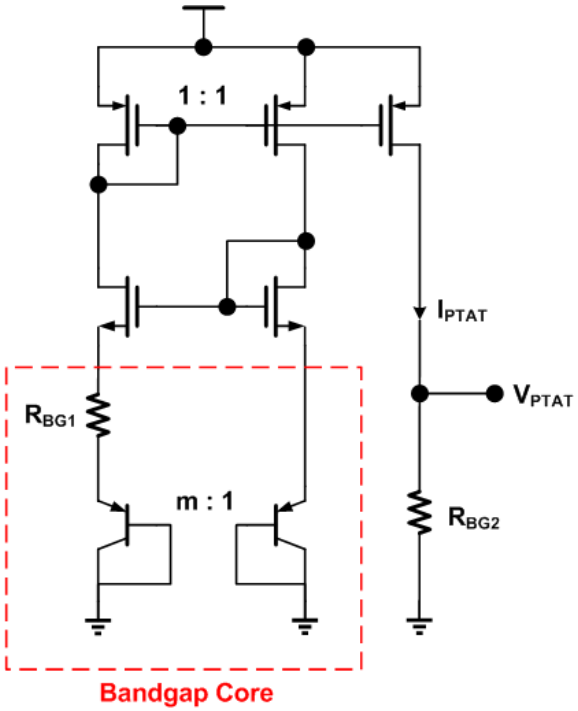


Figure 5.3: PTAT current/voltage generation circuitry in a BiCMOS process.

regulation of the switching converter. The transfer function for the above circuit can be calculated from the equivalent resistance of the transconductor:

$$R_{EQ} = \frac{1}{G_m} \,||\, R_{IN} \,||\, R_{OUT} \approx \frac{1}{G_m} \tag{5.1}$$

where, R_{IN} /R_{OUT} is the input/output impedance of the transconductance amplifier, which can be made large (MΩ range). The equivalent integrator transfer function is given by:

$$H_I(s) = \frac{1}{sR_{EQ}C_0} = \frac{G_m}{sC_0} \tag{5.2}$$

The assumptions for the above are that the buffer amplifier has bandwidth much larger than the integrator bandwidth, and that the capacitor C_0 is much larger than the parasitic

capacitances present on the input of the buffer and transconductance amplifiers. Finally, as discussed in Section 4.4, the integrator bandwidth is targeted to be 100 KHz for f_{SW} = 1 MHz.

We choose a Bipolar-input based transconductor due to its excellent properties of being linearly scalable with the bias current. The small-signal transconductance (G_m) of Bipolar is given as:

$$G_m = \frac{I_C}{V_T}, \quad V_T = \frac{kT}{q} \tag{5.3}$$

Here, I_C is the collector current and V_T is the thermal voltage. The G_m is completely independent of any process parameters, and depends only on the bias current. It can be seen that V_T is Proportional-To-Absolute-Temperature (PTAT). Thus, if we can make the collector current PTAT, the G_m can be made temperature independent as well. A PTAT current source is readily available from the bandgap reference circuit used for generating the on-chip temperature-compensated reference voltage, V_{BGAP}. Conceptually, this is shown in Fig. 5.3. The PTAT current and voltage is given as:

$$I_{PTAT} = \frac{V_T}{R_{BG1}} \ln(m), \quad V_{PTAT} = \frac{R_{BG2}}{R_{BG1}} \times V_T \ln(m) \tag{5.4}$$

where, 'm' is the ratio of the emitter areas of the PNP bipolar transistors in Fig. 5.3. Now, keeping the mind the ICMR requirements, a PMOS input-based folded-cascode amplifier would be a reasonable choice for an all-CMOS design [26]. However, as discussed before, we require a PNP-input based structure for linear scalability, which has the problem of finite input resistance (R_{IN}) [27]. This has the adverse effect of loading the G_m stage in feedback, and impacts the equivalent transconductance of the filter (see Eq. (5.1)). Hence, we avoid the

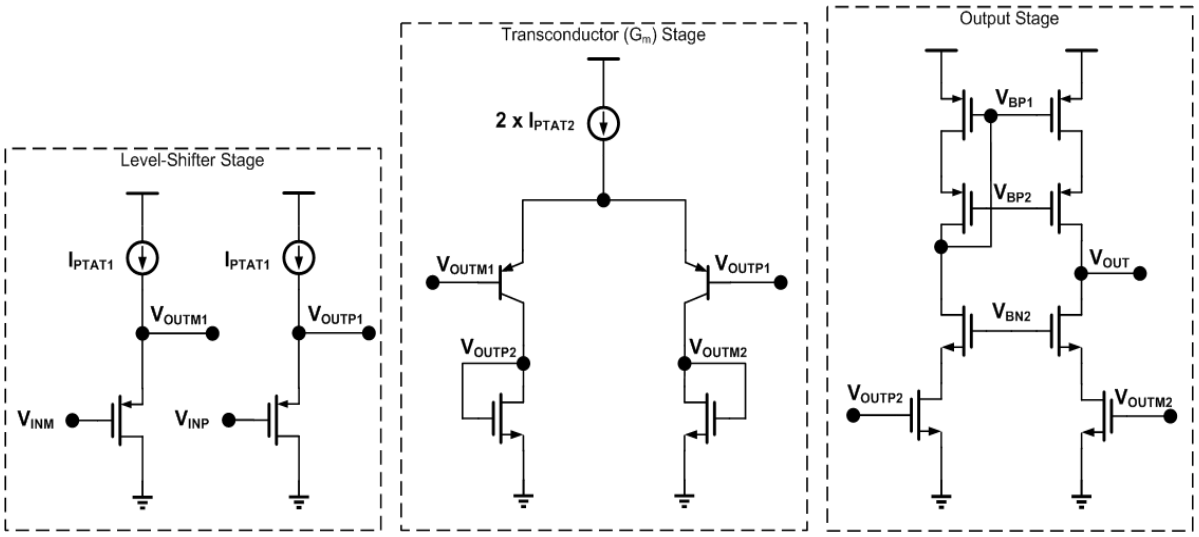


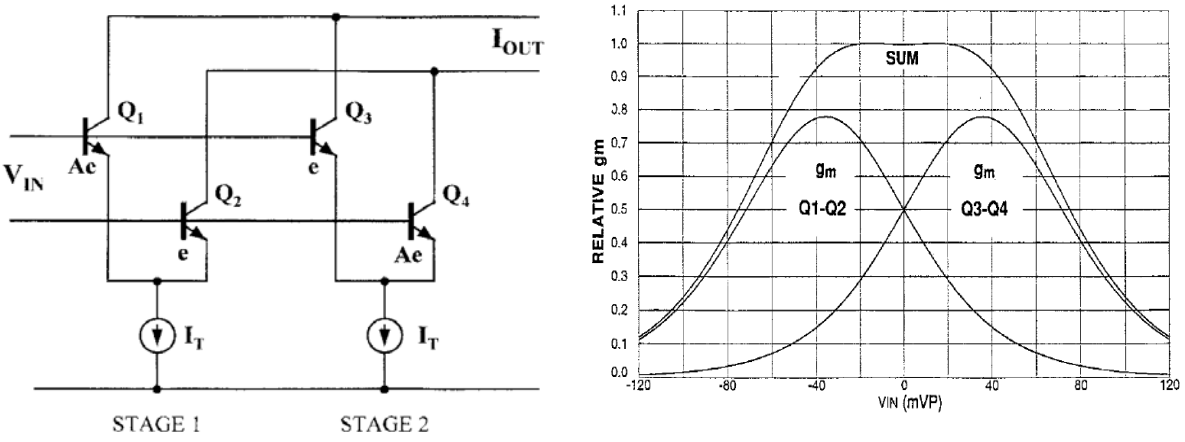
Figure 5.4: A BiCMOS Operational Transconductance Amplifier (OTA).

PNP-input folded-cascode architecture and instead use a level-shifter 1st stage (source-follower) with PMOS transistors, to drive the 2nd stage PNP transconductors, as shown in Fig. 5.4. The 3rd stage converts the differential current signal into a single-ended voltage output (V_{OUT} in Fig. 5.4). In addition, a cascoded output stage provides a large output resistance, as is required by Eqn. (5.1).

The voltage gain of the 1st stage must be included to calculate the "effective" transconductance of this OTA. Since the first two stages are fully-differential, we can perform the half-circuit analysis for a fully-differential input small-signal:

$$G_{m,\,eff} = A_1 \times G_m \tag{5.5}$$

$$A_1 = \frac{1}{1/g_{mp} r_\pi + (1+\gamma)} \tag{5.6}$$



(a) (b)

Figure 5.5: (a) Concept of a multi-tanh doublet. (b) G_m compensation [28].

Here, g_{mp} is the small-signal transconductance of the 1st stage PMOS and 'γ' is its body-effect parameter [26]. g_{mp} can be expressed in terms of the transconductance parameter ($K_P = \mu_P C_{OX}$) and the drain current $I_D = I_{PTAT1}$:

$$g_{mp} = \sqrt{2K_P \times I_D} = \sqrt{2K_P \times I_{PTAT1}} \tag{5.7}$$

The equivalent resistance at the output of 1st stage is the input resistance of the PNP given by 'r_π'. This resistance is related to the current-gain (β) of the BJT and its transconductance (G_m):

$$r_\pi = \frac{\beta}{G_m} = \beta \times \frac{V_T}{I_C} = \beta \times \frac{V_T}{I_{PTAT2}} \tag{5.8}$$

Now, from Eq. (5.6), the factor $g_{mp}r_\pi$ needs to be made much larger than 1, to make A_1 largely independent of the process parameters described in Eq. (5.7) and (5.8). However, r_π is dependent on β, which decreases with decreasing temperature. Hence, at low temperatures (~ -40 °C), the effective transconductance ($G_{m,eff}$) decreases. This will result in a slight decrease

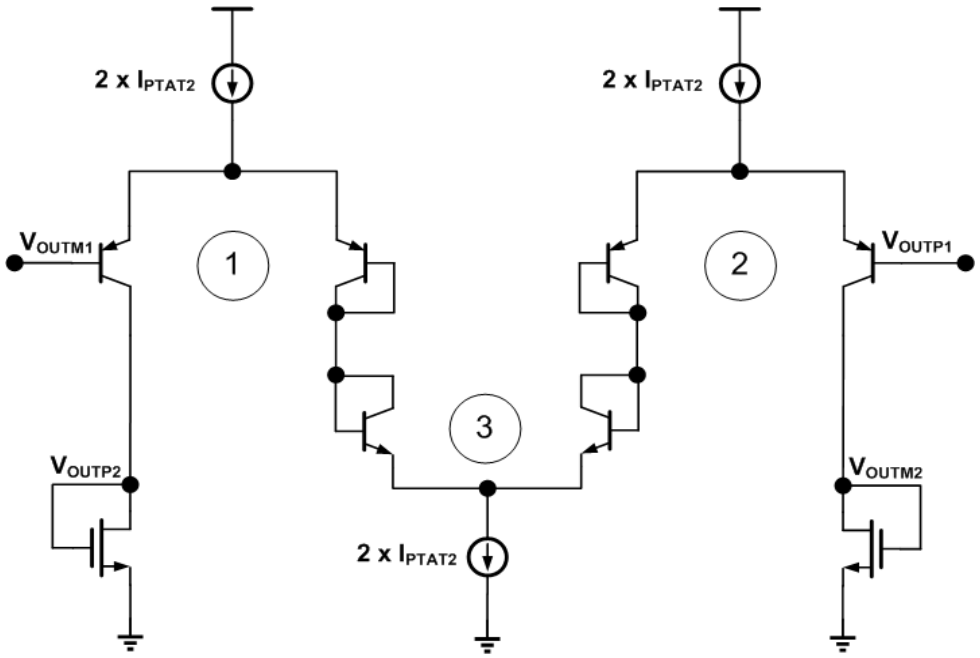


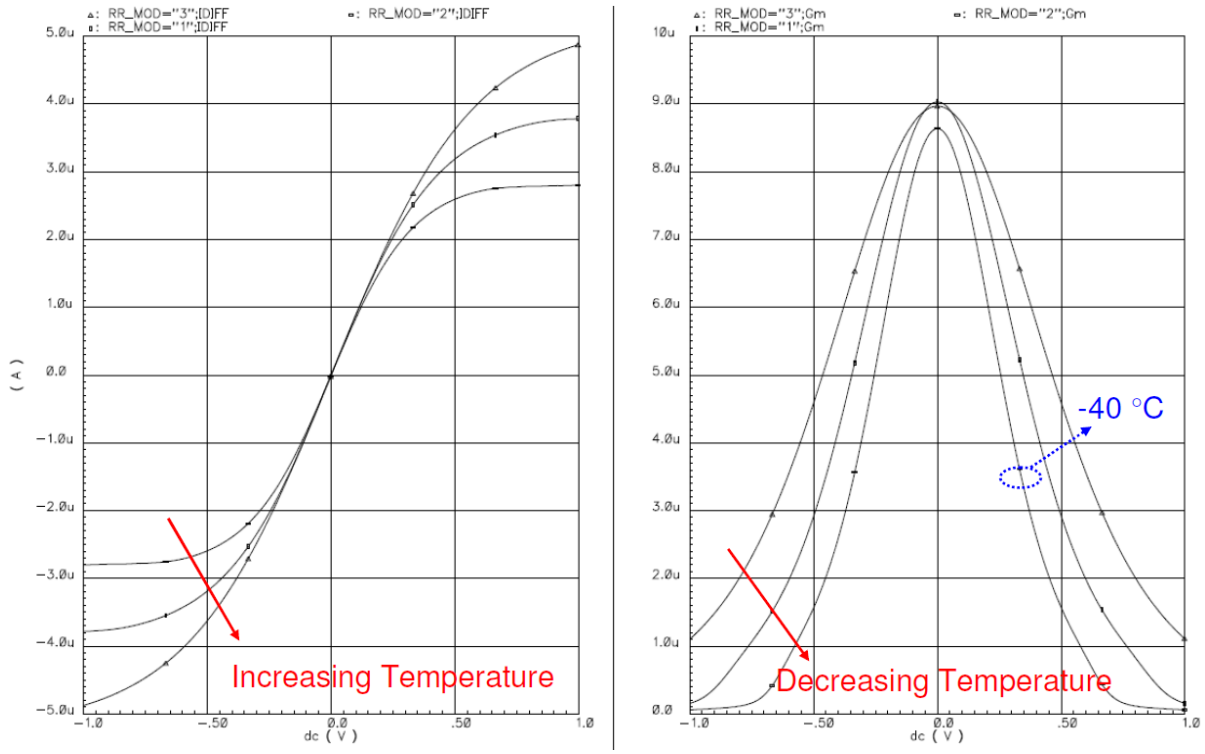
Figure 5.6: Proposed circuit to replace the G_m stage in Fig. 5.5 ($N = 2$).

of the open-loop bandwidth of the converter, and possibly an increase in the phase/gain margin. It must be hereby understood that ensuring a constant large-signal G_m over PVT variations is a difficult proposition. In addition, the C_0 variations (see Eqn. (5.2)) still need to be compensated via trimming.

With the OTA being linearly scalable, PVT compensated and meeting the ICMR requirements, we proceed to its differential linearity analysis. The large-signal differential output-current (i) to input-voltage (v) characteristic of a BJT differential pair (such as the PNP-based G_m stage in Fig. 5.4) is a 'tanh' function [28]:

$$i = I_C \times \tanh\left(\frac{v}{2V_T}\right) = I_{PTAT\,2} \times \tanh\left(\frac{v}{2V_T}\right) \tag{5.9}$$

The large signal transconductance can thus be given by:



(a) (b)

Figure 5.7: DC response showing differential (a) output current (b) transconductance, with large-signal differential input for the circuit in Fig. 5.6 for $N = 4$ case.

$$G_{m,\mathrm{L}} = \frac{I_{PTAT2}}{2V_T} \times \mathrm{sech}^2\left(\frac{v}{2V_T}\right) \tag{5.10}$$

The large signal transconductance (Eq. (5.10)) for OTA in Fig. 5.4 degrades by more than 50 % in the ±10 mV range. In addition, as is seen in Eqns. (5.9) and (5.10), the worst case for linearity is at the lowest temperature = -40 °C. This OTA's linearity performance is not sufficient for the Buck converter's transient response requirements, during soft-start and line/load transients. One way to improve linearity, while retaining the other performance benefits, is to use the multi-stage tanh compensation as described by Gilbert in [28]. In this

scheme, various BJT-based OTAs are connected in parallel by shifting their DC characteristic by an offset voltage (Fig. 5.6a). The offset can built-in by using asymmetrical devices in each differential pair in a multi-tanh configuration. The offset voltage is thus given by:

$$V_{OS} = V_T \times \ln(A) \tag{5.11}$$

where, '*A*' is the emitter area ratio in the differential pair (Fig. 5.6a). The various g_m combine in parallel to result in a flat-zone, resulting in high linearity (Fig. 5.6b). The problem with this circuit is the "explosion" of area in case the linearity needs to be extended beyond ±100 mV. As an example, we designed a quintet multi-tanh cell, having a linearity up-to ±100 mV differential signal (at nominal temperature of 27 °C), and already reached A = 55. This is clearly due to the logarithmic dependence of offset voltage (and hence the linearity range) on the ratio of the emitter areas (Eq. (5.11)). The solution we have adopted is a derived one from an all-CMOS version in [29]. Fig. 5.7 illustrates the basic circuit replacing the transconductance stage in Fig. 5.5. It can be seen that there are two PNP differential pairs and one NPN differential pair. Thus, if there are '*N*' PNP-pairs, correspondingly there will be '*N – 1*' NPN-pairs. It can thus be proved that the equivalent large-signal transconductance of this configuration is given by:

$$G_{m,\mathrm{L}} = \frac{I_{PTAT2}}{2 \times (2N-1) \times V_T} \times \operatorname{sech}^2\left(\frac{v}{2 \times (2N-1) \times V_T}\right) \tag{5.12}$$

Hence, the linearity performance of this cell is improved by a factor of '*2N – 1*'. Thus, it is eventually a technique to divide the input differential voltage across various differential pairs. The larger the value of '*N*', the better will be the linearity and worse will be amplifier

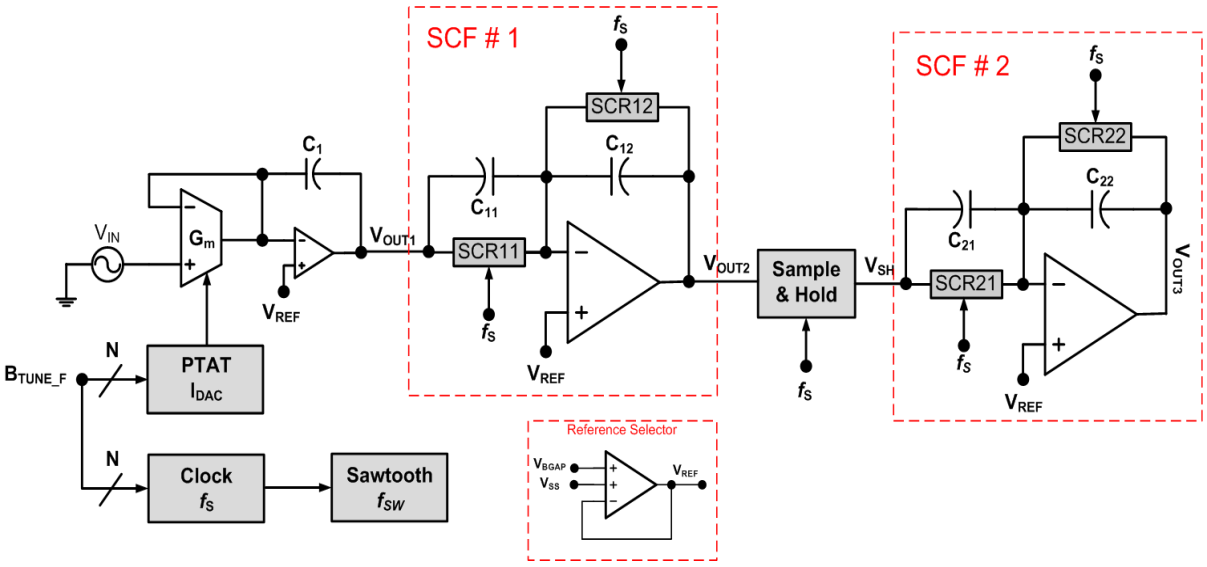


Figure 5.8: SCF architecture including the integrator tuning scheme using I_{DAC}.

offset. In our design, we have chosen a value of $N = 4$, which yields a 3σ offset of 12 mV in Monte Carlo Simulations across PVT variations.

Fig. 5.7 shows the large-signal differential output current and transconductance at three different temperatures of -40, 27 and 125 °C for I_{PTAT2} = 2 µA @ 27 °C. In the worst case at -40 °C, the $G_{m,L}$ degrades by 28 % from its nominal value at a differential input of ±200 mV and slewing is prevented up-to ±700 mV. As we will see in Chapter 8, this performance is found to be acceptable for the Buck converter closed-loop transient response. Another effect to be noted from Eq. (5.12) is the reduction of small-signal G_m by a factor of '$2N - 1$'. This has the important benefit of reduction of C_0 by the same factor (Eq. (5.2)), and results in significant area-reduction. It must be understood that the only way to reduce G_m in a Gilbert cell (Fig. 5.5) is by reducing I_{PTAT2} to the nA range (Fig. 5.4). However, this can degrade the frequency response of the integrator by introducing parasitic poles (mainly the

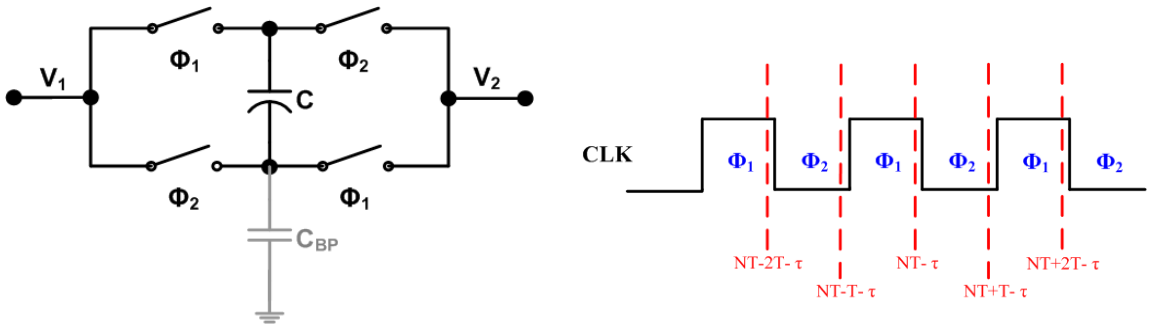


Figure 5.9: Circuit element for realizing BLT and its associated switch phases.

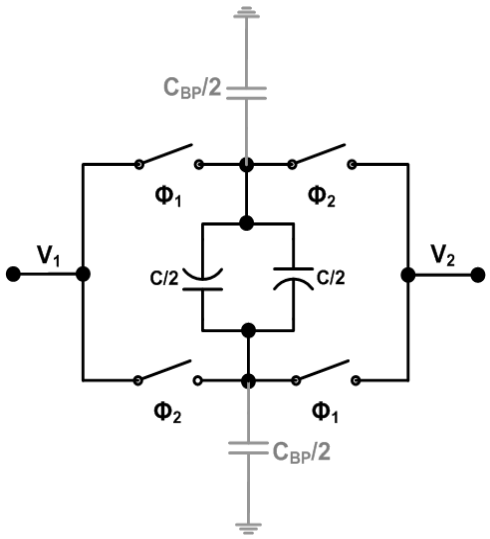


Figure 5.10: Improved BLT circuit element for symmetry and reduction of parasitics.

mirroring poles) at low frequency ($\sim f_{SW}$). These poles can directly result in a reduction of the phase margin at the converter's cutoff bandwidth $f_C \sim f_{SW}/10$, and is highly undesirable. With the OTA architecture fully developed, it can be seen from Eqns. (5.2) and (5.12) that the integrator bandwidth can be linearly tuned with a PTAT current based current DAC (I_{DAC}). This observation leads us to the updated SCF architecture schematic as shown in Fig. 5.8.

5.2 SCF # 1

There are two major challenges to the circuit realization of the high-pass SCF # 1 (Fig. 5.8). These are discussed in the following two sub-sections:

5.2.1 High-frequency pole implementation

It was concluded in Section 4.3 that using a sampling rate f_S = 2 MHz would help realize the high-frequency pole at 550 KHz using Bi-Linear s-z Transformation (BLT). In [22], a switched-capacitor circuit element which could synthesize the BLT was proposed, as shown in Fig. 35. It can be switching capacitor performs the sampling operation in both half-cycles of the clock and the sampling time period, T = $1/f_S = 1/2f_{CLK}$. Hence, the sampling rate is doubled for a given clock frequency, and we can thus choose $f_{CLK} = f_{SW}$ = 1 MHz. Now, the problem arises due to the bottom-plate capacitance (C_{BP} in Fig. 5.9), which can be 5 – 10 % of the main switching capacitor. Thus, C_{BP} interferes with the time constant being realized. A more severe problem occurs due to asymmetry in the switching behavior can result in spurious tones in the output spectrum at harmonics of the sampling rate of C_{BP}, given by f_{SW}. To alleviate these problems, we propose a simple fix in Fig. 5.10, in which both the circuit symmetry and reduction of bottom-plate capacitance (by 50 %) is achieved.

Now, we implement both SCR11 and SCR12 (Fig. 5.8) with the element shown in Fig. 5.10, to implement both the low-frequency zero and high-frequency pole. Thus, we get the circuit shown in Fig. 5.11, with the switch phases as shown. The SCF transfer function can be evaluated using the conservation of charge principles applied at the isolated node V_{FB2}. We can assume that $\tau = 0$ (Fig. 5.11) for simplicity. The initial charge of the system of

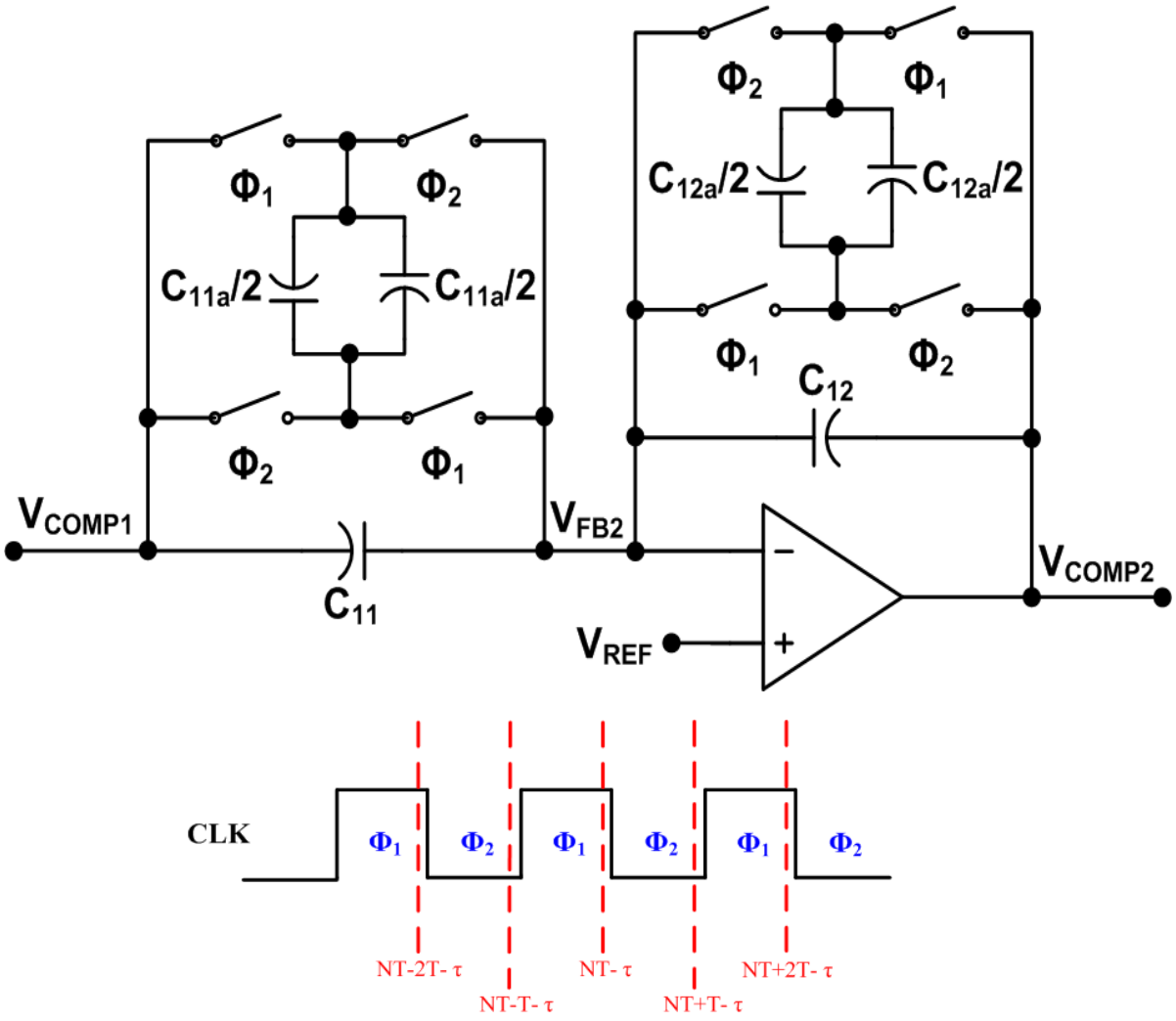


Figure 5.11: SCF # 1 circuit schematic with the switching phases indicated.

capacitors at $t = NT - T$ (end of phase Φ_2) is given by:

$$\sum q_i(t = NT-T) = (C_{11} - C_{11a})V_{OUT1}[NT-T] + (C_{12} - C_{12a})V_{OUT2}[NT-T]$$

The final charge $t = NT$ (end of phase Φ_1) is given by:

$$\sum q_f(t = NT) = (C_{11} + C_{11a})V_{OUT1}[NT] + (C_{12} + C_{12a})V_{OUT2}[NT]$$

Equate the initial and final charges by the law of conservation of charge:

$$\left(C_{11}+C_{11a}\right)V_{OUT1}\left[NT\right]+\left(C_{12}+C_{12a}\right)V_{OUT2}\left[NT\right]=\left(C_{11}-C_{11a}\right)V_{OUT1}\left[NT-T\right]+$$
$$\left(C_{12}-C_{12a}\right)V_{OUT2}\left[NT-T\right]$$

Rearranging like terms for V_{OUT1} and V_{OUT2}, we get,

$$\left(C_{11}+C_{11a}\right)V_{OUT1}\left[NT\right]-\left(C_{11}-C_{11a}\right)V_{OUT1}\left[NT-T\right]=-\left(C_{12}+C_{12a}\right)V_{OUT2}\left[NT\right]+$$
$$\left(C_{12}-C_{12a}\right)V_{OUT2}\left[NT-T\right]$$

Take the z-transform of this discrete-time difference equation to get:

$$\left\{\left(C_{11}+C_{11a}\right)-z^{-1}\left(C_{11}-C_{11a}\right)\right\}V_{OUT1}(z)=\left\{z^{-1}\left(C_{12}-C_{12a}\right)-\left(C_{12}+C_{12a}\right)\right\}V_{OUT2}(z)$$

$$\Rightarrow\left\{C_{11}\left(1-z^{-1}\right)+C_{11a}\left(1+z^{-1}\right)\right\}\times V_{OUT1}(z)=\left\{C_{12}\left(z^{-1}-1\right)-C_{12a}\left(1+z^{-1}\right)\right\}\times V_{OUT2}(z)$$

$$\therefore\frac{V_{OUT2}(z)}{V_{OUT1}(z)}=\frac{\left\{C_{11}\left(1-z^{-1}\right)+C_{11a}\left(1+z^{-1}\right)\right\}}{\left\{C_{12}\left(z^{-1}-1\right)-C_{12a}\left(1+z^{-1}\right)\right\}}=-\frac{\left\{C_{11}\left(1-z^{-1}\right)+C_{11a}\left(1+z^{-1}\right)\right\}}{\left\{C_{12}\left(1-z^{-1}\right)+C_{12a}\left(1+z^{-1}\right)\right\}}$$

$$\therefore H_{SCF1}(z)=-\frac{C_{11a}}{C_{12a}}\times\frac{1+\frac{C_{11}}{C_{11a}}\times\frac{\left(1-z^{-1}\right)}{\left(1+z^{-1}\right)}}{1+\frac{C_{12}}{C_{12a}}\times\frac{\left(1-z^{-1}\right)}{\left(1+z^{-1}\right)}}\qquad(5.13)$$

It can be seen that the transfer function is indeed a bilinear transformed pole/zero pair. We will rewrite Eqns. (4.3) - (4.7) here which are the reference equations for this SCF's design in Eq. (5.13):

$$H_{C2}(s)=-\frac{R_{12}}{R_{11}}\times\frac{\left(1+s\tau_{11}\right)}{\left(1+s\tau_{12}\right)}$$

$$\frac{1}{\tau_{11}} = 2\pi \times 20 \times 10^3 rad/s, \qquad \frac{1}{\tau_{12}} = 2\pi \times 745 \times 10^3 rad/s$$

The pole frequency has been increased from 550 to 745 KHz due to the effect of pre-warping in BLT (see Section 4.3). Now, we can do the s-z substitution using Eq. (2.13) in $H_{C2}(s)$ to get the reference transfer function for $H_{SCF1}(z)$:

$$s_a = \frac{2}{T} \times \frac{1 - z^{-1}}{1 + z^{-1}} = \frac{4}{T_{SW}} \times \frac{1 - z^{-1}}{1 + z^{-1}}$$

where, T_{SW} is the switching time period of the Buck Converter. Thus,

$$H_{C2}(s) = -\frac{R_{12}}{R_{11}} \times \frac{\left(1 + 4 \times \frac{\tau_{11}}{T_{SW}} \times \frac{1 - z^{-1}}{1 + z^{-1}}\right)}{\left(1 + 4 \times \frac{\tau_{12}}{T_{SW}} \times \frac{1 - z^{-1}}{1 + z^{-1}}\right)} \tag{5.14}$$

For a DC gain equal to unity, we can choose C_{11a} and C_{12a} to be unit capacitors (for target matching requirements). Finally, C_{11} and C_{12} can be calculated by comparing (5.13) and (5.14) and performing coefficient matching. In our design, we have chosen $C_{11a} = C_{12a} = 1.25$ pF, $C_{12} = 1$ pF and $C_{11} = 40$ pF.

5.2.2 *Effects of Finite Opamp Gain-Bandwidth*

In the foregoing analysis, we have assumed that amplifier is ideal with infinite gain and bandwidth such that the feedback node is always at virtual ground. However, as can seen, the above specifications for the amplifier can never be met, and hence the filter deviates from its ideal response. This is especially true for high-pass filters, wherein the high-frequency amplification should, intuitively, get limited by the amplifier's Gain Bandwidth

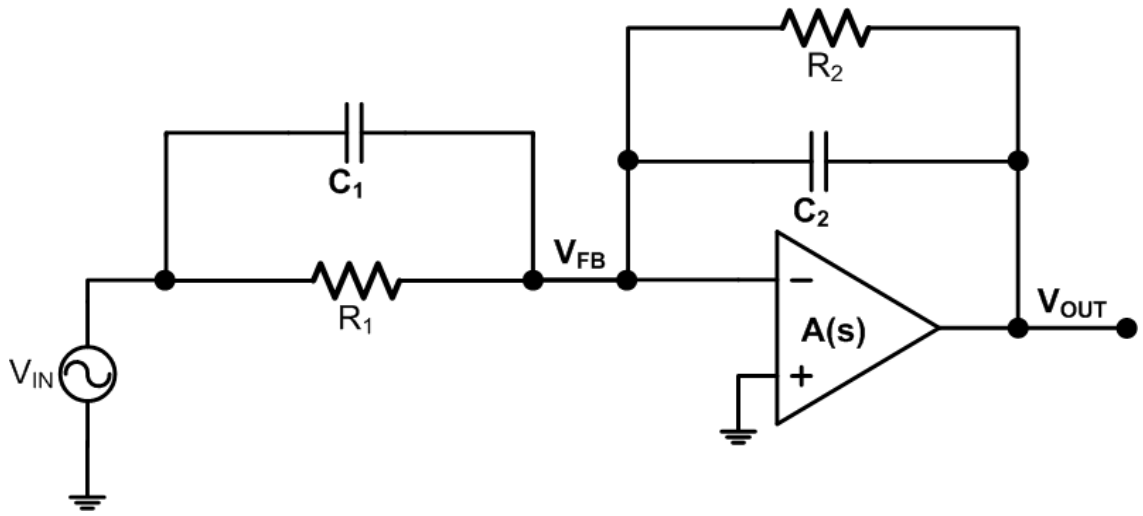


Figure 5.12: A 1st order analog high-pass filter with finite Gain Bandwidth Opamp.

(GBW). These effects and more are quantified in greater detail in this sub-section. Fig. 5.12 shows the example of a 1st order high-pass filter with a finite GBW amplifier. Now, we can readily write the following relationships for this case under consideration:

$$Z_{1,2}(s) = \frac{R_{1,2}}{1 + s\tau_{1,2}}; \quad \tau_{1,2} = R_{1,2}C_{1,2}$$

The feedback factor is given as:

$$B(s) = B_0 \frac{1 + s\tau_2}{1 + s\tau_2}; \quad B_0 = \frac{R_2}{R_1} \tag{5.15}$$

Now, with V_{FB} no longer a virtual ground node, we can write the following using KCL:

$$\frac{V_{FB}(s) - V_o(s)}{Z_2(s)} = \frac{V_i(s) - V_{FB}(s)}{Z_1(s)}$$

However, the amplifier maintains its input/output characteristics. We also assume a simple single-pole (s_0) model for the amplifier under consideration.

$$V_{FB}(s) = \frac{-V_o(s)}{A(s)}, \quad A(s) = \frac{A_0}{1 + s/s_0}$$

$$\therefore V_i(s) = -V_o(s)\left[\frac{Z_1(s)}{Z_2(s)}\left(1 + \frac{1}{A(s)}\right) + \frac{1}{A(s)}\right]$$

Thus, we can now calculate the filter transfer function in terms of A(s) and B(s):

$$\Rightarrow H(s) = \frac{V_o(s)}{V_i(s)} = \frac{-A(s)B(s)}{1 + A(s) + B(s)} \tag{5.16}$$

The above is a very fundamental relationship. Now, we need to substitute A(s) and B(s) to evaluate H(s). However, since the expression becomes too complex, we will solve for the numerator (N(s)) and denominator (D(s)) separately.

$$N(s) = -A(s)B(s) = -A_0B_0\frac{1 + s\tau_1}{\left(1 + \frac{s}{s_0}\right)(1 + s\tau_2)} \tag{5.17}$$

$$D(s) = 1 + A(s) + B(s) = 1 + \frac{A_0}{\left(1 + \frac{s}{s_0}\right)} + \frac{B_0(1 + s\tau_1)}{(1 + s\tau_2)}$$

$$\Rightarrow D(s) = \frac{\left[1 + B_0 + A_0 + \left(\frac{s}{s_0}\right)(1 + B_0) + \left(\frac{s^2}{s_0}\right)(B_0\tau_1 + \tau_2) + sB_0\tau_1 + s\tau_2 + A_0s\tau_2\right]}{\left(1 + \frac{s}{s_0}\right)(1 + s\tau_2)}$$

In the example HPF, the zero is located at a frequency much lower than the pole. Thus, $\tau_1 >> \tau_2$. In addition, the amplifier's DC gain is much larger than the DC feedback factor ($A_0 >> B_0$). Hence, we use these relations for approximation:

$$\Rightarrow D(s) = \frac{1}{\left(1+\frac{s}{s_0}\right)(1+s\tau_2)}\left[A_0 + s\left\{\frac{(1+B_0)}{s_0} + B_0\tau_1 + A_0\tau_2\right\} + s^2\left(\frac{B_0\tau_1}{s_0}\right)\right] \quad (5.18)$$

We can combine (53) and (54) to finally calculate *H(s)*,

$$H(s) = \frac{N(s)}{D(s)} = \frac{-B_0(1+s\tau_1)}{1+s\left\{\frac{(1+B_0)}{A_0 s_0} + \frac{B_0\tau_1}{A_0} + \tau_2\right\} + s^2\left(\frac{B_0\tau_1}{A_0 s_0}\right)}$$

Now, we will use the final approximation that the amplifier's GBW is much larger than the pole frequency ($1/\tau_2$):

$$\Rightarrow \frac{A_0 s_0}{1+B_0} >> \frac{1}{\tau_2}; \quad \tau_2 >> \frac{B_0\tau_1}{A_0}$$

$$\therefore H(s) = \frac{-B_0(1+s\tau_1)}{1+s\tau_2+s^2\left(\frac{B_0\tau_1}{A_0 s_0}\right)} = \frac{-B_0(1+s\tau_1)}{1+s\tau_2+s^2\left(\frac{\tau_1}{s_{0\_eff}}\right)} \quad (5.19)$$

where, s_{0_eff} is the effective GBW of the amplifier. The above is a 2nd order under-damped response characterized by the following parameters:

$$\omega_N = \sqrt{\frac{A_0 s_0}{B_0\tau_1}}; \quad \zeta = \frac{1}{2}\sqrt{\frac{A_0 s_0}{B_0\tau_1}} \times \tau_2 \quad (5.20)$$

There are several important observations from Eqns. (5.19) – (5.20):

i. The zero frequency is preserved and is the same as $1/\tau_1$.

ii. The pole frequency is not preserved. The pole is now complex and is present at the geometric mean of the amplifier's effective GBW (s_{0_eff}) and zero frequency ($1/\tau_1$).

iii. The natural frequency of oscillation (ω_N) and the damping factor (ζ) are a function of $A_0 s_0$, B_0, τ_1 and τ_2. Of these parameters, B_0, τ_1 and τ_2 are tightly controlled in the SCF realization of HPF in Fig. 38. However, $A_0 s_0$ (GBW of the amplifier) can vary over PVT variations. Thus, if we can ensure that the filter meets the design specifications for the worst-case minimum amplifier GBW across 3σ PVT variations. Since the amplifier GBW will only be greater than this minimum value, the complex pole will have a higher frequency and damping factor as dictated by Eq. (5.20). Hence, the closed-loop stability will be ensured.

5.2.3 *Opamp Design*

Keeping the foregoing analysis in mind, we ensured that the filter design would be acceptable for a worst-case Opamp GBW = 20 MHz. The first step for designing this Opamp would be to understand the loading requirements. For the high-pass SCF shown in Fig. 5.11, the equivalent loading is $C_{12} + C_{12a}$ = 2.25 pF. Add to this another 1 pF of the succeeding sample-and-hold stage, and we get 3.25 pF. Now, we design this amplifier for a worst case loading, $C_L \sim 4$ pF, thus giving some design margin. The Opamp schematic is shown in Fig. 5.13. It has a differential folded-cascode input transconductor pair for low ICMR requirements discussed in Section 5.1. The cascoded output from the 1st stage also helps in ensuring high DC gain (> 80 dB). Finally, we choose a floating class-AB output stage which can adequately drive the load capacitance C_L, without limiting the slew-rate [30]. The slew-

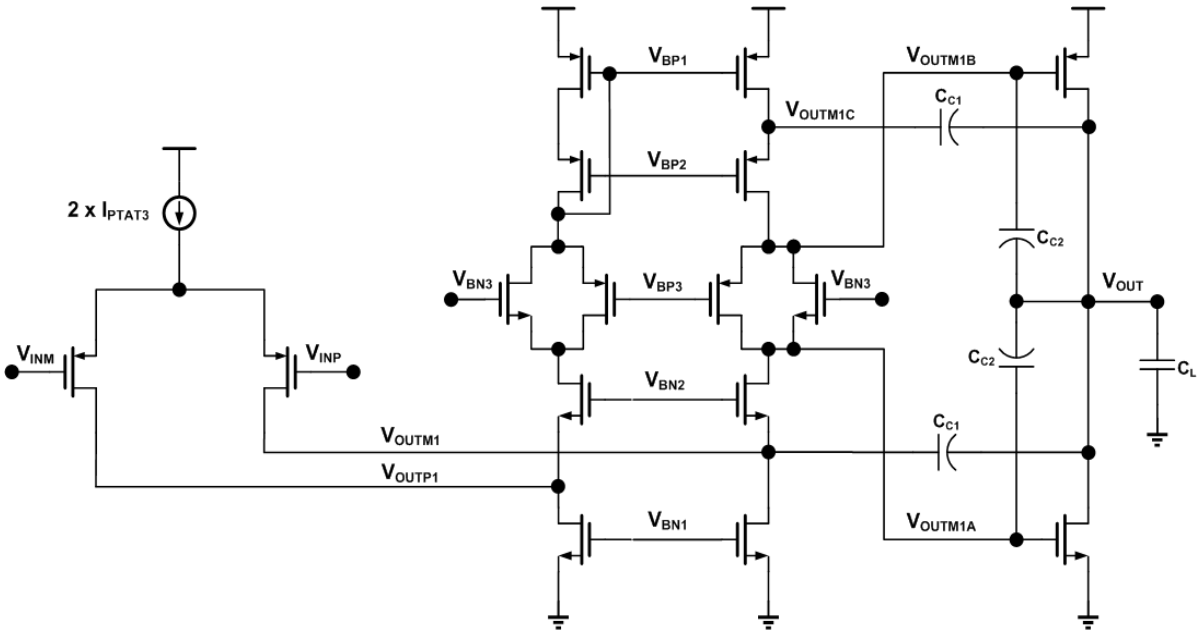


Figure 5.13: A folded-cascode amplifier with class-AB output stage.

rate is thus limited by the total compensation capacitance driven by the input tail current:

$$SR = \frac{C_{C1} + C_{C2}}{I_{PTAT3}} \tag{5.21}$$

The dominant pole is present at the output of 1st stage ($V_{OUTM1A,B}$) since it has the largest output impedance (R_{OUT1}). In addition, compensation capacitors C_{C1} and C_{C2} undergo miller multiplication by the 2nd stage in mid-band frequencies to present a large effective capacitance at $V_{OUTM1A,B}$. The target GBW of this amplifier is given by:

$$\omega_{GBW} = \frac{G_{m1}}{2 \times \left(C_{C1} + C_{C2}\right)} \tag{5.22}$$

where G_{m1} is the differential small-signal transconductance of the input pair. This expression is obtained clearly by using a single-pole approximation for the amplifier. However, there

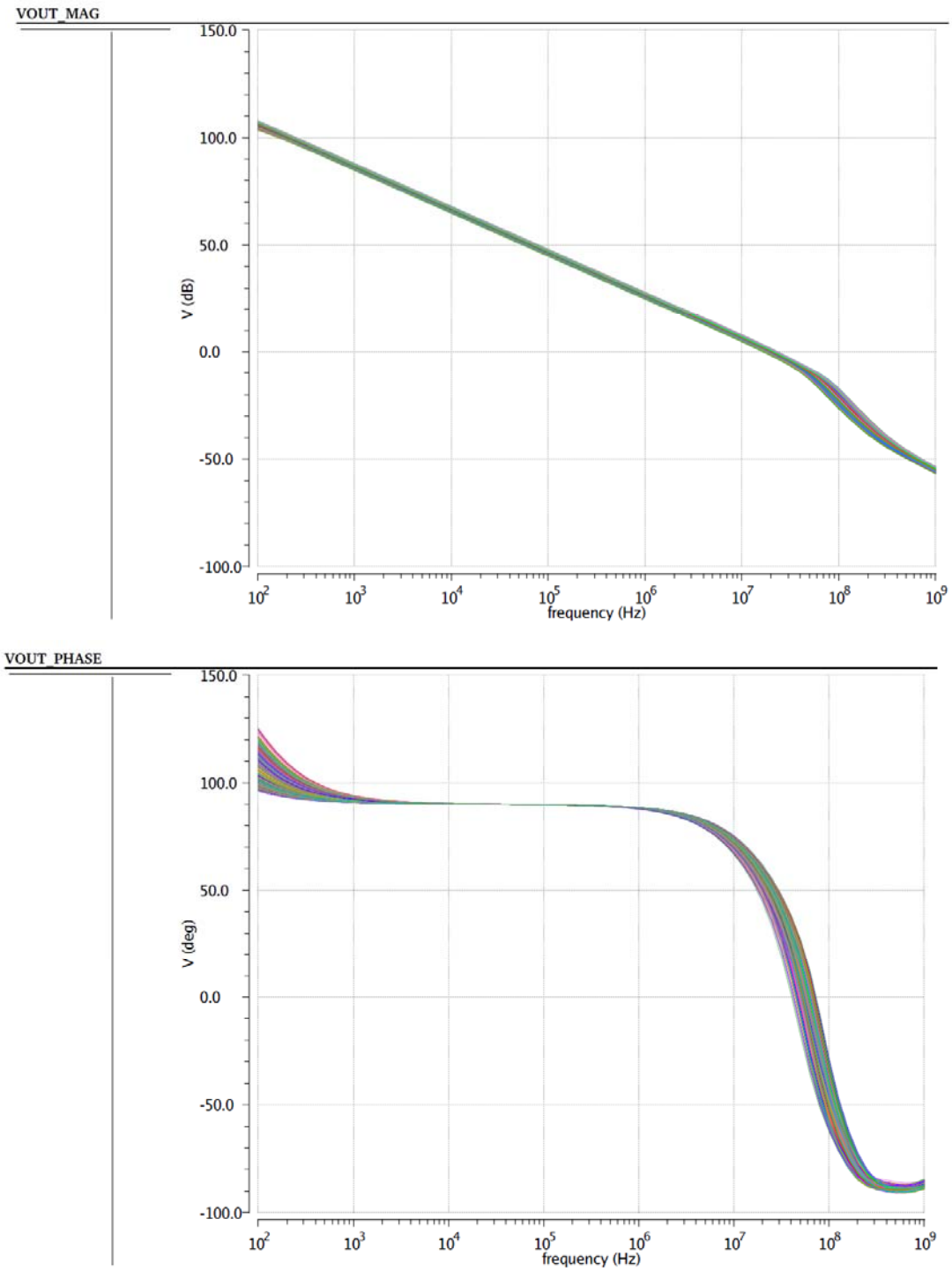


Figure 5.14: Monte-carlo output for AC response simulation of Opamp in Fig. 5.13.

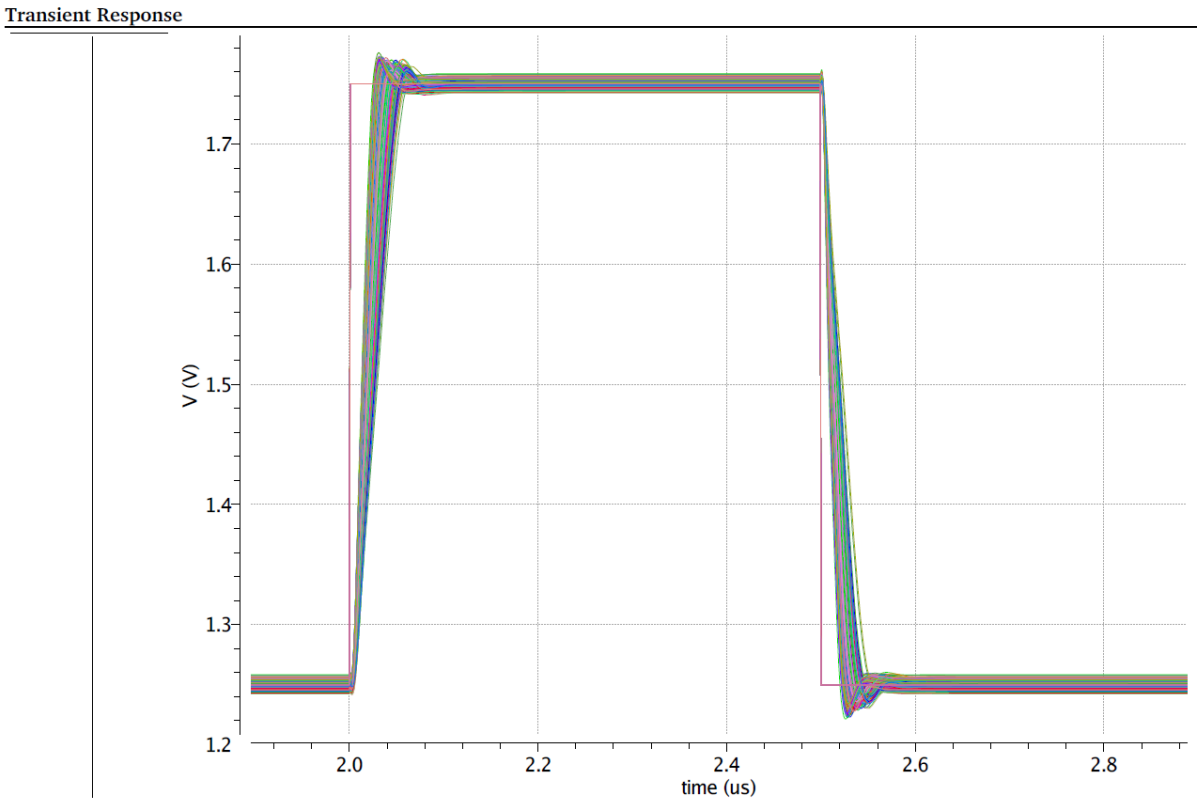


Figure 5.15: Monte-carlo output for step response simulation of Opamp in Fig. 5.13.

lies a non-dominant pole at the output node (V_{OUT}) driving a large capacitor (C_L). The location of this pole is given by:

$$\omega_{P2} = K \times \frac{G_{m2}}{C_L} = \frac{2 \times C_{C1}}{C_{PAR}} \times \frac{G_{m2}}{C_L}; \quad \omega_{P2} > \omega_{GBW} \tag{5.23}$$

where G_{m2} is the small-signal transconductance of the output stage, and C_{PAR} is the total parasitic capacitance present on $V_{OUTM1A,B}$. Now, it can be seen the non-dominant pole frequency is extended by 'K' times using this compensation scheme compared to what would have been feasible with the standard Miller compensation [26]. Thus, in miller compensation,

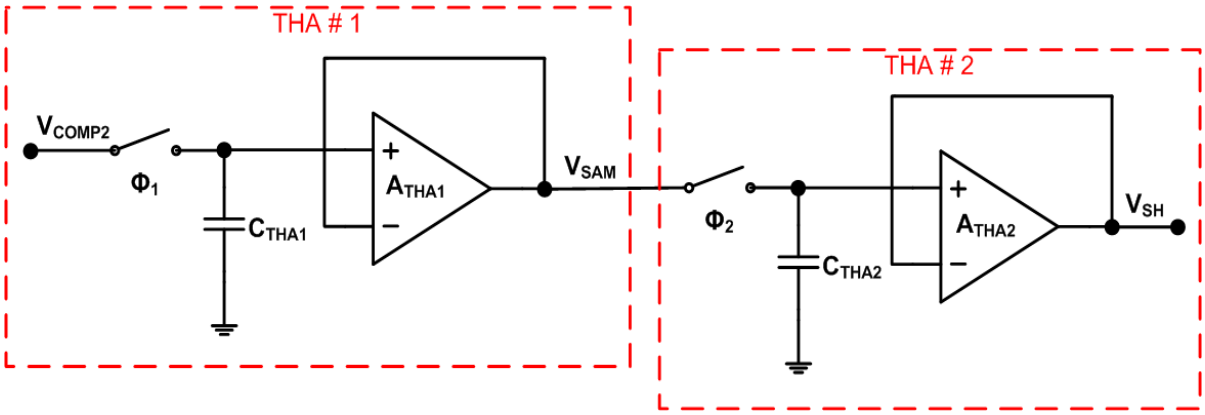


Figure 5.16: SHA implementation as a cascade of two THAs.

typically a RC compensation is used to non-dominant pole cancellation by a LHP zero to extend the amplifier GBW, and achieve sufficient phase margin (45° – 90°) for local stability. However, since the RC time constant can vary by ±40 %, the miller-compensated amplifier can require either external compensation components or trimming. With this scheme, since both the load and compensation capacitors are of the same type (Poly1 – Oxide - Poly2 capacitors), they tend to track each other over PVT variations. Finally, a PTAT bias current source is used to compensate for variations in various MOS transconductances over the entire temperature range (see Eqns. (5.22) and (5.23)).

Fig. 5.14 shows the output for Monte-Carlo simulation (absolute and relative process variability) for the open-loop AC response of the Opamp in Fig. 5.13 at three different temperatures of -40, 27 and 125 °C. It can be seen that the worst-case stability is ensured with -3σ Phase Margin (PM) of 50°. In addition, the worst-case Unity-Gain Bandwidth (UGB: same as GBW) of the amplifier is 20.6 MHz. Fig. 5.15 shows the response of the amplifier to a 0.5 V input voltage step (in 1 ns), under the conditions just described. The

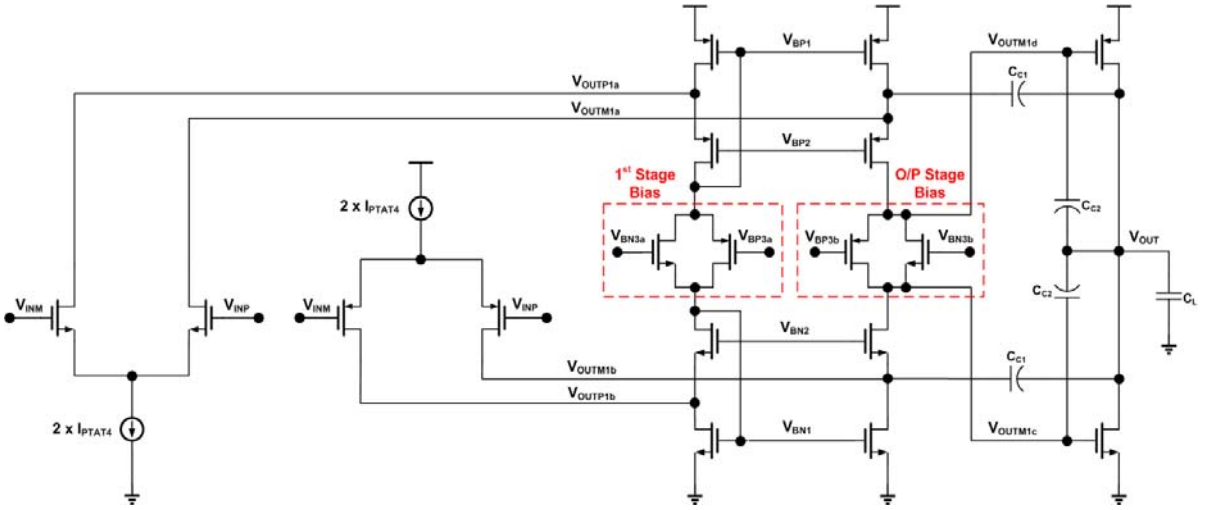


Figure 5.17: A rail-to-rail amplifier with class-AB output stage.

amplifier settles well within the half switching period ($T_{SW}/2$ = 500 ns). To ensure a nice slewing response, C_{C2} (< C_{C1}) is used, which acts a high-frequency bypass and improves the large signal response. It is also important to understand here that the large signal response would improve for smaller and slower step inputs, which would be a more realistic operating condition for this Opamp. Finally, it must be mentioned that this performance for the amplifier is achieved by consuming only 100 μA of static current at nominal temperature (27 °C).

5.3 Sample-and-hold Amplifier (SHA)

The Sample-and-Hold Amplifier (SHA) is really a cascade of two Track-and-Hold Amplifiers (THA), operating on the complementary phases of a clock. While there exist several possible implementations for the SHA [18], we have chosen the one in Fig. 42 for its simplicity and the fact that it is able to hold the signal for the entire half clock-cycle. It must

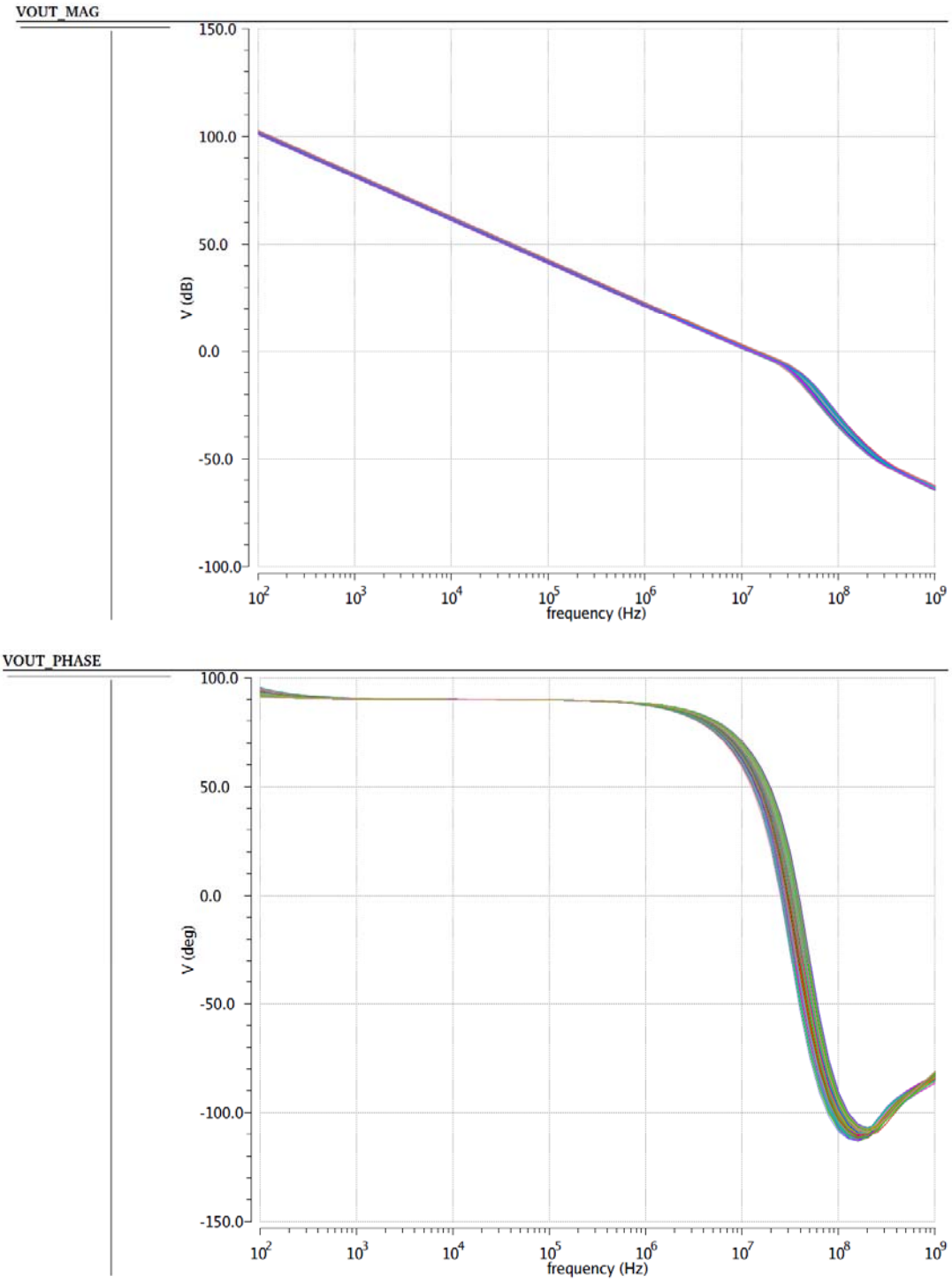


Figure 5.18: Monte-carlo output for AC response simulation of Opamp in Fig. 5.17.

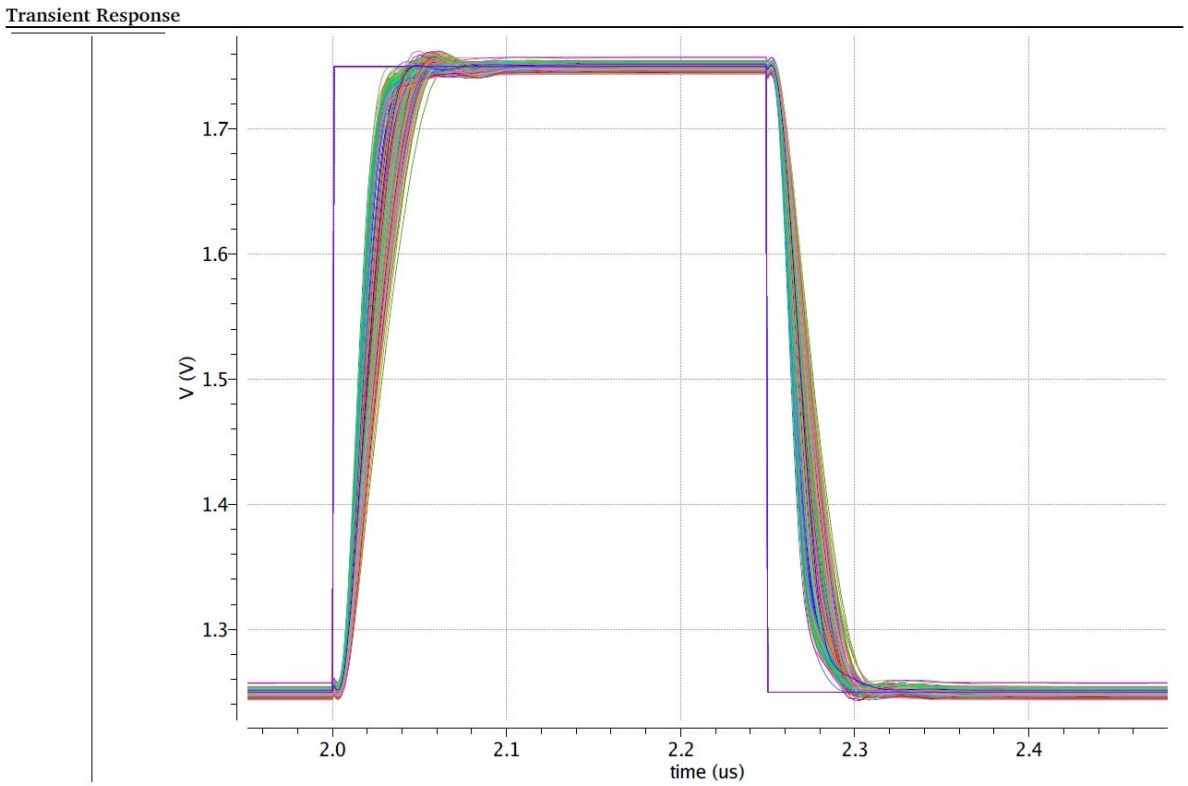


Figure 5.19: Monte-carlo output for step response simulation of Opamp in Fig. 5.17.

be noted that the SHA stage needs to have rail-to-rail input/output common-mode voltage requirements, in order to maximize the dynamic range of the filter, and prevent any undesirable amplifier saturation. This makes the SHA design inherently power hungry.

In addition, as discussed earlier, the SHA operates at $f_S = 2 \times f_{SW} = 2$ MHz, and thus each THA amplifier needs to settles sufficiently within 250 ns. While THA # 1 can take this much time for settling, we would prefer THA # 2 to take minimum amount of time for settling since we want to minimize the delay beyond *T/2*. Thus, it would be preferred if its GBW is maximized. One limit to maximizing the GBW is the large capacitance seen by THA

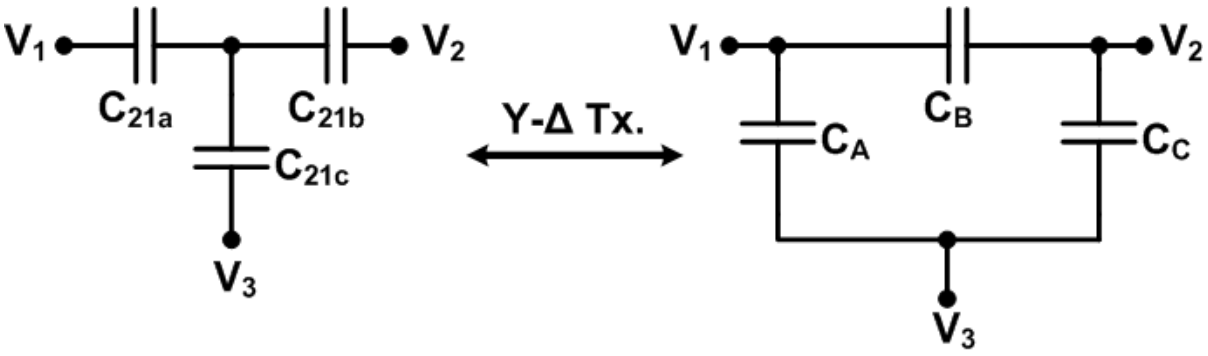


Figure 5.20: Basic concept of T-network approach (Star-Delta transformation).

2 due to the succeeding SCF stage. From Section 5.2.1, we can conclude that the loading would be 41.25 pF, which is extremely large, and can result in huge power dissipation in A_{THA2}. We have tackled this issue in design of SCF # 2 in the next section, and were able to reduce this value down to ~ 8 pF. We have employed the rail-to-rail amplifier topology shown in Fig. 5.19 for implementing the two THA amplifiers in Fig. 5.18. This topology ensures rail-to-rail input/output voltage operation for wide dynamic range. In essence, folded-cascode based complementary NMOS/PMOS input pairs can provide rail-to-rail ICMR. The worst case for stability is during mid-rail, when both the pairs are turned *On*. On the other hand, the worst case for GBW is at high/low rail, when only one of the pairs is *On*. This is assuming that the NMOS/PMOS input pairs are sized to have the same transconductance for a given bias current. In such a scenario, the worst case GBW is exactly half of the mid-rail GBW. The worst case GBW requirements can be calculated from the 5τ (= 250 ns) settling requirements of the THA # 2. Hence,

$$f_{GBW} \geq \frac{1}{2\pi} \times \frac{1}{\tau} = 3.2\ MHz \qquad (5.24)$$

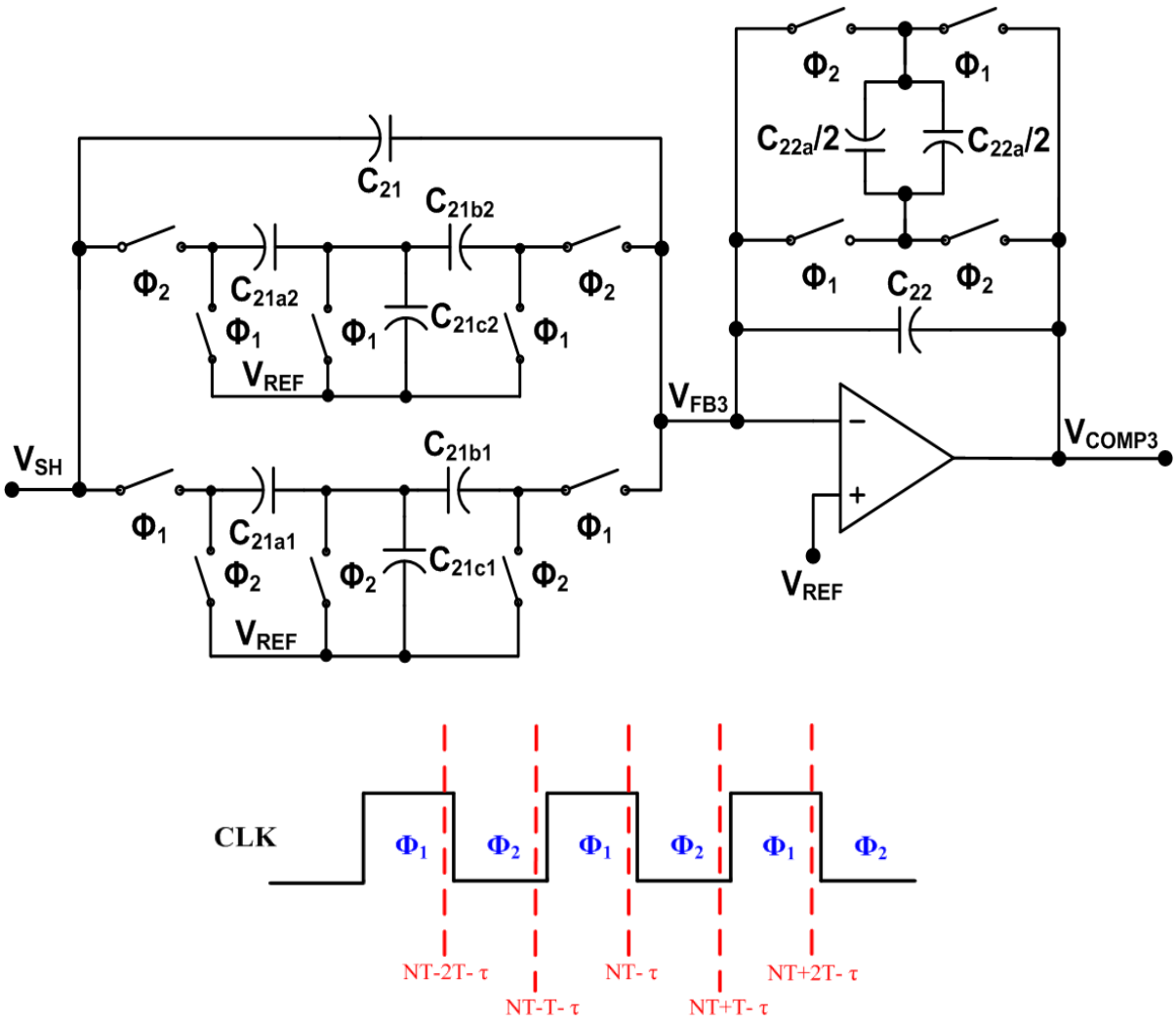


Figure 5.21: Proposed schematic of SCF # 2 and its associated switch phases.

In Fig. 5.18, we show the mid-rail monte-carlo simulation results for the THA # 2 amplifier design across PVT variations, to check for worst-case stability. It can be seen that the GBW is ensured to be more than 12 MHz for mid-rail input common-mode condition, and hence more than 6 MHz at high/low rails. Thus, we are able to ensure by design that the condition in (5.24) is satisfied across PVT variations. It must be added that the amplifier slewing is not

included in the settling requirements. This is a reasonable assumption for class-AB output stage based amplifiers, even when they experience large-signal transients. Fig. 5.19 shows the 0.5 V step response monte-carlo simulations results for mid-rail conditions for the amplifier under consideration.

5.4 SCF # 2

The large capacitance C_{11} (in Fig. 5.11) arises from the fact that C_{11a} needs a minimum size in order to meet the matching requirements and to ensure low variability in parasitic-sensitive SCF architecture. Thus, if we can find a way to realize a lower (effective) C_{11a}, we can lower the value of C_{11}, for the target sampling rate and zero time constant requirements. A T-network based integrator for synthesizing very large time constants is proposed in [31]. The underlying concept is shown in Fig. 5.20. We can write the following relationships for the same:

$$C_A = \frac{C^2}{C_{21b}}, C_B = \frac{C^2}{C_{21c}}, C_C = \frac{C^2}{C_{21a}}; \quad C^2 = \frac{C_{21a}C_{21b}C_{21c}}{C_{21a} + C_{21b} + C_{21c}} \tag{5.25}$$

Now, consider the Double-sampling T-network based switched-capacitor HPF, as shown in Fig. 5.21. The double-sampling input network is needed to support the BLT output network, operating on both clock phases. Hence, this leads to duplication of the T-network, and the two operate on complementary phases. We must also mention that the two networks are symmetrical and hence, $C_{21a,b,c1} = C_{21a,b,c2} = C_{21a,b,c}$.

Now, it can be seen that in phase Φ_2, capacitors $C_{21a,b,c1}$ are reset to the common mode voltage given by V_{REF}, while in phase Φ_1, these capacitors are connected to the SCF's

input voltage (V_{SH}) to share charge with the reset of the system via the isolated net at V_{FB3}. The equivalent capacitor that shares charge is given by C_B in Eq. (5.25). Using the expression for C_B and the principle of charge conservation, we can evaluate the transfer function of SCF # 2, as given in Eq. (5.26).

$$H_{SCF2}(z) = -\frac{C_{21}}{C_{22}} \frac{1 + \frac{C_{21a}}{C_{21}} \cdot \frac{C_{21b}}{C_{21c}} \cdot \frac{1}{\left(\frac{C_{21b}}{C_{21c}} + \frac{C_{21a}}{C_{21c}} + 1 \right)} \cdot \frac{1}{1 - z^{-1}}}{1 + \frac{C_{22}}{C_{22a}} \cdot \frac{1 + z^{-1}}{1 - z^{-1}}} \tag{5.26}$$

It is clear from the above equation that this is a hybrid methodology for zero and pole realizations. Now, we can choose the values of $C_{21a,b,c}$ to achieve the desired zero frequency. For the target zero frequency (20 KHz) and a sampling rate of 2 MHz, we get the following values of capacitances: C_{21} = 5 pF, C_{21a} = 3.5 pF, C_{21b} = 1 pF and C_{21c} = 10 pF. Thus, we get a total capacitance of 34 pF, which is not a significant reduction from the previous case of 41.25 pF. Ofcourse, the values of capacitors C_{22} and C_{22a} are unaffected.

Using Eq. (5.25), we get C_A = 2.4 pF, C_B = 0.25 pF and C_C = 0.69 pF. Thus, the benefit of the T-network approach is the dramatic reduction in the loading of the previous stage (V_{SH}) and given by $C_A + C_B + C_{21}$ = 7.65 pF compared to 41.25 pF in SCF # 1. Thus, we can achieve a fast THA # 2 amplifier stage (see Fig. 5.16) without burning too much power.

5.5 Gain Stage

A direct consequence of reduction in the effective switching capacitor value is the reduction in DC gain, if C_{22a} is unchanged. Hence, a non-inverting gain stage is required to compensate for this reduction, to meet the filter specifications as outlined in

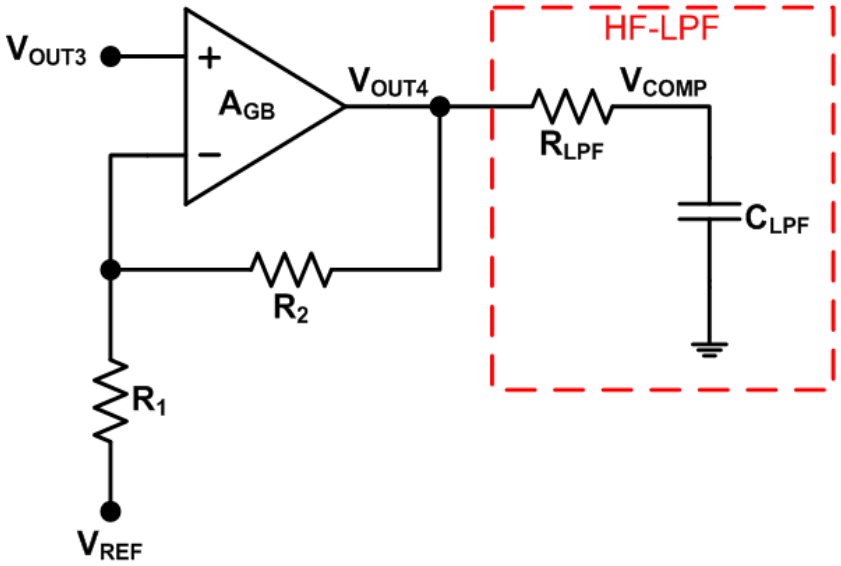


Figure 5.22: Gain-Block amplifier followed by a RC low-pass filter.

Section 4.1. This can easily be accomplished using the circuit in Fig. 5.22. The transfer function is given as:

$$\frac{1}{H_{GB}(s)} = \frac{1}{A_{GB}(s)} + \frac{1}{1+B_0} \tag{5.27}$$

Here, $A_{GB}(s)$ is the single-pole amplifier transfer function and B_0 is DC feedback factor.

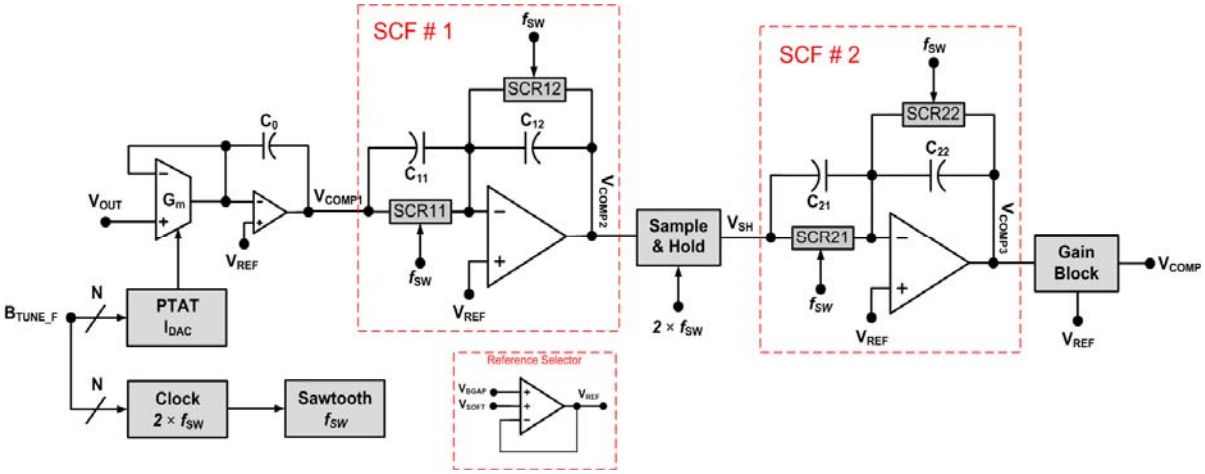


Figure 5.23: Final proposed Type-III SCF architecture.

$$A_{GB}(s) = \frac{A_0}{1 + s/s_0}; \quad B_0 = \frac{R_2}{R_1}$$

$$\therefore \frac{1}{H_{GB}(s)} = \frac{1}{A_0} + \frac{s}{A_0 s_0} + \frac{1}{1 + B_0} \approx \frac{s}{A_0 s_0} + \frac{1}{1 + B_0}$$

$$\Rightarrow H_{GB}(s) = \frac{1 + B_0}{1 + \frac{s(1 + B_0)}{A_0 s_0}} \tag{5.28}$$

Hence, it can be seen that the closed-loop system has a pole at the ratio of the amplifier's UGB and the DC gain ($1 + B_0$) of the system. Thus, the amplifier design needs to make sure that this parasitic pole is well outside f_{SW} (= 1 MHz) to avoid any degradation in phase margin. Finally, we Low-Pass Filter (LPF) the output voltage (V_{COMP4}) to provide a clean compensation (V_{COMP}) signal to the PWM comparator (see Fig. 1.6).

Thus, with the changes incorporated in the Type-III SCF architecture in Sections 5.2 – 5.5, we present the finalized schematic in Fig. 5.23. We have now represented the SCR implementations to be driven by f_{SW} as a result of double-sampling techniques employed.

Chapter 6

6. Practical Considerations for the Interfacing Circuitry

The Type-III SCF described in the previous section needs to be interfaced with auxiliary circuits to produce the final Pulse-Width Modulated (PWM) signal for closed-loop control of the Buck converter (see Fig. 1.6). These will be discussed in the following sub-sections:

6.1 Double-sampling SCF considerations

For SCFs employing doubling-sampling techniques, it is important that the mismatch between the two sampling paths is minimized [32]. The impact of mismatch is more severe in the case of SC-HPFs, since any spurious high-frequency content gets implicitly amplified. The mismatch can arise from two sources:

a. Sampling Capacitor Mismatch

   The mismatch between the sampling capacitors can lead to unequal charge sharing in the two double-sampling paths. This can firstly be minimized by choosing a given unit capacitor size, which is already considered for the accuracy of the time constants being realized. In our design, a matching accuracy of better than 1 % is ensured. In addition, as was described in Section 5.2, we have ensured symmetric bottom-plate parasitics since the SCF design is parasitic-sensitive. Finally, careful layout is required in order to make the two paths highly symmetric.

b. Clock Duty-cycle Mismatch

The effect of mismatch in the clock duty-cycle in a double-sampling SCF architecture is similar to the path mismatch error occurring in the two half-cycles of the clock. This effect is known as non-uniform sampling [32]. We were able to model this effect in simulations, by introducing a fixed duty-cycle mismatch, and were able to ensure the robustness of the proposed architecture for up-to 2 % mismatch. As described in Section 6.3, we have ensured by design that these design requirements are met via the proposed SCF clocking scheme.

6.2 DC Coupling Effect

The switched-capacitor network behaves like a resistor at DC (and at frequencies much lower than the sampling rate), which was also concluded in Section 2.1. Based on this, we can deduce that the proposed Type-III SCF is equivalent to the circuit in Fig. 6.1 at DC (and low frequencies). Here, we have excluded the SHA stage for the sake of simplicity.

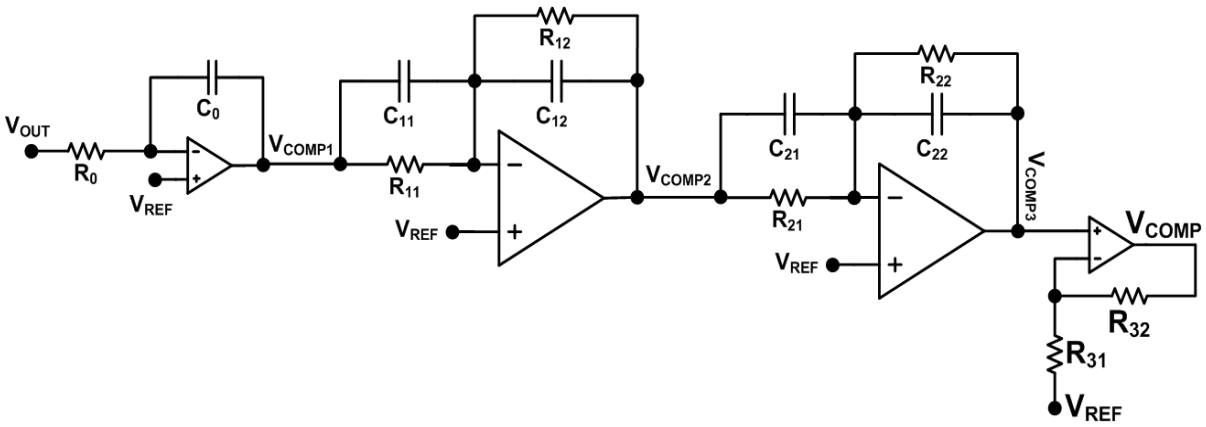


Figure 6.1: Equivalent Type-III SCF architecture at low frequencies.

It can be seen from Fig. 6.1 that the 1st stage (integrator) is AC coupled to V_{OUT}. Thus, V_{COMP1} can assume any voltage within the rails for any given value of V_{OUT} (and hence V_{REF} since V_{OUT} follows V_{REF} in closed-loop configuration). Now, it must be seen that V_{COMP1} is DC coupled to V_{COMP}, and indirectly also to the intermediate voltages V_{COMP2} and V_{COMP3}. Thus, at steady-state, the various filter voltages are directly dictated by V_{COMP} signal, which is dependent on the sawtooth waveform and the duty cycle value. Now, the following relations hold, assuming zero offset amplifiers in the signal chain:

$$V_{COMP3} = \frac{1}{R_{31} + R_{32}} \times \left(R_{31} \times V_{COMP} + R_{32} \times V_{REF} \right) \tag{6.1}$$

$$V_{COMP2} = V_{REF} + \frac{R_{21}}{R_{22}} \times \left(V_{REF} - V_{COMP3} \right) \tag{6.2}$$

$$V_{COMP1} = V_{REF} + \frac{R_{11}}{R_{12}} \times \left(V_{REF} - V_{COMP2} \right) \tag{6.3}$$

It can be seen from (6.1) – (6.3) that if V_{COMP} deviates too far from V_{REF}, the various voltages can get saturated to either the positive or negative rail. Thus, it would be best if V_{COMP} follows V_{REF}, and it would also be the case during soft-start conditions as well. Another way to view this situation would be by considering that there is only a given range of V_{COMP} that can be accommodated within the rail without saturating one or more amplifiers in the signal chain (at any given V_{REF}). While we are assuming a DC operating point for this case, we must also understand that V_{COMP} will fluctuate above/below the steady-state value during line/load transients and soft-start. In addition, the situation is exacerbated by the fact that the amplifiers and the PWM comparator will have offsets. These effects can severely limit the

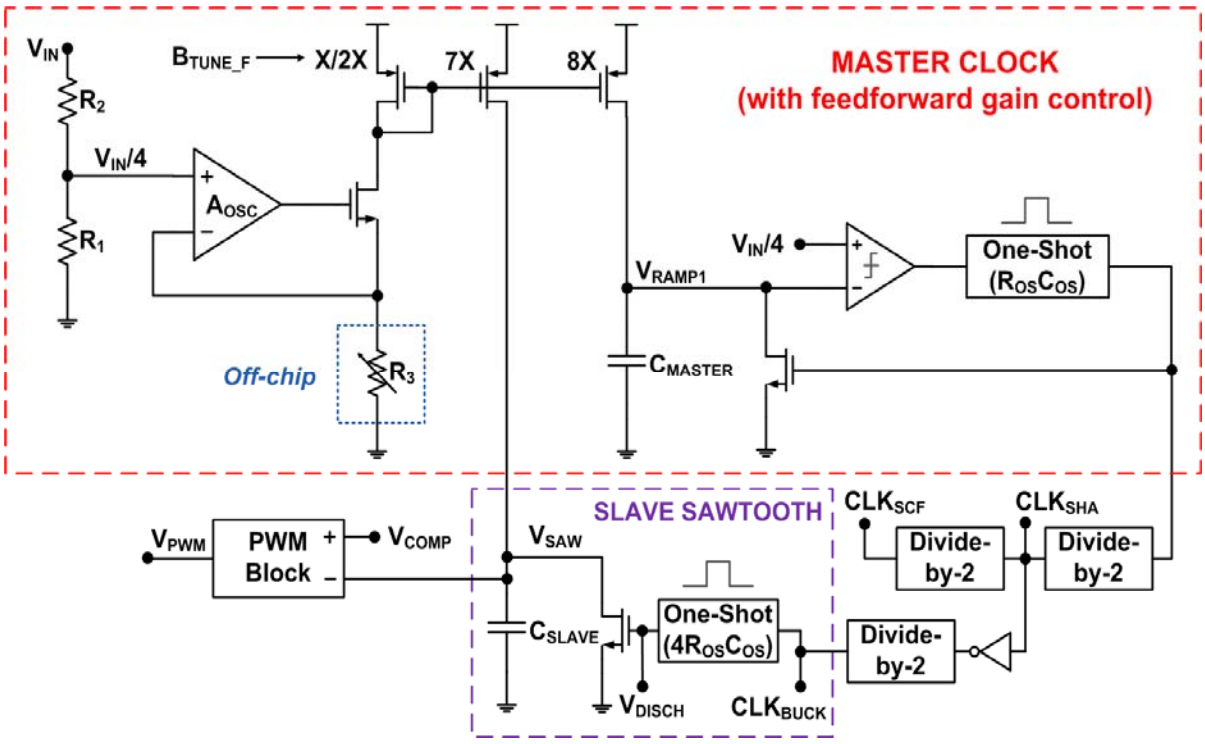


Figure 6.2: Proposed clocking scheme for the Type-III SCF architecture.

dynamic range of the proposed Type-III SCF. To alleviate this problem, we have carefully designed the sawtooth waveform generator and PWM comparator in the following sub-sections.

6.3 Proposed Clocking Scheme

The clocking scheme for the proposed SCF is shown in Fig. 6.2. Firstly, as discussed in Section 6.1, we have tried to ensure that the duty cycle mismatch is minimized for the double-sampling SCF architecture. For this, we have generated a master clock operating at frequency $4 \times f_{SW}$, having a duty-cycle given by $R_{OS} \times C_{OS}$. Thereafter, the master clock is divided-by-2 to generate the SHA clock ($2 \times f_{SW}$). The SHA clock is further divided-by-2 to

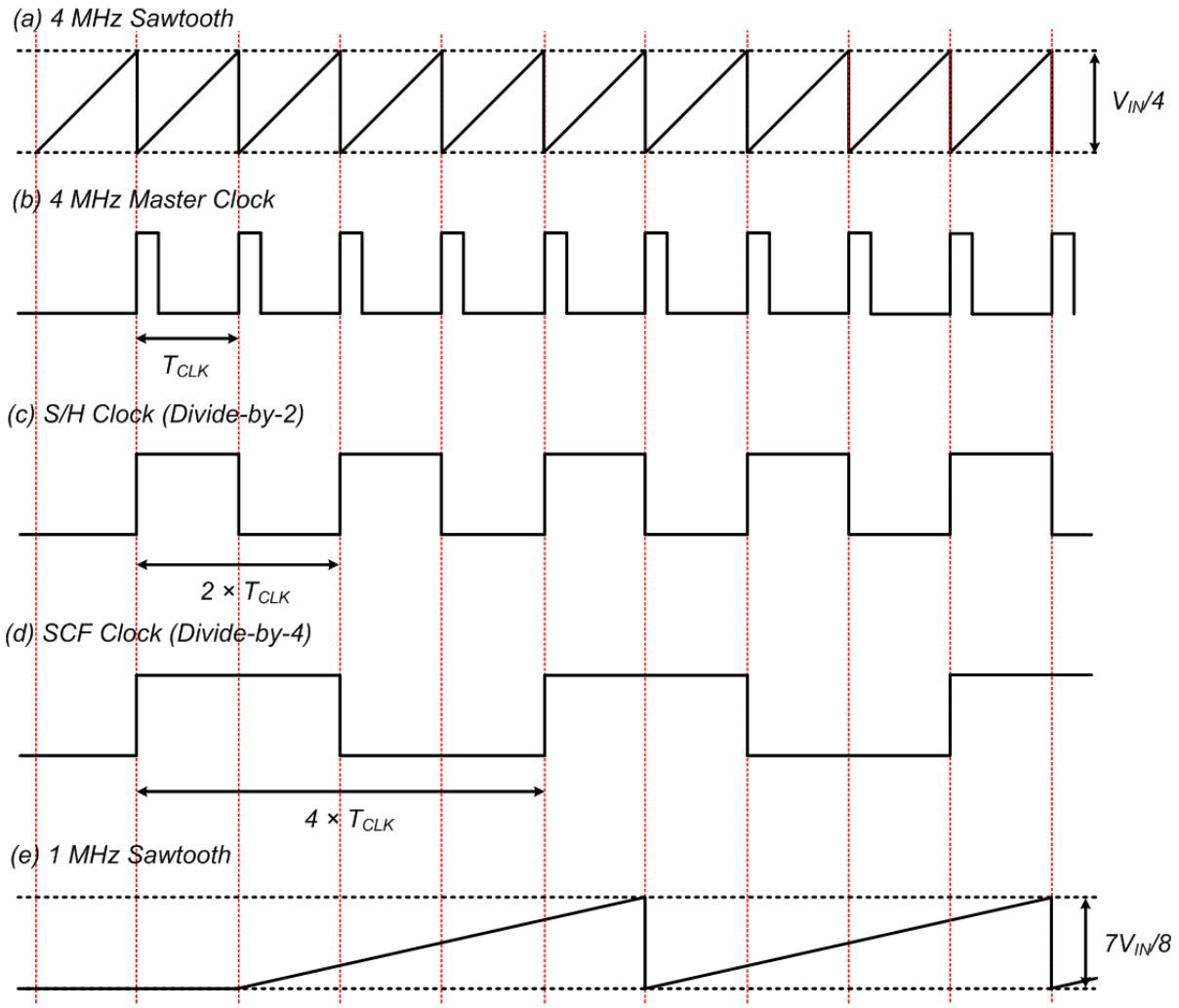


Figure 6.3: Various clock and sawtooth waveforms for the case f_{SW} = 1 MHz.

generate the SCF clock operating at f_{SW}. It must hereby be understood that it is very difficult to directly generate a clock having low duty-cycle mismatch, and hence dividing a higher frequency clock is a very effective mechanism for ensuring these specifications. Thereafter, the only duty-cycle mismatch arises due to the jitter present in the master clock, which can be typically < 1 % for clocks in the MHz range. We were able to confirm via simulations by

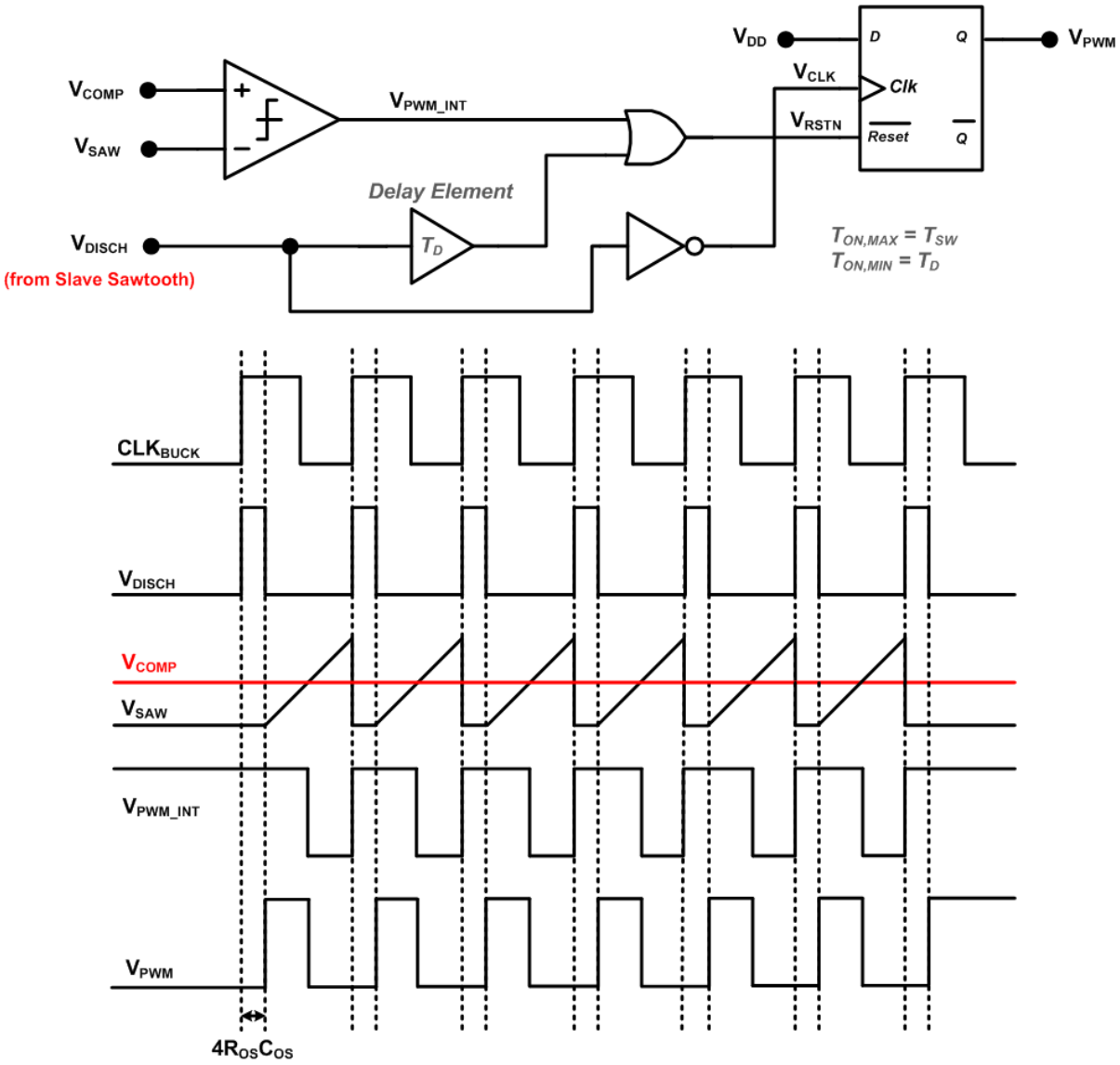


Figure 6.4: PWM Comparator Block and its associated waveforms.

introducing a hard jitter, that this is indeed a sufficient criterion to ensure a safe operation for the SCF. As can be seen from Fig. 6.2, the master clock has relaxation oscillator architecture, which can be configured to operate at either 2 MHz or 4 MHz based on the configuration bit given by B_{TUNE_F} = [0, 1]. The master clock architecture can be extended to

generate the sawtooth waveform generator for ensuring a fixed feed-forward gain given by: $V_{IN}/|V_{SAW}| = 8/7$, which is implicitly ensured for both configurations of B_{TUNE_F}. In addition, we have also ensured a near rail-to-rail sawtooth waveform generator to provide wide dynamic range for a robust SCF operation (as discussed in Section 6.2). Finally, the various waveforms are shown in Fig. 6.3, assuming zero delays for both the comparator and one-shots in Fig. 6.2.

6.4 PWM Comparator Block

The PWM comparator block has two important design requirements:

1. We need to synchronize the PWM pulse with the sawtooth ramp start, in order to eliminate the impact of the slave sawtooth's (see Fig. 6.3) one-shot time constant variation ($4 \times R_{OS} \times C_{OS}$) from the target V_{COMP} value. While the asynchronous PWM comparator's delay can also impact the target V_{COMP} value, this delay is not as significant. In addition, it can be precisely controlled by choosing PTAT biasing current for the comparator. The proposed PWM comparator block and the associated timing waveforms are shown in Fig. 6.4. As can be seen from the waveforms, the D Flip-Flop (DFF) synchronizes the PWM pulse with the sawtooth ramp, and hence $V_{COMP} \sim 7/8 \times V_{REF}$. In addition, the DFF also ensures that there is no spurious switching during the entire switching cycle. Thus, this provides a robust solution with low jitter and controlled EMI performance. It is also important to notice that the proposed circuit can allow duty-cycles from almost 0 to 1, thereby facilitating a good load transient response for the closed-loop system.

2. A rail-to-rail ICMR for the asynchronous PWM comparator front-end needs to be ensured in order to accommodate the near rail-to-rail sawtooth waveform, as described in Section 6.3. The circuit schematic for this comparator is shown in Fig. 6.5. As can be seen it has complementary NMOS/PMOS input pairs acting as transconductance elements summing currents onto the nodes V_{OUTP1} and V_{OUTM1}. For the NMOS input pair, the load is a diode-connected low-V_{THP} PMOS option available in the technology. This allows ICMR to go beyond the V_{DD} rail. The high ICMR can be given as:

$$V_{CM,H} \leq V_{DD} + V_{THN,B} - \left|V_{THP,L}\right| - V_{DSAT} \tag{6.4}$$

Here, $V_{CM,H}$ is the high ICMR of the comparator, V_{DD} is the supply rail, $V_{THN,B}$ is the threshold voltage of the input NMOS pair (with body-effect), $V_{THP,L}$ is the threshold voltage of the low-V_{TH} PMOS load transistor and V_{DSAT} is its overdrive voltage. Under nominal conditions, V_{THN} = 0.7 V, $V_{THP,L}$ = - 0.3 V, and V_{DSAT} = 0.2 V. Hence, even without the input NMOS pair's body-effect:

$$V_{CM,H} \leq V_{DD} + 0.2\,V \tag{6.5}$$

For the PMOS input pair, the low ICMR is given by:

$$V_{CM,L} \geq V_{THN} - \left|V_{THP,B}\right| + V_{DSAT} \tag{6.6}$$

Here, $V_{THP,B}$ is the input PMOS threshold voltage with body-effect. Under nominal conditions, V_{THP} = - 0.9 V. Thus, even without input-pair PMOS' body-effect:

$$V_{CM,L} \geq 0\,V \tag{6.7}$$

The biggest motivation for using such a structure compared to a folded-cascode structure for ICMR enhancement is that the latter can severely limit the speed of the comparator,

by introducing extra biasing transistors. This structure, with fewer transistors offers faster settling time for a given current consumption. To increase the speed further, we have employed local negative feedback in the 1st stage of the comparator. This feedback limits the voltage swing on the 1st stage during positive or negative slewing events, thereby allowing it to respond faster to the transients. However, care must be taken during design to ensure that it does not interfere with the operation of the final stage of the comparator across PVT variations. We were able to achieve ~ 20 ns of delay at f_{SW} = 1 MHz and nominal conditions using this structure, while consuming 35 µA of bias current.

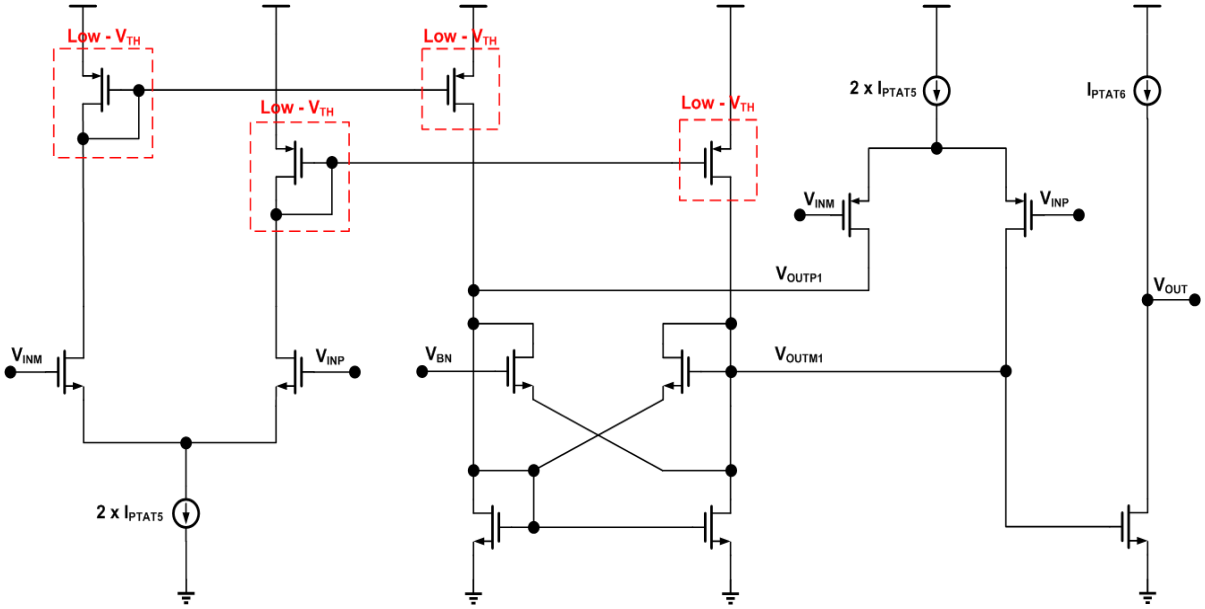


Figure 6.5: Rail-to-rail ICMR asynchronous PWM Comparator.

Chapter 7

7. Simulation Results

In this section, we will present and discuss the simulation results of the proposed Type-III SCF. We will first show the frequency response of the proposed filter and compare it with the desired filter response. In addition, we will compare the transient step response performance of the proposed Type-III SCF with its analog counterpart.

7.1 Open-Loop Frequency Response

The frequency response of the SCF cannot be directly simulated using standard techniques of small-signal AC analysis about a DC operating point. The reason is that the SCF does not have a steady-state operating condition. Intuitively, this is because an SCF is a switching circuit having an operating point which is "periodic" in time. The period is really equal to the sampling time period of the filter. Hence, the simulator first calculates the steady-state operating point of the SCF using Period Steady-State (PSS) analysis in SpectreRF (by Cadence) [24]. Thereafter, small time-varying signals are applied on top of this operating point to evaluate the frequency information from the same. This simulation is a part of the Periodic AC (PAC) analysis [24]. Clearly, in order to obtain high-frequency information from PAC, the PSS would have to calculate smaller time step information.

The PSS/PAC simulator has an advantage over other simulators like SWITCAP [25] that it can be used to simulate transistor models, which can be used to model the various PVT variations. In addition, several non-idealities like Opamp finite gain-bandwidth/slewing,

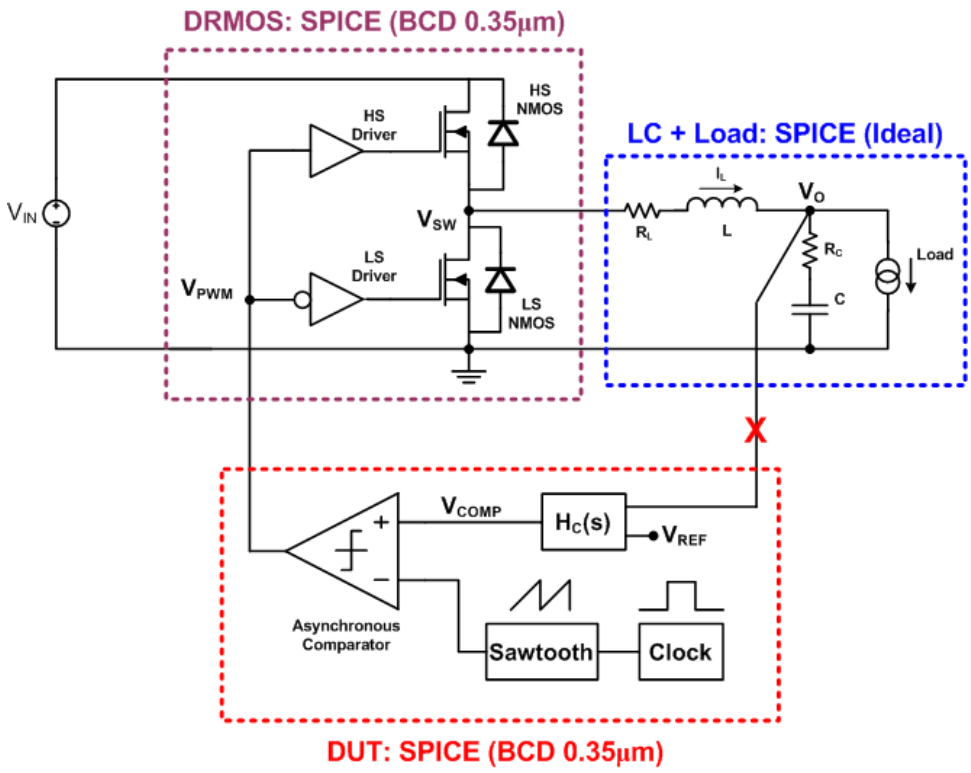
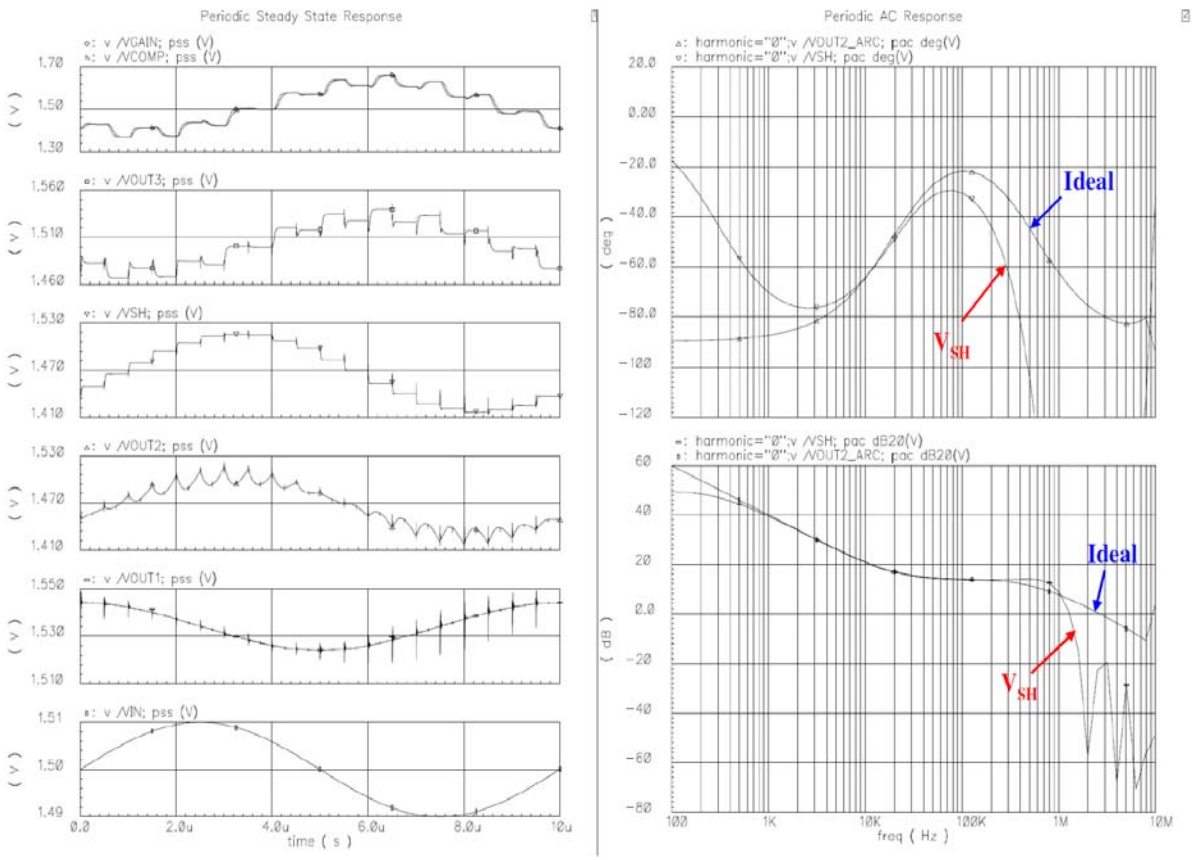


Figure 7.1: Simulation setup for characterizing the DUT.

effects of parasitics, mismatches between various charge-transfer paths and non-linearity/charge injection of switches can all reflect themselves upon the frequency response. Hence, these simulation results are extremely realistic. Finally, it must be added that PSS/PAC analysis can be applied to any switching circuit with a periodic operating point such as RF mixers and oscillators. Hence, it is also applicable to switching power converters, which can be part of the same simulation environment, giving us a *unified* simulation strategy.

Fig. 7.1 shows the complete simulation setup for the characterization of the proposed Device Under Test (DUT), which is the Type-III SCF and the PWM modulator. Thus, the

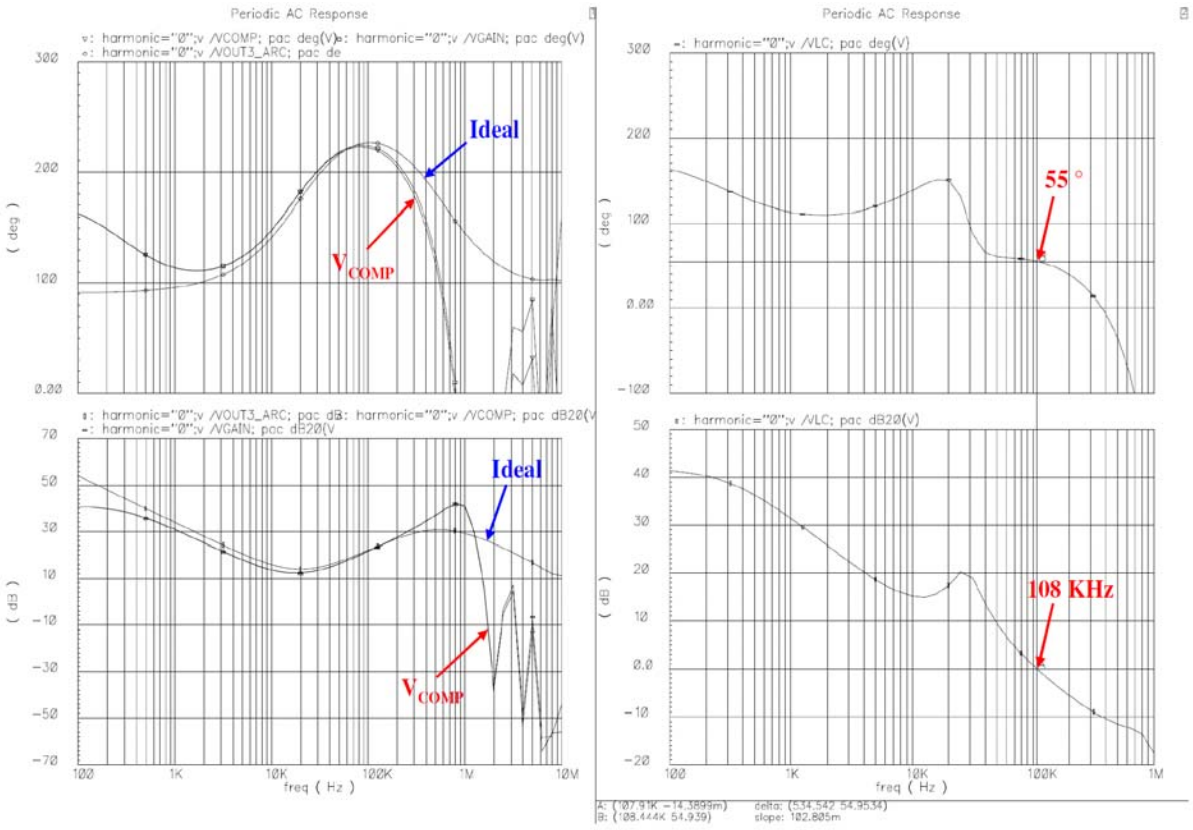


(a) (b)

Figure 7.2: Simulation of Fig. 7.1 showing results for (a) PSS (b) PAC (V_{SH}).

DUT is a SPICE-level netlist that contains only the models from TI's 0.36-µm BCD process. In addition, we have a reference design in the same process for DRMOS (Drivers and MOSFET) from I_{LOAD} = 1.5 A part. Finally, the LC filter and the load are modeled by ideal SPICE components. This setup is consistent with the fact that only the LC filter is realized by using discrete components for our target application (see Section 1.1).

Now, the PSS/PAC analysis is conducted in open-loop configuration for the case f_{SW} = 1 MHz (Figs. 7.2 and 7.3). The feedback loop is broken at the input to the compensator



(a) (b)

Figure 7.3: Simulation of Fig. 7.1 showing PAC results for (a) V_{COMP} (b) V_{OUT}.

(indicated by the red cross in Fig. 7.1). At this point, a tone at a frequency of 100 KHz is injected with DC voltage equal to the V_{OUT} value (= V_{REF}) at 1.5 V as a reference case. As can be seen from the PSS results in Fig. 7.2a, the simulation converges with a time period of 10 µs. In this time, both the low and high frequency content is captured. It can be seen that although the intermediate SCF signals ($V_{COMP1,2,3}$ and V_{SH}) have some high-frequency switching transients, the final V_{COMP} (topmost trace) signal is quite clean. This is important if the switching jitter needs to be minimized for the Buck converter.

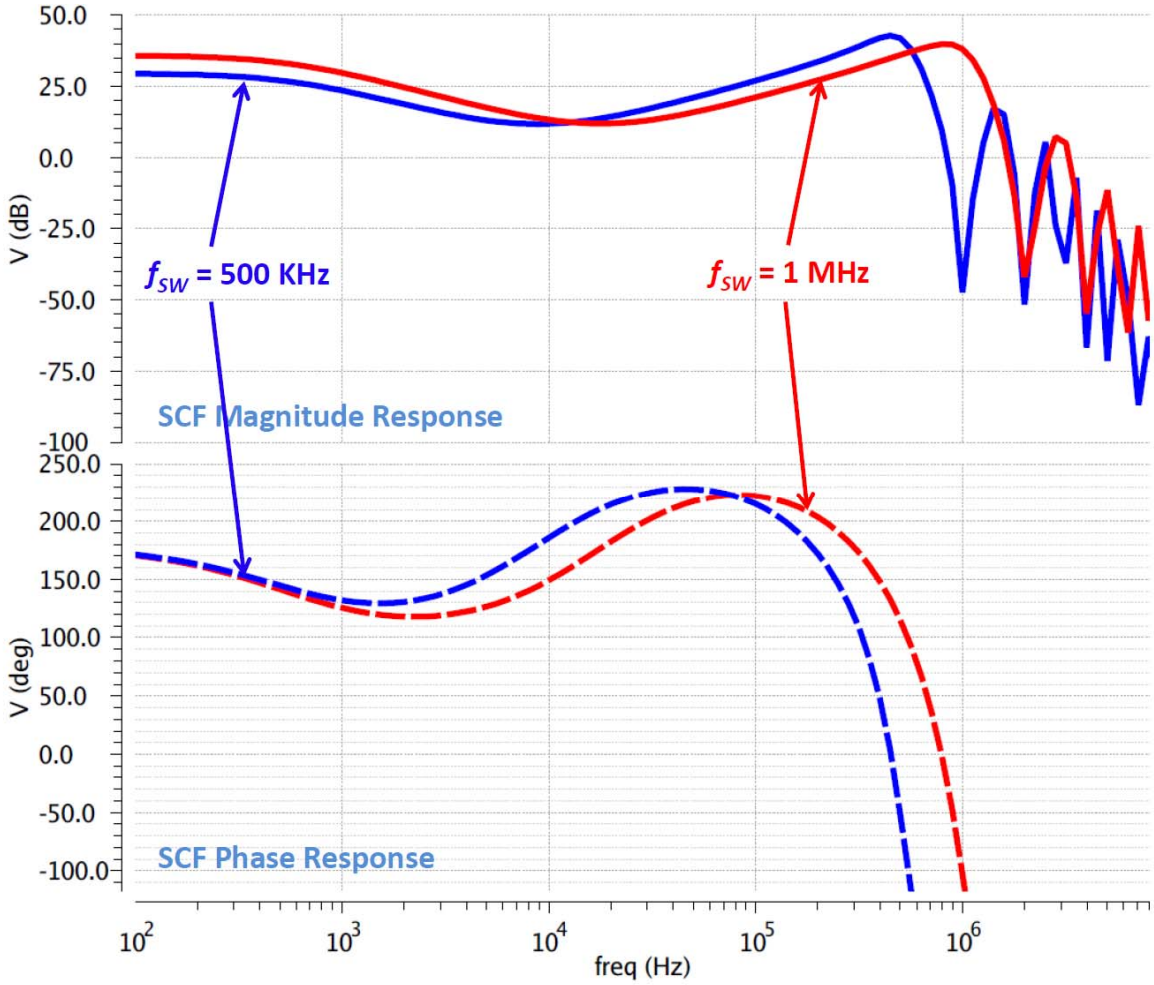


Figure 7.4: Simulation of Type-III SCF showing PAC results B_{TUNE_F} = [0, 1].

The PAC results for the V_{SH} signal is shown in Fig. 7.2b, which must be compared with the V_{COMP2} signal in Fig. 1.19. It can be seen that the DC gain is lower than the expected value. This is because of the fact that the integrator needs to be made lossy in order for it to have a stable DC operating point in open-loop configuration. However, the integrator bandwidth and the zero frequency are as expected. As discussed in Section 5.2.2, the pole has now become complex. It can also be observed that the sample-and-hold effect produces nulls at multiples

of f_S (= 2 × f_{SW} = 2 MHz) in the magnitude response, but has little effect in the edegradation is somewhat compensated by the extra degree of freedom we have with the T-network in SCF # 2. Thus, we adjust the DC gain and zero frequency of SCF # 2 to get the response as shown in Fig. 7.3a. As can be seen from the final open-loop response (output of Buck) in Fig. 7.3b, a phase margin of 55° and a Unity-Gain Bandwidth of 108 KHz is achieved at nominal conditions of process and temperature.

To check the scalability of the Type-III transfer function w.r.t. the switching frequency (f_{SW}), we have checked the PAC results for the two configurations of B_{TUNE_F} = [0, 1], corresponding to f_{SW} = 0.5 and 1 MHz, respectively. The results are shown in Fig. 7.4 for nominal conditions, and we can see that the filter transfer function scales linearly. Once again, the gain degradation at low frequencies (and DC) is attributed to the integrator made lossy to stabilize the DC operating point of the filter operating in open-loop configuration.

7.2 Closed-Loop Transient Response

The same setup in Fig. 7.1 is used for evaluating the closed-loop load transient step response for three different cases: In the first case, we have used the conventional analog Type-III filter as shown in Fig. 1.9. In the second case, we have used the cascaded version of the continuous-time analog Type-III filter as described in Fig. 4.1. In the third and final case, we have employed our proposed SCF based Type-III compensation (Fig. 5.23). In all cases, we have employed amplifiers with limited GBW (= 20 MHz), and no slewing distortion. In addition, the feedforward gain is made unity for all cases (V_{IN} = $|V_{SAW}|$). All these measures are undertaken to compare truly linear settling response of all the three filters under

Table 7.1: Open-loop frequency response of various Type-III filter embodiments

Type-III Filter Topology	Bandwidth	Phase Margin	Gain Margin
Conventional ARCF	118 KHz	61.4°	15.0 dB
Cascaded ARCF	114 KHz	55.9°	13.1 dB
Cascaded SCF	112 KHz	54.8°	9.9 dB

consideration. Finally, as can be seen in Table 7.1, the three filters are designed for near-similar closed-loop frequency responses for a given Buck Converter power stage (f_{LC} = 29 KHz and f_{ESR} = 1 MHz) at a given switching frequency, f_{SW} = 1 MHz. It can be seen that compared to the conventional Type-III filter, both the continuous- and discrete-time filters, implemented via cascaded sections, have lower phase and gain margin. This can be directly attributed to the presence of parasitic complex-poles in the filters' transfer function. This effect was observed and quantified in Section 5.2.2.

The closed-loop load step (0 – 1.5 A) responses of the conventional ARCF, cascaded ARCF and cascaded SCF (with near-similar frequency responses) are shown in Figs. 7.5 – 7.7, respectively. It can be seen that the cascaded filters (both ARCF and SCF) show slight degradation in undershoot/overshoot compared to the conventional ARCF, which can be directly attributed to their slightly degraded frequency responses. It is interesting to observe that while the SCF has a sample-and-hold delay, its impact is completely modeled by its analog frequency response, and has little impact on the closed-loop transient. It must be also be understood here that this sampled-data (discrete-time) analog filter is part of another sampled-data system (switched-mode buck converter), whose sampling rate is lower (half) than that of the compensation filter. Thus, the sampling present in the compensation filter has

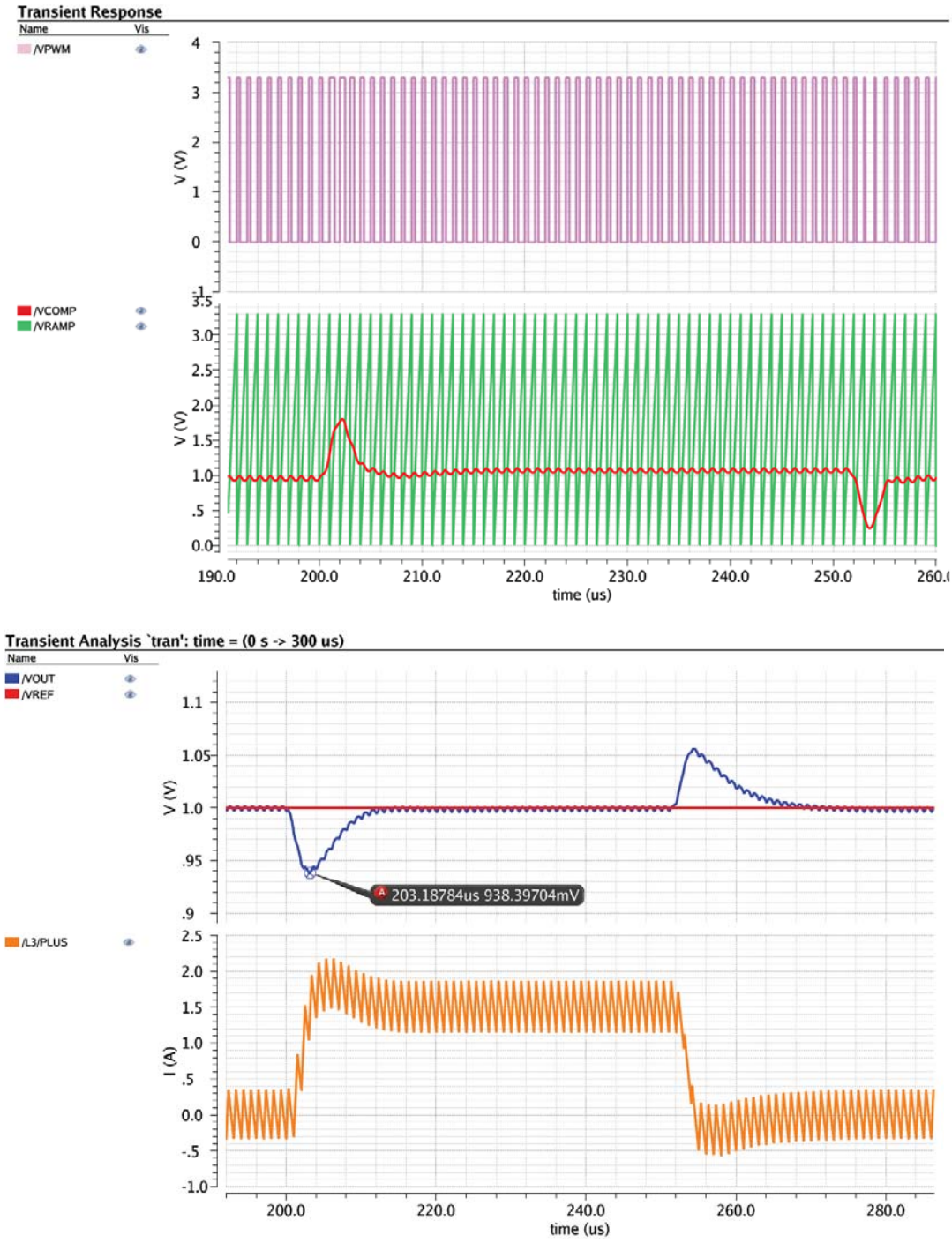


Figure 7.5: Simulation of load step response for conventional ARCF in Fig. 1.9.

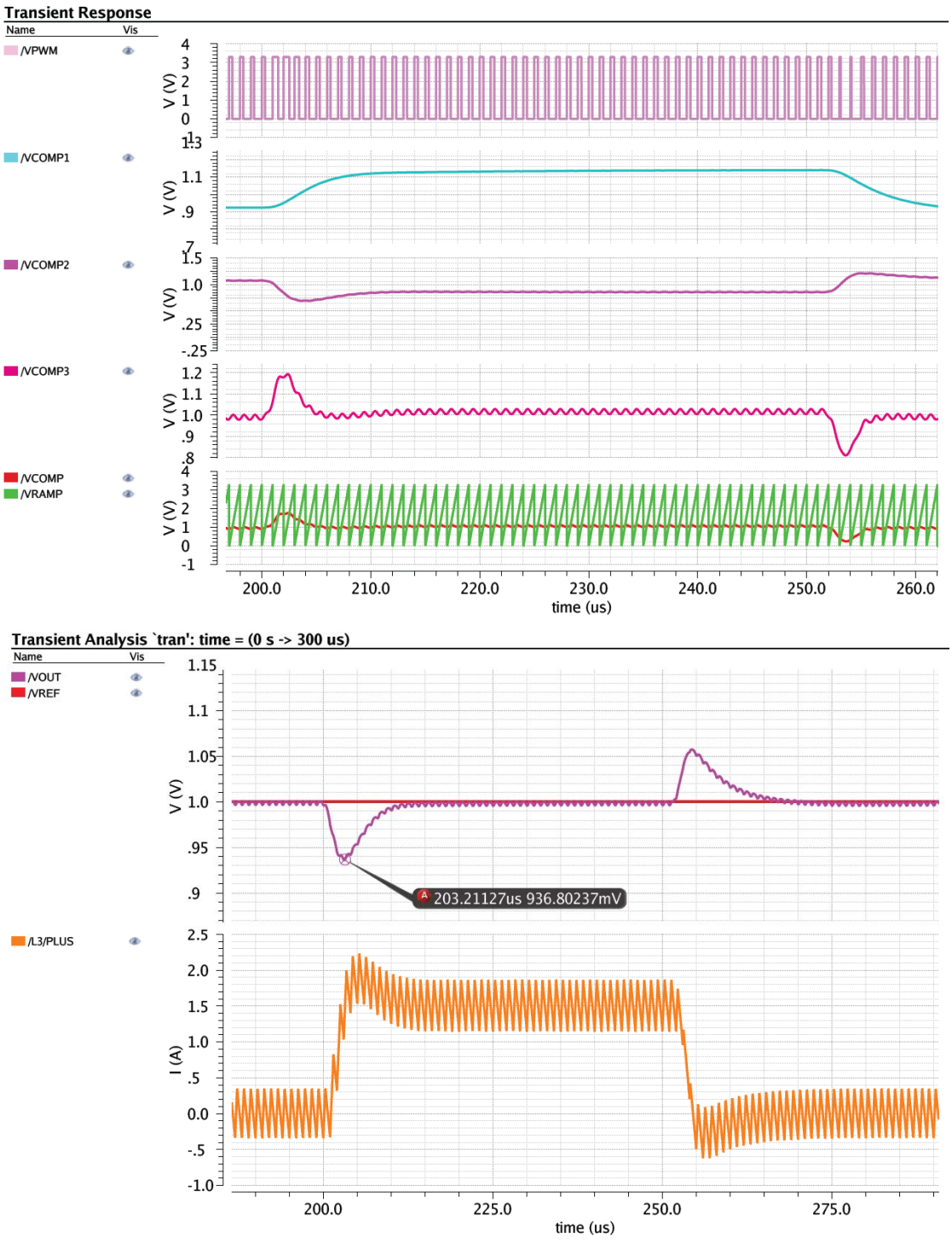


Figure 7.6: Simulation of load step response for cascaded ARCF in Fig. 4.1.

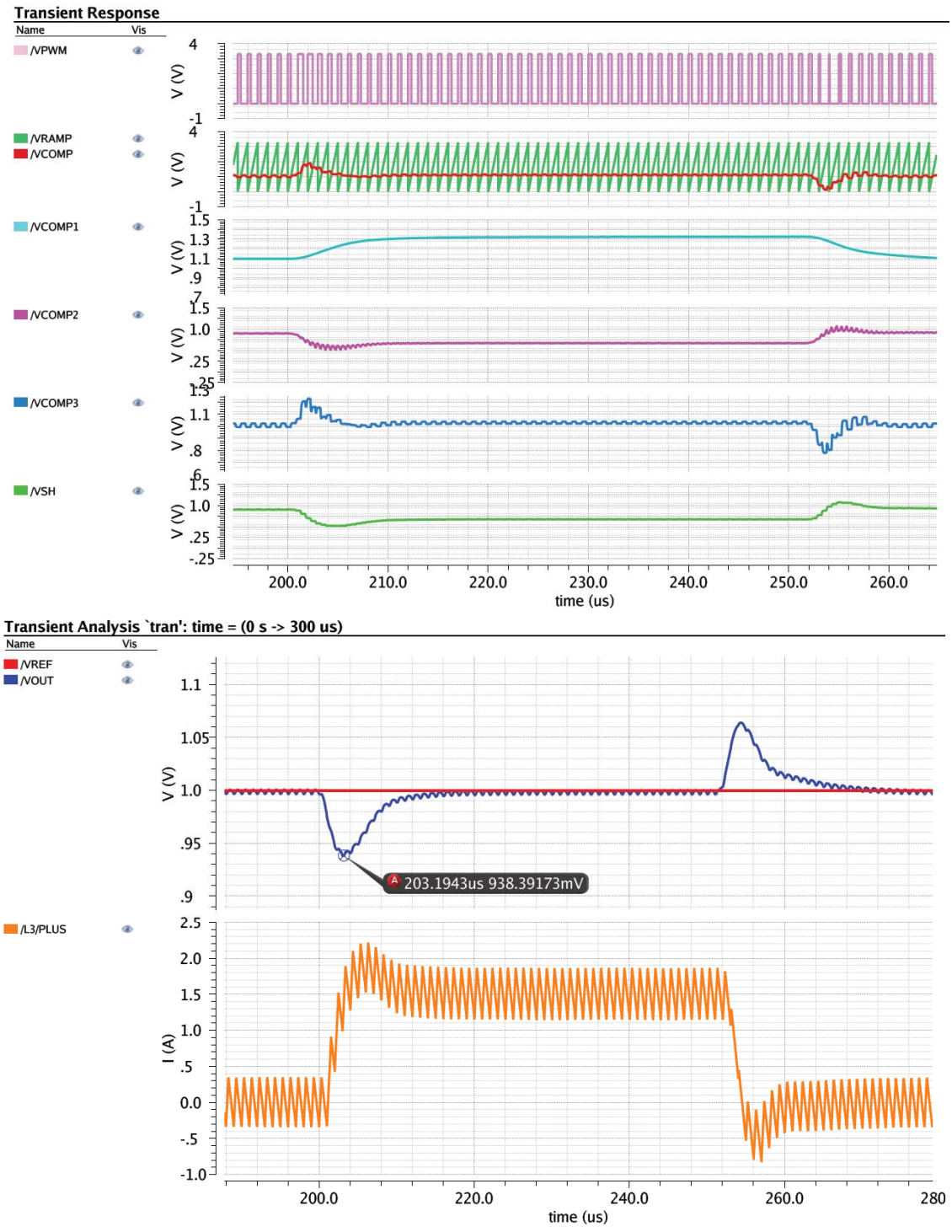


Figure 7.7: Simulation of load step response for cascaded SCF in Fig. 5.23.

little impact on the performance of the complete system, being compensated via a low-frequency (cutoff frequency at $f_{SW}/10 - f_{SW}/5$) linear control methodology. Thus, we can conclude that the proposed filter theory can have a wide applicability.

Chapter 8

8. Measurement Results

8.1 Power and Area Summary

The power consumption of various components of the proposed Type-III SCF is shown in Table 8.1. It can be seen that the total current consumption is ~ 1.1 mA from a 3.3 V supply voltage. This current consumption is lower than both the analog and digital implementations of this filter (see Section 1.2). The on-chip area consumed by this filter is a strong function of the total on-chip capacitance. In Table 8.2, we show the values of the various capacitors required to realize the proposed SCF in Fig. 5.23. The total capacitance is

Table 8.1: Nominal current consumption of the Type-III SCF

Design Block	**Static Current**
G_m–C OTA Stage	30 μA
G_m–C Buffer	105 μA
SCF # 1 Amplifier	110 μA
SCF # 2 Amplifier	105 μA
THA # 1 Amplifier	110 μA
THA # 2 Amplifier	120 μA
Gain Block	60 μA
Reference Selection Buffer	90 μA
PWM Comparator	35 μA
Master Oscillator	40 μA
Associated Bias Circuitry	240 μA
Bandgap Reference	60 μA
Total Static Current	*1105 μA*

Table 8.2: Capacitor values and area of the Type-III SCF

Capacitor	Value
C_1	14 pF
C_{11}	40 pF
SCR11	1.25 pF
C_{12}	1 pF
SCR12	1.25 pF
C_{21}	5 pF
SCR21	29 pF
C_{22}	1 pF
SCR22	1.25 pF
Total SCF Capacitance	*90 pF*
Capacitance Area (C_{P1P2})	*0.135 mm^2*

~ 90 pF. This capacitance is implemented using the highly-linear Poly2-Dielectric-Poly1 layers on the chip (available in most standard CMOS processes), and has a density of ~ 1.5 fF/μm^2. Thus, the area consumed is ~ 0.135 mm^2. However, it must be added that a considerable amount of area is also consumed due to the presence of several active elements in the proposed architecture. Fig. 8.1 shows the micrograph of the fabricated die in Texas Instruments' 0.36-µm BCD process. The filter active area is ~ 0.4 mm^2 while the controller's total active area is ~ 0.65 mm^2. It must be mentioned here that since the SCF architecture is parasitic-sensitive employing double-sampling techniques, the layout must be carefully handcrafted in order to:

1. Minimize parasitics on the charge-sharing nodes of the switching capacitors to minimize inaccuracies and mismatch.

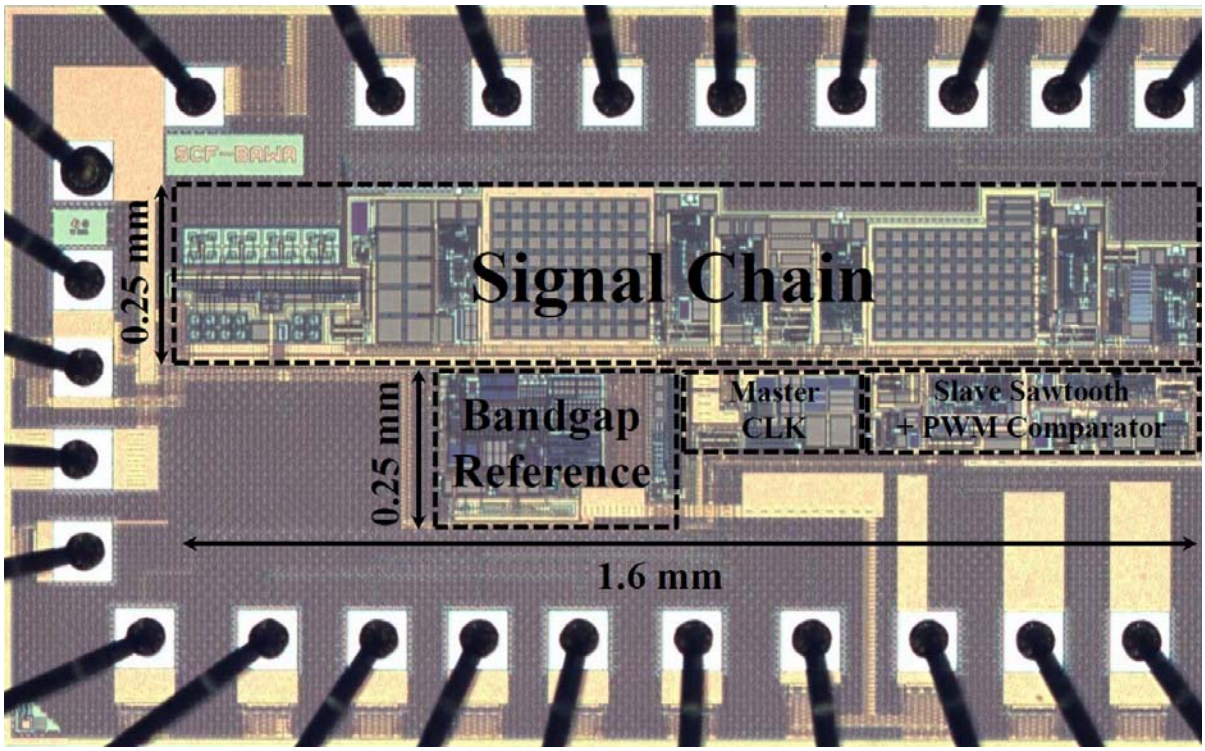


Figure 8.1: Die photo of the proposed Type-III controller IC.

2. Shield the feedback nodes of the SCF amplifiers from clock signals (having high dV/dt) in order to prevent any stray charge injection via coupling.
3. For double-sampling SC-HPF#2, ensure that the two sampling paths are symmetrically laid-out to minimize any mismatch in parasitics in order to prevent any spurious tones in the output spectrum.

It must be mentioned here that the focus of this work was to build a *first* working prototype and hence we did not pay special attention to power and area optimizations. As can be seen from Table 8.1, a lot of static current is dissipated in the associated bias circuitry for the

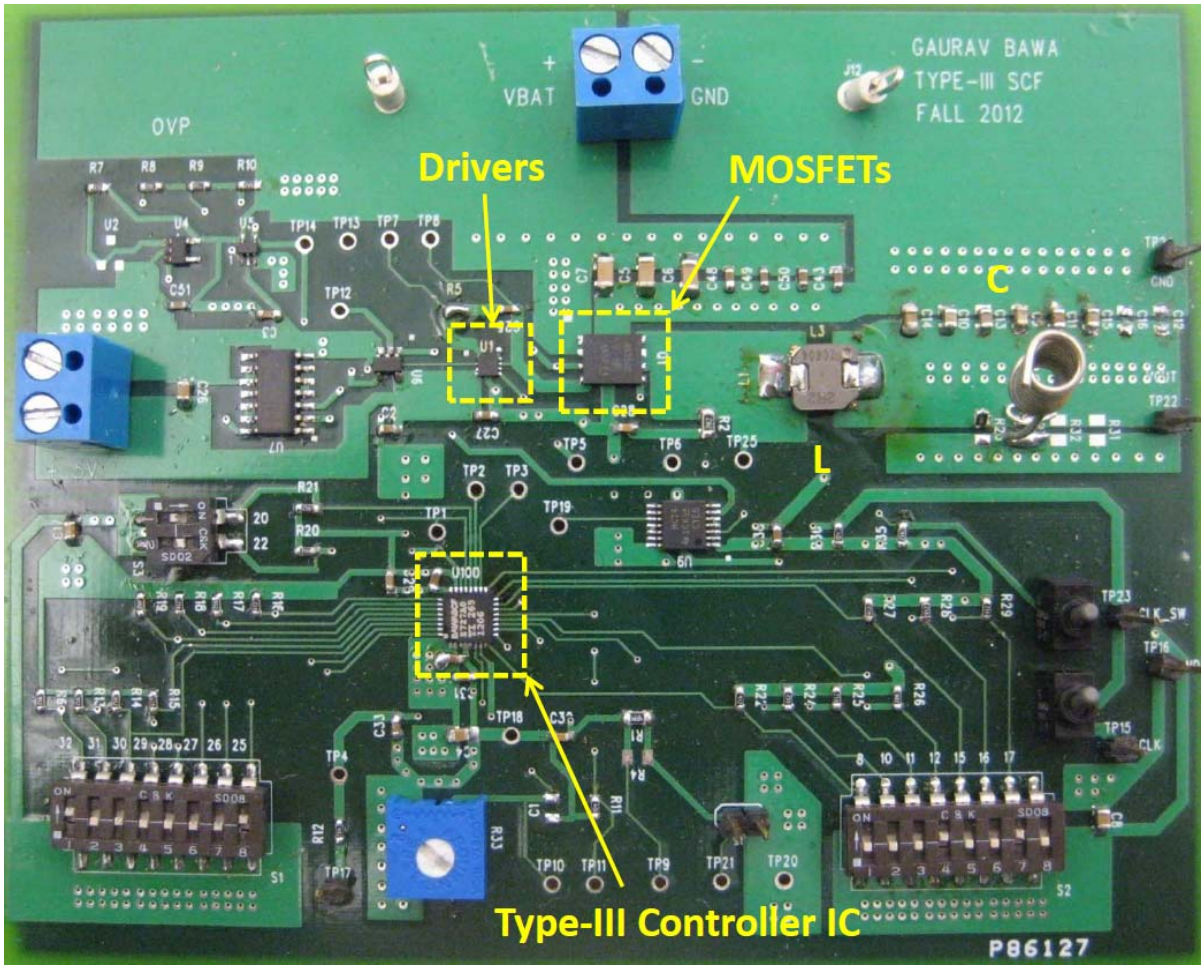


Figure 8.2: PCB photo for testing the proposed controller IC with Buck converter power stage.

analog blocks. Hence, the area and power performance can be improved further via simple design and layout optimization.

8.2 Measured Results

We designed and laid-out a 4-layer FR4 PCB for testing the functionality of the filter. The chip was bonded to a 32-pin QFN package and directly soldered onto the Printed Circuit

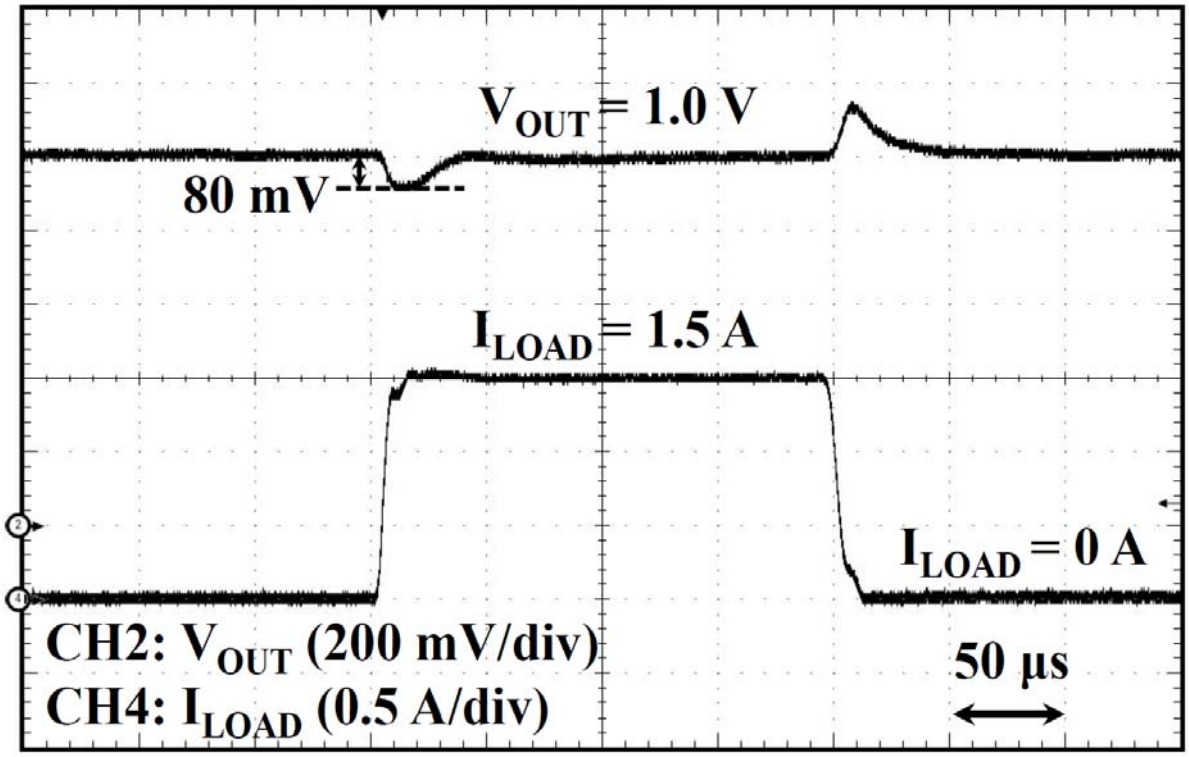


Figure 8.3: Measured waveforms showing the load step transient at f_{SW} = 0.5 MHz.

Board (PCB). Fig. 8.2 shows the PCB photo with the controller, high- and low-side drivers and MOSFET ICs indicated. We also included the Over-Voltage Protection (OVP) to prevent any damage to the MOSFET, and indirectly also prevent any saturation of the inductor. The SPM6530T low-DCR inductors and ceramic capacitors were used to ensure a high quality factor output LC filter.

We tested the compensation for two programmable switching frequencies f_{SW} = 0.5 and 1 MHz. For this, we scaled the LC filter almost linearly to ensure the same V_{OUT} ripple magnitude (< 0.5 % in our prototype). The low V_{OUT} ripple is ensured especially for the case when low-ESR ceramic output capacitors are employed. The ripple magnitude will be higher

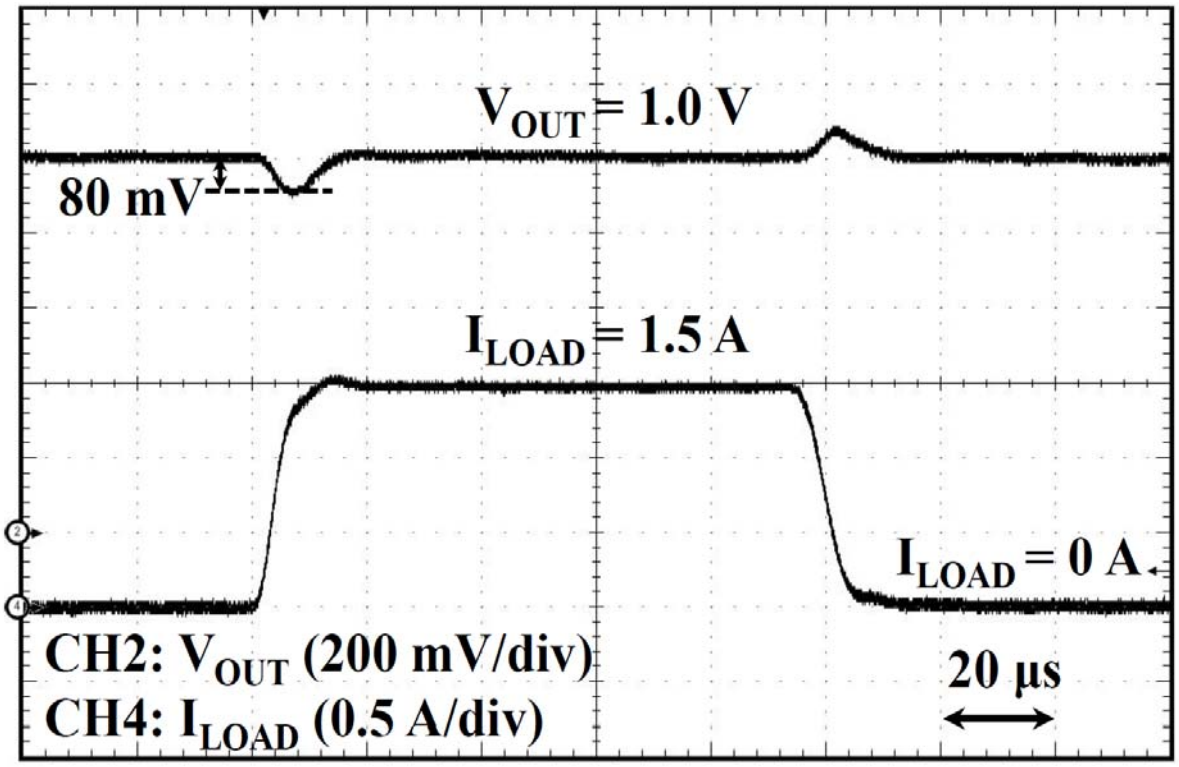


Figure 8.4: Measured waveforms showing the load step transient at f_{SW} = 1.0 MHz.

and the limits of AAF tested for the SCF when ESR values are higher. However, it must be noted that the higher ESR will also provide additional phase boost and stability is improved even further as long as the SCF response does not experience distortion. As discussed in Section 4.4, our design takes care of this even for a worst-case ripple magnitude of 5 %, yielding a truly universal Type-III compensation prototype.

Fig. 8.3 shows the measured load transient step response at f_{SW} = 0.5 MHz, V_{IN} = 3.3 V and V_{OUT} = 1.0 V from 0 – 1.5 A (and vice versa) at 0.3 A/µs. A voltage undershoot of 80 mV is observed for with a settling time of ~ 50 µs. The signal capture bandwidth for this

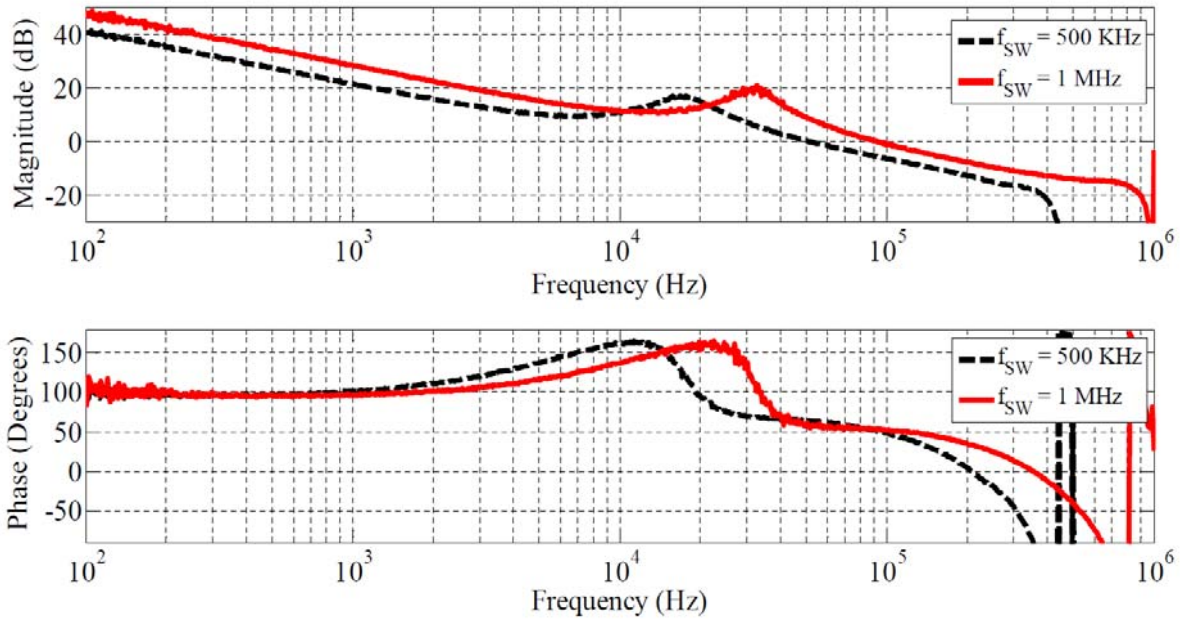


Figure 8.5: Measured loop response of the complete system at f_{SW} = 0.5 and 1.0 MHz.

measurement is 20 MHz. Fig. 8.4 shows the measured load transient step response at f_{SW} = 1.0 MHz, under exactly the same conditions described for the previous case. A voltage undershoot of 80 mV is observed for with a settling time of ~ 20 µs. The settling time of a truly linear system scales with the unity gain bandwidth of its open-loop frequency response. In Fig. 8.5, we show the open-loop frequency response of the system captured by a network analyzer (AP 200 [33]), for both cases of f_{SW}. It can be seen that the filter transfer function scales linearly with f_{SW}, and no distortion is observed, even at frequency limits close to the Nyquist bandwidth of the SCF (= f_{SW}). At higher frequencies, close to f_{SW}, we can observe slight gain peaking in the magnitude response, followed by a notch, due to the sample-and-hold effect of the fixed-frequency PWM control scheme. As can be inferred from Fig. 10, the

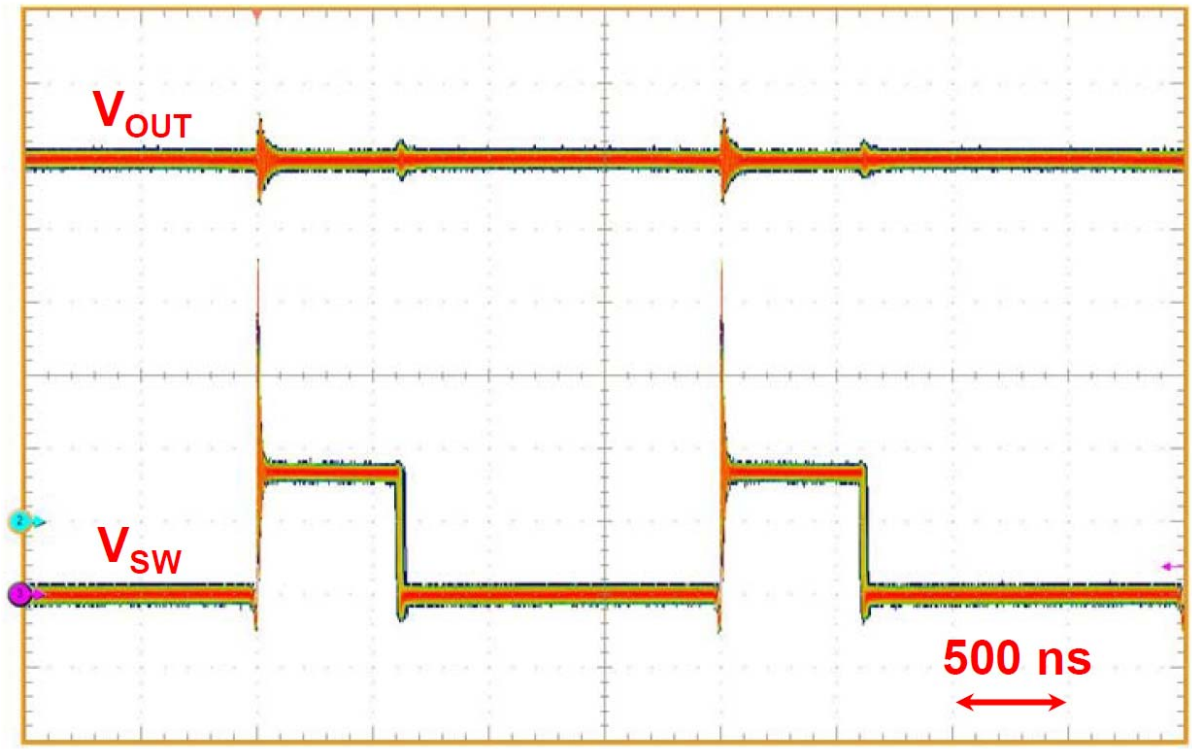


Figure 8.6: Measured waveforms showing the V_{SW} jitter performance at f_{SW} = 0.5 MHz and V_{IN}/V_{OUT} = 3.3/1.0 V.

loop is stabilized for both values of f_{SW}, with Phase-Margin (PM) = 63º, Gain Margin (GM) = 14 dB and Closed-Loop bandwidth, f_{CL} = 52 KHz when f_{SW} = 500 KHz; and PM = 55º, GM = 12 dB and f_{CL} = 95 KHz when f_{SW} = 1 MHz.

An important consideration for fixed-frequency control schemes, is the amount of jitter that the PWM pulse (and hence the switch-node) produces. This is because, due to large amount of current commutating between the high- and low-side MOSFETs, the amount of radiated EMI can be large and spread over wide frequency range if the switch-node experiences large amounts of jitter. Figs. 8.6 and 8.7 show the measured jitter performance of

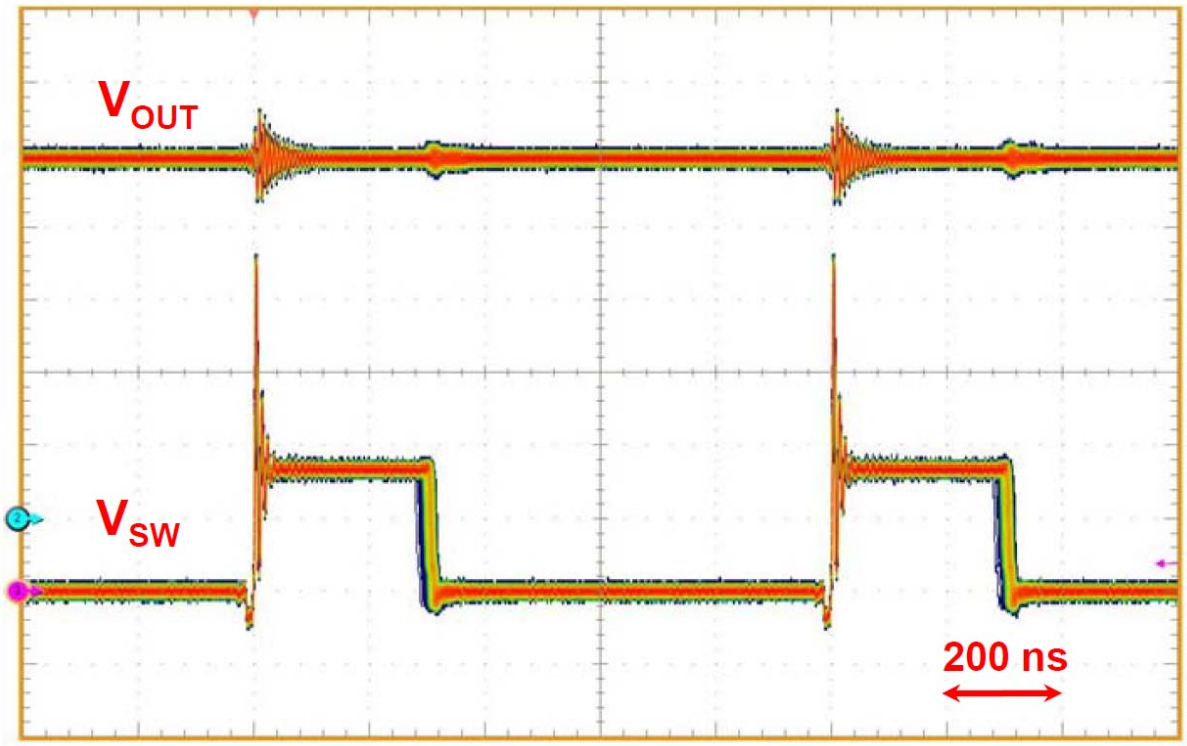


Figure 8.7: Measured waveforms showing the V_{SW} jitter performance at f_{SW} = 1.0 MHz and V_{IN}/V_{OUT} = 3.3/1.0 V.

the converter at V_{IN} = 3.3 V, V_{OUT} = 1.0 V, I_{LOAD} = 1.5 A and f_{SW} = 500 KHz and 1MHz, respectively, captured via a Tektronix DPO7104 Oscilloscope in the RTSA (Real-Time Spectrum Analyzer) mode with 200 MHz signal capture bandwidth.

The disturbance observed on the V_{OUT} signal (Figs. 8.6 and 8.7) is a high-frequency measurement artifact due to finite inductance of the measurement probe. In addition, as can be seen from the Fig. 8.6, these artifacts directly coincide with the switch node (V_{SW}) rising and falling edges. These edges indirectly correspond to the large amounts of current commutation occurring between the high- and low-side FETs, leading to high-frequency

Table 8.3: Type-III SCF controller IC specifications

Parameter	Value
Fabrication Technology	0.36 μm, 2P3M BCD process
Active Die Area (Total/Filter)	~ 0.65/0.4 mm^2
Switching Frequency (f_{SW})	0.5 and 1.0 MHz
V_{IN}	3.3 V
V_{OUT}	1.0 V
I_{LOAD}	1.5 A
Output Filter (L/C)	1.5 μH/64 μF @ f_{SW} = 0.5 MHz
	1.0 μH/30 μF @ f_{SW} = 1.0 MHz
Controller IC Supply (V_{DD})	3.3 V
Analog Core Static Current	800 μA
Filter Core Static Current	630 μA
Bias + Bandgap Static Current	300 μA
Total Static Current	1.1 mA

transients on V_{SW} and other nodes coupled to it. From Fig. 8.6, it can be inferred that while the V_{SW} rising edge has negligible jitter, the falling edge has higher jitter. The reason can be directly inferred from the proposed PWM comparator block circuitry shown in Fig. 6.4. It can be seen that the PWM rising edge directly coincides with the clock signal, while the falling edge is produced by the asynchronous comparator's decision. The jitter is directly related to the noise levels present in the comparator's environment, which include the supply switching noise, the input-referred noise of the comparator and the noise on the sawtooth waveform. Finally, the waveform jitter is direct function of the signal-to-noise ratio of the quantities being compared in the bandwidth of interest. Hence, the SCF's post-filtering, finite bandwidth of PWM comparator, and the large dynamic range of the sawtooth waveform, all

aid in PWM jitter reduction. In addition, as described in Section 6.4, the proposed PWM comparator latching scheme prevents any spurious switching inside the switching cycle, further ensuring a controlled EMI. To conclude, the performance specifications of the proposed controller IC are listed in Table 8.3.

8.3 Comparison with the state-of-the-art prototypes

In this section, we will compare the performance of the proposed Type-III controller implementation w.r.t. the state-of-the-art prototypes demonstrated in recent peer-reviewed literature. The Type-III filter implementation has been improved upon in both the all-analog and all-digital implementations. In [34] (and [35]), the Type-III filter function has been implemented in an all-analog fashion, as the sum of a Band-Pass Filter (BPF) and Low-Pass Filter (LPF). The LPF is essentially a lossy-integrator, which ensures high DC gain of the loop. The decoupling of the high-accuracy and high-bandwidth requirements of the Type-III function, eventually result in significant area and power savings. In [36], a Type-II filter is implemented on-chip by multiplication of the integrating capacitance in the time domain. This is accomplished by a pulsed scheme (with reduced duty-cycle) for the charging of the capacitor. A direct impact of this scheme would be degradation of the transient response of the controller. In [37] and [38], the Type-II filter is integrated on-chip by utilizing capacitive multiplication techniques derived from the Miller Theorem. It must be understood here that the extension of these Type-II filters to their respective Type-III counterparts is not straight-forward. Finally, since these filter constants are essentially RC based in [34] - [38], it would result in high on-chip variability and no frequency-scalability. This is fundamentally true for

all integrated ARCF implementations as discussed in Section 1.2, and this issue has not been addressed in the prior-art.

The digital PWM performance is mainly limited by the high-speed ADC front-end (fast transient response) and high-resolution DAC back-end (DC regulation accuracy), and has been a topic of active study and research in the recent years [39] – [45]. Researchers have been exploring various ADC and DAC architectures implementations in deep sub-micron technologies (typically < 90 nm), which is very attractive from faster transistor speed and higher digital density point-of-view. However, such technologies are always in the development cycle, and their fabrication is always an expensive, proposition. In addition, with the reduced supply voltages, the design of systems requiring a wide dynamic range is extremely challenging. Of these works, two are especially noteworthy. In [40], a novel ΔΣ modulation based high-speed voltage-to-frequency conversion ADC is employed to save power, followed by a Type-I DLL based DAC. The accuracy achieved is ±2 % while consuming only 0.59 mA from a 1.8 V supply for f_{SW} = 500 KHz. In [45], a SAR ADC based non-linear all-digital control loop is implemented in 65 nm CMOS technology for f_{SW} = 6.4 MHz. The result is a highly area and power efficient implementation.

Table 8.4 compares and contrasts the performance of the proposed Type-III compensation technique with the state-of-the-art works in recent publications, as considered in the foregoing discussion. Compared to the all-analog implementation in [35], it has higher programmability and variability, while consuming higher power. Compared to the all-digital implementation in [40], it consumes a similar amount of power, while ensuring a superior

Table 8.4: Performance comparison of the proposed scheme with recent published works

Performance Metric	**[35]** ***JSSC, 2010***	**[40]** ***ISSCC, 2010***	**[45]** ***JSSC, 2012***	***This Work***
Type-III Implementation	Analog	Digital	Non-Linear Digital	Sampled Analog
Main Idea	LPF + BPF	ΔΣ V-F ADC	Deep sub-μm Technology	SCF
Process Technology	0.36-μm CMOS	0.18-μm CMOS	65-nm CMOS	0.36-μm BCD
Filter Variability	High	Low	Low	Moderate
Frequency Scalability	None	High	High	Moderate
f_{LC}/f_{SW} (KHz)	34/1000	8/500	73/6400	32/1000
DC Regulation	1.8 V ± -- %	1.8 V ± 2 %	1.0 V ± 1 %	1.0 V ± 2 %
Load Step Undershoot	100 mV	130 mV	20 mV	80 mV
Load Step (I_L)	0.5 A	0.3 A	0.2 A	1.5 A
Load Step Rate (di/dt)	2.5 A/μs	-- A/μs	0.4 A/μs	0.3 A/μs
Power Consumption	30 μA	600 μA	116 μA	1100/800 μA
Active Area	0.35 mm^2	1.55 mm^2	0.038 mm^2	0.65/0.4 mm^2

DC and transient performance with a lower on-chip area. In [45], the benefits of a state-of-the-art process technology and non-linear control scheme are combined for power reduction and transient response improvement. In the future, the benefits of technology scaling can be applied to analog (and sampled-analog) techniques as well. In addition, the non-linear transient improvement techniques are already being employed in the analog domain as suggested in [46]. Its extension to the sampled-analog scheme is indeed straight-forward.

Chapter 9

9. Conclusions and Future Work

9.1 Conclusions

We have conceived a novel Switched-Capacitor Filter (SCF) based Type-III compensation for the linear PWM control of switch-mode Buck converters. We have laid the theoretical foundations necessary for the design of such a filter. In addition, we have designed a working prototype in a 0.36-μm BCD technology for a computing power supply, solving several implementation issues in the process. The filter design has been verified in both frequency- and time-domain experiments. This filter has the following two distinguishing features:

i. Fully-Integrated Design: Due to the low-variability of the time constants implemented on-chip with Process, Voltage and Temperature (PVT) variations, the filter can be made fully-integrated. This has the advantage of being significantly area and cost efficient compared to its analog counterpart. Finally, with the compensation being internal to the integrated circuit, it significantly eases up the system design for the power supply designer.

ii. Frequency-scalable Architecture: The filter time constants scale themselves based on the switching frequency selected by the power supply designer. From a design standpoint, the filter design thus needs to be done keeping in mind the highest operating frequency. To operate the SCF at higher frequencies, we would hence need to burn more power.

Table 9.1: Comparison of linear PWM control schemes (contemporary and proposed)

Performance Metric	***Analog***	***Digital***	***SCF***
Area	High[$]	Moderate	Low
Filter Variability	High[$]	Low	Low
Degrees of Freedom	Low	High	Moderate
Frequency Scalability	None	High	High
DC Regulation Accuracy	Good	Good[¥]	Good
Transient Response	Average	Average[¥]	Average
Power Consumption	Moderate	High[¥]	Moderate
Monolithic Solution	No	Yes	Yes

[$] Assuming fully-integrated RC components for the Analog Filter.
[¥] Digital Filter requires much higher power to achieve a DC and transient performance comparable to the Analog Filter.

To the best of our knowledge, such a filter prototype has never been attempted before. The closest attempt is made in [47] (and [48]), in which a switched-capacitor filter front-end is employed for the closed-loop control of a Single-Inductor-Multiple-Output (SIMO) DC-DC converter. However, the SCF only implements the analog summation front-end, one pole-zero pair, followed by a sample-and-hold. Thus, the SCF implementation is rather simplistic. In addition, the reference papers do not delve into the various anti-aliasing requirements of the SCF.

We would hereby like to qualitatively compare the performance of this filter with the analog and digital implementations presented in Section 1.2. The comparison based on various performance metrics presented in Table 1.2 has now been extended to Table 9.1, with the proposed SCF included for comparison. Again, the yellow shaded box represents the

most desirable performance amongst the three filters under consideration, for any given performance metric.

a. Compared to the analog filter, the proposed filter can be fully-integrated onto the die and has wider programmability and degrees of freedom. By exploiting the benefits of distributed analog signal processing, the proposed filter has even lower power dissipation compared to the conventional filter.
b. Compared to the digital filter, the proposed filter has much lower power dissipation, while guaranteeing a superior overall performance.

9.2 Future Work

We have observed that the proposed filter aims to combine the benefits of the analog and digital implementations, and it would indeed be desirable if the proposed filter can outperform the two in the future:

a. The proposed filter has a lower dynamic range compared to the analog filter, and needs improvement. One way to improve the dynamic range would be to employ fully-differential filter architecture. However, that would entail doubling of the area of the filter's passive components. In addition, this architecture would require Common-Mode Feed-Back (CMFB), which increases the design complexity and power consumption of the signal processing unit. An area and power efficient solution would indeed be desirable in the future.
b. The proposed filter incorporates the advantage of the digital filter in that it has added programmability and scalability for two configurable switching frequencies, while

providing a fully-integrated solution with minimal trimming requirements (of the integrator stage). However, it would be interesting and challenging to extend the degree of programmability (over wide tuning range) and scalability (for over a decade of switching frequencies) of its transfer function in the future. In addition, a completely monolithic, trimless solution would be highly desirable as well.

REFERENCES

[1] www.apple.com

[2] http://www.freescale.com/files/training_pdf/VFTF09_AC109.pdf

[3] http://www.eetimes.com/design/power-management-design/4011587

[4] "50 mA regulated step-down charge pump for 1.8 or 1.9 V logic," Feb. 2000, Maxim, data sheet of chip no. MAX1730.

[5] www.national.com/assets/en/appnotes/PowerDesigner103_portable.pdf

[6] R.W. Erickson and D. Maksimovic, "Fundamentals of Power Electronics," Kluwer Academic Publishers, 2nd Ed., 2000.

[7] "3-A Step-Down Regulator with Integrated Switcher," Mar. 2011, Texas Instruments, data sheet of chip no. TPS53311.

[8] S. Abedinpour, B. Bakkaloglu, and S. Kiaei, "A multistage Interleaved Synchronous Buck Converter With Integrated Output Filter in 0.18 um SiGe Process," *IEEE Trans. On Power Electronics,* vol. 22, no. 6, pp. 2164-2175, Nov. 2007.

[9] M. Alimadadi *et al.*, "A 3GHz Switching DC-DC Converter Using Clock-Tree Charge-Recycling in 90nm CMOS with Integrated Output Filter," *IEEE Intl. Solid-State Cir. Conf.,* pp. 532-620, Feb. 2007.

[10] P. Hazucha *et al.*, "A 233-MHz 80%-87% Efficient Four-Phase DC–DC Converter Utilizing Air-Core Inductors on Package," *IEEE J. Solid State Cir.,* vol. 40, no. 4, pp. 838-845, Apr. 2005.

[11] J. Wibben and R. Harjani, "A High-Efficiency DC–DC Converter Using 2 nH Integrated Inductors," *IEEE J. Solid State Cir.,* vol. 43, no. 4, pp. 844-854, Apr. 2008.

[12] S.S. Kudva and R. Harjani, "Fully-Integrated On-Chip DC-DC Converter with a 450X Output Range," *IEEE J. Solid State Cir.,* vol. 46, no. 8, pp. 1940-1951, Apr. 2011.

[13] R. Redl and J. Sun, "Ripple-based control of switching regulators – An Overview," *IEEE Trans. On Power Electronics,* vol. 24, no. 12, pp. 2669-2680, Dec. 2009.

[14] C. Song, "Accuracy analysis of constant-on current-mode dc-dc converter for powering microprocessors," *IEEE Proc. Applied Power Electronics Conf.*, pp. 97-101, Feb. 2009.

[15] "Digital PWM System Controller with 4-bit, 6-bit, or 8-bit VID Support," Feb. 2011, Texas Instruments, data sheet of chip no. UCD9244.

[16] R. Gregorian and G. Temes, "Analog MOS integrated circuits for signal processing," *Wiley*, 1986.

[17] U. Moon, "CMOS High-Frequency Switched-Capacitor Filters for Telecommunication Applications," *IEEE J. Solid State Cir.,* vol. 35, no. 2, pp. 212-220, Feb. 2000.

[18] D. Johns and K. Martin, "Analog Integrated Circuit Design," *Wiley*, 1997.

[19] C.A. Desoer and E.S. Kuh, "Basic Circuit Theory," *McGraw-Hill*, 1969.

[20] http://www.mathworks.com/help/toolbox/control/ref/sisotool.html

[21] K. Martin and A.S. Sedra, "Effects of the Op Amp Finite Gain and Bandwidth on the Performance of Switched-Capacitor Filters," *IEEE Trans. On Cir. and Sys.,* vol. 28, no. 8, pp. 822-829, Aug. 1981.

[22] G. Temes, H.J. Orchard and M. Jahanbegloo, "Switched-Capacitor filter design using the Bilinear z- transform", *IEEE Trans. On Cir. and Sys.*, vol. 25, no. 12, pp. 1039-1044, Dec. 1978.

[23] R. Gregorian and W.E. Nicholson, "A Switched-capacitor high-pass filter," *IEEE Trans. On Cir. and Sys.*, vol. 27, no. 3, pp. 226-229, Mar. 1980.

[24] http://www.designers-guide.org/Analysis/sc-filters.pdf

[25] http://www.cisl.columbia.edu/projects/switcap

[26] B. Razavi, "Design of analog CMOS integrated circuits," *McGraw-Hill*, 2000.

[27] A.S. Sedra and K.C. Smith, "Microelectronic Circuits," 5th ed., *Oxford University Press*, 2007.

[28] B. Gilbert, "The Multi-tanh principle: A tutorial overview," *IEEE J. Solid State Cir.,* vol. 33, no. 1, pp. 2-17, Jan. 1998.

[29] R.R. Torrance, T.R. Viswanathan and J.V. Hanson, "CMOS voltage to current transducers," *IEEE Trans. On Cir. and Sys.*, vol. 32, no. 11, pp. 1097-1104, Nov. 1985.

[30] R. Hogervorst, *et al.*, "A compact power efficient 3 V CMOS rail-to-rail input/output operational amplifier for VLSI cell libraries," *IEEE J. Solid State Cir.,* vol. 29, no. 12, pp. 1505-1513, Dec. 1994.

[31] W.M.C. Sansen and P.M.V. Peteghem, "An Area-Efficient Approach to the Design of Very-Large Time Constants in Switched Capacitor Integrators," *IEEE J. Solid State Cir.,* vol. 19, no. 5, pp. 772-780, Dec. 1984.

[32] J.J.F. Rijns and H. Wallinga, "Spectral analysis of double-sampling switched capacitor filters," *IEEE Trans. On Cir. and Sys.*, vol. 38, no. 11, pp. 1269-1279, Nov. 1991.

[33] http://www.apinstruments.com

[34] Y. Wu, S.Y.S. Tsui and P.K.T. Mok, "An area- and power-efficient monlithic buck converter with fast transient response," *IEEE Custom Integ. Cir. Conf.*, pp. 307-310, Sep. 2009.

[35] Y. Wu, S.Y.S. Tsui and P.K.T. Mok, "Area- and power-efficient monlithic buck converter with pseudo Type-III compensation," *IEEE J. Solid St. Cir.*, vol. 45, no. 8, pp. 1446-1455, Aug. 2010.

[36] S. Hong, *et al.*, "High area-efficient DC-DC converter using time-mode miller compensation (TMMC)," *IEEE Symp. On VLSI Circuits*, pp. 180-181, Jun. 2012.

[37] K. Chen, H. Huang and S. Kuo, "Fast transient DC-DC converter with on-chip compensated error amplifier," *IEEE Trans. On Cir. and Sys.-II*, vol. 54, no. 12, pp. 1150-1154, Dec. 2007.

[38] K. Chen, C. Chuang and T. Liu, "Bidirectional current-mode capacitor multipliers for on-chip compensation," *IEEE Trans. On Power Electronics*, vol. 23, no. 1, pp. 180-188, Jan. 2008.

[39] B.J. Patella, *et al.*, "High-frequency digital PWM controller IC for DC-DC converters," *IEEE Trans. On Power Electronics*, vol. 18, no. 1, pp. 438-446, Jan. 2003.

[40] H.H. Ahmad and B. Bakkaloglu, "A 300 mA 14 mV-ripple digitally controlled buck converter using frequency domain ADC and hybrid PWM generator," *IEEE Intl. Solid-State Cir. Conf.,* pp. 202-204, Feb. 2010.

[41] E.G. Soenen, *et al.*, "A robust digital DC-DC converter with rail-to-rail output range in 40 nm CMOS," *IEEE Intl. Solid-State Cir. Conf.,* pp. 198-200, Feb. 2010.

[42] S. Bandhopadhyay, Y.K. Ramadass and A.P. Chandrakasan, "20 μA to 100 mA DC-DC Converter with 2.8 to 4.2 V battery supply for portable applications in 45 nm CMOS," *IEEE Intl. Solid-State Cir. Conf.,* pp. 386-387, Feb. 2011.

[43] J. Shi, *et al.*, "Practical considerations for a digital inductive switching DC-DC converter with direct battery connect in deep sub-micron CMOS," *IEEE J. Solid State Cir.,* vol. 47, no. 8, pp. 1946-1959, Aug. 2012.

[44] Q. Chen, *et al.*, "Monolithic digitally controlled buck converter with TDC-based ADC sharing delay cells with DPWM," *IEEE Electronics Letters*, vol. 48, no. 20, pp. 1303-1304, Sep. 2012.

[45] S. Cliquennois, *et al.*, "A 65-nm, 1-A Buck Converter with multi-function SAR-ADC based CCM/PSK digital control loop," *IEEE J. Solid State Cir.,* vol. 47, no. 7, pp. 1546-1556, Jul. 2012.

[46] P. Liu *et al.*, "A high-efficiency CMOS DC-DC converter with 9-μs transient recovery time," *IEEE Trans. On Cir. and Sys.-I*, vol. 59, no. 3, pp. 575-583, Mar. 2012.

[47] M. Belloni, *et al.*, "A 4-output single-inductor DC-DC buck converter with self-boosted switch drivers and 1.2 A total current," *IEEE Intl. Solid-State Cir. Conf.,* pp. 444-446, Feb. 2008.

[48] M. Belloni, *et al.*, "A high efficiency 4-output single inductor DC-DC buck converter with self-boosted snubber," *Springer Analog Integ. Cir. and Signal Processing,* pp. 169-177, Jan. 2011.