ABSTRACT

SHE, XU. Control and Design of a High Voltage Solid State Transformer and its Integration with Renewable Energy Resources and Microgrid System. (Under the direction of Dr. Alex Q. Huang).

Solid State Transformer (SST) has been regarded as one of the most emerging technologies in the power distribution system. It has the advantages of low volume, low weight, fault isolation, and potential additional functions, such as voltage regulation, harmonic filtering, reactive power compensation, and etc. However, the involvement of large number of power devices makes the control of SST a challenge. In addition, the high voltage and high power hardware design of the SST is not easy, certain design methodology needs to be developed. Furthermore, the cost of the SST is much higher than the traditional transformer, how to justify this cost gap is also of great importance.

In this dissertation, a systematic literature review is conducted for the development of SST in the future distribution system. The key components essential for the SST are reviewed and different techniques are compared. It is pointed out that the SST consists of multilevel/modular power converter structure with advanced power devices and magnetic materials achieves best performance in terms of the size and efficiency in high voltage operation condition. While the challenges, including control architecture and design methodology, need to be addressed. In addition, the potential markets for SST need to be identified for possible commercialization of the technology.

In this research work, a three-stage modularized type SST based on Si IGBT is selected as the research target aiming at developing advanced control technologies, design methodology, and application areas of the SST.

The first part of the dissertation focuses on the analysis, control, and design of the presented three-stage SST topology. First of all, the voltage and current sharing issues of the presented SST topology are analyzed and addressed. Firstly, a new control structure and design methodology is proposed for balancing the voltage of the rectifier stage by using the feedback regulation. This controller minimizes the coupling effect between the voltage balance controller and the original system controller. Therefore, the design of the original system controller can be as easy as the two-level converter system, and the two controllers will not interact with each other. Secondly, the modulation based voltage balance method is also explored with extremely fast voltage balance response. The design of the control system can also be regarded as a two-level converter system and the voltage balance is achieved by choosing the most suitable switching pairs of the H-bridges. Thirdly, a current sensor-less current balance controller is proposed for the parallel operated DC/DC stage. This method does not need any additional current sensors and can achieve the power sharing among converters of DC/DC stage well. Fourthly, a 3.6kV-120V/10kVA SST hardware prototype is designed and demonstrated for the smart grid application. The proposed control methods in chapter 3 and chapter 5 are adopted in this high voltage SST prototype. Various tests are conducted to verify the key characters of the presented SST topology compared with the traditional transformer.

The second part of the dissertation focuses the on the advanced application of presented SST in the future renewable energy and microgrid systems. Firstly, a family of SST interfaced wind energy systems are proposed with the integrated functions of active power transfer, reactive power compensation, and voltage conversion. The proposed wind energy system can effectively replace the traditional transformers and reactive power compensation devices, therefore a highly compact and integrated system can be obtained and the cost of the SST can be better justified. Secondly, a SST interfaced microgrid system and its centralized power management strategy are proposed. The presented microgrid system can access the distribution system without bulky transformers and can manage both the AC and DC grid simultaneously, operating like an AC/DC hybrid microgrid. In this condition, SST plays as an energy router, benefiting the future residential systems.

All the technologies proposed in this work are original and provide value information for further promotion and commercialization of the SST concept.

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Control and Design of a High voltage Solid State Transformer and its Integration with Renewable Energy Resources and Microgrid System

by
Xu She

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APPROVED BY:

Dr. Alex Q.Huang Committee Chair	Dr. Iqbal Husain
Dr. Srdjan Lukic	Dr. David Lubkeman

DEDICATION

To my parents, my parents in law, and Huan Hu

BIOGRAPHY

Xu She was born in Hunan, China. He received the B.S. degree in electrical engineering (major) and B.A. degree in English (minor), with honor from Huazhong University of Science and Technology, China, in 2007. He received his M.S. degree majored in power electronics and motor drive with honor from the same university in 2009. He started to pursue his Ph.D. degree in North Carolina State University in 2009.

From August 2009 to July 2010, he has been working on the modeling of the green energy hub and DC microgrid project. Since August 2010, he has been working on the solid state transformer project. He was the team leader of Solid State Transformer (SST) group and Medium Voltage DC (MVDC) transmission group at Future Renewable Electric Energy Delivery and Management (FREEDM) Systems Center. From May to August 2012, he was an intern with high power conversion systems laboratory at GE global research center, US, conducting research on next generation high voltage dc transmission (HVDC) system.

His research interests are high power/voltage converters and their industrial applications, and renewable energy resources integration.

His role in the first job will be a research engineer (lead professional career band) in high power conversion systems laboratory at GE global research center.

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Chapter 1 Introduction

1.1 The distribution transformer

1.1.1 Introduction of the distribution transformer

Power generation, transmission, and distribution are the three main constituents of the modern power system, in which the transformer plays a most critical role [1]. Transformers enable high efficiency and long distance power transmission by boosting the voltage to a higher one in the generation side with the so called power transformer. In the distribution system side, this high voltage is stepped down for industrial, commercial, and residential use with the so called distribution transformer.

The distribution transformer provides final voltage transformation to the end users in the distribution system, which usually with voltage level less than 34.5kV at high voltage side. At the low voltage side, 120/240V split single phase system and 480V three phase systems are usually adopted in the US.

The distribution transformer can be classified from different perspective of view. According to the phase number, it can be classified into three phase transformer and single phase transformer. According to the installation method, it can be classified into pole mounted transformer and pad mounted transformer. The pad mounted transformers are installed for the distribution system with lines located at ground level or underground. While the pole

mounted transformers are mounted on a utility pole. According to the insulation medium, it can be classified into liquid-immersed transformer and dry type transformer.

The distribution transformers are widely used in various applications, such as renewable energy resources integration, high power charge station, traction system, reactive power compensator, active power filter, and etc., as shown in Figure 1-1[2][3]. It functions as a passive interface between the distribution system and the low voltage loads/sources. Therefore, the voltage quality of the grid cannot be guaranteed if no additionally devices are installed.

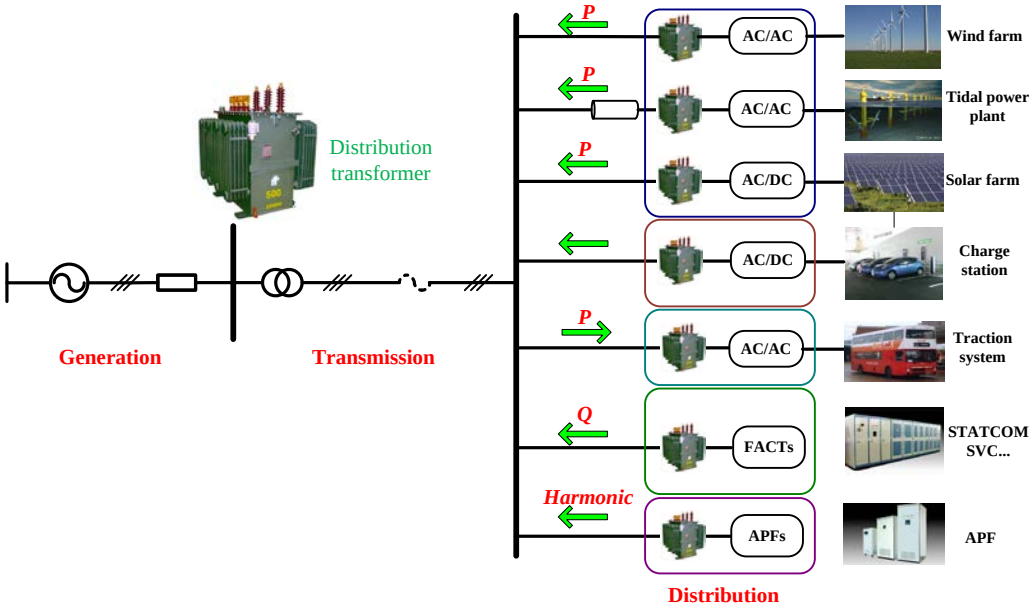
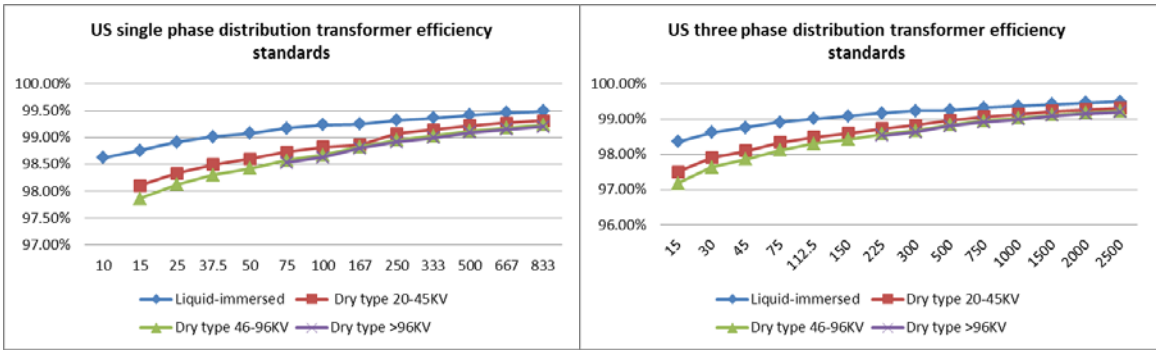


Figure 1-1 Application of distribution transformer in modern power grid

1.1.2 Characteristics of the distribution transformer

The US department of energy (DOE) released a standard for liquid and dry type distribution transformers in October 2007, effective since January 2010[4]. This regulation covers all distribution transformers manufactured after January 2010, and defines the minimum efficiency standards as shown in Figure 1-2 for both single-phase and three-phase transformers. It is seen that the overall efficiency of the distribution transformer required by the standard is higher than 97 % irrespective of power rating, and this value approaches 99.5 % for most liquid-immersed power transformers. In addition, the standard calls for a higher requirement for the liquid-immersed type transformer since it can transfer heat more effectively, thus the core temperature does not rise as much, which would decrease efficiency. Therefore, the first characteristic of the conventional distribution transformer is high efficiency.



(a) (b)

Figure 1-2 Distribution transformer national efficiency standards of US: (a) Single phase transformer (x-axis: power (kVA); y-axis: Efficiency; BIL: Basic Insulation Level); (b) Three phase transformer (x-axis: power (kVA);

Table 1-1 lists the typical dimensions and weights of the GE-PROLEC three-phase pad mount distribution transformer [5]. As seen, due to the large amount of copper and iron used, traditional transformers are bulky, requiring space and incurring in high costs for transportation. Hence, the second characteristic of the conventional distribution transformer is heavy weight and low power density. Decreasing the volume and weight can bring economic advantages to both manufactures and customers.

Table 1-1 Typical dimensions of GE-PROLEC three-phase pad mount transformers

kVA	*Front Height (in.)*	*Front Width (in.)*	*Total Depth (in.)*	*Rear Width (in.)*	*Rear Height (in.)*	*Typical Weight (lbs.)*
75	63	72	53	71	52	2965
112.5	63	72	53	71	52	3050
150	63	72	53	71	52	3250
225	65	72	55	71	54	3350
300	65	72	55	71	54	3800
500	69	72	55	71	54	4500
750	77	72	74	71	58	6200
1000	77	75	75	71	59	9400
1500	77	76	76	77	67	12200
2000	87	78	79	71	69	13200
2500	87	78	79	71	69	13800

The standard costs for three-phase pad mount distribution transformers range from $40/kVA to $100/kVA for size ranging from 50 to 150kVA[6]. Table 1-2 shows the typical cost data for a three phase pad mount transformer. As can be seen, the cost of the conventional distribution transformer is very low compared with the power electronics devices. Therefore, the third characteristic of the conventional distribution transformer is the low cost.

Table 1-2 Typical cost data of three phase, pad mount transformer

Size (kVA)	12.5kV	34.5kV
75	7749	10584
150	9450	11605
300	11718	15574
500	13608	20034
750	21257	21377
1000	25515	28350

Additionally as aforementioned, the conventional transformer is a passive interface between high voltage and low voltage system. Therefore, the disturbances, such as voltage sag/swell and harmonics at one side of the transformer will easily affect the other. From this perspective of view, the fourth characteristic of the conventional transformer is the poor voltage regulation and harmonic isolation capability.

The development trends of the traditional power transformers are mainly focused on new magnetic materials, insulation materials, manufacturing processes, and other economic

factors. Nevertheless, new technologies need to be developed to considering the increasing demand of the power quality and rapid development of the smart grid technologies.

1.2 The solid state transformer concept

Recently, together with other technological advancements, power electronics is being seriously considered as one of the advantageous technologies that could empower future smart grids, doing so at all levels of electrical power systems. Power electronics is one of the key enabling technologies in electrical engineering nowadays. This is not entirely new, as high power converters played an increasing role in both distribution and transmission power systems over the past decades, for instance, in high voltage direct current (HVDC) transmission systems and flexible ac transmission system (FACTs) devices, such as static Var compensator (SVC), static synchronous compensator (STATCOM), unified power flow controller (UPFC), and others [7]. Another portion of high power converters have found increasing number of applications in renewable energy systems, especially in the case of large penetration of renewable resources, such as solar and wind[8], [9].

In the recent decade, another high power converter, named solid state transformer (SST) (also known as power electronic transformer or intelligent universal transformer), has caught much attention and has been extensively investigated for distribution systems [10], [11], [12], [13], [14], [15], [16]. The earliest concept of SST was introduced in [17], where it was dubbed “electronic transformer”. Over the past few years, several efforts have been made to deliver a low voltage SST prototype[18], [19], [20], [21]. However, SSTs at the present time

are limited by power devices and circuit topologies, specifically in terms of their voltage rating and efficiency, and as such have not penetrated into distribution systems.

The SST is a power electronic device that replaces the traditional 50/60 Hz power transformer by means of high frequency transformer isolated AC-AC conversion technique, which is represented in Figure 1-3. The basic operation of the SST is firstly to change the 50/60 Hz AC voltage to a high frequency one (normally in the range of several to tens of kilohertz), then this high frequency voltage is stepped up/down by a high frequency transformer with significantly decreased volume and weight, and finally shaped back into the desired 50/60 Hz voltage to feed the load. In this sense, the first advantage that the SST may offer is its reduced volume and weight compared with traditional transformers.

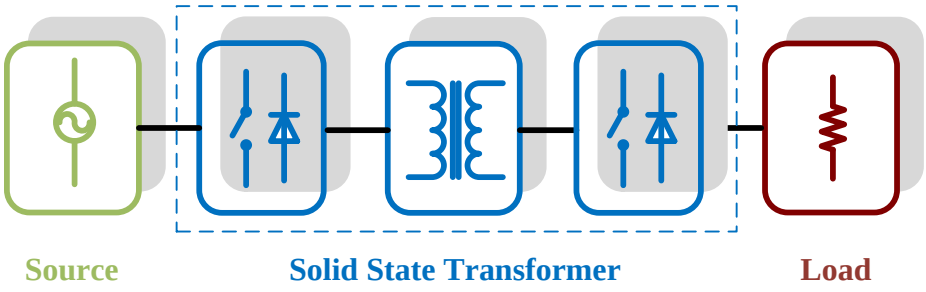


Figure 1-3 Configuration of Solid State Transformer

It is further seen from the configuration of the SST that some other potential functionalities that are not owned by the traditional transformer may be obtained. First, the use of solid state semiconductor devices and circuits makes the voltage and current regulation a possibility; similarly to FACTS devices. This brings promising advantages such as power flow control,

voltage sag compensation, fault current limitation, and others, which are not possible for traditional transformers. Second, voltage source converters connected from the secondary terminal of the SST could readily support a regulated DC bus, which could be connected to DC microgrids enabling this new microgrid architecture.

Although the concept of SST is straight forward, its implementation is a challenge. The SST is essentially a high power and high voltage power electronic circuit, of which the operation is always a challenge from both hardware and control point of view. In addition, SST contains many other components besides the high frequency transformer, such as power devices, gate drivers, heat-sinks, control circuits, cooling system, auxiliary power, and other ancillary circuitry. As such, the sought lower volume and weight reduction may not be guaranteed without a careful design. In fact, the effectively decrease of the volume and weight of the SST can be easier to achieve when the power rating is higher, in which condition the transformer dominants the volume and the weight of the system. Furthermore, in order to find more market drivers for the SST commercialization, new application areas of the SST needs to be identified. Therefore, it is highly demand to look deeper into the SST technologies and find better solutions.

1.3 Dissertation outline

This dissertation focuses on proposing new control solutions, design methodology and application areas for a modular, cascaded multilevel, three-stage SST topology. The organization of the dissertation is shown in Figure 1-4 , in which three technical parts are covered, including the control system design, hardware design, and application of SST.

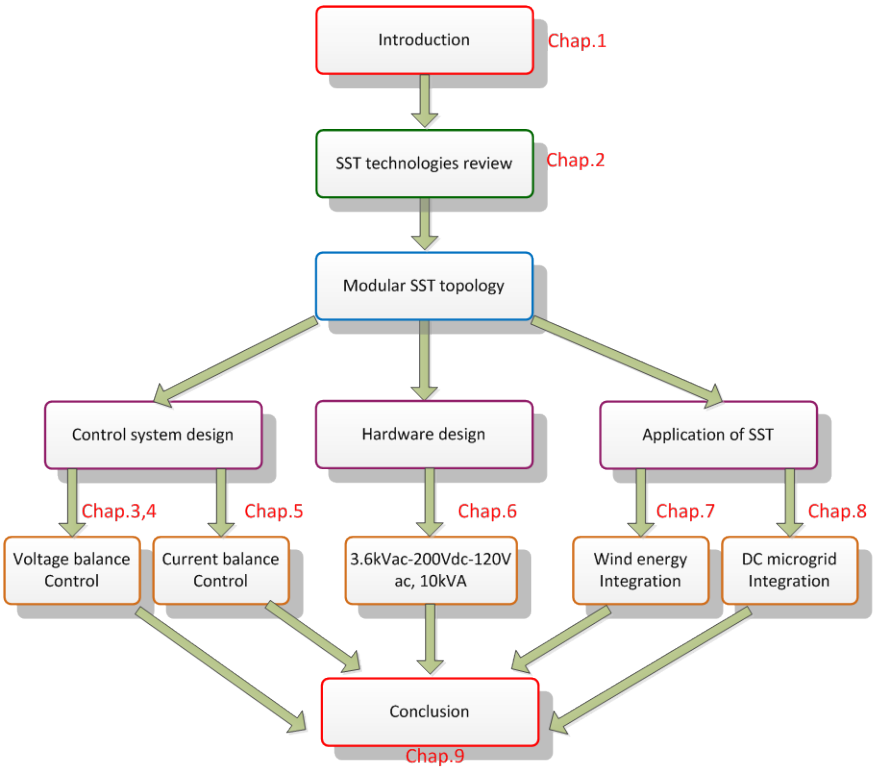


Figure 1-4 Organization of the dissertation

Specifically, the dissertation can be divided into nine chapters:

Chapter 1 provides the background and motivation of the proposed work.

Chapter 2 comprehensively reviews the key technologies essential for the development and commercialization of the SST, including the power device, high frequency transformer, circuit topology, and application areas. In each category, the technology challenges are pointed out and recommendations for the future works are provided. A cascaded multilevel three stage SST topology is picked as the research target and the control challenges are presented. The picked topology, together with advanced power device and high frequency

transformer technology, can fulfill the demand of the high voltage and high power operation of the modern power distribution system.

Chapter 3 proposes the voltage balance technique for the cascaded multilevel rectifier stage by using the feedback control method, aiming at minimizing the coupling between the system controller and voltage balance controller.

Chapter 4 proposes another voltage balance technique for the cascaded multilevel rectifier stage by using the modulation strategy, which enables the ultra-fast voltage balance capability.

Chapter 5 proposes the current balance technique for the parallel operated DC/DC stage. A novel current sensor-less current balance strategy is proposed. The proposed method can achieve the current balance controller without any current sensor in the DC/DC stage, therefore is deemed to be cost effective.

Chapter 6 presents the hardware development of a 3.6kV-120V/10kVA SST prototype for smart grid application. The presented design methodology is verified by experimental results, providing useful experiences for the SST design.

Chapter 7 investigates the integration issues of the SST with renewable energy resources. A family of SST interfaced wind energy systems with integrated functions of active power transfer, reactive power compensation, and voltage conversion are proposed. The proposed wind energy systems make fully utilization of the functions of the presented SST topology. Therefore, the cost issues of the SST can be better justified.

Chapter 8 presents the integration issue of the SST with microgrid system. Specifically, a SST interfaced zonal microgrid system and its centralized power management strategy is

proposed. The proposed microgrid system enables the power management among distribution system, dc microgrid and ac microgrid, providing new solution for the future residential system.

Chapter 9 concludes the major contributions of the dissertation and proposes the future work.

Chapter 2 Solid State Transformer Technologies and its Application in Power Distribution System: Review and Scope of the Work

Different from the conventional power electronic circuit, the SST combines the high voltage, high power, and high frequency operation, which make the design and operation of it a real challenge. As previously shown in Figure 1-3, the SST consists of power electronic circuit and the high frequency transformer. From the circuit point of view, different power devices can be combined with different circuit topologies for this application. In addition, different core materials and transformer structures may be considered to build the high frequency transformer. Furthermore, the SST can be applied in different areas, which are the main market drivers for it. This chapter provides a critical review to the key technologies essential for the development of the SST and correspondingly proposes the recommendation for the future works[2]. Since the control of the SST depends on the topologies, therefore it is not covered in this review. Lastly, a cascaded multilevel converter based three stage solid state transformer topology is picked as the research target, and the correspondingly research focuses of this dissertation is presented [3][22].

2.1 High voltage power devices

2.1.1 State-of-art technology

The existing SSTs are mainly targeted at the distribution voltage level, which ranges from 2.3 kV to 35 kV. In order to realize an efficient, highly compact, and reliable SST in the distribution system, high voltage and high frequency operated power devices are necessary. A recommended switch voltage rating based upon the practical guidelines for various distribution voltages in both two-level and three-level based topologies is shown in Table 2-1, where the actual values may be different according to the design considerations [23].

Table 2-1 Preferred blocking voltage of power devices in the distribution system

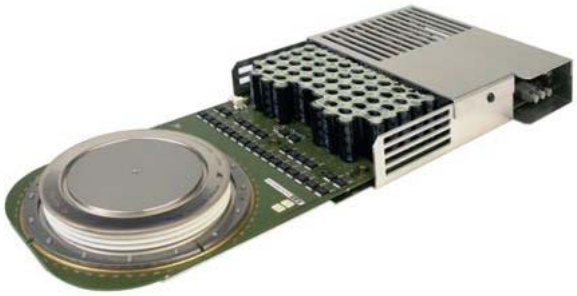
RMS line voltage (AC)	*Switch voltage rating (V)*	
	2 level	**3 level**
2400	6244	3122
4160V	10823	5412
7200V	18733	9367
12000V	31221	15611
12470V	32444	16222
13200V	34343	17172
13800V	35904	17952
14400V	36465	18233
22900V	59580	27290
34500V	89761	44881

Clearly, the switch voltage rating is quite high when it is applied in the distribution system with simple two-level or three-level converters, and this poses a big challenge to the development of SST. One possible solution is to adopt modular structures (series connection of converters) or multilevel converters with low voltage and high speed power device [24]. The downside of this approach is that from a size reduction point of view, too many discrete components increase the size and weight of the system. This is naturally not acceptable for applications where these parameters are of importance. Alternatively, high voltage power devices are under consideration, which can still be combined with the use of modular topologies for very high voltage levels.

Figure 2-1 shows the high voltage insulated gate bipolar transistors (IGBT), integrated gate commutated thyristors (IGCT), and emitter turn-off thyristors (ETO), which are suitable for high voltage application. These devices can be used in some very high power applications. However, they cannot operate at high switching frequency due to switching loss limitations, and thus the practical switching frequency is generally lower than 1 kHz [25], [26]. This is not feasible for the SST since the low switching frequency may not guarantee the effective reduction of volume and weight in the transformer.

Series connection of low voltage power devices may therefore be one of the solutions for high voltage operation. The penalty of this method is the large loop inductance intrinsic to this configuration, which once again prevents the modules from operating in high frequencies due to the additional induced voltage, which may damage the devices themselves as well as other SST components.

(a) Powerex 6.5KV, 600A IGBT



(b) ABB 4.5kV, 3.6kA asymmetric IGCT

(c) 4.5kV/4kA self-powered ETO

Figure 2-1 High voltage power semiconductor devices

Integrated module packages of series connected power devices could be the solution to the standard series connection discussed above [27], achieving minimum loop inductance and enabling high frequency operation. Nonetheless, the increased conduction voltage drop of the

resultant power module decreases the system efficiency, making it very hard to achieve efficiency levels comparable to traditional 50/60 Hz transformers.

Wide band-gap materials, such as 4H-silicon carbide (4H-SiC) have been adopted for the next generation post-silicon devices in high voltage applications. Table 2-2 lists the characteristics comparison between 4H-SiC and Si (EBG: energy band gap; BEF: breakdown electric field; TC: thermal conductivity; SEDV: Saturated electron-drift velocity). It can be seen that SiC material has a larger energy band gap which makes it capable of operating at a higher temperature. In addition, the 10 times larger breakdown electric field enables the SiC devices to switch at higher voltage, higher current, and higher frequency condition. Both of these two characteristics suit well SST applications.

Table 2-2 Comparison of material characteristics of 4H-SiC and Si

material	*EBG (eV)*	*BEF(V/cm)*	*TC (W/m.K)*	*SEDV(cm.sec)*
4H-SiC	3.26	2.2 (10^6)	380	2.0(10^7)
Si	1.12	2.5 (10^5)	150	1(10^7)

A systematic investigation has been done on high voltage SiC devices in smart grid application [28]. 10-15 kV SiC MOSFET and IGBT (both P and N channel) have been designed and evaluated, indicating that 10 kV SiC MOSFETs are the best choice for high frequency applications above 2 kHz at room temperature, while IGBTs can handle higher current than MOSFET at low frequency. Considering the low volume and small size

requirement of SST, the SiC MOSFET is preferred when the voltage is lower than 10-15 kV due to its majority carrier conduction mechanism [28], [29], [30].

A 15 kV/10 A SiC MOSFET has been recently designed and fabricated by Cree Inc. The loss data of the device was measured by using double-pulse test characterization. In addition, a customized 6.5KV/25A Si IGBT was also tested in [14]. As a comparison, Table 2-3 presents the turn-on and turn-off loss of the 15 kV/10A SiC MOSFET and 6.5kV/25A customized Si IGBT. It is shown that the SiC MOSFET can substantially reduce switching loss, especially the turn off loss, thus can potentially boost efficiency. In addition, the weight and size of SiC power device can also be reduced greatly, as shown in Figure 2-2.

Table 2-3 Switching loss comparison of devices

Test condition	***3.8kV,10A,25^{0}C***	***6kV,10A,25^{0}C***
Power device	6.5kV Si IGBT	15kV SiC MOSFET
Turn on loss	64.4mJ	14.46mJ
Turn off loss	32.7mJ	1.88mJ

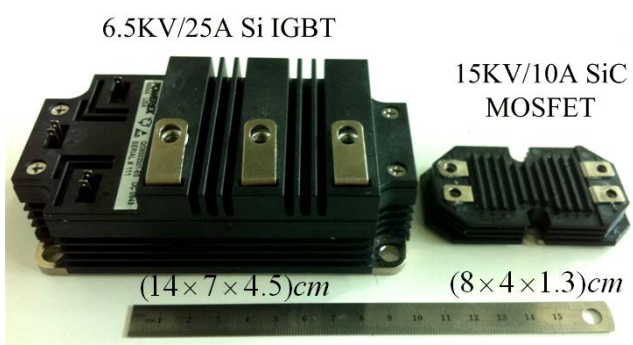


Figure 2-2 Size comparison between Si IGBT and SiC MOSFET

In the applications where the high power is required, parallel operation of SiC MOSFET is feasible due to its positive temperature coefficients for on-resistance. Figure 2-3 shows the 10kV/120A SiC half bridge module, which is adopted in a 1MVA solid state transformer design [16].

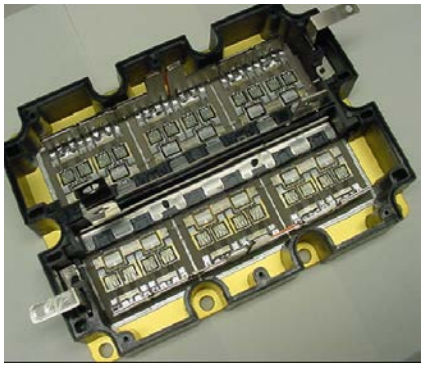


Figure 2-3 10kV/120A SiC half bridge module using twelve 10kV/10A SiC DMOSFET and six 10kV/ 10A SiC JBS Diode [16]

Nevertheless, the on-resistance of SiC MOSFETs increases significantly as their blocking voltage and operation junction temperature increase, making it unsuitable for applications where the desired blocking voltage is higher than 10-15 kV [28]. In this condition, bipolar devices such as SiC IGBTs play an important role due to their low conduction loss, moderate switching time, superior high temperature operation, and excellent safety operation area (SOA)—thus efficiency would not be compromised. The high resistance of p+ substrate caused by incomplete ionization and low hole mobility in the n-channel SiC IGBT has been a challenge, and efforts are mainly now on the P-channel SiC IGBT [31], [32], [33]. For high frequency applications such as for SST, N-channel SiC IGBT performs better due to its faster

switching speed, a result of the low current gain of the PNP transistor[34], [35]. 15 kV SiC IGBT is being developed for a 100 kVA transformer-less intelligent power substation (TIPS), in which the 20 kHz operation frequency will further decrease the volume of the system with an expected efficiency of 98.4 % [36].

Finally, if the required current handling capability is larger (>1000A, >20kV), SiC GTOs and thyristors with high switching frequency (10 kHz hard-switched and 100 kHz soft-switched) will be most suitable [37].

Figure 2-4 gives the prediction of the ultimate current and voltage rating for future SiC power devices [29]. It is concluded that SiC MOSFET will play an important role in the application with voltage less than 15kV, whereas IGBT dominate the range from 15-20kV. With operating voltage higher than 20kV, SiC GTO/Thyristor is the preferred choice.

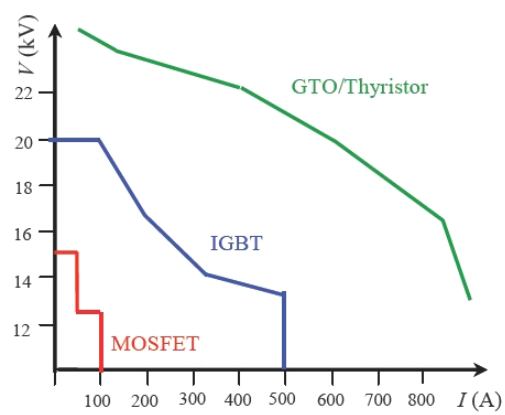


Figure 2-4 Ultimate current and voltage ratings for future SiC power devices [24]

2.1.2 Recommendation for future work

Advanced packages of series connected devices of commercial semiconductor chips is a cost-effective solution considering the availability of SiC power devices. Wide band gap power devices capable of high voltage and high frequency switching still need further development. Although high voltage wide band gap devices have been reported, they are far away from the optimized one and also cost significantly more than their silicon counterparts. The issues of how to terminate the edge to support high breakdown voltage and how to reduce the doping of drift layer have to be addressed [37]. In addition, in order to push the power rating of SST to several MW and higher, high current devices and proper device packages will also be needed. Furthermore, eliminating the use of oil means potential higher operating temperatures, implying that high temperature power devices should also be evaluated.

2.2 High voltage and high frequency transformers

2.2.1 State-of-art technology

The high frequency transformer is the main component in the SST, which replaces the traditional 50/60 Hz transformer. In order to fulfill the high voltage, high power, and high frequency operation requirements, many issues and challenges need to be addressed. First of all, the selection of the magnetic material is critical to achieve high power density and low loss in the transformer. In addition, its structure and winding configuration affect the efficiency at high frequency, thus should be carefully investigated in order to satisfy

efficiency requirements. Furthermore, advanced thermal design is a challenge in order to avoid the breakdown of the system for such a high voltage and high power system. Lastly, the high voltage operation of SST makes the insulation requirement extremely strict, especially when oil is eliminated and a compact design is required.

Several magnetic materials can be considered for high power applications, such as silicon steel, ferrite, amorphous, and nanocrystalline[38], [39]. Table 2-4 shows the comparison of different magnetic materials. Generally speaking, the silicon steel cores have high saturation flux density and also high permeability. However, the loss of this material under high frequency operation is high. Advanced silicon steel material can reduce the losses at high frequency to a relatively low value, while the saturation flux density is also reduced. Although the core loss of the ferrite core is moderate and the cost of it is low, ferrite cores are not preferred in the SST application due to their low saturation flux density, which results in a larger core size, conflicting with the high compact design requirement of the SST.

The Fe-amorphous alloy is a good choice for SST applications. The saturation flux density of this material may be as high as 1.56 T and its loss is also moderate. In addition, large cores, such as the C-type, are available, which suits well high power applications. However, the loss of this material with operating frequency higher than several tens of kHz can only be controlled by a low flux density, which leads to larger volumes. Another alternative is the Co-amorphous alloy that has a much lower loss compared with Fe-amorphous cores, however with a much limited saturation flux density.

Table 2-4 Comparison of different magnetic materials

Material	Alloy Composition	Loss (W/Kg) (20KHz,0.2T)	Saturation B_{sat} [mT]	Magneto-striction (10^{-6})	Permeability (50Hz) μ_4 - μ_{max}	Max working Tem.[°C]
Grain oriented silicon steel	$Fe_{97}Si_3$	>1000	2000	9	2k-35k	120
Advanced silicon steel	$Fe_{93.5}Si_{6.5}$	40	1300	0.1	16k	130
High performance ferrite	MnZn	17	500	21	1.5k-15k	100/120
Fe-amorphous alloy	$Fe_{76(}Si,B)_{24}$	18	1560	27	6.5k-8k	150
Co-amorphous alloys a	$Co_{73}(Si,B)_{27}$	5	550	<0.2	100k-150k	90/120
Co-amorphous alloys b	$Co_{77}(Si,B)_{23}$	5.5	820	<0.2	2k-4.5k	120
Co-amorphous alloys c	$Co_{80}(Si,B)_{20}$	6.5	1000	<0.2	1k-2.5k	120
Nanocrystalline alloys I	FeCuNbSiB	4.0	1230	0.1	20k-200k	120/180
Nanocrystalline alloys II	FeCuNbSiB	4.5	1350	2.3	20k-200k	120/180
Nanocrystalline alloys III	FeCuNbSiB	8.0	1450	5.5	100k	120/180

Overall, the nanocrystalline core is the best candidate among all for satisfying both the power density and efficiency requirements. On the one hand, its saturation flux density is much higher than ferrite—power density can be guaranteed, while on the other hand, its core loss is the lowest among all the materials in question, promising high efficiency. Only two important factors should be taken into account if the nanocrystalline core is considered. First, the cost of this core is relatively high, thus it is not suitable when the cost is the dominating limitation in the design. Second, the standard off-the-shelf core is toroidal uncut tape-wound core, thus further modifications are needed if other core shape is needed.

Three 10 kVA, 3.8 kV to 400 V, 3 kHz transformers using the Metglas SA2605SA1 amorphous core have been demonstrated [40]. The results obtained indicated that 97 % efficiency could be achieved with the selected core. In [41], design considerations for four

different high frequency transformers, specified at 100 kVA/20 kHz, 100 kVA/3 kHz, 33.3 kVA/20 kHz, and 33.3 kVA/3 kHz, were presented. The amorphous core was selected achieving design efficiency higher than 99 %. Comparisons of different core materials for a 250 kVA, 5 kV to 380 V, 20 kHz transformer were conducted, and the conclusion showed that nanocrystalline core achieves the best overall performance, while the amorphous core is preferred under cost considerations [42]. A 150kVA/10kHz transformer based on amorphous core was designed as shown in Figure 2-6.

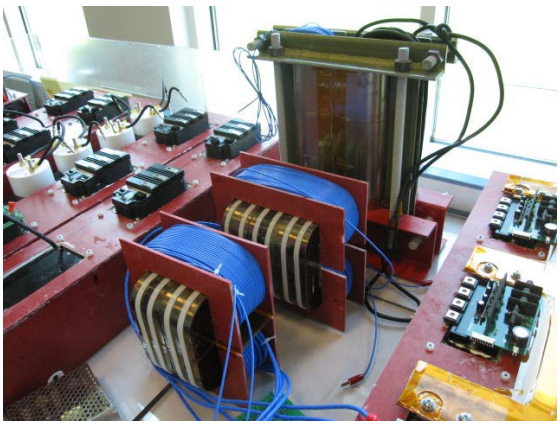


Figure 2-5 10kVA, 3.8kV-400V, 3kHz transformer based on amorphous core [40]

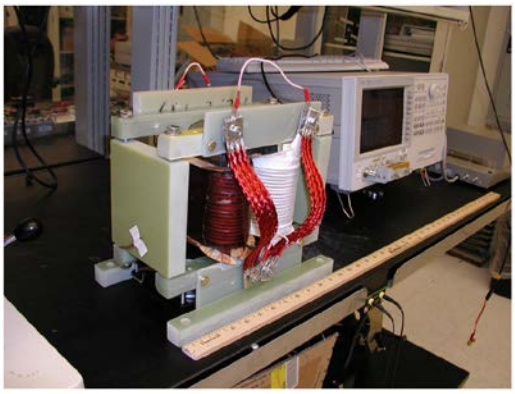


Figure 2-6 150kVA, 1.7kV-377.8V, 10 kHz transformer based on amorphous core [42]

In order to achieve extremely high efficiency and ultra-compact design, the nanocrystalline core VITROPERM 500F was investigated for a 1MW, 12 kV to 1.2 kV, 20 kHz transformer. The efficiencies for different core configurations were calculated, estimating that the efficiency could be as high as 99.99 % [43]. In [44], a 350kW, 8kHz transformer based on nanocrystalline core was designed for the medium frequency railway system, as shown in Figure 2-7.

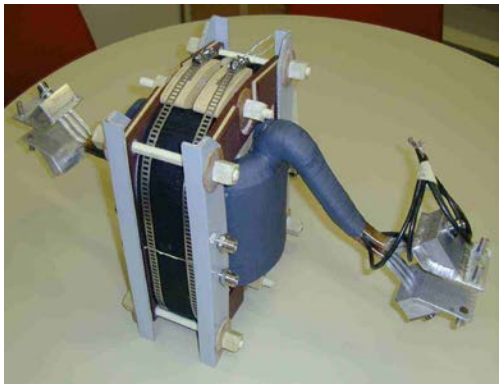


Figure 2-7 350kW, 8kHz transformer based on nanocrystalline core [44]

Transformer structures are of equal importance in order to satisfy high power density and high efficiency requirements. Generally speaking, there are two types of structures, solenoidal and coaxial winding transformers [33]. The solenoidal is the most common geometry of a transformer, in which the magnetic flux flows in parallel with the cylindrical axis and the current encircles the cylindrical axis.

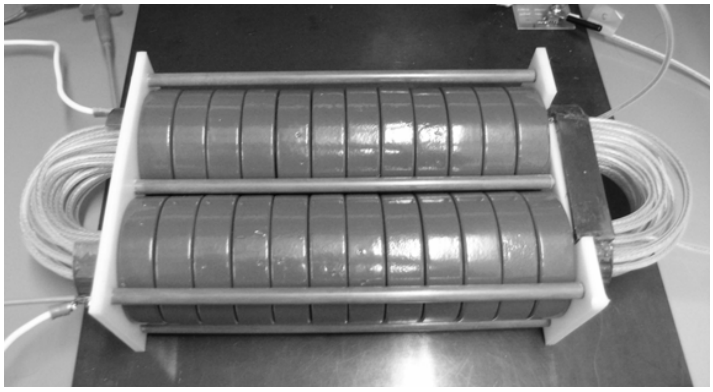
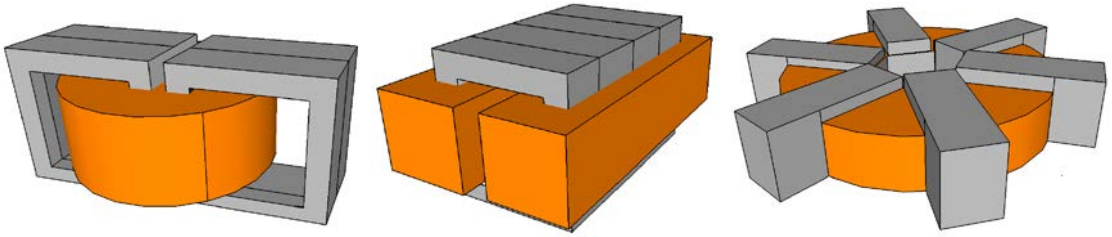


Figure 2-8 Structure of coaxial winding transformer [39]

In the coaxial structure, the flux encircles the cylindrical axis and the current flows in parallel with the cylindrical axis [45], as shown in Figure 2-8. Although it is easy to control and predict the leakage inductance of the transformer by using the coaxial structure, the solenoidal structure is preferred in most design cases due to its advantages from a design point of view, easier manufacturing, and lower cost [40], [41], [42], [43]. In addition, the flexibility of the solenoidal structure in terms of turn ratio is better than the coaxial structure. For both of these structures, multiple cores can be combined to build an equivalent larger window area, which is suitable for high power and high frequency applications [40], [41], [42].

Different solenoidal transformer structures are considered: namely core type, shell type, and matrix type transformers as shown in Figure 2-9 [43]. The core type transformer provides better insulation between the primary and secondary because of the inherent separation between its two windings. Shell type transformers provide a higher degree of mechanical protection to the winding because of the way the core surrounds it. In addition, a shell type transformer magnetic circuit is equivalent to a parallel electric circuit, so it has a lower reluctance compared to a core type transformer of similar cross-sectional area. In the high voltage step ratio condition, the matrix-type transformer can be used by inter-wiring core with series and parallel conductors [46], [47]. The manufacturing of the core type transformer is the easiest and this configuration is adopted the most.



(a) (b) (c)

Figure 2-9 Different solenoidal transformer structures: (a) shell type; (b) core type; (c) matrix type

Another two factors that should be taken into account are the thermal and insulation design, which are briefly introduced here. Compared with the conventional transformer, the thermal and insulation aspects are much more difficult in the SST since much less space is expected and oil-free operation is preferred. Natural convection is definitely the most

attractive solution if it is achievable [40]. However, different thermal dissipation methods can also be adopted depending on the application, among which the fan-cooled and water-cooled heat-sinks are the most common for high power density designs [43]. As to the insulation for this dry type transformer design, suitable solid insulating materials, such as epoxy, have to be inserted at the places where air is not enough for this high voltage and highly compact transformer design [40],[41], [43]. In addition, high voltage insulation wire is also an attractive candidate which significantly reduces the complexity of the transformer construction [43].

2.2.2 Recommendation for future work

The high voltage and high frequency transformer is the key component in the envisioned SST concept. Optimum design procedures should be further investigated to achieve high efficiency and low volume designs based on existing core materials, wires, and insulation means. It is also expected that better alloy optimization and process development can be done such that new core materials can be used [42]. In addition, efforts can be directed to the prediction of the parameters of the transformer, which is of great importance for higher frequency operation. Lastly, low volume and weight is always the emphasis for the design, thus good thermal designs are highly desirable.

2.3 Solid State Transformer topologies

2.3.1 State of the art technology

Numerous converter structures can realize the functions of isolated AC-AC conversion thus potentially suit for SST application [10], [11], [12], [13], [14],[16],[21],[36],[43],[44][24], [48], [49], [50], [51], [52], [53], [54], [55], [56], [57], [58], [59], [60], [61], [62], [63]. In order to document these topologies, an approach to classify the possible configurations has been presented [64], [65]. Considering possible conversion stages, there are four basic topology configurations as shown in Figure 2-10, namely type A, B, C, and D. Type A is the direct AC-AC conversion with transformer isolation to step down from high voltage AC (HVAC) to low voltage AC (LVAC) [21],[48], [49], [50], [51]. In type B, an isolated AC-DC conversion stage provides the low voltage DC (LVDC) followed by a DC-AC conversion stage to provide the low voltage AC [52], [56],[58], [59], [60], [63] (the topology in [52] can be categorized in either type B or C due to two isolated transformer adopted). Type C also contains the two-stage conversion, in which the galvanic isolation and voltage step-down are done by the DC-AC stage, therefore low voltage DC link is not available [54],[62]. Type D is a three-stage conversion with high frequency isolation in the DC-DC stage, thus both high voltage DC and low voltage DC link can be obtained [10], [11], [12], [13], [14], [16], [24], [36], [43], [44],[53], [55], [57], [61].

In addition, considering the limitation of the power devices and magnetic components, the aforementioned SST topologies may have to be connected in series or parallel for high

voltage and high power applications, as shown in Figure 2-11. Three possible connections are illustrated, which are input series output parallel (ISOP), input parallel output parallel (IPOP), and input series output series (ISOS). The input parallel output series (IPOS) connection is not included since it is the same with ISOP in this application. It is worth to point out that these SST configurations still fall into the four categories aforementioned from the conversion stage point of view.

The proposals in type A present possible low cost and light weight solutions due to the simple configuration. Four-quadrant power devices may be needed in case of bidirectional voltage and current operating condition. However, the lack of DC link makes them unsuitable for applications where reactive power compensation is required. In addition, disturbances on one side may also affect the other side, which is the drawback of traditional transformers. Type B and type C SSTs adopt two-stage configurations, with an isolation stage in either the high or low voltage sides. Four-quadrant power devices are also needed on the AC side of the isolation stage for bidirectional power flow. Compared with the type A configuration, reactive power compensation is possible for type B and C SSTs if suitable topologies are chosen. In addition, topologies in type A and B configuration are not suitable for high voltage operation since zero-voltage-switching (ZVS) is hard to be guaranteed in such a wide input range, and also mature multilevel topologies cannot be easily applied in the high voltage side. In this condition, high switching losses may not be avoided without sacrificing switching frequency, leading to lower efficiency and difficult thermal management. Type C topologies may not face such a problem since lots of works have been done for high voltage AC/DC conversion[66] . Nonetheless, the lack of the low voltage DC

bus makes the integration of renewable resources on the low voltage (potentially residential) side unfeasible.

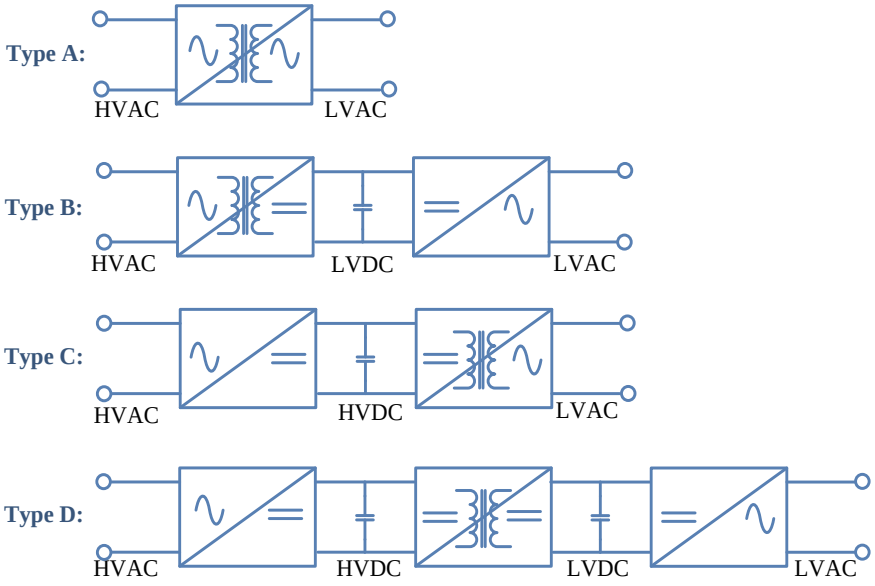


Figure 2-10 Topology classification of SST

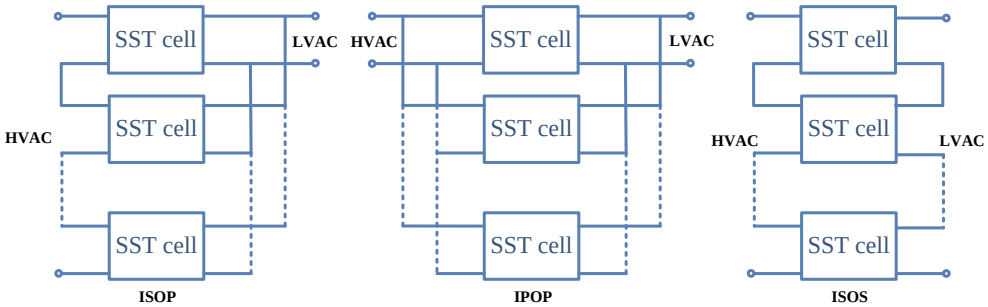


Figure 2-11 SST in high voltage and high power system

Most of the SSTs that have been designed for field application so far adopt the type D configuration since more available topologies can be chosen for each stage providing ample

room to optimize its performance in terms of efficiency, volume, and weight. Many attractive features, such as VAR compensation, voltage sag compensation, renewable energy resources and energy storage integration, and bidirectional power flow, may be potentially achieved. Four well known high voltage SST designs, namely the UNIFLEX [10], EPRI [13], GE [16], and ABB [67], are highlighted here since they have already been designed and fully tested for different applications. Table 2-5 summarizes the performance comparison of these four SST topologies.

Table 2-5 Performance comparison of four SST topologies

	UNIFLEX	*EPRI*	*GE*	*ABB*
Power rating	300 kVA	45 kVA	1MVA	1.2MVA
Phase number	Three	Single	Single	Single
Voltage rating	3.3 kV	2.4 kV	13.8 kV	15 kV
Transformer frequency	2 kHz	20 kHz	20kHz	1.8kHz
Eliminates oil	No	Yes	Yes	Yes
Var compensation	Yes	Yes	No	Yes
Voltage sag compensation	Yes	Yes	No	Yes
Voltage regulation	Yes	Yes	Yes	Yes
Harmonic isolation	Yes	Yes	Yes	Yes
Common DC link	No	Yes	Yes	Yes
Energy storage option	Yes	Yes	Yes	Yes
Fault isolation	Yes	Yes	Yes	Yes
Bidirectional power flow	Yes	No	Yes	No
Control complexity	complicated	Average	Easy	Average
Efficiency	92%	96%	98%	95%
Delivery Year	2009	2012	2011	2012
Application	Smart grid	DC charge station	Substation	Traction

Figure 2-12 shows the UNIFLEX SST topology for smart grid application [10]. Basically, it is a three-stage and three port power electronics converter used for universal and flexible power management for future electricity network. The cascaded multilevel converter is adopted as the front-end stage with several interleaving DC/DC converters as the intermediate stage. It interfaces 3.3kV distribution level voltage with low voltage grids, such as 415V system. Amorphous is adopted as the transformer core material and the operating frequency is chosen to be 2 kHz. Oil is adopted for insulation and cooling for this medium frequency transformer.

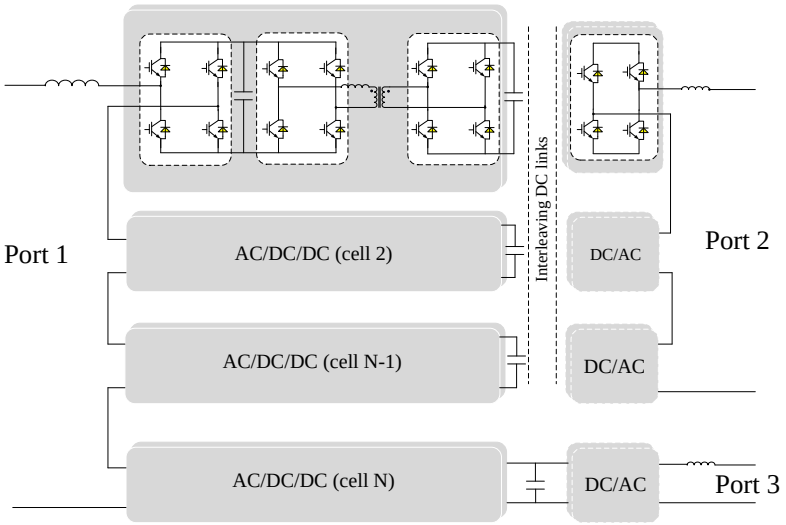


Figure 2-12 UFNIFLEX SST topology for smart grid application

Figure 2-13 shows the EPRI SST topology for DC fast charger application. The diode-clamped multilevel converter is applied for the high voltage side for both rectifier stage and primary side of DC/DC stage, in which the 18kV/60A multilevel IGBT module by using the integrated module packaging method is adopted. The simple diode rectifier is adopted for the

secondary side of DC/DC stage to generate the low voltage DC link. The ferrite core is used in the high frequency transformer with operating frequency of 20 kHz. In the DC fast charger application, another high efficiency DC/DC converter is connected to interface with the battery pack.

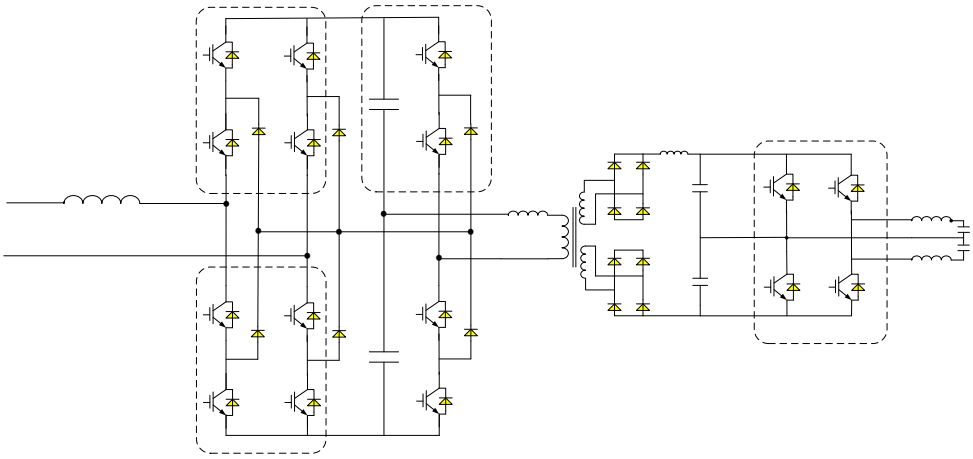


Figure 2-13 EPRI SST topology (with inverter stage) for DC fast charger application

Figure 2-14 shows the basic unit of GE SST topology for substation application. The 10kV/120A SiC half bridge module is adopted for the high voltage side and they are connected in series to reduce the voltage stress. The switching frequency of the unit is chosen to be 20 kHz and nanocrystalline core is therefore chosen as the core material for the transformer to reduce the core loss. One of the distinguished characteristic of this unit is the high efficiency due to the line frequency switching in both high and low voltage rectifier/inverter side and soft switching capability in the DC/DC stage. However, this unit

can only fulfill the basic voltage transformation and isolation functions of the conventional transformer, therefore may not be suitable for smart grid and traction applications.

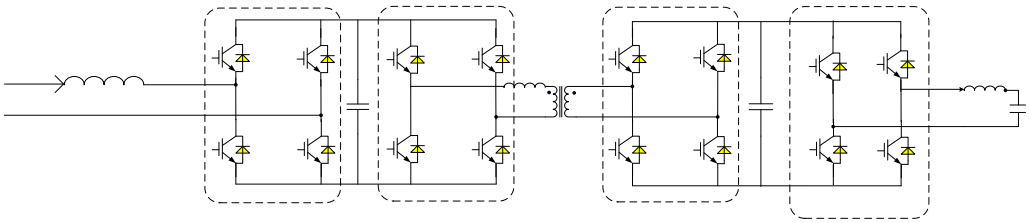


Figure 2-14 Basic unit of GE SST topology for substation application

Figure 2-15 shows ABB SST topology for traction application [67]. Cascaded multilevel converter is adopted as the input stage to interface with 15kV grid, and 6.5kV IGBT is chosen as the main switch for the H-bridge module. LLC resonant converters are then cascaded to each DC link with the secondary side connected in parallel to step down the voltage, and nanocrystalline core is adopted for the transformer design. There is no dedicated control implemented for the DC/DC stage of the system, meaning that the LLC converter operates in open-loop mode at its resonant frequency point for maximum available efficiency operation.

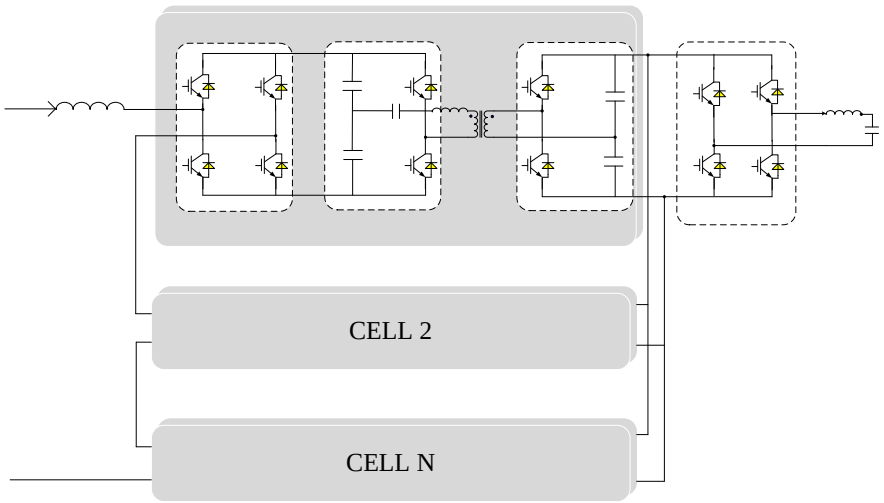


Figure 2-15 ABB SST topology for traction application

2.3.2 Recommendation for future work

The development of the SST can be divided into two paths. The first one looks for modular topologies using low voltage, high switching speed, and commercial power devices. The main issue with these topologies is the complex control algorithm needed, which has set the main research direction in this case, as well as how to minimize the volume and weight. The second path uses advanced post-silicon devices, such as high voltage SiC MOSFET/IGBT, to significantly reduce the volume and weight and potentially push the voltage and power rating to a much higher level. In this path, the main effort is how to solve the problem of extremely high dv/dt in the high voltage and high frequency operating condition. The soft switching techniques for DC/DC converter are well established. Therefore, soft switching techniques for the rectifier/inverter should be the research focus. In this condition, single stage or two stage topologies can be possibly adopted. For even higher voltages and higher power

applications, the best method is to integrate the above two approaches.

2.4 Applications of SST in the future distribution grid

2.4.1 State of the art technology

Efforts have been made to design and implement SSTs with satisfactory performance, as well as explore its use in the distribution system level. This is extremely important since new technologies have to rely on the market to survive. Figure 2-16 on one hand shows the traditional distribution system, where the transformer is adopted for integrating the renewable energy resources and energy storage devices, powering the traction/locomotive system, and interfacing the reactive power compensator/active power filters. On the other hand, the proposed future distribution system based on SST is also shown in Figure 2-16, which summarizes the potential application areas of the SST. It is seen that the SST can functionally replace the traditional transformer and some power electronics converters, thus indicating a potential more integrated and compact system.

a. Voltage transformation and regulation

The SST has found its application in traction systems, as shown in [44],[56], [57], [58], [59], [60], [61]. The traditional line-frequency transformer and back to back converter are replaced by the SST. Therefore, a more compact and lighter system can be obtained. 1.2 MVA hardware prototype has already been developed by ABB as presented before.

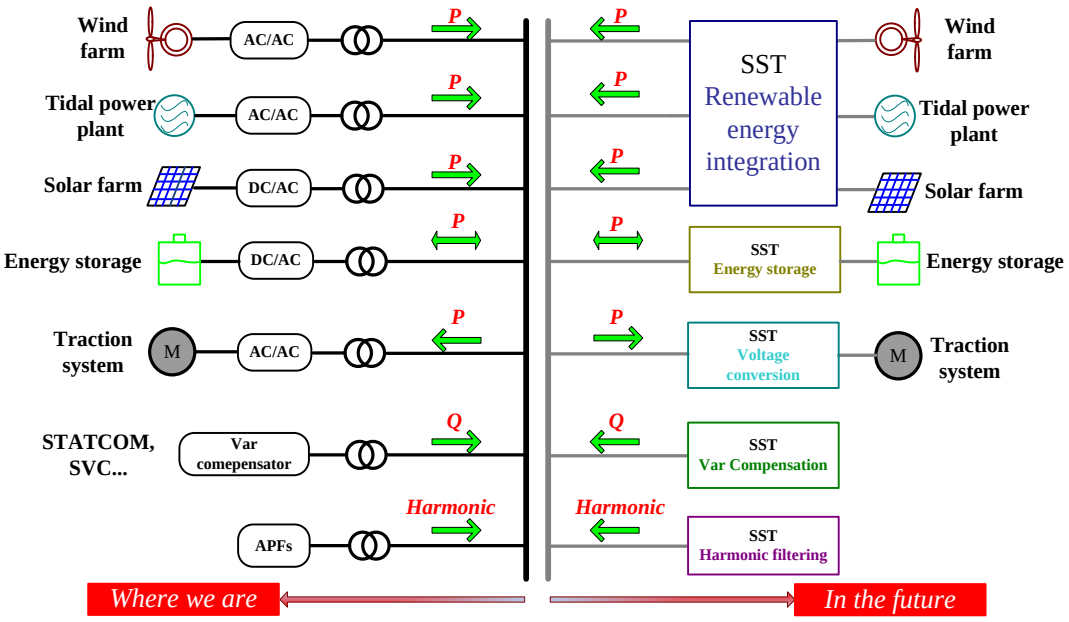


Figure 2-16 Proposed future distribution-level system architecture

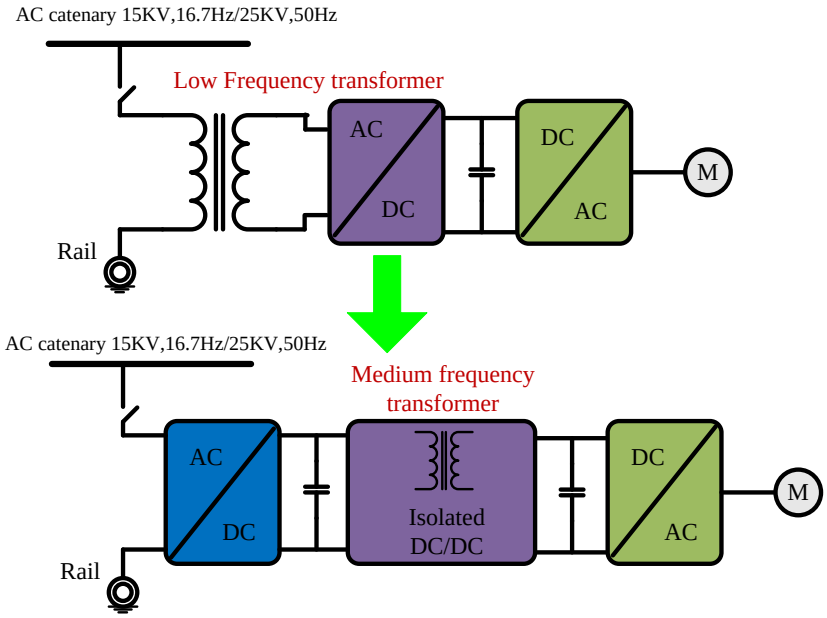


Figure 2-17 SST based tractions system

In addition, with the high penetration of renewable energies, such as solar [68], [69], wind [46],[70], and tidal power plants, the SST can also be adopted to directly connect these with the distribution system. Figure 2-18 shows the example wind energy system interfaced by the SST instead of the line frequency transformer for reducing the size and weight of the system.

Moreover, SST can also be potentially integrated with energy storage devices when its DC link is available. EPRI has demonstrated a 45 kVA, 2.4 kV fast charging station based on SST technology. The concept of this technology is shown in Figure 2-19. It exhibits higher efficiency and substantially decreased weight, thus overwhelming its counterparts [67].

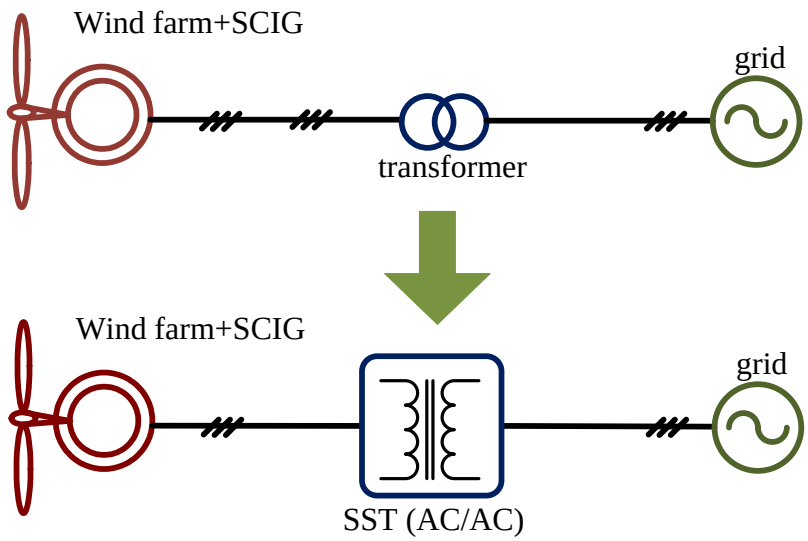


Figure 2-18 Wind energy system interfaced by SST

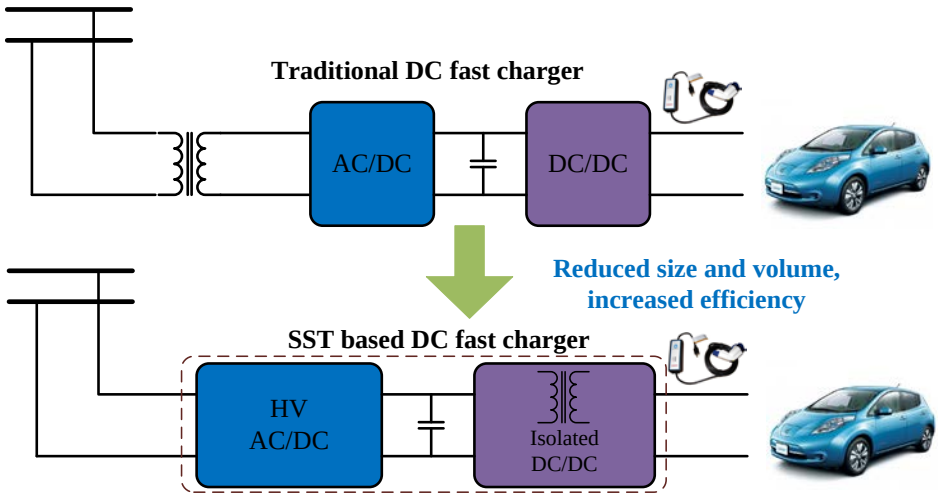


Figure 2-19 SST based DC fast charger

b. Reactive power compensation and Active filtering

As presented before, the SST may also provide VAR compensation depending on the topology adopted. SST-based dynamic voltage restorers were also studied in [71]. The SST may also take the responsibility of harmonic current filtering, while the capability of it depends greatly on the bandwidth of its controller, which is in turn governed by the switching frequency of the SST [72]. By combining these two functions, SST can also be utilized as the unified power quality conditioner (UPQC).

Figure 2-20 shows the proposed novel UPQC structure utilized in the distribution system. This UPQC gets rid of both the shunt and series transformer, which are all operating at line frequency. Therefore the size and weight of the system can be dramatically reduced. From the voltage conversion and isolation point of view, this UPQC can be regarded as a SST.

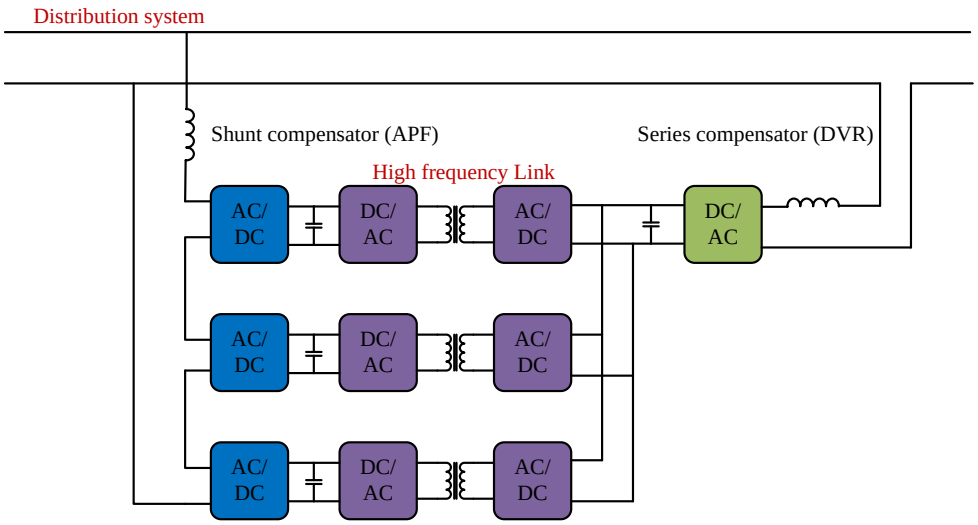
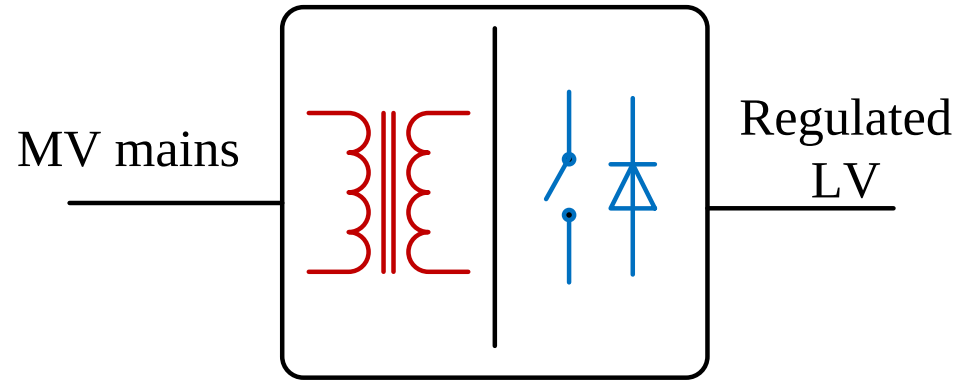
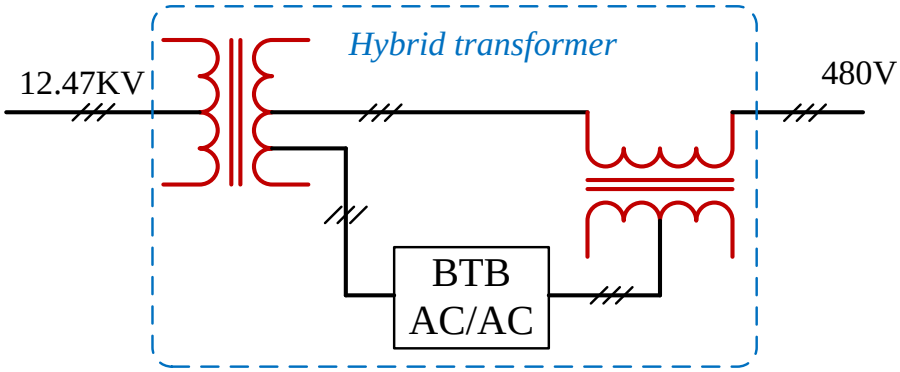


Figure 2-20 High frequency link UPQC structure

Considering the reliability and challenge in building the hardware for the high power SST, a more feasible path for the SST to replace the traditional transformer is to first adopt the so called hybrid distribution transformer concept, which is shown in Figure 2-21 [73]. The basic idea is to integrate the partial power converter with the traditional distribution transformer, thus the additional functions, such as voltage regulation, reactive power compensation, harmonic filtering, and etc. can be achieved in a certain range. ABB together with EPRI has successfully developed a 12.47kV/480V, 500kVA hybrid transformer with topology shown in Figure 2-21(b), in which a back to back (BTB) converter is integrated with a line frequency transformer. The rating for the power electronic converter is 125kVA, which is 25% of line frequency transformer rating. It can provide additional functions, such as voltage compensation, unbalance compensation, and fault diction compared with the traditional transformer [73].



(a) Concept of hybrid transformer



(b) Implementation of a 500kVA, 12.47kV/480V hybrid transformer [73]

Figure 2-21 Hybrid distribution transformer

c. Smart grid integration

The SST has also been proposed as an energy router to integrate with the smart grid [74]. Figure 2-22 shows the envisioned SST based smart grid architecture. The basic idea is to utilize the low voltage DC link as the common bus to connect the renewable energy resources (DRER) and distributed energy storage devices (DESD). Compared with the conventional ac/dc microgrid architecture which needs discrete components to regulate the power flow, this SST plays like an energy hub to coordinately manage the power flow among distribution system, dc microgrid, and ac microgrid. The idea itself is new while no

demonstration of such kind of system is provided yet before the work in this dissertation.

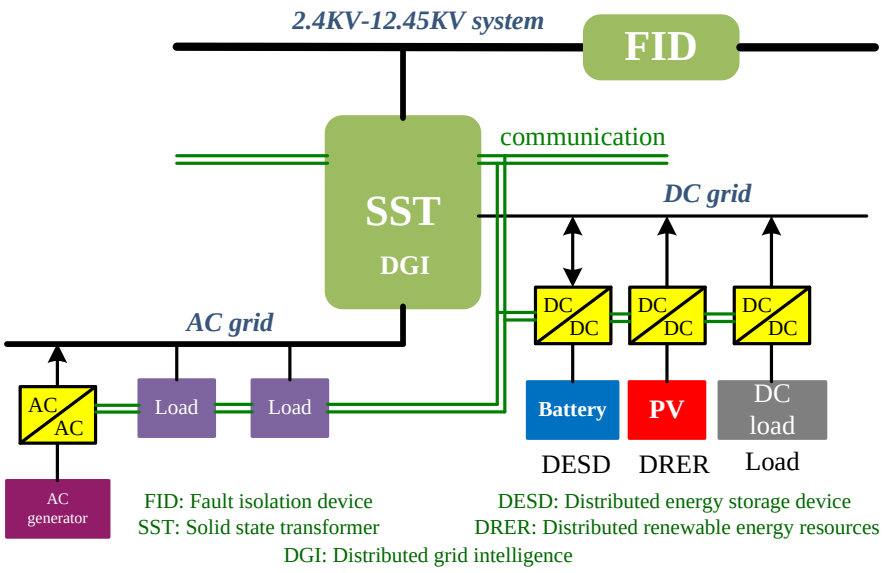


Figure 2-22 SST for smart grid integration

d. Fault isolation and limitation

Unlike the passive power transformer, SST embedded with certain control functions may also enact fault isolation and limitation. A protection method was proposed by using the SST, which showed satisfactory performance in real time digital simulations (RTDS)[75].

2.4.2 Recommendation for future work

Although it seems straightforward that the SST can replace the traditional transformer, it should be noted that stability problems given the increased proportion of regulated power electronics could ensue in the system. Efforts should be made thus in this direction to ensure that stability is maintained. Nonetheless, it is foreseen as an additional capability of the SST,

that it could actively stabilize the power system by monitoring the loading conditions upstream and downstream from its location. In addition, although SST can potentially achieve a more compact and smarter future distribution system, few detailed study, including system demonstration and power management strategies are available. It is therefore desirable to gain more experience in this area. Furthermore, how to integrate more functions of the SST in a single system and therefore to reduce the cost gap between SST and the conventional transformer needs more investigation.

2.5 Scope of the work of the dissertation

2.5.1 Research background

It is seen from the literature review that the SST technology has been a hot research topic, especially in the traction and smart grid areas. The emphasis and motivation of the presented work is to design a 3.6kV-120V/10kVA SST prototype, which can be integrated with the Green Energy Hub proposed by Future Renewable Electric Energy Delivery and Management (FREEDM) systems center. The basic diagram of the Green Energy Hub in the FREEDM systems center is depicted in Figure 2-22, in which the SST behaves as an active interface between distribution system and the residential system. The SST in the presented FREEDM systems can be regarded as an energy hub, which integrates with the advanced communication technology, can manage the power flow within distribution system, ac and dc residential grid.

As discussed before, the three-stage SST topologies dominate in the real hardware designs targeted at the distribution system. In addition, the modular multilevel topology is the most promising one when high voltage/power operation is needed. In this dissertation, a cascaded multilevel converter based three-stage SST topology, shown in Figure 2-23, is presented as the research target. This topology is named as generation-I solid state transformer in the FREEDM systems center. The cascaded multilevel converter is adopted as the front-end to interface with the distribution system, while dual active bridge (DAB) converter is adopted as the DC/DC stage with the secondary side connected in parallel to generate a low voltage DC. The DAB converter is adopted here because of the low components, high power density and high efficiency characteristics of it. In the last stage, an inverter is used to generate the low voltage AC for residential use. In this dissertation, 6.5kV Si based IGBT is adopted for the power stage and amorphous core is adopted for the transformer design in this design to verify the main concept of the SST and to develop suitable control algorithms and application areas of it. However, the same topology can be applied when with high voltage SiC devices and nanocrystalline core switching at a much higher frequency, and therefore achieve much better power density and potential improvement of the efficiency.

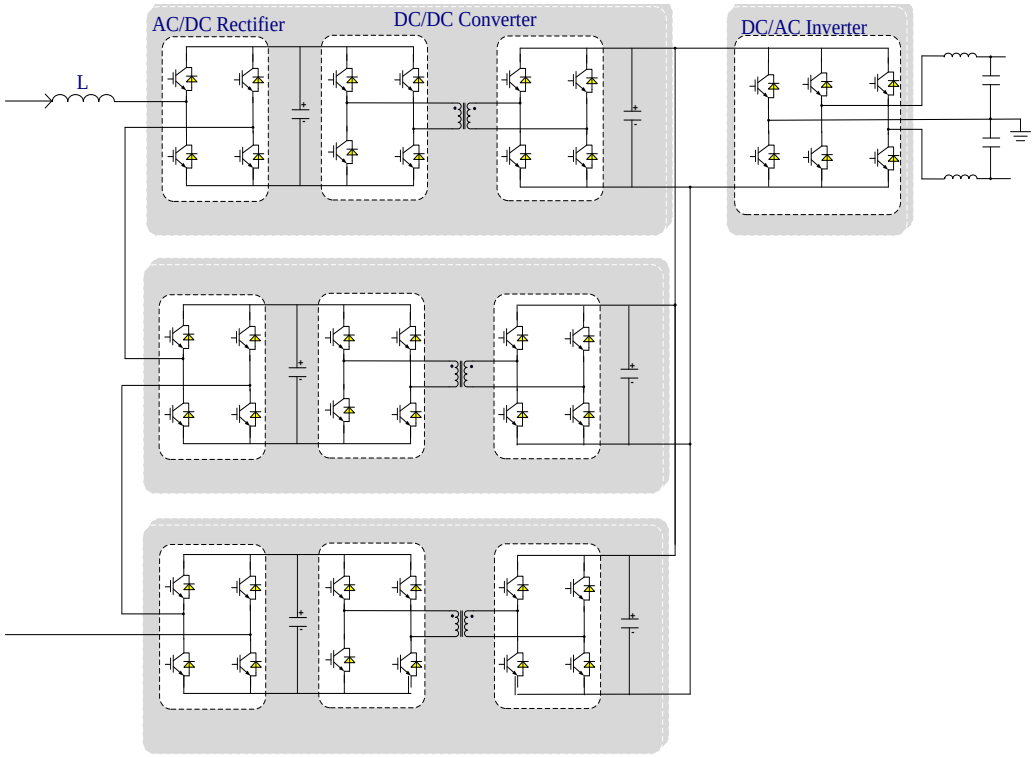


Figure 2-23 Topology of a cascaded multilevel converter based three stage SST

2.5.2 Research objectives and challenges

Two important factors need to be addressed when designing the controller for this cascaded multilevel converter based three-stage SST:

(1). The DC link voltages at the front-end rectifier stage will not be identical when with different operating conditions for each H-bridge. The voltage unbalance cause unequal voltage stress of the power devices, decreasing the reliability of the system. From this perspective of view, the voltage balance in the rectifier stage should be guaranteed.

(2). Even when the input and output voltage of each DAB converter becomes the same, the current among DAB converters in the DC/DC stage may be different, which cause unequal current and thermal stress in each module. From this perspective of view, the current balance in the DC/DC stage should be guaranteed.

Different methods have been proposed in the previous works, and these methods can be classified according to the availability of the voltage and current balance controller. Basically, there are four possible combinations as shown in Figure 2-24. The methods are published in [67][76][77] and [78] and are marked as [1]-[4], respectively. Obviously, if the parameters of the modules are totally identical, the voltage and current balance controller are not necessary, and this is demonstrated in [67]. Otherwise, the voltage and current balance controllers should be taken into account.

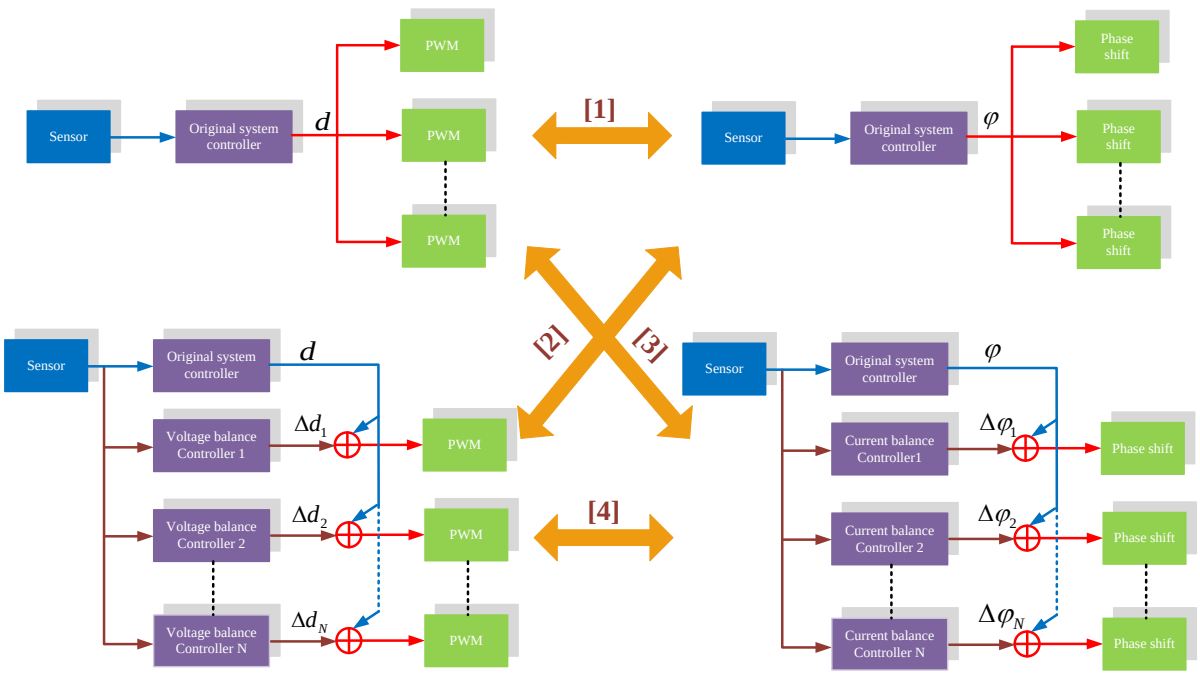


Figure 2-24 Different control methods for the presented SST topology

Then two questions come out subsequently:

(1).What is the main reason for voltage and current unbalance?

(2). Are voltage and current balance controller both necessary?

Figure 2-25 shows the equivalent circuit at the output of the rectifier stage. The output voltage of the rectifier can be represented by:

$$v_{out} = i_{out}.Z = (i_{in} - i_c).Z = [f(i_{hac}, S_{rec}, P_{device}) - f(P_c)].Z \qquad (2\text{-}1)$$

Where, i_{hac} is the input current of the rectifier, S_{rec} is the switching pattern of the H-bridge, P_{device} stands for the parameters of the device, e.g. voltage drop, and P_c stands for the parameters of the capacitor, e.g. equivalent of the series resistor (ESR). Shown in Eq. (2-

1), i_{in} is the function of i_{hac} , S_{rec} , and P_{device} . In addition, the value of i_c relates to the parameters of the capacitor.

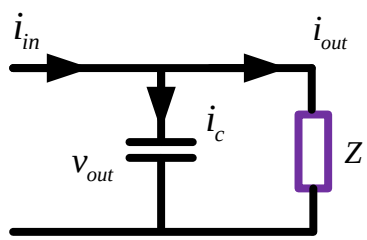


Figure 2-25 Equivalent circuit at the output of rectifier stage

Since the currents are equal for all the H-bridges due to the series connection fashion, Eq. (2-1) shows that the unbalance of the DC link voltage could be caused by the mismatch of active and passive components, different switching patterns, a limited control resolution, and different loads. Among all these issues, the load conditions at DC port of each H-bridge dominates when the active power is delivered. Other issues, such as the mismatch of the power devices, switching patterns, and control resolutions, are regulated to be small by the manufactures and design. Therefore, if the load condition of each H-bridge is the same, the voltage balance of the cascaded multilevel rectifier stage can be nearly guaranteed.

In the presented SST topology, several DAB converters are cascaded with rectifier, to which it operates as an active load. Figure 2-26 shows the equivalent circuit of the DAB converter considering only the fundamental component.

The power transferred can be calculated by:

$$P = \frac{V_1.V_2.\sin\varphi}{X_L} = \frac{f(V_{hdc}, S_h, P_{device}).f(V_{ldc,}S_l, P_{device}).\sin\varphi}{X_L} \qquad (2\text{-}2)$$

Where, V_{hdc} and V_{ldc} are the input voltage and output voltage of the DC-DC converter, S_h and S_l are the switching patterns of the H-bridges in the primary side and secondary side of the converter, P_{device} stands for the parameters of the device, e.g. voltage drop. Similarly, the differences among the power devices used in each DAB converter are also small, therefore may be neglected. However, parameters of the high frequency transformer, especially the impedances, may vary in a relatively large range. This claim can be verified by looking at different power transformer standards, although they are targeted at the line frequency transformer. In fact, due to the parasitic parameter effects at high frequency, the impedance of the high frequency transformer should be more difficult to control.

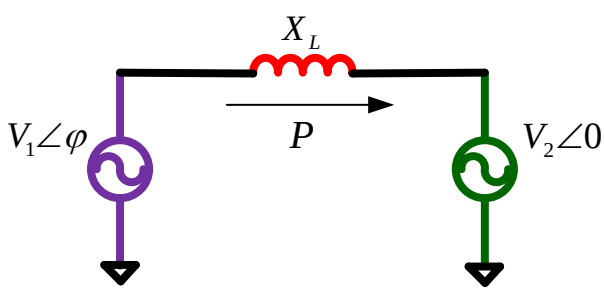


Figure 2-26 Equivalent circuit of the DAB converter

Table 2-6 shows the comparison of different power transformer standard, especially the ANSI/IEEE and IEC, for tolerance of the turns-ratio and impedance [79]. It is seen that difference of the turns-ratio of the transformer could also be controlled within a very small range, normally less than 0.5% of the rated value. However, the impedance tolerance could

be as high as ±7.5% to ±10% with different impedance range. In this condition, we may allow 15% to 20% parameter mismatch for two different transformers manufactured.

Therefore, we can foresee that the impedance mismatch of the high frequency transformer contributes most to the voltage unbalance of the rectifier stage. Furthermore, this will also raise the current unbalance issue in the DC/DC stage even if the DC voltage is balanced by certain mechanism as shown in chapter 5. From this perspective of view, dedicated controllers should be developed to ensure the voltage and current sharing of the system.

Table 2-6 Comparison of the tolerances of impedance and turns-ratio of power transformer: ANSI/IEEE and IEC standard [79]

Subject Issue	ANSI / IEEE		IEC	
	Standards	Requirements	Standard	Requirements
	C57.12.00-2010		IEC 60076-1	
Tolerances impedance	9.2	Two winding transformer Impedance of transformer > 2.5% Tolerance ±7.5% Impedance ≤ 2.5% , Tolerance ±10% Three winding, zig –zag winding and auto-transformers tolerance ±10%	9(3) & (4)	Two winding transformer a) Principal tapping Impedance value is ≥ 10% tolerance ±7.5% Impedance value <10% Tolerance ±10% Any other tapping of the pair Impedance value is ≥ 10% tolerance ±10.0% Impedance value <10% Tolerance ±15% Multi-winding & auto transformer Principal tapping ±10% of specified value Any other tapping of the pair ±10% of the design value for that tapping Other pairs of winding , to be agreed but ≥ 15%
Tolerances ratio	9.1	Transformer at no load 0.5% of the nameplate voltage. When the volts per turn of the winding exceeds 0.5% of the nameplate voltage, the turns ratio of the winding shall be to the nearest turn.	9(2)	At no load on principal tapping Lower of a) ± 0.5 % of specified ratio b) ±1/10 of actual percentage impedance on the principal tapping Other taps (same pair) ± 0.5% of design value of turns ratio Other taps(further pairs) ± 0.5% of design value of turns ratio

Based on aforementioned analysis, the answers to the above questions are:

(1) The main reason of the voltage and current balance issue of the system comes from the parameters mismatch of the high frequency transformer, especially the impedance difference of the DC/DC stage.

(2) Considering the parameter mismatch, the current balance controller of the DC/DC stage is necessary, however the voltage balance controller of the rectifier stage may be avoided considering the small parameter difference among the power devices and DC capacitors.

In fact, take voltage balance controller into account will help balancing the DC link voltage from the source point of view, which is complementary to the current balance controller from the load point of view. Therefore, two controllers can work together for the better stabilization of the system, especially for reducing the voltage overshoot at the start-up caused by the parameter mismatch. In addition, the voltage balance controller in the rectifier stage is needed if considering the extreme operating condition, such as fault tolerant operation. For example, if one of the DAB converters fails and it is bypassed, the voltage balance controller in the rectifier stage is needed to reduce the voltage imbalance caused by the power imbalance of the DC/DC stage. Furthermore, the involvement of the voltage balance controller of the rectifier stage may reduce the hardware component of the current balance controller of the DC/DC stage, which is shown later in chapter 5. Therefore, both controllers may be needed and can actually contribute to the performance of the system.

Various methods have been proposed to maintain the balance of DC capacitor voltages in cascaded multilevel converter based applications. These methods can be grouped into two categories.

The first one achieves DC voltage balance by utilizing advanced modulation techniques. The selective harmonic elimination (SHE) modulation was used to balance the DC capacitor voltage by swapping the pulse signals [80], [81],[82]. These methods are simple and the number of the DC sensors can be greatly reduced since no feedback loop is involved for balancing the voltage. However, these methods can only balance the DC voltage imbalance caused by the inconsistent drive pulse. The space modulation method proposed in [83], [84], [85] may be modified to achieve the voltage balance with extremely fast response however this is not done before the work presented in [15]. In [86], a modular strategy for control and voltage balance of cascaded H-bridge rectifiers is presented, which is mainly based on PWM reconfiguration according to the working situation.

The second method achieves the voltage balance by using feedback loop control. The methods based on regulation of the phase shift-angle are proposed in [87]. A good small-signal based voltage balance control for STATCOM has been proposed in [88] and it has minimum effect on voltage quality. In [89], an overview of three Proportional-Integral (PI)-based control methods for multilevel active rectifier is presented and the tuning process of the Proportional-Resonant (PR) controller is also given. The authors in [90] propose a model-based voltage balance controller in the shunt active filter application by adding a regulation loop and a balance loop to adjust the two DC voltages to the same desired value. Watson et al. presents an interesting feedback control with SHE modulation, designed with the aim of DC voltage balance at a low switching frequency [91]. The authors in [92], [93] propose the voltage balance controller, which is divided into clustered control and individual control for motor drive and STATCOM application. In [94], the per-phase voltage balance control is

proposed. All aforementioned methods are instructive, although they do not address the coupling effect between voltage balance controller and original system controller. Several controllers have been proposed with consideration of the coupling issue. In[95], [96], a modular strategy for voltage balance control of cascaded H-bridge rectifiers is proposed. However, a cosine value is included in the denominator of the loop, making the system easily unstable. By distributing the duty cycles to each H-bridge according to the output of the DC voltage balance controller, the method proposed in [97] achieves the DC voltage balance as well as guarantees the power transferred by the rectifier. Authors in [98] propose an active vector superposition method for STATCOM application. Comparing with modulation index regulation and phase-shift regulation, the active vector superposition method shows the best performance in terms of stability and regulation capability. However, this method is based on the vector analysis in steady state and still does not decouple the control loops when considering the dynamic response of the system. Furthermore, only P controller can be adopted for this method, therefore the steady state error exists. In fact, a good mathematical modeling of the system can help identifying the coupling terms between two controllers in all the operating conditions, and therefore guide the controller architecture design to eliminate it. However, this is not done before the work presented in this dissertation.

The current balance controller is also investigated by previous works for the presented SST topology. In order to balance voltage of the rectifier stage as well as the power of the DC/DC stage with various parameter mismatch, voltage and power balance controllers are proposed in[78], which can achieve good performance according to the simulation. However, this method needs additional current sensors for the DAB stage and these current sensors

should be high speed ones since it uses the DAB leakage inductor current as the feedback, which is a high frequency AC one. In [77], a common duty ratio controller for the rectifier stage in the single phase d-q coordinate and feedback feed-forward controller for the DAB stage are proposed. However, this method only considers the voltage balance among the DC links in the front-end cascaded multilevel rectifier. The power balance issue when considering the parameter mismatch among the DC/DC converters is not demonstrated. Furthermore, the disturbance in either low voltage or high voltage DC link will be transferred directly to the other by using this method due to the feed-forward control fashion. In this condition, as one of the distinguished advantages of the SST, the disturbance rejection capability is affected. Similar converter structures are also proposed in [61] and [76]. However, the parameters in the DC/DC stage are assumed to be the same by appropriate design and no dedicated controller is presented. Therefore, how to balance the current in the DC/DC stage with minimized hardware and software effort considering the parameter mismatch of the system is not addressed well.

In addition, the design and experimental demonstration of the SST prototype for smart grid application is also a challenge considering the high voltage and high power operation, as well as the communication requirement. Lots of previous works in academia mainly focuses on the low voltage conceptual verification of the SST, very few detailed design information are provided for high voltage SST especially in the smart grid application. Therefore, the design methodology of the high voltage SST should be provided for readily use in the smart grid environment.

Furthermore, except for the control and design issues of the presented SST topology, the exploration and demonstration of SST in the future distribution system is of great importance. As presented in 2.4, although researches have been done to integrate SST with various renewable energy resources, the SST is just a simple replacement to the traditional transformer or only one function is used, making the cost of it much higher than its counterpart [44],[56], [57], [58], [59], [60], [61]. How to integrate more functions of SST in a single system and therefore to minimize the cost gap between two technologies are still not clear.

Lastly, although it is known that the SST can be potentially integrated with the microgrid system[74]. No system evaluation and demonstration have been developed before. It is therefore highly demanded to develop a system evaluation platform and corresponding power management strategy to demonstrate the advantages of such kind of a system.

Considering the challenges discussed above, the objective of this dissertation is to:

(1). Develop advanced control architectures for this modular type SST with satisfied voltage and current sharing performance at the minimal cost.

(2) Present the design methodology of the high voltage SST and demonstrate the advanced features of it by using the proposed control methods.

(3). Develop a novel SST interfaced wind energy system with integrated functions of active power transfer, reactive power compensation, and voltage conversion.

(4). Demonstrate the integration of SST with zonal DC microgrid with centralized power management strategy.

Chapter 3 A New Voltage Balance Controller for the Cascaded Multilevel Rectifier Stage: Minimize the Coupling Effect

3.1 Introduction

Multilevel converters are appealing solutions for high voltage applications since it is generally difficult to utilize a single power semiconductor to switch directly [66]. Cascaded multilevel converter has gained considerable attention recently compared with other multilevel topologies due to their advantages in terms of modularization, extendibility, and minimization of power semiconductors[66],[99], [100]. It has been proposed and widely employed in high voltage and high power applications such as inverters in ac motor drives, battery system, static synchronous compensators (STATCOM), and active power filters (APF) [74], [75], [93–95]. Another attractive application is to use of this topology as a bidirectional active rectifier because of the available distinct dc links feeding separate loads [89]. It can reduce harmonic distortion on the AC side and provide satisfactory regulation for all DC links. A good application example is the solid-state transformer (SST), which adopts a seven-level cascaded rectifier as the high voltage side interface with distribution systems [78].

DC capacitor voltage imbalance is an inherent problem multilevel converter. In a cascaded multilevel converter, this may result from the mismatch of active and passive components, different switching patterns, a limited control resolution, and different loads (operating as

rectifiers) [88], [89]. The imbalance of the DC capacitor voltage will lead to the degradation of input current, imbalance of loss in each H-bridge, and, potentially, the collapse of the entire system (over voltage, over current, etc.) [103]. This problem becomes more serious when it operates as a rectifier with several loads connected to each DC port since it may have larger variance of power distribution among H-bridges. More specifically, three DAB converters, which act as an active load, are connected to three DC ports to share the total power of the system in the SST application. With the parameter mismatch in the DC/DC stage, the power will become unequally distributed and DC voltages will diverge if no voltage balance control is adopted. Under this situation, some devices in rectifier stage face the risk of over-voltage failure, which may collapse the whole SST system. Obviously, voltage balance capability is necessary for reliable operation of the system.

Figure 3-1 shows the generalized voltage balance control based on feedback control loop by regulating the duty cycle. It is noted that the methods that only regulate the phase shift between the PWM voltage and the current is not covered. Basically, a so called original system controller, which consists of dual-loop structure, is adopted to generate the common duty cycle d for modulation. If the loads connected in each DC link are balanced and the effect of the small mismatch of circuit parameters are neglected, this common duty cycle can be applied to each H-bridge for synthesizing the desired PWM voltage. However because of the load differences when operating as the rectifier, additional modification of the duty cycle Δdi is needed and it is generated by the voltage balance controller.

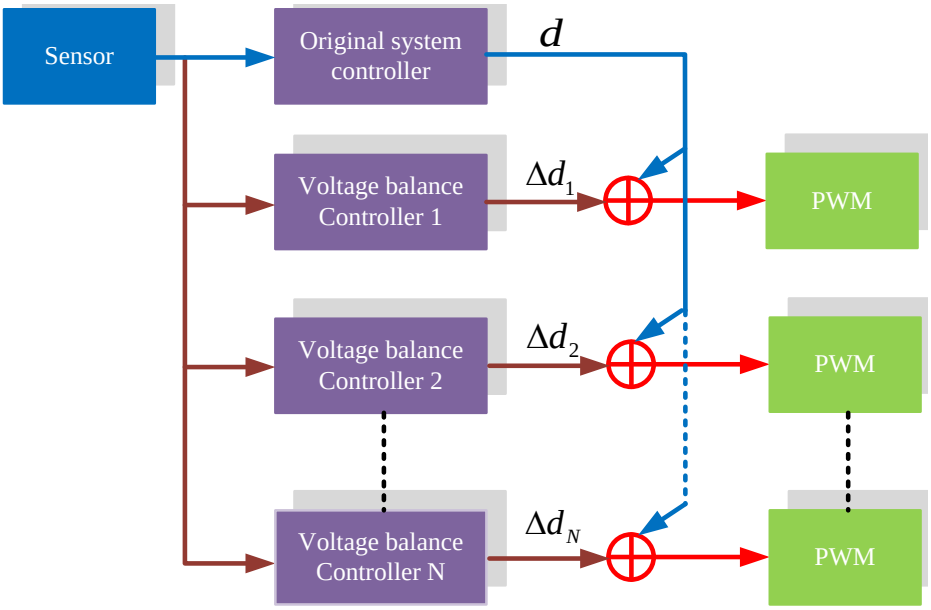


Figure 3-1 Generalized voltage balance control diagram based on feedback control loop

The basic requirement for a DC voltage balance controller is to balance the DC link voltages under all operating conditions. While a good DC voltage balance controller should also be simple, fast, and easily expanded to a cascaded converter with N H-bridges. Additionally, the reactive power should be controlled independently of the active power, thus it can potentially be equally distributed in each H-bridge cell according to the requirements. Furthermore, the voltage balance controller should couple with the original system controller as little as possible. The last point emphasized here requires a control system that can be separated into two decoupled layers. The upper layer controls only the total DC voltage and power factor without considering the DC voltage imbalance, which is defined as the original system controller. The lower layer only eliminates the DC voltage differences among H-bridges, which is defined as the voltage balance controller. By doing such, the design

procedure of two controllers can be decoupled and the design process can be as simple as a two level converter.

In this chapter, a new voltage balance controller in d-q coordinate is proposed to reduce/eliminate the coupling effect between the voltage balance controller and the original system controller for single-phase cascaded multilevel converters[104], [105]. D-q vector control is adopted since it has the advantage of zero tracking error for AC signals, thus has been adopted in many applications [93], [94]. Moreover, this method can realize regulation of active and reactive power independently, thus has the potential to fulfill the concept proposed in [95], [96], which can balance DC capacitor voltages as well as maintain equalized reactive power distribution among H-bridges if an individual modulation is applied . It is necessary to point out that the same methodology can be applied to the three phase system.

This chapter firstly establishes the average model and small signal model in d-q coordinate with consideration of DC voltage imbalance for a single-phase cascaded multilevel converter. Then the coupling term between two controllers is identified and a control scheme is proposed to eliminate it. Design considerations, including transfer functions and effective voltage-balancing area of the proposed control system are illustrated. Comparisons between the proposed method and previous methods are conducted and the potential realization of equal reactive power distribution is demonstrated. Furthermore, reference generation techniques for voltage balance controller are discussed and proved to be of significant impact to the DC voltage balance during the startup process. A suitable reference is then chosen to

eliminate this undesired impact. Finally, simulations and experiments are provided to validate the theoretical findings [104][105].

3.2 Controllability analysis of the voltage balance controller

The controllability of the voltage balance controller mainly depends on the saturation of the modulation index, which should theoretically be less than one. Different voltage balance controller may have different controllable range. In order to identify the suitable method to synthesis the needed PWM voltage, the vector analysis in d-q coordinate is adopted to illustrate this. It is noted that the vector analysis only gives the steady state description of the system.

For analysis simplicity and without losing generality, take cascade multilevel rectifier with three H-bridges as an example. Figure 3-2 demonstrates the vector analysis of operation principle and stability analysis of the proposed method. $\dot{v}_{ab1}, \dot{v}_{ab2}, \dot{v}_{ab3}$ are the PWM voltage of each H-bridge with no voltage imbalance. When the load is unbalanced, certain modifications of the duty cycles, which are Δd_1, Δd_2, and Δd_3 , should be adopted. Without losing generality, assuming that:

$$\Delta d_1 > \Delta d_2 > 0 > \Delta d_3 \tag{3-1}$$

There are two possible ways to do this.

(1) The modification of duty cycle is added to the original active duty circle. Shown in the red line of Figure 3-2, by adding an active vector to original PWM voltage, $\dot{v}_{ab1m}$ and $\dot{v}_{ab2m}$ are synthesized.

(2) The modification of duty cycle is added to both active and reactive duty cycle, as shown in the purple line of Figure 3-2.

Considering the assumption made in (1), the first H-bridge decides the effective controllable area, which is illustrated in shaded area of Figure 3-2. Originally, the H-bridge 1 works at point A without the voltage balance controller. Assuming that H-bridge 1 works at critical mode by using the first method as shown in point B, H-bridge 1 will work at point C by using the second method. In this condition, the modulation index of two methods will be:

$$(d_d + \Delta d_1)^2 + (d_q + \frac{\Delta d_1 d_q}{d_d})^2 > (d_d + \Delta d_1)^2 + (d_q)^2 = 1 \qquad (3\text{-}2)$$

Obviously, the first H-bridge works under over-modulation, which implies that the DC capacitor voltage balance is not guaranteed anymore. Therefore, the first method should be adopted for maximizing the controllable range.

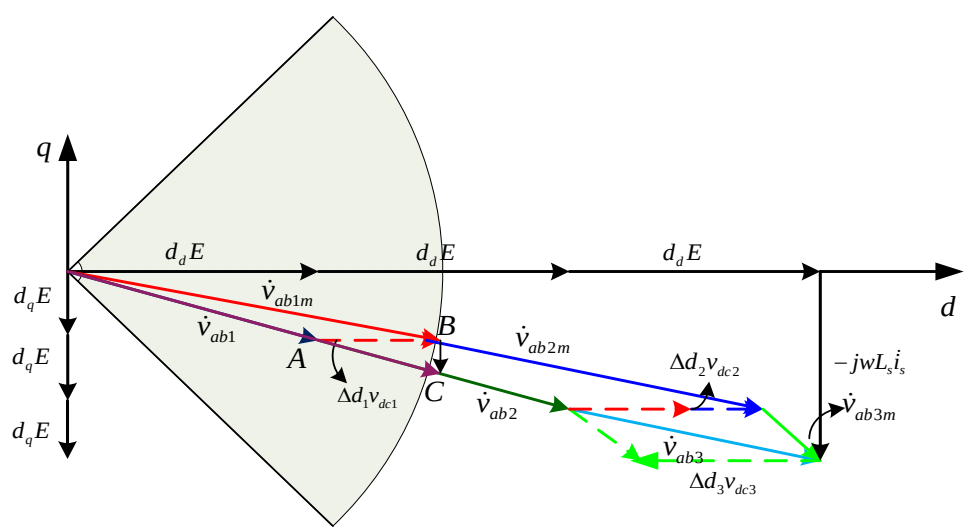


Figure 3-2 Controllability analysis of the voltage balance controller

3.3 Modeling of system in d-q coordinate considering voltage imbalance

Figure 3-3 shows the configuration for a single-phase cascaded multilevel rectifier with N H-bridges. v_s is the voltage at point of common coupling (PCC), L_s is the smoothing inductor, and R_s is the equivalent resistor of the inductor ,wire, and switching losses. C_i and R_i ($i = 1...N$) are DC capacitors and loads in each DC output. N H-bridges are connected in series to synthesize a 2N+1 level waveform, which is v_{ab}, from N isolated DC voltages, which are denoted as $v_{dc1} - v_{dcN}$. T_{aij} $(i = 1...N,\ j = 1...4)$ denotes the switches in the converter.

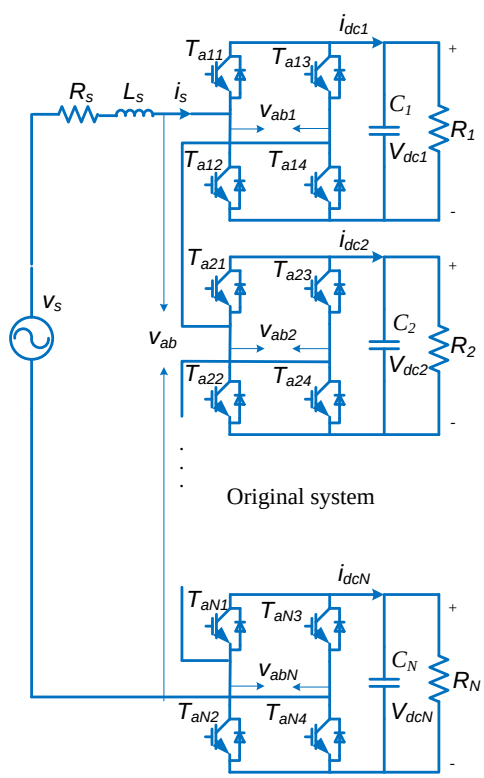


Figure 3-3 Original N H-bridges cascaded multilevel rectifier

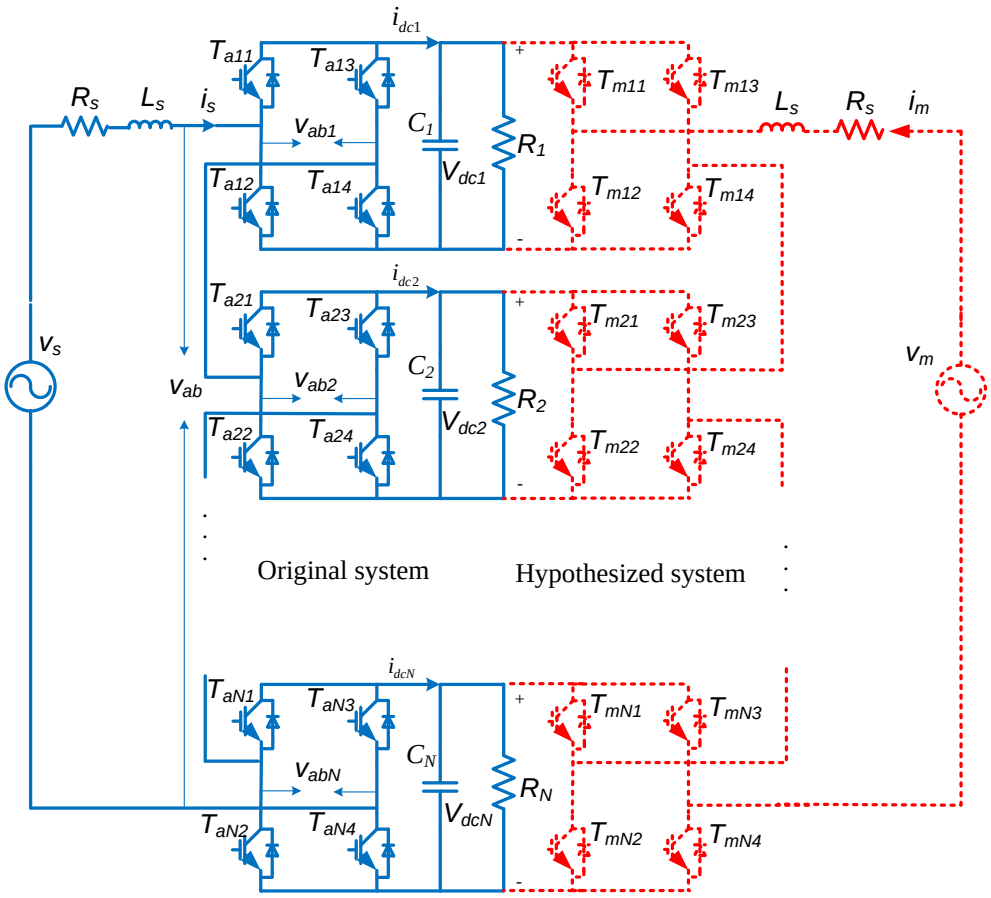


Figure 3-4 N H-bridges cascaded multilevel rectifier with hypothesized phase

In contrast to the three-phase system, there is only one phase in the single-phase system. In order to realize the single-phase d-q transformation, N imaginary H-bridges, lagging 90^0 from the original N H-bridges, must be hypothesized [106]. The hypothesized H-bridges are illustrated in the dotted-line shown in Figure 3-4. The inductor currents in the real and hypothesized cascaded H-bridges are represented as i_s and i_m while the PCC voltage for the hypothesized converter is v_m . $T_{mij}(i=1...N, j=1...4)$ denotes the switches in the hypothesized converter. The relationship between the AC values in original system and hypothesized

system, such as v_s and v_m, is shown in Figure 3-5. The v_m, which is shown in the dotted-line, lags 90^0 with the v_s, represented by the solid-line. The detailed theory of the single-phase d-q transformation can be found in [29].

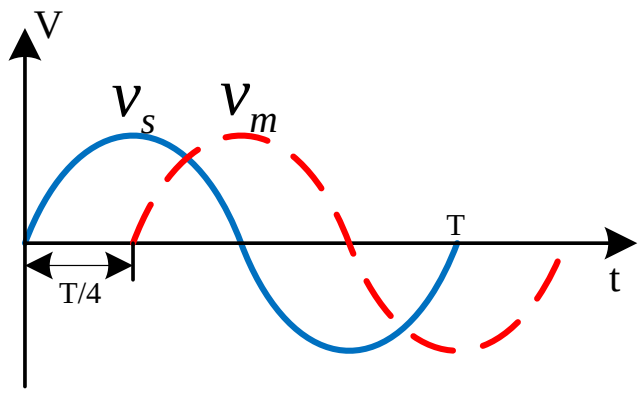


Figure 3-5 Relationship between values in real and hypothesized circuits

Define the switching functions of both real and hypothesized phase in cascaded converter as:

$$S_{ai} = \begin{cases} -1, T_{ai2}, T_{ai3} ON \\ 0, T_{ai1}, T_{ai3} ON; or T_{ai2}, T_{ai4} ON \ (i = 1...N) \\ 1, T_{ai1}, T_{ai4} ON \end{cases} \qquad S_{mi} = \begin{cases} -1, T_{mi2}, T_{mi3} ON \\ 0, T_{mi1}, T_{mi3} ON; or T_{mi2}, T_{mi4} ON \ (i = 1...N) \\ 1, T_{mi1}, T_{mi4} ON \end{cases}$$

Take S_{ai} as an example for illustration. If the switches T_{ai2} and T_{ai3} are conducted, the switching function S_{ai} equals to -1 and v_{abi} equals to $-v_{dci}$. If the switches T_{ai1} and T_{ai4} are conducted, the switching function S_{ai} equals to 1 and v_{abi} equals to v_{dci}. Otherwise if the switches T_{ai1} and T_{ai3} are conducted or switches T_{ai2} and T_{ai4} are conducted, the switching function S_{ai} equals to 0 and v_{abi} equals to 0. S_{mi} has the same definition with S_{ai}. However, it

is worth to point out that S_{mi} is introduced just for single-phase am-dq transformation, and it is not applied to real control since the hypothesized phase is not physically existed. Applying the Kirchhoff's law (KVL and KCL) to Figure 3-1(b), the system state-space equations are described as:

$$\begin{bmatrix} \frac{d}{dt} i_s \\ \frac{d}{dt} i_m \end{bmatrix} = \begin{pmatrix} \frac{-R_s}{L_s} & 0 \\ 0 & \frac{-R_s}{L_s} \end{pmatrix} \begin{bmatrix} i_s \\ i_m \end{bmatrix} + \begin{bmatrix} v_s \\ v_m \end{bmatrix} \frac{1}{L_s} - (\frac{v_{dc1}}{L_s} \begin{bmatrix} S_{a1} \\ S_{m1} \end{bmatrix} + \frac{v_{dc2}}{L_s} \begin{bmatrix} S_{a2} \\ S_{m2} \end{bmatrix} + \ldots + \frac{v_{dcN}}{L_s} \begin{bmatrix} S_{aN} \\ S_{mN} \end{bmatrix}) \tag{3-3}$$

$$i_s S_{ai} + i_m S_{mi} = C_i \frac{d}{dt} v_{dci} + \frac{v_{dci}}{R_i} (i = 1 \ldots N) \tag{3-4}$$

Define the average duty cycle in a switching period as shown in (3-5):

$$d_{ai} = \overline{S_{ai}}, d_{mi} = \overline{S_{mi}} (i = 1 \ldots N) \tag{3-5}$$

Average the voltage and current in a switching period, which are denoted as $\overline{v_s}$, $\overline{v_m}$, $\overline{i_s}$, $\overline{i_m}$, and $\overline{v_{dci}}$. The averaged state-space equation of the system is shown as:

$$\begin{bmatrix} \frac{d}{dt} \overline{i_s} \\ \frac{d}{dt} \overline{i_m} \end{bmatrix} = \begin{pmatrix} \frac{-R_s}{L_s} & 0 \\ 0 & \frac{-R_s}{L_s} \end{pmatrix} \begin{bmatrix} \overline{i_s} \\ \overline{i_m} \end{bmatrix} + \begin{bmatrix} \overline{v_s} \\ \overline{v_m} \end{bmatrix} \frac{1}{L_s} - (\frac{\overline{v_{dc1}}}{L_s} \begin{bmatrix} d_{a1} \\ d_{m1} \end{bmatrix} + \frac{\overline{v_{dc2}}}{L_s} \begin{bmatrix} d_{a2} \\ d_{m2} \end{bmatrix} + \ldots + \frac{\overline{v_{dcN}}}{L_s} \begin{bmatrix} d_{aN} \\ d_{mN} \end{bmatrix}) \tag{3-6}$$

$$\overline{i_s} d_{ai} + \overline{i_m} d_{mi} = C_i \frac{d}{dt} \overline{v_{dci}} + \frac{\overline{v_{dci}}}{R_i} (i = 1 \ldots N) \tag{3-7}$$

The am-dq transformation matrix is defined in (3-8) and its inverse matrix is (3-9) [106].

$$T = \begin{pmatrix} \sin\theta & -\cos\theta \\ \cos\theta & \sin\theta \end{pmatrix} \tag{3-8}$$

$$T^{-1} = \begin{pmatrix} \sin\theta & \cos\theta \\ -\cos\theta & \sin\theta \end{pmatrix} \tag{3-9}$$

where, θ is the phase information of v_s obtained from a PLL.

Substitute (3-9) into (3-6) and (3-7):

$$\frac{d}{dt}[(T^{-1})\begin{bmatrix}\overline{i_{sd}}\\ \overline{i_{sq}}\end{bmatrix}]=\begin{pmatrix}\frac{-R_s}{L_s} & 0\\ 0 & \frac{-R_s}{L_s}\end{pmatrix}T^{-1}\begin{bmatrix}\overline{i_{sd}}\\ \overline{i_{sq}}\end{bmatrix}+T^{-1}\begin{bmatrix}\overline{v_{sd}}\\ \overline{v_{sq}}\end{bmatrix}\frac{1}{L_s}-(\frac{\overline{v_{dc1}}}{L_s}T^{-1}\begin{bmatrix}d_{d1}\\ d_{q1}\end{bmatrix}+\frac{\overline{v_{dc2}}}{L_s}T^{-1}\begin{bmatrix}d_{d2}\\ d_{q2}\end{bmatrix}+...+\frac{\overline{v_{dcN}}}{L_s}T^{-1}\begin{bmatrix}d_{dN}\\ d_{qN}\end{bmatrix})$$

(3-10)

$$\begin{bmatrix}d_{ai}\\ d_{mi}\end{bmatrix}^T T^{-1}T\begin{bmatrix}\overline{i_s}\\ \overline{i_m}\end{bmatrix}=\left[T\begin{bmatrix}d_{ai}\\ d_{mi}\end{bmatrix}\right]^T T\begin{bmatrix}\overline{i_s}\\ \overline{i_m}\end{bmatrix}=C_i\frac{d}{dt}\overline{v_{dci}}+\frac{\overline{v_{dci}}}{R_i}(i=1...N) \tag{3-11}$$

Recall that the following equation is satisfied:

$$T\frac{d}{dt}(T^{-1})=\begin{pmatrix}0 & -w\\ w & 0\end{pmatrix} \tag{3-12}$$

Where, w is the angular frequency of the grid voltage.

The state-space equations of the system in d-q coordinate are then simplified as:

$$\begin{bmatrix}\frac{d}{dt}\overline{i_{sd}}\\ \frac{d}{dt}\overline{i_{sq}}\end{bmatrix}=\begin{pmatrix}\frac{-R_s}{L_s} & w\\ -w & \frac{-R_s}{L_s}\end{pmatrix}\begin{bmatrix}\overline{i_{sd}}\\ \overline{i_{sq}}\end{bmatrix}+\begin{bmatrix}\overline{v_{sd}}\\ \overline{v_{sq}}\end{bmatrix}\frac{1}{L_s}-(\frac{\overline{v_{dc1}}}{L_s}\begin{bmatrix}d_{d1}\\ d_{q1}\end{bmatrix}+\frac{\overline{v_{dc2}}}{L_s}\begin{bmatrix}d_{d2}\\ d_{q2}\end{bmatrix}+...+\frac{\overline{v_{dcN}}}{L_s}\begin{bmatrix}d_{dN}\\ d_{qN}\end{bmatrix}) \tag{3-13}$$

$$d_{di}\overline{i_{sd}}+d_{qi}\overline{i_{sq}}=C_i\frac{d\overline{v_{dci}}}{dt}+\frac{\overline{v_{dci}}}{R_i}(i=1...N) \tag{3-14}$$

If perturb the equation (3-13) and (3-14), and erase the DC steady-state value of operating point and higher order small-signal items, the averaged model above can be transferred into the small-signal model, which is depicted in Figure 3-6. This small signal model will be used to guide the controller design procedures presented in the section III-B.

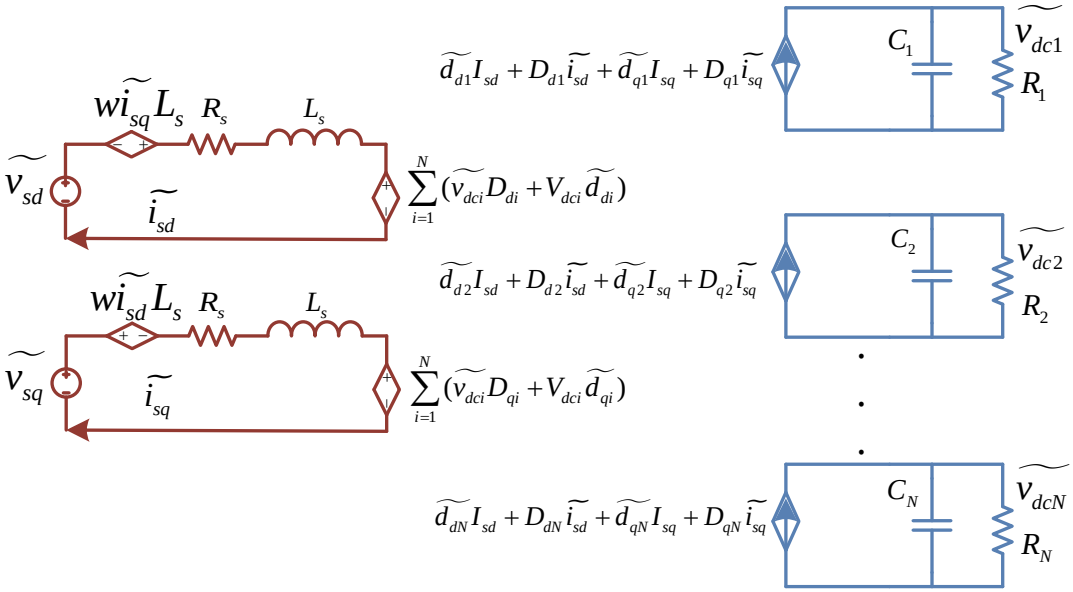


Figure 3-6 Small signal model of the system in the d-q coordinate

In the cascaded multilevel converter, the DC capacitor voltage is regulated by the active current. The reactive current is controlled to a specific value for reactive power compensators (such as in STATCOM) and zero for unity power factor operation of active rectifiers. Figure 3-7 demonstrates the dual loop controller in the d-q coordinate for a cascaded multilevel rectifier with N H-bridges. In Figure 3-7, NE is the reference of total DC voltage, V_{sbase} is the base value of the PCC voltage and is chosen to NE in the chapter, and I_{sbase} is the base value of the input current. H_{ed}, H_{id}, and H_{iq} are the controllers for DC bus voltage, active current, and reactive current respectively. The am-dq transformation is applied based on (3-6) and the phase information is obtained by applying a phase locked loop (PLL) to the single phase PCC voltage. The d-q decoupling control is derived from (3-11) and (3-12), which is similar with the classical d-q decoupling control in a three-phase system. PCC voltage feed-forward

control is also implemented so that the distortion of the grid voltage will not affect the controller since only the L-type filter is adopted in this chapter. In the DC voltage loop, a notch filter at 120 Hz is added to the feedback path to eliminate the second harmonic component in the DC capacitor voltages by assuming that the grid frequency is 60 Hz. If the controller considers the balanced condition and controls only the total DC voltage, it is called the original system controller in this chapter. If the system is unbalanced, certain modification has to be made for active component of duty cycles, which are $\Delta d_1, \Delta d_2, \ldots \Delta d_n$, as shown in dotted arrow, and these are given by an additional voltage balance controller.

The number of regulation loops for DC voltages cannot be more than that of DC links, guaranteeing no conflict among controllers. Since the total DC voltage is already regulated by the original system controller, only N-1 additional closed loop regulation can be added, and an open loop modification of duty cycle should be adopted for one of the H-bridge. If this open loop modification is not well designed, the additional voltage-balancing controller is coupled with the original system controller. The object of this chapter is to minimize the coupling effect between the original system controller and the voltage balance controller so that they can be designed separately.

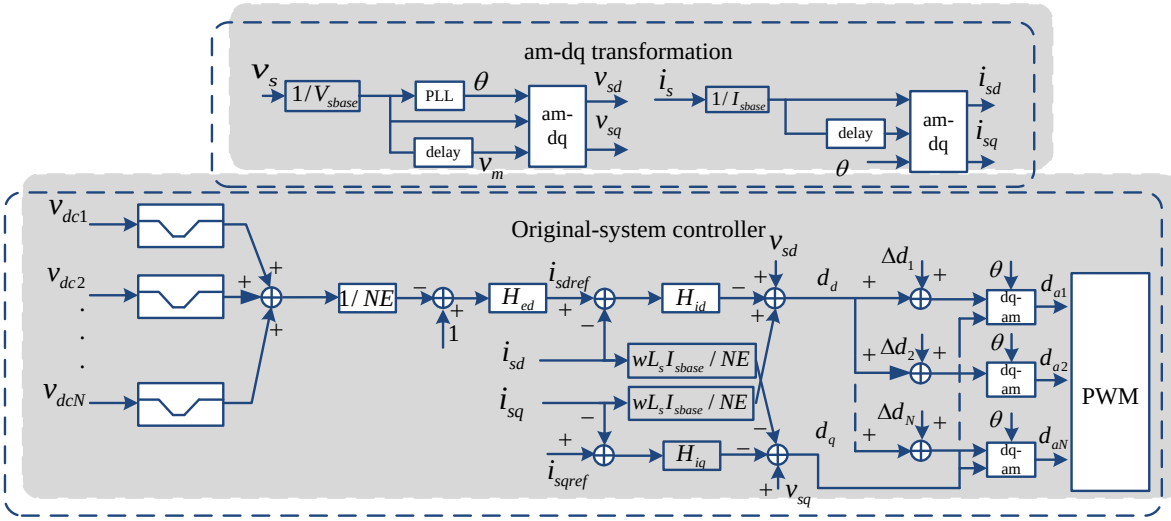


Figure 3-7 D-q coordinate controller for cascaded multilevel converter with N H-bridges

3.4 A New voltage balance controller with minimized effect to original system controller

3.4.1 Theoretical analysis

DC voltage in each capacitor may become imbalanced for many reasons including the case of different loads connected to each DC port. Although the total voltage remains controlled by the original system controller, the unequal distribution of voltage among H-bridges exists. Active power should be re-distributed among H-bridge modules in order to achieve voltage balance.

The dynamic equation for the original system controller can be described by:

$$
\begin{aligned}
L_s \frac{di_{sd}}{dt} &= -R_s i_{sd} + wL_s i_{sq} + v_{sd} - N\overline{E}d_d \\
L_s \frac{di_{sq}}{dt} &= -R_s i_{sq} - wL_s i_{sd} + v_{sq} - N\overline{E}d_q
\end{aligned}
\tag{3-15}
$$

Where, d_d and d_q are active and reactive duty cycle generated by it.

The average voltage of all DC links is assumed to be $\overline{E}$, which should be selected as the reference for the voltage balance controller as shown in (3-16). This will be explained in detail in part IV.

$$N\overline{E} = \sum_{i=1}^{N} v_{dci} \tag{3-16}$$

When DC voltages become imbalanced, voltages in DC ports are denoted as $v_{dci}(i = 1...N)$ and $d_{di}, d_{qi}(i = 1...N)$ are the modified duty cycles. The dynamic equation for the system is:

$$\begin{aligned} L_s \frac{di_{sd}}{dt} &= -R_s i_{sd} + wL_s i_{sq} + v_{sd} - \sum_{i=1}^{N} v_{dci} d_{di} \\ L_s \frac{di_{sq}}{dt} &= -R_s i_{sq} - wL_s i_{sd} + v_{sq} - \sum_{i=1}^{N} v_{dci} d_{qi} \end{aligned} \tag{3-17}$$

This can be rewritten as:

$$\begin{aligned} L_s \frac{di_{sd}}{dt} &= -R_s i_{sd} + wL_s i_{sq} + v_{sd} - N\overline{E}d_d + (N\overline{E}d_d - \sum_{i=1}^{N} v_{dci} d_{di}) \\ L_s \frac{di_{sq}}{dt} &= -R_s i_{sq} - wL_s i_{sd} + v_{sq} - N\overline{E}d_q + (N\overline{E}d_q - \sum_{i=1}^{N} v_{dci} d_{qi}) \end{aligned} \tag{3-18}$$

Comparing (3-18) with (3-15), it is clear that $(N\overline{E}d_d - \sum_{i=1}^{N} v_{dci} d_{di})$ and $(N\overline{E}d_q - \sum_{i=1}^{N} v_{dci} d_{qi})$ are the additional terms added by the voltage-balancing controller. The key strategy of the proposed method is to eliminate this additional term so that the voltage balance controller will not affect the pre-designed original system controller.

Define the coupling index as:

$$J_1 = (N\overline{E}d_d - \sum_{i=1}^{N} d_{di} v_{dci})^2 = (N\overline{E}d_d - \sum_{i=1}^{N} (d_d + \Delta d_{di})(\overline{E} - \Delta v_{dci}))^2 \tag{3-19}$$

$$J_2 = (N\overline{E}d_q - \sum_{i=1}^{N} d_{qi} v_{dci})^2 \tag{3-20}$$

Where, Δd_{di} is the modification of duty cycle and Δv_{dci} is the error between the reference and the feedback voltage for each DC link. Since the reactive duty cycles are not modified and this means $d_q = d_{qi}$. (3-20) is already zero since $\overline{E}$ is chosen as shown in (3-16). The problem of how to minimize J_1 can be achieved if equation (3-21) is satisfied.

$$\sum_{i=1}^{N} (d_d + \Delta d_{di})(\overline{E} - \Delta v_{dci}) = N\overline{E}d_d \tag{3-21}$$

Expand (3-21) further leads to:

$$\sum_{i=1}^{N} d_d \overline{E} - \sum_{i=1}^{N} d_d \Delta v_{dci} + \sum_{i=1}^{N} \Delta d_{di} \overline{E} - \sum_{i=1}^{N} \Delta d_{di} \Delta v_{dci} = N\overline{E}d_d \tag{3-22}$$

(3-22) can be simplified as:

$$\sum_{i=1}^{N} (\overline{E} - \Delta v_{dci})\Delta d_{di} = \sum_{i=1}^{N} (v_{dci})\Delta d_{di} = \sum_{i=1}^{N} \Delta v_{dci} d_d \tag{3-23}$$

Equation (3-23) describes the relationship among modifications of active duty cycles, which are marked as Δd_{di}. As presented above, an open loop modification of active duty cycle should be added for one of the H-bridges. Without losing generality, assuming that the modifications of active duty cycles for the first N-1 H-bridges are generated by PI controller, thus eliminating the difference between the feedback value and the reference value for the voltage-balancing controller.

$$\Delta d_{di} = k_{pi}(v_{dcref} - v_{dci}) + k_{ii}\int (v_{dcref} - v_{dci})(i = 1...N-1) \tag{3-24}$$

Then the open loop modification of active duty cycle in the Nth H-bridge should meet:

$$\Delta d_{dN} = \frac{\sum_{i=1}^{N} \Delta v_{dci} d_d - \sum_{i=1}^{N-1} v_{dci} \Delta d_{di}}{v_{dcN}} \tag{3-25}$$

to eliminate the coupling effect.

The proposed voltage-balancing controller is shown in Figure 3-8, where $H_{edci}(i = 1...N-1)$ are PI controllers for the first N-1 H-bridges, and Δd_{dN} is obtained from (3-25). It should be noted that (3-25) provides the fundamental relationship among modification values of active duty cycles for all H-bridges, which is especially important and differs from previous methods especially when DC capacitor voltages are not exactly the same.

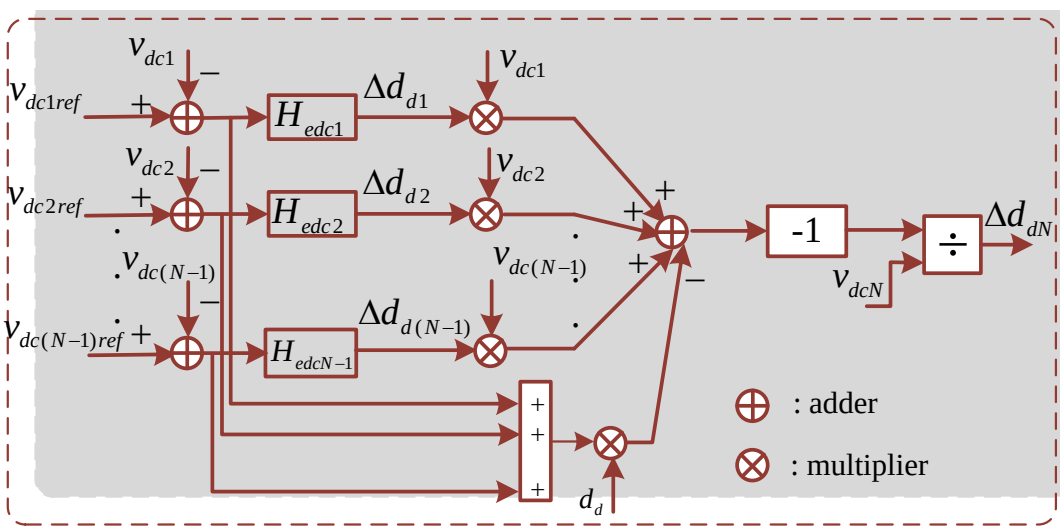


Figure 3-8 Proposed voltage balance controller for cascaded multilevel converter

3.4.2 Discussion on controller design procedure and effective voltage balance area

The proposed control system contains an original system controller and N-1 closed-loop voltage balance controllers. The design of such a system follows certain procedures. The

original system controller is initially designed by assuming that no voltage imbalance exists, and this is reasonable since the coupling effect is eliminated. The design of this controller is similar with the traditional dual loop control system [94]. The key open loop transfer functions of the system can be derived according to the small-signal model shown in Figure 3-6.

(1) Control-to-output current transfer functions G_{i_{sd},d_d} and G_{i_{sq},d_q}

Because of the d-q decoupled controller presented in the chapter, cross-coupling between current regulation loop of d-axis and q-axis is eliminated, thus the control-to-output current transfer functions are:

$$G_{i_{sd},d_d} = \frac{\widetilde{i_{sd}}}{\widetilde{d_d}} = \frac{N\overline{E}}{SL_s + R_s} \tag{3-26}$$

$$G_{i_{sq},d_q} = \frac{\widetilde{i_{sq}}}{\widetilde{d_q}} = \frac{N\overline{E}}{SL_s + R_s} \tag{3-27}$$

(2) Current-to-output voltage transfer functions $G_{vdci,i_{sd}}$, $G_{vdci,d_{di}}$

Since $\widetilde{d_q}$ responds to the generated reactive power and the DC capacitors will be charged and discharged within a half cycle, the contributions of this charge and discharge are cancelled. Therefore, $\widetilde{d_q}$ does not affect the average value of DC capacitor voltage in a half cycle. Similarly, $\widetilde{i_{sq}}$ does not influence the average value of the DC capacitor voltage in a half cycle either. Therefore, only the transfer function from $\widetilde{v_{dci}}$ to $\widetilde{d_d}$ and the transfer function from $\widetilde{v_{dci}}$ to $\widetilde{i_{sd}}$ are under consideration.

$$G_{v_{dci},i_{sd}} = \frac{\widetilde{v_{dci}}}{\widetilde{i_{sd}}} = \frac{D_d R_i}{R_i C_i s + 1} (i = 1, 2..., N) \tag{3-28}$$

$$G_{v_{dci},d_d} = \frac{\widetilde{v_{dci}}}{\widetilde{d_d}} = \frac{I_{sd}R_i}{R_iC_is+1}(i=1,2...,N) \tag{3-29}$$

In addition, the effect of the digital delay is also taken into account in this chapter and it is represented by:

$$G_D = \frac{1-sT_D/2}{1+sT_D/2} \tag{3-30}$$

Where, T_D is the switching period of the system.

The overall small signal model of the original controller is shown in Figure 3-9. Since the inductor current dynamics are faster than the capacitor voltage dynamics, the current regulation loop and voltage regulation loop can be designed separately based on the time scale separation principle [19].

The loop gains for d and q current channel are expressed as:

$$T_{l,i_{sd}} = \frac{1}{NE}H_{id}G_DG_{i_{sd},d_d} \tag{3-31}$$

$$T_{l,i_{sq}} = \frac{1}{NE}H_{iq}G_DG_{i_{sq},d_q} \tag{3-32}$$

The controller should be designed such that enough phase margin is obtained for both $T_{l,i_{sd}}$ and $T_{l,i_{sq}}$, and thus the stable and robust operation of the system are guaranteed. In addition, considering the d-q decoupled control strategy adopted in the chapter, the current dynamics can be totally decoupled into two linear systems, and as such the conventional PI control method can be applied.

The loop gain for DC voltage channel is shown in (3-33), which can be used for DC loop regulator design.

$$T_E = \frac{1}{NE} H_{ed} G_{f,E} \frac{T_{l,isd}}{1+T_{l,isd}} \sum_{i=1}^{N} \left(\frac{G_{v_{dci},d_d}}{G_{i_{sd},d_d}} + G_{v_{dci},i_{sd}} \right) \tag{3-33}$$

Where, $G_{f,E}$ stands for the notch filter in the DC voltage feedback loop. An optimized compensator design can obtain enough phase margin of the control loop, which in turn guarantees the stability of the original system controller.

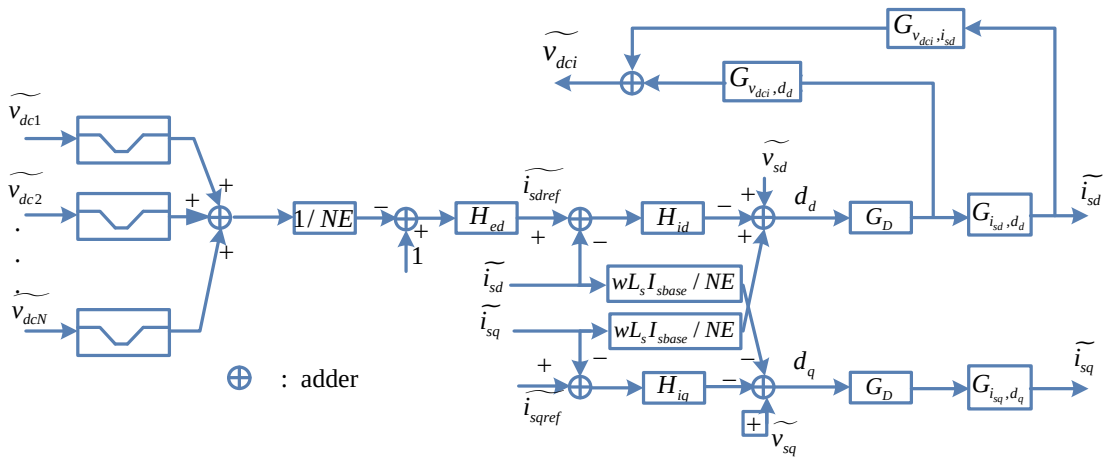


Figure 3-9 Small-signal representation of the original-system controller

The output of voltage balance controller is added to the original system controller to modify the active duty cycle for each H-bridge. Since the original system controller is designed with certain phase margin, the addition of a voltage balance controller will not lead to instability. However due to the limitations of the modulation index, the allowed active power difference among H-bridges is limited. The effective voltage-balancing area should be pre-defined. The voltage-balancing constraint can be derived as shown below [78]. According to the circuit shown in Figure 3-4:

$$\sum_{i=1}^{N} V_{abi} = V_s - jwL_s I_s \tag{3-34}$$

$$V_{abi} = (d_{di} + d_{qi} j)\overline{E}(i = 1...N) \tag{3-35}$$

Substitute (3-35) into (3-34) and rearrange the terms:

$$\sum_{i=1}^{N} d_{di} = \frac{V_s}{\overline{E}} \tag{3-36}$$

$$\sum_{i=1}^{N} d_{qi} = \frac{-wL_s I_s}{\overline{E}} \tag{3-37}$$

The active power of each H-bridge is calculated as

$$P_i = I_s d_{di} \overline{E} = \frac{P_{in}}{V_s} d_{di} \overline{E}(i = 1...N) \tag{3-38}$$

When loads connected to DC ports are different, the active power consumed by them is different. Without losing generality, assume that $d_{d1} \geq d_{d2} \geq ... \geq d_{dN}$. For each H-bridge, the operation is limited by the modulation index:

$$d_{di}^2 + d_{qi}^2 \leq 1(i = 1...N) \tag{3-39}$$

Substitute (3-38) into (3-39) and assume that the reactive power is equally distributed among H-bridges, the following constraints for active power distribution is obtained:

$$\frac{P_1}{\sum_{i=1}^{N} P_i} \leq \frac{E}{V_s}\sqrt{1 - (\frac{wL_s I_s}{N\overline{E}})^2} \tag{3-40}$$

As shown in (3-40), the voltage balance operation of the system is limited by its active power distribution. Equation (3-40) is a good estimation of the power difference allowed for the designed system.

Finally, the N-1 DC voltage-balancing controllers are designed within the preset PI output limitation according to the real operating conditions. The detailed PI parameter design and tuning process is the same as the standard two-level converter system, and therefore is not detailed here.

3.4.3 Comparison of proposed methods with previous methods

In order to compare the proposed method with the previous methods proposed in [88], [95], [91], [98], [78], all of which try to balance the DC bus voltage in the d-q coordinate. The expressions for modification of equivalent active duty cycle in these studies are analyzed below.

(1) Method proposed in [94]

This method is based on the per-phase modification concept, and the modifications of duty cycles are defined as

$$\Delta d_{di} = k_{pi}(v_{dcref} - v_{dci}) + k_{ii}\int(v_{dcref} - v_{dci})(i = 1...N) \tag{3-41}$$

This method may not be theoretically suitable since it has a total of N+1 voltage loops to control N DC voltages and thus may cause oscillation in the system.

(2) Method proposed in [97]

This method is the same as the one used in [91], shown as:

$$\begin{aligned} k_i &= k_{pi}(v_{dcref} - v_{dci}) + k_{ii}\int(v_{dcref} - v_{dci})(i = 1...N) \\ d_{di} &= d_d \frac{k_i}{\sum_{i=1}^{N} k_i} \end{aligned} \tag{3-42}$$

The idea is to distribute the duty cycle to each H-bridge so that the total power transferred is guaranteed. The relationships among modifications of duty cycles are satisfied as shown in

$$\sum_{i=1}^{N} \Delta d_{di} = 0 \tag{3-43}$$

(3) Method proposed in [78]

This method is actually the same with method in[97] , illustrated as:

$$\begin{aligned} \Delta d_{di} &= k_{pi}(v_{dcref} - v_{dci}) + k_{ii}\int (v_{dcref} - v_{dci})(i = 1...N-1) \\ \Delta d_{dN} &= -\sum_{i=1}^{N-1} \Delta d_{di} \end{aligned} \tag{3-44}$$

The summation of the duty cycle modification is equal to zero, shown as

$$\sum_{i=1}^{N} \Delta d_{di} = 0 \tag{3-45}$$

(4) Method proposed in [95] [98]

These two methods align the modification of the duty cycle to the direction of the current, and therefore only modify the active power component. Based on the physical meaning of the method, the equivalent duty cycle modification for the last H-bridge is:

$$\Delta d_{dN} = \frac{-\sum_{i=1}^{N-1} v_{dci} \Delta d_{di}}{v_{dcN}} \tag{3-46}$$

The difference between the proposed method and previous methods is that the proposed method can eliminate the coupling effect in both steady and dynamic state operations. However, the methods in [88], [95], [91], [98], [78] can only eliminate the coupling effect when in the steady state operation. This can be understood by assuming that the system has operated in a steady state after load disturbance, meaning that the DC bus voltages have

converged to the same value ($v_{dc1} = v_{dc2} = ... = v_{dcN}$) and the total DC bus voltage has regulated back to the reference value ($\Delta v_{dci} = 0$), the expression in (3-25) is equivalent to those in (3-43), (3-45) and (3-46). In some applications, such as when the cascaded converter is operating as a rectifier with load on each DC port, power in each DC port always changes. Therefore, the DC bus voltage is always in a dynamic state. During these dynamic responses, the DC voltages maybe unbalanced. In this situation, the addition of the voltage-balancing controller proposed in [91], [78],[94], [97] will affect the dynamics of the original system controller. Therefore, the method proposed in the chapter provides the generalized express that achieves the decoupling for all the operation conditions.

For the purpose of comparing the performance of different methods, the coupling index $(N\overline{E}d_d - \sum_{i=1}^{N} v_{dci} d_{di})^2$ is taken as the criterion. It is clear that the lower the coupling index is, the better the performance is.

Table 3-1 System parameters

Parameters	Value
Source Voltage	80V RMS
Source frequency	60Hz
DC link voltage	150V (50V each)
Switching frequency	1080 Hz
Input inductance	50 mH
DC link capacitor	200 uF
DC load resistor	250 Ω

The simulation is conducted and comparison is made between the proposed method and the method in [91], [78],[94], [97]. In the simulation, three H-bridges are cascaded to a seven-level converter. The system parameters are shown in Table 3-1.

Figure 3-10 demonstrates the value of coupling index $(N\overline{E}d_d - \sum_{i=1}^{N} v_{dci} d_{di})^2$ for both cases when there is a voltage imbalance caused by the load change at t= $2\,S$. In this scenario, the load connected to the third H-bridge is changed from 250 Ω to 500 Ω. The dotted line is the coupling index adopting the proposed method, and the solid one is the index adopting the method equivalent to the one proposed in this chapter. One can see that before the load disturbance, the coupling index for both cases approximates zero, demonstrating the coupling effect elimination for both methods in the steady state operation. Unlike the proposed method, in which the coupling index is still zero when voltage becomes imbalanced, the coupling index using the methods proposed in [91], [78],[94], [97] grows when imbalance occurs and decreases as the voltage becomes balanced. Clearly, the previously proposed methods will bring an additional term to the original system dynamics when the voltages are imbalanced (dynamic operation condition), and it is eliminated by the proposed method. One should also notice that the coupling interaction worsens when the voltage imbalance is significant. The wider the range of load changes, the larger the effect of the additional term to the original system dynamics becomes. Noting that the effect of the coupling item to the original system controller is unpredictable, and will bring unexpected change of the original system control loop, thus it is undesirable. The proposed controller can eliminate this effect

such that the two controllers can be designed separately in order to achieve the desired performance.

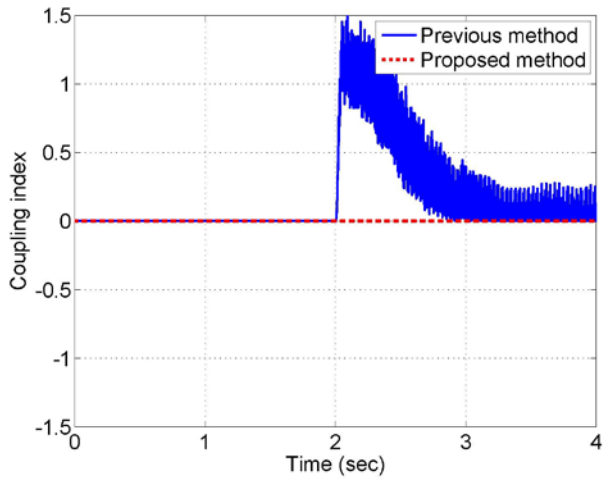
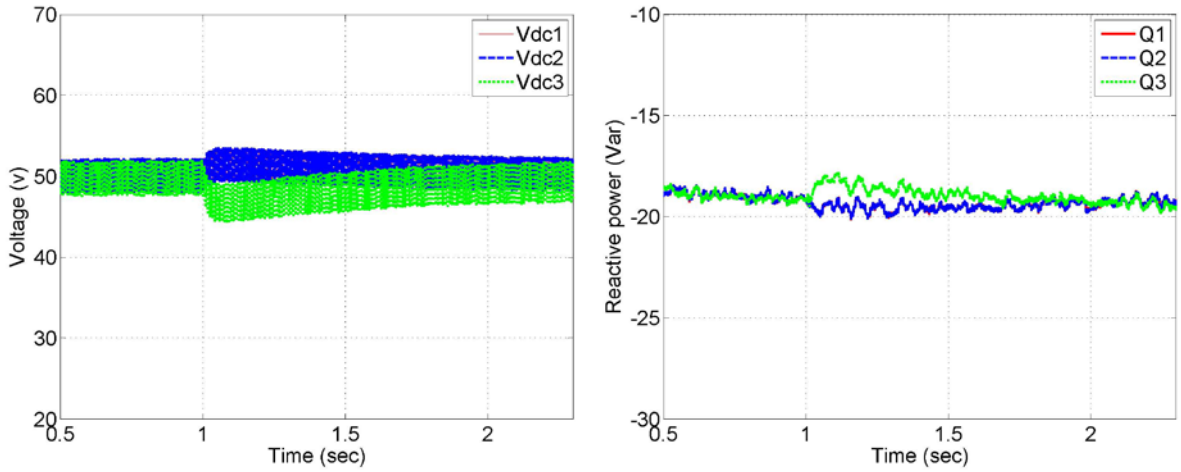


Figure 3-10 Comparison of $(NEd_d - \sum_{i=1}^{N} v_{dci} d_{di})^2$ between proposed method and previous methods

3.4.4 Potential of reactive power balance among H-bridges

As discussed in 3.4 of the chapter, the proposed method also has the potential advantage of balancing reactive power among H-bridges. This can be achieved if an independent modulation strategy is adopted for each H-bridge [95]. In order to verify the same function of proposed method with the methods proposed in [95], simulation studies are also conducted. The modulation strategy adopted in each H-bridge is the unipolar sinusoidal pulse width modulation (SPWM) without phase shifts among them and with the switching frequency set to 3 KHz so that the same passive components can be used. The reactive current reference is set to 0.2, which stands for sending reactive power from grid to converter, with a base value

of 3 A. The load in the third H-bridge is changed from 250 Ω to 200 Ω at t=1 s and the results are depicted in Figure 3-11. As can be seen from Figure 3-11 (a), the proposed voltage-balancing controller can effectively balance the DC bus voltage in a short time. From Figure 3-11 (b), when DC voltages are balanced, although the active power is unbalanced among H-bridges due to different DC loads, the reactive power is still balanced. The results are the same as shown in [95], thus verifying the equal reactive power distribution capability of the proposed method.



(a) DC voltage balance (b) Reactive power balance

Figure 3-11 DC voltage and reactive power balance among H-bridges

3.4.5 Experimental results

The validity of the proposed method is verified experimentally in a seven-level active rectifier cascaded by three H-bridges. The system parameters are shown in Table 3-1. A scaled version of SST prototype is developed in the lab shown in Figure 3-12. It composes of

three modules, in which the single-phase two-level rectifier, DAB, and single phase inverter is designed. Three modules can be connected to compose the studied SST topology. We use the rectifier stage of the prototype to verify the proposed control algorithm. The device adopted is the INFINEON 20N60CFD power MOSFET. Two 25 mH inductors (ferrite core with air gap) are connected in series to compose the desired 50 mH input filter inductor. Since the experiments are carried out in a low frequency and very low current situation, the input inductance is chosen to be relatively large. However, this will not affect the performance evaluation. Two 100 μF, 200 V capacitors produced by Nichicon are paralleled in each DC output. The controller is realized by using the TI TMS320F 28335 DSP. In the experiments, the input AC voltage is generated from digital AC power supply and three variable resistance load banks are used as the loads. Although some other factors mentioned in part I may also affects the voltage balance, only the voltage imbalance brought by the different load is considered since it can emulate a wide range of voltage imbalance for better verification. Of course, the proposed method can balance the voltage caused by all the possible reasons mentioned in the part I.

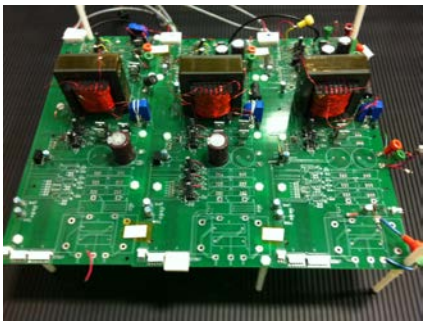
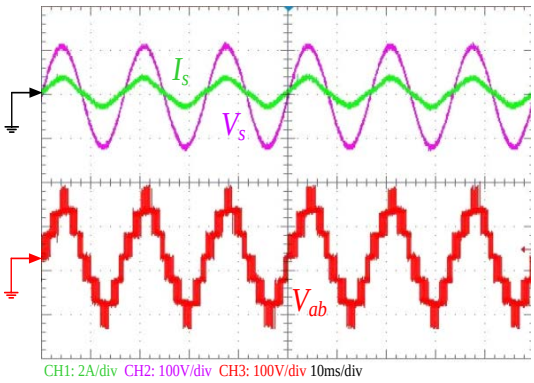


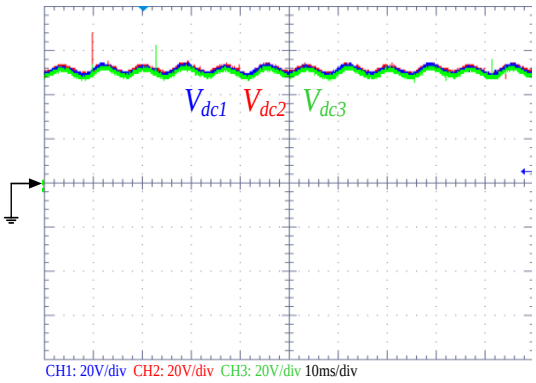
Figure 3-12 Hardware setup for experiments: A scaled down SST prototype

Figure 3-13 shows the experimental results of the proposed method and is explained as follows. Figure 3-13 (a) shows the waveforms of AC voltage, PWM voltage, and AC current when identical 250 Ω loads are connected to all three DC links. Since the converter is cascaded by three H-bridges under the phase shifted pulse width modulation (PS-PWM) [30], it generates a seven-level PWM voltage. The input current is in phase with the input voltage, indicating a unity power factor operation. Figure 3-13 (b) shows the balanced DC voltages, which are all controlled to 50 V in this operating condition.

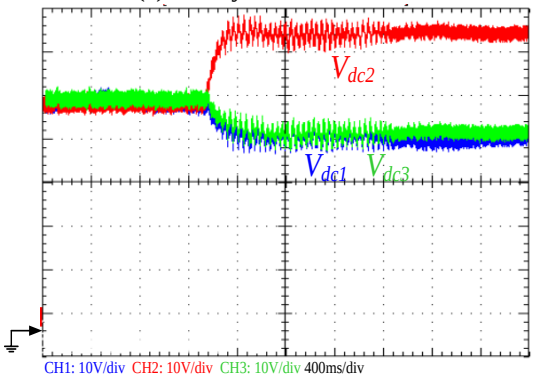
In order to verify the effectiveness of the proposed voltage-balancing controller, the comparison is made between the dynamic response of DC voltages without the voltage-balancing controller and with the voltage balance controller when load R_2 changes from 250 Ω to 400Ω. Figure 3-13 (c) shows the DC voltages without the voltage balance controller. The voltage values diverge because of the load difference (V_{dc2} increases, V_{dc1} and V_{dc3} decrease). In the Figure 3-13 (d), the DC voltages converge to 50V rapidly with the aid of the proposed voltage balance controller. This evidences the effectiveness of the proposed voltage balance controller.



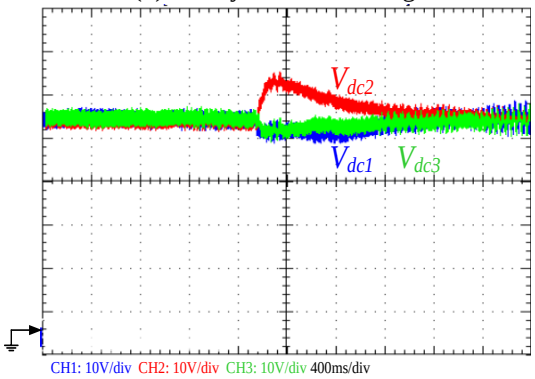
(a) Steady state AC waveforms



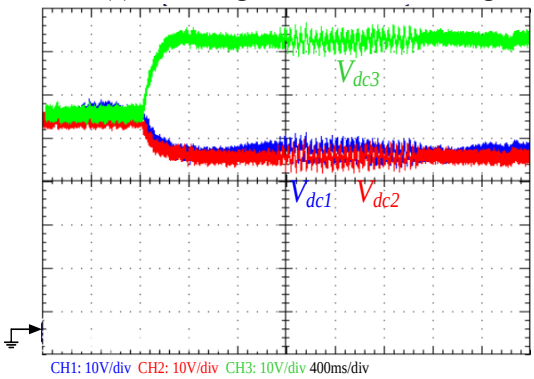
(b) Steady state DC voltages



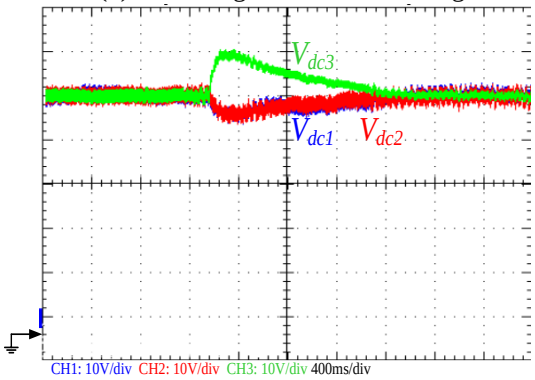
(c) DC voltage imbalance in H-bridge 2



(d) DC voltage balance in H-bridge 2



(e) DC voltage imbalance in H-bridge 3



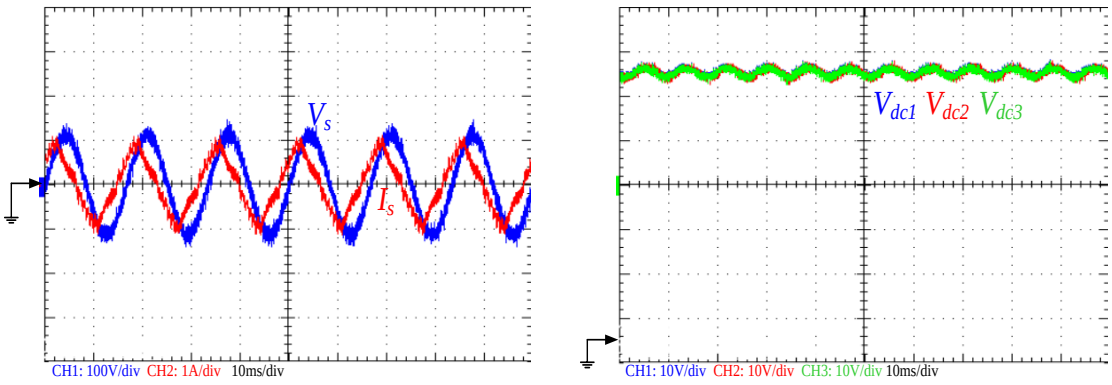
(f) DC voltage balance in H-bridge 3

Figure 3-13 Experimental results of cascaded seven-level converter

Considering that the modification mechanism of the duty cycle for the third H-bridge is different from the first and the second H-bridge because of the open loop modification manner, a test is also conducted by changing the load in the third H-bridge from 250 Ω to 400 Ω. In Figure 3-13 (e), three DC voltages diverge without the voltage balance controller. V_{dc3} becomes higher than 50 V and V_{dc1}, V_{dc2} becomes lower than 50 V. While in Figure 3-13 (f), the voltages converge to 50 V immediately after the loads change due to the effectiveness of the proposed voltage balance controller.

It can be concluded from Figure 3-13 that the proposed voltage balance controller can effectively balance the DC voltage for all H-bridges.

A similar experiment is also carried out as presented in [95] in order to verify the equal distribution of reactive power with different DC loads. In this experiment, the system operates in a capacitive mode thus reactive power exists in the system, as shown in Figure 3-14 (a). The DC load connected to the third H-bridge is set to 220 Ω, which is different from the first two H-bridges, thus the active power is different among H-bridges. As can be seen from Figure 3-14 (b), by using the proposed controller with an individual SPWM for each H-bridge, the DC ripple voltages are exactly the same for all three H-bridges. This means the reactive power distribution should also be the same since the DC ripple voltage is proportional to the reactive power exchanged within the circuit [95]. The conclusion matches well with the one presented in [95], thus verifying the potential of equal reactive power distribution capability.



(a) Input voltage and current (b) DC ripple voltage balance

Figure 3-14 Reactive power balance under unbalanced load condition

3.5 Investigation of reference generation techniques of voltage-balancing controller

In part III, the relationship among modification of duty cycles of H-bridges is analyzed. Another important, yet easily ignored problem is how to design the reference generation for the voltage-balancing controller. In earlier literatures, the evaluation of the voltage-balancing controller in soft start-up process is rare. In previous PI-based control algorithms, the reference of the voltage balance controller is not mentioned [86], [91], [95], [96] or is given by a fixed value that is equal to the steady state value [89],[90],[94],[78].The authors in [76] adopt the average value of DC voltages as the reference without giving any explanation. This part analyzes the effect of the reference generation techniques to the start-up process and answers the question why average value should be chosen as the reference for voltage-balancing controller.

In industrial applications, a soft start-up process is required especially for a high power and high voltage converter, in which huge inrush current may damage the power semiconductor devices. Figure 3-15 shows the typical DC bus voltage of a rectifier using a soft start algorithm. The system is first charged through a resistor connected between PCC and the cascaded H-bridges in order to avoid a large inrush current. The resistor is then bypassed and a diode charge is performed to charge the DC capacitor voltage. When the diode charge is finished, a ramp current charge with only the current loop regulation is used to further charge the DC capacitor voltage and approach the rated value. Finally, the DC outer loop is closed to perform the steady state regulation.

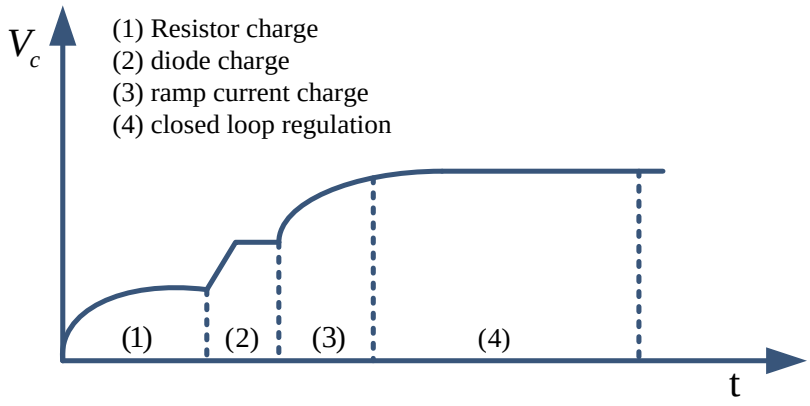


Figure 3-15 Soft-start algorithm of rectifier

It is understood that when the system works under the soft-start process, the total DC capacitor voltage is below the desired value. If the reference for the voltage balance controller remains constant, even if the voltages are balanced, there will still be a

modification value generated by the voltage balance controller, which may lead to an undesired DC bus regulation performance. In order to eliminate this phenomenon, this chapter recommends the use of the average DC bus voltages of all H-bridges as the reference for the DC voltage-balancing controller. By adopting this method, the DC capacitor voltage will be balanced during the start-up process since the reference is changing with the actual DC bus voltage, then the effect of the voltage-balancing controller to the original system controller will be further minimized and the two controllers are completely decoupled. Based on the above discussion, the entire control system is shown in Figure 3-16, where the am-dq transformation is based on (6), the dual loop controller is based on (11) and (12), and the voltage balance controller is based on (23). The entire system controller is separated into two layers. The upper layer is the original system controller and the lower layer is the voltage-balancing controller.

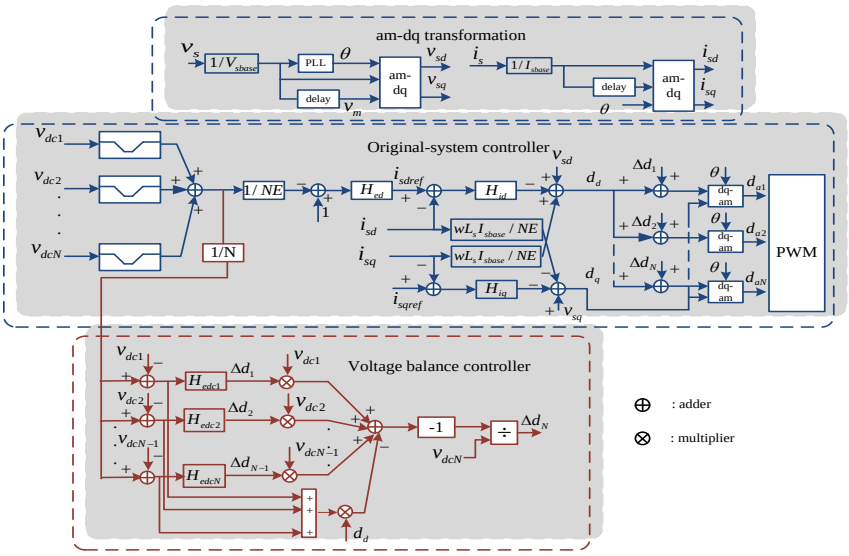
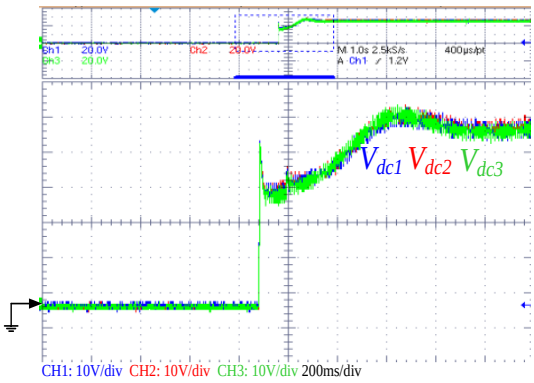
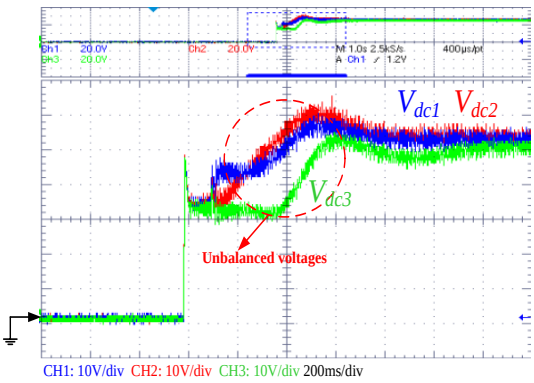


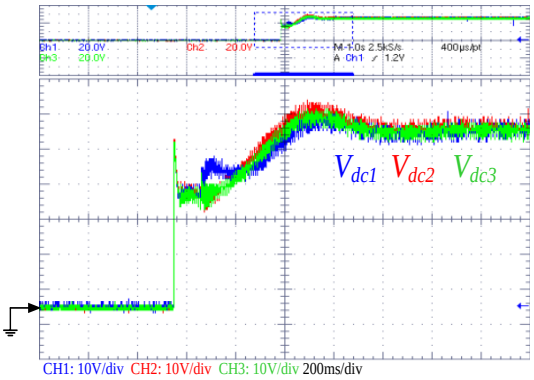
Figure 3-16 Control diagram of cascaded rectifier under d-q coordinate



(a) Without voltage-balancing controller



(b) With traditional voltage reference generation



(c) With presented voltage reference generation

Figure 3-17 Comparison of different voltage reference for balance controller

In order to compare the performance of the presented reference generation method with traditional ones in [89],[90],[94],[78], a soft-start performance is evaluated for three cases under balanced load condition, and the waveforms are given in Figure 3-17. Figure 3-17 (a) shows the DC voltages in a soft-start process without the voltage balance controller. Since the system is balanced naturally, the voltages are balanced for both start-up and steady state operation. Figure 3-17 (b) shows the soft-start with the voltage balance controller by using a fixed reference. Although the voltages are balanced in steady state, an imbalance is observed

in the start-up process, as shown within the dotted circle. As previously noted, this is because the voltage-balancing controller will always see a tracking error in the start-up process and try to regulate it if a fixed reference is adopted. V_{dc1} and V_{dc2} tracks the 50 V fixed reference while the total DC voltage is less than 150 V during the start-up, thus makes the V_{dc3} quite low in this period. Figure 3-17 (c) shows the soft-start with the proposed voltage-balancing controller, in which the reference is equal to the averaging of the DC capacitor voltages. The voltages will remain balanced and equal to 1/3 of the total DC voltages, and this indicates that this method has no effect to the original control system even during the start-up process.

In conclusion, the fixed reference for the voltage-balancing controller will bring voltage imbalance during the start-up process, as shown in Figure 3-17 (b), while a dynamic reference can solve this problem, as shown in Figure 3-17 (c). One should also notice that the imbalance may be also observed in the dynamic response even when total DC voltage is not well regulated. The average of the DC voltages should be chosen as the reference so that the voltage-balancing controller will only see the imbalance among DC outputs without considering the total DC voltage.

3.6 Conclusion

Previous papers designed the voltage balance controller without considering its coupling effect on the original system controller comprehensively. This chapter has investigated this problem in detail. Two important factors, namely the modification of duty cycle and reference generation for voltage balance controller, are investigated. This chapter proposes

an effective voltage balance controller that not only balances the DC voltages, but also minimizes the coupling effect. Theoretical analysis, simulation verification, and experimental demonstration are provided. It is recommended to design the voltage balance controller to achieve minimal effect on the original system controller so that the system dynamics will be maintained in both the steady and dynamic state responses.

Chapter 4 A Novel Modulation Strategy with Ultra-fast Voltage Balance Response for Cascaded Multilevel Rectifier Stage

4.1 Introduction

In the chapter 3, the voltage balance controller based on feedback regulation loop is analyzed and a new control strategy is proposed. The cascaded multilevel rectifier faces more challenge in DC voltage balance control compared with inverter application since it has larger power difference range due to load change. Under this situation, parameters tuning for PI controller is relatively complex since comprise has to be made between fast regulation and PI saturation. This becomes especially obvious with which has a modulation index. On one hand, fast regulation is expected to balance the voltage in a short time. On the other hand, PI saturation of voltage balance controller should be considered especially when one H-bridge operates with light load. All these reasons motivate to a new voltage balance scheme with good voltage balance capability, which means fast and accurate response in presented SST application. In other multilevel topologies, such as NPC multilevel converter, space vector modulation with optimum switching selection has been widely used in voltage balancing controller design [101]. This idea has been adopted in this chapter to design the voltage balance strategy for cascaded multilevel converters[15].

Basically, the efforts in this chapter is trying to find an alternative modulation based solution for cascaded multilevel converter so that the voltage balance range is equal to PI based solution while the complex PI tuning process can be avoided.

In [83], [85], a two-dimensional description for cascaded five-level converter is proposed and the same concept can be extended to cascaded multilevel converter. It gives an illustration of the cascaded multilevel converter by using multi-dimensional representation. However, the voltage balancing issue is still addressed by additional PI controller, which incurs the same problem with traditional PI based method. Based on the concept proposed in [83], [85], a modulation technique with additional voltage balance capability is proposed in this chapter for SST application. Specifically, this chapter applies the three-dimensional (3D) space modulation strategy to the cascaded seven-level rectifier in a three stage SST topology. By further analyzing the operation area of the system and utilizing the most suitable switching pairs for each H-bridge according to the operation condition, this method has the same voltage balance range with PI based solution and can balance the DC voltages under any power factor in a short time[15].

4.2 3-D space modulation technique for cascaded seven-level converter

In the diagram of FREEDM systems, a single phase SST is connected to a 12.45kV distribution system (7.2kV phase voltage). By using the 6.5 kV Si IGBT, a cascaded seven-level rectifier based three-stage SST topology can be adopted shown in Figure 4-1.

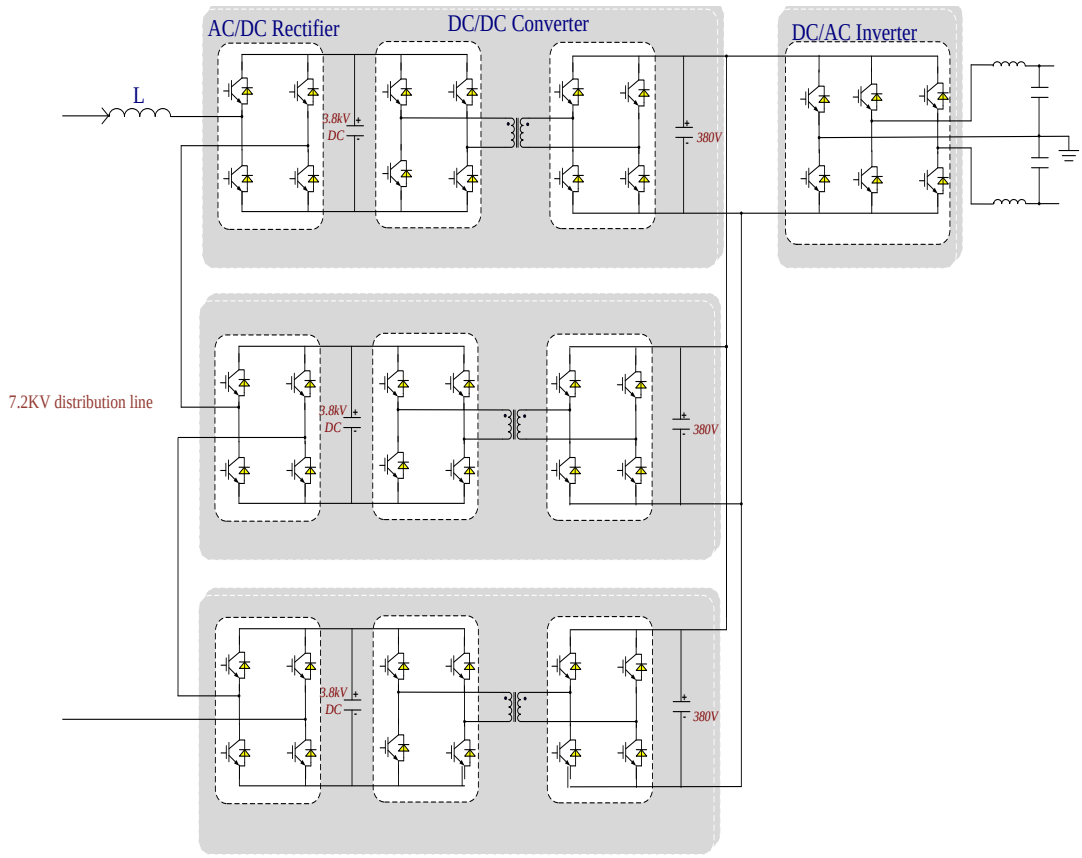


Figure 4-1 Topology of presented SST topology used in 12kV distribution line with 6.5 kV Si IGBT

4.2.1 3-D space description for cascaded seven-level converter

Figure 4-2 shows the cascaded seven-level rectifier in the presented SST topology. v_s is the point of common coupling (PCC) voltage, i_s is the input current absorbed from the grid, $v_{hi}\,(i=1,2,3)$ are the PWM voltages of three H-bridges, and $v_{dci}\,(i=1,2,3)$ are three DC voltages. L_s is the boost inductor, R_s is the equivalent resistor for inductor, wire and switch conduction

loss, $C_i(i=1,2,3)$ and $R_i(i=1,2,3)$ are the DC capacitor and load respectively. $S_{ij}(i=1,2,3;\ j=1,2,3,4)$ stands for switches in each H-bridge.

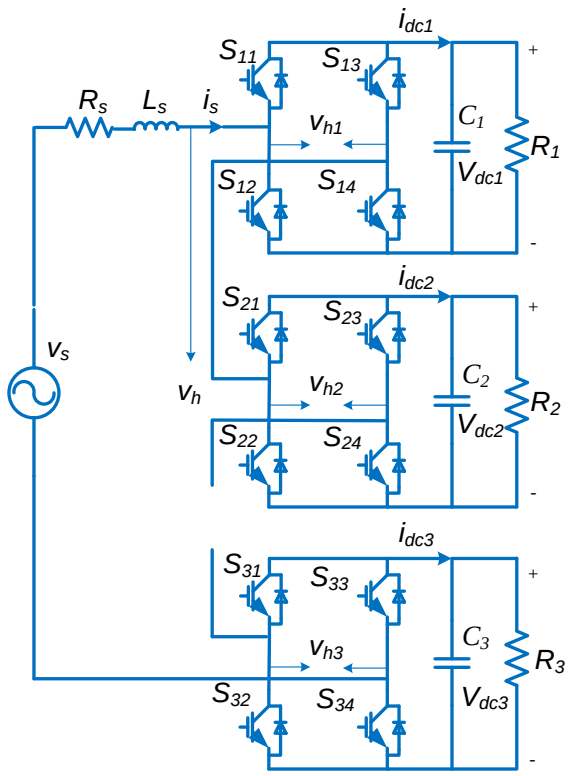


Figure 4-2 Cascaded seven-level converter

Define the switching function as follow:

$$F_i = \begin{cases} -1, S_{i2}, S_{i3} ON \\ 0, S_{i1}, S_{i3} ON; or S_{i2}, S_{i4} ON\ (i=1,2,3) \\ 1, S_{i1}, S_{i4} ON \end{cases} \tag{4-1}$$

Considering about the switching pair (F_1, F_2, F_3), there are altogether 27 possible combinations for cascaded seven-level converter. The switching pair indicates that it is

possible to establish a three-dimensional space description of the system, as shown in Figure 4-3. All switching pairs are located in three-dimensional space to form a cubic. The cascaded multilevel converter can have different ways to generate the desired PWM voltage since it is the sum of PWM voltage of all cascaded H-bridges, and each H-bridge has its own individual modulation process. For cascaded seven-level converter, the total PWM voltage is the sum of three PWM voltages generated by three H-bridges, as illustrated below. Assuming:

$$v_{ab} = (v_{h1} + v_{h2} + v_{h3}) / E = 3a \tag{4-2}$$

, where E is the desired DC voltage for each H-bridge.

Geometrically, it composes a plane that intersects each axis with intercept of $3a$. Two possible operation planes are depicted. One stands for the situation $v_{ab} > 0$ and the other one stands for the situation $v_{ab} < 0$, as shown in Figure 4-3. Take $v_{ab} > 0$ as example, if the DC voltages are balanced, the system will operate at (a, a, a), which is the center of the gravity. Otherwise, the system may operate in other point of the plane described by (4-2) according to the operating conditions, which will be analyzed below.

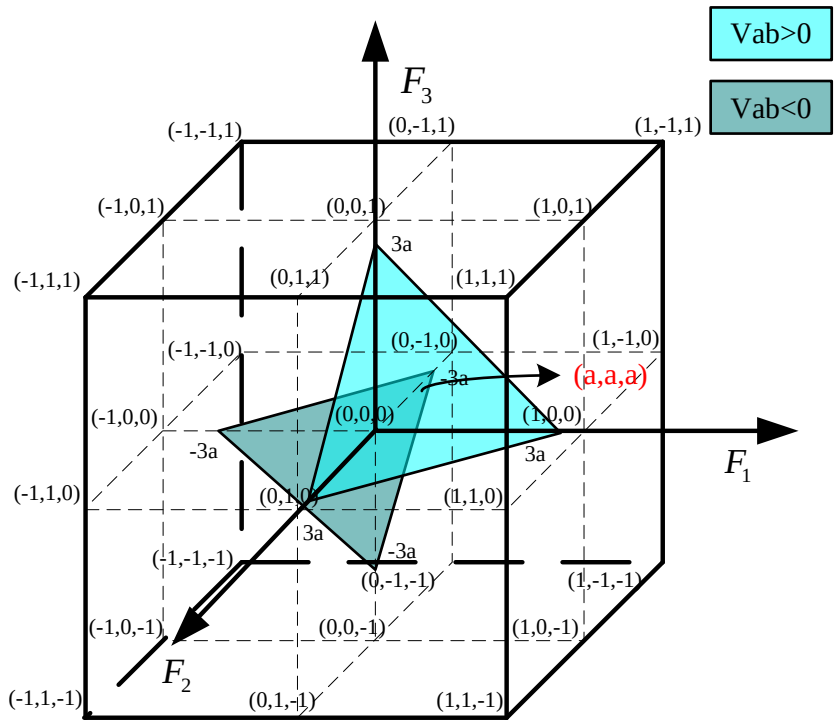


Figure 4-3 Three-dimensional control region of cascaded 7-level converter and operation plane

In order to analyze and illustrate the possible operation areas under different situations, take the situation $v_{ab} > 0$ as an example. Assuming the average value of three DC bus voltages is σ, take the operation triangle out as shown in Figure 4-4. The plane is divided into twelve sections if we consider the trend of DC voltages relates to their average voltage. For example, if the system is operating in section 1 or 2, v_{dc1}, v_{dc3} will increase and v_{dc2} will decrease. The difference is that it has the relationship $v_{dc1} \geq v_{dc3} \geq \sigma \geq v_{dc2}$ in section 1. While in section 2, it has the relationship that $v_{dc3} \geq v_{dc1} \geq \sigma \geq v_{dc2}$. Based on the similar analysis and classification methodology, the trends of all 12 sections are summarized as shown in table II. According to the operation situation of the cascaded converter, specifically, the DC voltages

of each output, the system will change its operation point from (a,a,a) to different areas described by Table 4-1. The situation that $v_{ab} < 0$ can be analyzed similarly and it is not repeated in this chapter.

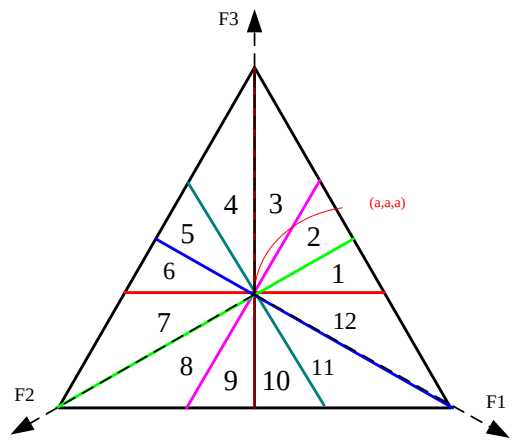


Figure 4-4 Possible operation areas when v_{ab} is positive

Table 4-1 Trend of DC voltages in each area when $v_{ab} > 0$

Operating situation	Operation area
$v_{dc1} \geq v_{dc3} \geq \sigma \geq v_{dc2}$	1
$v_{dc3} \geq v_{dc1} \geq \sigma \geq v_{dc2}$	2
$v_{dc3} \geq \sigma \geq v_{dc1} \geq v_{dc2}$	3
$v_{dc3} \geq \sigma \geq v_{dc2} \geq v_{dc1}$	4
$v_{dc3} \geq v_{dc2} \geq \sigma \geq v_{dc1}$	5
$v_{dc2} \geq v_{dc3} \geq \sigma \geq v_{dc1}$	6
$v_{dc2} \geq \sigma \geq v_{dc3} \geq v_{dc1}$	7
$v_{dc2} \geq \sigma \geq v_{dc1} \geq v_{dc3}$	8
$v_{dc2} \geq v_{dc1} \geq \sigma \geq v_{dc3}$	9
$v_{dc1} \geq v_{dc2} \geq \sigma \geq v_{dc3}$	10
$v_{dc1} \geq \sigma \geq v_{dc2} \geq v_{dc3}$	11
$v_{dc1} \geq \sigma \geq v_{dc3} \geq v_{dc2}$	12

4.2.2 Factors that affect the DC voltage balance

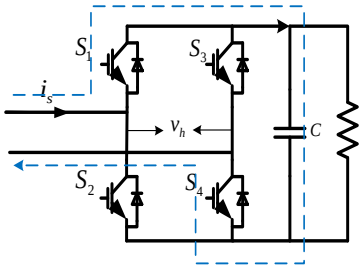
If the system is imbalanced, operation point no longer locates in the (a,a,a). In order to balance the DC voltages, most suitable switching pairs that benefit to voltage balance have to be utilized. The problem arises what are the factors that affect the DC voltages.

According to the characteristics of the H-bridge converter, the current path of it can be shown in Figure 4-5 (a)-(h). It can be seen that the DC voltages will be affected by the direction of i_s and v_h. In Figure 4-5 (a) and (d) i_s will charge the DC voltage. In Figure 4-5 (b) and (c) i_s will discharge the DC voltage. While i_s will not affect the DC voltage in Figure 4-5 (e)-(h).

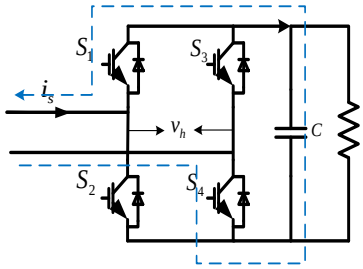
The conclusion can be got that the DC bus voltage is affected by the value of PWM voltage v_h and the input current, which can be summarized as shown in Table 4-2. $v_{dci}\uparrow$ and $v_{dci}\downarrow$ mean the trend of DC voltage affected by i_s rather than the real change of the DC voltages since there is load connected to DC port, which will absorb the power from DC capacitor.

Table 4-2 Factors influence the DC voltage

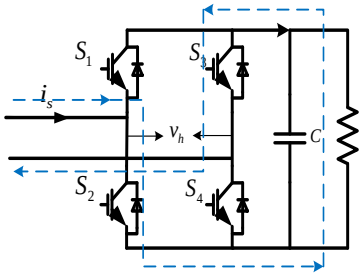
$i_s.v_h > 0$	$v_{dci}\uparrow$
$i_s.v_h < 0$	$v_{dci}\downarrow$



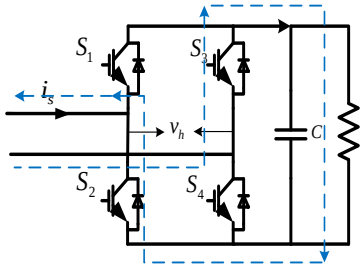
(a) $v_h>0, i_s>0$



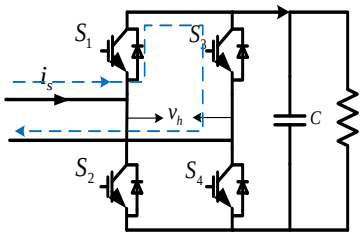
(b) $v_h>0, i_s<0$



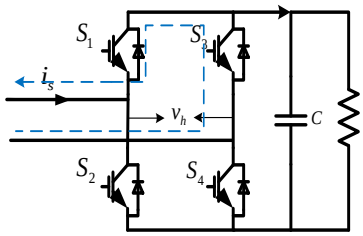
(c) $v_h<0, i_s>0$



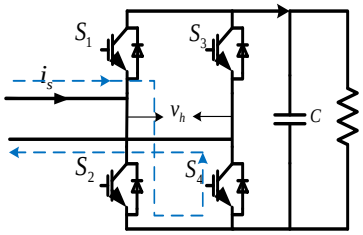
(d) $v_h<0, i_s<0$



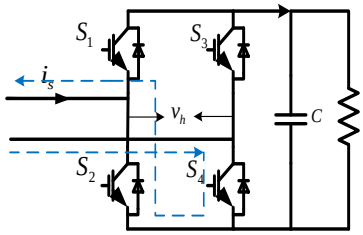
(e) $v_h=0, i_s>0$



(f) $v_h=0, i_s<0$



(g) $v_h=0, i_s>0$



(h) $v_h=0, i_s<0$

Figure 4-5 H-bridge converter DC voltage charge path

4.2.3 3-D space modulation

Having understood the operation area for cascaded seven-level converter and the factors affect the DC bus voltages, this part describes the proposed 3D space modulation scheme step by step.

Step 1: Identify the two layers from which the vectors are chosen

For cascaded seven-level converter, the 27 switching pairs can possibly compose seven layers to separate the cubic space into six sub-spaces according to the value of $F_1 + F_2 + F_3$. These layers are marked by different colors, as shown in Figure 4-6. Table 4-3 lists the switching pairs in each layer.

Table 4-3 Switching pair in each layer

layer	Switching pairs
-3	[-1,-1,-1]
-2	[0,-1,-1] [-1,0,-1][-1,-1,0]
-1	[0,-1,0][1,-1,-1][0,0,-1][-1,1,-1][-1,0,0][-1,-1,1]
0	[-1,0,1][0,-1,1][1,-1,0][1,0,-1][0,1,-1][-1,1,0][0,0,0]
1	[-1,1,1][0,0,1][1,-1,1][1,0,0][1,1,-1][0,1,0]
2	[0,1,1] [1,0,1][1,1,0]
3	[1,1,1]

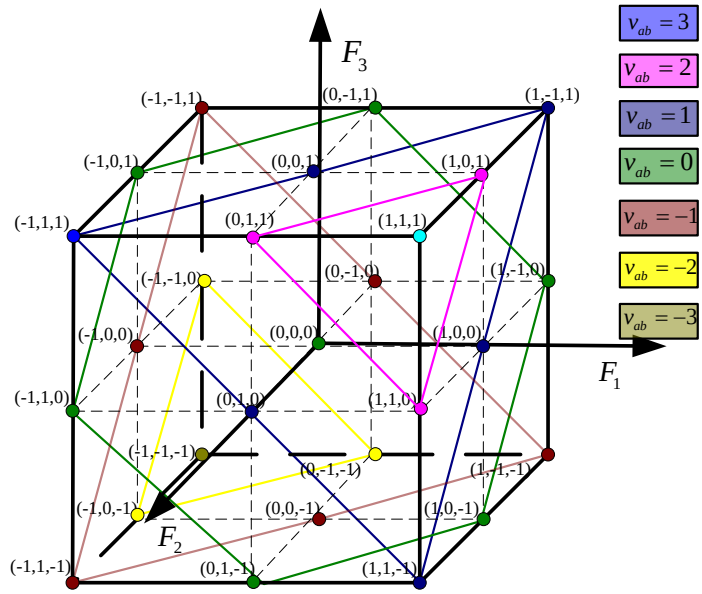


Figure 4-6 Sub-space division by different layers

The six sub-spaces stand for $v_{ab} \in$ [-3,-2],[-2,-1],[-1,0],[0,1],[1,2],[2,3] respectively. If do not consider about the over-modulation, the cascaded-seven level converter will always run in these six subspaces. Then the two switching pairs from the nearest two layers are selected to hypothesize the desired PWM voltage.

Step 2: Choose the two switching pairs according to the DC bus values

Having chosen the layers used to hypothesize the desired PWM voltage, the step 2 is to choose the switching pairs most suitable for voltage balance. In order to understand the principle of choosing switching pairs better, projecting all the layers into the same plane, and the situation where $v_{ab} > 0$ is shown in Figure 4-7. Layer 0, 1, 2, and 3 are depicted in the figure. The operation plane is also projected as shown in the dotted triangle. As has been

discussed in 4.2.1, the possible operation plane is divided into 12 sub-sections, as shown in Figure 4-7. The control objective is to operate the system towards the origin of the coordinate, which indicates the balance of the system. According to the analysis 4.2.2, under the situation that $v_{ab} > 0$, a positive current will charge the capacitor and a negative current will discharge the capacitor. The switching pairs in the operation sub-section will contribute to the balance of the system when $i_s < 0$, while the switching pairs in the opposite sub-section will contribute to the balance of the system when $i_s > 0$. Thus in order to balance the DC voltages, the following principles should be adopted to choose the two switching pairs from two layers according to the analysis in 4.2.2:

1. The switching pairs should be chosen from the operation sub-section boundary when $i_s < 0$
2. The switching pairs should be chosen from the opposite sub-section boundary when $i_s > 0$
3. If there is no switching pair located in the sub-section boundary, choose the nearest switching pair.

For example, if the system operates in the section 1, $v_{ab} \in [0,1]$, and $i_s > 0$, the switching pairs from opposite sub-section, which is the sub-section 7 according to principle 2 should be chosen. The switching pair chosen from layer 0 is (-1,1,0) and the switching pair chosen from layer 1 is (0,1,0). Similarly, if the system operates in the section 1, $v_{ab} \in [0,1]$, and $i_s < 0$, the switching pairs from operation sub-section, which is the sub-section 1 according to principle 1 should be chosen. The switching pair chosen from layer 0 is (1,-1,0), and the switching pair chosen from the layer 1 is (1,-1,1). If $v_{ab} \in [1,2]$, and $i_s > 0$, the switching pair chosen from

layer 1 is (0,1,0). While there is no switching pair available in the opposite sub-section boundary in layer2, the nearest one is chosen according to principle 3, and it is (0,1,1). If $v_{ab} \in [1,2]$, and $i_s < 0$, the switching pair chosen from layer 1 is (1,-1,1), and switching pair chosen from layer 2 is (1,0,1). If $v_{ab} \in [2,3]$, and $i_s > 0$, the switching pair chosen from the layer 2 is (0,1,1), which is the nearest one, and the switching pair from layer 3 can only be (1,1,1). While if $v_{ab} \in [2,3]$, and $i_s < 0$, the switching pair chosen from layer 2 is (1,0,1) and the switching pair chosen from the layer 3 is (1,1,1). All other situations can be analyzed similarly based on these principles. Table 4-4 summarizes the switching table under the situation $v_{ab} > 0$, $i_s > 0$, and Table 4-5 summarizes the switching table under the situation $v_{ab} > 0$, $i_s < 0$.

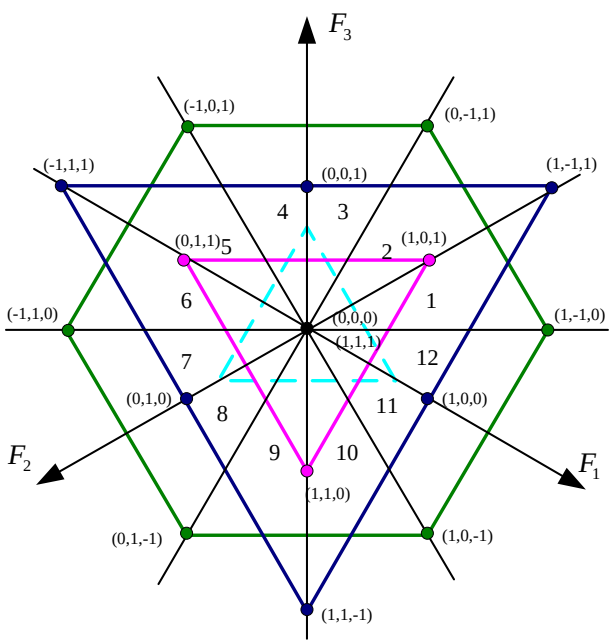


Figure 4-7 Switching pair selection diagram when $v_{ab}>0$

Table 4-4 Switching table $v_{ab}>0$, $i_s>0$

Operating situation	section	[0,1]	[1,2]	[2,3]
$v_{dc1} \geq v_{dc3} \geq \sigma \geq v_{dc2}$	1	(-1,1,0)(0,1,0)	(0,1,0) (0,1,1)	(0,1,1) (1,1,1)
$v_{dc3} \geq v_{dc1} \geq \sigma \geq v_{dc2}$	2	(0,1,-1) (0,1,0)	(0,1,0) (1,1,0)	(1,1,0) (1,1,1)
$v_{dc3} \geq \sigma \geq v_{dc1} \geq v_{dc2}$	3	(0,1,-1)(1,1,-1)	(1,1,-1) (1,1,0)	(1,1,0) (1,1,1)
$v_{dc3} \geq \sigma \geq v_{dc2} \geq v_{dc1}$	4	(1,0,-1)(1,1,-1)	(1,1,-1) (1,1,0)	(1,1,0) (1,1,1)
$v_{dc3} \geq v_{dc2} \geq \sigma \geq v_{dc1}$	5	(1,0,-1)(1,0,0)	(1,0,0) (1,1,0)	(1,1,0) (1,1,1)
$v_{dc2} \geq v_{dc3} \geq \sigma \geq v_{dc1}$	6	(1,-1,0) (1,0,0)	(1,0,0)(1,0,1)	(1,0,1) (1,1,1)
$v_{dc2} \geq \sigma \geq v_{dc3} \geq v_{dc1}$	7	(1,-1,0)(1,-1,1)	(1,-1,1) (1,0,1)	(1,0,1) (1,1,1)
$v_{dc2} \geq \sigma \geq v_{dc1} \geq v_{dc3}$	8	(0,-1,1)(1,-1,1)	(1,-1,1) (1,0,1)	(1,0,1) (1,1,1)
$v_{dc2} \geq v_{dc1} \geq \sigma \geq v_{dc3}$	9	(0,-1,1)(0,0,1)	(0,0,1) (1,0,1)	(1,0,1) (1,1,1)
$v_{dc1} \geq v_{dc2} \geq \sigma \geq v_{dc3}$	10	(-1,0,1) (0,0,1)	(0,0,1)(0,1,1)	(0,1,1) (1,1,1)
$v_{dc1} \geq \sigma \geq v_{dc2} \geq v_{dc3}$	11	(-1,0,1)(-1,1,1)	(-1,1,1) (0,1,1)	(0,1,1) (1,1,1)
$v_{dc1} \geq \sigma \geq v_{dc3} \geq v_{dc2}$	12	(-1,1,0)(-1,1,1)	(-1,1,1) (0,1,1)	(0,1,1) (1,1,1)

Table 4-5 Switching table $v_{ab}>0$, $i_s<0$

Operating situation	section	[0,1]	[1,2]	[2,3]
$v_{dc1} \geq v_{dc3} \geq \sigma \geq v_{dc2}$	1	(1,-1,0)(1,-1,1)	(1,-1,1) (1,0,1)	(1,0,1) (1,1,1)
$v_{dc3} \geq v_{dc1} \geq \sigma \geq v_{dc2}$	2	(0,-1,1)(1,-1,1)	(1,-1,1) (1,0,1)	(1,0,1) (1,1,1)
$v_{dc3} \geq \sigma \geq v_{dc1} \geq v_{dc2}$	3	(0,-1,1)(0,0,1)	(0,0,1) (1,0,1)	(1,0,1) (1,1,1)
$v_{dc3} \geq \sigma \geq v_{dc2} \geq v_{dc1}$	4	(-1,0,1) (0,0,1)	(0,0,1)(0,1,1)	(0,1,1) (1,1,1)
$v_{dc3} \geq v_{dc2} \geq \sigma \geq v_{dc1}$	5	(-1,0,1)(-1,1,1)	(-1,1,1) (0,1,1)	(0,1,1) (1,1,1)
$v_{dc2} \geq v_{dc3} \geq \sigma \geq v_{dc1}$	6	(-1,1,0)(-1,1,1)	(-1,1,1) (0,1,1)	(0,1,1) (1,1,1)
$v_{dc2} \geq \sigma \geq v_{dc3} \geq v_{dc1}$	7	(-1,1,0)(0,1,0)	(0,1,0) (0,1,1)	(0,1,1) (1,1,1)
$v_{dc2} \geq \sigma \geq v_{dc1} \geq v_{dc3}$	8	(0,1,-1) (0,1,0)	(0,1,0) (1,1,0)	(1,1,0) (1,1,1)
$v_{dc2} \geq v_{dc1} \geq \sigma \geq v_{dc3}$	9	(0,1,-1)(1,1,-1)	(1,1,-1) (1,1,0)	(1,1,0) (1,1,1)
$v_{dc1} \geq v_{dc2} \geq \sigma \geq v_{dc3}$	10	(1,0,-1)(1,1,-1)	(1,1,-1) (1,1,0)	(1,1,0) (1,1,1)
$v_{dc1} \geq \sigma \geq v_{dc2} \geq v_{dc3}$	11	(1,0,-1)(1,0,0)	(1,0,0) (1,1,0)	(1,1,0) (1,1,1)
$v_{dc1} \geq \sigma \geq v_{dc3} \geq v_{dc2}$	12	(1,-1,0) (1,0,0)	(1,0,0)(1,0,1)	(1,0,1) (1,1,1)

Similarly, the projected diagram under the situation $v_{ab} < 0$ is shown in Figure 4-8, where layer -3,-2,-1,0 are projected. The operation plane is also projected as shown in the dotted triangle. According to the analysis in 4.2.2, under the situation that $v_{ab} < 0$ a positive current

will discharge the capacitor and a negative current will charge the capacitor. The switching pairs in the operation sub-section will contribute to the balance of the system when $i_s > 0$, while the switching pairs in the opposite sub-section will contribute to the balance of the system when $i_s < 0$. Thus in order to balance the DC voltages, the following principles should be adopted to choose the two switching pairs from two layers according to the analysis in 4.2.2:

1. The switching pairs should be chosen from the operation sub-section boundary when $i_s > 0$
2. The switching pairs should be chosen from the opposite sub-section boundary when $i_s < 0$
3. If there is no switching pair located in the sub-section boundary, choose the nearest switching pair.

For example, if the system operates in the section 1, $v_{ab} \in [-1,0]$, and $i_s < 0$, the switching pairs from opposite sub-section, which is the sub-section 7 according to principle 2 should be chosen. The switching pair chosen from layer 0 is (-1,1,0), and the switching gain chosen from layer -1 is (-1,1,-1). Similarly, if the system operates in the section 1, $v_{ab} \in [-1,0]$, and $i_s > 0$, the switching pairs from operation sub-section, which is the sub-section 1according to principle 1 should be chosen. The switching pair chosen from layer 0 is (1,-1,0), and the switching pair chosen from the layer -1 is (0,-1,0). If $v_{ab} \in [-2,-1]$, and $i_s < 0$, the switching pair chosen from layer -1 is (-1,1,-1) and the switching pair chosen from layer -2 is (-1,0,-1). If $v_{ab} \in [-2,-1]$, and $i_s > 0$, the switching pair chosen from layer -1 is (0,-1,0). While there is no

switching pair available in the operation sub-section boundary in layer -2, the nearest one is chosen according to principle 3, and it is (0,-1,-1). If $v_{ab} \in [-3,-2]$, and $i_s < 0$, the switching pair chosen from the layer -2 is (-1,0,-1), and the switching pair from layer -3 can only be (-1,-1,-1). While if $v_{ab} \in [-3,-2]$, and $i_s > 0$, there is no switching pair available in the operation sub-section boundary in layer -2, the nearest one is chosen according to principle 3, and it is (0,-1,-1) .The switching pair chosen from the layer -3 is (-1,-1,-1). All other situations can be analyzed similarly based on these principles. Table 4-6 summarizes the switching table under the situation $v_{ab} < 0$, $i_s > 0$, and Table 4-7 summarize the switching table under the situation $v_{ab} < 0$, $i_s < 0$.

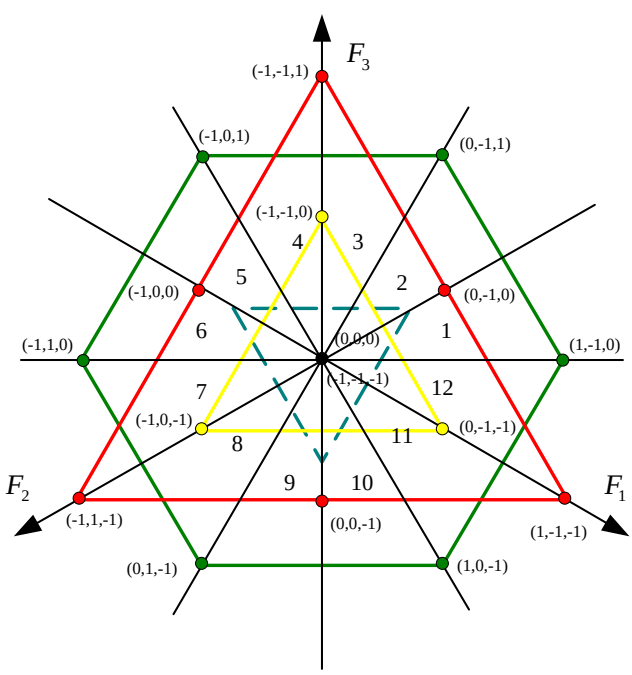


Figure 4-8 Switching pair selection diagram when $v_{ab} < 0$

Table 4-6 Switching table $v_{ab}<0$, $i_s>0$

Operating situation	section	[0,-1]	[-1,-2]	[-2,-3]
$v_{dc2} \geq \sigma \geq v_{dc3} \geq v_{dc1}$	1	(1,-1,0)(0,-1,0)	(0,-1,0)(0,-1,-1)	(0,-1,-1) (-1,-1,-1)
$v_{dc2} \geq \sigma \geq v_{dc1} \geq v_{dc3}$	2	(0,-1,1) (0,-1,0)	(0,-1,0)(-1,-1,0)	(-1,-1,0) (-1,-1,-1)
$v_{dc2} \geq v_{dc1} \geq \sigma \geq v_{dc3}$	3	(0,-1,1)(-1,-1,1)	(-1,-1,1) (-1,-1,0)	(-1,-1,0) (-1,-1,-1)
$v_{dc1} \geq v_{dc2} \geq \sigma \geq v_{dc3}$	4	(-1,0,1) (-1,-1,1)	(-1,-1,1) (-1,-1,0)	(-1,-1,0) (-1,-1,-1)
$v_{dc1} \geq \sigma \geq v_{dc2} \geq v_{dc3}$	5	(-1,0,1)(-1,0,0)	(-1,0,0)(-1,-1,0)	(-1,-1,0) (-1,-1,-1)
$v_{dc1} \geq \sigma \geq v_{dc3} \geq v_{dc2}$	6	(-1,1,0) (-1,0,0)	(-1,0,0)(-1,0,-1)	(-1,0,-1) (-1,-1,-1)
$v_{dc1} \geq v_{dc3} \geq \sigma \geq v_{dc2}$	7	(-1,1,0)(-1,1,-1)	(-1,1,-1) (-1,0,-1)	(-1,0,-1) (-1,-1,-1)
$v_{dc3} \geq v_{dc1} \geq \sigma \geq v_{dc2}$	8	(0,1,-1) (-1,1,-1)	(-1,1,-1) (-1,0,-1)	(-1,0,-1) (-1,-1,-1)
$v_{dc3} \geq \sigma \geq v_{dc1} \geq v_{dc2}$	9	(0,1,-1)(0,0,-1)	(0,0,-1)(-1,0,-1)	(-1,0,-1) (-1,-1,-1)
$v_{dc3} \geq \sigma \geq v_{dc2} \geq v_{dc1}$	10	(1,0,-1) (0,0,-1)	(0,0,-1)(0,-1,-1)	(0,-1,-1) (-1,-1,-1)
$v_{dc3} \geq v_{dc2} \geq \sigma \geq v_{dc1}$	11	(1,0,-1)(1,-1,-1)	(1,-1,-1) (0,-1,-1)	(0,-1,-1) (-1,-1,-1)
$v_{dc2} \geq v_{dc3} \geq \sigma \geq v_{dc1}$	12	(1,-1,0) (1,-1,-1)	(1,-1,-1) (0,-1,-1)	(0,-1,-1) (-1,-1,-1)

Table 4-7 Switching table $v_{ab}<0$, $i_s<0$

Operating situation	section	[0,-1]	[-1,-2]	[-2,-3]
$v_{dc2} \geq \sigma \geq v_{dc3} \geq v_{dc1}$	1	(-1,1,0)(-1,1,-1)	(-1,1,-1) (-1,0,-1)	(-1,0,-1) (-1,-1,-1)
$v_{dc2} \geq \sigma \geq v_{dc1} \geq v_{dc3}$	2	(0,1,-1) (-1,1,-1)	(-1,1,-1) (-1,0,-1)	(-1,0,-1) (-1,-1,-1)
$v_{dc2} \geq v_{dc1} \geq \sigma \geq v_{dc3}$	3	(0,1,-1)(0,0,-1)	(0,0,-1)(-1,0,-1)	(-1,0,-1) (-1,-1,-1)
$v_{dc1} \geq v_{dc2} \geq \sigma \geq v_{dc3}$	4	(1,0,-1) (0,0,-1)	(0,0,-1)(0,-1,-1)	(0,-1,-1) (-1,-1,-1)
$v_{dc1} \geq \sigma \geq v_{dc2} \geq v_{dc3}$	5	(1,0,-1)(1,-1,-1)	(1,-1,-1) (0,-1,-1)	(0,-1,-1) (-1,-1,-1)
$v_{dc1} \geq \sigma \geq v_{dc3} \geq v_{dc2}$	6	(1,-1,0) (1,-1,-1)	(1,-1,-1) (0,-1,-1)	(0,-1,-1) (-1,-1,-1)
$v_{dc1} \geq v_{dc3} \geq \sigma \geq v_{dc2}$	7	(1,-1,0)(0,-1,0)	(0,-1,0)(0,-1,-1)	(0,-1,-1) (-1,-1,-1)
$v_{dc3} \geq v_{dc1} \geq \sigma \geq v_{dc2}$	8	(0,-1,1) (0,-1,0)	(0,-1,0)(-1,-1,0)	(-1,-1,0) (-1,-1,-1)
$v_{dc3} \geq \sigma \geq v_{dc1} \geq v_{dc2}$	9	(0,-1,1)(-1,-1,1)	(-1,-1,0)(-1,-1,1)	(-1,-1,0) (-1,-1,-1)
$v_{dc3} \geq \sigma \geq v_{dc2} \geq v_{dc1}$	10	(-1,0,1) (-1,-1,1)	(-1,-1,1) (-1,-1,0)	(-1,-1,0) (-1,-1,-1)
$v_{dc3} \geq v_{dc2} \geq \sigma \geq v_{dc1}$	11	(-1,0,1)(-1,0,0)	(-1,0,0)(-1,-1,0)	(-1,-1,0) (-1,-1,-1)
$v_{dc2} \geq v_{dc3} \geq \sigma \geq v_{dc1}$	12	(-1,1,0) (-1,0,0)	(-1,0,0)(-1,0,-1)	(-1,0,-1) (-1,-1,-1)

Step3: Calculate the switching time

Having chosen the switching pairs according to the working situation of the system, the next step is to calculate the switching time for each H-bridge. In order to simplify the

calculation of switching time, the mapping technique presented in [107] is adopted to calculate the dwelling time of each switching pair. The calculation of the switching time is explained below. The function “floor” means rounds the value to nearest integer less than the value, while the function “ceil” means rounds the value to nearest integer larger than the value.

If $v_{ab} > 0$:

$$a = floor(|v_{ab}|) \quad t_2 = (|v_{ab}| - a)T_s \;\; t_1 = (a + 1 - |v_{ab}|)T_s \tag{4-3}$$

If $v_{ab} < 0$:

$$a = abs(ceil(v_{ab})) \quad t_2 = (|v_{ab}| - a)T_s \;\; t_1 = (a + 1 - |v_{ab}|)T_s \tag{4-4}$$

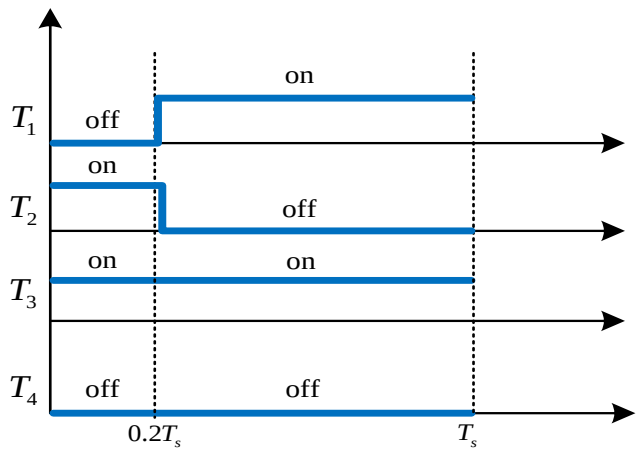
For each H-bridge converter, the switching selections are then defined as shown in (4-5) in order to balance the loss for each device.

$$F_i = \begin{cases} -1, S_{i2}, S_{i3}ON \\ 0, i_s > 0 S_{i1}, S_{i3}ON \\ 0, i_s < 0 S_{i2}, S_{i4}ON \\ 1, S_{i1}, S_{i4}ON \end{cases} (i = 1, 2, 3) \tag{4-5}$$

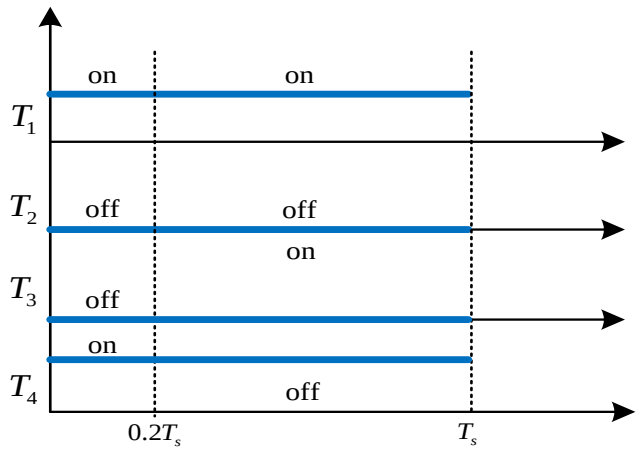
For example, if the system operate under the situation $v_{ab} = 0.8$, $i_s > 0$, and $v_{dc1} \geq v_{dc3} \geq \sigma \geq v_{dc2}$ .According to the Table. IV, the switching pairs chosen is (-1,1,0) and (0,1,0). Based on equation (3), we can calculate that :

$$a = 0, t_2 = 0.8T_s, t_1 = 0.2T_s \tag{4-6}$$

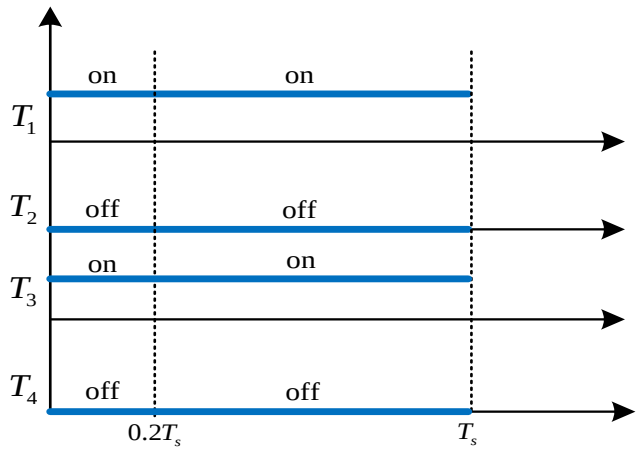
Figure 4-9 (a)-(c) illustrates the switching sequence for H-bridge 1, H-bridge 2 and H-bridge3 respectively according to principle described in (4-5).



(a) H-bridge 1



(b) H-bridge 2



(c)H-bridge 3

Figure 4-9 Switching sequences for H-bridges

4.2.4 Discussion of proposed 3D space modulation

Although the proposed 3D space modulation with voltage balancing capability is designed for cascaded seven-level converter, the concept can also be extended to cascaded converter with higher level. The graphical representation is difficult, while the concept remains valid. The most suitable switching pairs can be grouped according to analysis methodology presented and get the similar switching table as shown above. While it will be more complicated when the level increases which is the drawback of most space modulation techniques. Besides for the phase shifted PWM (PS-PWM) method, it can push the equivalent switching frequency to mf , where f is the effective switching frequency of each H-bridge cell and m is the number of cells cascaded [93], [94]. For the proposed 3D space modulation scheme, the equivalent switching frequency is equal to the effective switching frequency of each H-bridge, thus will lead to larger passive components. However, the switching loss for each H-bridge by adopting the proposed 3D space modulation is still competitive compared with PS-PWM with the same switching frequency especially operating in high modulation index situation. Since according to switch Table 4-4 to Table 4-7, the switching pairs that best for DC voltage balancing is always chosen, and lots of operation sections share the same switching pairs which lead to less unnecessary switching process, which promise a possible lower switching loss.

4.3 Simulation and Experiments Verification

In order to verify the proposed 3D space modulation strategies, simulation tests were conducted in scaled down single-phase cascaded seven-level converter. The parameters are shown in Table 4-8, and the system control method adopted in this chapter is the same as presented in [78], which is shown in Figure 4-10. Single-phase d-q coordinate control is adopted to realize better AC current tracking performance, and dual loop control strategy is adopted to realize fast total DC voltage regulation. Due to space limitation, no detail is repeated in this chapter. This basic controller can only control the total DC voltages, while the voltage balance is not guaranteed with traditional phase shifted PWM method. In [78], the additional DC voltage balance controller is proposed to balance the DC voltage and this controller is also described in Figure 4-10. Two individual DC voltage controllers are added for H-bridge 1and H-bridge 2 to modify the duty cycle. While for H-bridge3, since the total DC voltages is already controlled, the modification of duty cycle is set as $\Delta d_3=-(\Delta d_1+\Delta d_2)$. The following simulation and experimental results will demonstrate the ability of proposed 3D space modulation strategy without any additional individual control loop compared with this PI-based solution.

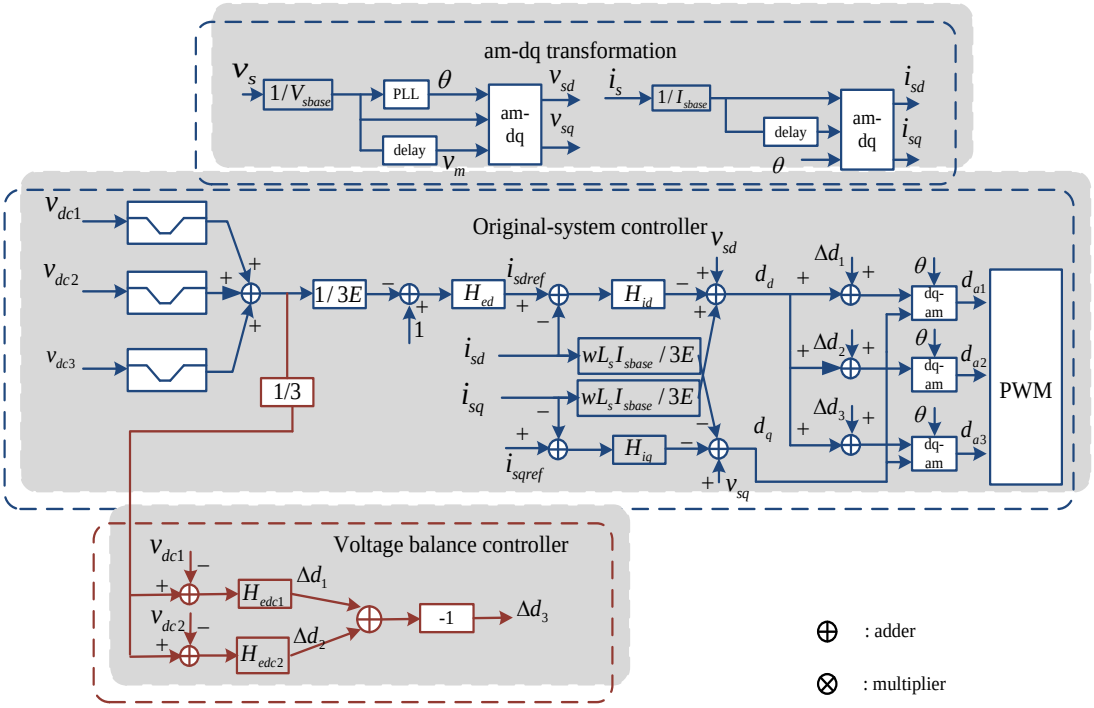
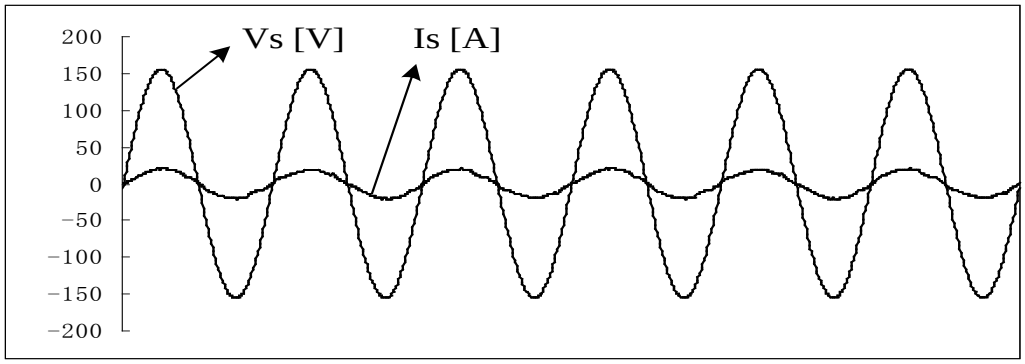


Figure 4-10 Control diagram for single-phase seven-level converter under single-phase d-q coordinate

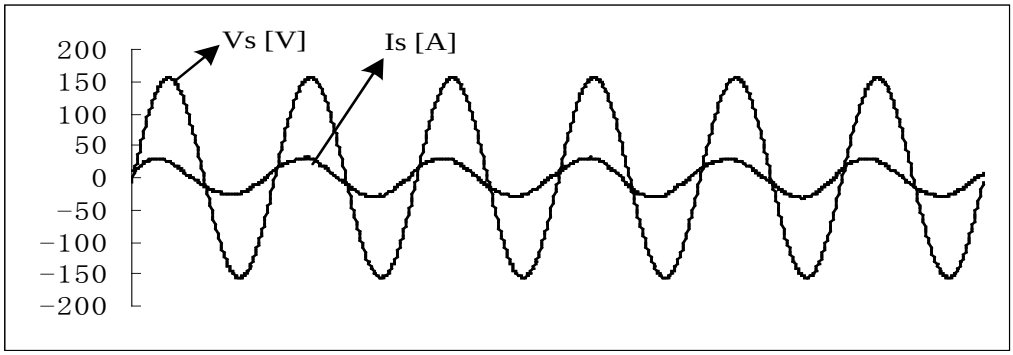
Table 4-8 System parameters for simulation

Source voltage	110V (rms)
Source frequency	60Hz
DC link voltage	70*3=210V
Switching frequency	10KHz
Input inductance	3.5mH
DC link capacitor	2700uF

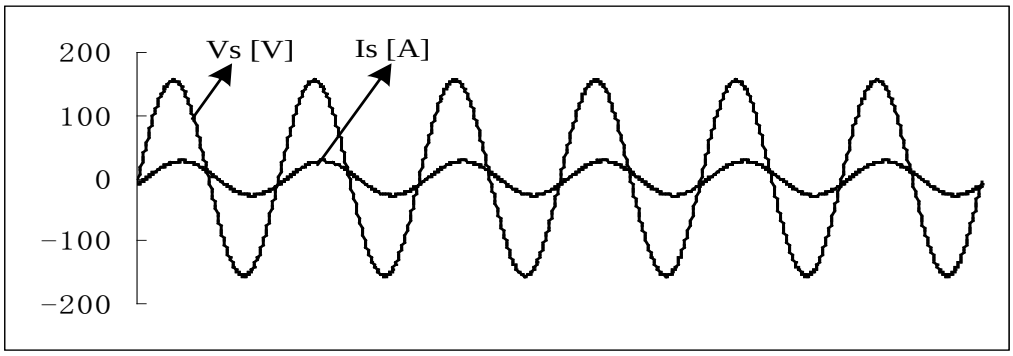
Figure 4-11 (a) to Figure 4-11 (c) show the steady state regulation performance, the loads in three DC ports are set to 7A. Figure 4-15 (a)-(c) show voltage and current under the unity power factor operation, capacitive mode operation (PF=0.866), and inductive mode operation (PF=0.866) respectively. Figure 4-12 shows the three DC voltages, which are all controlled to 70V.



(a) Unity power factor operation



(b) Capacitive mode operation



(c) Inductive mode operation

Figure 4-11 Input voltage and current under different operating modes

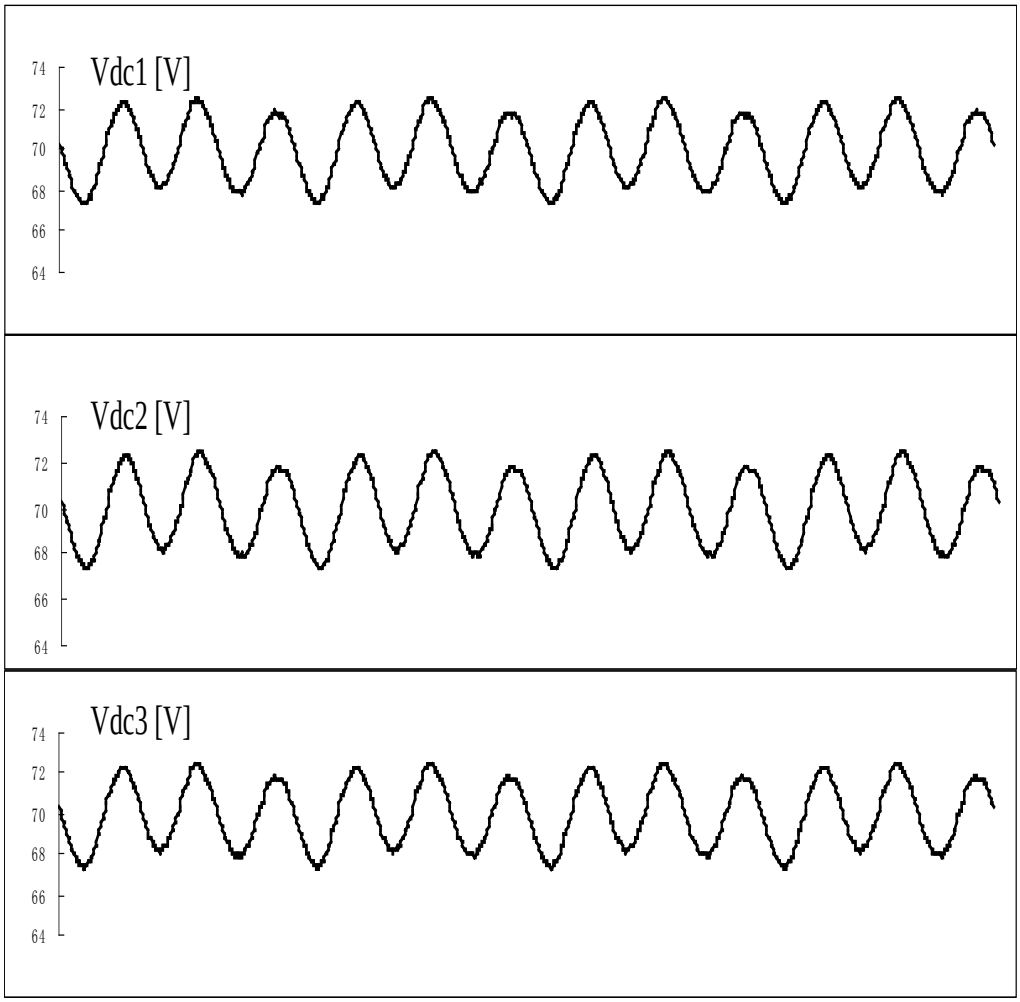


Figure 4-12 DC bus voltages under balance situation

In order to verify the voltage balancing capability of proposed 3-D space modulation scheme, the loads connected to each DC port are set to 7A, 8.75A, and 14A respectively. In Figure 4-13, voltage balance capability under unity power factor operation mode is demonstrated. Before 3D space modulation works, the normal PS-PWM is adopted as modulation method, and the DC voltages are imbalanced. When the 3D space modulation is added, the DC voltages converge to 70V within 20ms without any overshoot. Similarly,

voltage balancing capability is tested for capacitive mode operation as shown in Figure 4-14, and inductive mode operation as shown in Figure 4-15. It is obviously that the proposed 3D space vector modulation can also balance the DC voltages in these two modes.

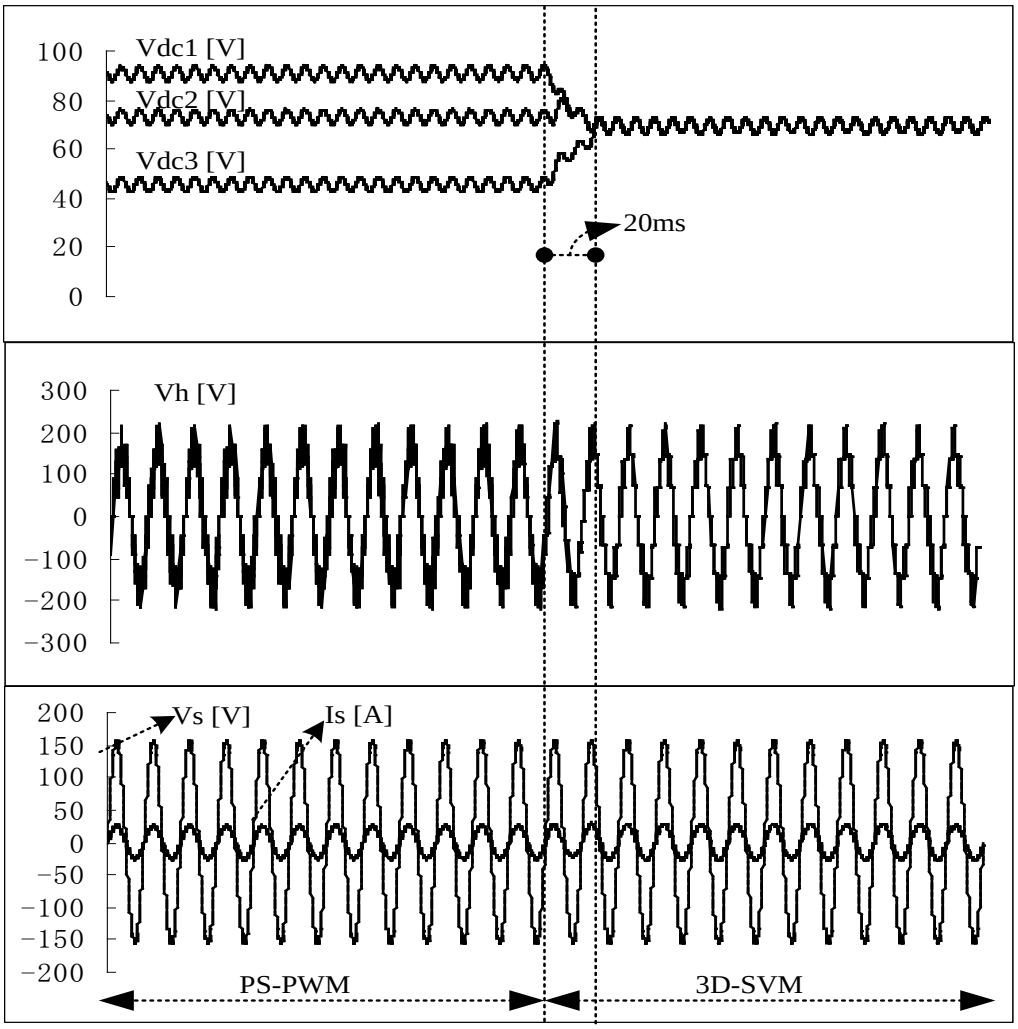


Figure 4-13 Voltage balance under unity power factor mode

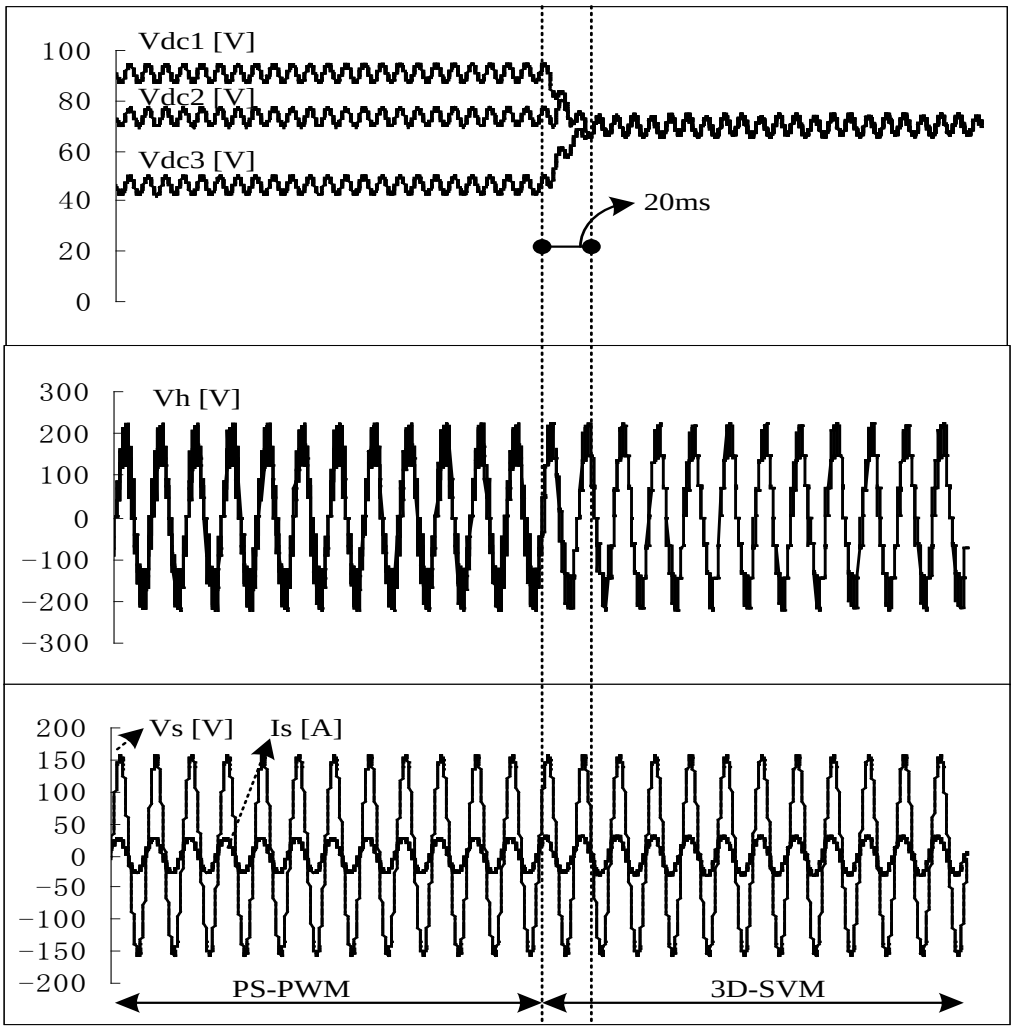


Figure 4-14 Voltage balance under capacitive mode

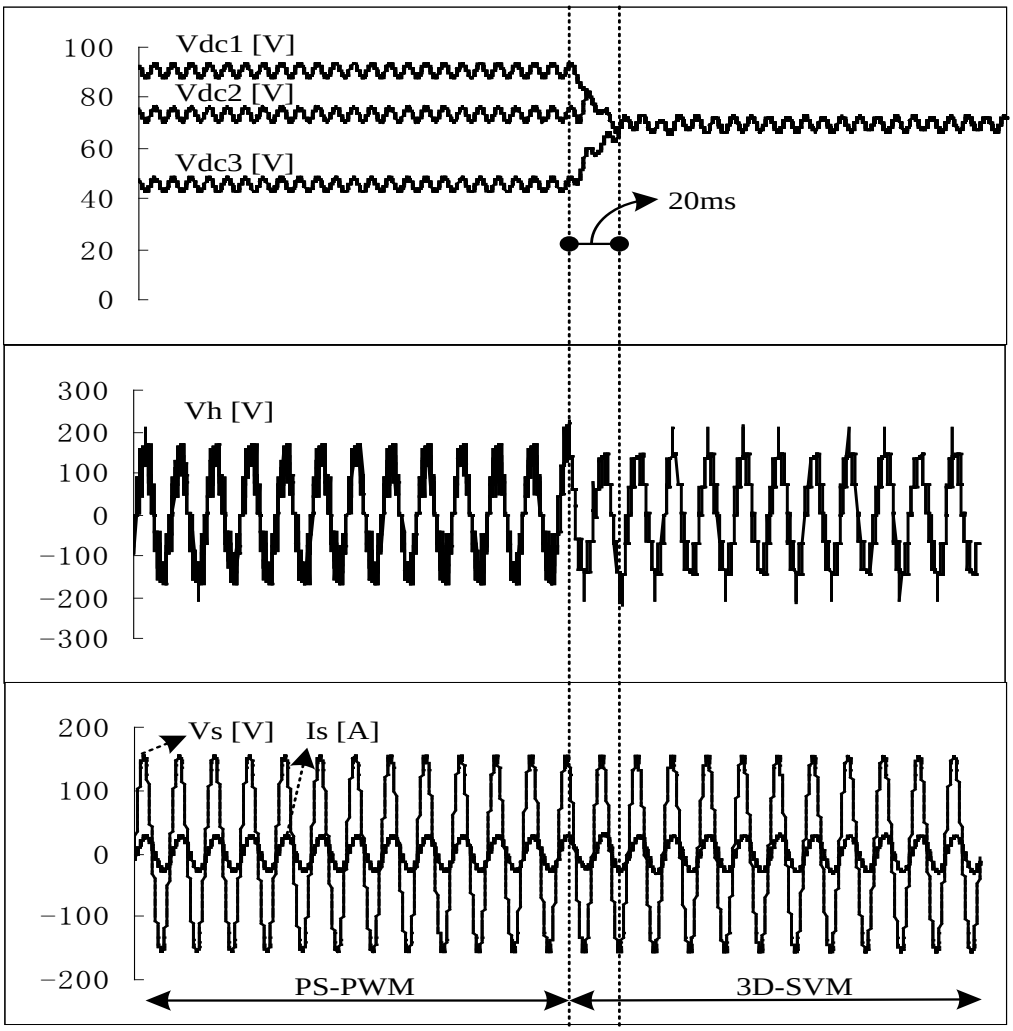
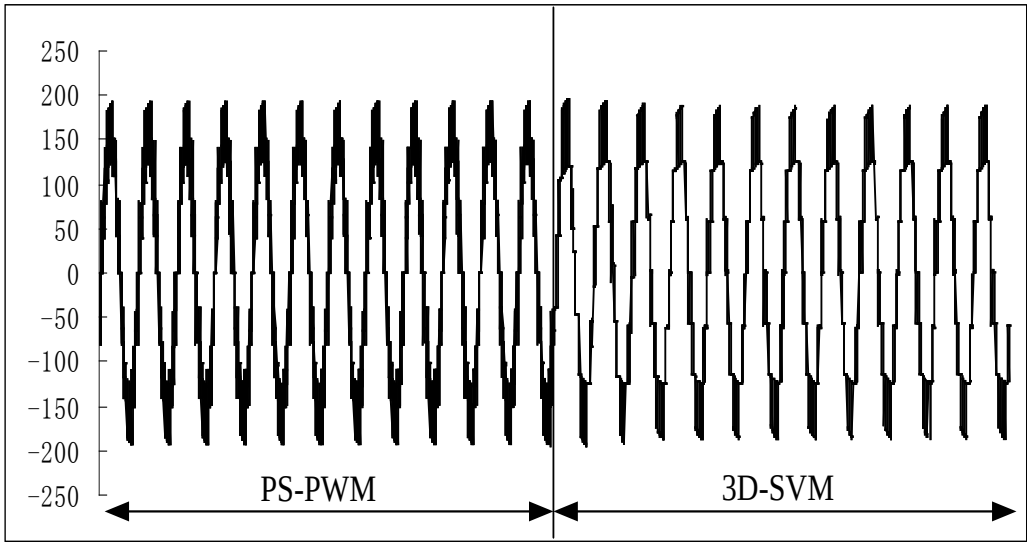
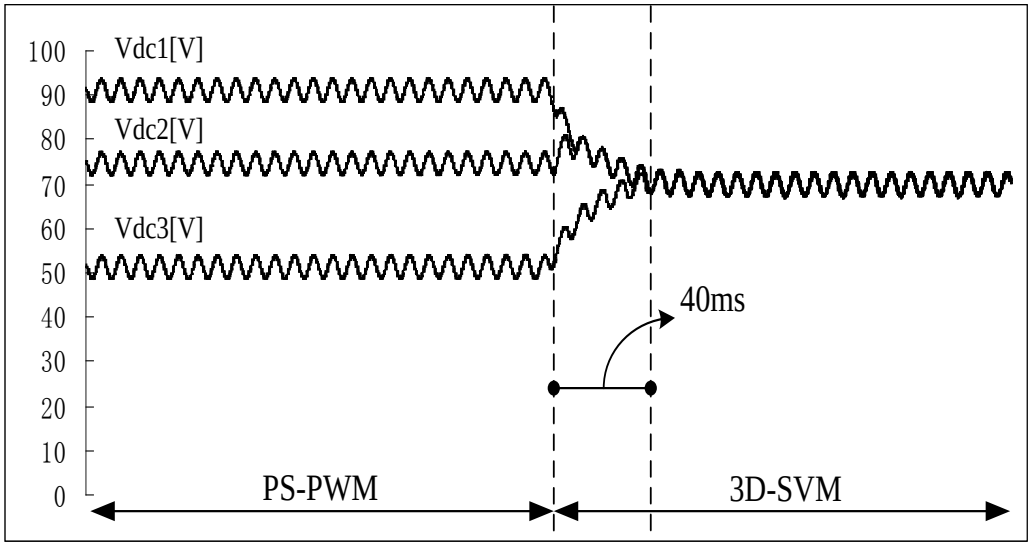


Figure 4-15 Voltage balance under inductive mode

In high power, high voltage application area, the switching frequency of multilevel converter is generally set to relatively low, such as 1 kHz, for loss reduction. In order to verify the effectiveness of the proposal in low switching frequency operation, tests are made with switching frequency of 1 kHz, as shown in Figure 4-16. Due to relatively low switching frequency, the DC balance time will be longer compared with 10 kHz, and it is about 40ms. The effectiveness of the proposal in low switching frequency operation is also excellent.



(a) PWM voltages



(b) DC voltages

Figure 4-16 3D space modulation with 1kHz switching frequency

Figure 4-17 shows the scaled down cascaded seven-level rectifier prototype and the experiments are carried out to verify the proposed method. The system parameters are shown in Table 4-9. The load connected to each DC port is 25Ohm for balanced state operation.

Table 4-9 System parameters for experiments

Source voltage	110V (rms)
Source frequency	60Hz
DC link voltage	70*3=210V
Switching frequency	10KHz
Input inductance	3.5mH
DC link capacitor	900uF

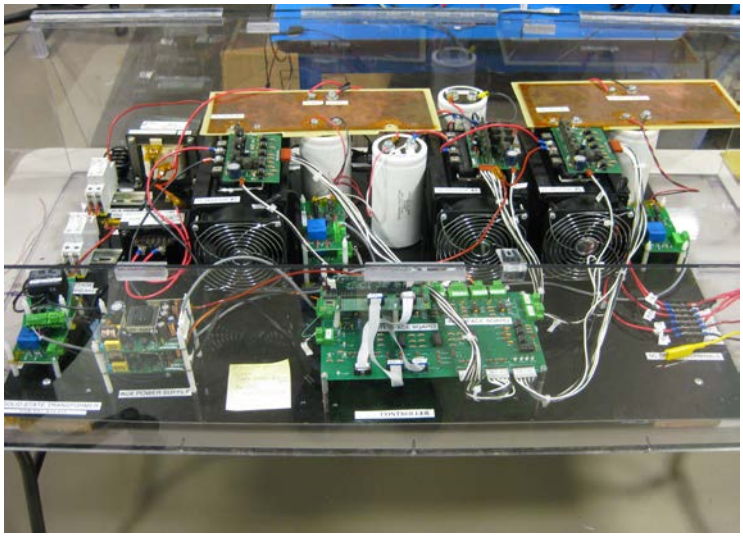
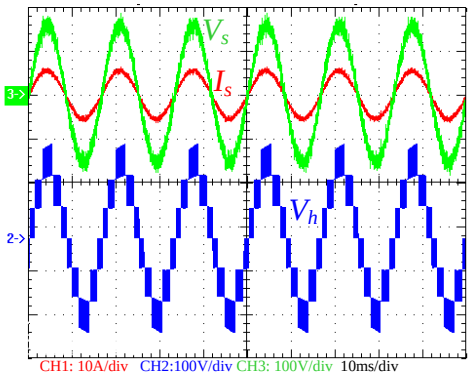
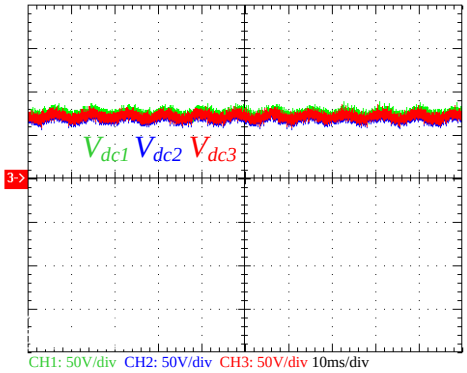


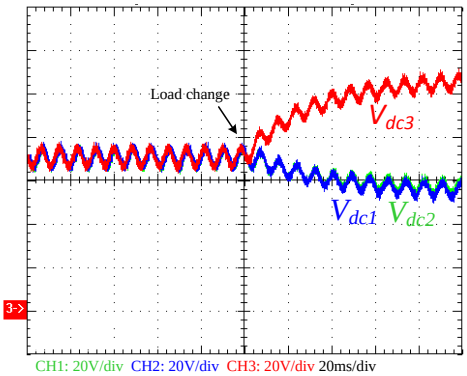
Figure 4-17 Cascaded seven-level converter prototype



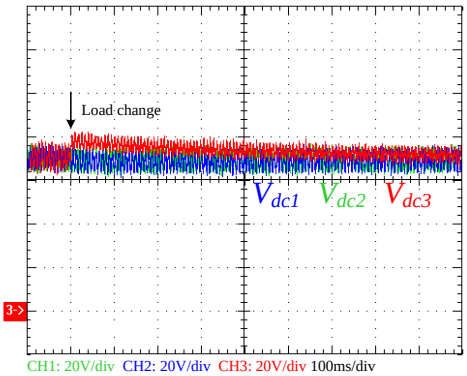
(a) AC side waveforms with balanced load



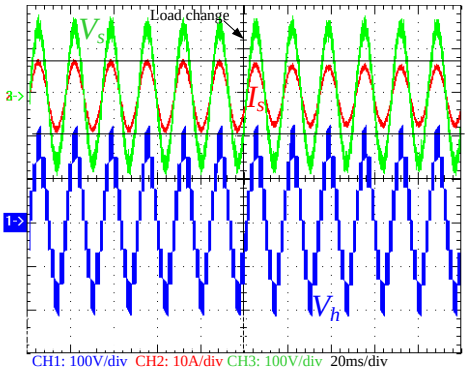
(b) Balanced state DC voltages with balanced load



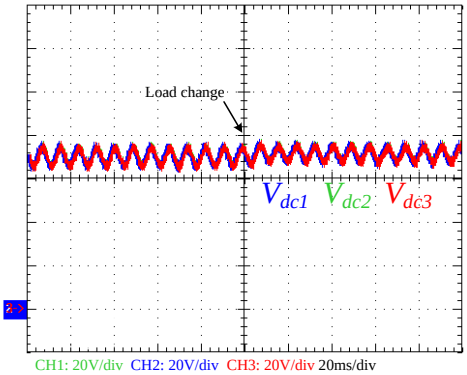
(c) DC voltage imbalance with traditional PS-PWM



(d) DC voltage balancing under PI-based solution



(e) 3D space PWM under load change condition



(f) DC voltage balancing with 3D space PWM

Figure 4-18 Performance comparison of different voltage balance methods

Figure 4-18 (a)-(f) shows the key operation waveforms of proposed 3-D space modulation. Figure 4-18 (a) shows the balanced state AC side waveforms, which include input voltage,

input current, and PWM voltage. The current is in phase with the voltage thus indicates the unity power factor operation mode. The PWM voltage is a seven-level voltage due to three H-bridge cascaded together. Figure 4-18 (b) shows the balanced state DC voltages, which are all controlled to 70V. In Figure 4-18 (c), the load connected to H-bridge 3 is changed to 50Ohm under the traditional PS-PWM method without additional voltage balancing controller. The DC voltages will diverge due to unequal power distribution among each H-bridge. If the PI-based solution presented in [10] is adopted (Kp=1, Ki=2 under per-unit calculation), as shown in Figure 4-18 (d), the voltage will gradually converge to the 70V while the dynamic is low, which has been shown in many other works [17],[18]. Figure 4-18 (e) and (f) present the voltage balance performance by adopting proposed 3-D space modulation. Figure 4-18 (e) shows the AC input voltage, input current, and PWM voltage. Due to the load change, the input current will decrease, as marked by the dotted line. Figure 4-18 (f) shows the DC voltages under load change, the voltages maintain balanced even at the point when load changes, thus indicates the extreme good voltage balancing capability of the proposed method.

4.4 Conclusion

In this chapter, a novel 3-D space modulation with voltage balancing capability is proposed for rectifier stage of presented Solid State Transformer. By choosing the most suitable switching pairs for each H-bridge, this method provides an alternative view in investigating the voltage balancing mechanism in cascaded multilevel converter. Compared with traditional PI based voltage balancing method, it has a fast and accurate performance. The

Simulation and Experimental results demonstrate the excellent performance of the proposed method.

Chapter 5 A High Performance and Low Cost Power Balance Controller for DC/DC stage

5.1 Introduction

DC/DC converter with high frequency isolation is adopted as the middle stage to step down the voltage. In the presented modularized SST topology, the parallel operated DAB converters are adopted. By using this modularized approach, high power rating SST can be easily achieved. However, due to the parameter mismatch, especially the leakage inductance, the power may be unequal for each DC/DC converter, and therefore the current stress of them will not be the same if only the voltage balance controller is adopted for the rectifier stage. In fact, it is shown in chapter that the power balance controller is necessary for the system, while the voltage balance controller may only be needed for easy implementation of the power balance controller. However, two controllers working together will ensure the best voltage balance performance in both dynamic and steady state operation. In addition, the voltage balance controller can minimize the voltage imbalance issue when in the fault tolerant operating condition.

Some previous works have been done to address these issues. In [77], a common duty ratio controller for the rectifier stage in the single phase d-q coordinate and feedback feed-forward controller for the DAB stage are proposed. However, this method only considers the voltage balance among the DC links in the front-end cascaded multilevel rectifier. The power

balance issue when considering the parameter mismatch among the DC/DC converters is not covered. In addition, the presented fixed gain feed-forward method makes the disturbances in either side of the DC/DC stage easily reflects to the other side. Therefore, the source/load disturbance rejection capability, which is one of the core advantages of the SST, will be affected. In order to balance voltage in the rectifier stage as well as the power in the DC/DC stage with various parameter mismatch, voltage and power balance controllers are proposed in [78], which can achieve good performance according to the simulation. However, this method needs additional current sensors for the DAB stage and these current sensors should be high speed ones since it uses the DAB leakage inductor current as the feedback, which is a high frequency AC one.

In this chapter, the single phase d-q coordinate controller is also adopted for the cascaded multilevel rectifier as presented in [104], [105], while a novel power balance controller for the DC/DC stage is proposed without sensing any current in the DC/DC stage[108], [109]. Experimental results in a seven-level SST with three modules in both rectifier and DAB stages are presented for verifying the concept.

5.2 A current sensor-less power balance controller for DC/DC stage

5.2.1 Power balance issue of the parallel operated DAB converters

Figure 5-1 shows the topology of the DAB converter adopted in the parallel operated DC/DC stage. It is featured with bidirectional power flow, soft switching capability in a wide operation range (high efficiency), and low component part (high power density)[110].

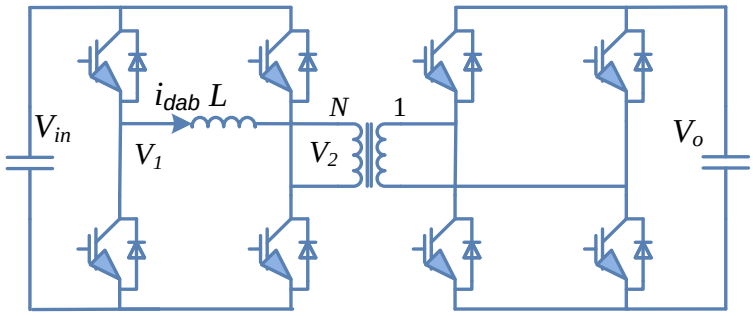


Figure 5-1 Topology of DAB converter

The basic operation principle of the DAB converter is depicted in Figure 5-2 , in which the voltage ratio of input and output equals to the transformer turn ratio. This mode is called unity mode. If the voltage ratio of the input and output voltage is higher than the transformer turn ratio, it is called buck mode, otherwise it is called the boost mode.

By adjusting the phase-shift between the primary side H-bridge and the secondary side H-bridges, the power transferred by this circuit can be described as [110]:

$$P = \frac{V_{in} V_o}{2\pi f N L} \phi \left(1 - \frac{\phi}{\pi}\right) \tag{5-1}$$

Where, V_{in}, V_o are the input and output voltage, N is the turns ratio of the transformer, f is the switching frequency of the converter, L is the equivalent inductance (include leakage inductance of the transformer and auxiliary inductance) in the primary side, and ϕ is the phase shift of the PWM signal between primary and secondary side H-bridge. It is observed from (1) that if the same phase shift is adopted for all DAB converters, the mismatch of the parameters, such as transformer leakage inductance, will cause the unbalanced power sharing among them. Therefore, different phase shift may be needed for the each DAB converter.

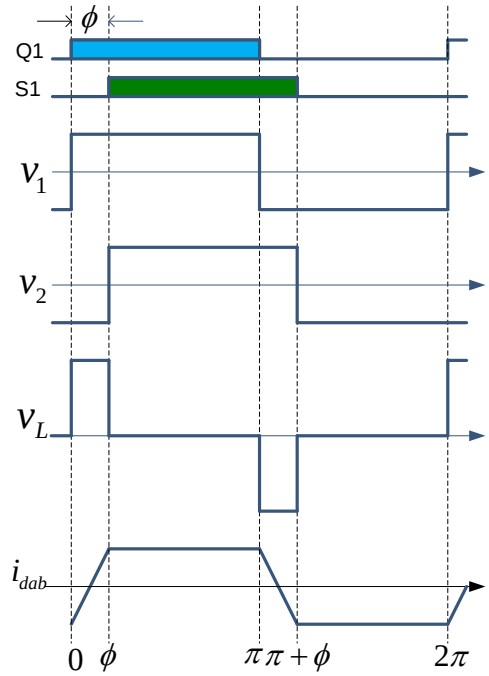


Figure 5-2 Operation principle for DAB converter

Figure 5-3 shows the generalized control structure for the DC/DC stage. Basically, the original system controller generates the common phase shift ϕ for regulating the low voltage DC bus. The current balance controller is adopted to generate the modified phase shift for each DAB converter, therefore to achieve the current balance among them.

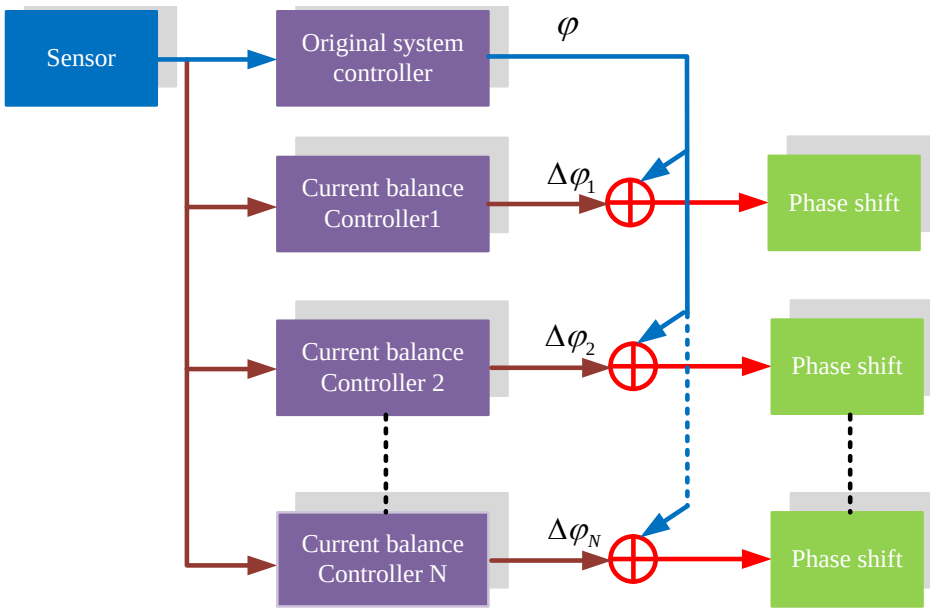


Figure 5-3 Generalized current balance controller for DC/DC stage

A power balance controller has been proposed in [78], which is depicted in Figure 5-4. The average power of DAB converter is calculated and different phase shift is generated for each of them. This method needs additional current sensors for the DAB stage, which adds cost to the system. In addition, the sensed DAB current is a high frequency one, therefore requires high speed sensors as well as high performance analog to digital converter (ADC) for implementation in digital signal processor (DSP). Furthermore, the calculation of the power is also not easy. In this condition, the performance of the controller may not be guaranteed in the real hardware setup. In fact, no experiment results are reported for the power balance controller proposed in [78].

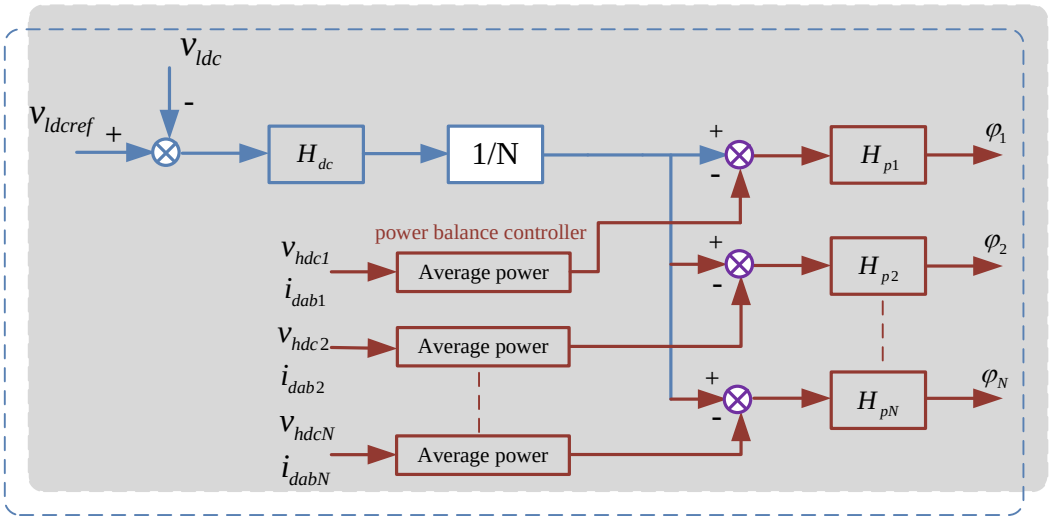


Figure 5-4 Power balance controller for DC/DC converters [78]

The power balance controller that is proposed in [77] that can potentially remove the current sensors, and it is shown in Figure 5-5 and Figure 5-6. The idea of this controller is that one of the high voltage DC bus is regulated by the dual-loop controller in the rectifier stage. Additionally, the feed-forward term is applied in the controller of the DC/DC stage, and therefore regulates high voltage DC to be the same. Since the common duty cycle is applied for all the H-bridges in the rectifier stage, the power balance is also achieved. However, due to the feed-forward control fashion of the DC/DC stage, the disturbance in the high voltage/low voltage side will be easily transferred to the other side. In this condition, the distinguished disturbance rejection capability of the presented SST topology will be affected.

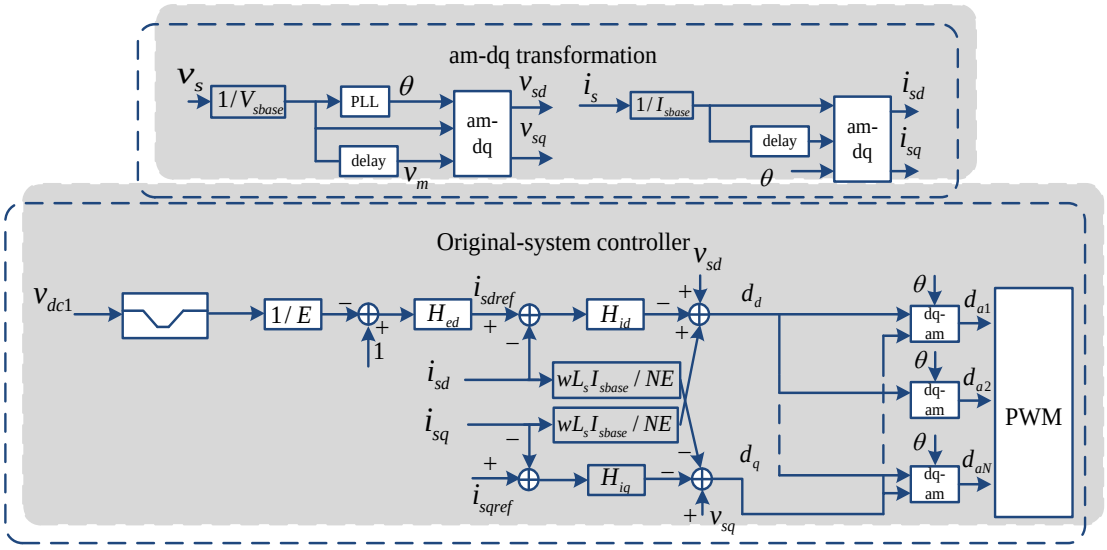


Figure 5-5 Rectifier stage controller with common duty cycle

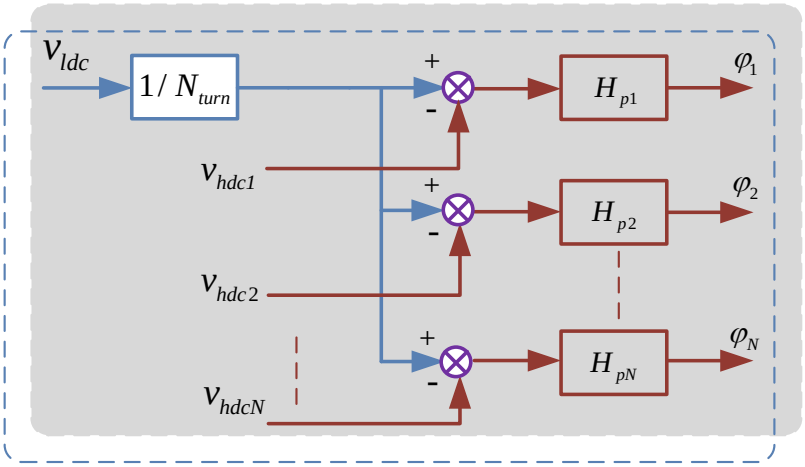


Figure 5-6 Power balance controller for DC/DC converters [77]

Figure 5-7 shows another possible solution of achieving voltage balance and power balance by regulating the phase shift of the DAB converters [111]. The DC voltage at the high

voltage DC link is used as the feedback for the DC/DC stage. Different phase shift is generated for each DAB converter to ensure the voltage balance at the rectifier stage, and therefore the power is also balanced according to (5-1) for the DAB stage. This method gets rid of the drawbacks that exists in the [77] aforementioned. However, only the power balance controller in the DC/DC stage contributes to the DC voltage balance in the rectifier stage, which may limit its regulation capability and the potential performance in the fault tolerant operation.

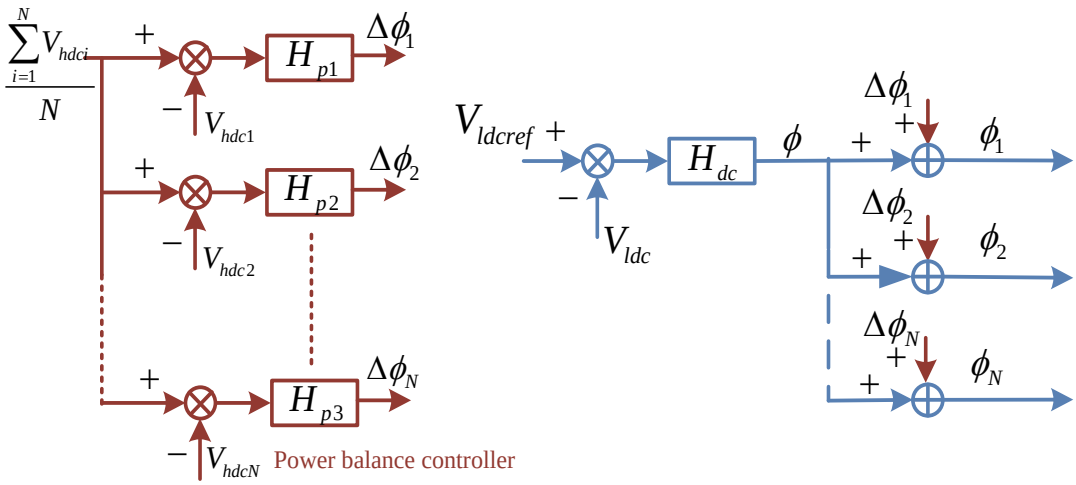


Figure 5-7 DC/DC stage controller with power balance control capability

In order to solve aforementioned problem, a novel power balance controller is proposed by using the active component of duty cycles in the cascaded multilevel rectifier stage as the feedback signal for the DC/DC stage. By using this method, no additional current sensor is needed and high performance can be achieved.

5.2.2 Relationship between active component of duty cycle in rectifier stage and the transferred power

According to the circuit shown in Figure 3-4 in chapter 3, the following derivations can be made as proved in [78]:

$$\sum_{i=1}^{N} V_{abi} = V_s - jwL_s I_s \tag{5-2}$$

$$V_{abi} = (d_{di} + d_{qi}\, j)V_{dci}\,(i = 1...N) \tag{5-3}$$

Substitute (5-3) into (5-2) and rearrange the terms:

$$\sum_{i=1}^{N} d_{di} V_{dci} = V_s \tag{5-4}$$

$$\sum_{i=1}^{N} d_{qi} V_{dci} = -wL_s I_s \tag{5-5}$$

The active power of each H-bridge is calculated as:

$$P_i = I_s d_{di} V_{dci}\,(i = 1...N) \tag{5-6}$$

Base on the law of conservation of energy and neglect the losses in the converter system, the power of each H-bridge in the cascaded multilevel rectifier, which is P_{reci}, should be equal to the power of the DAB connected to it, which is P_{dabi}:

$$P_{reci} = I_s d_{di} V_{dci} = P_{dabi} = \frac{V_{dci} V_o}{2\pi\, fNL_i} \phi_i \left(1 - \frac{\phi_i}{\pi}\right)(i = 1...N) \tag{5-7}$$

Due to the series connection of the cascaded multilevel rectifier, the current flows through each H-bridge cell should be the same, which is i_s. Therefore, the equalization of $d_{di} V_{dci}$ indicates the power balance among the DAB converters.

For the cascaded multilevel rectifier topology, if the loads in the DC links are the same, the DC voltage balance of the cascaded multilevel rectifier stage can be nearly guaranteed and the active power component of the duty cycle d_{di} should be almost the same.

This observation motivates the core idea in this chapter: the active power component of the duty cycle in each module of rectifier stage can be used as the feedback of the power balance controller in the DC/DC stage. By actively regulating the phase shift of DAB converters, the active power component of duty cycles in the rectifier stage will be the same, meaning the power balance condition is achieved. In turn, if the power transferred in each DC link is the same, the DC voltage will be balanced automatically as aforementioned. Therefore, the same duty cycle can be applied to each H-bridge in the rectifier stage to ensure the voltage balance of the system in the final steady state.

5.2.3 Novel cost effective power balance controller for the paralleled DAB converters

Figure 5-8 shows the proposed current sensor-less power balance controller for the parallel operated DAB converters in the presented SST topology. In this controller, a common phase shift is generated by the DC voltage regulation loop. The active power component of duty cycle for each H-bridge cell in the rectifier stage is adopted as the feedback signal for the power balance controller, the reference of which is set to the average value of them as shown in the redline of Figure 5-8. The active power component of duty cycle is a DC signal therefore the traditional PI controller can be directly applied. By using this power balance controller, the modification of the phase shift for each DAB converter is generated, which is

denoted as $\Delta\phi_1, \Delta\phi_2, \ldots \Delta\phi_N$. These modifications are added to the common phase shift to compose the individual phase shift for each DAB converter. In the final steady state, the active component of the duty cycles $d_{di}(i=1...N)$ will be identical, and the power flows through the DAB converters will be the same.

It is seen from Figure 5-8 that the proposed power balance controller does not need any current sensor, therefore is cost effective. In addition, the dynamic in the one side of the DC/DC stage will not affect the other due to the closed loop regulation. Furthermore, the active power component of duty cycles for the rectifier stage can be easily accessed from the DSP, thus the implementation is very simple.

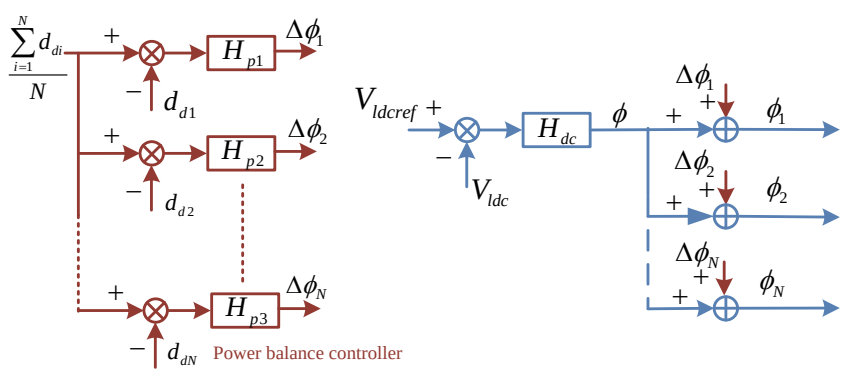


Figure 5-8 Current sensor-less power balance controller for DC/DC stage

5.3 Simulation and experimental results

In order to verify the proposed method, simulation and experimental results are carried out in a three-stage seven-level SST system. In this system, a cascade seven-level rectifier with

three modules is adopted as the front-end stage, and three DAB converter is connected to each high voltage DC link with secondary side connected in parallel.

5.3.1 Simulation results

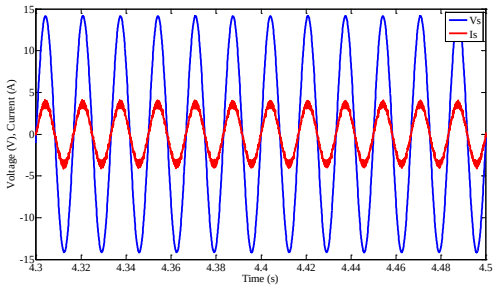
Table 5-1 gives the main parameters used for the simulation. The leakage inductance and magnetizing inductance for the transformer 1 are 3mH and 18mH. The leakage inductance and magnetizing inductance for the transformer 2 and 3 are 4mH and 34mH.

Table 5-1 Parameters of the system

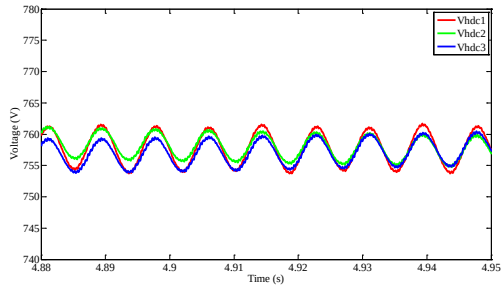
Rectifier stage (3 modules)		DC/DC stage (3 modules)		Inverter stage (1 module)	
Switching frequency	1.2 KHz	Switching frequency	3.6 KHz	Switching frequency	10.8 KHz
Input voltage	High voltage DC	Transformer turns ratio	Low voltage DC	Low voltage AC	Load condition
1200V	760V*3=2280V	2:1	380V	240V	20 Ω

Figure 5-9 illustrates the simulation results without dedicated power balance controller and with voltage balance controller shown in Figure 3-16. Figure 5-9 (a) shows the input voltage and current at the high voltage side, indicating the system operating at unity power factor mode. Figure 5-9 (b) presents the DC voltages at high voltage DC link, in which the average value for three DC voltages are the same, while the ripple for the first one is higher due to the heavier load condition (larger power transferred). Figure 5-9 (c) illustrates current flowing through the DAB leakage inductor. Because of the smaller leakage inductance and magnetizing inductance, the current for the first DAB converter is larger than the other two, indicating a higher current stress. Figure 5-9 (d) gives the output DC voltage, AC voltage and

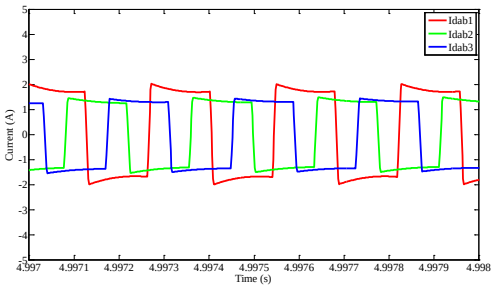
current of the SST. The active power component of the duty cycle is also shown in Figure 5-9 (e). Due to the different load condition in the system, the duty cycle is different for each H-bridge in the rectifier stage to balance the voltages among them.



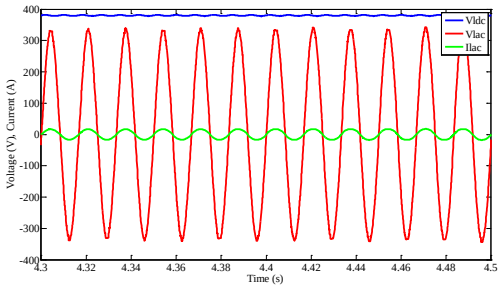
(a) Input voltage (scale to 1/120) and current



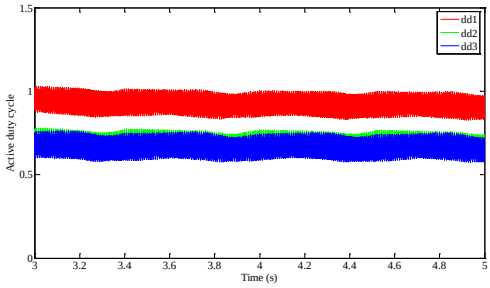
(b) DC voltages of cascaded multilevel converter



(c) DAB leakage inductor currents

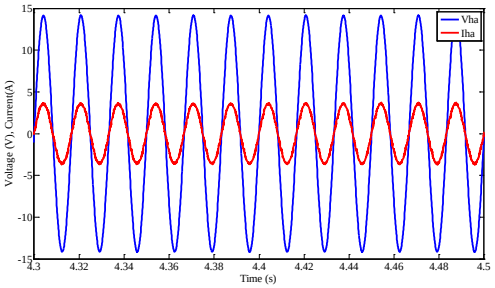


(d) Output DC voltage, AC voltage, and current

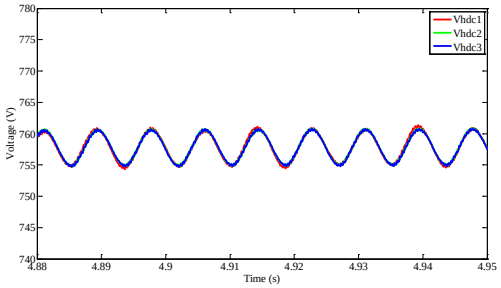


(e) Active power component of duty cycle in cascaded multilevel rectifier

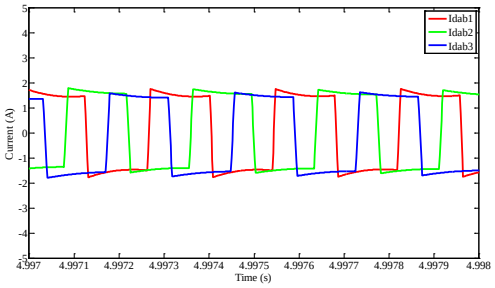
Figure 5-9 Performance of the system without power balance controller



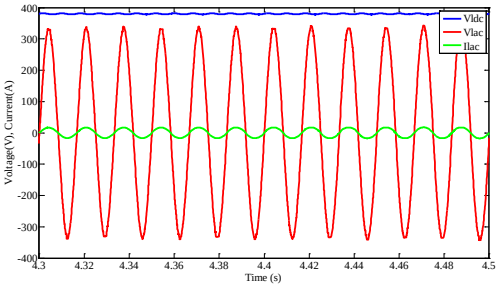
(a) Input voltage (scale to 1/120) and current



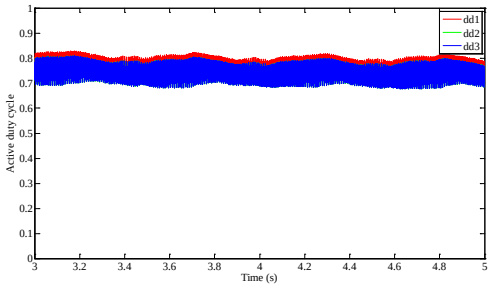
(b) DC voltages of cascaded multilevel converter



(c) DAB leakage inductor currents



(d) Output DC voltage, AC voltage, and current



(e) Active duty component of cascaded multilevel rectifier

Figure 5-10 Performance of the system with power balance controller

As a comparison, Figure 5-10 illustrates the simulation results with dedicated power balance controller and with voltage balance controller shown in Figure 3-16. Figure 5-10 (a) shows the input voltage and current at the high voltage side, indicating the system operating at unity power factor mode. Figure 5-10 (b) presents the DC voltages at high voltage DC link, in which the average value for three DC voltages are the same, while the ripple for them

are also the same. Figure 5-10 (c) illustrates current flowing through the DAB leakage inductor. Due to the effect of the power balance controller, the currents are already balanced for the three DAB converters. Figure 5-10 (d) gives the output DC voltage, AC voltage and current of the SST. The active power component of the duty cycle is also shown in Figure 5-10 (e). Due to the same load condition in the system, the duty cycle is the also the same for each H-bridge in the rectifier stage. Therefore, the proposed power balance controller can effectively address the power unbalance issue in the DC/DC stage of the presented SST topology.

5.3.2 Experimental Results

In order to verify the proposed method, experimental results are carried out in a three-stage seven-level SST prototype shown in Figure 5-11. The key parameters of the test set-up are shown in Table 5-2.

Table 5-2 Parameters of the prototype

Rectifier stage (3 modules)		**DC/DC stage (3 modules)**		**Inverter stage (1 module)**	
Switching frequency	1.2 KHz	Switching frequency	3.6 KHz	Switching frequency	10.8 KHz
Input voltage	High voltage DC	Transformer turns ratio	Low voltage DC	Low voltage AC	Load condition
600V	320V*3=960V	2:1	160V	100V	20 Ω

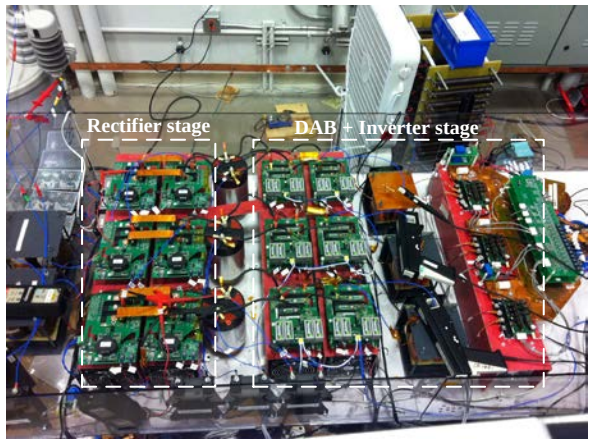


Figure 5-11 A three-stage SST prototype

In order to verify the effectiveness of the proposed method, the transformers in three DAB converters are made different on purpose. The leakage inductance and magnetizing inductance for the transformer 1 are modified to 3.32mH and 18.95mH by adding a copper sheet on top of the core as shown in Figure 5-11. The leakage inductance and magnetizing inductance for the transformer 2 are 4.02mH and 34.12mH. The leakage inductance and magnetizing inductance for the transformer 3 are 4.15mH and 37.56mH.

The single-phase d-q coordinate system controller together with voltage balance controller shown in Figure 3-16 is adopted for the rectifier stage. Experimental results without dedicated power balance controller for DC/DC stage are presented in Figure 5-12. Figure 5-12 (a) shows the waveforms of input AC voltage v_s, input seven-level PWM voltage v_{pwm}, input current i_s, and high voltage DC link 3 V_{dc3}. The current is in phase with the voltage, indicating the unity power factor operation. Figure 5-12 (b) gives the voltages V_{dc1},V_{dc2} and V_{dc3} at high voltage DC links, which are identical due to the voltage balance controller of the

rectifier stage. Figure 5-12 (c) presents the waveforms of low voltage DC link V_{ldc}, low voltage AC output voltage v_{lac} and current i_{lac}. Fig .6(d) illustrates the leakage inductor current of DAB converters, which are i_{dab1}, i_{dab2} and i_{dab3}. Because of the parameter mismatch, the module 1 has the largest current due to its lowest leakage inductance and magnetizing inductance, as shown in the red circle. The RMS value of the current for three DAB are 0.808A, 0.622A, and 0.609 A, respectively. Therefore the power is unbalanced for the three DAB converters.

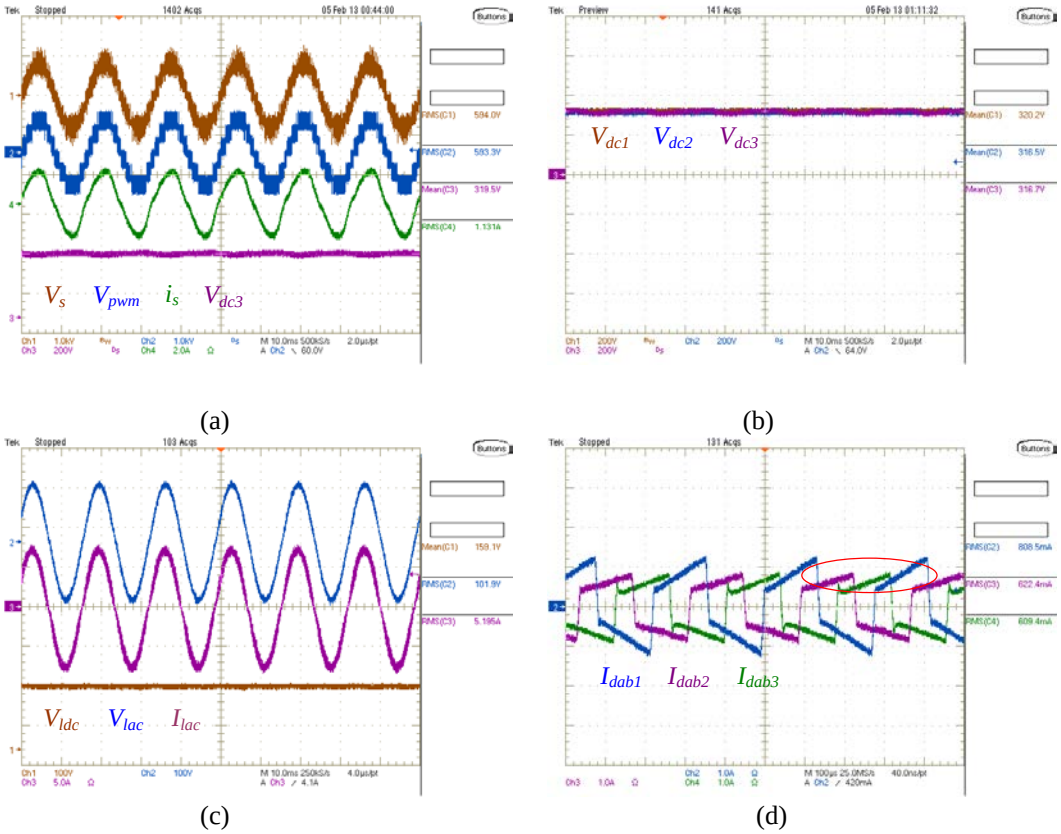


Figure 5-12 Experimental results without power balance controller: (a) Input voltage, current, PWM voltage, and High voltage DC link; (b) High voltage DC links; (c) Output DC voltage, AC voltage and current; (d) DAB leakage inductor current;

Figure 5-13 shows the waveforms when the proposed power balance controller is added. Figure 5-13 (b) demonstrates that the DC voltages can also be balanced with the proposed control system. As the comparison, Figure 5-13 (d) shows the currents in the three DAB converters. The change of the current without/with the proposed power balance controller can be observed from the red cycle marked in Figure 5-12 (d) and Figure 5-13 (d). The RMS values of the DAB currents in this condition are 0.665A, 0.642A, 0.644A, respectively, which are nearly balanced. Therefore, the proposed current balance controller is verified in the steady state operation.

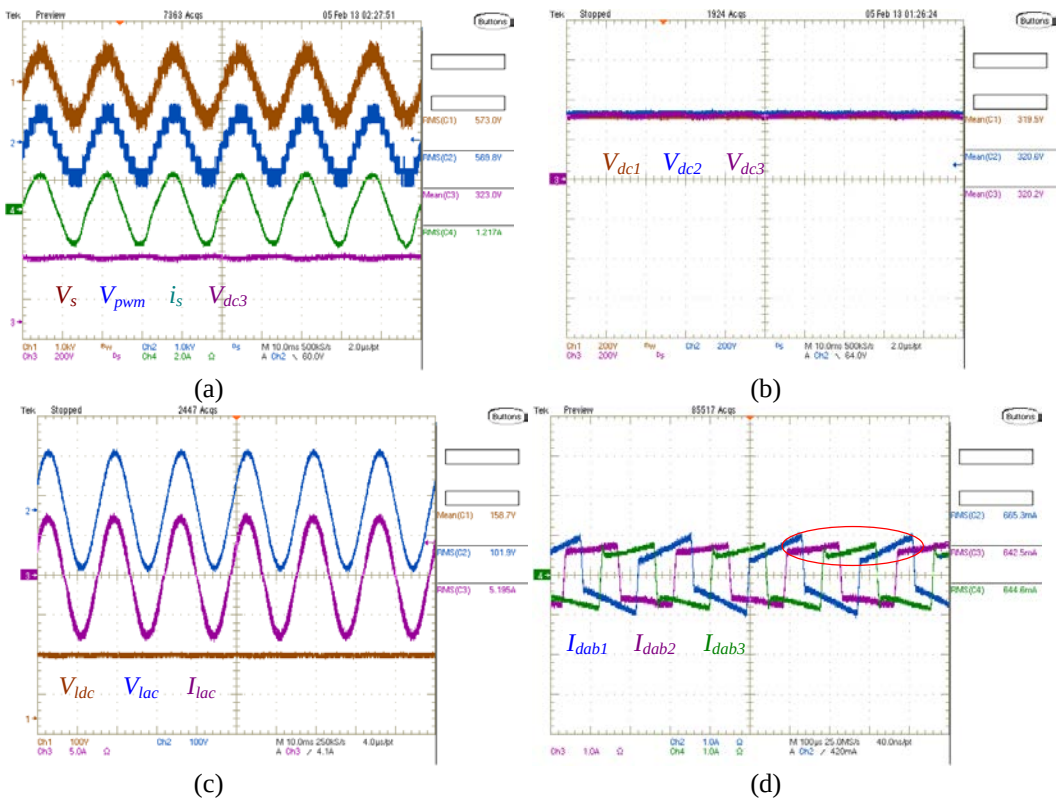
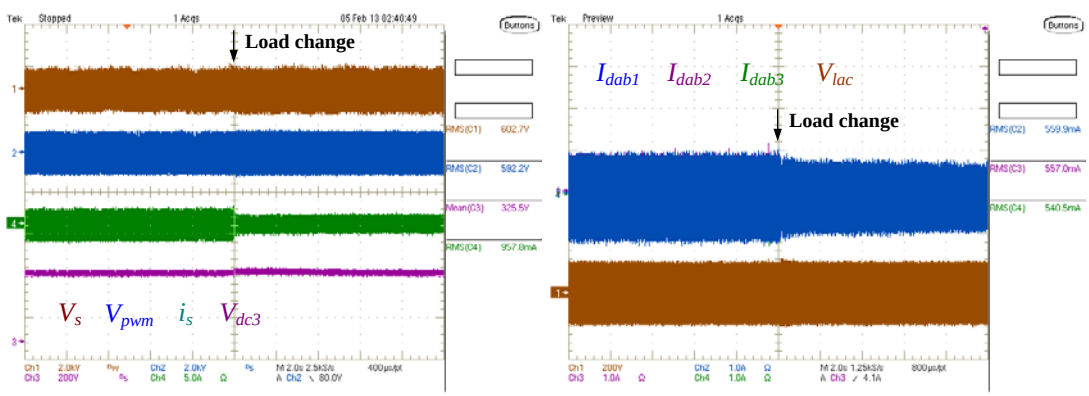


Figure 5-13 Steady state performance with proposed power balance controller: (a) Input voltage, current, PWM voltage, and High voltage DC link; (b) High voltage DC links; (c) Output DC voltage, AC voltage and current; (d) DAB leakage inductor current.

Dynamic performance of the proposed controller is also verified by changing the load from 20Ω to 40Ω at AC output side and the test results are demonstrated in Figure 5-14. Figure 5-14(a) depicts the waveforms of input AC voltage v_s, input seven-level PWM voltage v_{pwm}, input current i_s, and high voltage DC link 3 V_{dc3}. Due to the load change, the input current decreases and enters into the new steady state in a short time. The same dynamic process can be observed for the DC voltage V_{dc3}. Figure 5-14 (b) shows the DAB current i_{dab1}, i_{dab2} and i_{dab3}, as well as output voltage v_{lac}. The DAB currents decrease when the load changes while they are still nearly balanced in the dynamic process. Therefore, the dynamic response of the proposed controller system is also satisfied. Therefore, it can be concluded that the proposed power balance controller can effectively reduce the power difference among DAB converters without using any current sensor in the DC/DC stage.



(a) (b)

Figure 5-14 Dynamic performance with proposed power balance controller: (a) Input voltage, current, PWM voltage, and High voltage DC link; (b) DAB leakage inductor current and output AC voltage.

5.4 Conclusion

A novel current sensor-less power balance controller is proposed for a cascaded multilevel converter based solid state transformer. This method uses the active power component of duty cycle in the rectifier stage as the feedback signal for the power balance controller in the DAB stage. Therefore, no current sensor is needed and it is a cost effective solution. Experimental results in a seven-level solid state transformer are presented for verifying the proposed method.

Chapter 6 Hardware Design and Demonstration of a 3.6kV-120V/10kVA SST for Smart Grid Application

6.1 Introduction

This chapter presents the hardware design and test of the high voltage SST prototype in FREEMDM systems center[112], [113]. Shown in Figure 6-1, 10kVA SST that interface a 3.6kV AC grid to 120V grid is presented. The main parameters of the system are shown in Table 6-1. The SST delivers power from the 3.6kV AC port to both 120V AC grid and 200V DC grid. The power rating for low voltage DC grid is 4kW and AC grid is set to 6kVA.

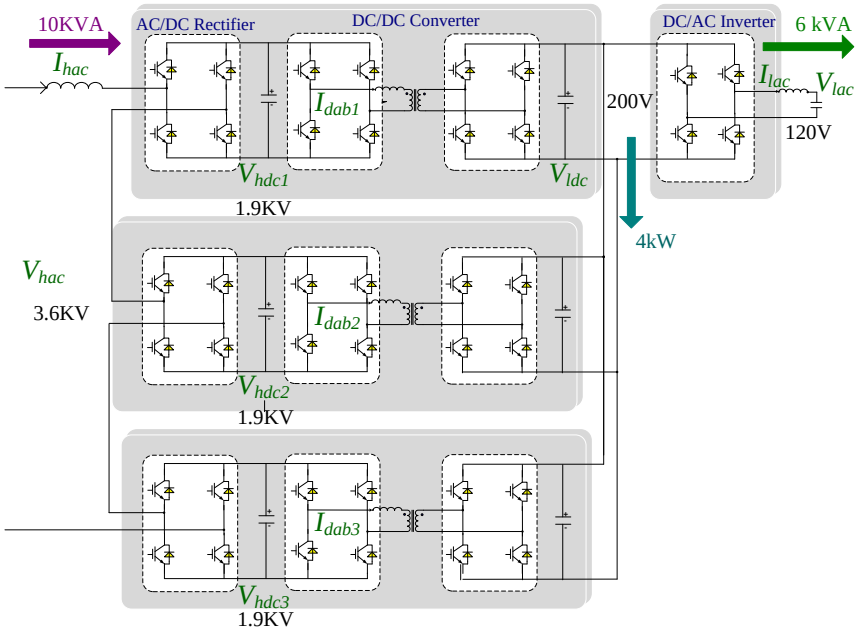


Figure 6-1 Topology and specification of a three-stage solid state transformer

Table 6-1 Parameters of the modified SST

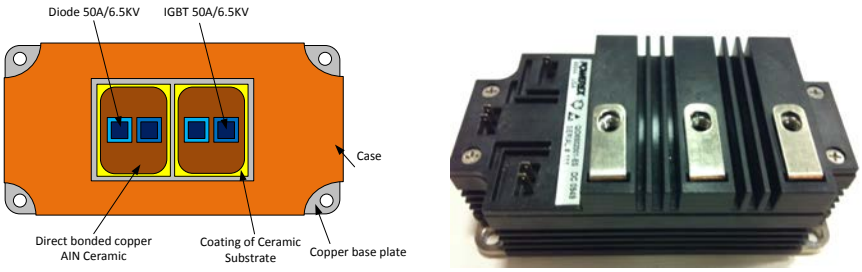
Power rating P	10kVA	Input voltage	3.6kV
input current	2.78A	High voltage DC	5.7 kV
Low voltage DC	200V	Low voltage AC voltage	120V
Low voltage DC current	20A	Low voltage AC current	50 A

The rating of the system is determined by modifying the original voltage target to one half while keep the current rating. This is because we decide to use the commercialized concept gate driver core in our gate driver design. However it is necessary to point out the same design methodology can be applied to a 7.2KV input SST unit with a higher voltage gate driver circuit.

6.2 Power devices and switching frequencies selection

It is seen that the device under consideration at the SST input side should be a high voltage and low current one. The commercially available high voltage power devices, such as ABB 6.5kV IGBT, show a minimum current of 200 A. Therefore, it is not cost-effective from design point of view. A 6.5kV IGBT dual module with anti-parallel diodes has been re-packaged. Shown in Figure 6-2 (a), two ABB 6.5kV/25A IGBT chips and two 6.5kV/50A diode chips are adopted to compose the H-bridge configuration, in which the normal wire-bonding technology is adopted. Figure 6-2(b) shows the prototype of the module. The minimum clearance distance of this package design in the air is 19 mm and the creepage distance is 78 mm, which complies with IEC-60077-1 standard. This device is adopted as the

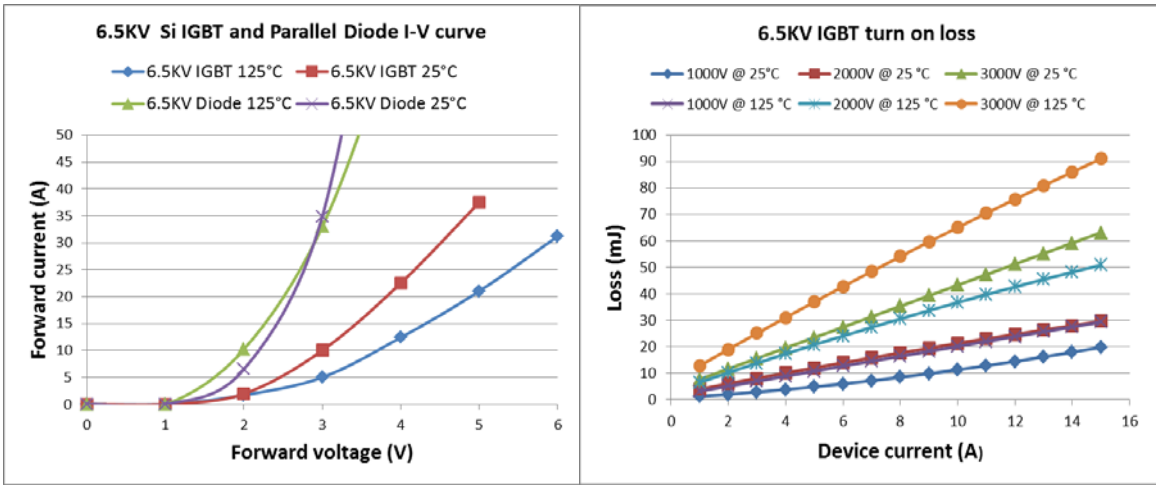
high voltage power device for both rectifier stage and primary side of the DC/DC stage. The relatively higher voltage rating is chosen for this lab prototype design in order to keep relatively larger margin.



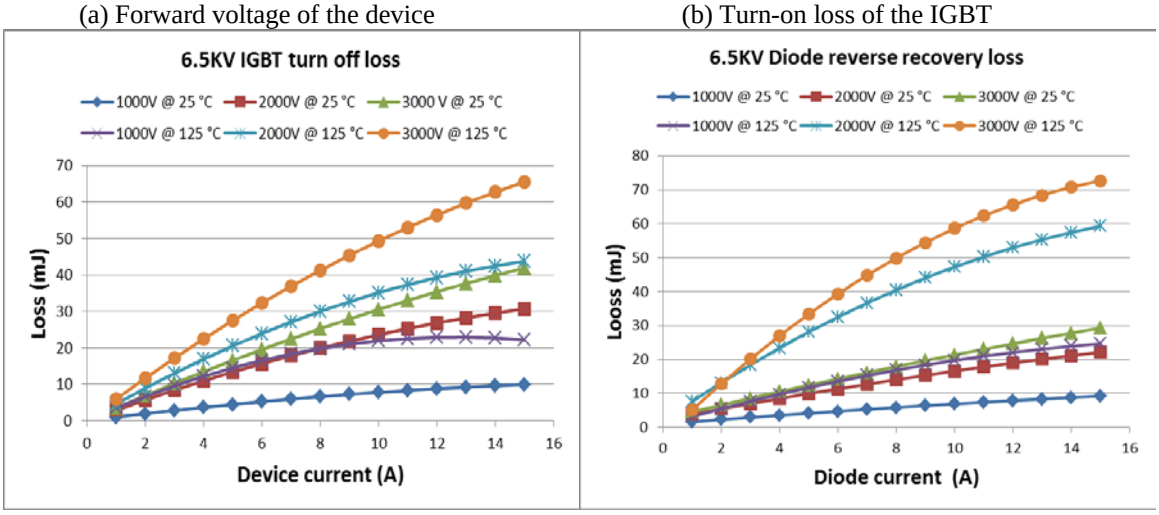
(a) Dual module layout (b) Module prototype

Figure 6-2 Re-packaged 6.5kV/25A Si IGBT module

Since this power device is not commercially available, the loss information of it is tested in the lab by using the double pulse tester, and the results are shown in Figure 6-3. Figure 6-3(a) shows the forward characters of the IGBT and anti-parallel diode under different temperatures. Figure 6-3 (b) and (c) show the switching loss of the IGBT at different operating voltages and temperatures. Figure 6-3 (d) shows the reverse recovery loss of the diode during turn-off process. The tests show that the power device losses increase with the increasing of the temperature, operating current, and voltage.



(a) Forward voltage of the device (b) Turn-on loss of the IGBT



(c) Turn-off loss of IGBT (d) Reverse recovery loss of diode

Figure 6-3 Characterization of the 6.5kV/25A IGBT

Three 600V/150A intelligent power modules (IPM) PM150CL1A060 from POWREX are selected as the low voltage side power devices. This module integrates the built-in protection and can support up to 20 kHz switching frequency. Since only two legs of each module are needed for the low voltage side of DAB converter, the third leg of the IPM module 1 and module 2 compose the inverter stage, and no additional module is needed.

The selection of the switching frequency in each conversion stage should consider the control implementation, converter size, efficiency, and thermal. From control point of view, the phase shift pulse-width modulation (PS-PWM) strategy is adopted for the rectifier stage to minimize the filter size, and this needs to accurately phase shift the carriers of each H-bridge to cancel the harmonics [105]. Also for the DC-DC stage, the interleaving concept originated from the multiphase DC/DC converter is adopted for minimizing the ripple across the output capacitor [114]. Both of these need the accurate positioning of the PWM signals. As shown later in section E, the A/D sampling and control of all three stages are implemented in the same interrupt loop of digital signal processor (DSP). The interrupt period is set as the reciprocal of the equivalent switching frequency of the inverter stage, of which the switching frequency is the highest. Therefore, the switching frequency of the inverter stage should be selected as N times to that of rectifier and DC/DC stages. In this condition, the high resolution control can be achieved for all three stages.

Generally speaking, a higher switching frequency can help reducing the size of passive components. However, the increased switching losses bring challenges to efficiency improvement and thermal design. Trade-off has to be made among different requirements. The optimal switching frequency with Si IGBT based inverter is generally chosen between 5 kHz to 20 kHz. In this design, the switching frequency of the low voltage inverter is selected to be 10.8 kHz, which is multiple times of 60 Hz line frequency. Therefore it is easy to implement the digital phase locked loop (PLL) and control algorithm. The switching frequency of the 6.5kV IGBT are generally lower than 1 kHz to limit the switching loss in the hard switching operation mode. Considering enough margin between the device current

rating (25A) and the maximum operating current (< 4A), a slight higher switching frequency may be allowed. In the final design, the switching frequency of the rectifier stage is set to 1.2 kHz considering the compromise between the loss and input filter size. The zero voltage switching (ZVS) is achieved for the DAB converter [43]. In this condition, the turn-on loss of IGBT and reverse recovery energy loss of the parallel diode will be very small. However, the turn-off loss of the DAB converter is still high due to its inherent operating principle. As shown in Fig.5, the turn-off loss is about 1/4 to 1/3 of the total switching loss for this 6.5kV/25A IGBT module, hence the switching frequency of the DC/DC stage is set to 3.6 kHz, which is 3 times of the switching frequency of the rectifier stage to keep the similar loss and thermal performance.

Table 6-2 lists the designed parameters of the components in the prototype. The design method of these parameters is given in the appendix A.

Table 6-2 Calculated parameters of the power stage

Parameter	**Value**	**Remark**
Input L filter	135 mH	15% ripple current, 0.11 pu
High voltage DC link capacitor	38μF	15% 120Hz ripple voltage
High frequency transformer	Turn ratio: 9.5:1	Equivalent duty cycle D=1
	leakage inductance: 33 mH	Maximum phase shift $\frac{\pi}{3}$
Low voltage DC link capacitor	20mF	5% 120 Hz ripple voltage
Output inverter filter	L: 1 mH ;C: 30uF	1080 Hz cut off frequency

In this chapter, the design of the major components in the high voltage side, including high voltage AC inductor, high voltage transformer, high voltage gate driver and its power supply, are highlighted and the rest components of the power stage are listed without explanation. In addition, the developed universal control platform is introduced in detail. Lastly, test results are provided for verifying the high voltage operation of the system.

6.3 High voltage and high frequency transformer design

There are some considerations for this specific transformer design. First of all, considering the high voltage IGBT adopted, the operating frequency of the transformer is set to 3.6 kHz. The performance/cost factor of the design should be as high as possible for this operating frequency. Secondly, the required inductance for power transfer is about 30 mH in this condition as shown in Table 6-2. From the system power density point of view, it is highly required to integrate this inductor into the leakage inductor of the transformer.

Several materials can be considered for the high frequency and high power transformer design, such as ferrite, nanocrystalline, and amorphous. The ferrite core has the characters of low loss while its saturation flux density is also low (0.4T). It is suitable for the applications, in which the operating frequency is in the range of more than 100 kHz. The targeted operating frequency of the high voltage transformer is 3.6 kHz as aforementioned. If the ferrite core is adopted, the size and weight of the transformer may be an issue. In addition, the ferrite core is brittle, and the mechanical strength of ferrite may not be strong enough to support the transformer structure with switching frequency of 3.6 kHz. Therefore it is not

recommended in this specific design. Nanocrystalline core achieves good performance in both the power density and efficiency. One on hand, it has a high saturation flux density, which is about 1.2T. On the other hand, the core loss of this material is also low in the range of kHz to tens of kHz. However, the cost of this material is relatively high and the off-the-shelf shape of the core is also limited to toroidal uncut tape-wound core. The leakage inductance is quite small due to toroidal core with low number of turns. Additional inductor will be needed for the DAB operation, thus sacrifice the power density. In fact, the nanocrystalline core is recommended to be used in the application where the operating frequency is higher than 10 kHz. The amorphous core has the highest saturation flux density (1.56T) among all three candidates, and the loss of the core at several kHz is acceptable for the system. These two characters provide space for optimizing the efficiency in terms of the flux density and switching frequency. In addition, the cost of the amorphous core is low and therefore it shows perfect performance/cost factor is perfect in terms of the switching less than 5 kHz. Therefore it is chosen for the design.

Three versions of the transformer prototype are designed based on amorphous core, as shown in Figure 6-5. The purpose of designing three version of the transformer is twofold: (1) verify the possibility of improving the power density of the system by using customized components; (2) verify the controller system when considering the parameter mismatch among the modules.

The design consideration and methodology of the prototype is detailed in [40]. The version 1 is based on the commercialized Metglas AMCC-1000 core and three cores are put together to compose the needed core cross section area. In order to push the power density to a higher

value, the customized core and wire are adopted for the version 2 design by keeping the same maximum flux density (0.25T). It is shown in Figure 6-4 that about 30% size and weight reduction is achieved compared with version 1. By increasing the maximum flux density (0.35T), version 3 shows the possibility of further increasing the power density, which is about 2/3 of the version 2 design. However, the higher flux density operation brings high audible noise, therefore should be considered in the design of the system. It is noted that the designed transformer prototype was initially designed for a higher voltage system, while it can be used in the presented system without modification. From this perspective of view, a more conservative and therefore compact design could be achieved with the same design methodology for the presented system. Table 6-3 shows the parameters of the designed transformer in the presented SST system. It is seen that parameters of three transformer prototype are different, and these will be used to demonstrate the voltage and current sharing capability of the presented controller.

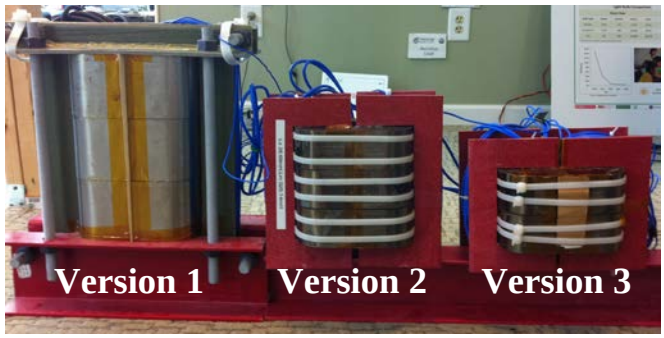


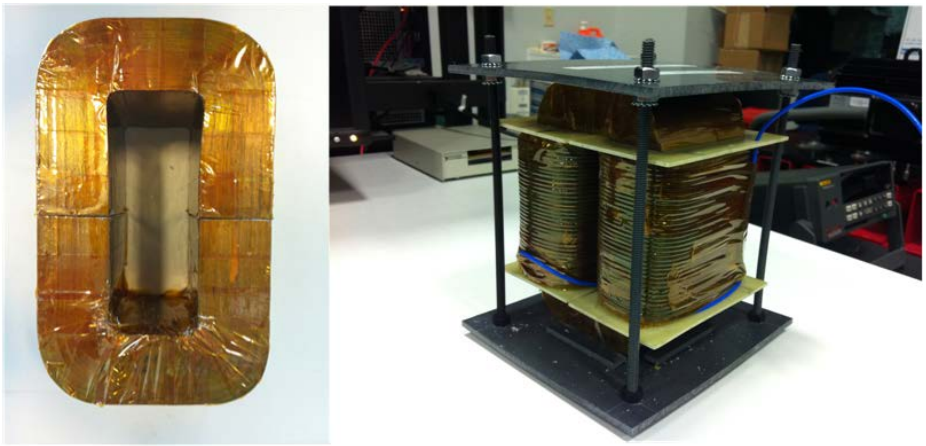
Figure 6-5 High voltage and high frequency transformer for DC/DC stage

Table 6-3 Parameters of the transformer in the SST prototype [40]

	Prototype-1	Prototype-2	Prototype-3
Core material	Metglas SA2605SA1	Metglas SA2605SA1	Metglas SA2605SA1
Operating frequency	3kHz	3kHz	3kHz
Pin	6kW	6kW	6kW
KVA	10kVA	10kVA	10kVA
Primary voltage	3.8kV	3.8kV	3.8kV
Secondary voltage	400V	400V	400V
Primary current	2.6A	2.6A	2.6A
Secondary current	25A	25A	25A
Turns ratio	9.5:1	9.5:1	9.5:1
Mag. Inductance	235 mH	468.9mH	314.2mH
Leak. Inductance	36 mH	30.3 mH	29.7 mH
Efficiency	96.76%	97.3%	97.16%

6.4 Input filter design

Considering the high inductance value and high operation voltage condition of the designed filter, three inductors are cascaded together to compose the input L filter. Therefore, the inductance for each one is about 45mH. The amorphous core is chose as the core materials due to its high saturation flux density (1.56T), low profile, low temperature and low core loss[115]. Therefore, both the copper loss and the core loss can be controlled to be low. The selected core and the one designed inductor are shown in Figure 6-6. The AMCC-1000 C core from Metglas was selected and 10 AWG (3*70/33) customized high insulation wire is used [40]. The turn number of the inductor is 120 and a 1.2 mm air gap is inserted (0.6mm in each side). The measured inductance of the designed inductor is 50 mH and the equivalent series resistance (ESR) is 0.93 Ω. Three inductors are assembled to compose the input filter. Three inductors are assembled to compose the input filter, of which the current rating is 5A (RMS) considering the efficiency and certain margin. In this condition, the maximum flux density is 1.08 T.



AMCC 1000 Amorphous core **Assembled input inductor unit**

Figure 6-6 Selected core and assembled input inductor (one unit)

6.5 Gate driver design

When the power devices operates in H-bridge configuration with high voltage DC link, the high dv/dt brings the challenge for the gate driver design. Specifically, the isolation with small coupling capacitor between upper and bottom device has to be used to reduce the common mode noise. Since this package is for 3.3 kV IGBT and is different from the standard 6.5kV IGBT, the on-the-shelf 6.5kV IGBT gate driver cannot be directly used. Therefore, a customized gate driver design is required. In the modified SST prototype, the DC link voltage is reduced to 2kV. Therefore, the concept gate driver core 2SC0535T is chosen for demonstration, as shown in Figure 6-7[116].

The 2SC0535T is a driver core equipped with CONCEPT's latest SCALE-2 chipset. It comprises a complete dual-chip IGBT driver core with selectable operating mode, fully

equipped with and isolated DC/DC converter, short circuit protection, advanced active clamping, and supply-voltage monitoring. It targets at IGBT up to 3.3kV with switching frequency up to 100 kHz. It can provide 35A gate driver current and 2×5w gate driver power. The coupling capacitor between the primary and secondary side of isolation transformer is 19 pF.

Two factors need to be taken care of when design the gate driver based on the driver core:

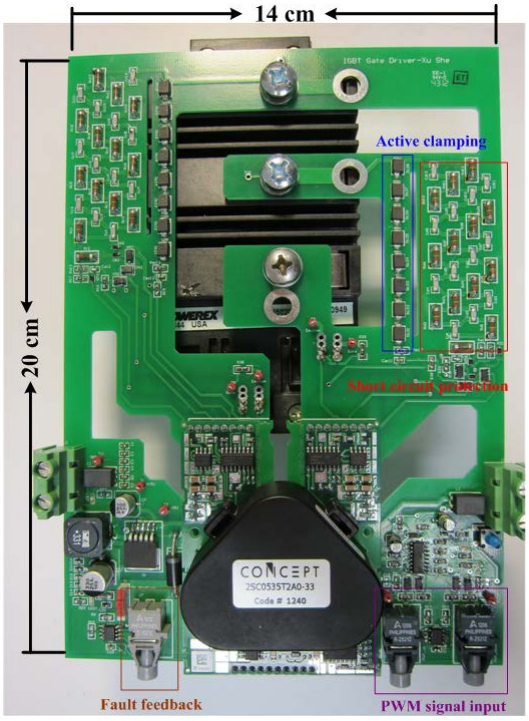
(1). The output gate channel of the driver core should be located as close as possible to the gate and source of the power devices, therefore to reduce the loop inductance;

(2). Enough creepage distance should be kept in order to withstand the high voltage operation.

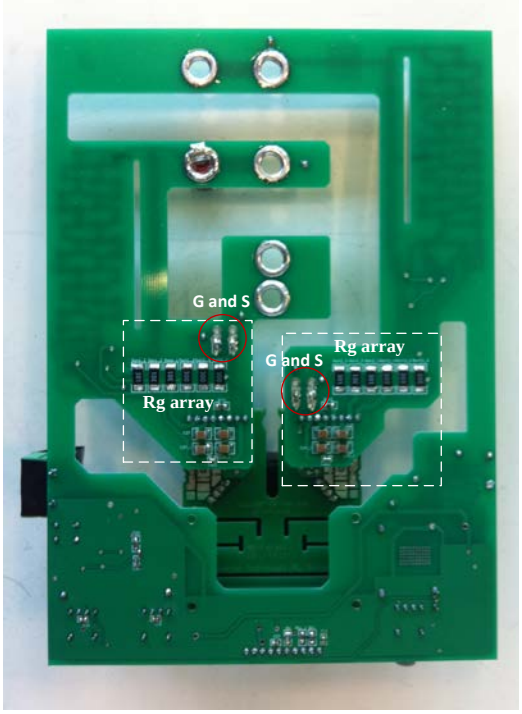
Figure 6-7 Concept gate driver core 2SC0535T [116]

A customized gate driver was designed for the high voltage IGBT used in the SST prototype based on this driver core, as shown in Figure 6-8. Figure 6-8 (a) shows the top view of the designed gate driver attached to the IGBT. The gate driver core is attached to a customized mother board, in which the active clamping circuit, short circuit protection

circuit, power supply under-voltage protection circuit, and fault indication circuit are integrated. Two PWM signals are transmitted by optical fiber from the central controller and one fault feedback signal is sent back for blocking the PWM. The slot is carefully designed in order to increase the creepage distance. Figure 6-8 (b) shows the bottom view of the designed gate driver. The gate resistor array is placed as close as possible to the gate of the device in order to minimize the loop inductance. The external turn-on resistance is 100Ω and the turn-off resistance is 10Ω.



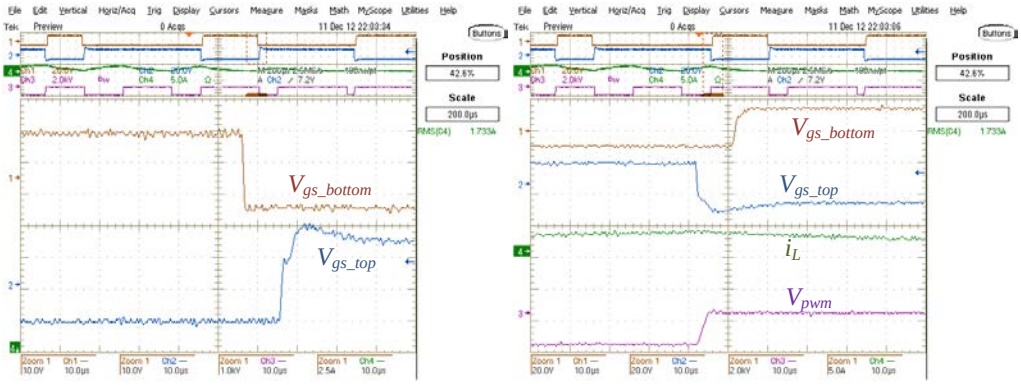
(a) Top view of the gate driver



(b) Bottom view of the gate driver

Figure 6-8 Designed high voltage IGBT gate driver based on Concept gate driver core 2SC0535T

The designed gate driver was tested in a single phase H-bridge inverter with DC link setting as 2kV. The modulation index 0.8 and the inductive load (470Ω, 56mH) is adopted. The dead time is set to 8μs. The test results are shown in Figure 6-9. It is seen that with the designed gate driver, the inverter can operate well in the high voltage operation condition. The cross-talking between the two devices is very small.



(a) Turn on of the top devices (b) Turn on of the bottom devices

Figure 6-9 Switching performances of the IGBT driven by the designed gate driver

6.6 Power supply for the IGBT gate driver in a cascaded structure

In the presented SST topology, three H-bridge converters are cascaded to compose a multilevel rectifier. The cascaded structure brings challenges for the design of IGBT gate driver power supply since devices at the top H-bridge will see a 6kV potential voltage if all the IGBTs are powered by the source with the same ground. In this condition, both the insulation level of the single IGBT gate driver is not enough and the coupling capacitance is higher than the required (recommend to be less than 2pF). The best solution to solve this

problem is to power the IGBT from the local DC link, shown in Figure 6-10. In fact, system method has been adopted widely in HVDC system using the VSC technology. The challenge for this method is to design a very high step-down ratio DC/DC converter. In our design case, this should be from 2000V to 15V. This method is suitable for a commercial product design when all the hardware and software designs are fixed, meaning that the input voltage of the high step-down ratio DC/DC converter is also fixed for both start-up threshold and steady state.

Since it is the laboratory prototype that we are designing is for function verification purpose, the DC bus may be much lower than desired threshold voltage during the test. In addition, the DC voltage may even unstable in the tuning of the control parameters. In this condition, a simple and reliable method to power the IGBT gate driver for the test purpose is highly required.

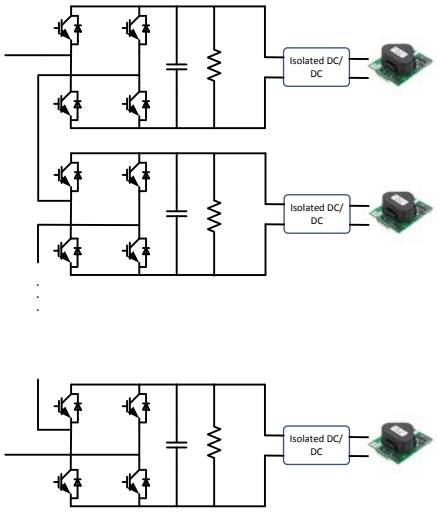


Figure 6-10 IGBT gate driver power supply solution in cascaded structure

Figure 6-11 shows the alternative approach to power the IGBT gate driver for the test purpose. Basically, the idea is to use an ultra-isolation line frequency transformer to float the gate driver for each H-bridge converter. A normal AC/DC power supply can then be used to power the IGBT gate driver. This ultra-isolation transformer should be able to achieve isolation higher than 6kV and with a very small coupling capacitor. By doing such, the gate drivers for each H-bridge will only “see” the 2kV DC link without being interrupted by the common noise comes from the other bridges.

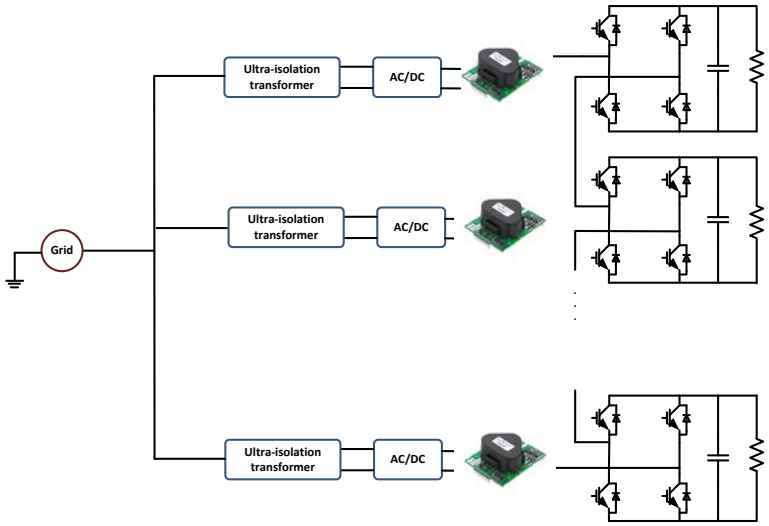


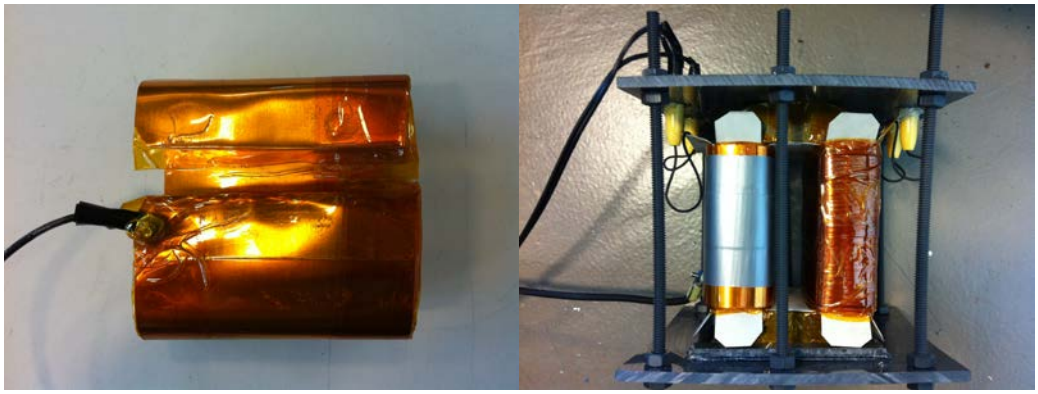
Figure 6-11 Alternative solution for power the IGBT gate driver by using ultra-isolation line frequency transformer for test purpose

In order to achieve this, three isolation transformers are designed and assembled. The amorphous core is used due to the line frequency operation of the transformer. In order to achieve the high isolation and low coupling capacitance, two design considerations are taken in to account:

(1) The distance between the primary and secondary side winding should be located far away from each other.

(2) Shielding layer is inserted for minimizing the coupling capacitance.

Figure 6-12 shows the designed 0.9 turn copper shielding layer and the assembled isolation transformer. The amorphous AMCC-400 core is adopted. AWG#22 wire is used for both primary side and secondary side winding and the turn-ratio are set to 430 and 450 respectively, considering 5% regulation rate[38]. The copper shielding layer is wound in the primary side of the transformer and it is connected the ground. By doing such, a large capacitor is formed between the primary side and the ground. Therefore, most of the common mode current flows directly to the ground without going to secondary side of the transformer. Certain margin is kept in the design of the transformer and the power rating for this transformer is 100W, which is far more than what IGBT gate driver needs. The isolation of the transformer is tested under 10kV DC between primary and secondary side winding without observing any insulation problem. We do not measure the coupling capacitance however it is estimated to be at least lower than 0.005pF due to the combination of separate winding and shielding techniques.



(a) 0.9T shielding layer connected to ground (b) Assembled isolation transformer

Figure 6-12 Ultra-isolation transformer for the IGBT gate driver power supply

The assembled isolation transformer is tested in the rectifier stage with only current loop, which easier the test procedure. A suitable current reference is chose to boost the DC voltage to be higher than the maximum value of the input voltage. Figure 6-13 shows the test results, in which the input of the rectifier stage is 3.7kV, the DC bus voltage is about 6kV (2kV for each H-bridge), and the power rating is about 8 kW. The PWM voltage in this condition is clear, indicating that the PWM signal is not disturbed by the common mode noise. Therefore, the designed ultra-isolation line frequency transformer can provide good immunization to the common noise in the presented system.

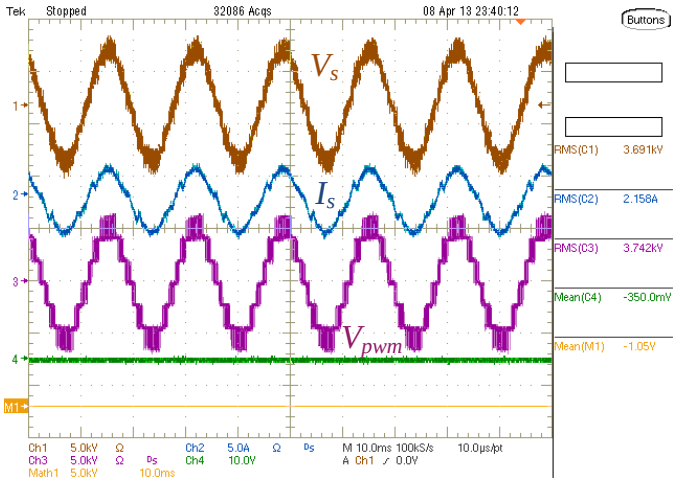


Figure 6-13 Test results of the rectifier stage with ultra-isolation transformer
(3.7kV input voltage, 6000V DC link)

6.7 Other components

Other components in the final power stage design are given in Table 6-4, no explanation is given since these are all on-the-shelf product.

Table 6-4 Other components in the final power stage design

High voltage DC link capacitor	Two 75uF/2250V film capacitor from Vishay connected in series
High voltage sensors (For input voltage and high voltage DC links)	DV4200/SP4 high voltage sensor from LEM
Low voltage DC link capacitor	Four 5600uF/450V electronic capacitors from Vishay connected in parallel
Low voltage power devices	PM150CL1A060 IPM Module from POWREX
Output inverter filter	L: 1mH/40mΩ (Magnetics Kool Mu core) C: 30uF/600V from GE capacitors
Low voltage sensor (for low voltage DC link and output AC voltage)	LV25-P voltage sensor from LEM
Current sensor (for both input and output current)	LA100-P current sensor from LEM

6.8 Universal control platform design

As mentioned in the previous chapters, the SST is the energy hub in the presented FREEDM systems and also an attractive active interface in the future distribution system. An intelligent control platform with communication functions is designed for the SST in the smart grid environment. Figure 6-14 shows the signal flow path of the presented control platform. Basically, the command will be generated by the central control room and transmitted to the ARM board by wireless communication. Then, this command will be delivered to the local DSP+FPGA control board, in which the switching sequence of the SST is generated. Further, the interface board sends the PWM signal optically to the SST. In the reversed signal path, the status of the SST is fed back to the central control room for monitoring and control.

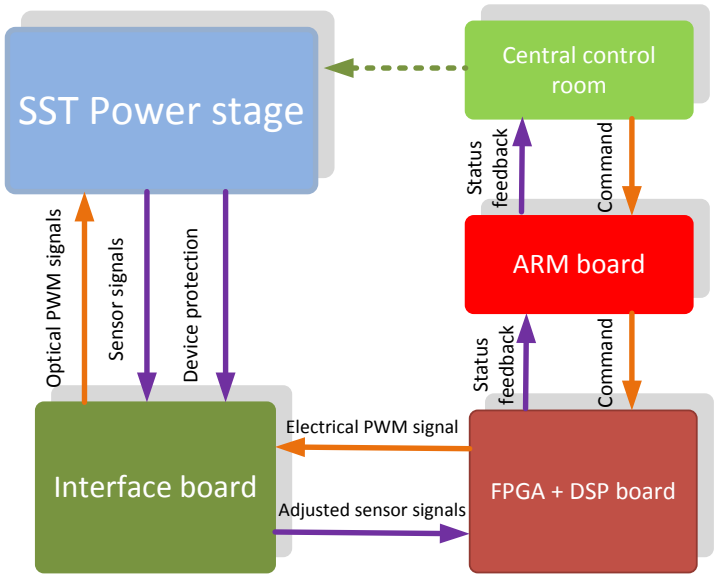


Figure 6-14 Universal controller signal flow path

A highly flexible and compact universal control hardware platform is designed for the SST prototype to operate as the energy hub, as shown in Figure 6-15. It consists of three major components, namely, interface board (top), local controller board (middle) and ARM communication board (bottom). These three components are stacked on top of each other to form a compact and reliable structure.

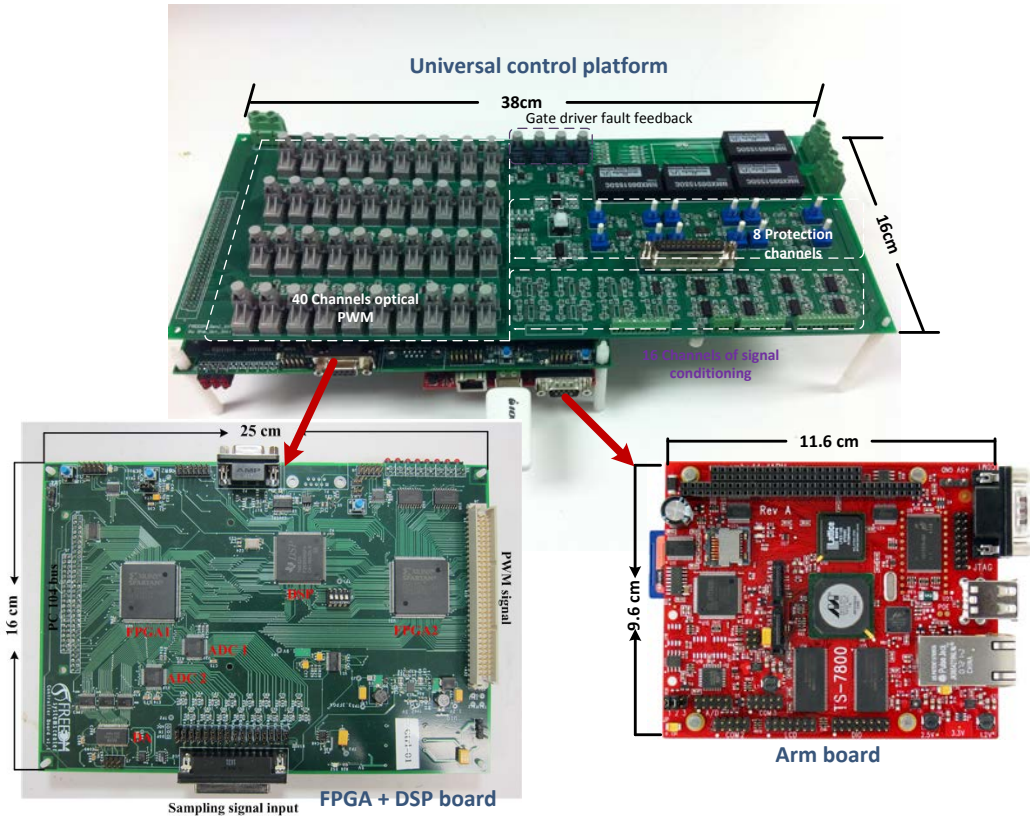


Figure 6-15 Universal control platform for SST prototype

The interface board is responsible for signal processing, hardware protection, and electrical to optical PWM conversion. 40 channels of optical fiber PWM are available to transmit switching signal to power devices. In addition, there are 16 channels of analog

conditioning circuits to adjust the signals from the sensor to the desired range for analog to digital conversion. 8 channels of hardware protection are embedded in the interface board. Fault signals are generated by comparing the outputs of the conditioning circuit with the preset threshold values, and to turn off the PWM signal quickly. The gate driver protection signals are also fed back to the interface board to turn off all the PWM signals during the gating fault.

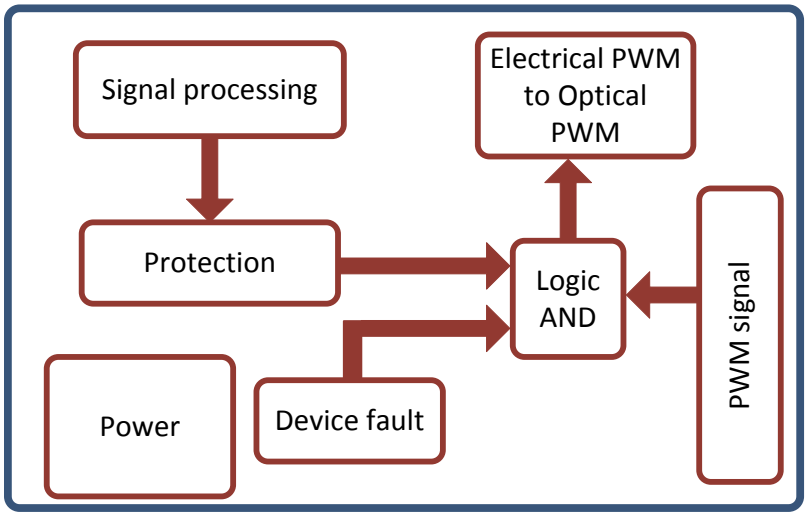


Figure 6-16 Functional diagram of interface board

The control algorithm and PWM synthesis is implemented in local controller board. TI TMS28335 DSP and two Xilinx Spartan XC3S400 FPGAs are adopted as shown in Figure 6-15. The major function of FPGA #1 is to synthesize the PWM signal and send the interruption signal to the DSP to enable control algorithm. The task of FPGA #2 is two-fold: on one hand, it is used to generate AD signal and transmit the digital signal to the DSP. On

the other hand, FPGA #2 also communicates with ARM board through PC104 interface in a fast and reliable fashion. Furthermore, two AD7606 from analog device with total 16 analog-to-digital conversion channels are available in this local control board for precisely data acquisition. DA chip (DAC7744) is also designed for debugging purpose.

The communication between the central control room and DGI is achieved by using the ARM board TS-7800, which features Marvell 500MHz ARM9 SBC, providing gigabit Ethernet. Both wire/wireless communications can be realized. In addition, the web-based human machine interface (HMI) is designed for setting the command and monitoring the status of the system over the communication link, as shown in Figure 6-18. The authorized user can log on the system to operate the SST. Therefore, the SST together with the DGI can be applied into the smart grid environment [117].

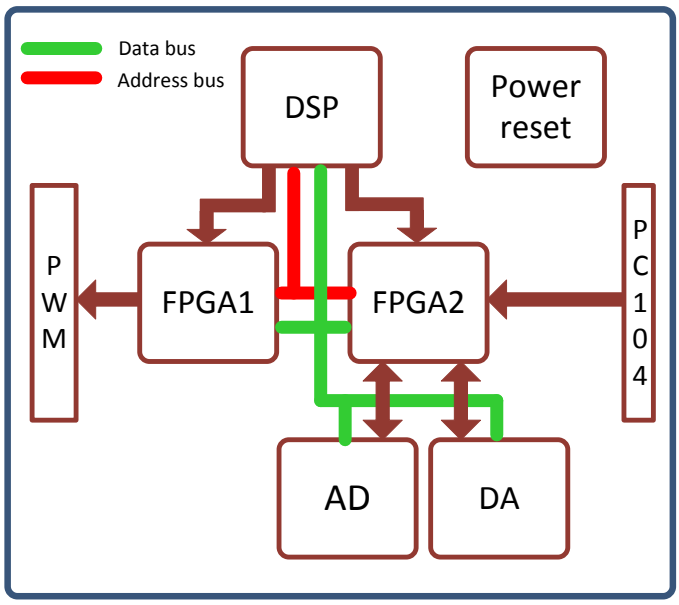


Figure 6-17 Functional diagram of local controller board

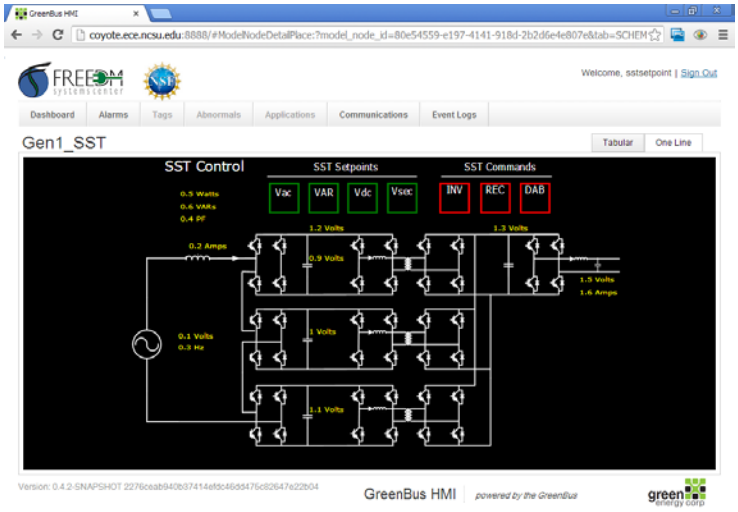


Figure 6-18 HMI interface for control and monitoring

6.9 Hardware of the prototype and experiment set-up

Based on the designed components aforementioned, the SST hardware has been built. Figure 6-19 shows the 3-D layout of the prototype. From the left to the right are the input cascaded multilevel rectifier stage, high voltage DC link, high voltage side of the DC/DC stage, high frequency transformer, low voltage side of the DC/DC stage, and inverter stage.

The hardware has been built and this unit is shown in Figure 6-20. The size of the SST prototype is 72×30×10 inches. A wire is used for the high voltage DC link due to the small current rating while a two layer copper bus bar is designed for the low voltage side DC bus. An universal optical to electrical PWM interface board is put on the low voltage bus bar to drive the low voltage side IPM. All the high voltage sensors are mounted on the side of the enclosure.

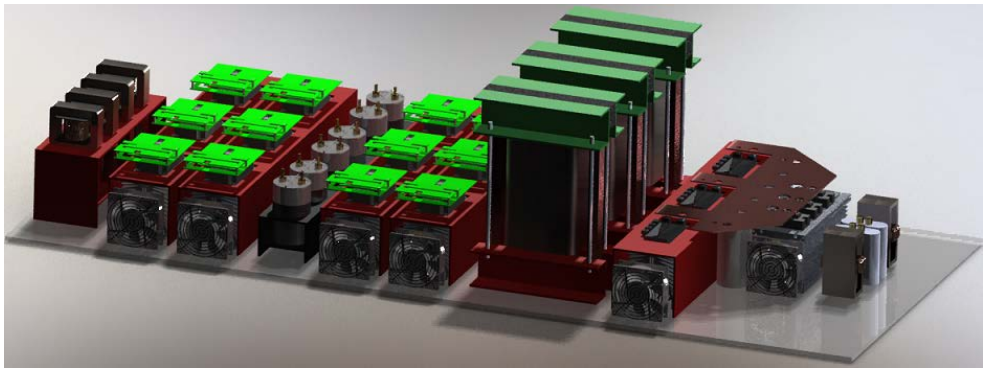


Figure 6-19 3-D layout of the SST prototype

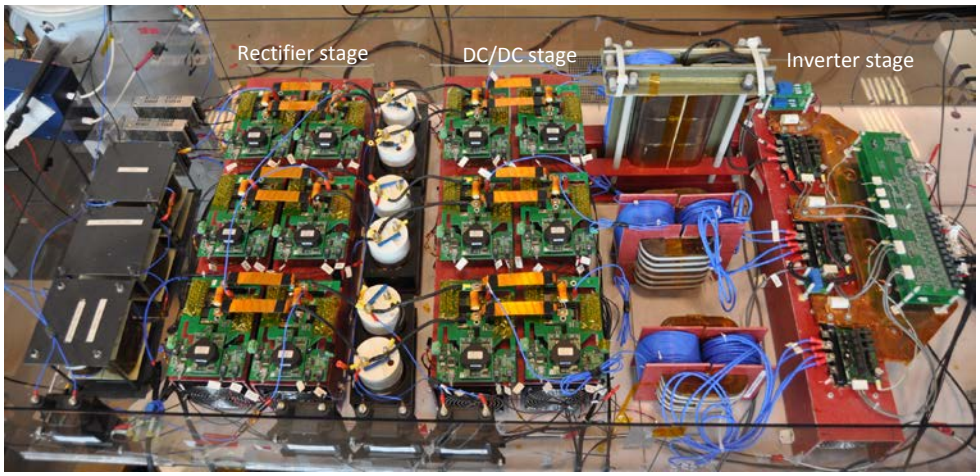


Figure 6-20 Assembled SST prototype

Figure 6-21 shows the test set-up for the experiments. In order to generate a high voltage input for the SST, A 25kVA, 120-7.2kV single phase pole mounted distribution transformer is connected to the 20kVA VARIAC. By adjusting the output voltage of the VARIAC, a voltage ranges from 0-7.2kV can be obtained. A 120/240V, 20kVA pure resistive load bank is connected at the low voltage output AC side and a resistive load bank is connected at the low voltage output DC side. The command of the SST is set at the central control desk and is

sent to the local control board through the WIFI. The key operating parameters of SST, such as voltage, current, and power, are monitored in the central control desk as well.

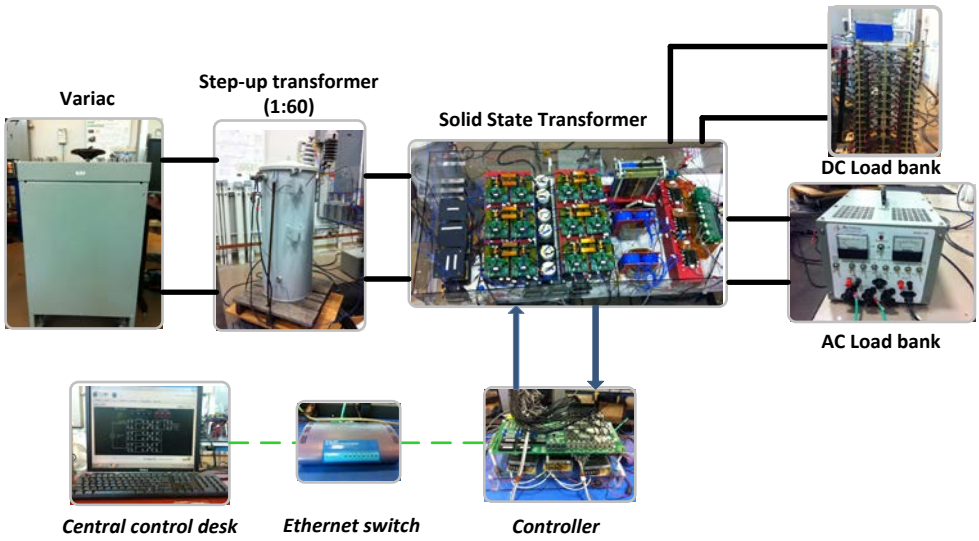


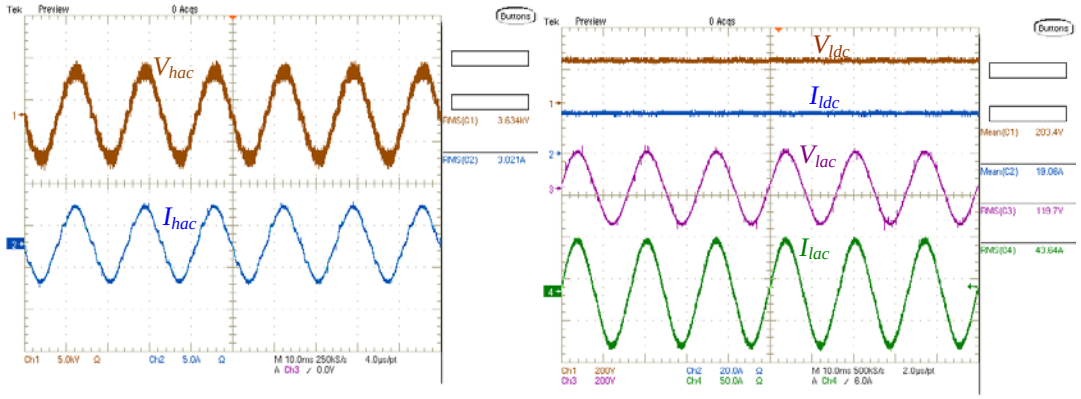
Figure 6-21Test set-up of SST

6.10 Experimental results

6.10.1 Steady state operation of SST

Figure 6-22 shows the steady state operation waveforms of the SST prototype. The input voltage is about 3.6kV and the load power is about 9kW, of which the load at the low voltage AC port is about 5.2kW and the load at the low voltage dc port is about 3.8kW. It is seen from Figure 6-22 (a) that the input current is in phase with the voltage, indicating the unity power factor operation. Figure 6-22 (b) shows the voltage and current at both AC and DC

low voltage port. The low voltage DC bus is regulated to about 200V and the low voltage AC output is regulated to 120V.

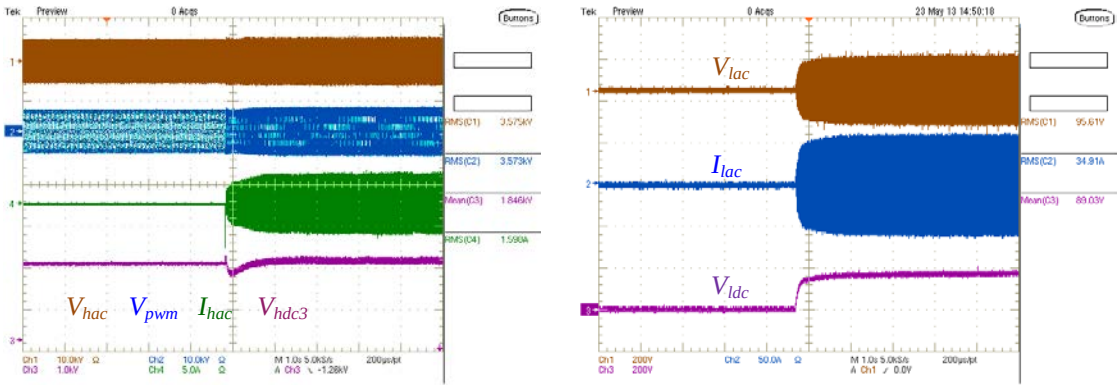


(a) Input voltage and current (b) Output voltage and current: AC and DC

Figure 6-22 Steady state operation of SST

6.10.2 Start-up of the SST

It the test, we do not implement the pre-charge of the prototype, and the input voltage increases gradually to the rated value. Before the start-up, all the PWM signals are blocked and the rectifier stage of the SST operates at the diode-rectifier mode. A specific start-up process is designed for the SST prototype considering the interactions among each stage. The start-up process of the SST is shown in Figure 6-23, in which the PWM control is enabled for the all three stages. As can be seen from Figure 6-23 that the load power increases gradually and there is a dynamic regulating process for the high voltage DC bus. Nevertheless, the start-up for all three stages show satisfied overshoot injection capability.



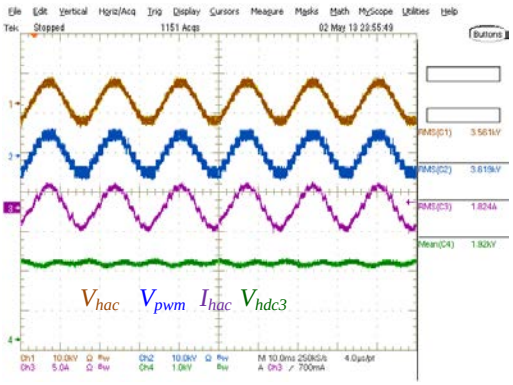
(a) Input voltage, current, PWM voltage, and High voltage DC link 3

(b) Output AC voltage and current and DC voltage

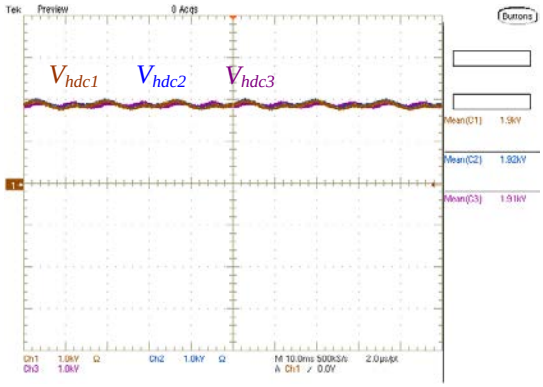
Figure 6-23 Start-up of the SST

6.10.3 Verification of Voltage and current sharing of SST

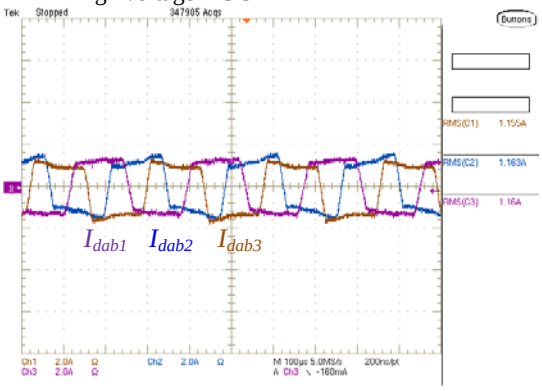
Figure 6-24 shows the steady state experimental results of the presented SST topology. The input voltage is 3.6kV and the output voltage is 120V. The load power condition is about 5.2kW, which is connected to the inverter side. Figure 6-24 (a) shows the input voltage V_{hac}, PWM voltage V_{pwm} , input current I_{hac}, and high voltage DC link3 voltage V_{hdc3}. It shows that the system operates at unity power factor. Originally, the input voltage of the SST is adjusted to 3.62kV. After the start-up of the SST, the input voltage is pulled down to 3.56kV due to the high output impedance of the system. Figure 6-24 (b) shows the three DC link voltages, which are identical and regulated to about 1.9kV. Slight steady state regulation error is observed in the test, which may be caused by either the sensor error or PI regulator. However, this small error is acceptable for this high voltage application.



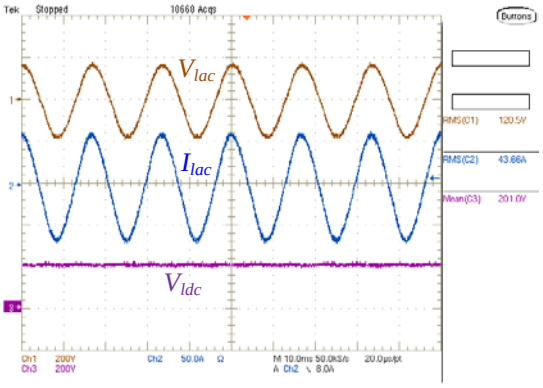
(a) Input voltage, current, PWM voltage, and high voltage DC 3



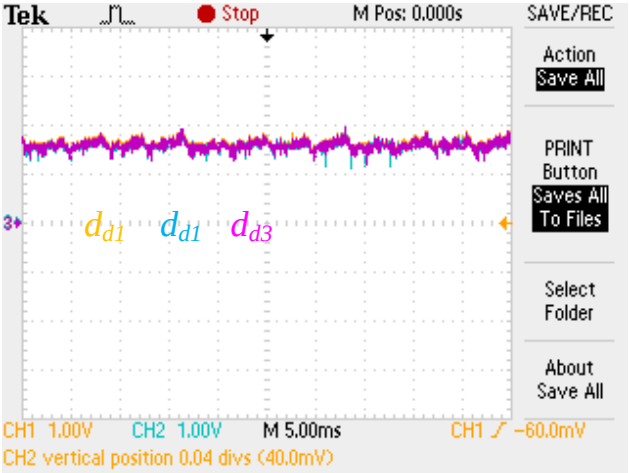
(b) High voltage DC



(c) Currents in the DAB converters



(d) Output DC voltage, AC voltage and current



(e) d-axis duty cycle of the rectifier stage

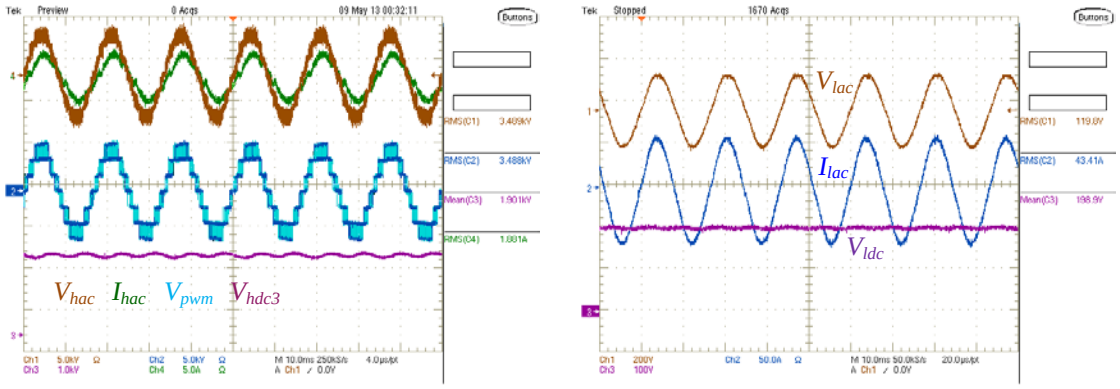
Figure 6-24 Experimental results for 3.6kV-120V, 5.2kW load condition

Figure 6-24 (c) shows the three DAB currents. With the current balance method proposed in Chapter 5, the RMS value for three currents are 1.16A, 1.163A, and 1.155A, respectively. Therefore, the power transferred in each DAB converter is almost same. The shape of the transformer are not the same because the turns ratio of each transformer may not be exactly equal to each other, however this evidences that the power can be balanced even with different current shapes caused by difference of the turns ratio. Figure 6-24 (d) shows the regulated low voltage DC link V_{ldc} , output AC voltage V_{lac}, and output AC inductor current I_{lac}. The low voltage DC link is regulated to 200V and the output voltage is regulated to 120V. Figure 6-24 (e) shows the active duty cycle components of the rectifier stage observed by using the D/A port in the local control board. All three duty cycles are the same in the steady state, verifying the proposed current sensor-less current balance controller.

6.10.4 Reactive power support to grid

The reactive power regulation capability of SST is also demonstrated, as shown in Figure 6-25 and Figure 6-26, in which the inductive mode operation and capacitive mode operation of SST are depicted respectively. The SST transforms the voltage from 3.6kV to 120V and the load is about 5.2kW at the AC side. In Figure 6-25, the reactive power at the high voltage side is set to 2kVar, while the value is set to -2kVar in the case of Figure 6-26.The input voltage in Figure 6-25 is pulled down to 3.49kV due to the high output impedance of the step-up transformer used and the inductive mode operation of the system. In Figure 6-26, the input voltage is about 3.6kV, which is higher than the one when with unity power factor operation (3.56kV), due to the capacitive mode operation. It is demonstrated from the

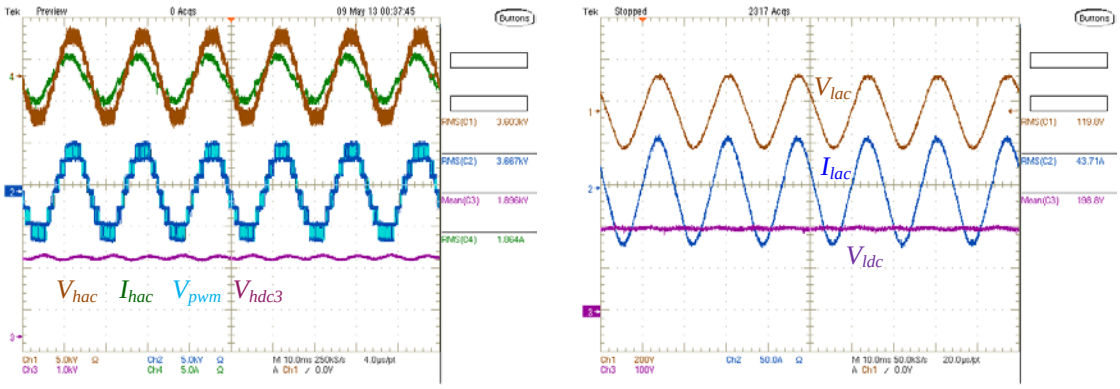
experimental results that the designed SST can provide the desired reactive power to the grid, therefore can potentially enhance the grid voltage profile.



(a) Input voltage, current, PWM voltage, and high voltage DC 3

(b) Output DC voltage, AC voltage and current

Figure 6-25 Inductive mode operation of SST



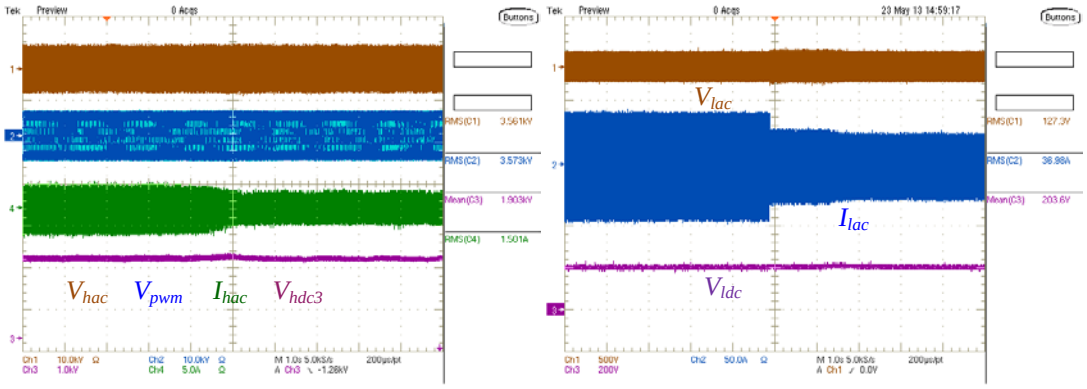
(a) Input voltage, current, PWM voltage, and high voltage DC 3

(b) Output DC voltage, AC voltage and current

Figure 6-26 Capacitive mode operation of SST

6.10.5 Load change operation

In order to demonstrate the voltage regulation capability of the designed SST prototype and the control system, the load is changed from 5.2kW to 3kW, as shown in Figure 6-27. Figure 6-27 (a) shows the dynamic response at input side, in which the input current also drops due to the decreased load condition. Figure 6-27 (b) shows the low voltage DC link V_{ldc} , output AC voltage V_{lac}, and output AC inductor current I_{lac}. Due to the load change, the output AC inductor current drops immediately. However both the AC and DC output voltage are still regulated to the desired value with very small dynamic response. Therefore, the load disturbance rejection capability of the SST is verified.



(a) Input voltage, current, PWM voltage, and high voltage DC 3

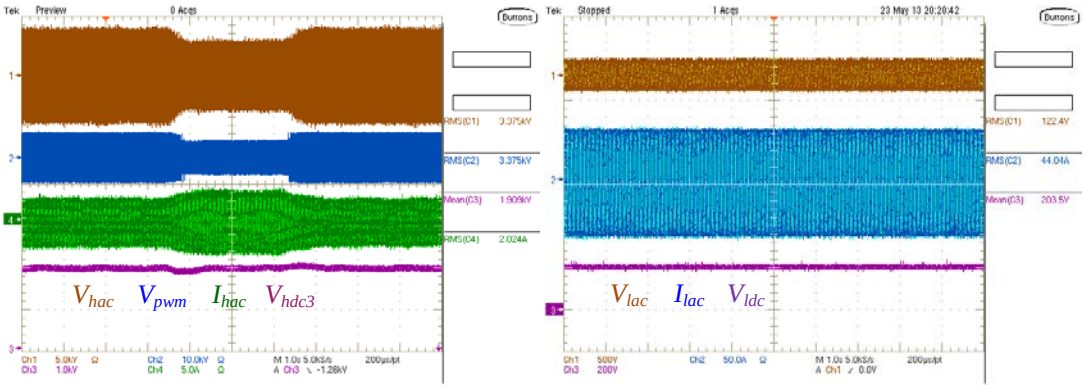
(b) Output DC voltage, AC voltage and current

Figure 6-27 SST operation under load change: 5.2 kW-3kW

6.10.6 Input voltage sag operation

Another distinguished advantage of the presented SST topology compared with the normal transformer is the source disturbance rejection capability. Figure 6-28 shows the 25% voltage

sag test of the designed SST prototype and the AC load is 5.2kW. Shown in Figure 6-28 (a), the voltage sag is created by adjusting the output voltage of VARIC and it lasts for 3s. Since the load condition is kept the same, the current increases during the voltage sag. Figure 6-28 (b) shows the low voltage DC link V_{ldc} , output AC voltage V_{lac}, and output AC inductor current I_{lac}. All the waveforms keep the same during the voltage sag process because of the closed-loop regulation and constant load condition. Therefore, the input voltage sag will not affect the power supply quality of the output voltage, indicating a strong source disturbance rejection capability of SST compared with traditional transformer.



(a) Input voltage, current, PWM voltage, and high voltage DC 3

(b) Output DC voltage, AC voltage and current

Figure 6-28 SST voltage under input voltage sag (25% voltage sag)

6.10.7 Efficiency of the SST

Figure 6-29 shows the efficiency of the SST prototype. Since the SST is for the smart grid application, in which both AC and DC outputs are available, the efficiency is recorded by putting loads at both AC and DC ports and the system operates as a three-port converter.

In the first three recorded points, only DC load is connected to the SST and gradually increases to 4 kW. The efficiency of the system is around 92%. For the last five recorded points, DC load is kept the same and AC load is gradually increased to 6 kW, and the overall efficiency of the system ranges in 84% to 88% because of the additional inverter stage.

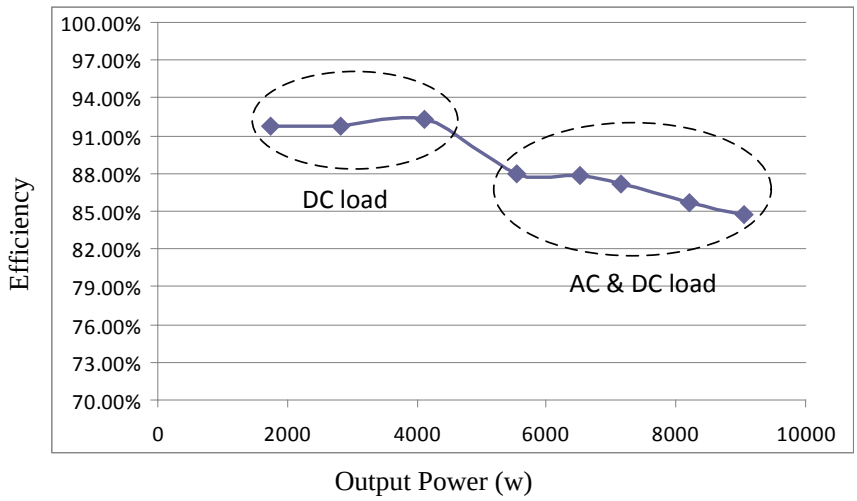


Figure 6-29 Efficiency of the SST prototype

6.11 Discussion of the design

(1).Although the 3.6kV/10kVA voltage and power rating is not a standard value in the distribution system of US, we design this prototype for conceptual demonstration at the university-based laboratory. However, the higher voltage and power rating system can be designed based on the presented design methodology considering the modular structure of the system.

(2).The size and weight of the designed prototype is apparently larger than that of the conventional transformer. This is understandable because of the relatively small power rating of the lab prototype for demonstration purpose. In fact, the benefits of reducing the size and weight of the system can only be achieved when the proportional of the transformer is much larger that of the rest parts, including the power devices, auxiliary circuits, and etc. As the power increasing, the size and weight increasing rate of transformer will be faster than the rest parts, therefore the size the weight reduction targets can be achieved.

(3). The efficiency optimization of the power stage could be studied in the future by choosing optimized switching frequency, better magnetic components (such as nanocrystalline core), and etc. It is also expected that the potential efficiency of the SST technology will be much higher (>97%) if targeted at MW level design.

6.12 Conclusion

This chapter presents the system design and performance demonstration of a 3.6kV-120V/10kVA solid state transformer lab prototype for smart grid application. The hardware design of the SST power stage is presented to fulfill the key functions of the SST. In addition, the smart controller platform is designed to enable the application of the SST in the smart grid environment, in which the communication should be combined with the devices of the system. Several tests are conducted and experimental results are given to demonstrate the key characters of the designed SST system, including: (1) Var compensation; (2) Voltage regulation; (3) Source disturbance rejection.

Chapter 7 Solid State Transformer Interfaced Wind Energy Conversion Systems

7.1 Introduction

Given the present world energy state of affairs, it has become apparent that there is an immediate need for a concrete solution to its looming shortage, where wind energy has raised as a perfect solution thus far. In fact, since 2004, wind energy deployment has risen dramatically. Shown in Figure 7-1, global installed capacity increased from 94 GigaWatts (GW) at the end of 2007 to 283 GW at the end of 2012, at an average annual growth rate of nearly 25% [118],[119], [120].

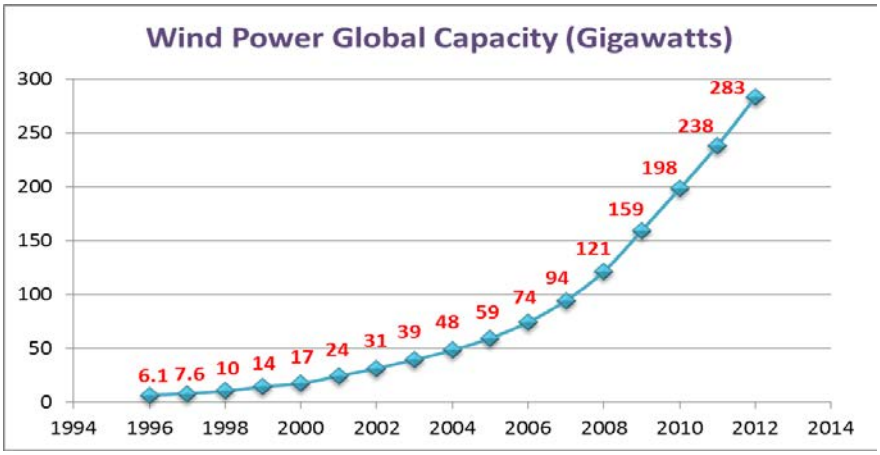


Figure 7-1 Global cumulative installed wind power capacity from 1996 to 2012 [118]

Wind power is an uncontrollable resource, which when combined with the nature of wind induction generators like the fixed-speed squirrel cage induction generator, makes for a

challenging integration of large WFs into the grid, especially in terms of stability and power quality [121]. To address this issue, utilities generally need to install reactive power compensation devices, such as static compensators (STATCOM) [121], [122], [123], [124], [125], [126], [127], [128]. Additionally, a large step-up power transformer is necessary to interface the low voltage wind generator to the distribution system, as well any STATCOM used in the system.

SST is considered as the promising candidate for the applications where low frequency transformers are dominating, such as traction/locomotives, solar/wind farm, charge station, and smart grid, for reducing the volume and weight of the system[58], [68], [70], [74]. In all the previous applications, only the benefit of reducing volume and weight of SST is considered. Although it is known that SST may provide the reactive power compensation capability, no literature has explored the SST in these applications, especially in the wind energy systems with reactive power compensation in addition to the solely voltage-conversion functionality. In addition, some of the previous SST topologies cannot fulfill the reactive power compensation due to lack of DC links [70]. Considering the wind generation system architecture and function, that of a STATCOM and power transformer, may be inherently embodied by the SST, thus makes it an attractive alternative to interface wind energy system into the grid, which is the key concept explored in this work. Specifically, this chapter contributes to looking at the advantages and possibilities offered by SST-interfaced wind energy systems, focusing on their integrated active power transfer, reactive power compensation capability, and voltage-conversion functions[129], [130]. To this end, a wind energy system with the squirrel-cage induction generator is studied as an example with

comparison to the conventional wind energy system architecture. Further, this chapter addresses the challenges for such a system: how to design a high voltage and high power SST for wind energy system. Correspondingly, a modular high voltage and high power three-phase SST topology is presented for this application with its basic single-phase building block analyzed in detail. Scaled down experimental results with single-phase SST prototype are presented for validation purposes of the integrated functions of active power transfer, reactive power compensation, and voltage-conversion. Lastly, Cost issue of the SST is also covered in the chapter[129], [130].

7.2 System Description

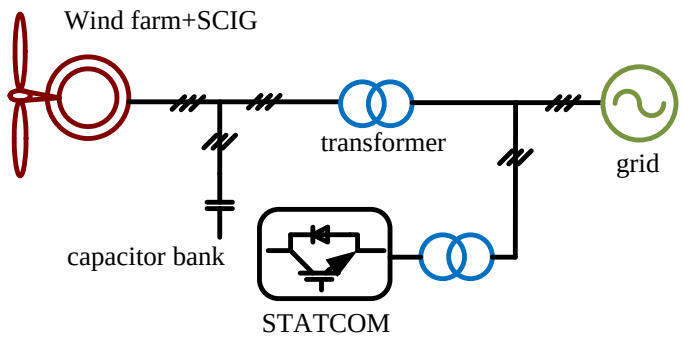
7.2.1 Wind generation systems overview

Several techniques are used to convert wind energy into electric energy, but the most popular and widely used is based on the induction generator. Presently, there are three main wind farm architectures, namely squirrel-cage induction generator (SCIG) based wind energy system [131], doubly-fed induction generator (DFIG) based wind energy system[132], and directly driven synchronous generator (DDSG) based wind energy system [133], shown in Figure 7-2. Figure 7-2 (a) describes the wind farms (WF) with SCIG, which is directly coupled with the grid and thus the most economical solution. The slip, and the resultant rotor speed of the generator, varies with the amount of power generated, thus a capacitor bank is generally placed in the terminal of the wind generator for the local reactive power compensation, which is necessary for the operation of this system. Figure 7-2 (b) shows the

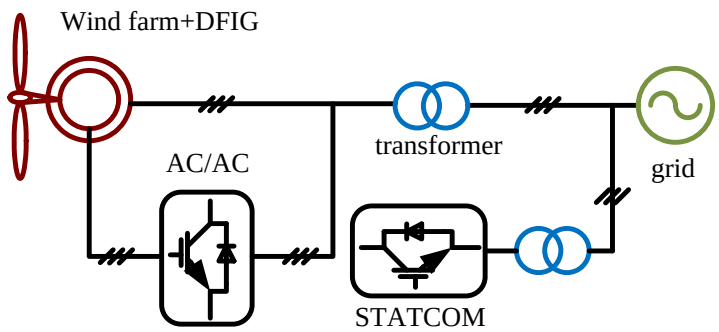
WF with DFIG, which employs partial power back to back converters to decouple the mechanical and electrical rotor frequencies. Figure 7-2 (c) lastly shows the WF with DDSG, which uses full power back to back converters that totally decouple the generator from the grid. The new WFs are tending to use DFIG or DDSG connected to grid with back to back converter; nevertheless, more than half of the existent WFs are still based on SCIG.

The nature of WFs is that their operation is highly dependent on the active and reactive power transferred to the grid, a condition normally reflected by the fluctuation of voltage magnitude at the point of common coupling (PCC). This sensitivity is exacerbated in the case of SCIG, since this type of generator is an inherent consumer of reactive power [119]. Additionally, in the case of faults causing a voltage drop at PCC, the induction generator speeds up consequently due to unbalance between the mechanical shaft torque and the generator's electromagnetic torque, in which case it draws more reactive power acting as a positive feedback contributing to the grid destabilization and PCC voltage collapse [122],[131].

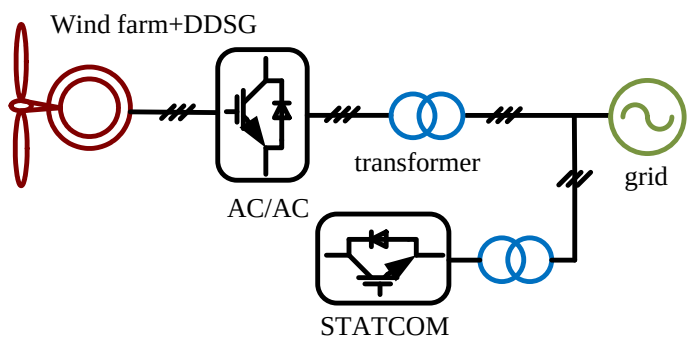
As seen, the modern power system has to confront some major operating problems such as voltage regulation, power flow control, transient stability, and damping of power oscillations, etc. Reactive power compensators, such as static compensator (STATCOM), are hence good solutions for regulating the PCC voltage [121], [122], [124], [125], [127], and it is also shown in Figure 7-2.



(a) WF with squirrel-cage induction generator



(b) WF with doubly-fed induction generator



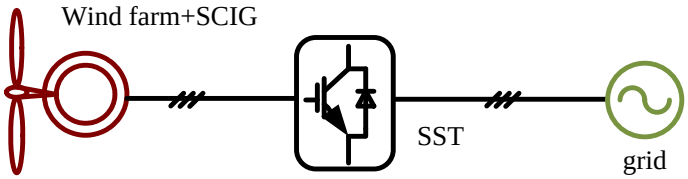
(c) WF with directly-driven synchronous generator

Figure 7-2 WFs with induction generator interfaced by normal transformer

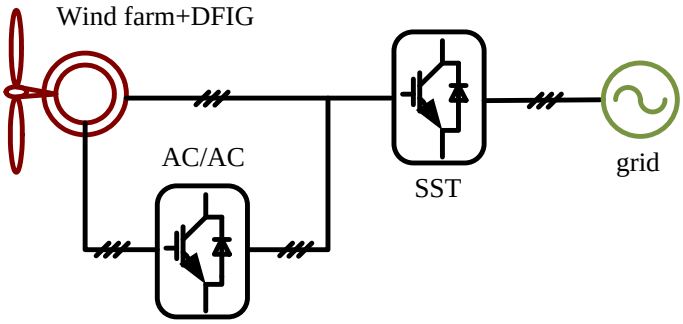
The downside of these WFs however is the use of large power transformers for both STATCOM and WF generators, although a low cost solution. The SST on the other hand has been regarded as a promising technology integrating active power transfer, reactive power compensation, and voltage- conversion, while no literature has explored the application of SST with full utilization of all the functions. Accordingly, the major contribution of this chapter is to propose a new family of SST-interfaced WF architectures effectively replacing the conventional transformer and reactive power compensator.

7.2.2 A family of SST interfaced wind farm systems

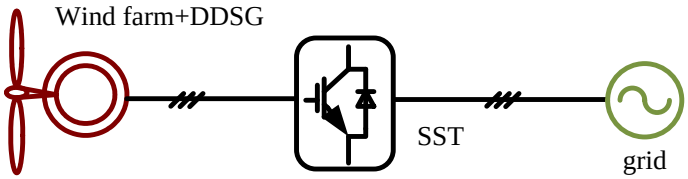
A family of wind energy system has been proposed as shown in Figure 7-3. Figure 7-3 (a) shows the case of a WF with SCIG, where the SST acts as the grid interface. The local capacitor bank, two conventional transformers, and the STATCOM as shown in Figure 7-2(a) are all functionally integrated into a single SST, which will be illustrated in the latter case study. Figure 7-3 (b) shows the case with DFIG, where the AC/AC back to back converter is retained for fully utilization of advantages of SCIG based WF, while two transformers and STATCOM are replaced by a SST. Lastly, Figure 7-3 (c), featuring DDSG with full power converters, shows how the SST can be used to replace the AC/AC converter, both step-up transformers and STATCOM. From these diagrams it is easily seen how the proposed SST-interfaced WFs represent a possible more compact and cable solution, and as such can be deemed to be a promising technology. This will be investigated in what follows.



(a) WF with squirrel-cage induction generator



(b) WF with doubly-fed induction generator



(c) WF with directly-driven synchronous generator

Figure 7-3 Proposed WFs with induction generators interfaced by SST

7.3 System Case Study

7.3.1 A Three-phase SST for system evaluation

Although different topologies can be adopted to implement the SST for the proposed application, the overall control objectives intrinsic to its operation are the same regardless of

its circuit topology; namely AC voltages for reactive power compensation and the DC voltages for active power transfer. For the sake of better illustration of control objectives of the SST in the proposed system, which are active power transfer, reactive power compensation, and voltage-conversion, a simple three-phase SST topology is initially adopted and analyzed neglecting the physical limitation of the power device and magnetic materials.

Figure 7-4 shows a cascaded type three-phase SST. Its first stage is a three-phase bidirectional AC/DC PWM rectifier, which can also be used in the DC/AC power conversion stage as depicted. Its DC/DC stage is embodied by a dual active bridge (DAB) converter, which represents the most attractive candidate for high power applications requiring isolation, as it can perform zero-voltage-switching (ZVS) in a wide operation range[110]. In the above SST configuration, v_{habc} is the PCC voltage, i_{habc} is the PCC current flowing into the SST, v_{hdc} is the high DC bus voltage, v_{ldc} is the low DC bus voltage, v_{labc} is the output voltage of inverter, and i_{labc} is the output current of inverter.

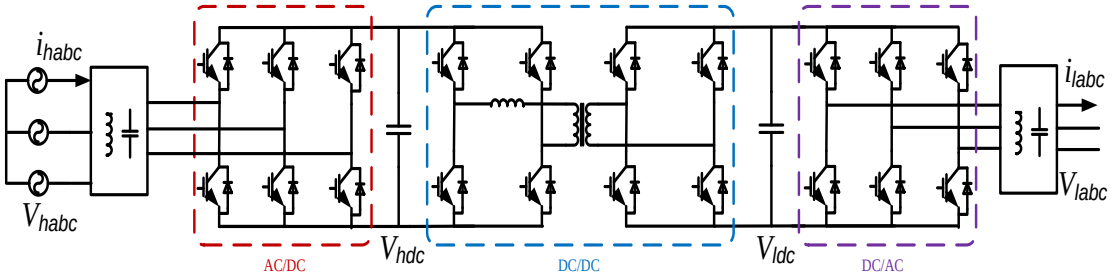


Figure 7-4 Three-phase SST for control illustration

Figure 7-5 shows the control system adopted with the integrated active power transfer, reactive power compensation, and voltage-conversion functions. In this study, we focus on the grid side performance enhancement, therefore no dedicated control on the generator side is considered for simplification. The SCIG operates as a fixed speed machine regardless of the wind speed. However, the variable speed control can be easily incorporated to reduce mechanical stress, dynamically compensate for torque and power pulsation, and achieve maximum power point tracking[134]. In the following parts, the controllers for all three conversion stages of SST are introduced.

A d-q axes vector controller is used to regulate the input currents of the three-phase AC/DC rectifier, where the d-axis loop is used to regulate the DC bus voltage, and the q-axis loop to regulate the SST reactive power generated, which in turn is governed by the PCC voltage magnitude loop. This control structure is exactly the same as that used in the well-known STATCOM, evincing how the SST integrates this compensator functionality. To regulate the active power flow, a phase regulation scheme is adopted for the DAB using a simple PI controller, which adjusts the phase shift between high- and low-side H-bridge converters. Lastly, the inverter stage is controlled using a conventional dual loop strategy in d-q coordinate, as shown in Figure 7-5. It is shown in the figure that the outer voltage loop is used to compensate for the reactive power consumption at the induction generator terminals, thus implementing the function carried out by the capacitor banks in the case of WFs with SCIG. In addition, the inductor current loop is cascaded as the inner loop such that fast dynamic responding can be guaranteed. It is also shown in the Figure 7-5 that the couplings between d-axis and q-axis control loop have also been taken into the consideration as this is

also necessary for a high performance system. Due to the bidirectional power transfer characteristics of the system, this controller can also transfer the power from the low voltage side to the high voltage side, which is the case in the presented system. Obviously, the presented control logic can enable the reactive power compensation function without the wind power input, thus the fully reactive power compensation function can always be maintained.

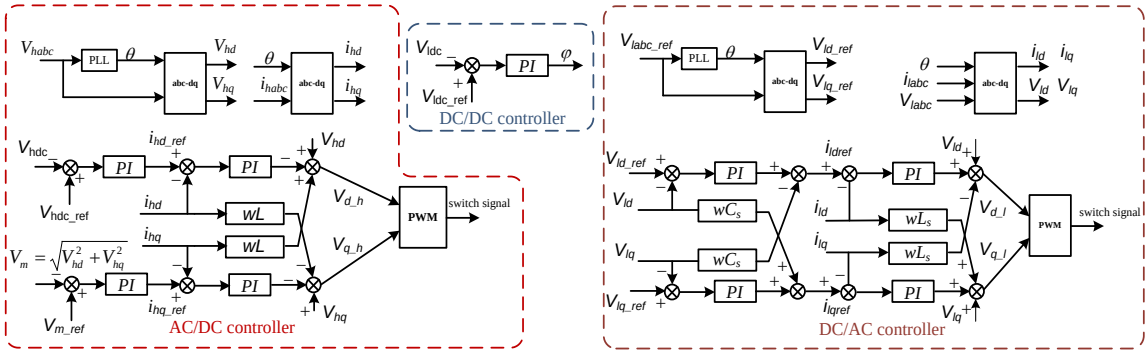
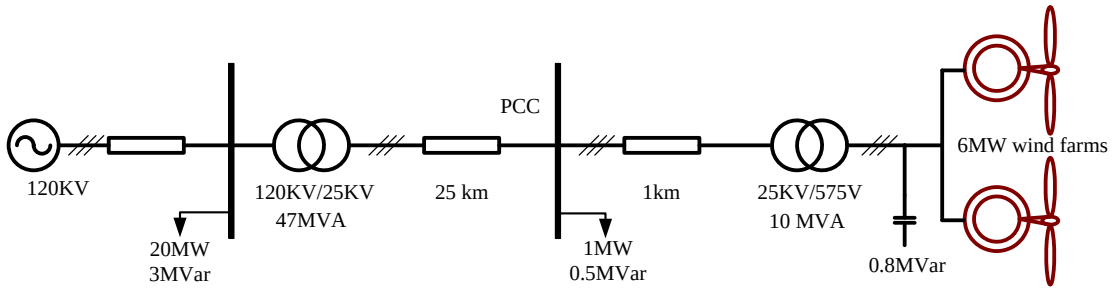


Figure 7-5 Control system for the three-phase SST in wind energy systems

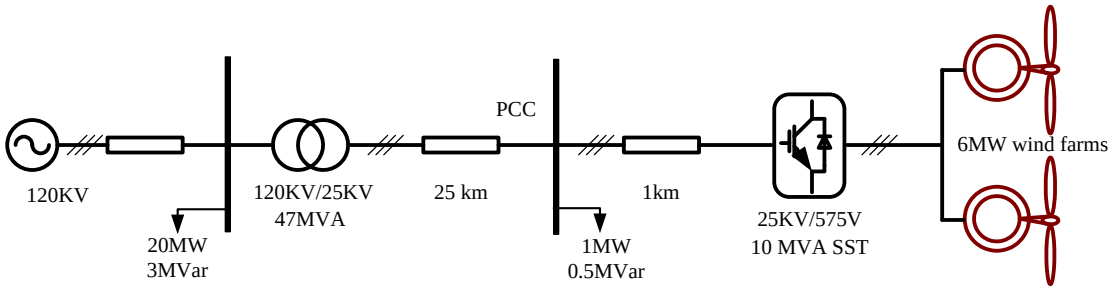
7.3.2 System study in SCIG driven WFs

A system study is carried out in a typical WF system, as shown in Figure 7-6 (This system is a demo from MATLAB 2008b). The SCIG driven case was used as the example since it presents the largest demand of the reactive power, and hence compensation needed, among the three types of generators under consideration. Nonetheless, the conclusion drawn from

the case study can also be applied to WF driven by DFIG and DDSG since the control objectives are exactly the same for all three systems.



(a) Conventional transformer interfaced wind farm with SCIG



(b) SST interfaced wind farm with SCIG

Figure 7-6 Power system plus WFs used in the case study

In this system, two 3.3MVA, 575V WFs with SCIGs are connected to a 25kV distribution system. Figure 7-7 shows the power characteristics of the wind turbine as a function of turbine speed under varying wind speeds. The base wind speed for the wind turbine is 9m/s(the cut-in speed of wind turbine is 4m/s and the cut-off speed of wind turbine is 25m/s), and the base rotational speed at the base wind speed is 1pu with the base of generator speed. The active power generated by the wind turbine at base wind speed is 3MW, which

corresponds to a power factor of 0.9. The pitch angle is set to zero and no pitch control is implemented in this study for simplification. The parameters of the SCIG are set as shown in Table 7-1. The parameters of the 120kV generator impedance and the transmission line are also listed in Table 7-2 and Table 7-3, respectively, which give the detailed description of studied power system. For the evaluation, Figure 7-6 (a) represents a WF interfaced by a conventional 10MVA power transformer (25kV/575V) without any additional compensator at the PCC. A 0.8MVar capacitor bank is installed in the generator terminal for local reactive power compensation. Figure 7-6 (b) on the other hand shows the proposed WF with a 10MVA three-phase SST, using the circuit topology depicted in Figure 7-4 and control method presented in Figure 7-5. The high voltage DC bus of SST is regulated to 38kV and the low voltage DC bus is regulated to 1200V. It is worth to remind again that although the power and voltage of the studied system is high, the simple topology depicted in Figure 7-4 is adopted for demonstrating the concept proposed in the chapter and this will not affect the conclusion drawn from the simulation results. In addition, the average modeling approach is adopted for this large time scale simulation, which is also valid for the verification purpose.

The simulation conducted for the conventional WF system is to demonstrate the natural power flow from the conventional WF to the distribution system in order to explore its impact on the PCC in terms of voltage regulation especially. The simulation for the proposed WF system on the other hand demonstrates the capability of proposed SST-interfaced WF system to perform reactive power compensation in order to suppress voltage fluctuation.

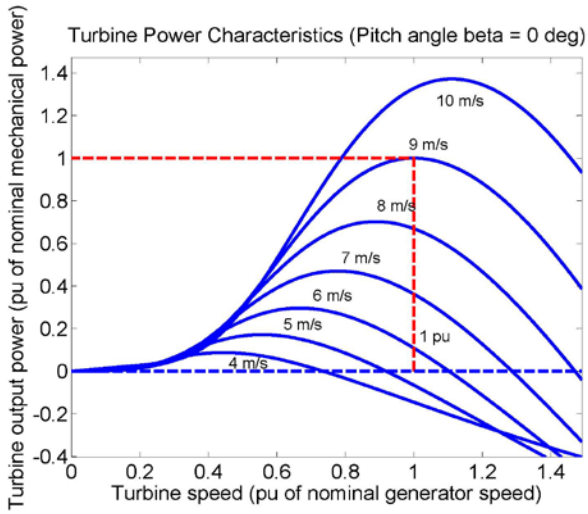


Figure 7-7 Power characteristics of wind turbine

Table 7-1 Parameters of a single SCIG

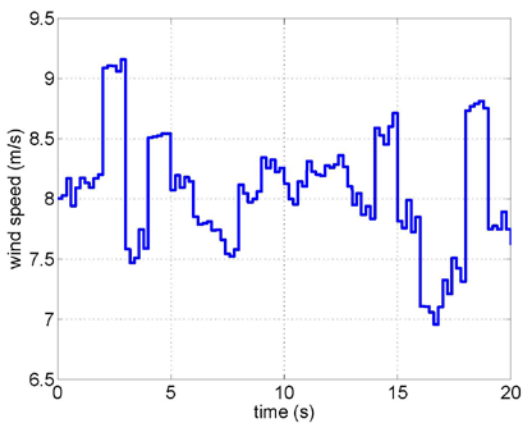
Nominal power	3.3MVA	Nominal voltage	575V
Nominal frequency	60HZ	Stator resistance (pu)	0.048
Stator inductance (pu)	0.075	Rotor resistance (pu)	0.018
Rotor inductance (pu)	0.1791	Mutual inductance (pu)	6.77
Inertia constant (s)	5.04	Pole pairs	3

Table 7-2 Parameters of 120kV generator equivalent impedance

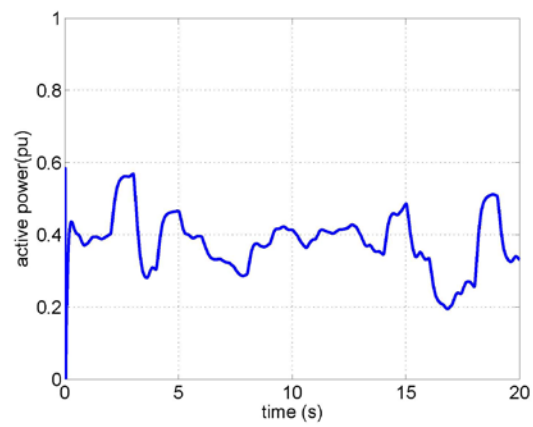
	Positive sequence	Zero sequence
Resistance (Ω)	0.5760	1.7280
Inductance (H)	0.0153	0.0459

Table 7-3 Parameters of transmission line (three-phase PI section)

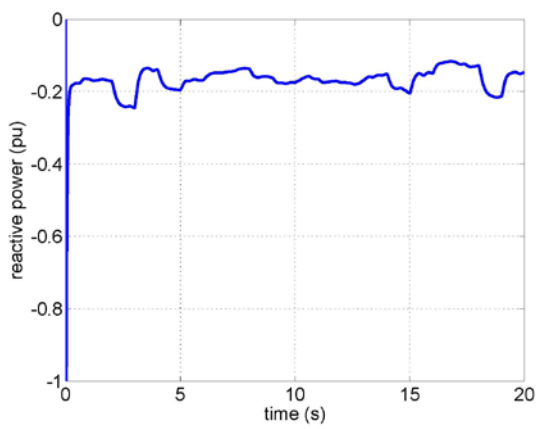
	Positive sequence	Zero sequence
Resistance (Ω/km)	0.1153	0.413
Inductance (H/km)	1.05e-3	3.32e-3
Capacitance (F/km)	11.33e-9	5.01e-9



(a) Wind speed profile



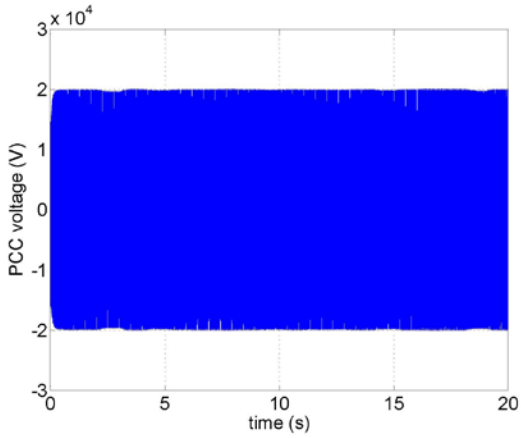
(b) Active power of WF (10MVA base)



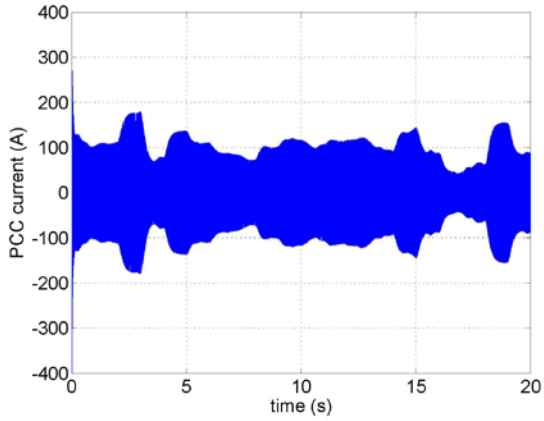
(c)Reactive power of WF (10MVA base)

Figure 7-8 Electrical characteristics of WF under study

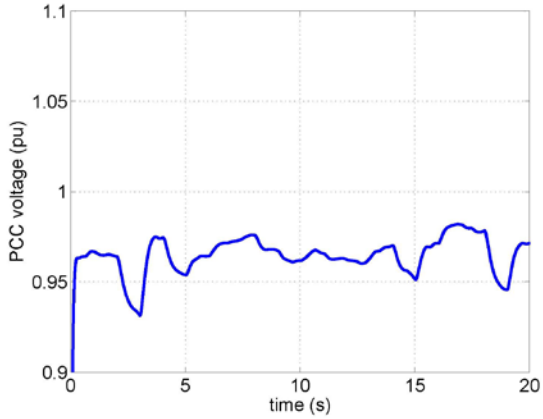
Figure 7-8 shows the electrical characteristics of the WF under study, where the wind speed profile shown in Figure 7-8 (a) is continuously changing around 8m/s. Accordingly, the active power transferred by the wind generator follows the same trend as shown in Figure 7-8 (b). Figure 7-8 (c) illustrates the reactive power at the induction generator terminal, which indicates a significant amount of reactive power consumption by the SCIG.



(a) PCC voltage



(b) PCC current



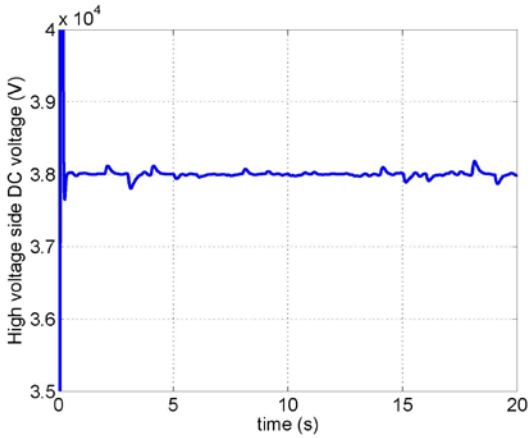
(c) PCC voltage RMS value (25KV base)

Figure 7-9 Simulation results of WF interfaced by conventional transformer

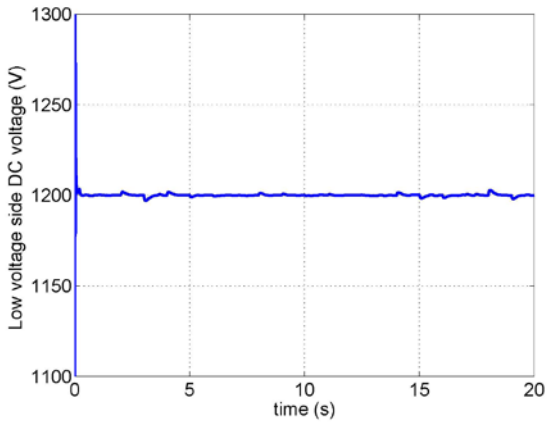
Figure 7-9 shows the simulation results of the WF interfaced by the conventional transformer, where the wind speed profile is the same as shown in Figure 7-9 (a). Figure 7-9 (a) and Figure 7-9 (b) are the PCC voltage and current in the presented system. Due to the fluctuation of the wind speed, the magnitude of current is changed accordingly. As a result, the PCC voltage is also affected, as shown in Figure 7-9 (c), which is less than the rating value and fluctuated.

As a comparison, Figure 7-10 shows the simulation results of the proposed SST-interfaced WF with integrated active power flow, reactive power compensation and voltage-conversion functions. Figure 7-10 (a) and Figure 7-10 (b) show the 38 kV and 1.2 kV DC voltage of three-phase SST respectively. It can be seen that the DC voltage is regulated well although there are some dynamic responses caused by the active power fluctuation. Figure 7-10 (c) and Figure 7-10 (d) show the PCC voltage and current in the proposed system. Compared with Figure 7-10 (b), the current is a little smaller since the PCC voltage is higher in the SST-interfaced system. In Figure 7-10 (e), the RMS value of PCC voltage is illustrated, which is within 1% of the nominal value as expected. Figure 7-10 (f) demonstrates the reactive power sent by the SST. The trend of reactive power is similar with that of the wind profile, thus compensates for the voltage fluctuation at PCC.

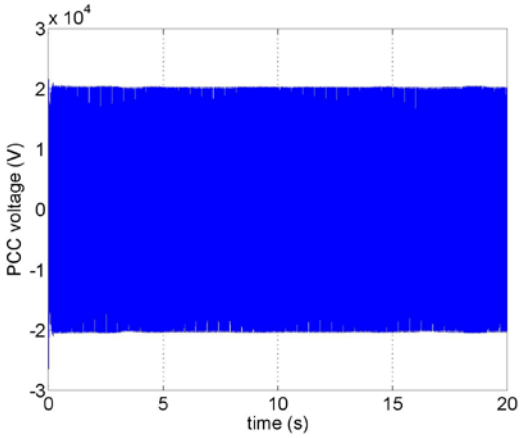
The results in Figure 7-8-Figure 7-10 evince the effectiveness of the SST as a potential WF interface for the integration of wind energy into the grid with less voltage fluctuation. It is clear that the proposed wind energy conversion system can fulfill the tasks of active power transfer, reactive power compensation and voltage-step.



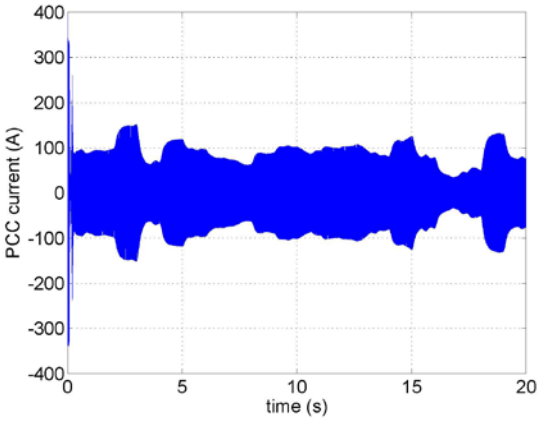
(a) 38KV DC voltage



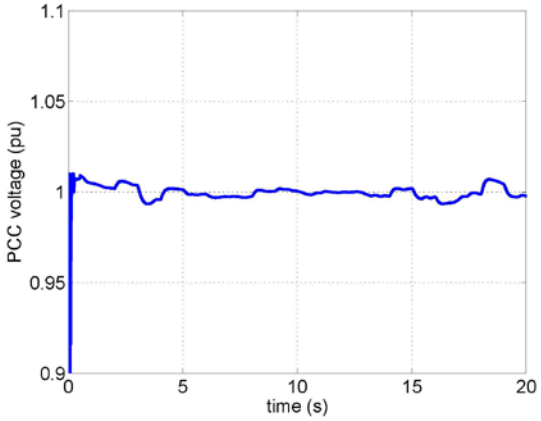
(b) 1.2KV DC voltage



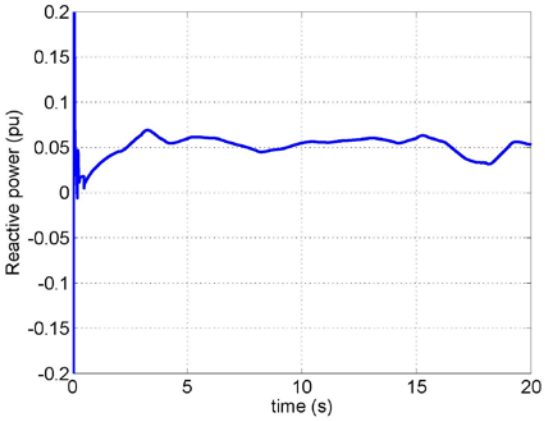
(c) PCC voltage



(d) PCC current



(e) PCC voltage RMS value (25KV base)



(f) Reactive power of SST (capacitive, 10MVA base)

Figure 7-10 Simulation results of WF interfaced by SST

The reactive power compensation capability of the SST is mainly limited by the power rating of it since both active and reactive power flows through the converter. Based on this consideration, the power stage should be designed so that the maximum current stress is within the range of the power device and passive components selected. In addition, since the proposed system can provide reactive power compensation, it can also be expected that the presented system can ride through the fault by injecting reactive power to the system as that of the STATCOM.

Furthermore, the concepts of integrating energy storage devices for profiling the power and improving the low voltage ride through (LVRT) performance can also be done. As an example, Figure 7-11 shows the proposed wind energy systems with integration of energy storage system.

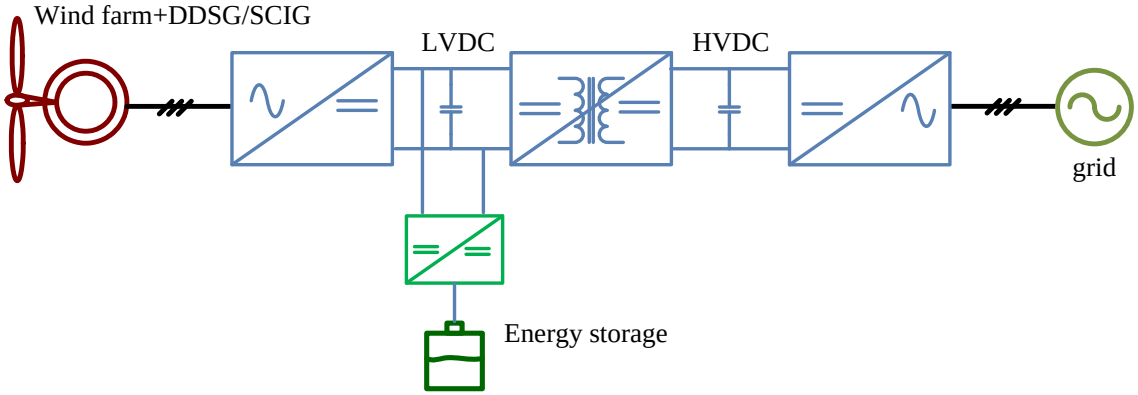


Figure 7-11 Integrating energy storage device in the proposed wind energy system with enhanced LVRT capability

7.4 Three phase SST topology suits for the proposed wind system

In order to realize the proposed wind energy system, the high voltage and high power SST is required, and this is a challenge considering the capability of power semiconductor devices. In this section, a promising high voltage and high power modular type SST topology is presented and analyzed for achieving the proposed wind energy system.

7.4.1 A Topology of a Modular Three-phase SST

Figure 7-12 demonstrates the presented modular, high voltage and high power three-phase SST topology in the proposed application. Three single-phase SSTs are connected to compose a three-phase SST, in which a high voltage and high power modular type single-phase SST is adopted as the basic phase building block. In the single-phase building block, the cascaded multilevel converter is utilized in the high voltage side with identical (low voltage) H-bridges, thus low voltage power device can be adopted. Several DAB converters with relatively high switching frequency (in the range of kHz to more than ten kHz decided by the power devices) are then parallel connected to each high voltage DC link regulating a common low voltage DC bus. In the last stage, conventional low voltage high power inverter technologies, such as device parallel or converter parallel, can be used to integrate with WFs. It is worth to point out that there is no limitation for the number of modules since this is the key feature of the cascaded type multilevel converter, the number of the modules is depended on the operating voltage and power device adopted.

The above converter structure represents a highly modular design, and as such opens the path to redundant operation, for reliability improvement. For instance, the N+1 redundant design can be incorporated to achieve fault tolerant operation [135]. In addition, it opens the path to modular manufacturing with its potential cost reductions due to economies of scale. In this way it tackles two of the main problems haunting the development of the SST, namely high voltage and high power operation, and reliability.

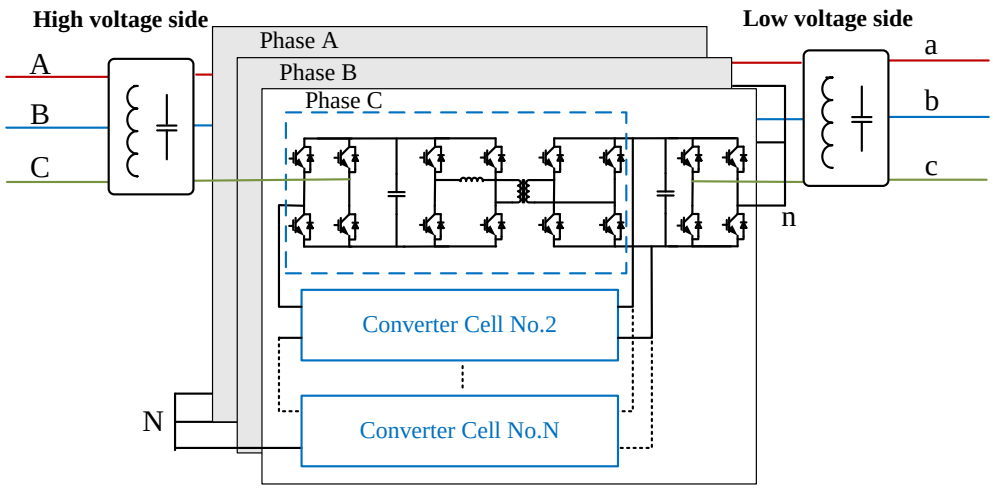


Figure 7-12 Proposed high voltage high power three-phase SST

The control of the proposed three-phase converter can actually be simplified to the control of single-phase converter shown in Figure 7-13 due to the phase building block configuration. This unit is exactly the same as what has already been discussed in previous chapters. Therefore, all the proposed control methods aforementioned can be applied to this specific application.

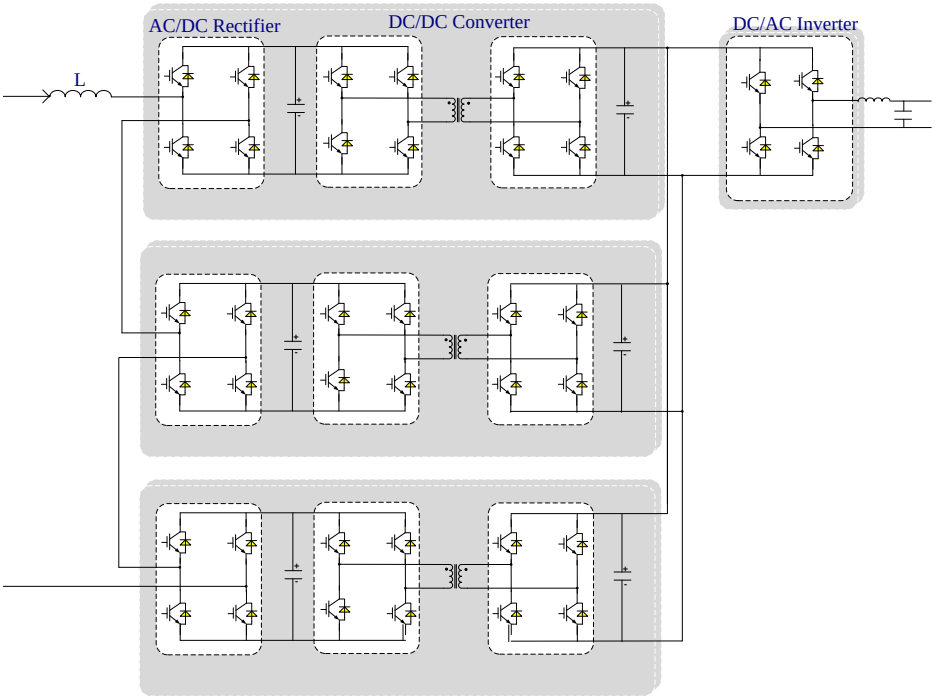


Figure 7-13 Single phase SST building block

7.4.2 Conceptual design and simulation of a 1MVA, 13.8kV-480V three phase SST

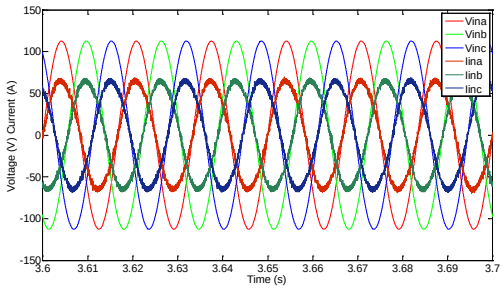
Based on the modular topology presented in Figure 7-12, a 1MVA, 13.8kV-480V three phase SST is conceptually designed. Due to the phase modular structure, the design methodology of the system is the same as presented in Chapter .5. In each phase module, three H-bridges with 6.5kV IGBT are cascaded in the rectifier stage, and three DAB converters are cascaded with each DC link. The high voltage DC links are controlled to 4300V each (total 12.9kV in each phase) and the low voltage DC link is controlled to 450V. The designed parameters of the system are summarized in Table 7-4.

Table 7-4 Parameters of the designed three phase SST topology

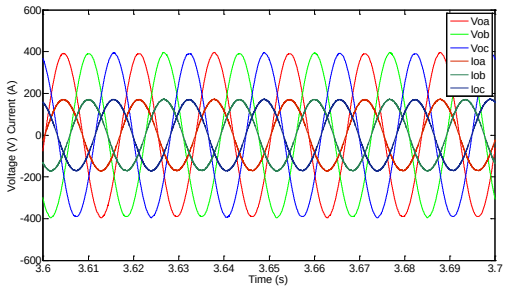
Rectifier stage	
Switching frequency	1.2kHz
Input filter L	24 mH
High voltage DC caps	750uH
Power devices	6.5kV, 250A IGBT
DC/DC stage	
Switching frequency	3.6kHz
Transformer Turns ratio	9.5:1
Transformer rating	200kVA
Transformer leakage inductance	1mH
Transformer magnetizing inductance	150 mH
Low voltage caps	200 mF
High voltage side power devices	6.5kV, 250A IGBT
Inverter stage	
Switching frequency	3kHz
Output filter L	100uH
Output filter C	250uF
Power devices	1200V, 3600A IGBT

Simulations have been conducted for the designed system. Figure 7-14 shows the 1MW system operation under the unity power factor. Figure 7-14(a) shows the input voltage and current of the three-phase SST, in which the current is in phase with the voltage, indicating the unity power factor operation. Figure 7-14(b) shows the output voltage and current of the

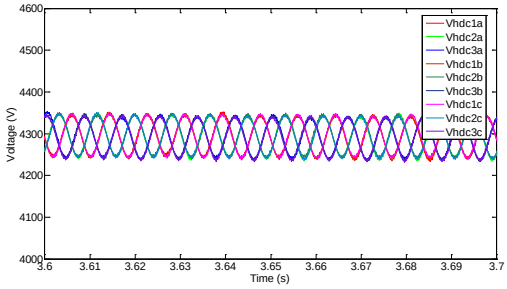
system. Since the resistive load is connected to the system, the output current is also in phase with the voltage. Figure 7-14(c) shows the voltages of nine DC links of high voltage side in all three phases, which are balanced and regulated to 4.3kV. Figure 7-14(d) shows the voltages of three DC links in low voltage side in all three phases, which are balanced and regulated to 450V.



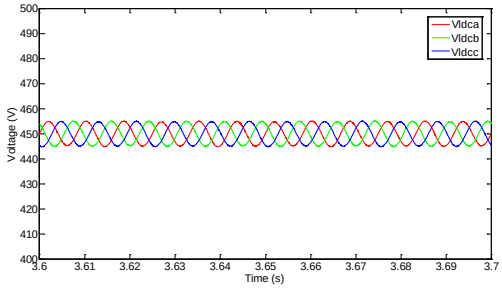
(a) Input voltage and current (Voltage scale to 1/100)



(b) Output voltage and current (current scale to 1/10)



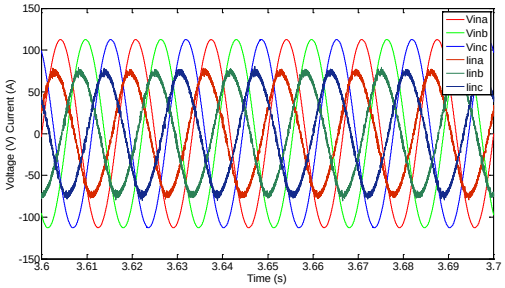
(c) High voltage DC links



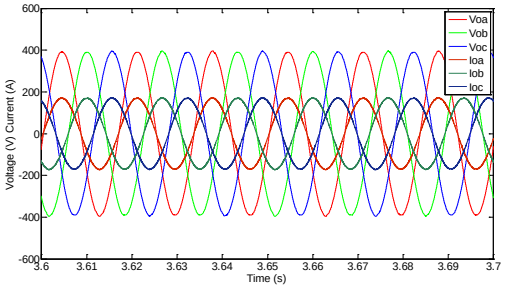
(d) Low voltage DC links

Figure 7-14 1MW system operation under unity power factor

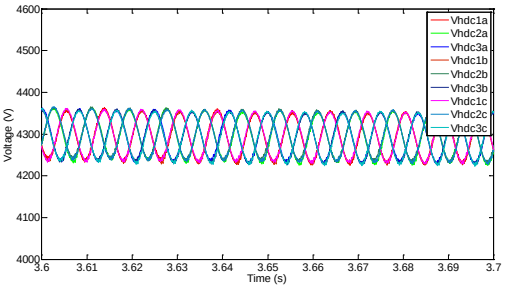
Figure 7-15 and Figure 7-16 present the capacitive and inductive mode operation of the designed three phase SST system, in which the reactive power is regulated to 0.5Mvar and -0.5Mvar respectively. It is seen from the Figure 7-15(a) and Figure 7-16(a) that the presented SST topology can achieve the satisfactory Var compensation performance.



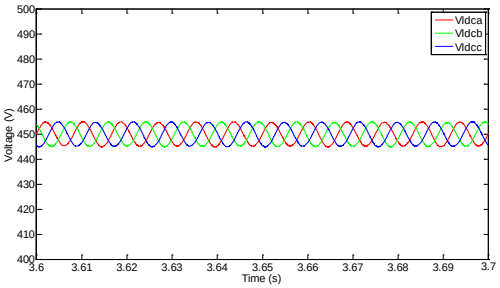
(a) Input voltage and current (Voltage scale to 1/100)



(b) Output voltage and current (current scale to 1/10)

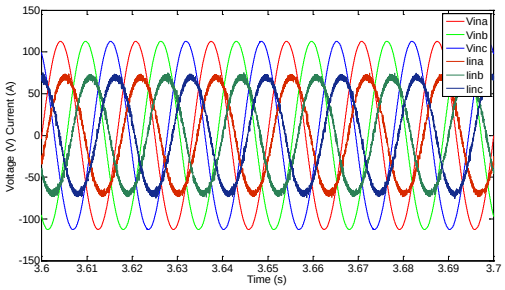


(c) High voltage DC links

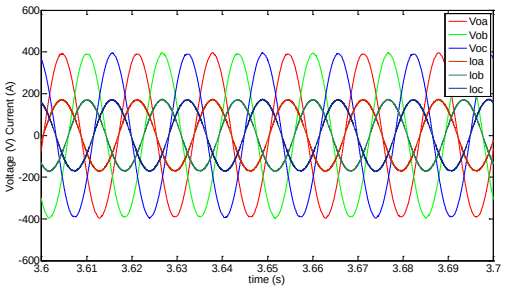


(d) Low voltage DC links

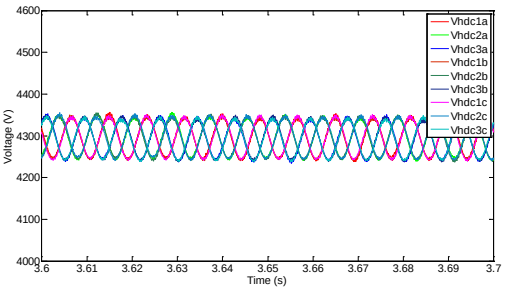
Figure 7-15 1MW, 0.5MVar capacitive mode operation



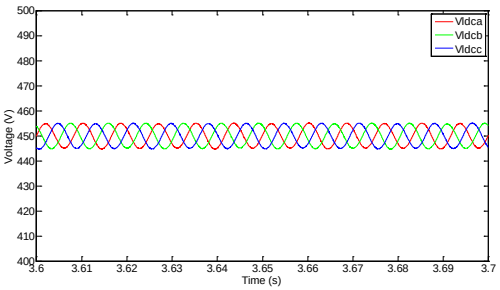
(a) Input voltage and current (Voltage scale to 1/100)



(b) Output voltage and current (current scale to 1/10)



(c) High voltage DC links



(d) Low voltage DC links

Figure 7-16 1MW, -0.5MVar inductive mode operation

In addition, the voltage and power ratings of the presented system can be easily increased due to the modular structure of the system. Therefore, the presented three phase SST topology can be applied in the proposed wind energy system with integrated functions of active power transfer, reactive power compensation, and voltage conversion.

7.4.3 Experimental results for verifying the SST functions

Experimental results are carried out in the designed single phase SST hardware setup for verifying the integrated functions of active power transfer, reactive power compensation and voltage conversion. In the experiments, the PCC voltage is set to 1800 V, and high DC voltage link is regulated to 2850V (950V each). The low voltage DC link is set to 100 V, and the inverter output is set to 60 V. A 1.3kW resistive load is connected in the low voltage AC terminals. Figure 7-17 to Figure 7-21 show the operation waveforms of the SST for both high voltage and low voltage side.

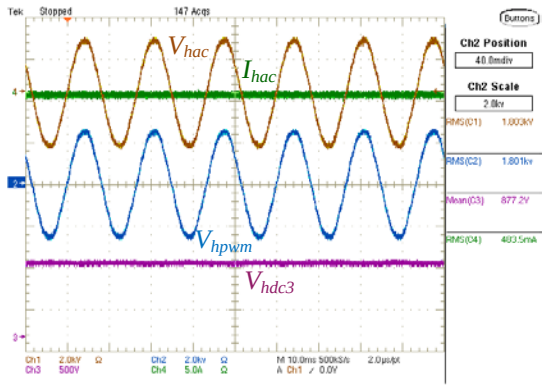
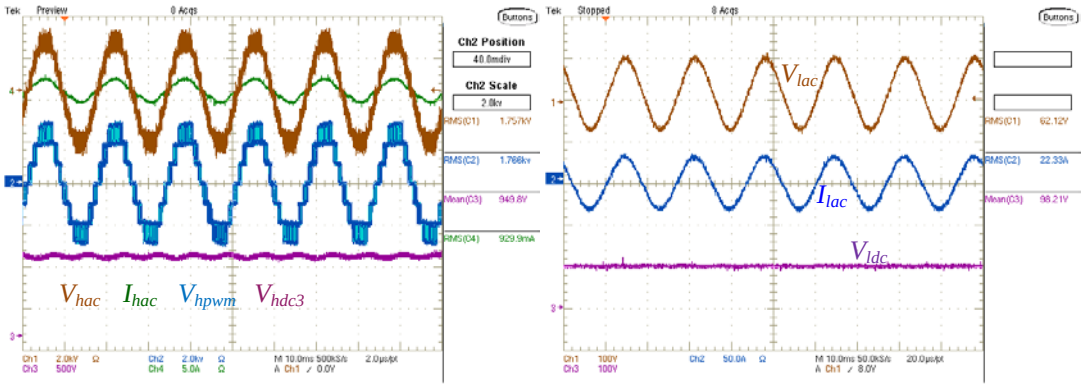


Figure 7-17 PCC voltage before start-up of the SST

Figure 7-17 shows the PCC voltage before the start-up of the SST, and the DC voltage is established by the diode rectifier. The PCC voltage is adjusted manually to 1.8KV through the VARIC and step-up transformer.

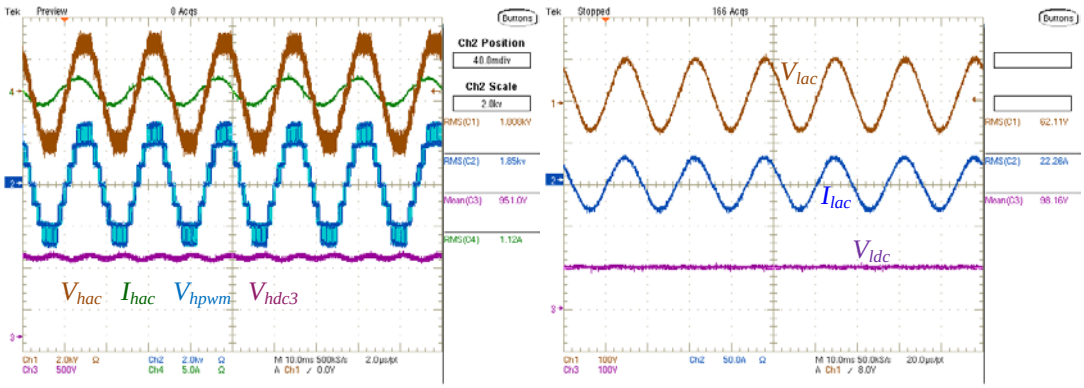
Figure 7-18 shows the operation waveforms of the SST without any reactive power generation. Because of the internal impedance of the VARIC and step-up transformer, the PCC voltage is decreased from 1.8kV to 1.757kV when SST supplies active power to the load. Figure 7-19 shows the capacitive operation mode of the SST, in which case the SST supplies additional capacitive power to the grid so that the PCC voltage is regulated back to 1.8KV.



(a) Input voltage, current, PWM voltage, and high voltage DC 3

(b) Output DC voltage, AC voltage and current

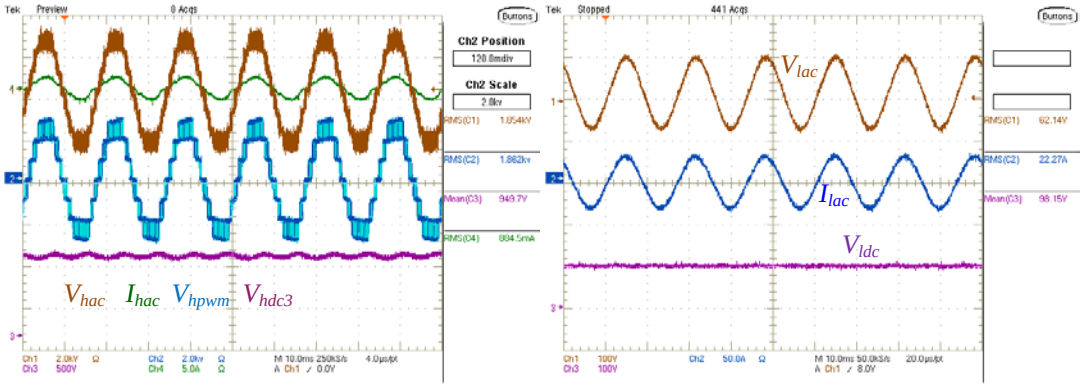
Figure 7-18 SST operation without capacitive power compensation



(a) Input voltage, current, PWM voltage, and high voltage DC 3

(b) Output DC voltage, AC voltage and current

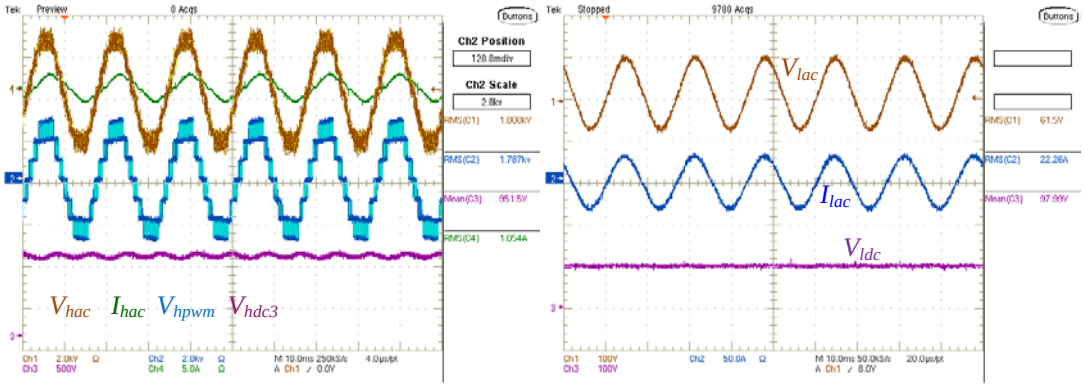
Figure 7-19 SST operation with capacitive power compensation



(a) Input voltage, current, PWM voltage, and high voltage DC 3

(b) Output DC voltage, AC voltage and current

Figure 7-20 SST operation without inductive power compensation



(a) Input voltage, current, PWM voltage, and high voltage DC 3

(b) Output DC voltage, AC voltage and current

Figure 7-21 SST operation with inductive power compensation

In order to verify the inductive power operation mode of the SST and its impact to the PCC voltage, the PCC voltage is manually adjusted to 1.854kV after SST operation, as shown in Figure 7-20. Figure 7-21shows the inductive power operation mode of the SST, in which the PCC voltage is regulated back to 1.8kV.

These results show that the developed SST can indeed transfer power between the grid and load terminal while providing the required Var to compensate for the fluctuating active power load demand. In this way the SST is expected to be capable of suppressing all voltage fluctuation in WFs using SCIG under the proposed system architecture.

7.5 Conclusion

Energy crisis calls for a large penetration of renewable energy resources, among which wind energy is a promising one. Voltage and frequency regulation is vital to meet the grid interaction requirements. This chapter has covered many key issues to compose the proposed wind energy system, including the system architecture, control objective, and component design. Specifically:

1. A family of wind energy system with integrated active power transfer, reactive power compensation, and voltage-conversion capability was proposed. Compared with the previous applications which utilize only the active power transfer and voltage-conversion functionalities, reactive power compensation capability is fully investigated.

2. The proposed family of wind energy system was demonstrated in the presence squirrel-cage induction generators, by far the most demanding case in terms of voltage fluctuation

and reactive power demand. Under the SST interface, the WF was rendered free of distribution power transformer and mandatory passive and active static power compensators.

3. A modular type, high voltage and high power three-phase SST topology was presented and its control strategy were investigated and shown to successfully carry out the tasks needed to interface WFs to the grid.

4. Experimental results are carried out in the developed SST prototype to verify the integrated functions of active power transfer, reactive power compensation, and voltage conversion.

5. The proposed techniques can also be applied to other renewable energy resources integration, such as wave energy, solar energy, and etc.

Chapter 8 Integration of Solid State Transformer with Zonal DC Microgrids

8.1 Introduction

AC power transmission and management has been dominating for more than a century due to its previous advantage in easier voltage step-up by using the conventional transformer technology, thus contributes to higher efficiency during the long distance transmission process. The advancing of power device and power electronics makes the DC transmission once again attracting our attention since change of DC voltage level is no longer the bottleneck of the technology. HVDC and MVDC are good examples [136]. With the world - wide energy shortage and deterioration of existing power grid, microgrid becomes one of the hottest research directions in the power area [137], [138], [139]. Previously, the emphasis is still on the AC microgrid due to the existing AC power grid architecture [140], [141], [142], [143]. With the consideration of DC nature of many key components in the smart grid, such as photovoltaic (PV), battery, fuel cell, super capacitor, and etc., as well as many DC type load, such as light-emitting diode (LED), DC microgrid has received more attention recently since it brings the opportunity for boosting the efficiency by eliminating the unnecessary power conversion stages [144], [145], [146], [147], [148].

Sustainable and smart building is one of the goals that smart grid researchers want to achieve. Figure 8-1 shows the integration opportunities for future buildings[149]. The

original idea is to power the building solely by using sustainable energy resources and manage the power flow intelligently with the aid of energy storage devices. In fact, the ultimate goal described here is to apply a so called zonal microgrid concept presented in this chapter [147] . Each building can be regarded as a zonal microgrid, within which it can generate and balance the power from sustainable energy resources and energy storage devices. Once achieving this, the newly established buildings, which can be considered as the new loads in the grid, will not affect the existing power grid. However, with the nature of uncertainty and intermittent characteristics of renewable energy resources, such as irradiation of solar, the reliability of smart building cannot be guaranteed if no other external backup power is available. The conflict between self-power of smart building and its demand of high reliability is a challenge.

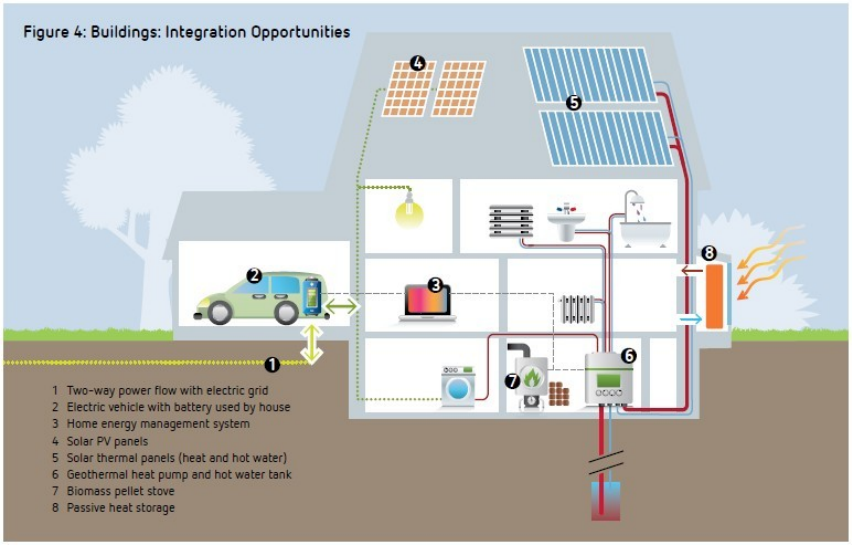


Figure 8-1 Integration opportunities for future building [149]

In the previous studies, the AC microgrid system can easily access the existing AC power grid, making it as the backup power source. However, the multiple DC-DC-AC conversion stages for the DC type renewable energy resources and energy storage devices make the system efficiency a notable problem[140], [141]. In the DC microgrid, the unnecessary conversion stages are eliminated, and an AC-DC converter is adopted as the interface with the AC power grid, hence the efficiency is increased [148]. However, both two types of microgrid cannot effectively manage the DC and AC networks coordinately since too many discrete stages are involved.

In this chapter, a promising microgrid architecture that integrates the solid state transformer with zonal DC microgrids is proposed[150]. In addition, a centralized power management algorithm that suitable for the proposed system. The main characteristics of the proposed system can be summarized as:

(1).Power factor regulation capability in the distribution system side.

(2).Integrated power management of AC and DC network.

(3).Maximum utilization of distributed renewable energy resources (DRER) and distributed energy storage device (DESD).

(4).Minimum burden for existing power grid without decreasing reliability and stability of the microgrid.

The operation principle of the proposed microgrid system is analyzed in detail and the performance of the system is verified by simulation [150][151].

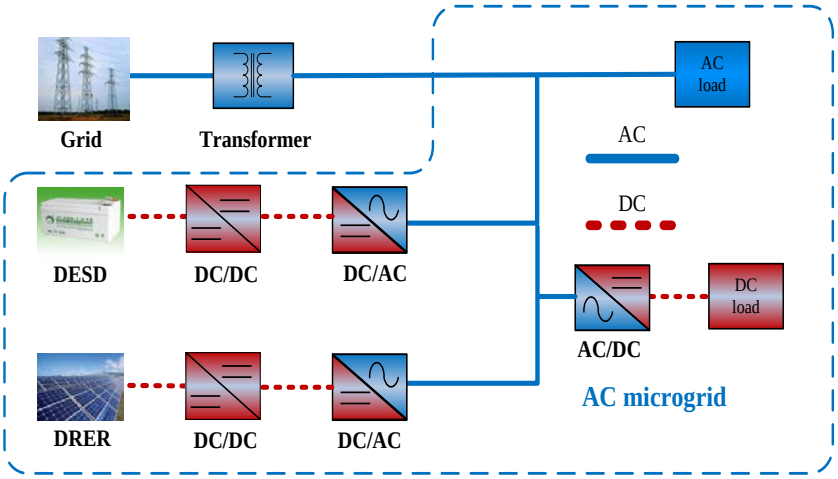
8.2 Proposed SST interfaced microgrid system

8.2.1 Existing AC and DC microgrid architecture

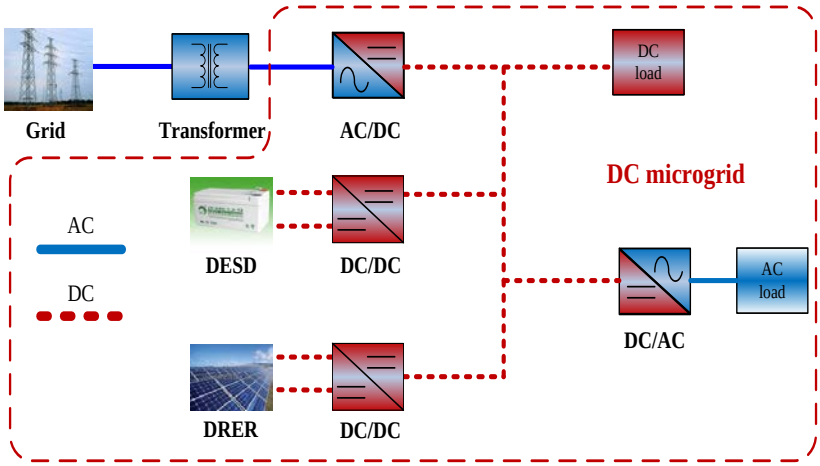
The terminology of AC and DC microgrid are mainly depended on the characteristics of the common bus, in which the power is managed and distributed. The typical single line representation of AC and DC microgrid architectures are depicted in Figure 8-2(a) and Figure 8-2 (b) respectively, where PV and battery are chosen as the typical DRER and DESD. For simple and fair comparison, the loads are assumed to be voltage compatible in this chapter, which means no additional converters are needed to match the voltage between the bus and load if both of them are AC or DC type.

Figure 8-2 (a) shows the typical configuration of an AC microgrid, in which AC mains is supplied by a step-down transformer from the distribution system. Since PV and battery are all DC type source, they need additional inverters to connect to AC mains. AC loads can be connected directly with the mains whereas DC loads need an additional rectifier to generate DC voltage. In the DC microgrid shown in Figure 8-2 (b), an AC/DC converter is necessary to establish the DC mains after the step-down transformer. PV and battery can be connected to DC mains by using DC/DC converters. DC loads can be integrated directly with DC mains whereas an inverter is needed for AC type loads. From the power generation perspective, DC microgrid owns advantage over AC microgrid since less conversion stages indicates a higher efficiency. Nonetheless, the two microgrids have too many separate power conversion stages thus may be difficult to manage the power of AC and DC networks coordinately. In addition, the conventional transformer makes the whole power system bulky and uncontrollable to

certain extent, bringing additional power quality issues.



(a) AC microgrid architecture



(b) DC microgrid architecture

Figure 8-2 Typical AC and DC microgrid architectures

8.2.2 Solid Transformer based microgrid

As aforementioned, SST does much more than just a voltage-step transformer. A functional diagram of the SST is illustrated in Figure 8-3. The SST typically includes a high-voltage AC to DC power conversion stage to generate a high voltage DC bus, a high-frequency DC/DC converter stage to produce a regulated low voltage DC bus, and a DC/AC stage to produce a regulated low voltage AC bus. Therefore, the SST is essentially a three-port energy router. It can integrate the distribution system, residential AC system and envisioned DC system. In order to improve the system efficiency, the DC type source and load are connected to DC port, whereas the AC type source and load are connected to AC port. The three-port characteristic of SST make it very suitable to enable a new microgrid that exhibits better performance compared with conventional AC and DC microgrids.

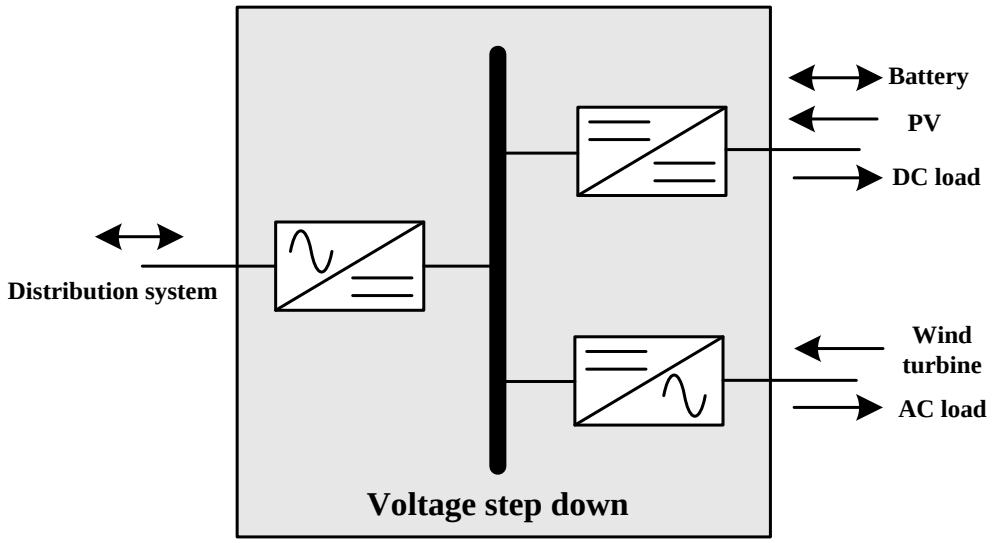


Figure 8-3 Functional diagram of SST

Figure 8-4 demonstrates the proposed SST based microgrid system. The AC load is connected to the AC mains of SST, and the DC source and load are connected to the DC mains for minimizing the conversion stages. The high voltage side of SST is connected with the distribution system thus the conventional transformer is got rid of.

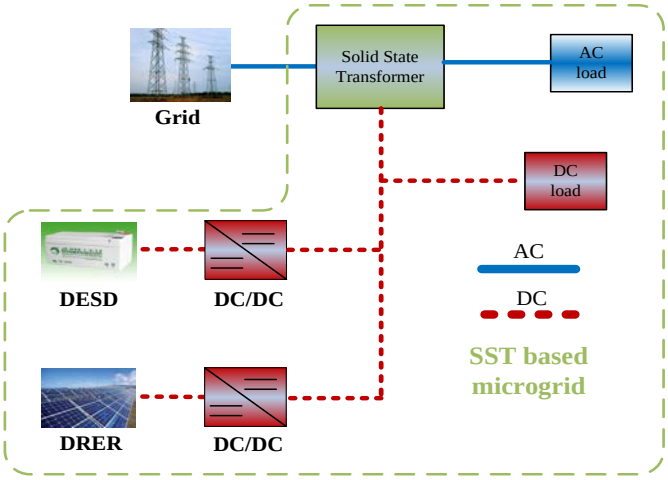


Figure 8-4 SST based microgrid architecture

As presented before, SST is essentially a three-port power converter, thus the AC and DC networks can be managed coordinately. The presence of SST can also isolate the distribution system from the residential side, thus the fault in one side will not affect another. Furthermore, the high voltage AC/DC converter in the distribution system side can realize the power factor regulation, promising the Var compensation capability. In this sense, the SST based microgrid is a more compact microgrid and shows superior characteristics over conventional AC and DC microgrid.

8.2.3 Zonal DC microgrid concept

Smart and sustainable building is a promising and realistic concept that makes full utilization of renewable energy resources and energy storage devices by adopting certain power management algorithms. Each building or a group of buildings can be regarded as a zone, within which the power is balanced. This means the buildings can supply their own power demand by using DRER and DESD. The zonal smart and sustainable building, once built, will have minimum effect to the existing power grid. DC microgrid wins more attention from the perspective of the conversion efficiency and has been studied extensively recently. This chapter will take the DC microgrid as the research target. Combining these two concepts, the zonal DC microgrid is obtained. The drawback of zonal DC microgrid lies in that it will face the problem of power supply reliability due to uncertainty and intermittent characteristics of renewable resources if no backup power supply is provided. Thanks to three-port characteristics of SST, the backup power can be obtained from the distribution system when the DRER and DESD can no longer maintain the power balance. The integration of SST and zonal DC microgrid potentially promises satisfactory performance.

8.3 System description and converter control

8.3.1 Studied microgrid system description

Figure 8-5 depicts the studied system of the proposed concept as well as the power converters adopted in it. A solid state transformer is connected between the distribution system and low voltage AC residential side. DC voltage is also available for integrating

multiple zonal DC microgrids. In the presented system, PV and battery are used as the studied DRER and DESD respectively to generate and balance the power within each zonal DC microgrid. For better illustrating the proposed concept, only one zonal DC microgrid integrated with SST is considered. The concept remains valid if multiple zonal DC microgrids are involved. A 20kVA single-phase solid state transformer is adopted in this study. By using state-of-art 15kV SiC power device developed by Cree Inc., a high-efficiency, three-stage converter topology can be possibly adopted, as shown in Figure 8-5. A single-phase AC/DC PWM rectifier together with a dual active bridge DC/DC converter generates the 400V DC bus from 12 kV distribution system. Then a single-phase split type inverter generates the 120V/240V dual output for residential application. A 10kW conventional boost converter is used as the interface between the PV panel and 400V DC bus, and a 10KW bidirectional buck-boost converter is adopted as the charger for battery packs. The parameters of the battery pack and PV panel used in this chapter are presented below.

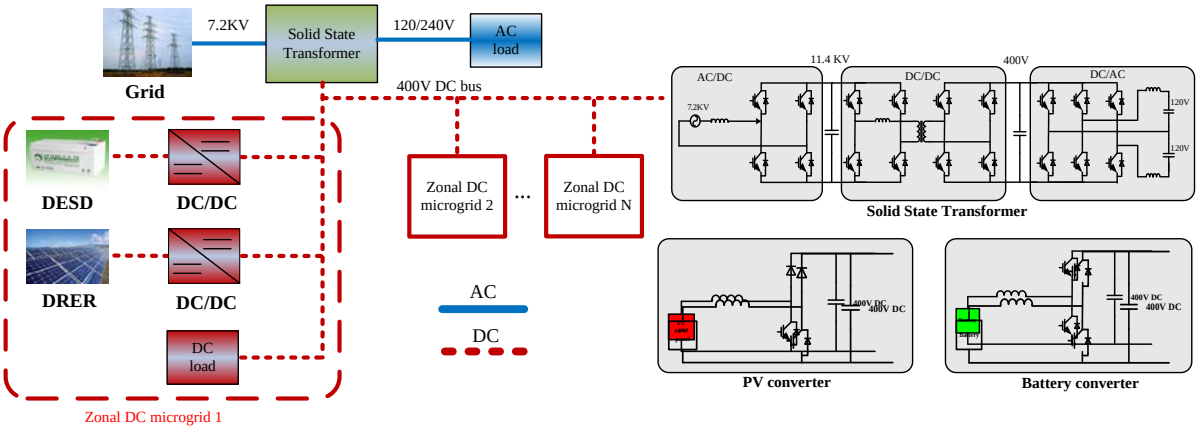


Figure 8-5 Solid state transformer integrated with zonal DC microgrid

Table 8-1 summaries the parameters of the single battery cell adopted in the system. Lithium-ion batteries are connected in series and parallel to serve as the distributed energy storage device.

Table 8-1 Battery pack parameters

Batter type	Li-ion
Single cell nominal voltage	3.6V
Single cell rated capacity	2Ah
Initial state of charge	80%
Cells in series	55
Cells in parallel	75
Maximum SOC	90%
Minimum SOC	10%
DOD limitation	20%
Charge rate limitation	30A

Figure 8-6 illustrates the discharge curve of the battery pack under different discharging currents, including 5A, 15A, and 30A. The nominal voltage of battery pack is about 210V and the nominal discharging current is 13A. State of charge (SOC), depth of discharge (DOD), and maximum charging/discharging rate are of great importance since it limits the battery life [152]. The maximum SOC of battery is set to 90% while the minimum SOC of battery is set to 10%. The DOD is limited to 20%, for more than 10 years-service time. The maximum charging or discharging current for the battery pack is set to 30A, which is 1/5 of

the capacity of the battery stacks, as generally recommended. For better illustration, the maximum charge or discharge power is adopted and set to 6kW due to the 210V nominal voltage of the battery pack. Initial SOC of the battery pack in the simulation is set to 80%.

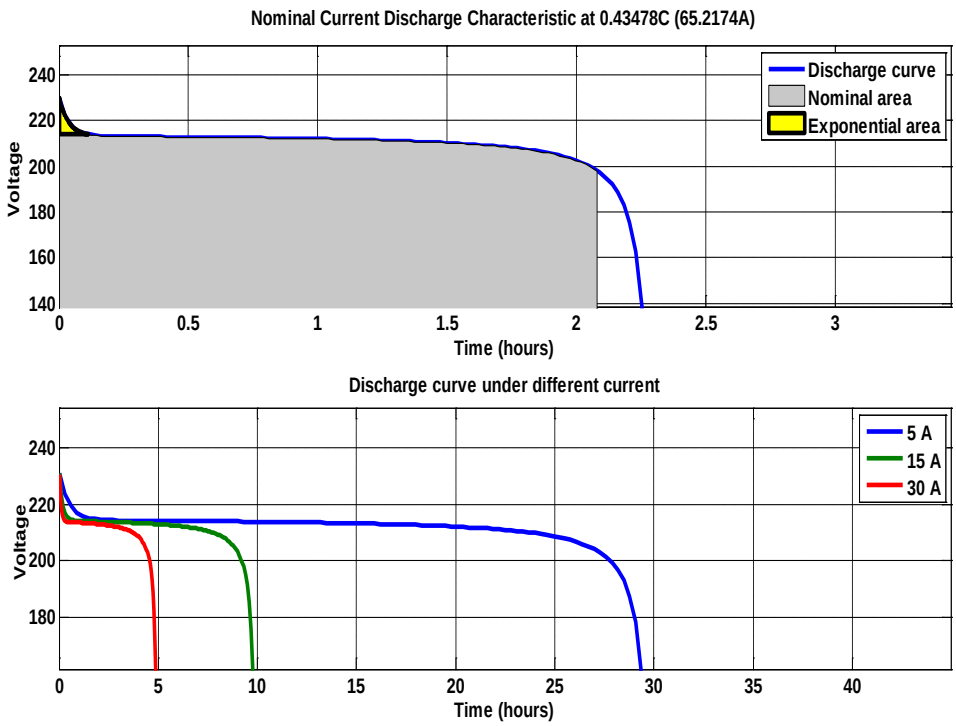


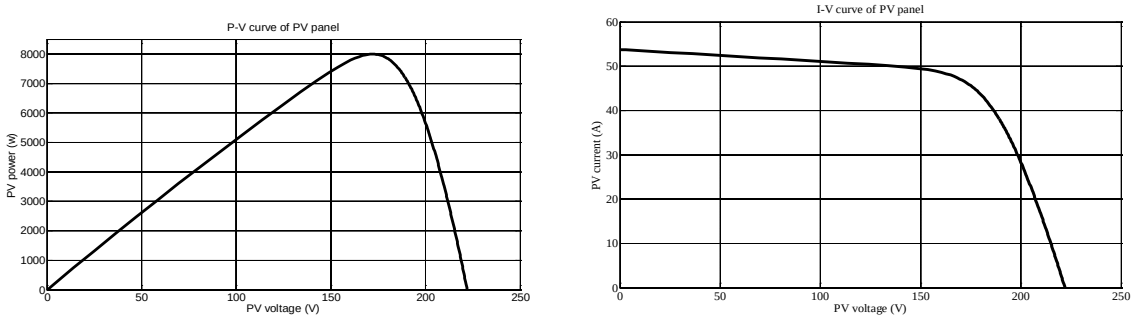
Figure 8-6 Discharge characteristics of battery pack

Table 8-2 describes the main parameters of the PV cell used in the study. The parameters are measured under the irradiation of 1kW/m^2 and the temperature of 25 ^{o}C. Figure 8-7 shows the tested characteristics of PV panel that consists of 100 PV cells, with the configuration of 10 cells in series and 10 series in parallel. Figure 8-7 (a) is the P-V curve of PV panel and Figure 8-7 (b) is the I-V curve of PV panel. It can be seen that under the

irradiation of 1kW/m^2, the maximum power that can be extracted from PV panel is about 8kW while the PV terminal voltage in this operating condition is about 172V.

Table 8-2 PV cell parameters (1kW/m^2, 25°C)

PV cell short circuit current	5.45A
PV cell open circuit voltage	22.2V
PV cell current at Pmax	4.65A
PV cell voltage at Pmax	17.2V
PV cell in series	10
PV cell in parallel	10



(a) P-V curve of PV panel (b) I-V curve of PV panel

Figure 8-7 PV panel characteristics (1kW/m^2, 25°C)

8.3.2 Solid state transformer control

The SST in the presented system is in charge of providing 400V DC bus as well as 120/240V AC bus for both DC and AC networks. For the single-phase three-stage SST

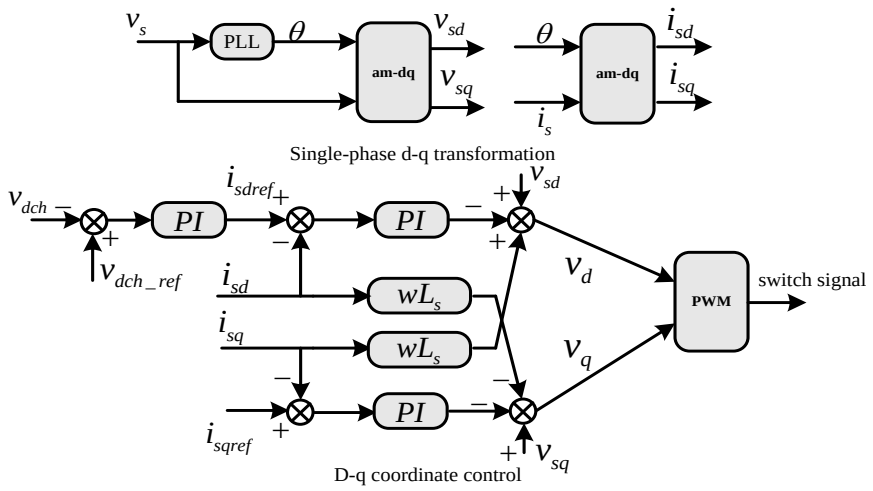
aforementioned, the control diagram can be represented by Figure 8-8 and the symbols are explained in Table 8-3.

Table 8-3 SST system symbols

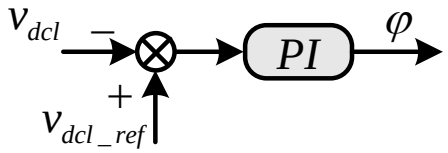
v_s	PCC voltage in distribution system
i_s	PCC current flows into SST
v_{dch}	11.4KV DC voltage
v_{dcl}	400V DC voltage
v_{l1}	120V AC voltage
v_{l2}	240V AC voltage
i_{l1}	Upper inductor current in low voltage AC side
i_{l2}	Lower inductor current in low voltage AC side

Single-phase d-q decoupled control is adopted for the AC/DC converter in the high voltage side to realize zero steady state error tracking of current, as shown in Figure 8-8 (a) [105]. Both high voltage DC bus and power factor at PCC are controlled by this dual loop controller. The regulator output of DC voltage loop is set as the reference for the inner active current loop for fast stabilizing the DC bus voltage. Reference of the reactive current loop is decided by the power factor requirement, and it is set to zero for unity power factor operation in the study [105]. For the DC/DC stage, since the topology adopted here is the dual active bridge DC-DC converter, the phase shift control is adopted, and it is shown in Figure 8-8 (b). By adjusting the phase shift between voltage in the primary side H-bridge converter and

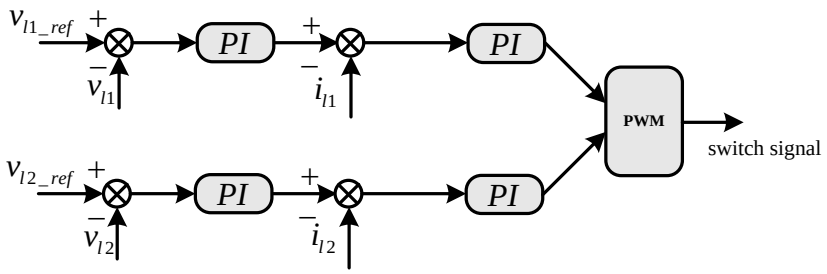
secondary side H-bridge converter, the power transferred is controlled and the low voltage side DC bus is regulated to the desired value, which is 400V [153].



(a) High voltage AC/DC stage control



(b) DC/DC stage control



(c) Low voltage DC/AC stage control

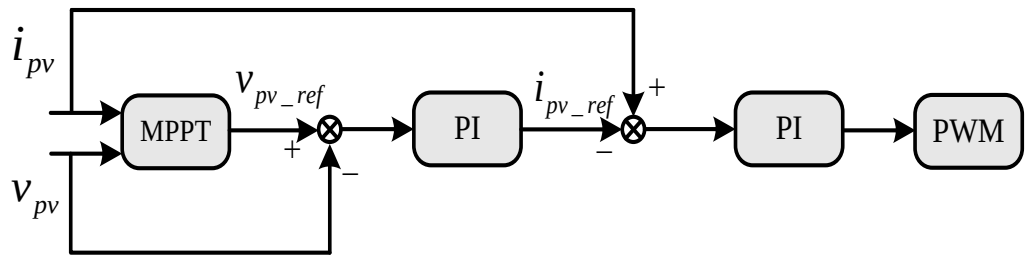
Figure 8-8 Control diagram of presented SST

The inverter stage adopts the dual loop controller, where the outer loop is the AC voltage loop and the inner loop is the inductor current loop [27]. Since it is the split phase inverter that adopted in the system, both 120V and 240V output voltages are regulated, as shown in Figure 8-8 (c) [153].

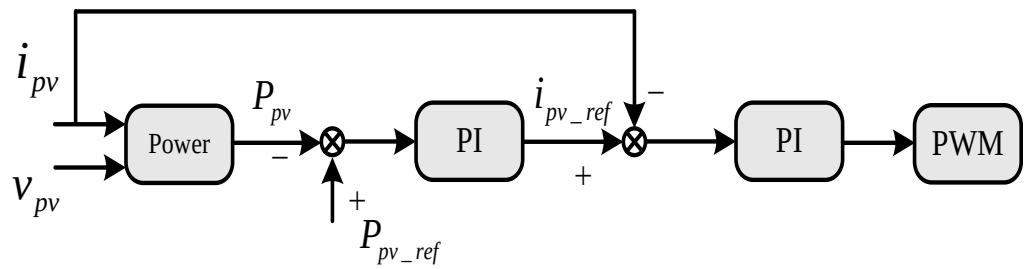
Generally, SST controls the DC bus voltage for zonal DC microgrid and supplies power for AC load. However, it will not transfer any power to zonal DC microgrid whenever the capability of local power balancing within each DC zonal microgrid is guaranteed. DC bus voltage regulated by bidirectional SST enables a smooth transfer among different grid connection operating modes, and this will be detailed in the following sections. Another possible function of SST is to detect the grid fault and then isolate the low voltage side networks from the high voltage distribution system. In this situation, the DC bus voltage will be regulated by energy storage devices.

8.3.3 PV converter control

As presented, traditional boost converter is used as the interface between low voltage PV panel and high voltage DC bus. The control of this boost converter can be divided into two cases. The first one is to operate the boost converter in the maximum power point tracking (MPPT) mode, and this is the normal case when the system operates in the grid connection mode and some operating conditions of the islanding mode. Another case is to operate the PV panel in the power tracking mode to supply the needed power of the system when operates in some other conditions of the islanding mode. Both of the cases are described in Figure 8-9, where v_{pv} is the voltage at PV panel terminal and i_{pv} is current that flows out of the PV panel.



(a) MPPT mode control



(b) Power tracking mode control

Figure 8-9 Control diagram of PV boost converter

In Figure 8-9 (a), the control diagram of MPPT mode is depicted. PV panel current and voltage are sensed for control purpose. Perturb and Observe (P&O) method is implemented to find the optimum operating voltage so that MPPT is achieved [154]. Meanwhile, dual loop control scheme is adopted to fast track the voltage reference. In this mode, since the increase of current reference will decrease the terminal voltage, the sign of inner current loop is different with outer voltage loop. When MPPT is off, the voltage tracking mode is adopted, as shown in Figure 8-9 (b). This mode occurs when the battery reaches the limitation of charging rate or SOC during the islanding mode. In this condition, PV has to balance the power within the system by assuming that the desired power is lower than maximum power

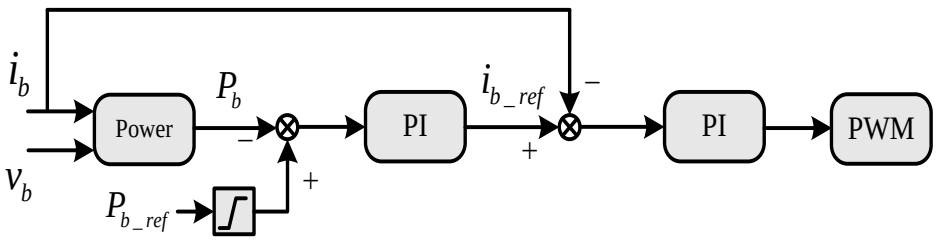
that PV can deliver. For the purpose of reduction of sensor number, PV panel voltage and current are also utilized for calculating the power. Then dual loop control is followed to track the desired power reference. The increase of power also indicates the increase of PV terminal current, thus the sign of two loops are the same. The chosen of the aforementioned controllers depends on the system operating modes, and these will be further analyzed in the next section.

8.3.4 Battery converter control

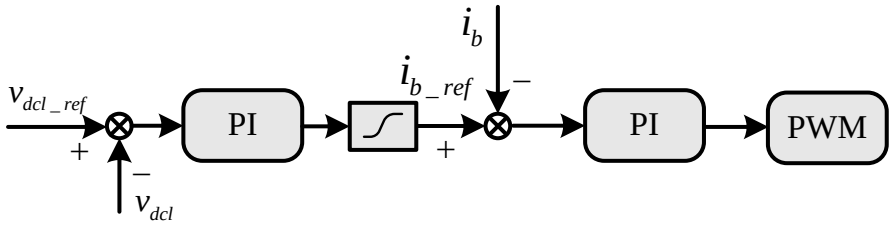
In the microgrid system, the status of energy storage devices decides the operating modes. Specifically, the operation of battery is limited by the state of charge (SOC) and the charging or discharging current [152]. When the SOC is not satisfied, the battery should stop working. Otherwise there are two operating modes for battery, as demonstrated in Figure 8-10, which are namely the power tracking mode and voltage tracking mode.

Figure 8-10 (a) shows the power tracking mode control for the battery converter, where v_b is the terminal voltage of the battery and i_b is the current that flows out of the battery pack. Operation in this mode indicates that there is no fault in the distribution side and the system is in grid connection mode. In this controller, the outer loop is the power control loop and the inner loop is the current control loop. The power reference limitation is set to 6kW for the battery pack in the presented system. Clearly, when the battery pack operates in the power limitation mode, the smooth transition can be achieved for SST since it automatically supplies the additional power for zonal DC microgrid by controlling the DC bus voltage. This characteristic will be demonstrated in later case studies. When fault occurs in the

distribution system and SST can no longer maintain the DC voltage, battery regulates the DC bus voltage and the system operates in the islanding mode. As shown in Figure 8-10(b), DC outer loop cascaded with current inner loop is implemented. Due to its bidirectional nature, the power can also be balanced within the zonal DC microgrid in a certain operating range.



(a) Power tracking mode control



(b) Voltage tracking mode control

Figure 8-10 Control diagram of battery bidirectional buck-boost converter

8.4 Power management algorithm

In order to operate the SST in the presented system as an energy router, an intelligent energy management (IEM) algorithm should be developed. As presented in [147], operating modes of zonal DC microgrid can be defined as shown in Figure 8-11, where three modes are

identified, namely active grid interaction mode, passive grid interaction mode, and islanding mode.

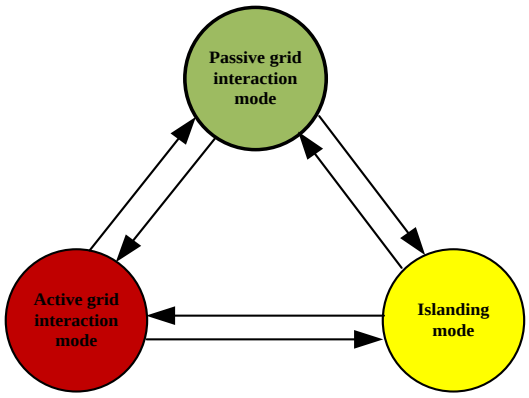


Figure 8-11 Zonal microgrid operating modes and transitions

In the passive grid interaction mode, SST controls the DC voltage. Although the zonal DC microgrid is interfaced with the distribution system, it balances the power within the network without any power being exchanged with SST. In the active grid interaction mode, due to limited power balancing capability of the DC zonal microgrid under certain operating conditions, additional power is transferred between SST and zonal DC microgrid. In the islanding mode, SST stops working and the battery regulates the DC bus. The DC zonal microgrid supplies the additional power for the load at AC side whenever extra power is available. The assumption is made in this chapter that SST, as the backup of DC zonal microgrid, can always supply enough power under the grid interaction mode by an optimized design. The whole power management algorithm aims at maximizing the utilization of PV and battery and minimizing the burden of existing AC grid, as well as ensuring a high reliability. If divided in detail, there are ten possible operating modes for the presented

system and they are shown in Figure 8-12. The nomenclature in the flow chart is defined in Table 8-4.

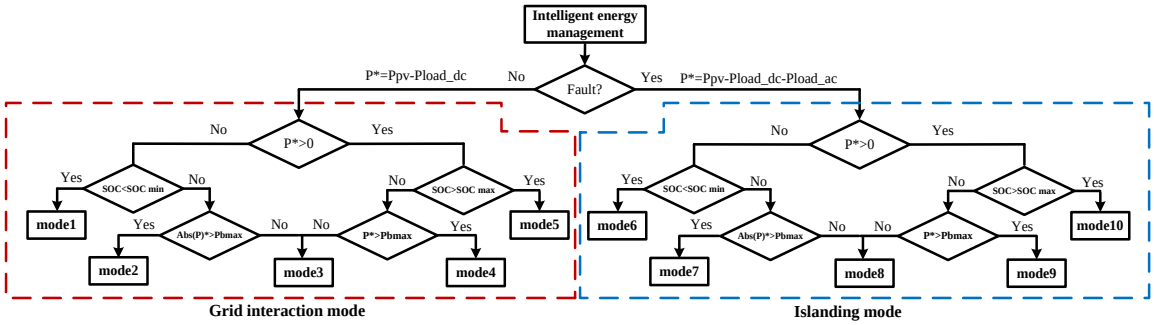


Figure 8-12 Intelligent energy management system diagram

Table 8-4 Nomenclature for IEM system

P_{pv}	Power of PV
P_{load_dc}	Power of DC load
P_{load_ac}	Power of AC load
SOC_{min}	Minimum allowed SOC
SOC_{max}	Maximum allowed SOC
P_{bmax}	Maximum allowed battery power

The division of the modes mainly depends on the operating status of the distribution system, battery SOC, and battery power. These modes are summarized and explained as following.

Mode 1: PV operates in MPPT mode, battery stops working and SST supplies the additional power for DC load.

Mode 2: PV operates in MPPT mode, battery operates in discharging power limitation mode and SST supplies the additional power for DC load.

Mode 3: PV operates in MPPT mode, battery balances the power within zonal DC microgrid, and SST only supplies power for AC load.

Mode 4: PV operates in MPPT mode, battery operates in charging power limitation mode and SST absorbs the additional power from zonal DC microgrid.

Mode 5: PV operates in MPPT mode, battery stops working and SST absorbs the additional power from zonal DC microgrid.

Mode 6: Part of loads is shedding, the system will operate into either mode 8 or mode 9 depends on the operating condition.

Mode 7: Part of loads is shedding, the system will operate into mode 8, 9, or 10 depends on the operating condition.

Mode 8: PV operates in MPPT mode and battery operates in voltage tracking mode.

Mode 9: PV operates in power tracking mode for supplying the total load power. In this mode, the power reference of PV converter is set to:

$$P_{pv} = P_{load_ac} + P_{load_dc} + P_{b\max} \tag{8-1}$$

The battery operates in voltage tracking mode and its absorbed power is fixed to charging

power limitation automatically.

Mode 10: PV operates in power tracking mode for supplying the total load power and the battery controls the DC bus voltage while no power is delivered to the load.

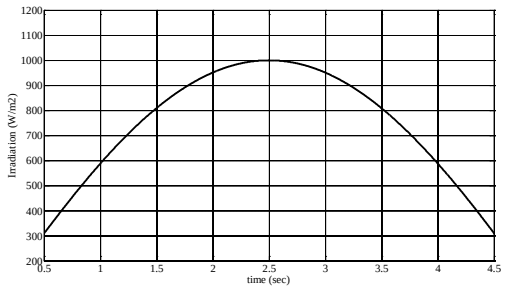
As can be seen above, mode 1, 2, 4, and 5 belongs to the active grid interaction mode. Mode 3 belongs to the passive grid interaction mode. Mode 6 to mode 10 belongs to the islanding mode. It is recommended that for a well-designed zonal DC microgrid system, a matched battery capacity needs to be designed. Then the system should operate in mode 3 for most of the time. Only when the local power balancing capability is limited, a transition to other modes occurs. Thus, the presented IEM system can maximize the utilization of PV and battery and minimize the effect to the existing AC power grid architecture.

8.5 System cases study

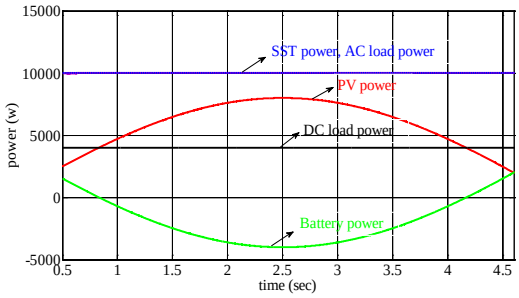
In order to verify the proposed microgrid system and the presented intelligent power management algorithm, a simulation platform is established by using the average modeling technique. The average model instead of the switching model is preferred for this large power system since it speeds up the simulation without losing the capability of capturing the main characteristics of the system. In the developed simulation platform, the power rating of SST is set to 20kVA, the maximum power of PV under the irradiation of 1kW/m^2 is set to 8kW, and the maximum charging/discharging power of battery pack is set to 6kW, all as presented before. Different load profiles are adopted to test different cases. Only parts of the cases are tested for demonstrating the main characteristics of the system due to page limitations.

8.5.1 Passive grid interaction (mode 3)

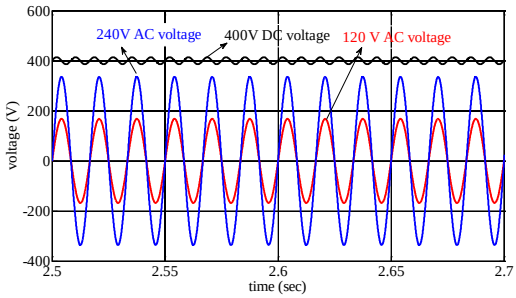
In order to emulate the operating mode 3, which is the passive grid interaction mode, the AC load for SST is set to 10kW, and DC load is set to 4kW. The key operating waveforms are shown in Figure 8-13.



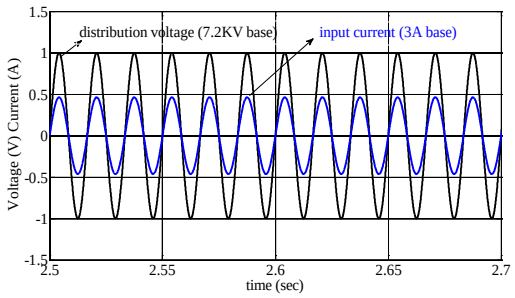
(a) Irradiation of PV panel



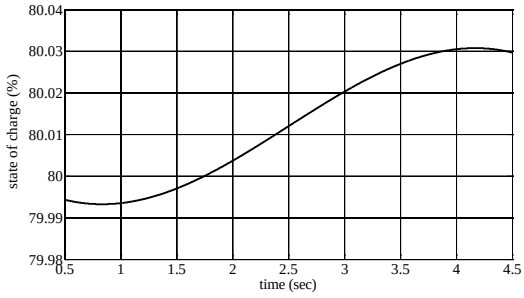
(b) Power distribution of the system



(c) low voltage terminal waveforms



(d) High voltage terminal waveforms



(e) SOC of the battery

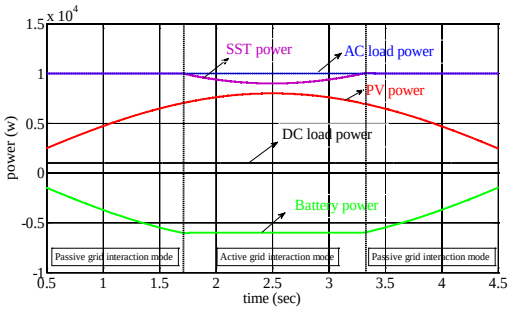
Figure 8-13 Mode 3 key operating waveforms

The irradiation of PV is gradually changing from 300W/m^2 to 1kW/m^2, and then back to 300W/m^2 to emulate the irradiation of a day, as shown in Figure 8-13 (a). Figure 8-13 (b) shows the power distribution of the presented system. The power of PV has the same trend with the irradiation. SST only supplies the AC load power, which is 10kW. Since the power of battery is within its limitation, it can balance the power between DC load and PV. Figure 8-13 (c) shows the well regulated low voltage terminal waveforms, including 400V DC and 120/240 V AC. In Figure 8-13 (d), SST input voltage and current are depicted. The current is in phase with voltage, indicating a unity power factor operation. Battery SOC is described by Figure 8-13 (e), where the initial SOC is set to 80%. The trend of SOC depends on the direction of current. A positive battery current discharges the battery and negative battery current charges the battery in the presented system.

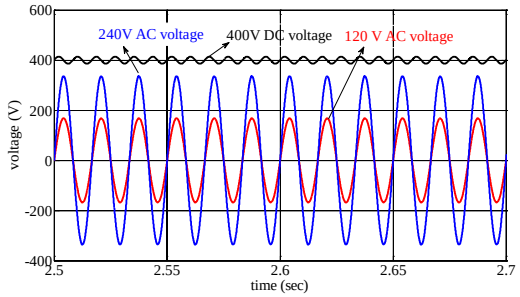
8.5.2 Transition from passive grid interaction mode to active grid interaction mode (mode 2 to mode3)

The transition from passive grid interaction mode to active grid interaction mode is demonstrated. Mode 2 and mode 3 are chosen to verify the operation, in which the AC load is set to 10kW and the DC load is set to 1kW. Key operating waveforms are documented in Figure 8-14. Figure 8-14 (a) shows the power distribution of the system. At the beginning, the power of battery pack is within the limitation and the system operates in the passive grid interaction mode (mode 3). With the irradiation of PV panel increasing, the charging power of the battery also increases. Then the system transits into the active grid interaction mode

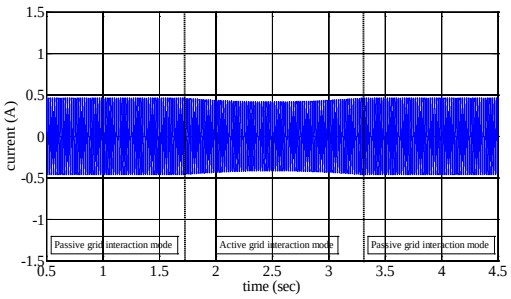
(mode 2) when battery power reaches 6kW limitation. The addtioinal power of zonal DC microgrid flows into the SST and supplies to the AC load. After that, the PV power decreases to certain value and the system operates back to passive grid interaction mode. Figure 8-14 (b) dipictes the well regulated AC and DC voltages. Figure 8-14 (c) demonstrates the input current of SST, which shows the same trend with SST power since the input voltage is fixed. Figure 8-14 (d) shows the SOC of the battery and it increases continuously. As can be seen, the transition between theses two modes is smooth and occurs automatically.



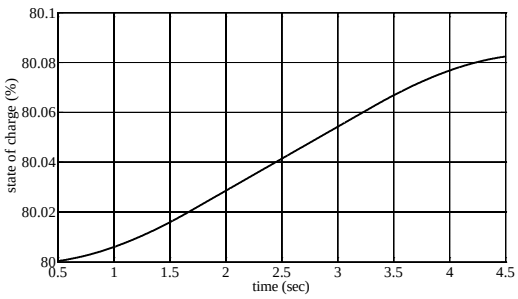
(a) Power distribution of the system



(b) Low voltage terminal waveforms



(c) Hig voltage terminal current (3A base)

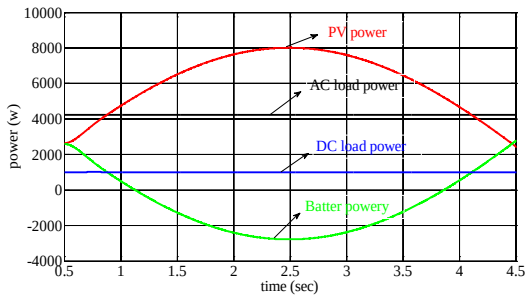


(d) SOC of the battery pack

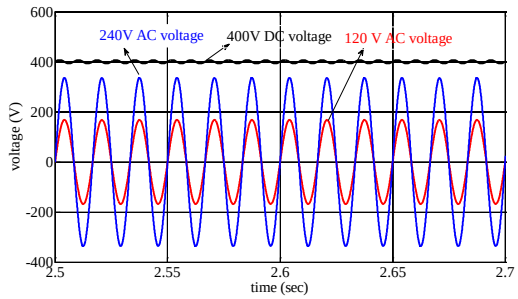
Figure 8-14 Mode trasition (mode 2 to mode 3) key operating waveforms

8.5.3 Islanding mode (mode 8)

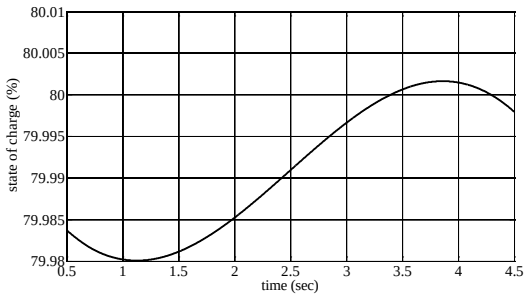
The microgrid transits into the islanding mode when fault occurs in the distribution system. How to detect the grid fault is not the emphasis and is not addressed in this chapter. For the demonstration purpose, operation of mode 8 is chosen and the waveforms are shown in Figure 8-15, where the AC load is set to 4.5 kW and the DC load is set to 1kW.



(a) Power distribution of the system



(b) Low voltage terminal waveforms



(c) SOC of battery pack

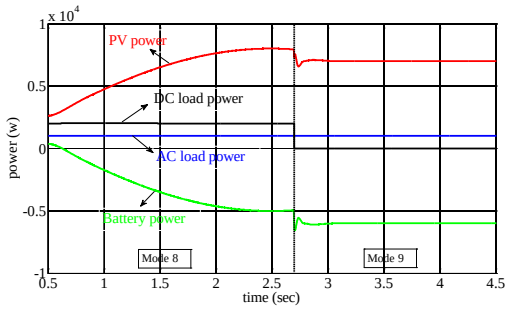
Figure 8-15 Mode 8 key operating waveforms

Power distribution of the system is shown in Figure 8-15 (a), where the battery balances the power between PV and load (both AC and DC load). Figure 8-15 (b) shows the key

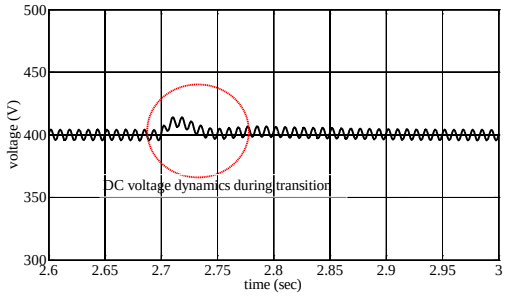
waveforms at low voltage terminal. It can be seen that the DC bus voltage is regulated well by the battery converter. Figure 8-15 (c) shows the SOC of the battery pack. When battery current is positive, the SOC decreases. Otherwise, the SOC increases.

7.5.4 Islanding mode transition (mode 8 to mode9)

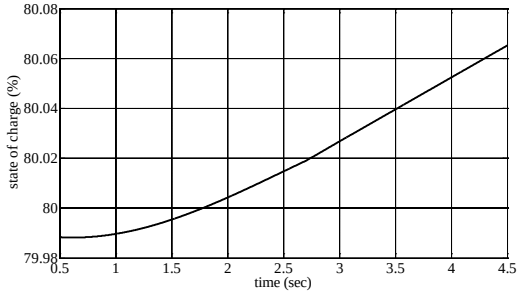
Finally, the modes transition in the islanding mode is studied. In the study, the AC load is set to 1kW, and the DC load changes from 2kW to 0kW at 2.7s. The key operating waveforms are shown in Figure 8-16.



(a) Power distribution of the system



(b) 400V DC bus voltage dynamics



(C) SOC of battery pack

Figure 8-16 Mode trasition (mode 8 and mode 9) key operating waveforms

Figure 8-16 (a) shows the power distribution in this case. Before DC load changes, the system operates in mode 8 and the battery can balance the power between PV and load. Thus PV is operating in MPPT mode for extracting maximum power available. When the DC load is cut at 2.7s, the power command of the battery is larger than 6kW and battery then operates in charing power limitation mode. PV no longer operates in MPPT mode and transits to power tracking mode. Figure 8-16 (b) illusrates the 400V DC voltage during the mode transtion. Due to the cutting down of DC load, a voltage overshoot occurs and recovers within 0.05s. SOC of the battery is given in Figure 8-16 (c), the battery is charged continuously. Clearly, the transition between different islanding modes is smooth.

It can be drawn from the simulation verification that the proposed SST based microgrid system is a promising candidate for the future smart power grid. However, the authors would also like to point out that there are still some other research opportunities that can be done for this microgrid configuration. Questions such as how to optimize the controller for each components and how to realize the seamless transition among different modes are still worth to be further investigated. In addition, the distributed controller can also be applied to the proposed system thus reduce the requirement of the communication. Furthermore, how to coordinate different SST based microgrids is also an interesting topic.

8.6 Conclusion

Solid state transformer has been discussed in recent years and researches are mainly focused on the topology evaluation and controller development. The detailed investigation and implementation of system integration of SST in the distribution system is still not so far

available. This chapter proposes a new microgrid system by integrating the SST with zonal DC microgrids. The integration issue of such a system is investigated in detail and a centralized power management algorithm is developed, which is another major contribution of the work. A system simulation platform is constructed and key characteristics of the proposed system are verified by simulation case study. The suggested SST based microgrid architecture is a promising and feasible substitute for modern distribution system.

Chapter 9 Conclusions, Contributions and Future Works

This chapter summarizes the major conclusions and contributions of the dissertation and proposes the future work.

9.1 Conclusions

This dissertation focuses on the control, design, and application of a cascaded multilevel converter based three-stage solid state transformer topology. The advanced control techniques, design methodology, and application areas of the presented SST topology are proposed.

(1) A systematic review of the solid state transformer technologies and its application in the future power distribution system is conducted in chapter 2. Four important research areas, namely high voltage power device, high voltage and high frequency transformer, SST topology, and application of SST, are reviewed and different technologies are compared. It is pointed out that the best performance of SST can be achieved by combing high voltage SiC power devices, nanocrystalline core material, and multilevel converter structures. However, the chosen of the components depends largely on some other factors, such as cost. From the controller development point of view, a cascaded multilevel three-stage SST is picked as the research target. It is pointed out that the voltage balance in the rectifier stage and current balance in the DC/DC stage are of importance to maintain the normal operation of the system. Therefore, advanced control techniques need to be developed. In addition, the potential advanced application of the SST is also highly desired.

(2) For the voltage balance controller in the rectifier stage, it is pointed out in this dissertation that coupling effect exists between the voltage balance controller and the original system controller if the feedback voltage balance control is adopted. This coupling effect makes the design of the two controllers depend on each other. Specifically, the work in Chapter 3 shows that both the reference for the voltage balance controller and the controller structure itself affect the coupling. In order to decouple the two systems, a new voltage balance controller is proposed that effectively eliminate the coupling term. The design methodology of the proposed control system is given and simulation and experimental results are provided to verify the proposed method.

(3) In order to achieve a fast voltage balance response, a modulation based voltage balance technique is proposed in chapter 4. This method directly chooses the best switch pairs according to the operation condition, and therefore guarantee the extremely fast voltage balance response. The detailed methodology to choose the switching pairs is given. Both simulation and experimental results are given to show the effectiveness of the proposed modulation strategy.

(4) Even if the voltage is balanced in the cascaded multilevel converter stage, the current may be different for the DAB converters in the DC/DC stage due to the parameter mismatch. Previous method to balance the current needs additional sensors and the performance is affected by the bandwidth of the system. This dissertation points out the active duty cycle in the rectifier stage can be a good indicator of the power balance in the DC/DC stage. Correspondingly, a novel current balance controller without using any current sensor in the DC/DC stage is proposed in chapter 5. The proposed method owns the merits of cost

effectiveness and easy implementation. Simulation and experimental results demonstrates the feasibility of the proposed method.

(5) A 3.6kV-120V, 10kVA SST prototype is developed and tested in chapter 6. The design methodology for the major components are introduced, including the high voltage input filter design, transformer design, high voltage gate driver design, and high voltage gate driver power supply design. In addition, a universal control platform is developed to enable the SST working as the energy router in the future smart grid system. The control methods proposed in chapter 3 and chapter 5 are adopted for this high voltage prototype. Experimental results are demonstrated for verifying the operation of the SST.

(6) In order to justify the cost gap between the SST and the traditional transformer and find the suitable market for SST, a novel family of SST interfaced wind energy systems is proposed in chapter 7. The proposed wind energy system using SST integrates the functions of active power transfer, reactive power compensation, and voltage conversion. Therefore, it can replace transformers and reactive power compensator in the SCIG type wind energy system. An average model based simulation is developed to verify the system performance of the proposed wind energy system. In addition, a three-phase SST topology that is suitable for the presented system is proposed and its single phase building block is analyzed and simulated to verify the functions of the SST. A SST prototype is built and experimental results are recorded to demonstrate the integrated functions of active power transfer, reactive power compensation, and voltage conversion.

(7) In order to integrate the SST with the microgrid system, the integration of SST with zonal DC microgrid system is investigated and a centralized power management strategy is

proposed in chapter 8. The presented microgrid system interfaces both AC and DC microgrid to the distribution system, therefore an active and highly compact energy router is formed. A microgrid simulation platform is established and several case studies are carried out to verify the operation principle of the proposed microgrid system.

9.2 Major contributions

The major contributions of the research in this dissertation are summarized as:

(1) A systematical literature review of the solid state transformer is presented. Key aspects for the development of SST, such as power devices, isolation transformer, topology, and application, are all summarized and compared. The grand design challenges are pointed out for the future research.

(2) A voltage balance controller based on feedback regulation is proposed for the rectifier stage to minimize the coupling effect of the voltage balance controller and the system controller.

(3) A voltage balance strategy based on the advanced modulation scheme is proposed for the rectifier stage to achieve fast voltage balance response.

(4) A current sensor-less current balance controller is proposed for the DC/DC stage, which owns the merits of low cost and easy implementation.

(5) A 3.6kV-120V/10kVA SST prototype based in high voltage Si IGBT is built and fully functional tested.

(6) A SST interfaced wind energy system is proposed with integrated functions of active power transfer, reactive power compensation, and voltage conversion.

(7) A SST interfaced microgrid system is proposed to coordinately manage the power among distribution system, ac microgrid, and dc microgrid.

9.3 Future work and suggestion

Possible future works can be conducted toward the following directions:

(1)The design of the SST prototype should be optimized to improve the efficiency. Application of SiC power devices and the nanocrystalline core can be one direction. In addition, the multi-objective optimization method could be used to achieve best performance.

(2) The design of the high voltage gate driver is very important. The commercialized gate driver can only handle up to 6.5kV IGBT. If higher voltage power devices, such as 15kV SiC IGBT, are adopted, how to design the high frequency isolation transformer with extremely small coupling capacitor should be addressed. Core-less transformer structure, such as the wireless power transfer, could be one of the solutions under the consideration.

(3) How to supply the power from high voltage DC bus if the cascaded converter structure is adopted should be investigated since this is a must in a product-level SST design. A high voltage, high step-down ratio DC/DC converter that steps down the voltage from floating DC link should be designed to achieve this.

(4) The controller design considering the interaction between each conversion stage should be addressed. A design guideline should be developed to ensure the stability of the controller

for such a cascaded power conversion system. Impedance based design methodology could be applied to such a system.

(5) For the proposed SST interfaced wind energy system, the low voltage ride through capability is not investigated yet. There are more works to do in this area. In addition, experimental works needs to be done with a real wind generator connected at SST low voltage port.

(6) The stability issues of the multiple SST connected to the grid, especially the weak grid, needs to be investigated. Corresponding damping techniques need to be proposed.

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APPENDICES

Appendix A

A.1 Calculation of input filter in the high voltage side

In the modified design, the input voltage is 3.6 KV while the power rating of the unit is 10KVA. The switching frequency of each H-bridge in the cascaded multilevel rectifier stage is set to 1.2 KHz with unipolar modulation scheme. In addition, the phase shift PWM method is adopted for reducing the harmonic components of the line current. Assuming that the peak-to-peak value of the current ripple, which is I_{rpp}, is less than 15% of the peak-to-peak value of the rated input current (7.856A), the required inductance can be calculated as:

$$L_h \geq V_{hacm}[\frac{V_{hdc} - V_{hacm}}{f_{eq} I_{rpp} V_{hdc}}] = 128mH \qquad \text{(A-1)}$$

Where, V_{hdc} is the total high voltage DC bus voltage (5700V), V_{hacm} is the maximum value of input AC voltage (5090V), and f_{eq} is the equivalent switching frequency (3.6 KHz). Choose the inductor value to be 135mH.

A2. Calculation of the capacitor in the high voltage DC link

The principle for calculating the DC capacitor in single phase system is to suppress the double-line frequency ripple voltage in certain range. The ripple voltage depends on the magnitude of ripple voltage and capacitor current. When the current is positive, the capacitor is charged, otherwise it is discharged. Assuming that charging time and discharging time are the same and the peak to peak ripple of the double-line frequency, which is 120 Hz in the design, is 15% of the DC value (1900V). The DC capacitor can be calculated as:

$$C_h = \frac{I_{hac}}{2 f_{ripple} (\frac{V_{hdc}}{3})} = 40uF \quad \text{(A-2)}$$

Where, I_{hac} is the rms value of the input current (2.778A), f_{ripple} is the 120Hz double-line frequency, and V_{hdc} is the total high voltage DC bus voltage (5700V).

A3. Calculation of key parameter of the transformer

In order to achieve ZVS in a wide range, the turn ratio of the transformer in set to be equal to the input and output ratio:

$$N = \frac{2000}{210} = 9.5 \quad \text{(A-3)}$$

Assuming that the maximum phase shift is 60° when maximum power is transferred, the leakage inductance can be calculated as:

$$L_r = \frac{(\frac{V_{hdc}}{3})^2 (\pi - \varphi)\varphi}{2D\pi^2 f_{dab} (\frac{P}{3})} = 33mH \quad \text{(A-4)}$$

Where, V_{hdc} is the total high voltage DC bus voltage (5700V), φ is the maximum phase shift (60°), D is the equivalent duty cycle (0.5), and P is the total power rating (10kVA).

A4. Calculation of low voltage DC capacitor

Assuming that charging time and discharging time are the same and the peak to peak ripple of the double-line frequency, which is 120 Hz in the design, is 8% of the DC value (200V). The DC capacitor can be calculated as:

$$C_l = \frac{I_{lac}}{2 f_{ripple}(V_{ldc})} = 21mF \qquad \text{(A-5)}$$

Where, I_{lac} is the rms value of the output current (83A), f_{ripple} is the 120Hz double-line frequency, and V_{ldc} is the total high voltage DC bus voltage (200V).

A5. Calculation of LC filter in low voltage AC side

. Assuming that the peak-to-peak value of the current ripple, which is I_{rpp}, is less than 10% of the peak-to-peak value of the rated output current (A), the minimum required inductance can be calculated as:

$$L_l \geq V_{lacm}[\frac{V_{ldc} - V_{lacm}}{f_{eq} I_{rpp} V_{ldc}}] = 0.17mH \qquad \text{(A-6)}$$

Where, V_{ldc} is the total high voltage DC bus voltage (200V), V_{lacm} is the maximum value of input AC voltage (170V), and f_{eq} is the equivalent switching frequency (21.6 KHz).

Considering the core loss of the inductor, choose the inductor to be 1mH. The filter cut-off frequency is chosen to be 1/10 of the switching frequency, which is 1080 Hz. The capacitor of the filter can be calculated as:

$$C_l = \frac{1}{L_f (2\pi f_{cut}{}^2)} = 21\mu F \qquad \text{(A-7)}$$