ABSTRACT

LENTIRO, AKALU LAMMADE. Low-Density, Ultralow-Power and Smart Radio Frequency Telemetry Sensor. (Under the direction of Dr. Paul Damian Franzon.)

Automated systems are required to better manage food sterility and identify time-temperature aseptic processing parameters to curb food safety issues. Sensor solutions can be used in conjunction with radio frequency identification (RFID) systems to meet these requirements. The integration of a temperature sensor (and other sensor types) with an RFID reader continues to be an actively researched area. The on-chip integration of sensors intended for food processing and other applications provide the opportunity for miniaturization, low-cost and ultralow power operation in extreme environmental conditions. Such sensors are also required to have a reasonable wireless range in battery-less designs and/or provide enough power when a battery is desired to be recharged wirelessly. Hence, features such as an efficient RF-to-DC power conversion at the front-end of the sensor, on-chip integration of as many of the sensor’s subcomponents as possible, and a design for ultralow power operation are critical.

This dissertation focuses on the demonstration of 3D IC design methodologies of a new type of inexpensive, small density, and ultralow power wireless CMOS temperature sensor that gathers temperature history in extreme 27-140 degree Celsius temperature ranges (with the potential to multiplex additional sensors) inside a food processing system and transmits data wirelessly. The sensor and associated core circuitry has been implemented in Tezzaron’s 0.13 μm 3D CMOS process. A significant portion of power is lost due to rectifier inefficiency during CMOS RF to DC conversions to charge the sensor’s power storage medium wirelessly. An efficient CMOS RF-DC conversion is achieved using CMOS diode threshold compensation and conduction angle enhancements to demonstrate more than 10% CMOS power conversion efficiency improvement. The sensor is designed to use optimized communication protocols and analog and digital design blocks for minimum power. The on-chip integration of components, reduction of the power supply voltage from the typical
power required by the CMOS process, subthreshold CMOS design of subcomponents and selective activation of design blocks has enabled the core components to operate with less than 1 μA of current. The power optimization has enabled the sensor to run long enough to sample and store the required data powered from a very tiny rechargeable supercapacitors. The 5 mm x 2.5 mm x 2.4 mm sensor is implemented in 0.13 μm 3D CMOS process. 3DIC technology is used to add capacitor arrays to stabilize the power supply when RF-powered.
Low-Density, Ultralow-Power and Smart Radio Frequency Telemetry Sensor

by

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BIOGRAPHY

Akalu Lentiro was born and raised in Ethiopia. He received M.S. in Electrical Engineering from North Carolina State University in 2008 and started working towards his Ph.D. in CMOS design of a smart RF telemetry the same year. Currently, he is a Sr. Hardware Engineer at Sisoft Inc., consulting at Cisco Systems and responsible mostly for pre- and post-route signal integrity analysis of both PCB and ASIC package designs for high-speed serial links and medium speed parallel-bus DDR designs. He has been working as a Signal Integrity Engineer in the same organization since 2010. He is a member of the US National Scholars Honor Society, Eta Kappa Nu and the Institute of Electrical & Electronics Engineers (IEEE).
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<table>
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<tr>
<th>Abbreviation</th>
<th>Description</th>
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<tbody>
<tr>
<td>3DIC</td>
<td>Three-dimensionally integrated circuit</td>
</tr>
<tr>
<td>AC</td>
<td>Alternating current</td>
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<td>ADC</td>
<td>Analog-to-digital converter</td>
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<td>ASK</td>
<td>Amplitude Shift Keying</td>
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<tr>
<td>BW</td>
<td>Bandwidth</td>
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<tr>
<td>CAD</td>
<td>Computer-aided design</td>
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<tr>
<td>CMOS</td>
<td>Complementary metal-oxide-semiconductor</td>
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<tr>
<td>CRC</td>
<td>Cyclic Redundancy Code</td>
</tr>
<tr>
<td>CTAT</td>
<td>Complementary-To-Absolute-Temperature</td>
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<tr>
<td>CW</td>
<td>Continuous wave</td>
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<tr>
<td>DAC</td>
<td>Digital-to-analog converter</td>
</tr>
<tr>
<td>DC</td>
<td>Direct current</td>
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<tr>
<td>DIP</td>
<td>Dual In-line Package</td>
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<td>DRAM</td>
<td>Dynamic random access memory</td>
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<tr>
<td>EDA</td>
<td>Electronic design automation</td>
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<tr>
<td>EM</td>
<td>Electromagnetic wave</td>
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<tr>
<td>EPC</td>
<td>Electronic Product Code</td>
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<td>ESD</td>
<td>Electrostatic discharge</td>
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<tr>
<td>FD</td>
<td>Frequency domain</td>
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<tr>
<td>HF</td>
<td>High frequency</td>
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<tr>
<td>IC</td>
<td>Integrated circuit</td>
</tr>
<tr>
<td>ISM</td>
<td>Industrial Scientific Medical</td>
</tr>
<tr>
<td>ISO</td>
<td>International Organization for Standardization</td>
</tr>
<tr>
<td>LF</td>
<td>Low frequency</td>
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<tr>
<td>LVS</td>
<td>Layout versus schematic</td>
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<tr>
<td>MEMS</td>
<td>Micro-Electro-Mechanical Systems</td>
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<tr>
<td>MOS</td>
<td>Metal-oxide-semiconductor</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Metal-Oxide-Semiconductor Field Effect Transistor</td>
</tr>
<tr>
<td>NMOS</td>
<td>N-channel Metal-Oxide-Semiconductor</td>
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<tr>
<td>PCB</td>
<td>Printed circuit board</td>
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<tr>
<td>PDN</td>
<td>Power distribution network</td>
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<tr>
<td>PMOS</td>
<td>P-channel Metal-Oxide-Semiconductor</td>
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<tr>
<td>POR</td>
<td>Power On Reset</td>
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<tr>
<td>PTAT</td>
<td>Proportional to Absolute Temperature</td>
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<tr>
<td>PVT</td>
<td>Process, Voltage and Temperature</td>
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<tr>
<td>Abbreviation</td>
<td>Description</td>
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<td>------------------------------------------------</td>
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<tr>
<td>PWM</td>
<td>Pulse Width Modulation</td>
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<td>RF</td>
<td>Radio frequency</td>
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<td>RFID</td>
<td>Radio-frequency identification</td>
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<td>ROM</td>
<td>Read-only memory</td>
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<tr>
<td>SDRAM</td>
<td>Synchronous dynamic random access memory</td>
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<tr>
<td>SNR</td>
<td>Signal-to-noise ratio</td>
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<tr>
<td>SPICE</td>
<td>Simulation Program with Integrated Circuit Emphasis</td>
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<tr>
<td>SRAM</td>
<td>Static random access memory</td>
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<tr>
<td>TD</td>
<td>Time domain</td>
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<tr>
<td>TSV</td>
<td>Through-silicon via</td>
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<tr>
<td>UHF</td>
<td>Ultra-high frequency</td>
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<td>VLF</td>
<td>Very low frequency</td>
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Chapter 1  Introduction

1.1  Motivation

Thanks to modern technology, the closely intertwined global economy has enabled the shipment of food products to the US from all over the world. Salmonella, e-coli and other food-safety-related infections cause over 76,000,000 illnesses, 300,000 hospitalizations and 3,000 food-related deaths in the US [42]. This has created a need for stringent processing requirements. The U.S. Food and Drug Administration (FDA) requires food processes that demonstrate conservative experimental validation techniques so that every part of the food product receives adequate heat treatment to ensure commercial sterility. Automated systems are required to better manage sterility and identify different food processing parameters to curb food safety issues. Sensor solutions can be used in conjunction with radio-frequency identification (RFID) systems to better manage food sterility and identify different processing parameters to curb food safety issues. This provides a wide range of application possibilities. RFID systems have become very popular in recent years for public transportation, retail, security access control and many other wide-ranging applications. [7] Advancements in low-density and improved battery life have further fueled these developments. Wireless telemetry has been demonstrated in low-power, short-range systems such as implanted biomedical and RFID cards and high power systems such as wireless transmission of solar power in space. [4] Technological advancements have pushed sensor applications into thermal, optical, chemical-sensing, magnetic and robotic control. Research is also underway to develop RF-powered systems.

The designs of wireless telemetry systems have many technical challenges and continue to spur research in this area. The integration of a temperature sensor (and other sensor types) with an RFID reader continues to be an actively researched area and has been discussed in several publications. The sensors intended for food processing and other similar applications are low-cost and are ideally miniaturized to meet density requirements. These sensors need to operate in extreme environmental conditions (e.g., a food-processing furnace) for a long
time, utilizing ultralow power. Such sensors are also required to have a reasonable wireless range closer to the RFID base station in battery-less designs and/or provide enough power when a micro-battery is desired to be recharged wirelessly, as in the case of this design. RF systems in higher frequencies (for example, in ultra-high frequency (UHF) band) provide longer communication ranges and reduced antenna sizes. Regardless of the range, it is difficult to extract enough power from incident RF signals for two reasons. First, FCC regulations limit the power that can be emitted from base stations, resulting in the need for the analog and digital sub-circuits in the sensor to operate at a very low power, thereby requiring a very efficient power conversion at the front-end of the sensor. Additionally, RF-to-DC rectification efficiency using standard CMOS diodes is usually poor and hence very efficient power conversion at the front-end of the sensor is required at such low power levels. Hence, features such as an efficient RF-to-DC power conversion, on-chip integration of as many of the sensor’s subcomponents as possible, and design for ultralow power operations continue to spur more research. Finally, the sensors need to ‘handshake’ with an industry standard external reader and the designed system should be small enough in size to meet buoyancy and volume requirements in multiphase food processing systems. Many publications focus on RF-DC power conversions using Schottky diodes and power conversion improvement using standard CMOS [11, 26]. Other previous works focus on low power designs by optimizing the protocols [6]. In this work, 3D IC design of a new type of sensor is introduced. The sensor uses a reduced power supply, subthreshold CMOS biasing, and clock gating to run the analog and digital circuits with less than 1 µA of current. A biasing of the CMOS diode has been employed to help compensate for threshold and maximize rectifier output voltage and efficiency of the conversion. The design of the sensor in 0.13 µm 3D CMOS process technology is described in detail in this thesis.

1.2 System Overview
This dissertation demonstrate the design, fabrication and testing of a new type of small volume (10 mm x 11 mm x 4 mm), small density and ultralow power smart RF telemetry for
aseptic processing. The sensor is inserted into a non-radiating food processing heat exchanger in the range of 27-140 degrees Celsius to continuously sample and store the aseptic processing temperature profile information as the sensor traverses the heat exchanger. While doing new sampling, the previous time-temperature conversion history of the multi-phase food particulates is simultaneously stored into memory. The sensor completes the sample and store cycle by the time it reaches the end of the allocated memory and goes into sleep mode. The sensor requires timekeeping for starting the temperature sensor and continuing data sampling every fraction of a second. A state machine creates control signals by counting the clock cycles. The timekeeping used either for data collection or digital controls needs to provide a frequency reference that is independent of process, supply voltage and temperature variations.

The sensor requires its own energy source when operating in the isolated food processing heat exchange, which exists in environments difficult for the RF wave to penetrate. The sensor must be powered from a battery or supercapacitor during the sample and store phase and taken to a remote reader once off the tube to read out the data logged. The sensor’s memory remains powered with a separate supercapacitor to retain its content. The leakage power of the memory must be optimized so it can retain its content for a long time during sleep mode with no read and write switching activities.

The sensor requires a contactless data transfer to a remote host, as wired data upload is impractical. It also needs a mechanism to recharge the supercapacitors. Compared with other wireless sensor networks (WSNs), RFID is an ideal interface because it enables the use of basic transceiver circuitry for barcode and telemetry. The sensor needs to recharge the supercapacitors and transfer its data when it sees an incident RF closer to a base station. RFID UHF Gen 2 features applications that have both reliable long read/write ranges and smaller size sensors. It can be battery-assisted (battery-powered) with a high operational lifetime and improved read rates, security, universal standard functions, interoperability and ways to select sensors in a dense environment.
The sensor should be small enough in size to meet density requirements in a multiphase food processing system. The 3DIC implementation of the sensor facilitates the integration of sub-components vertically along the z-axis, reduces power as a result of lower parasitics, and miniaturizes the design by reducing area/volume footprint.

In summary, there are many technical design challenges. The sensor is required to be as small in size as possible, 10 mm x 11 mm x 4 mm, to ensure it can fit in a capsule during data collection and can meet density requirements, and 1.28 gm/cm^3 inside the food processing system. The sensor needs to utilize a lower range of microwatts of power for improved battery life as the life of the battery has a direct relation to its size. For size, power, and cost reasons, many of the sensors’ sub-components need to be integrated into a single chip. When the use of a battery is considered a possibility, the selection of a micro-battery becomes a challenge for the operation of the sensor in extreme temperatures outside industrial and military temperature ranges. The variation in temperature affects electron mobility both in an active and passive device, and batteries discharge faster. The operation of the sensor in extreme temperatures makes many circuits have a higher resistance and, in some cases, malfunction. The dynamic and leakage power consumption of subcomponents also increases with temperature. These sub-circuits need a special design in order to compensate for temperature and function in such extreme environments. The interfacing of the sensor with a wireless system facilitates dynamic acquisition of data and power harvesting for charging supercapacitors, but the efficiency of RF-DC rectification efficiency using standard CMOS diodes is poor. The RF interfaces, including the antenna, has to be part of the design optimization in terms of size and power of the sensor. Therefore, the design and optimization of each of the individual components for the smallest possible size, ultralow power and operation in extreme environments gets very critical.

The sensor incorporates on-chip CMOS circuits for the temperature sensor, a DC-DC converter, ADC, clock generation, memory, an energy-scavenging RF-DC power converter, charger, digital control, demodulation and backscatter that are integrated with off-chip components, crystal resonator and a supercapacitor as shown in block diagram in Figure 1.1.
The crystal resonator provides a low-noise, low-frequency, temperature-compensated and accurate reference frequency to sample and store a specific volume of data. The sensor uses an antenna (or on-chip inductor coil) for energy scavenging and wireless data transmission.

![Diagram of the proposed system]

**Figure 1.1**—The proposed system

### 1.3 Contributions

This thesis explores many technical areas but the main contributions in this work are summarized as follows:

1. **Improved RF-DC Rectifier Efficiency**: A novel biasing of the diode in a standard CMOS process and improved diode conduction are introduced. The goal of the biasing the diode and increasing conduction of the diode is to compensate for the CMOS threshold and maximize rectifier output voltage and RF-to-DC power conversion efficiency at the front-end of the sensor. This is critical for delivering enough power to recharge super-capacitors.

2. **Ultralow Power and Integrated Sensor Design**: A new type of highly integrated sensor that can operate in extreme temperatures utilizing ultralow power is realized.
Since the size of the sensor’s power storage is directly proportional to its lifetime, an integrated and miniaturized ultralow power sensor that can be powered from a tiny super-capacitor is presented. Novel biasing techniques and optimized architectures including clock gating and optimized protocols are implemented to control PVT (process, voltage and temperature) variations in the system and operate circuits with an ultralow power.

The concepts in the dissertation are organized into seven chapters. Chapter 2 presents an overview of a smart sensor design. It details the challenges of realizing a small-sized and ultralow-power smart sensor. It also highlights integration, size, power scavenging and storage, low-power operation and wireless design challenges. The following chapter, chapter 3, dives into the details of the front-end part of the sensor design, including antenna coil, RF-to-DC conversions, and other RF interface designs. In chapter 4, ultralow power design methodologies of the core circuit elements including the sensor, the sub-nA clock design, and ADC/DAC are explored. This chapter also highlights the ultralow power designs using sub-threshold biasing and insensitivity to temperature, processes and voltage variation. This includes a biasing proportional to absolute temperature (PTAT) used as a temperature sensor and a biasing insensitive to temperature (bandgap) for a reference voltage to the ADC. Chapter 5 details the digital control design including the sensor finite state machine and the state machine that controls sensor-to-RFID handshaking for data transfer. Chapter 6 covers testing the sensor and results. Finally, chapter 7 concludes the thesis.
Chapter 2 System Overview

This chapter introduces the overall design of a sensor. It provides background information on system architecture of a smart sensor and describes the design constraints involved in implementing a radio frequency (RF) telemetry system.

2.1 Smart Sensor Overview

Most modern systems for biomedical and industrial applications make use of sensors to gather analog data from the “analog world” and use analog-to-digital converters (ADC) so that the data can be processed by the digital components. During the conversion, the digital block processes the digital data to store it into memory and/or to make control decisions. There are many types of biomedical and industrial sensors in modern systems, including intraocular pressure, airflow, humidity, seismic activity, humidity, et cetera. Thermal sensors, for example, provide a digital data for thermal management inside a CPU by running fans when the computer system gets too hot.

The sensors that monitor the temperature of a CPU need to continuously track temperature variations in the system. Hence, the sensors require time keeping to start the temperature sensing when, for instance, the power cycles and the sensors’ ADC continue recording data every fraction of a second until the power is down. The finite state machines of these sensors also have timing requirements to provide control signals. The timekeeping used either for data collection or digital controls need to provide frequency references that are independent of process, supply power and temperature variations.

Sensors provide even wider applications when integrated with RF, mainly wireless sensor network (WSN) and radio frequency identification (RFID). In many cases, the wireless sensors are mounted on animals or objects for continuous monitoring and data collection over a long period of time. The sensors could get powered wirelessly when the sensing occurs within the RF read range closer to the base station. In this case, the power utilization of the sensors is affected by their energy scavenging capability. In other cases, the sensors
may also require energy independence from the base station for their entire life span with no manual recharge. The sensors could be placed in isolated locations to gather sensory data, powered from a micro-battery, and brought to a base station to read the data. This is to say that the sensor designs have to operate independent of the base station for power when data sampling occurs outside the RF read range and in environments that are difficult for RF wave to penetrate—for example, a sensor floating on the surface of a liquid and monitoring the temperature inside a non-radiating container, as is the case in this study.

In many of these cases, the design of the sensors faces many technical challenges. The sensors are usually required to be as small in size as possible to ensure they can fit in an enclosure or they can be mounted on an object or inserted into the body of an animal or human. Sensors could be required to have a certain density so that buoyancy is maintained if they were to float on the surface of a liquid. The sensors may be powered wirelessly when the use of a battery is medically unsafe or when battery life is insufficient for the operation of the sensor. For many of these reasons, many of the sensors’ sub-components need to be integrated into a single chip. When the use of a battery is considered a possibility, the selection of a micro-battery becomes a challenge for the operation of sensors in extreme environments—for example, in temperatures outside industrial or military temperature ranges. The variation in temperature corresponds to a voltage magnitude as it affects electron mobility in an active device and resistance of a resistor. The operation of sensors in extreme temperatures makes many circuits malfunction. The power consumption of subcomponents also increases with temperature. These sub-circuits need a special design to be able to function in such extreme environments. Therefore, the design and optimization of each of the individual components for smallest possible size, ultralow power, and operation in extreme environments gets very critical.

2.1.1 Sensor Architecture
The design of sensors is fueled by the advancements in silicon technology and CMOS process scaling that provide high density and small parasitics transistors. This breakthrough
in micro electro-mechanical system (MEMS) and very large scale integration (VLSI) provided the ability to integrate millions and billions of transistors into a single chip also known as System on Chip (SoC) to minimize power and miniaturize sensors. [8] The SoC trend has benefited in terms of density and power reduction. Technological advancements have pushed sensor applications into thermal, optical, magnetic and chemical sensing and extended to robot control of automated systems, home security, patient monitoring, warehouse inventory, drug management, et cetera.

The sub-components of a sensor design that can be integrated onto a single chip include power-harvesting and power-conditioning components, sensors or transducers, analog-to-digital converters, memory, communication circuits, clock generators and digital controllers. The chip could also be interfaced with external components for frequency reference crystals, power backup batteries and the RF interface systems. Figure 2.1 shows a sensor that could integrate various functions into a single chip package.

![Figure 2.1—High-level sensor components](image-url)
Sensors manifest the change in electrical behavior of both active components such as transistors and passive components like resistors when exposed to the sensing environment. Temperature sensors, commonly used in many electronics applications, for example, provide electrical changes when exposed to a changing temperature. The analog-to-digital converter (ADC) provides the digital representation of the analog signals due to changes in electrical behavior. The timer provides timing of data conversions, the finite state in the digital logic and communications to from an external interface. The digital data can be stored into memory or read out to an external interface. The following sub-sections describe important design trade-offs involving size, power and interfacing.

2.2 RF Interfacing

The major part of making sensor designs smart is interfacing them with wireless sensor network (WSN) nodes and RFID. Wireless sensors have benefited from the advancements in low-power CMOS design, energy scavenging, packaging, transistor miniaturization, networking and MEMS designs. Wireless sensors monitor environmental parameters and transmit data wirelessly. The wireless interfaces facilitate dynamic acquisition of data and power harvesting for the sensor interfaces. The network of sensors can provide redundancy (or fault tolerance) for operation in extreme environments, higher accuracy and more area coverage. The maturation of RFID technology over time has enabled the integration of RFID with WSN. This has further expanded the application possibilities.

2.2.1 RFID Systems

The components of an RFID reader include a high-frequency transmitter and receiver module, a control unit and a coupling antenna or coil. The transponder is an electronic microchip with a coupling element also known as an antenna or coil that has the ability to “talk to” an RFID reader. [14, 15, 16, 17, 18] Integrated CMOS sensors with RFID are an optimal solution because Universal Product Code (UPC) barcode labels in the standard RFID
are not sophisticated enough to store complete inventory and rewrite the data. The possibility of contactless data transfer in RFID between the transponders and the reader provides many application options. RFID system includes a sensor (also known as transponder) and a base station.

2.2.1.1 RFID Transponder Types

Transponders or sensors are designed to be active, passive or semi-passive. Active sensors transmit and receive data to and from other network nodes in an RFID. These sensors are used for tracking of trains and containers and have complex circuitry for power scavenging, independent of the nodes in the network, and transmit and receive circuits to initiate communication with others in the network. [17, 18] Active sensors have a short operational lifetime because they usually use an internal battery source. These transponders are for higher speed and longer range communication with the reader, but the far field communication can be less reliable.

Passive sensors, on the other hand, are cheap tags and use basic circuitry for barcode and telemetry. They rely on a base station for power and data, independent of a battery; hence, they have a long operational lifetime. These types of transponders use reliable inductive coupling (or “near-field coupling”) to “wake up” the system, bi-directionally demodulate signals and backscatter data. [13] The communication between the reader and the transponder is similar to a primary and secondary transformer type of coupling. The voltage induced in the transponder’s antenna coil is rectified to be used as a power source.

Semi-passive sensors are expensive tags with a simpler circuit compared to active sensors. They are battery-assisted (battery-powered) with a medium operational lifetime and no integrated transmitter.
2.2.1.2 RFID Applications

The application limit of RFID is up to our imagination. There is no field where RFID is not utilized in our daily life. RFID is implemented in many areas of automated data capture that use RF for contactless identification of objects. RFID has diverse applications for contactless smartcards and electronic access control, automated electronic barcodes (EPC), and low-cost sensors as an RF telemetry, including biomedical products, implantable devices, production automation, library management, and animal identification, to name a few.

2.2.1.3 RFID Standards

RFID standards are important factors in the development of the RFID technology to ensure inter-operability between various vendors, whereas FCC regulations are mainly focused on allocation of frequency bands and power emissions. [18] An RFID reader and a transponder operate by following a set of air-interfacing rules (or protocols) that define the RF band, data rates, signal modulation, data coding, collision detection and unique transponder ID. This enables the reader and the transponder to work together by defining how a transponder receives an interrogation signal from a reader, how the transponder responds, and how the response data is modulated when the transponder responds with data.

The International Standards Organization (ISO) and Joint Technical Committee (JTC) have adopted many types of standards over the years for animal identification (ISO TC 23), packaging (ISO TC 122), freight containers (ISO TC 104), road telematics (ISO TC 204), integrated circuit cards for credit cards (JTC 1/SC 17) and automatic identification and data collection techniques (JTC 1/SC 31) and others. [18] The ISO and EPCglobal have ratified standards that incorporate incompatible, poorly performing and proprietary RFID applications and electronic products into a single economical proliferation worldwide supply chain standard. [17] The ISO 18000 standard for RFID is mostly for supply chain management. The Electronic Product Code global (EPCglobal) standard defines transitions
from barcode to Electronic Product Code. [18] EPCglobal categorizes RFID transponders into classes, as shown in Table 2.1, based on their function and operation of storing data. [18]

<table>
<thead>
<tr>
<th>Class</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Class 0</td>
<td>Read only</td>
<td>ID written once by the manufacturer</td>
</tr>
<tr>
<td>Class 1</td>
<td>Write Once</td>
<td>Data written once by the manufacturer or the user</td>
</tr>
<tr>
<td>Class 2</td>
<td>Read/Write passive tags</td>
<td>Read and write data into the memory</td>
</tr>
<tr>
<td>Class 3</td>
<td>Battery assisted semi-passive tags</td>
<td>Read and write data into the memory</td>
</tr>
<tr>
<td>Class 4</td>
<td>Battery assisted active tags</td>
<td>Read and write data into the memory</td>
</tr>
</tbody>
</table>

### 2.2.2 Frequencies of RFID Systems

The Federal Communications Commission (FCC) has allocated a range of frequencies for RFID communication between a transponder and a base station, described in Table 2.2. These frequencies range from low frequency to higher frequencies and both electric and magnetic fields are present in all of the frequency bands. The allocation of the frequency bands depend on the nature of the target application and the data transfer rates and read ranges associated with them. Higher frequencies generally provide faster data transfer rates and longer read ranges. [16, 31] Tags participate in the RFID medium depending on antenna size and distance from the reader. When a sensor that has resonance at HF is brought closer to HF RFID base station, it predominantly experiences the magnetic field and its operation is in "near-field", also known as inductive coupling. [16] UHF RFID systems, on the other hand, mostly employ "far-field" electro-magnetic radiation. But tags with the right kind of
antenna can experience the same near-field magnetic energy in UHF. Based on Faraday's law, the effect of magnetic coupling is much higher as the frequency increases.

Table 2.2—RFID frequency band [9]

<table>
<thead>
<tr>
<th>Band</th>
<th>Frequency description</th>
<th>Range (pros and cons)</th>
<th>Application Examples</th>
</tr>
</thead>
<tbody>
<tr>
<td>125 KHz-134 KHz</td>
<td>Low-Frequency (LF)</td>
<td>&lt; 0.5 m (short read range, slow data transfer rate, less sensitive to interference)</td>
<td>Access control, animal tracking, vehicle immobilizers, healthcare applications, product authentication</td>
</tr>
<tr>
<td>3 MHz - 30 MHz (13.56 MHz)</td>
<td>High-Frequency (HF)</td>
<td>&lt; 1 m (higher read rate than LF)</td>
<td>Smart Cards, Smart shelve tags for item level tracking, library Books, airline baggage, maintenance data logging</td>
</tr>
<tr>
<td>860 MHz to 930 MHz (915 MHz)</td>
<td>Ultra-High Frequency (UHF)</td>
<td>~3 m (longer read range, faster read rate, sensitive to interference-materials like water can detune the antenna for far-field communication, smaller antenna)</td>
<td>Pallet tracking, carton tracking, electronic toll collection, parking lot access</td>
</tr>
<tr>
<td>2.4 GHz</td>
<td>Microwave</td>
<td>~1 m (shorter range, highest data rate, highly sensitive to interference, smallest antenna)</td>
<td>Airline baggage, electronic toll collection</td>
</tr>
</tbody>
</table>

UHF spectrum enables long-range RFID communication a reality. This has tremendously expanded worldwide application opportunities in supply chain management. UHF has popular distribution and logistics applications and is the basis for the Electronic Product Code (EPC) standard driven through the Auto-ID Center. [16] The different versions (generations) of UHF protocols have enhanced the applications of RFID systems with improved read rates, security, tag density, universal standard functions, interoperability and
ways to select sensors in a dense environment, as shown in Figure 2.2. UHF Gen 2 features applications that have both reliable long read/write range and smaller size tags/sensors.

The effect of the environment on radio waves is also important. RFID systems surrounded by materials that have very low permeability, such as non-ferrous metals, bounce off of radio waves and those materials, like water, whose molecular reactions have the tendency to absorb shorter wave lengths at higher frequencies in far fields.

2.2.3 **Antenna Coil Design**

The detection of a continuous-wave RF signal from an RFID reader and the backscattering of data from the sensor or tag back to the reader are achieved using an antenna or coil. The wireless detection of an incoming carrier-wave RF signal and the propagation of a signal from the sensor in the form of a carrier wave are governed by basic laws of physics. This is
the result of the transformation of a time-domain (TD) guided electromagnetic (EM) wave in the form of time-varying current in a transmission line/waveguide into a frequency-domain (FD) EM wave freely propagating in space and magnetic fields varying with time. This produces induced electric fields in the reverse direction. [31]

2.2.3.1 Inductance and Resonance

As discussed in the previous section, each RFID sensor that operates in a specific frequency band has its own antenna coil to transmit and receive data and power. A spiral inductor used as an antenna has a parasitics capacitance and these parasitics capacitances resonate with the inductance at a frequency given by Equation (2.1): [34, 9]

\[
\omega_0 = \frac{1}{\sqrt{L_s C_s}}
\]

where

- \( L \) is inductance
- \( C_s \) is the total capacitance of each turn

At resonance frequency, the inductance and capacitance along the wire cancel and a current flows in response to an incident field limited only by the radiation resistance. The self-resonant frequency (\( \omega_0 \)) occurs when the inductive impedance (\( X_L \)) is equal to the capacitive impedance (\( X_C \)) and it decreases with an increase in the inductor size, since an increase in inductor size contributes to an increase in the parasitics capacitances as well. The reactance of an inductor is similar to an ideal inductor at lower frequencies. The reactance then deviates from the ideal behavior and increases at a faster rate until it reaches a peak at the inductor’s resonance frequency (\( \omega_0 \)). [34] The reactance begins to decrease with frequency beyond the resonance point, making the inductor look like a capacitor (\( \frac{1}{i\omega C} \) term dominates). If an antenna is made too large, the inductance rises beyond a certain point and then the required matching capacitor values become very small and capacitance matching becomes problematic.
The performance of the inductor is heavily dependent on the quality factor \( Q \). The quality factor is the measure of how lossy the inductor is and it is a function of geometrical parameters and frequency, as described in Equation (2.2)

\[
Q = \frac{\text{Energy stored}}{\text{Energy dissipated}} = \frac{\text{Im}(Z_{in})}{\text{Re}(Z_{in})} = \frac{\omega_0 L_0}{R_0}
\]

where \( Z_{in} \) is the impedance looking into any one of the inductor ports when the other side of the port is grounded.

Based on Equation (2.2), a “perfect” conductor with a negligible series resistance will have an infinite quality factor (or will retain 100% of its stored magnetic energy intact with no dissipation). This, however, is not practical in real-life on-chip or off-chip implementations. The energy stored in the reactive components increases relative to the dissipation by the radiation resistance and the load. [34] This makes the smaller coil antennas to become more narrow-band because the bandwidth of a resonator is inversely proportional to \( Q \). They will have more difficulty performing across all the frequencies required.

The quality factor, especially of on-chip spiral inductor implementations, is very small. The optimization of the inductor layout is critical to improve the quality factor and have the desired inductance in the smallest area possible while maintaining low parasitics capacitances and still meeting the target resonance frequency. [34] The use of wide conductors (or large diameter wires) will have an overall reduced DC and AC resistance in the windings. The windings can be designed to have wider spacing since this will generally decrease the capacitance between windings. In the case of off-chip implementations, air has a lower dielectric and the inductor can also be wound around ferromagnetic materials like iron that have a very high permeability.

### 2.2.3.2 Inductor Modeling

As discussed in the earlier sections, the resonance frequency of the antenna coil determines the size of the antenna and is a function of its wavelength. For instance, the length of an
antenna coil that works in 900 MHz range is 16.6 cm length, which is half of its wavelength. Such a long wire can be coiled to miniaturize the wire structure and get the equivalent amount of energy from an incident field. There are many variations of the spiral inductor geometry, including square, octagonal, and circular. The inductance of a spiral is the measure of how much magnetic energy it can store. [34] The geometric shapes of a spiral determine the inductance. The higher the number of windings an inductor coil has, the greater its flux density and hence an increased inductance.

The inductance of a coil with \( N \) number of turns can be determined by the ratio of total flux linkages to the current that creates the magnetic flux. [34, 9] All of the turns in a coil have a self and mutual inductance contribution. When there are \( N \) loops of current carrying conductors, the magnetic flux of the loop (self-inductance) and the result of the proximity effect occurring from near-by turn (mutual inductance) are considered. The mutual inductance of conductor coils that carry currents in the same direction is positive. Therefore, the total inductance is the self-inductances of individual segments and the positive and negative mutual inductance between the conductor turns. The larger the coil, the more computationally complex this becomes. Suppose the portions of the two turns of a circular spiral inductor with a width of \( w \) are carrying \( 1e^{-\beta z} \) current (the same magnitude and direction) and the turns are separated by spacing, \( s \), as shown in Figure 2.3. The vector magnetic potential in 3D space due to the current based on Ampere’s Law can be written in Equation (2.3) as follows: [31, 34]

\[
A_z(x, y, z) = \int_{-l/2}^{l/2} \frac{\mu_0 1e^{-\beta z}}{4\pi \sqrt{(x-x')^2+(y-y')^2+(z-z')^2}} dz'
\]  

Equation (2.3)

Assuming the current is uniform in the conductor flowing in the \( z \)-direction, the magnetic potential becomes Equation (2.4):

\[
A_z(x, y, z) = \int_{-l/2}^{l/2} \frac{\mu_0 1e^{-\beta z}}{4\pi \sqrt{x^2+y^2+(z-z')^2}} dz'
\]  

Equation (2.4)
Figure 2.3—Self and mutual-inductance of a planar circular spiral inductor

The magnetic flux on the first conductor due to the second conductor of length $l_2$ separated by spacing of $s$ can be expressed in Equation (2.5) as: [31, 34]

$$\Phi_z(x, y, z) = \int_S B \cdot ds = \int_{l_2} A_z(x, y, z) \cdot dz = \int_{l_2} A_z(0, s, z) \cdot dz =$$

$$\frac{\mu_0 l_1}{4\pi} \int_{l_2/2}^{l_2/2} \int_{r_1/2}^{r_1/2} \frac{e^{-j\beta z}}{\sqrt{s^2 + (z - z')^2}} \, dz' \, dz$$

(2.5)

where

- $B$ is the magnetic field
- $ds$ is infinitesimal portion of the conductor surface
- $l_2 = 2\pi r_2$ and $l_1 = 2\pi r_1$ are lengths of the outer and inner conductors respectively
- $r_1$ is the radius of the inner loop
- $r_2$ is the radius for the outer loop ($r_2 = r_1 + w + s$)

Equation (2.5) can also be written as Equation (2.6):

$$\Phi_z(x, y, z) = \frac{\mu_0 l_1}{4\pi} \int_{l_2/2}^{l_2/2} \int_{r_1/2}^{r_1/2} \frac{e^{-j\beta z}}{\sqrt{s^2 + (z - z')^2}} \, dz' \, dz$$

(2.6)
The mutual inductance between the loops is expressed as \textbf{Equation (2.7)}:

\[
L_m = \frac{d\Phi_0}{di} = \frac{d\phi_z(x,y,z)}{di}
\]  

\textbf{(2.7)}

There are many simplified formulas in the literature for the estimation of the inductance of the spiral inductors. However, the flow of current in more complex structures that have sharp bend angles, conductor cutouts, et cetera, is not intuitive and computationally involving. Also, there are high frequency effects that affect the distribution of current in a conductor coil, namely skin depth (\(\delta\)). Conductors, at high frequency, experience an exponential decay of current density. [34] The skin depth (\(\delta\)) expressed in \textbf{Equation (2.8)} is a function of current density (\(J\)) and depth (\(z\)) within the conductor. [34]

\[
\delta = \sqrt{\frac{\rho}{\pi \mu_0 f}}
\]  

\textbf{(2.8)}

The skin depth forces the material resistivity (\(\rho\)) to increase and make the charges to move to the surface of the conductor, as indicated in \textbf{Equation (2.9)}. This causes the current to flow at the surface of the conductor to the path of least resistivity. [34]

\[
R = \frac{\rho L}{tW} \left( \text{ohm} \frac{\text{square}}{} \right)
\]  

\textbf{(2.9)}

where

- \(R\) is the resistivity
- \(t\) is the thickness
- \(W\) is the width
- \(L\) is the length of the conductor

This problem is more prevalent in thin conductors that have high conductivity (lower resistivity). [9] The conductor current will not be attenuated by the skin resistance if the metal thickness implemented is several skin depths thick.

In summary, it is not obvious to predict the flow of the current in 3D structures, unlike simple 1D-dimensional wires where a right-hand rule (RHR) can be employed. There are many ways to solve for inductance of a spiral inductor and hence the resonance frequency to make engineering design decisions. The Maxwell equations can be approximated by using
empirical algorithms to obtain the overall inductance (both self and mutual inductance) for $N$ turns spiral. This can be very useful when trying to get initial design parameters and optimize the design. The spiral inductors can also be analyzed as segmented or lumped circuit models. A more complex process and time-involved full-fledged 2D and 3D finite-element field solvers can be employed for more accurate designs.

The lumped $\pi$ models of a conductor's self-inductance, series resistance and the associated capacitances for each segment (or turns) of an inductor, a current source for coupling between turns (mutual inductance), and more models for bends can be integrated into a circuit simulator in a segmented circuit model. [31] It gets very cumbersome to calculate and simulate for a spiral with a large number of turns.

However, the compact lumped models, shown in Figure 2.4, provide a simpler integration into a circuit simulator using $\pi$ circuit for the spiral with series resistance ($R_S$), the inductance ($L$) and capacitance ($C_S$) in the series branch and the spiral-substrate oxide capacitance ($C_{OX}$), the spiral-to-substrate parasitics capacitances ($C_{Sub}$) and resistance ($R_{Sub}$) in the shunt branches. The accuracy of $\pi$ model becomes less practical at high frequencies.
There are many empirical models to approximate the inductance value with varying level of error offset. The inductance of a spiral can be predicted accurately by Equation (2.10) [34, 9]

\[
L = 1.17 \mu_0 \frac{N^2 (D_{\text{out}} + D_{\text{in}})}{1 + 2.75 \psi}
\]  

(2.10)

where

- \(N\) is the number of turns
- \(D_{\text{out}}\) is the diameter of the spiral
- \(D_{\text{in}}\) is the width of the inductor center

and

\[
\psi = \frac{D_{\text{out}} - D_{\text{in}}}{D_{\text{out}} + D_{\text{in}}}
\]  

(2.11)

The output diameter can be approximated by \(R_i + 2N(S+W)\) for an \(N\)-turn circular spiral with inner radius of \(R_i\), trace width of \(W\) and trace separation of \(S\).
The parasitics resistors and capacitors have more intuitive expressions. An accurate expression of the series resistance that factors an increase in resistance with frequency due to the skin effect is as in Equation (2.12) [9, 34]:

$$R_s \approx \frac{l}{\omega \sigma \delta (1 - e^{-t/\delta})}$$  \hspace{1cm} (2.12)

where

- $\sigma$ is the conductivity of the conductor
- $t$ is the turn thickness
- $\delta$ is the skin depth

If skin effect is negligible, the series resistance (Ohmic resistance) of the spiral in Equation (2.13) is calculated from the cross sectional area of the inductor.

$$R_s \approx \frac{l}{W t \sigma}$$  \hspace{1cm} (2.13)

where

- $l$ is the total length of the inductor winding
- $W$ is the width of the winding
- $t$ is the thickness of the metal layer
- $\sigma$ is the conductance of the metal

The total length is approximately perimeters of the $N$-turns circle based on the median radius $R$ (i.e. $l \approx N \times \pi \times R$). The parallel plate spiral-substrate oxide capacitance ($C_{ox}$) between the conductor and the substrate accounts for most of the inductor's parasitics capacitance approximated by Equation (2.14) [31]:

$$C_{ox} \approx \frac{1}{2} \frac{\varepsilon_{ox}}{t_{ox}} lw$$  \hspace{1cm} (2.14)

where

- $\varepsilon_{ox}$ is the oxide permittivity ($\varepsilon_{ox} = 3.4510^{13}$ F/cm)
- $t_{ox}$ is the oxide thickness between the spiral and the substrate
The series capacitance \( (C_s) \), as written in \textbf{Equation (2.15)}, is mainly due to the shunt capacitance between the spiral and the metal underpass via barrel required to connect the inner end of the spiral inductor to external reference circuitry. \[ c_s \approx \frac{\varepsilon_{ox}}{t_{ox,M1-M2}} \pi \omega^2 \] where \( t_{ox,M1-M2} \) is the oxide thickness between the spiral and the underpass.

The substrate modeling includes current flowing into the substrate due to the displacement current through \( C_{ox} \) and the image current sinking through the substrate. The substrate capacitance \( (C_{sub}) \) models displacement eddy current flow in the substrate area given by \textbf{Equation (2.16)}: \[ c_{sub} \approx \frac{1}{2} C_o l w \] where \( C_o \) is the substrate capacitance per unit area, which is a fitting parameter.

The flow of Eddy current in the substrate tends to decrease the effective inductance and also add loss to the substrate modeled as substrate resistance \( (R_{sub}) \) is expressed in \textbf{Equation (2.17)}: \[ R_{sub} \approx \frac{2}{G_o l w} \] where \( G_o \) is the substrate conductance per unit area in the fitting parameter since the substrate impedance is difficult to model.

The analytical model gives the basic resonance frequency of interest to start optimization of the inductor design. Field solvers provide the most accurate representation of the model by solving Maxwell's equations numerically to model distributed 3D electromagnetic systems for a given boundary condition. \[33\] They are ideal for verifying design structures since they are generally computationally intensive. The response of the spiral inductor to an incident CW in a frequency domain can be characterized using scattering parameters (S-parameters), which represent an outgoing wave from the inductor coil as a function of the S parameter.
response of the coil from the incoming wave. The 3D solvers refine the model automatically by employing an optimized meshing and robust material frequency dependency to generate S-parameter. [30] These solvers pick initial meshing based on wavelength and add more tetrahedral during subsequent adaptive meshing to give solutions that are as accurate as possible, with a computationally reasonable memory and time need.

2.3 Power Storage and RF Power Range
The latest upsurge in sensors and handheld devices has created an increasing demand for low-power applications. Wireless sensor applications can operate in an ultralow power to conserve energy. These sensors in some cases have ways to extract energy from the environment to charge a battery or power the system directly. Sensors use energy scavenging to convert an existing source of energy into a form of power that the sensor can use and to store the power for use during data capture in the event the power source is not available in the sensing environment or the power supply is not reliable. The potential power sources in this regard are power scavenging sources including RF, solar power, vibrational energy, thermal energy and the human body. These sources of energy are not consistent and may not guarantee the operation of the system. The read and wireless power range of RFID-type sensors have increased from short range to long range in the latest designs. [9] The vibration energy sources involve the use of piezoelectric materials to generate electric potential or to use electromagnetic transducers to generate vibrations.

2.3.1 Power Storage
The transistor feature scaling and the popularity of electronics allow the decrease in size and power consumption, paving the way for devices that can be powered by batteries. However, the uses of these batteries present many challenges. They need to be either recharged periodically or replaced. The batteries also need to have the right size and weight as they are the critical components for miniaturizing the sensor and correct operation when exposed to
extreme environmental conditions. **Figure 2.5** shows the packaging off-chip sensor sub-components, with capacitors (in purple) taking the lion’s share of the area. The advancements in capacitor technology provide supercapacitors that have equivalent density to a battery and work in extreme environmental conditions.

![Figure 2.5—Packaging off-chip sensor sub-components](image)

The advancements in power scavenging sources enable higher power density compared to batteries. Finding small-size batteries that can meet the energy density requirement of a miniaturized sensor is a challenge. Also batteries have a shortened battery lifetime when operated in extreme environments. Batteries discharge at a relatively accelerated rate as operational temperature increases even for a sensor design with low-power operations. There are various types of commercial micro-batteries based on their voltage, capacity (mAh), chemistry for primary or rechargeable use, size, and packaging that are suitable for sensor applications. High temperature sensing rules out the use of the chemical batteries and these batteries, including the metal batteries that can be used in extreme temperatures, have a poor density.
The following Table 2.3 summarizes some of the batteries. The operating temperature range for best chemistry batteries is in -20 to +55 degree C and that of metal batteries in -30 to +75 degree C. A chip type electric double layer capacitors specified for operating range of -55 +125 degree C have been tested to run up to +140 degree C.

Table 2.3—The energy density of battery power sources

<table>
<thead>
<tr>
<th>Battery type</th>
<th>Vol. Energy Density Wh/dm3</th>
<th>Energy density Wh/kg</th>
<th>Self-discharge % per year</th>
<th>Cycle Life</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nickel–cadmium(Ni-Cd)</td>
<td>100</td>
<td>30-35</td>
<td>15-20%</td>
<td>300</td>
</tr>
<tr>
<td>Nickel Metal Hydride (Ni-MH)</td>
<td>175</td>
<td>50</td>
<td>20%</td>
<td>300</td>
</tr>
<tr>
<td>Lithium-ion(Li-ion)</td>
<td>200</td>
<td>90</td>
<td>5-10%</td>
<td>500</td>
</tr>
<tr>
<td>Alkaline</td>
<td>300</td>
<td>125</td>
<td>4%</td>
<td>1</td>
</tr>
</tbody>
</table>

2.3.2 RF Power Range

Sensors and their base station (or readers for RFID systems) require their own antenna to be able to communicate. A reader transmits CW to the sensor by modulating an RF signal in the correct frequency band. When a sensor lies within the range of the reader, an alternating RF voltage is induced on the sensor coil (or antenna) and is rectified in order to provide a DC supply voltage for the operation of the sensor.

The power received by the sensor is a direct function of the antenna size of the base station and its magnetic field strength. A larger antenna has a lower signal-to-noise ratio (SNR) and it needs to be shielded to remain within the Federal Communications Commission (FCC) power emission requirements. Antennas in general have unique characteristics depending on the frequency of operation. At low frequency, the sensors’ antennas are inductively coupled
and require many coil turns to get enough inductance and consequently enough induced voltage, because the induced voltage by the sensor’s coil is directly proportional to frequency. At high frequency, smaller sized antenna coil can be used for longer range communication. At UHF and microwave, a very small antenna coil can be employed for medium to long range communications, which also significantly helps in miniaturizing wireless sensors. The UHF antenna coils are usually implemented as inductive matching structures like folded dipoles to optimize power delivery. [9]

The radiation patterns of sensors with a dipole antenna are orientation and polarization depending on the antenna of the base station. The three regions of an antenna are reactive near-field, and radiating near-field and far-field, as depicted in Figure 2.6. The reactive near field is in close proximity to the antenna and is predominately reactive. The field strength in the form of a standing wave decreases in $1/R^3$ fashion in this region. A shift in angle can cause no coupling to occur. Near-field coupling occurs within one wavelength of the electromagnetic field. [8] The radiating near field is a region between reactive near field and far-field with both standing waves and traveling waves from both regions. The field strength in this region decays at a rate of $1/R^2$. The field distribution in the far-field region is predominately travelling waves and the field decreases in strength at a rate of $1/2$. [6]
The power received \( P_{RX} \) by an antenna or coil in the radiating near field can be expressed using Friis’ transmission formula (see Equation (2.18)) [6]:

\[
P_{RX} = \frac{(P_{TX} \cdot G_{TX}) \cdot G_{RX} \cdot \lambda^2}{(4\pi)^2} = \frac{(EIRP) \cdot G_{RX} \cdot \lambda^2}{(4\pi)^2}
\]  

(2.18)

where

- \( \lambda \) is wavelength (which is 33 cm for a 900 MHz system)
- \( G_{RX} \) is the gain at the receiver
- \( G_{TX} \) is the reader antenna gain
- \( R \) is the distance between sensor and reader with a \((4\pi R)^2\) hypothetical sphere area
- \( P_{TX} \cdot G_{TX} \) is the effective radiated power \((EIRP)\) by a base station which is limited by the FCC regulations

The received power \( P_{RX} \) diminishes quadratically with distance. The received power using an inductor coil decays even faster, as shown in Figure 2.7.
Figure 2.7—Wireless power range using off-chip antenna and coil

Figure 2.7 is an estimate for an industry standard RFID reader that has a maximum power of 36 dBm, an antenna of gain 7 dBi and a 3.1 dB loss from a shielded 25 ft coaxial antenna cable. This propagates a maximum power of 32.1 dB. The received power using an inductor coil is with an assumption of an AWG-30 inductor coil with a diameter of 0.25 mm, given by Equation (2.19):

\[ P_{RX} = \frac{A_{eff} \ast EIRP}{4 \pi R^2} \]  

(2.19)

where

\[ A_{eff} = h \ast (r_{major} - r_{min}) \]  

is the effective coil area wound around a dielectric of height (h), with the inner and outer radiiuses as \( r_{min} \) and \( r_{major} \) respectively.

Power delivery efficiency increases with an increase in transmit power. Additional transmit power (or extended transmit time) is required if the sensor nodes in a network are dense. The sensor needs high active current to achieve high transmit power level in the range of 0dBm (1mW), which is challenging to achieve with weak energy scavenging and backup micro-
batteries. On the other hand, the data payload and traffic pattern of sensors is not as demanding as a wireless LAN. The rate for a sensor usually is in the range of a few kbits/s and the data packets and patterns are predictable, which significantly reduces the energy/bit required to transmit and receive data. [9, 11] However, wireless sensors need to receive sufficient power to run the sensor’s digital block during an RFID inventory session and charge the batteries that run the core circuits and the memory. Yet the sensor design has to operate at ultralow power. The actual power received by a sensor could be significantly less, depending upon several loss mechanisms, including antenna mismatch. The standing wave ratio (SWR), in Equation (2.20), measures the amount of reflections due to antenna mismatch.

\[ V_{SWR} = \frac{V_{RF} + V_{ref}}{V_{RF} - V_{ref}} \]  

where

- \( V_{RF} \) is the incident wave
- \( V_{ref} \) is the reflection wave due to possible antenna mismatch

The impedance matching network can be designed using L-network connected through a 50Ω feedline trace. The equivalent RLC of the antenna can be calculated and a parallel or series-parallel RLC matching circuit can be used as matching network. **Figure 2.8** shows examples of an antenna matching network with inductance, parallel capacitance and damping resistance. The specific component values for \( L \) and \( C \) can be determined based on a mismatch factor that can be verified by the Voltage Standing Wave Ratio. The impedance matching becomes a challenge in large antennas where inductance is normally very large.
When the sensor is in the radiating range of the reader, the incident AC (RF) signal starts to get rectified to DC to charge up the capacitor and supply a constant DC for the sensor system. The small DC voltage is multiplied to improve the low amplitude obtained from the weak incident RF and provide practical voltage for the system. Usually low-threshold Schottky diodes are used for efficient charge pumping from the UHF reader’s weak incident RF signal and the charge is converted to a DC supply voltage and stored in a high density and high-temperature-resistant supercapacitor or non-chemistry battery when the sensor is in close proximity with RFID reader.

2.4 Low-Power Sensors

The main design goal of portable electronics is low-power operation to maximize battery lifetime by reducing energy per cycle. Hence, energy efficiency is the most important aspect of sensor and medical telemetry design to operate the devices with a micro battery. The design for low power and low cost involves trading off power with integration. The integration of components in a single chip can be traded off with power in a multi-chip architecture that involves optimized analog designs in SiGe processes and low-power digital designs in a standard CMOS process. [8] The multi-chip solutions increase size, complexity and cost of system level design and packaging. CMOS sensor designs have become attractive
due to scaling of transistor feature size, low cost of fabrication and the possibility of putting analog and digital designs in the same chip.

The transistor scaling lowers power and improves speed due to improvement in doping level of the substrate. Transistor scaling also reduces vertical and lateral dimensions miniaturizing the overall IC. However, the threshold voltage and supply voltage has not scaled with transistor dimensions. [10] Figure 2.9 shows the ITRS roadmap for supply voltage and gate length.

Short channel effects such as drain-induced barrier lowering and punch-through, surface scattering, and velocity saturation inhibit some of the benefits of transistor scaling. As the gate length decreases and starts to fit the depletion-layer widths of the source and drain junction regions, the gate bias not only depletes the channel in the vertical direction (gate length direction), but also in the lateral direction (gate width direction). [10] The electric field, from the gate to the channel, pulls electrons to the surface interface between the gate oxide and the silicon substrate, which tend to scatter and, in some cases, trap electrons, thereby reducing the mobility of electrons along the interface. [10] As the channel length gets smaller, the horizontal electric field strength increases, yielding higher electron velocities, which approach thermal velocities where the thermal scattering of electrons reduces the slope of velocity with increasing electric field, causing velocity saturation. [10] This is not an issue in MOS processes that have trench isolation since the gate is surrounded by dielectric and there is no semiconductor region beyond the gate edges. [10] The surface potential (Vds) as a function of position is constant for long-length transistors.
2.4.1 Design for Low Power

Low-power and small area wireless CMOS sensor designs need optimized power to run the sensor’s digital block, the core circuits and the memory. The sensor operation life span is determined by the energy consumption of each design block. There are many ways to reduce power. The design sub-blocks of the sensor need periodic wake-up and low-power operation to save power. Most sensors stay idle when not actively collecting data, which is a portion of the sensor’s lifetime. The sub-components need to be turned off when not actively in use and woken up just before the sensor goes operational. The power of the RFID finite state machine can be managed separately so it can be turned off, for example, when the digital control is not managing communication with the base station. Also the internal power of the sensor could be cutoff whenever the sensor is not actively doing sample and store. The power of the wakeup circuit can be supplied through a backup power source, like a battery. Large capacitors can also be used as a backup source. Sensors could be powered from a supercapacitor or a battery during the sample and store cycle until the end of the allocated memory is reached.
The design of integrated ultralow power sensors (other micro-battery supplied applications) can also be achieved by reducing the supply voltage below the threshold of the transistor (sub-threshold) for some parts of the chip sub-components, as shown in Figure 2.10. The supply voltage scaling to reduce dynamic power, Equation (2.21), is a trade-off with the circuit performance and it is not appropriate for all interfaces. The supply voltage reduction impacts frequency of operations of CMOS circuits. High supply voltage circuits can function at higher frequencies and power consumption is mainly dynamic due towitching activity by circuits. The requirement for ultralow power operation can be met when high performance operation of the device is not a requirement.

\[ P_{\text{dyn}} = \frac{E}{T} = \frac{1}{T} \int_0^T V_{dd} I_{dd(t)} \, dt = \frac{V_{dd}}{T} (T f C V_{dd}) = C V_{dd}^2 f \]

where

- \( f \) is the switching clock frequency
- \( I_{dd(t)} \) is the instantaneous current conduction
- \( dt \) infinitesimal small delta time
- \( C \) is the parasitics capacitance.

Whereas lower supply voltage circuits function at lower frequencies and power consumption is predominately static, CMOS transistors, which are non-ideal switches, consume leakage power, as shown in Equation (2.22), even when they are turned off.

\[ P_{\text{stat}} = V_{dd} I_{\text{leakage}} \]

where

- \( V_{DD} \) is the supply voltage
- \( I_{\text{leakage}} \) is the leakage current of the circuit

Leakage power could be reduced using less parasitics in the circuit and reduced supply voltage. Reduced transistor parasitics is not directly proportional to dynamic power. The transistor technology scaling provides reduction in parasitics and supply voltage. These smaller feature size transistors still have to be optimized for reduced leakage and dynamic powers.
2.4.2  Current Mirrors

The supply voltage can be reduced and made independent of the global power supply by stacking multi-transistors in a cascade configuration in current mirrors. The leakage current can be controlled by using a cascode pull-up and pull-down transistors. These transistors provide a gated rail when the active node in the circuit is being pulled-up or pull-down. When the circuit is idle, the gating transistors provide a high impedance path to the supply rails. The pull-up (and pull-down) transistors need to be sized weak enough to lower leakage and strong enough to match the robustness of the system [10]. The sub-threshold biased designs limit the dynamic range (or amplitude) and hence the resolution of the ADC and other analog circuits. An increased transconductance can be obtained by sub-threshold biasing of low frequency analog circuit design. The duty cycle of the sensing and digital signal processing components is very small. The power consumption of these components can be optimized with design for reduced leakage and algorithmic sleep and power down. 

The interface circuits for wireless communication contribute the higher portion of the power

Figure 2.10—Effect of supply voltage on MOS dynamic power consumption
budget. The use of high frequency reduces the size of components (for example, antennas and capacitors) to be integrated but this requires a trade-off with a high power requirement for high frequency operations, as the transistors that are designed to operate at high frequencies need to be biased with higher current. Low-power transceivers for wireless sensor designs are based on lowering the data rate and scaling the transistor technology while still maintaining communication at the carrier frequency of interest.

The transistor’s scaling helps to meet the required unity-gain frequency easily and optimize it for ultralow power operations. This makes sub-threshold biasing more feasible. A CMOS with a gate-to-source voltage \( V_{gs} \) lower than the threshold of the transistor in sub-threshold operation acts like a SiGe process (BJT) device and the drain current given is expressed in Equation (2.23), as [2]:

\[
I_{ds} = \mu_{eff} C_{ox} \frac{W_{eff}}{L_{eff}} (m-1) \mu_T^2 \exp\left( \frac{V_{gs} - V_{th}}{m V_T} \right)
\]  

(2.23)

where

- \( m \) is the sub-threshold factor in the range of 1 to 3, \( V_g = \frac{KT}{Q} \).
- \( \frac{W_{eff}}{L_{eff}} \) is the aspect ratio of the transistor
- \( \mu_{eff} C_{ox} \) is the channel charge-carrier effective mobility and gate oxide capacitance per unit area, respectively

Applying Taylor’s series expansion to the exponential term in Equation (2.23) is Equation (2.24):

\[
I_{ds} = \mu_{eff} C_{ox} \frac{W_{eff}}{L_{eff}} (m-1) \mu_T^2 \left\{ 1 - \frac{(V_{gs} - V_{th})}{m V_T} + \frac{1}{2} \left( \frac{V_{gs} - V_{th}}{m V_T} \right)^2 - ... \right\}
\]  

(2.24)

Since \( V_{gs} - V_{th} \) is small, the higher order terms can be neglected, and Equation (2.24) can be approximated as Equation (2.25):

\[
I_{ds} = \mu_{eff} C_{ox} \frac{W_{eff}}{L_{eff}} (m-1) \mu_T^2 \left( \frac{V_{gs} - V_{th}}{m V_T} \right)
\]  

(2.25)
\[ I_{ds} \approx \mu_{\text{eff}} C_{\alpha V} \frac{W_{\text{eff}}}{L_{\text{eff}}} (m-1) \frac{1}{V_T^2} \left( 1 - \frac{V_{gs} - V_{th}}{mV_T} \right) \]  

(2.25)

A transistor bias is used to reduce an increased noise figure (NF) due to the MOS transistors operating in a weak inversion region. [10] Also, a current mirror design for temperature, voltage and process variation for all the circuits within a block is very important. The sub-threshold design, despite its low-power advantage, has design challenges, including device modeling and device mismatch. A current mirror that reduces the effect of supply voltage variation is needed in the design of digital-to-analog converters (DAC) or analog-to-digital converters (ADC), sampling clocks and other important components. Stable frequency reference for time-keeping is very important in sensor design. The data collected by sensors depends on the reference clock source since the timing and frequency of data sampled is critical. This affects the resolution of the ADC, the response of the finite state machine in the system, and the time the sensor will be active and running off of a battery or supercapacitor. Sensors utilize storage devices to store sensory data and processing routines, as applicable. High-density and low-power memory design options are critical for most sensor designs. A low-power SRAM that has high density and low latency can be designed without the significant challenge of designing the SRAM in sub-threshold.
Chapter 3   Sensor RF Front-End Design

3.1 Introduction

The proceeding chapters cover the design, fabrication and testing of a new type of small area, small density, low-power and low-density wireless CMOS temperature sensor using 3D IC. The 3D IC is a vertical multi-tier stacking of integrated circuit (IC) designs as wafers, dies, or devices. [40, 41] The integration of sensor sub-components vertically along the z-axis can help facilitate integration of the sub-components, reduce power as a result of lower parasitics, and miniaturize the design by reducing area/volume footprint. However, low-power and low-data-rate sensors will not take advantage of the reduced interconnect delay in the 3D IC process as performance optimization is not the main challenge in these designs. Also, sensors expected to operate at high temperatures with logic designs on two or more tiers of the 3D may experience thermal issues due to limited thermal conductivity. [40, 41]

The sensor under discussion is used for storing time-temperature history inside a food processing system for easier gathering of food safety parameters. The sensor has been designed to be inserted into particulates during thermal processing of multiphase foods, to sample data every second until it reaches the end of memory, and to then respond with data when interrogated by an external industry standard RFID reader in 860-960 MHz frequency range. Batteries or supercapacitors power the sensor and its memory during the sampling phase. In the presence of an RFID, the incident RF signal is used to charge the supercapacitors, power the digital block of the sensor, and transmit data back to the reader. The sensor must receive sufficient power to run its digital block during an RFID inventory session and charge the supercapacitors that power the core circuits and the memory.

The design description of the sensor is broken into three main design sub-blocks. These design sub-blocks include the RF front-end design, the digital logger design, and digital logic design. In this chapter, we will be focusing on the front-end of the design, including the on-chip coil. The purpose of this design block is to modulate and demodulate data to and from the RFID reader and scavenge power from the carrier wave in the UHF band when the sensor
is in the range of the RFID reader. When the sensor lies within the range of the reader, RF voltage is induced on the sensor’s internal coil (or an optional external antenna) which is rectified in order to provide a DC supply voltage for the sensor’s operations. A baseline study has been done to power a sensor directly off an RF (AC) source, without AC to DC rectifications. [19] This AC-powered approach greatly simplifies the front-end hardware complexity by not requiring RF-to-DC power conditioning. This work is not covered in this thesis. The direct powering of the sensor from an RF source is infeasible in the reflective environment in which the proposed sensor will work. The sensor’s front-end block includes an on-chip coil (or interfaces for the optional antenna), modulator/demodulator, rectifier, limiter, power regulator, and DC-to-DC converter and charger, as shown in Figure 3.1.

![Figure 3.1—Block diagram for the front-end system](image)

The sensor design and associated core circuitry has been implemented in a Tezzaron 0.13 µm 3D CMOS process. The 3D Tezzaron IC process is a multi-tier wafer stack fabrication based on the Chartered 130 nm Low Power CMOS process. The process stacks top and bottom wafers through micro-bumps and an optional DRAM device with I/O pads. [32] The through-
silicon vias (TSVs) connect the optional memory wafer bonded to the back side of the top (WTOP). Many dummy TSVs are also used in the process for thinning and metallization. The input and output pads of the chip were designed on the top tier for signals coming into the chip and going out of the chip.

The top (WTOP) and bottom (WBOTTOM) wafers are bonded face-to-face. Each wafer has 6 metal layers. [32] The top wafer is flipped left-to-right, aligned, and bonded to the bottom tier to minimize the parasitics load through shorter via stubs. [32] The complete simplified 3D stackup with the thickness of the metals layers indicated is shown in Figure 3.2.
Figure 3.2—Simplified face-to-face stack-up of Tezzaron 3D process

The geometry details of the TSV and the metal conductor are summarized in Table 3.1 and Table 3.2. The stackup for the dielectric layer is provided in the table in the appendices.
Table 3.1—3D process TSV depth [32]

<table>
<thead>
<tr>
<th>Description</th>
<th>Depth (microns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>From top of STI to bottom of TSV</td>
<td>5</td>
</tr>
<tr>
<td>Top of BSM to bottom of TSV</td>
<td>0.3</td>
</tr>
</tbody>
</table>

Table 3.2—3D process conductor layer stackup [32]

<table>
<thead>
<tr>
<th>Conductor</th>
<th>Thickness (microns)</th>
<th>Variation (+/- %)</th>
<th>EP specification top and bottom width W drawn/W Si (tw/bw) (microns)</th>
<th>Variation (+/- %)</th>
<th>Si process top and bottom space S drawn/S Si (ts.bs) (microns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TM</td>
<td>0.86</td>
<td>15</td>
<td>0.44/(0.50/0.42)</td>
<td>10</td>
<td>0.46/(0.40/0.48)</td>
</tr>
<tr>
<td>M5</td>
<td>0.42</td>
<td>15</td>
<td>0.20/(0.22/0.20)</td>
<td>15</td>
<td>0.21/(0.19/0.21)</td>
</tr>
<tr>
<td>M4</td>
<td>0.42</td>
<td>15</td>
<td>0.20/(0.22/0.20)</td>
<td>15</td>
<td>0.21/(0.19/0.21)</td>
</tr>
<tr>
<td>M3</td>
<td>0.42</td>
<td>15</td>
<td>0.20/(0.22/0.20)</td>
<td>15</td>
<td>0.21/(0.19/0.21)</td>
</tr>
<tr>
<td>M2</td>
<td>0.42</td>
<td>15</td>
<td>0.20/(0.22/0.20)</td>
<td>15</td>
<td>0.21/(0.19/0.21)</td>
</tr>
<tr>
<td>M1</td>
<td>0.31</td>
<td>15</td>
<td>0.16/(0.20/0.18)</td>
<td>15</td>
<td>0.18/(0.14/0.16)</td>
</tr>
<tr>
<td>Poly</td>
<td>0.16</td>
<td>10</td>
<td>0.13/(0.13/0.13)</td>
<td>10</td>
<td>0.18/(0.18/0.18)</td>
</tr>
<tr>
<td>BSM</td>
<td>0.7</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

In this design, the top-tier (WTOP) wafer implements the logic, including an on-chip coil, and the bottom tier (WBottom) houses the capacitor array to absorb short power cycles and stabilize the power supply during sample and store operations. The following sections describe each design sub-block in more detail.

3.2 On-chip Spiral Inductor Design

A circular on-chip spiral inductor that provides higher $Q$, sufficient antenna gain and ease of layout has been implemented. The geometry of a circular spiral inductor is specified by the number of turns ($N$), metal width ($W$) and spacing between adjacent turns ($S$). The number of
turns and lateral dimensions determine mostly the inductance of the coil and both the vertical dimensions and lateral dimensions affect the parasitics capacitances and resistances. The time-varying current flows in the conductors in a series that forms the spiral due to the time-varying voltage in these segments of the spiral-creating inductance. This time-varying current causes out-of-phase electromagnetic behavior in the frequency domain. The coil has been implemented in the back metal layer for its largest thickness in the Tezzaron’s 3D CMOS process metal stackup and hence it has low inductor series resistance and spiral-to-substrate oxide capacitance. The series resistance could have been reduced further by strapping multiple metal layers together but this would be traded off with an increase in spiral-to-substrate oxide capacitance. Figure 3.3 shows the cross-section of the spiral inductor in the stackup of this process technology.

**Figure 3.3**—Cross section of on-chip spiral inductor

Field solvers provide the most accurate representation of the model by solving Maxwell's equations numerically to model-distributed 3D electromagnetic systems for a given boundary condition. [33] HFSS, an EM 3D field solver from Ansoft, has been used for an accurate modeling of the circular spiral inductor in a frequency range for the selected simulation
parameters based on the data from the preliminary empirical model approximations for the target resonance frequency in the 860 MHz to 960 MHz range. The coil drawn in Cadence Virtuoso Layout could also have been imported into HFSS as a GDS file using the correct stack-up technology file to verify the design. The structure has been drawn by selecting the desired inner radius, width, and spacing of the spiral inductor with vias and underpass connections. The materials for the conductor, oxide, substrate, and air with the corresponding relative permittivity, permeability, and conductivity, as required, have been defined using the Tezzaron’s 3D CMOS process stackup data. A radiation boundary airbox is drawn and a PEC boundary assigned. A driven terminal solution type in HFSS and Waveport ports between the structure and ground has been assigned for both terminals to emulate external interface of the on-chip coil to the sensor and emulate ground-signal-ground (GSG) probing. The multilayer 3D structure drawn in HFSS is shown in Figure 3.4.

![Figure 3.4—Layout of a spiral inductor, not to scale](image)

3.2.1 **Coil Design Verification**

There are many design parameters to gauge the electromagnetic frequency-dependency behavior of the spiral inductor design. The scattering parameters (S-parameters) generally
capture the steady-state behavior of linear time-invariant (LTI) passive components in a circuit. The response of the spiral inductor to an incident CW in a frequency domain can be characterized using these S-parameters. At resonance frequency, the incoming wave at input port of the spiral coil compared to the reflected wave in the same port \((S_{11})\) appears open. **Figure 3.5** shows simulated \(S_{11}\) for the 7-turn circular spiral inductor. This spiral inductor with a higher number of turns has many parasitics series resistances, capacitances and inductances, creating multiple resonance frequencies in a wide frequency range at a higher GHz and lowering the quality factor. The input reflection coefficient \((S_{11})\) plot shows resonance only at the frequency of interest since the frequency range in the plot is lowered to a 900 MHz range (below 1.8 GHz). The null is located at about 910 MHz, close to the central frequency in 860–960 MHz band.

**Figure 3.5**—\(S_{11}\) (left) and VSWR (right) plots of the coil
The plot of voltage standing wave ratio (VSWR) as a function of frequency characterizes the effect of reflection on transmitted waves due to loss at the antenna coil. The magnitude of the VSWR is the lowest at resonance frequency. Multiple resonance frequencies in a wide frequency range can be observed with the VSWR as well.

A far-field gain pattern has been simulated for the coil and the total field has been plotted from one end of the coil for an example frequency of 950 MHz, shown in the pattern in Figure 3.6.

![Figure 3.6—Far-field radiation pattern plots](image)

The width of the inductor trace selected for the design gives optimum quality factor. The highest quality factor occurs at the resonance point as expected. The inductance value is high, since we are using multiple turns to help increase the flux linkages. Figure 3.7 displays the plot of impedance as a function of frequency. The plot shows the real and imaginary parts of the impedance vary throughout the frequency range and give zero imaginary impedance at the self-resonant frequency. It also shows that the optimum width used has helped to keep the
impedance lower. These high-$Q$ passive components can guarantee a low insertion loss and high return loss.

![Simulated impedance plot](image)

**Figure 3.7—Simulated impedance plot**

The charging of the battery-assisted sensor in this design requires communication with the RFID reader in the UHF band and starts the power conversion processes using the charge pump circuit. The weak RF power coupled through the coil (or an external antenna) uses multi-stage RF-to-DC rectification. Then a capacitor deposits charge (or energy) in the final stage of the charge pump.

The capacitor provides an additional juice for running the sensor, besides the external batteries or supercapacitors, during sample and store. In this design, the charge (or energy) gets deposited in the capacitor to stabilize power charge cycles. The voltage in the final stage of the rectifier has a ripple as a result of the RF source. The ripple voltage can be expressed as in **Equation (3.1).**

$$V_{\text{ripple}} = \frac{i_{\text{out}}}{f_{\text{RFout}}} = \frac{V_{\text{out}}}{f_{\text{RFout}}L_{\text{out}}}$$  \hspace{1cm} (3.1)
This expression demonstrates that the ripple can be reduced by using a large capacitor in the final stage of the power scavenging process. This capacitor also provides an additional stability for running the sensor, besides the external batteries or supercapacitors, during sample and store. The capacitor gets charged by the DC voltage obtained during RF-to-DC rectification, described in the next section. The whole bottom tier of the 3D CMOS process has been used to design the storage capacitor. The multi-layer capacitor stackup has a very thin dielectric thickness in the Tezzaron process, which provides a capacitor with relatively higher capacitance per unit area. The multi-plate capacitors are implemented as a set of parallel capacitors in z-axis in a stackup, shown in Figure 3.8.

![Image](image_url)

*Figure 3.8—Multi-plate (multi-stack) metal-dielectric-metal capacitor*

The capacitance of a metal-dielectric-metal capacitor relates to the area of the metal plates ($W \times L$), the dielectric constant of the dielectric laminate relative to free space ($\varepsilon_\circ \varepsilon_r$) and the
thickness of the dielectric \((d)\) that fills the spacing between the plates, as shown in Equation (3.2).

\[
C = C_1 + C_2 + \cdots + C_n = n \frac{\varepsilon_0 \varepsilon_r W L}{d} \approx 9.7 \mu F
\]  

(3.2)

where

\[
\begin{align*}
\varepsilon_0 & \quad \text{is 8.85 pF/m dielectric constant of free space} \\
\varepsilon_r & \quad \text{is relative dielectric constant} \\
d & \quad \text{is the thickness of the dielectric}
\end{align*}
\]

This expression shows that a higher capacitance can be obtained from more capacitor plate area, higher dielectric constants and/or thinner laminates. The capacitance values approximated using the above equation can effectively remove the ripple, assuming a 1 kohm load resistor, 1.5 V voltage in the final stage and the UHF electromagnetic incident wave to the rectifier. A military-qualified surface mount chip capacitor with similar capacity, part \# CWR11D(5)335(1)(2)(3)(4), will add an extra 7.3 mm x 4.3 mm x 2.8 mm area if integrated off-chip. The chip capacitor also experiences as much as 2.7 \(\mu\)A leakage current at 25 degree C compared to the low leakage of FTEOS-based MIM capacitors implemented as part of the 5 mm x 2.5 mm x 2.4 mm chip in this design. The 3D simulation of the capacitor tier stackup and the approximate capacitance, which is in the microfarad range in DC, is shown in Figure 3.9.
3.3 Charge-Pump Circuit Design

This section focuses on the design of charge-pump circuits. The charge pumps—also known as rectifiers or voltage multipliers that are of interest in this section—couple incident RF signals to provide DC voltage for use with DC-powered sensors or transducers. The incoming electromagnetic field is rectified to generate supply voltage. A maximum rectifier efficiency and output DC voltage is achieved when the threshold of transistors is set to the minimum level. In legacy systems, charge pumps are implemented using Schottky diodes that demonstrate fast switching due to their low turn-on voltage and minimum substrate losses. [11, 26] However, Schottky diodes are not supported by standard complementary metal-oxide semiconductor (CMOS) processes. Charge pumps in a multi-stage CMOS process can be engineered in novel ways to lower turn-on voltages, minimize substrate losses and parasitics, maximize DC output and provide high AC-to-DC conversion efficiency. Hence, body bias-control and the use of low-threshold transistors of the CMOS process can be employed to help minimize threshold and maximize rectifier output and efficiency.
3.3.1 Background Information

Rectifiers convert a weak incident RF signal to DC power. Many approaches exist for rectifying AC signals. The traditional two-stage Dickson charge pump is shown in Figure 3.10. During the positive phase of RF input, considering the first stage in Figure 3.10, the second diode (D2) is forward-biased and, hence, the shunt (or coupling) capacitor is charged; whereas during negative RF input, the series (or multiplying) capacitor is charged, since the second diode is reverse-biased. These voltages are summed for $N$-number of charge pumping stages, hence the name-charge multiplier.

![Figure 3.10—Two-stage Dickson charge pump [6]](image)

CMOS rectifiers work like Schottky diodes. Low-threshold voltage, $N$-stage CMOS peak-to-peak detector diodes are connected in series, as shown in Figure 3.11. The charge transfer transistors M1 to M4 push charge in one direction to pump the high output voltage and generate appropriate output DC voltage. However, the threshold voltage of CMOS diodes is generally very high; hence, they have low power conversion efficiency. An implementation of a two-stage Dickson multiplier circuit with a CMOS used as a diode is shown in Figure 3.11.
This example uses low-series resistance MOS capacitors. The coupling capacitors \( C_c \) transfer electric charges to the next stage by coupling the input voltage \( V_{RF} \) with the voltage of the pumping stage (e.g. \( V_{DSM1} \) for the first stage). The multiplying capacitors \( C_m \) are output capacitors, which store energy derived from the pumping stage and are usually larger. The DC output voltage from \( N \)-stage voltage double-circuit for a given RF (AC) input voltage to the rectifier \( V'_r(t) = V_{RF} \cos(2\pi f_0 t) \) is described in **Equation (3.3)**:

\[
V_{DC} = 2N(V_{RF} - V_{ON})
\]  

(3.3)

where

- \( N \) is the number of stages
- \( V_{RF} \) is the amplitude of the incident RF signal at the rectifier
- \( V_{ON} \) is the turn-on voltage of the CMOS diode

The amount of current flow across transistors depends on the terminal voltage. The IV characteristic of CMOS transistors is shown in **Figure 3.12**. In saturation, the source to drain current flow across the CMOS diode can be expressed as follows in **Equation (3.4)**:

\[
I_{DS} = \frac{\mu_0 C_{ox} W}{2L} (V_{gs} - V_{th})^2
\]

(3.4)
The gate-to-source voltage is the amount of voltage that passes the threshold barrier and turns on the diode. The input across all the diodes in the charge coupling stage is the RF voltage. In CMOS diodes, the gate and the drain terminals are connected directly. Therefore, the output DC voltage is a function of the input voltage, the terminal voltages required to turn on the transistors, the threshold voltage, and the number of stages as given in Equation (3.5):

\[
V_{DC} = 2N \left( V_{th} - \frac{2I_{th}}{\mu_C W} - V_{th} \right) \tag{3.5}
\]

The threshold voltage is the initial voltage required to bridge the carrier depletion between the source and the drain terminals of the transistor. The required initial threshold voltage can be modified by engineering the bulk terminal of the transistors. The body bias control of connecting the bulk to the source is related by the square root of the bias voltage. The threshold voltage \(V_{th}\) of the diode is shown in Equation (3.6):

\[
V_{th} = V_{th0} + \gamma (\sqrt{2\Phi_f + V_{th0}} - \sqrt{2\Phi_f}) \tag{3.6}
\]
where

\[ V_{th} \]

is the threshold voltage when the source and the substrate are at the same voltage level

\[ V_{BS} \]

is the source-bulk voltage

The Fermi potential \( (\Phi_F) \) and the body-effect coefficient parameter \( (\gamma, \text{ which is dependent on the CMOS process technology}) \), respectively, are expressed in Equation (3.7) and Equation (3.8) as:

\[
\phi_F = \frac{kT}{q} \ln \left( \frac{N_d}{n_i} \right) \tag{3.7}
\]

and

\[
\gamma = \frac{\sqrt{2qN\varepsilon\varepsilon_0}}{C_{ox}} \tag{3.8}
\]

The capacitance is dependent on the oxide thickness \( (T_{ox}) \) and the dielectric of the oxide material in the CMOS process (e.g. FTEOS) relative to air \( (\varepsilon_r\varepsilon_0) \), and is used as follows in Equation (3.9):

\[
C_{ox} = \varepsilon_{ox} \frac{T_{ox}}{T_{ox}} = \varepsilon_r\varepsilon_0 \frac{3.7(8.85\times10^{-14})}{T_{ox}} \approx \frac{3.27\times10^{-13}}{T_{ox}} \frac{F}{cm^2} \tag{3.9}
\]

### 3.3.2 Optimization of Charge Pumps

There are many parameters that can be optimized in CMOS charge pumps. The aspect ratios of the transistors determine the amount of current passing through the diodes. An increase in aspect ratio increases the amount of current flowing through the transistors. But at the same time, higher aspect ratio increases the size of the active region that contributes to more leakage current flow. Therefore, higher DC output voltage is achieved when a lower \( V_{th} \) CMOS that requires a small turn-on current, larger MOSFET aspect ratio, increased charge pumping stages and higher incident RF power is used. Figure 3.13 shows the effect of the input power on the output voltage at different bias points of the transistor.
The analysis of the MOSFET charge pump will not be complete without a large signal analysis to account for all parasitics associated between the gate (G), drain (D), source (S) and bulk (B) of the diodes. Figure 3.14 shows the large signal representation of a single stage charge pump. The sum of parasitics capacitors at node X and the node voltage are given respectively as Equations (3.10) and (3.11):

\[
C_{S(X)} = C_{BS(M1)} + C_{BD(M2)} + C_{GB(M2)}
\]

(3.10)

\[
V_{S(X)} = \frac{C_C}{C_C + C_{S(X)}} V_{RF}
\]

(3.11)

Therefore, the output voltage for N-stages is Equation (3.12):

\[
V_{out} = 2N \left( \frac{C_C}{C_C + C_{S(X)}} V_{RF} - V_{DN} \right)
\]

(3.12)

Equation (3.12) shows that an increase in parasitics lowers the output voltage. The parasitics capacitance is dependent on the area of the diode, the oxide thickness (T_{OX}) and the dielectric of the oxide material in the CMOS process. The higher aspect ratio MOS increases the size of the active region that contributes to more leakage current flow. An increase in the output
current due to the higher number of charge pumping stages and larger aspect ratio transistors are traded-off with the efficiency of the rectification due to an increase in parasitics in the design.

Figure 3.14—N-Stage Charge Pump and Large signal model representation of the MOSFET charge pump

An increase in the number of stages and larger aspect ratio transistors, as described above, are traded off with efficiency of the rectification due to an increase in parasitics in the design. Also, incident RF power is limited by FCC radiation regulations. As described in chapter 2, the received power is determined by the transmitted power from the RFID reader, the gain on the reader antenna, the gain provided by the sensor’s coil, the transmission wavelength and range of the sensor. [9, 27] The main factor impacting the power at the sensor’s antenna coil is impedance mismatch. RLC filters, similar to the one in Figure 2.8, are used to match the 50-ohm (or 75-ohm) impedance of the external antenna (or internal coil) to the higher impedance looking into the voltage multiplier that could be as high as in kOhm range. The
incident power expressed as the magnitude of the voltage wave can be written in **Equation (3.13)** as:

\[
P_{\text{RX}} = \left| \frac{V_{\text{RF}}^2}{Z} \right|
\]  

(3.13)

where

\[ Z \] is the impedance and it is 377 Ohm for a plane wave in free space.

The power received by the sensor, as described in the literature review section and **Equation (2.18)**, is a function of the sensor’s antenna size, distance to the base station, the antenna size of the base station, and its magnetic field strength. The input voltage magnitude to the charge pump obtained from the received power, therefore, is **Equation (3.14)**:

\[
V_{\text{RF}} = \sqrt{2}|Z| \left| \frac{P_{\text{RX}}}{R_c} \right| = \sqrt{2} |Z| \sqrt{\frac{G_{\text{RX}} P_{\text{TX}} G_{\text{RX}}}{R_c} \left( \frac{\lambda}{4\pi R} \right)}
\]  

(3.14)

where

\[ R_c \] is the load impedance.

Every MOSFET diodes in the charge pumping stage are in parallel and can be modeled approximately as a channel resistance \((R_d)\) in parallel with capacitance \((C_d)\). [6] The MOS power leakage is represented by substrate resistance \((R_s)\) and a parallel capacitance \((C_s)\). [6] The charge pumping MOSFET is recharged in positive half-period and discharged in negative half-period. In DC, the multiplying and coupling capacitors appear open. The multiplying and coupling capacitors can be approximated to be large enough to appear short at higher frequencies (in RF band).
Therefore, the overall input impedance and capacitance looking into the charge pump can be approximated in Equation (3.15) and Equation (3.16) as:

\[
R = \frac{1}{2N} \cdot \frac{R_d \cdot R_s}{R_d + R_s} \\
\text{(3.15)}
\]

and

\[
C = 2N \cdot (C_d + C_s) \\
\text{(3.16)}
\]

where

- \( R_d \) is the resistance of MOS diode
- \( R_s \) is the substrate resistance
- \( C_d \) is the capacitance of the MOS diode mainly due to gate-to-source (\( C_{gs} \)) and drain-to-source (\( C_{ds} \)) capacitances

The higher number of charge pump stages decreases impedance, since the MOS multiplying stages are in parallel. When an external antenna is in use, the capacitive contribution from the pad and ESD components dominate the matching value of \( C \) in the RLC filter.

The power delivered at sensor’s antenna or coil is limited and for this reason the efficiency of the charge pump is a very critical parameter. High conversion efficiency at the given operating power translates into smaller power dissipation across the diodes and a higher output voltage. It has been noted that the charging efficiency in MOS diodes is generally poor. The reason for the poor efficiency is that the RF input has to bias the CMOS diode by

\[
\text{Figure 3.15—Model of a one-stage charge pump}
\]
overcoming the threshold voltage of the MOS; which could be as high as 0.6 V. The charge pump conversion efficiency is given by Equation (3.17):

\[
\eta = \frac{P_{dc}}{P_{rf}} = 1 - \frac{P_{loss}}{P_{rf}}
\]

(3.17)

where

- \( P_{rf} \) is the input power
- \( P_{dc} \) is the output power
- \( P_{loss} \) is the circuit power loss

The output power \( (P_{DC} = I_{DC} * V_{DC}) \) is the power delivered at the output of the rectifier from the input power after the power loss during the conversion process.

The input power to the rectifier system from the root mean square input RF voltage is Equation (3.18):

\[
P_{rf} = \left( \frac{V_{rf}}{\sqrt{2}} \right)^2 = \frac{V_{rf}^2}{2R}
\]

(3.18)

Hence, the efficiency in Equation 3.17 can be expressed in Equation (3.19) as:

\[
\eta = \frac{P_{dc}}{P_{rf}} = V_{dc} * I_{dc} * \frac{2R}{V_{RF}^2}
\]

(3.19)

The output DC current is the mean current of the coupled input sinusoidal current in the conduction angle in the range of \(-\theta/2\) to \(+\theta/2\), as described in Equation (3.20): [6]

\[
I_{DC} = \frac{1}{2\pi} \int_{-\theta/2}^{\theta/2} I_{dc(\theta)} d\theta
\]

(3.20)

This expression shows that an improvement in conduction angle range \(\theta = -\frac{\theta}{2} \text{ to } +\frac{\theta}{2}\) can improve efficiency significantly. The power loss for a single diode consists of power loss during both charging and discharging written in Equation (3.21): [6]

\[
P_{loss} = \frac{1}{T} \int_{0}^{T/2} I_{dc(t \text{ diode})} V_{dc} \ dt = I_{ch}^2 R + I_{dis}^2 ch R = \left( \frac{V_{rf}/\sqrt{2}}{R} \right)^2 R + \left( \frac{V_{rf}/\sqrt{2}}{|Z|} \right)^2 R = \frac{1}{2} V_{rf}^2 \left( \frac{1}{R} - R \omega^2 C_d \right)
\]

(3.21)
where

\[ Z \text{ is the impedance that can be expressed as } \frac{1}{j \omega C_d} \]

From the above equations, it can easily be deduced that power loss (\( P_{\text{loss}} \)) is minimum and efficiency is maximum when the MOS channel resistance is in perfect match with the impedance as specified in Equation (3.22):

\[ R = \frac{1}{\omega C_d} \quad (3.22) \]

The transconductance of the diode is the levels of carrier mobility in the channel or gain across the MOSFET and is a function of the output current.

The transconductance in saturation region can be expressed in Equation (3.23) as:

\[
g_m = \frac{dI_{ds}}{dV_{gs}} = \frac{d}{dV_{gs}} \left( \frac{\mu_n C_{ox} W}{2 L} (V_{gs} - V_{th})^2 \right) = \frac{\mu_n C_{ox} W}{L} (V_{gs} - V_{th}) = \frac{2I_{ds}}{V_{gs} - V_{th}} \quad (3.23) \]

The maximum charge pump operation occurs when output impedance is high. This is achieved in the saturation region, where the output current varies slightly with the drain to source input. Hence, the resistance derived from the transconductance in the saturation region is expressed in Equation (3.24):

\[
R_c = \frac{1}{g_m} = \frac{V_{gs} - V_{th}}{2I_{ds}} \quad (3.24) \]

The maximum rectifier efficiency is achieved when \( V_{th} \) is as small as possible, output current across the MOS is increased and input voltage is not too high to avoid substrate loss by large devices. The higher number of stages and aspect ratio increases the current across the diodes but large devices increase substrate loss (leakage). Therefore, a higher number of charge pumping stages decreases efficiency of the charge pump but enough number of rectification stages are required to get sufficient output DC voltage. The output DC current in each stage is mainly limited by the RF signal providing a small conduction angle.
3.3.3 Previous Works

The goal of the design improvements in the charge pump is to multiply the extremely low DC voltage from an incident RF more efficiently and provide a practical voltage for charging a supercapacitor or battery and operating the rest of the circuits. As described in the previous sections, the conventional rectifier circuits show poor voltage output and power conversion efficiency due to the high threshold of the diodes in a standard CMOS process, which is equal to or above 0.3 V in Tezzaron 0.13 μm 3D CMOS. Many of the literatures are focused on improving power conversion efficiency centers around the cancellation of this threshold voltage. The architectures reported in [4] and [6] provide improvements in CMOS threshold reduction and an increase in the conduction angles. A DC-to-DC rectification design in [12] also demonstrates the means to manage the conduction angle using clock-offset to maximize the rectification efficiency. Much of the previous research in this area proposes designs [4, 6] which increase transistor count, parasitics and/or design complexity for not-so-high power conversion efficiency. These designs use PMOS and NMOS diodes, and variation between PMOS and NMOS in some processes can cause a significant input voltage offset and thereby reduce efficiency. Other implementations also use an external threshold (vth) cancelation scheme to overcome the overall threshold [44], as shown in Figure 16. An external biasing voltage is provided to compensate for threshold voltage drop. The biasing voltage supplied from an external source will require additional power generation budget and defeats the purpose of output DC voltage and power efficiency improvements.
3.3.4 Improved Charge Pump

The design proposed in this thesis implements CMOS diode threshold compensation using static biasing of the gate. The gate of the diode in the charge pump is isolated with a capacitor to store static charge from a leakage current and provide a compensation voltage, \( \Delta V_{gs} \), as shown in Figure 17.
The delta voltage required to compensate for threshold can be characterized from Equation (3.4). The currents in both diodes in saturation can be expressed as in Equations (3.25) and (3.26):

\[ I_{D,M2} = \frac{\mu_0 C_{ox} W}{2} \left( V_{gs} - V_{th} \right)^2 \]  
\[ I_{D,M1} = \frac{\mu_0 C_{ox} W}{2} \left( V_{gs} + V_{gs}' - V_{th} \right)^2 \]

Based on the voltage-current equation for charge pumping transistors in saturation region, a fully zero threshold implementation could be achieved by adding a static gate biasing of the rectifying transistor and creating a voltage offset. The MOS-based capacitors are charged to increase the gate-to-source voltage of the charge pumping transistor by the threshold voltage (i.e., \( V_{gs}' = V_{gs} + V_{th} \)), cancelling out the bulk effect completely. The improved architecture, in Fig. 10, uses diode-connected minimum length NMOS-based transistors with the bulk connected to the source to eliminate bulk effect and hence reduce the effective threshold voltage.

The charge pump, in Figure 3.18, has been implemented in the 0.13\( \mu \)m 3D Tezzaron low-threshold CMOS process to further minimize threshold and maximize the rectifier performance.
The charge pumps in the first two stages provide enough voltage to power a ring oscillator that drives the charge pumps in the following stages. The ring oscillator provides non-overlapping and lower frequency clock inputs to the next stages to increase the conduction phase and minimize power consumption. The low frequency and the 180-degree phase offset help to turn off rectification stages, completely preventing the reverse charge flow, and turn on during the conduction cycle more effectively by the higher voltage generated. This comes at the expense of some increased parasitics capacitance at pumping nodes. This design helps to cancel out threshold effect, reduce reverse current flow and maximize the conduction angle, which increases DC current output and maximum power conversion efficiency.

As described in the earlier section, the sizing of the transistors in the charge pump involves making a trade-off between increasing the output voltage versus the risk of a decrease in power conversion efficiency due to an increase in leakage current. The high aspect ratio (W/L) transistors increase the output DC current but the leakage current increases as well, which makes the power efficiency suffer. An increase in the number of charge pumping
stages also involves making a trade-off between increases in an output DC voltage versus a decrease in the power efficiency as a result of an increase in parasitics. The schematic level Spectre simulation confirms that the output voltage increases with an increase in the number of stages, as shown in Figure 3.19, but cascading a higher number of charge pumping stages decreases the power delivery efficiency. The presence of too many stages increases the parasitics capacitance of the diodes, which also appear in parallel to the antenna. A trade-off has been made between the increase in output DC voltage and the parasitics of the system as a result of multiple charge pump stages. The input RF voltage is multiplied to a higher value by a number of stages as shown in the time-dependent simulation. The resulting signal is then rectified by the series diodes. Sufficiently high DC supply voltage is generated from a weak RF signal from EIRP of approximately 1.62 w (based on RF range calculations).

Figure 3.19—Spectre transient output from the improved multi-stage rectifier
The coupling MOS capacitors are sized so that the time constant of the capacitors is larger than the period of the input AC signal to minimize ripple in the output DC voltage, as expressed in **Equation (3.27)**.

\[
\tau = R C_c = \frac{V_{dc}}{I_{out}} C_c \gg T = \frac{1}{f_{RF}} \quad (3.27)
\]

A larger range of coupling capacitor is acceptable to ensure the time constant exceeds 1nS period of the input signal for the first two stages. However, sizing the coupling capacitor too high delays the transient response of the output DC voltage (and the startup time of the charge pump circuit). High voltage ripple due to the low frequency is compensated by using a higher value capacitor for the last four stages.

### 3.4 Limiter and Regulator Circuit Design

The limiter circuit ensures the input voltage level to the voltage regulator is below the transistor breakdown voltage [2, 4,5]. As it is apparent from the voltage multiplier design section, the level of the output DC voltage (and current) is dependent on the input AC voltage. The rectifier input AC voltage is a function of the incident RF signal. When the sensor is very close to the reader, the output DC voltage could spike and provide a voltage that can exceed the transistor breakdown voltage and damage the sensor chip. The limiter is comprised of a voltage dividing circuit that provides the optimum output voltage (or a limited power amplitude) and a current leak off when the voltage exceeds the intended output voltage in near field.

A low-power linear voltage regulator provides further supply voltage stabilization by locking the output DC voltage to a stable voltage supply. Probably one of the most important parts of the fully differential opamp design is the current mirror and the bias circuits. The aspect ratios ($W/L$) of the NMOS and PMOS transistors in the bias circuit were set to keep all the transistors in saturation sourcing or sinking a fixed current to generate the required bias voltages for all parts of the design. The gate-to-source voltage for saturation drain current $I_1$
of an NMOS transistor M14 of the supply independent biasing circuit shown in Figure 3.20 is Equation (3.28):

\[ V_{GS,M14} = V_{T,M14} + \sqrt{\frac{2I_1}{\mu_n C_{ox} W_{M14}}} \]  

Equation (3.28)

Figure 3.20—Start-up and biasing circuit

The cascode configuration of the current mirror improves the input common mode range and power supply rejection ratio. The differential cascode transconductance stages allow for a high \( g_m \) (and low drain current), as the current flows down through a series of connected NMOS and PMOS transistors with the current splitting evenly in the differential pair. And the gate-to-source voltage with a saturation drain current \( I_2 \) of an NMOS transistor M18 is in Equation (3.29) as:

\[ V_{GS,M18} = V_{T,M18} + \sqrt{\frac{2I_2}{\mu_n C_{ox} W_{M18}}} \]  

Equation (3.29)
The saturation drain current is approximated based on the aspect ratio the transistor needs to maintain to stay in saturation, and, finally, the given Vgs is calculated. The current is defined independent of supply. The effect of channel-length modulation can be ignored. The KVL in the M14 through M18 loop is in Equation (3.30) is:

\[ V_{GS,M14} = V_{GS,M18} + R_2 I_2 \]  

(3.30)

The PMOS mirrors force the two currents (I_1 and I_2) across M14 and M18 to be equal, and therefore Equation (3.25) can be expressed as Equation (3.31):

\[ V_{L,M14} + \frac{2I_2}{\mu_n C_{ox} W_{M14}} = V_{L,M18} + \frac{2I_2}{\mu_n C_{ox} nW_{M14}} + R_2 I_2 \]  

(3.31)

The body effect differences between M14 and M18 can be neglected to simplify Equation (3.31) as Equation (3.32):

\[ I_2 = \frac{1}{R_2^2} \frac{2}{\mu_n C_{ox} W_{M14}} \left(1 - \frac{1}{\sqrt{n}}\right)^2 \]  

(3.32)

Based on Equation (3.27), the biasing current can have more than one operating point. Hence the startup circuit guarantees that the biasing circuit will have a unique stable output current when the power is on and turn transistors off when there is no input power. [28] The KVL in the M13 through M17 outer loop of the current mirror is expressed in Equation (3.33):

\[ V_{DS,M14} + V_{GS,M13} = V_{GS,M17} + V_{DS,M18} + R_2 I_1 \]  

(3.33)

If the current through the bias MOS with an aspect ratio of W/L is I_1 and if we want to sink or source 10*I_1 current across a specific node of the MOS in any part of the design, we can use the same W/L aspect ratio as the bias circuit and provide a multiplier of 10 for the transistor of interest to fully mirror and track the bias circuit and stay in saturation. Therefore, the common gate, common source or common drain transistors in the design follow a proportional sizing ratio to that of the bias circuit.

The voltage regulator with limiter, in Figure 3.21, also includes a startup and self-biased circuit and bandgap reference circuit. The voltage is regulated by taking the feedback signal to compare with a bandgap reference voltage in an error amplifier, and then the output of the
amplifier can be used as a controlled signal to change the resistance of the pass transistor. [3]

![Figure 3.21—Limiter and regulator](image)

The derivation equations for reference voltage biasing are discussed in chapter 4. The output from the power regulator also provides a power on reset (POR) signal. When the generated supply voltage from the charge pump circuit is high enough, the reset signal goes to a “low” state to initiate a new state in the digital state machine circuitry indicating that the rectified voltage has reached a reliable, regulated level. [4] The power amplifier provides characteristic hysteresis output to avoid false triggering.

### 3.5 Battery Charger and DC-to-DC Converter

The two batteries / supercapacitors are used: one to power the core circuits of the sensor that samples temperature data and another to power the data storage memory (SRAM). These batteries get charged using an on-chip charging circuit. When an external RF carrier wave (CW) is available and rectified and regulated, the charger circuit power up and starts charging the batteries. A rectified, limited and regulated DC is used to provide an overcharge and discharge protection. **Figure 3.22** shows the complete charging circuit. Battery is first
charged at a constant current (CC) rate to its upper threshold \( (V_{ref}) \) of 2.5 V, followed by a constant voltage (CV), until the charging current drops to about five percent of the initial applied CC rate. [25] The biasing by the current mirror works as described in the regulator section. The current mirror generates a reference current for the tail \( I_x \) (n1 \( I_{bias} \)) and \( I_y \) (n2 \( I_{bias} \)). When the battery cell is fully discharged, the regulator (or amplifier) output is driven high and the voltage sense amplifier drives the PMOS into cutoff. [25, 29] The full current difference \( I_x - I_y \) is reflected via the current-mirror to provide the battery cell with a constant current of \((n1-n2)I_{bias}\). Simultaneous constant-current and constant-voltage charging loops provide the charge process without disruption. [25]

**Figure 3.22—Charging system**

The nominal supply voltage for the 130 nm technology CMOS process is 1.5 V but the charger can charge the supercapacitor up to 2.5 V. The charging and discharging on the batteries has been modeled using gain-controlled current source, as shown in Figure 3.23. The maximum charge and discharge current is 500 \( \mu \text{A} \). The time required to charge the batteries in use with this design with a nominal voltage of 2.5 V, 0.3 mAh capacity and
optimum charge and discharge current of 25 μA has been calculated to be about 12 hours using Equation (3.34):

\[ i(t) = C \frac{dv(t)}{dt} \implies t = C \int \frac{dv(t)}{i(t)} \]  

(3.34)

![Figure 3.23—Rechargeable battery/supercapacitor model](image)

The power is consumed from an energy source, such as a battery, through the supply voltage and current. The impact of supply voltage, especially on dynamic power consumption, is very dominant, as described in chapter 2, as dynamic power is proportional to the square of the supply voltage. Hence, the stringent power requirement in the sample and store part of the sensor system requires the higher supply voltage from the battery be reduced to a low supply voltage of 0.9 V to easily design the circuits in the low-power and sub-threshold operations as desired. The DC-to-DC converter has been designed to calibrate the supply voltage to the required voltage level of 0.9 V for use with the low-voltage, low-power part of sample and store circuits. The sample and store operations are running at low frequencies and hence the reduced supply voltage will not have any performance impacts on them. [24, 29] The DC-to-DC converter, shown in a block diagram in Figure 3.24, employs an error amplifier, a reference voltage generator from the input voltage, and a voltage divider.
The voltage divider provides the required output voltage of 0.9 V from the reference voltage. The output voltage is given by \textbf{Equation (3.35)}:

\[
V_{\text{out}} = V_{\text{ref}} \left(1 + \frac{R_1}{R_2}\right)
\] (3.35)

The amplifier in the DC-to-DC converter is a comparator circuit that compares the reference voltage with the output voltage and calibrates the output current. [25] The capacitor provides the additional stabilization so changes to the output voltages are slow enough for the comparator to calibrate back to the desired voltage. \textbf{Figure 3.25} shows the temperature and process-independent 0.9 V output supply voltage from the DC-to-DC converter. The derivations for temperature-independent bandgap biasing are covered in chapter 4.
3.6 Demodulator and Backscatter Design

As described in chapter 2, the equivalent inductance and capacitance of the sensor’s antenna coil resonates at the frequency of the reader in the range. The signal from the reader has power and data. The sensor listens to the reader for commands and responds back to the reader with acknowledgement commands or data. The reader transmits a CW to the sensor by modulating the RF signals. The sensor listens to what the reader wants it to do and complies with the commands. It backscatters data by changing the load connected to the sensor’s coil antenna, based on the transmit bit stream. A bias control in conjunction with a ring oscillator provides the clock and digital data embedded in the CW, using double-sideband amplitude shift keying (DSB-ASK), single-sideband amplitude shift keying (SSB-ASK), or phase-reversal amplitude shift keying (PR-ASK). [4, 5]

The modulation of data is achieved using a pulse-interval encoding (PIE) format wherein data is passed to the sensor by pulsing the CW at differing time intervals to indicate a 0 or 1 bit.

The demodulator and backscatter, in Figure 3.26, include interfaces for receiving commands from the reader, interpreting them, and uploading the sensor’s data and sending
acknowledgment commands back to the reader. The decoder and the serializer are part of the digital design section in chapter 5.

The demodulated data and clock are in use in the digital control for decoding commands from the RFID reader and clocking out the backscatter data from memory at a bit rate ranging between 40 to 640 Kbps. [18] The signal is demodulated and the information in the signal is decoded to perform logic functions required by the RFID protocol.

In the demodulator design, the envelope signal and its slowing moving part are compared by the discriminator to produce the demodulated signal in digital format. A fast-charge pump or envelope detector, a peak detector, and a comparator are the main parts of the demodulator system that works as a data slicer, shown in Figure 3.27.
The envelope detector uses a charge pump or rectifier circuit. The envelope from the reader is detected using a similar type of charge pump circuits, described in the rectifier section. The capacitors are sized carefully to couple the reader signal power. Like in the rectification case, the coupling capacitors of the envelope detector are sized such that the pulse interval of the pulse-width-modulated (PWM) signal is smaller than that of the time constant of the capacitors. The correct sizing of the coupling capacitors helps reduce the signal ripple from the RFID reader to the sensor.

The envelope detector is followed by a low pass filter formed with the variable drain-source resistance of an NMOS and a capacitor. The integrator that generates the ramp voltage for the discriminator uses an RC filter. The envelope detected signal has been connected to an MOS resistor and integrated across an MOS capacitor to provide the output ramp voltage, as in **Equation (3.36)**, before the next pulse edge. [10]

\[
V_0 = -\frac{1}{C_M} \int_0^T V_{\text{env}} \, dt = -\frac{1}{C_M} \frac{V_{\text{env}} T}{R_M}
\]  

The discriminator handles clock and data recovery (CDR) of the PWM signal. The CMOS discriminator has hysteresis characteristics for error-free hit detection. The output is
compared to the discriminator threshold to detect a digital “0” and “1.” [7] Figure 3.28 shows an ASK demodulator.

![Figure 3.28—Example simulation of the ASK demodulator](image)

The downlink backscattering communication to the RFID reader by the sensor depends on the impedance variations or impedance modulation by modifying the capacitance of a varactor connected to the antenna (or coil), depending on a switch transistor driven by a logic low and high form of data using ASK, as shown in Figure 3.29. The varactor is connected to the coil terminals through a blocking capacitor. The voltage across the varactor is controlled by a current-biased inverter. [5] The varactor, connected between two capacitors, is driven by inverters into positive and negative voltage references. The input is connected to switching on-or-off NMOS devices.
When the modulated signal from a serializer launches into the backscatter, the inverter turns on and then turns on the switch connected to the varactor diode. The inverter is sized to avoid modifying the pulse width of the modulated signal. The switch is sized at a minimum dimension to set low-output resistance so the impedance seen from the matching network is negligible compared to the antenna resistance. The RFIC protocols described in chapter 5 ensure the correct polarity and the ability to discriminate the reflection from the sensor to the other reflection sources, including environmental obstacles and antennas.
Chapter 4     Low-Power Sensor Data Logger

4.1 Introduction
The sensor’s data logger samples and stores the brief time-temperature aseptic processing history of the food particulates that can be reviewed when needed. One of the biggest challenges in miniaturizing battery-assisted sensors is the fact that the size of the batteries and supercapacitors they use is directly proportional to their lifetime. The data sampling and collection circuits need to be designed for ultralow power operations and as low sampling frequency as possible to increase operational life expectancy of the sensor, while employing a supercapacitor that is as small as possible, which is the biggest contributor to the overall sensor volume and cost. The low-power data-logging block includes the temperature sensor, ADC, clock generator and memory. The data logger also has important interfaces that provide a stable voltage reference to ensure normal operation of the sensor in extreme temperatures.

This section describes the designs of the current mirror, temperature sensor, clock generator and ADC circuits, shown in Figure 4.1. The temperature sensor has a voltage output (in mV) that corresponds to the temperature reading (in degree C). It shows a linear change in voltage output as a function of a change in temperature in the range of 27-140 degree C. The clock generator uses an external 32 KHz quartz crystal resonator as a stable frequency reference, an on-chip voltage-controlled oscillator to drive the reference frequency and a frequency divider to get the desired sampling frequency from the 32 KHz crystal resonator for sampling sensory data. The ADC samples the real-time voltage data representative of the sensor’s temperature in volts to provide a digital readout from the on-chip memory. The sensor can wirelessly retrieve digital modulated data preloaded on the on-chip memory. When sampling data, the ADC uses stable reference voltage that shows no variation with temperature and a sensory voltage that varies with temperature to continuously monitor the changes in temperature.
4.2 Low-Power Current Mirror Design

In chapter 3, we discussed one of the most critical aspects of an ultralow power sensor design. The goal of achieving ultralow power sensor design starts with optimizing the output DC current and power conversion efficiency of the charge pump. Chapter 3 also briefly covered DC-to-DC converters for lowering the global supply voltage to a supply voltage that can still provide acceptable signal-to-noise ratio supply voltage, which is another important aspect of ultralow power design. The optimization of a digital state machine for optimized and power-aware communication between a sensor and RFID reader is covered in chapter 5. This section discusses the other major task in achieving an ultralow power and temperature compensated sensor design by decreasing the power consumption of the sensor’s individual circuit blocks. Current mirrors provide reliable supply voltage, temperature, and process-independent biasing. Lowering the global supply power is the quickest way of reducing dynamic power in design blocks, but current mirrors can also be used to minimize power and operate the sub-circuits in ultralow power when the available supply voltage is above the threshold voltage of the transistor technology. The lengths of the transistors in the current mirror are generally chosen at a size that is longer than the minimum, to limit the effect of
channel-length modulation. The current mirror operates in sub-threshold because of cascode transistors. The sub-threshold implementation helps to keep the length of current mirror transistors smaller at such low currents, and lower supply voltage (VDD) is achieved. The cascode transistors still need to be large enough to saturate the drain currents in order to get a current necessary to meet the minimum requirement. Without the cascode, the current directly depends on the supply voltage. The gate resistance is reduced by using a multi-finger gate structure.

The CMOS sub-threshold low voltage and supply independent biasing circuit has been used in many parts of the low-power CMOS sensor applications. The biasing circuits complementary to absolute temperature (CTAT) and proportional to absolute temperature (PTAT) for positive and negative temperature slopes, respectively, are implemented. [2] The process and temperature coefficient variations affect magnitude of both the positive and negative slope currents. A temperature independent reference (bandgap) is generated by summing CTAT and PTAT, as shown in Figure 4.2. [2]

![Figure 4.2—The bandgap reference](image)
A positive temperature coefficient current can be balanced with a negative coefficient current by carefully sizing the two current mirrors to provide temperature independent biasing. The pure MOSFET current reference circuit core is shown in Figure 4.3, with the diodes operating in sub-threshold region.

![Figure 4.3—All MOS PTAT and CTAT](image)

For CTAT biasing in M1, M2, M3 and \( R_1 \) loop, in Figure 4.3, the voltage across \( R_1 \) is equal to the voltage across M1, since drain source voltage across M2 is the same as M3, as written in Equation (4.1).

\[
I_{CTAT}(T) = V_{GS1} \implies I_{CTAT} = \frac{V_{GS1}}{R_1(T)} \quad (4.1)
\]

where

\( R_1(T) \) is the temperature dependence of the resistor, \( R_1(T) = R_{ref}\{1 + \alpha[T - T_{ref}]\} \), with \( R_{ref} \) as the conductor resistance at the reference temperature \( T_{ref} \), and \( \alpha \) is the temperature coefficient of resistance for the conductor material.
The temperature dependence of the conductor material dominates that of the diode, as shown in Figure 4.4.

![Figure 4.4—CTAT response from Spectre](image)

The KVL in the M10, M11, and $R_2$ loop for the PTAT bias generator can be written as in Equation (4.2):

$$V_{GS10} = V_{GS11} + I_{PTAT}R_2(T) \Rightarrow I_{PTAT} = \frac{V_{GS10} - V_{GS11}}{R_2(T)}$$  \hspace{1cm} (4.2)

The substitution from Equation (2.25), if channel length modulation effects are ignored since M10 and M11 are big channel length transistors, yields the PTAT current approximating equation. The resulting equation makes the current directly proportional to absolute temperature and is more dominate over the resistor’s temperature dependence. The scaled PTAT and CTAT can be added, as shown in Figure 4.2, to generate a bandgap response. The CTAT and PTAT currents need to have similar slopes for the temperature
variation to cancel each other out and give a current that is independent of temperature. The bandgap reference similarly gives supply-independent biasing. The KVL across the cascode current mirrors for both the CTAT in Equation (4.1) and the PTAT in Equation (4.2) give a current that is independent of supply voltage. Figure 4.5 shows an ideal equal magnitude negative slope (CTAT) and the positive slope (PTAT) sum to provide a temperature-compensated bandgap, provided in Equation (4.3).

\[
\frac{\partial I_{bg}}{\partial T} = \frac{\partial (I_{CTAT} + I_{PTAT})}{\partial T} = \frac{\partial \left\{ \frac{(W/L)_{CTAT}}{24} + I_{PTAT} \right\}}{\partial T} = \frac{(W/L)_{CTAT}}{(W/L)_{PTAT}} I_{PTAT} \approx 0
\]  

(4.3)

Figure 4.5—Ideal representation of temperature-compensated biasing

The resistors and transistors for the PTAT and CTAT mirrors used in this design have been carefully sized to obtain the desired current in nA range on each branch. Similar types of current mirrors that provide supply- and process-independent biasing are used in many of the circuits in the sensor design. As discussed in the previous section, current mirrors need a startup circuit to start biasing the circuits in a normal operating point for proper functionality.
4.2.1 Temperature Sensor

A low-power, low-voltage temperature sensor is implemented using a bipolar PNP junction transistor as a linear temperature-dependent source, as shown in Figure 4.6. The sensor is a variation of the sensor reported in [2] and operates at 0.9 V in the 27-140 degree C temperature range.

![Temperature sensor diagram](image)

Figure 4.6—Temperature sensor

The output current (collector current) of a bipolar transistor depends on a constant source current. The source current is dependent on area and temperature. The $pn$ junction diode equation for a collector current is expressed in Equation (4.4):

$$I_c = I_s \exp \left( \frac{V_{BE}}{V_T} \right)$$  \hspace{1cm} (4.4)

The resulting base-emitter junction voltage, $V_{BE}$, shows high temperature sensitive as follows in Equation (4.5):
The base-to-emitter voltage, $V_{BE}$, has a negative temperature slope, assuming $I_c$ is constant, as shown in Equation (4.6):

$$\frac{\partial V_{BE}}{\partial T} = \frac{\partial V_T}{\partial T} \ln \frac{I_c}{I_s} - \frac{V_T}{I_s} \frac{\partial I_s}{\partial T}$$  (4.6)

The voltage differences between two $pn$ junctions create a positive temperature slope, as shown in Equation (4.7):

$$\Delta V_{BE} = V_{BE1} - V_{BE2} = V_T \ln \left( \frac{I_c}{I_s} \right) - V_T \ln \left( \frac{I_c}{nI_s} \right) = V_T \ln(n) = I_s R_s \Rightarrow I_s = \frac{V_T \ln(n)}{R_s}$$  (4.7)

The source current ($I_s$) has a positive thermal slope (PTAT). The temperature sensor detects voltage-temperature variations and provides the analog data for sampling at low clock frequency. Its output is linearly proportional to temperature with a slope of +2.4 mV per degree C when supplied from a 0.9V power supply. This means a very high resolution ADC is required to convert the voltage representation of the temperature into a digital read out in wide temperature range. In the final design the sensor is supplied from a higher Vdd than 0.9V to trade-off power by high resolution and power hungry ADC. The temperature sensor requires calibration to a known temperature to determine the temperature offset values. A test temperature is used as the known calibration temperature for the sensor in the external RFID reader API.

### 4.3 Low-Power Clock Design

This section describes the design of a low-power, low-frequency and temperature-independent clock generation system for battery-operated sampling of the sensory data. The clock generation system uses crystal resonator as a frequency reference. The quartz crystal resonator is piezoelectric material that vibrates when an electric potential is applied to it. [1, 21] The clock generation system uses 32.768 kHz quartz resonator. The low frequency and small size of the 32.768 kHz quartz resonator made it ideal for the sensor design like in many
4.3.1 Crystal Resonator

A quartz crystal resonator, commonly used in wristwatches as a precise and stable frequency source, meets design requirements for an extremely low-power, low-supply voltage, low-frequency, low-jitter and high-temperature operation. The quartz crystal resonator implemented in a feedback oscillation system provides a stable oscillation powered with a DC supply. The high quality factor of the inductor in the quartz crystal is the main reason for the high stability. A crystal resonator can be modeled as a series RLC circuit. The LC model of the crystal, shown in the right side of Figure 4.8, provides the ideal oscillation frequency when powered by a DC. The KVL in the resonator loop can be expressed in time domain or converted to frequency domain using Laplace transform. The voltage across the inductor is expressed in Equation (4.8):

\[ V = L \frac{di}{dt} \quad \Rightarrow \quad V(s) = LsI(s) \]  

(4.8)

The current in the capacitor, which is the same in magnitude as the current across the inductor, can be defined by Equation (4.9):

\[ i_c = C \frac{dv}{dt} \quad \Rightarrow \quad I(S) = sCV(s) \]  

(4.9)

Therefore, the KVL across the resonator written in both time and frequency domain is expressed in Equation (4.10):

\[ L \frac{d^2i(t)}{dt^2} + Ri(t) + \frac{1}{C} \int_0^t i(t)dt = v(t) \Rightarrow L \frac{d^2i(t)}{dt^2} + R \frac{di(t)}{dt} + \frac{1}{C} i(t) = 0 \]  

(4.10)

This can be re-written in frequency domain, as shown in Equation (4.11):

\[ LsI(s) + RI(s) + \frac{1}{sC} I(s) = \frac{I(s)(Ls^2+Rs+s^2)}{s} = V(s) \]  

(4.11)

The terms can be rearranged to provide an expression for admittance, as shown in Equation (4.12).
\[
\frac{s}{L(s^2 + \frac{R}{L}s + \frac{1}{LC})} = \frac{s}{L(s^2 + 2\omega s + \omega^2)} = \frac{Y(s)}{V(s)} = Y(s) \quad (4.12)
\]

where
\[\omega = \frac{1}{\sqrt{LC}} \quad \text{and} \quad \varphi = \frac{R}{2L}\]

The poles, for \(Y(s) \to \infty\), are the solutions for the quadratic equation in the denominator, as shown in Equation (4.13)
\[
s = -\varphi \pm \sqrt{\varphi^2 - \omega^2} \quad (4.13)
\]

The topology of an oscillator system includes a crystal resonator, gain amplifier, and a feedback network. The whole system needs to work together to start resonance and maintain stable resonance as long as current is supplied. The complete feedback system is illustrated in Figure 4.7. The feedback system introduces an intermediate error parameter \((X)\), shown in Equation (4.14), which is the difference between the optional external input \((V_i)\) and the feedback system \((F)\). [21, 23, 35]
\[
X = V_i - FV_o \quad (4.14)
\]

The output signal, \(V_o\), is amplified by a linear amplifier with a gain, \(A\), expressed in Equation (4.15):
\[
V_o = AX \quad (4.15)
\]

Therefore, substituting for the error parameter in Equation (4.10) can be rewritten as Equation (4.16):
\[
\frac{V_o}{A} = V_i - FV_o \leftrightarrow \frac{V_o}{V_i} = \frac{A}{1 + AF} \quad (4.16)
\]

For the closed loop gain to meet the Barkhausen criteria of oscillation [23], the denominator in Equation (4.16) is zero. This means that the closed loop gain is greater than or equal to unity and the phase is 360 degrees, as can be seen in Equation (4.17) and Equation (4.18).
\[
1 + AF \geq 0 \implies |AF| \geq 1 \quad (4.17)
\]
\[
< AF = 2\pi n \quad (4.18)
\]

where
\[n \quad \text{is an integer} \ 0, 1, 2, \ldots,\]
The energy will alternate between magnetic and electric forms, shown in the right side of Figure 4.7, to provide the resonance.

![Feedback system](attachment:image.png)

**Figure 4.7—Feedback system**

The overall topology of the oscillator includes a crystal resonator, gain amplifier, feedback network, buffer and frequency divider as shown in Figure 4.8. The equivalent impedance of the resonator is the parallel combination of the shunt capacitive reactance with the series combination of the inductive and capacitive reactance’s of the motional capacitance and inductance, as calculated in Equation (4.19).

\[
Z(j\omega) = R + \left(\frac{\frac{1}{j\omega C} + j\omega L}{\frac{1}{j\omega C} + j\omega L}\right) \frac{1}{\frac{1}{j\omega C} + j\omega L} = R + \frac{1}{\omega} \left(\frac{\omega^2 LC - 1}{(C_0 + C) - (\omega^2 LCC_0)}\right) = Z_c
\]  

(4.19)

where

- \(C\) is the motional capacitance
- \(R\) is the motional resistance
- \(C_0\) is the shunt capacitance of the resonator.

The quality factor \((Q)\) of the resonator is due to its inductive or capacitive nature. The quality factor of the quartz crystal is high and therefore the series resistance in Equation (4.19) is negligible. This simplifies the equivalent impedance to Equation (4.20):
\[ Z(j\omega) = \frac{1}{\omega} \left( \frac{\omega^2 LC - 1}{(C_0 + C) - (\omega^2 LCC_0)} \right) \]  

(4.20)

The series resonance of the crystal as a result of the motional L and C is achieved when the capacitive and inductive reactance are equal in magnitude and 180 degrees out of phase, to provide the series resonance in \textbf{Equation (4.21)}.

\[ \omega_s L = \frac{1}{\omega_s C} \Rightarrow \omega_s = \frac{1}{\sqrt{LC}} \]  

(4.21)

The series resonance dominates when the shunt capacitance \((C_0)\) is much larger than \(C\) and the impedance in \textbf{Equation (4.20)} is kept minimum \((Z_c \approx 0)\). The crystals as an inductive load provide parallel resonance as a result of motion inductance \((L)\), motion capacitance \((C)\) and shunt capacitance \((C_0)\), which causes a higher load resistance. The parallel resonance occurs when the inductive reactance has the same magnitude and 180-degree phase shift to the capacitive reactance of the motion and shunt equivalent capacitances, as expressed in \textbf{Equation (4.22)}.

\[ \omega_p L = \frac{1}{\omega_p C} + \frac{1}{\omega_p C_0} = \frac{1}{\omega_p} \left( \frac{1}{C} + \frac{1}{C_0} \right) \]  

(4.22)

Therefore, \textbf{Equation (4.22)} provides the parallel resonance as indicated in \textbf{Equation (4.23)}:

\[ \omega_p = \frac{1}{\sqrt{LC}} \sqrt{1 + \frac{C}{C_0}} = \omega_s \sqrt{1 + \frac{C}{C_0}} \]  

(4.23)

The parallel resonance frequency occurs when impedance in \textbf{Equation (4.19)} is at a maximum \((Z_c \approx \infty)\). The series resonant resistance for a capacitive dominated resonance is expressed in \textbf{Equation (4.24)} as:

\[ R = \frac{1}{Q_0 C} \]  

(4.24)

The load resistance of the crystal due to the shunt capacitance can modified by the load capacitance through \textbf{Equation (4.25)}: [35]

\[ R_L = \frac{1}{\frac{1}{R\omega^2(C_0 + C_L)^2}} \]  

(4.25)

where

\[ C_L \quad \text{is } C_1 \text{ in series with } C_2 \quad \text{and provides the additional load capacitance parallel with the crystal.} \]
The parallel resonance in Equation (4.23) is modified by the load capacitance as in Equation (4.26):

\[
\omega_p = \omega_0 \sqrt{1 + \frac{C}{C_0 + C_L}}
\]  

(4.26)

The level of frequency pulling \((p)\) beyond the resonance frequency of the crystal by the load and its impact on the operating frequency is calculated as follows in Equation (4.27): [24]

\[
p = \frac{\omega_0 - \omega_p}{\omega_0}
\]  

(4.27)

The pulling expression implies that when the pulling value is very small, then the exact operating frequency is as close to the resonance frequency of the resonator as possible. The equivalent impedance of the resonator is shown in Equation (4.28):

\[
Z_r = R + \frac{j}{\omega C_0} \frac{\omega_0^2 - \omega_p^2}{(\omega^2 - \omega_p^2)}
\]  

(4.28)

Figure 4.8—Ultralow power clock generation block diagram
4.3.2 Oscillator Core Circuit

As discussed, the clock system uses a small battery/supercapacitor to generate a low frequency clock to sample analog data. The clock design needs to generate not only a low frequency but also stable frequency with respect to time and temperature. The clock circuits are also optimized for ultralow power operation. The high Q resonator provides low phase noise and good stability. But as discussed in the previous section, the condition for oscillation is fulfilled when the combined loop-gain of an amplifier and the feedback network is equal to or better than unity with a phase of $2\pi$. The core circuit implemented with a CMOS inverter is based on the Pierce topology, as shown in Figure 4.9.

![Figure 4.9—Oscillator core circuit](image)

The core circuit can be divided between the contribution of the resonator, discussed in section 4.3.1, and the amplifier. The amplifier provides the negative impedance (180-degree phase shift) required to sustain oscillation. The transistors M1 and M2 are the sources of the
transconductance in the oscillator core. The linear approximation of the amplifier is shown in Figure 4.10.

![Figure 4.10](image)

Figure 4.10—Point analysis of crystal oscillator and linear AC representation

In the AC-represented design, the current and voltage across $Z_2$ can be expressed in Equation (4.29) and Equation (4.30) respectively as:

$$I_{Z2} = V_g g_m + I_1 = I_1 Z_1 g_m + I_1$$  \hspace{1cm} (4.29)

and

$$V_{Z2} = I_{Z2} Z_2 = (I_1 Z_1 g_m + I_1) Z_2$$  \hspace{1cm} (4.30)

where

$$g_m = g_{m1} + g_{m2}$$

The two transistors in the amplifier are added based on the AC analysis. The equivalent voltage and impedance in parallel with the shunt capacitor is expressed in Equation (4.31) and Equation (4.32) as:

$$V_{eq} = V_{Z2} + V_{Z1} = (I_1 Z_1 g_m + I_1) Z_2 + I_1 Z_1$$  \hspace{1cm} (4.31)
\[
Z_{eq} = (Z_1 \cdot g_m + 1)Z_2 + Z_1 = Z_1 + Z_2 + g_m Z_1 Z_2 \quad (4.32)
\]

The equivalent impedance looking into the core hence is expressed in Equation (4.33):
\[
Z_a = \frac{Z_1 + Z_2 + g_m Z_1 Z_2}{Z_0} = \frac{Z_0 Z_1 + Z_0 Z_2 + g_m Z_0 Z_1 Z_2}{Z_0 + Z_1 + Z_2 + g_m Z_1 Z_2}
\quad (4.33)
\]

The condition for oscillation is fulfilled when the impedance looking into the core is the same as the equivalent impedance of the resonator \((Z_a + Z_c = 0)\), as shown in Figure 4.10, is expressed in Equation (4.34):
\[
\frac{Z_0 Z_1 + Z_0 Z_2 + g_m Z_0 Z_1 Z_2}{Z_0 + Z_1 + Z_2 + g_m Z_1 Z_2} + R + \frac{j}{\omega} \left( \frac{\omega^2 LC - 1}{(C_0 + C) - (\omega^2 LC C_0)} \right) = 0 \quad (4.34)
\]

Therefore, the critical transconductance needed to sustain the oscillation can be calculated with the formula in Equation (4.35): [35]
\[
g_{m,\text{crit}} = \frac{\omega}{QC} \frac{\left(c_1 c_2 + c_2 c_0 + c_1 c_0\right)^2}{c_1 c_2} \quad (4.35)
\]

The parallel-resonance frequency is attained when the resistance \((R)\) matches the real part of the impedance.

The shunt and the load capacitance are much larger than \(C\), as expressed in Equation (4.36):
\[
C_0 + \frac{C_1 C_2}{C_1 + C_2} \gg C \quad (4.36)
\]

All of the capacitances including the loading capacitances are minimized to decrease the critical transconductance and hence the power consumption. The maximum transconductance can be calculated with the formula in Equation (4.37). [35]
\[
g_{m,\text{max}} = \omega (c_1 + c_2 + \frac{c_1 c_2}{c_0}) \quad (4.37)
\]

The MOS amplifier has high input impedance and causes mismatch from the series resonant resistance. The input impedance of the amplifier \((Z_i)\) is matched to low series resonance \((R)\). The feedback resistor modifies the input impedance of the CMOS inverter, as shown in Equation (4.38). [35]
The 32.768 KHz crystal resonator model selected for use with this design has motional capacitance \( C \) of 1.8 fF, motional resistance \( R \) of 50 kohm, shunt capacitance \( C_0 \) of 0.9 pF, load capacitance \( C_1 \) and \( C_2 \) of standard value. These mechanical characteristics provide an inductor with inductance and a quality factor calculated based the equations provided as 13 kh and 54,000, respectively. The parallel resonance resistance of the crystal is modified by load capacitance and can be calculated to get a \( R_L \) of 2.6 Mohm, which is the same as \( Z_l \). When a buffer with gain \( A \) of 10 is implemented, then \( R_f = 2.6 M\Omega \times 10 = 26 M\Omega \) is required for a successful oscillation. Thus the feedback resistance, \( R_f \), needs to be equal or greater than 26M\( \Omega \) to drive the inverter. Accordingly, the calculated frequency pulling, the critical minimum and maximum transconductance values based on the equations are approximately 9e-16, 320 nA/v and 27 \( \mu \)A/v respectively. The test circuit implemented, in Figure 4.11, uses a low pass filter that tunes to the frequency of oscillation. The low-power amplifiers provide the critical transconductance required for oscillation. The feedback resistor selected is high enough to drive the amplifier.
Figure 4.11—Oscillator core circuit test system

Figure 4.12 shows the 32 KHz transient output waveform from the test circuit. The resonance settles after an initial delay. The HSpice model of the resonator has been used in this simulation. The Spectre simulation of a crystal resonator with such a big inductance value requires an initial stimulus current to kick-start the resonance.
4.3.3 Oscillator Circuit Integration

The reference clock, generated from temperature-compensated biasing and amplitude control with an external crystal resonator, provides process, voltage, and accurate, temperature-variation-proof frequency. The integration of the oscillator circuit for ultralow power clock generation includes the oscillator core, swing control, amplifier, and the frequency divider. In the final design, a CMOS inverter is used as a gain amplifier, similar to the oscillator core circuit of Figure 4.11.

The complete schematic of the clock generation system, including the oscillator core, the swing control that limits the current in the oscillator, the buffer, and the frequency divider, is shown in Figure 4.13. The transistors are biased in weak inversion with large gate lengths for maximum transconductance and ultralow power consumption. The use of an inverter as opposed to a single MOS transistor reduces the current burned by half, since the two transistors in the inverter are in parallel. The capacitor C4 is much larger than C1 and C2. It
is used to smooth the source voltage of M9. The feedback $R_f$ is required to be sized high enough to drive the amplifier and provide a successful resonance.

The swing control provides the minimum current for starting an oscillation in the oscillator core for optimized current consumption. The tail current in the swing control circuit manages the amplitude and reduces power dissipation. The low pass filter blocks the AC components of the input voltage from the gates of the oscillator core to the tail of the swing control. The swing control transistors are biased in weak inversion and are implemented in cascode to provide isolation from $V_{DD}$ and hence ensure supply and process independent biasing.

An ultralow power amplifier is used to buffer the amplitude of the oscillator, which has been reduced for current consumption reasons, to the supply voltage level before using it as an input to the frequency divider. An inverter is used in the final stage to drive the output to rail-to-rail, as shown in the simulated plot in Figure 4.14.

![Figure 4.13](image.png)

**Figure 4.13—The overall schematic of the clock generation system**

The sensor design requires the 32.678 kHz reference clock be divided by a power of two to generate approximately 1 Hz clock for low frequency data sampling in the analog-to-digital converter. The robustness of the frequency divider and ultralow power consumption are the key to frequency divider selection. The low frequency division in this design has the
flexibility to use static dividers (i.e., latches), which are not optimum for noise cancellation. The injection-locked dividers can operate at higher frequencies with a narrow band locking and cancel out noise. [1, 21]

The divide-by-4 is implemented using low-power ring oscillators, which ensure 50/50 duty-cycle. The next stage dividers are implemented using standard cells. The ring oscillators provide a low frequency and multi-phase injection locking. The clock generation system powered by 0.9 V power supply consumes a total of 80 nA current.

![Buffered output waveform from the frequency divider](image)

**Figure 4.14**—Buffered output waveform from the frequency divider

### 4.4 Analog-to-Digital Converter

The analog-to-digital converter (ADC) samples the real-time analog data at the rising edge of the clock to provide the digital representation of the input analog data from the temperature sensor. There are many ADC architectures, depending on sampling resolution, speed,
accuracy, and noise immunity. Some of these architecture options include flash ADC for high-speed and low-resolution designs, dual-slope ADC for low-speed and high-resolution applications, and successive approximation register (SAR) ADC for very low-speed and medium resolution designs. [20] The SAR ADC architecture fulfills the ultralow power requirement for a long battery life, operating at a low sampling rate and medium-to-low resolution.

4.4.1 SAR ADC
One of the most attractive architectures for low-power, low-sampling and medium resolution ADC is successive approximation register (SAR) ADC. [20] SAR ADC operates based on a binary search algorithm. The implemented SAR ADC following the methodology in [36, 37] includes a 9-bit successive approximation register (SAR) for binary search, capacitive DAC that uses a binary-weighted capacitor array with sample and hold (S/H) circuits, and a dynamic latch comparator, as shown in Figure 4.15.

![Figure 4.15—SAR analog-to-digital converter block diagram](image)

Figure 4.15—SAR analog-to-digital converter block diagram
Figure 4.16 provides a more detailed representation of the SAR ADC implemented, including the DAC designed using binary-weighted capacitor arrays. The following sections describe each design block in more detail.

![SAR analog-to-digital converter](image)

**Figure 4.16—SAR analog-to-digital converter**

### 4.4.2 Design of SAR

The successive approximation register (SAR) used in this design, in **Figure 4.17**, is similar to the SAR described in [37]. A low-power-transmission-gate-based D flip-flop (DFF) that can handle set and reset logics is implemented. The main functions of the SAR are pushing the initial MSB approximation to the right value every clock cycle to load the results from the comparator for the next MSB, and holding the output bits. It sets the sample to high, by the end of the current conversion processes in the eleventh clock cycle. The next sampling starts when the sample is driven high.
The following table, Table 4.1, summarizes the operation of the SAR. Initially, sample is driven high and all the output registers are cleared. Then when the second clock fires, sample is held low for the next ten clock cycles and MSB register is set as an initial value. Then the comparator fills the MSB register with the actual bit value based on the feedback from the DAC. The successive registers push the MSB to the right every clock cycle and perform the other operations until the end of the conversion process in ten clock cycles.
Table 4.1—9-bit SAR operation

<table>
<thead>
<tr>
<th>Clock tick</th>
<th>Sample</th>
<th>DAC Bits</th>
<th>DAC out</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>0 0 0 0 0 0 0 0 0 0</td>
<td>$=$</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>1 0 0 0 0 0 0 0 0 0</td>
<td>D8</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td>D8 1 0 0 0 0 0 0 0 0</td>
<td>D7</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>D8 D7 1 0 0 0 0 0 0 0</td>
<td>D6</td>
</tr>
<tr>
<td>5</td>
<td>0</td>
<td>D8 D7 D6 1 0 0 0 0 0 0</td>
<td>D5</td>
</tr>
<tr>
<td>6</td>
<td>0</td>
<td>D8 D7 D6 D5 1 0 0 0 0 0</td>
<td>D4</td>
</tr>
<tr>
<td>7</td>
<td>0</td>
<td>D8 D7 D6 D5 D4 1 0 0 0 0</td>
<td>D3</td>
</tr>
<tr>
<td>8</td>
<td>0</td>
<td>D8 D7 D6 D5 D4 D3 1 0 0 0</td>
<td>D2</td>
</tr>
<tr>
<td>9</td>
<td>0</td>
<td>D8 D7 D6 D5 D4 D3 D2 1 0 0</td>
<td>D1</td>
</tr>
<tr>
<td>10</td>
<td>0</td>
<td>D8 D7 D6 D5 D4 D3 D2 D1 1 0</td>
<td>D0</td>
</tr>
</tbody>
</table>

4.4.3 Digital to Analog Converter (DAC) Design

The DAC, in Figure 4.18, output voltage successively approximates charge distribution of the sample input voltage based on binary weighted capacitor array. As described in the previous section, initially the analog input signal ($V_{in}$) is sampled at the rising edge of the clock and the SAR registers are reset to zero. Then the SAR approximates the most significant bit (MSB) as the one to start the conversion process. The DAC converts this digital data from the SAR into an analog voltage and the output voltage from DAC evaluated with the reference voltage becomes an input to the comparator. The comparator compares the input signal to the DAC output. If the input voltage is smaller than the output from the DAC, the comparator changes the MSB ($D_n$) to zero. Otherwise, a logic one is generated. The SAR loads the comparator signal and approximates the next MSB until the least significant bit (LSB) is known, which takes 10 clock cycles per conversion for a 9-bit ADC.
This means that during each clock cycle, one bit of digital output signal (Dn) gets changed, as shown in Equation (4.39). [20]

\[
V_{\text{COMP}} = -V_{\text{in}} + D_8 \frac{V_{\text{ref}}}{2^1} + \ldots + D_1 \frac{V_{\text{ref}}}{2^7} + D_0 \frac{V_{\text{ref}}}{2^8} + V_{\text{ref}}
\]  

(4.39)

Figure 4.18—Block diagram of the DAC and logic for the bottom plate of the DAC

The sample and hold (S&H) switch provides the control logic. The sample control signal is high when an input is available for sampling and provides the analog input to the comparator, regardless of whether the “Data” signal is high or low. When there is no analog input signal to sample, then the “Sample” control signal is held low and the DAC selects the positive or negative reference voltage, depending on whether the “Data” bit status is low or high, respectively. The control logic provides a power-saving element by running the ADC only when there is data to sample.

Therefore, during sampling, the common terminal at the top plate of the capacitor is connected to the positive reference and the bottom plate is connected to the analog input. [36] In hold mode, the top terminal is disconnected from the positive reference and the analog input is available to the comparator input. The output node of the DAC that has been charged
to the positive reference voltage level is discharged by the input voltage. A simple transmission gate and basic logic gates are used to implement this S&H logic. The aspect ratios of the transistors for this logic are kept small, due to low sampling frequency in this design.

The minimum base capacitances of the capacitors in DAC capacitor array are binary weighted. This is to say that the unit capacitance for each bit position is equal to a value of $C_{\text{unit}} 2^n$. The size of the base capacitance is limited by the process thermal noise floor and resolution of the ADC. [36, 37] The base capacitance ($C_{\text{unit}}$) is sized as small as possible to reduce parasitics. A minimum of 18 fF capacitance has been implemented with a 0.13 um Tezzaron process in this design. A dummy capacitor is used to equal the binary weighted capacitor value of the one bit above the MSB to the total capacitance of all the weighted capacitors in the array. [37] The following table, Table 4.2, summarizes the capacitor sizes of the binary weighted capacitors array including the dummy capacitor in the DAC.
Table 4.2—DAC capacitor components

<table>
<thead>
<tr>
<th>Component</th>
<th>Binary weight</th>
<th>Size (fF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>C0</td>
<td>0</td>
<td>18</td>
</tr>
<tr>
<td>C1</td>
<td>1</td>
<td>36</td>
</tr>
<tr>
<td>C2</td>
<td>2</td>
<td>72</td>
</tr>
<tr>
<td>C3</td>
<td>3</td>
<td>144</td>
</tr>
<tr>
<td>C4</td>
<td>4</td>
<td>288</td>
</tr>
<tr>
<td>C5</td>
<td>5</td>
<td>576</td>
</tr>
<tr>
<td>C6</td>
<td>6</td>
<td>1152</td>
</tr>
<tr>
<td>C7</td>
<td>7</td>
<td>2304</td>
</tr>
<tr>
<td>C8</td>
<td>8</td>
<td>4608</td>
</tr>
<tr>
<td>Dummy</td>
<td>0</td>
<td>18</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td></td>
<td><strong>9216</strong></td>
</tr>
<tr>
<td>Above MSB</td>
<td>10</td>
<td>9216</td>
</tr>
</tbody>
</table>

4.4.4 Design of the Comparator

The comparator, shown in block diagram Figure 4.19, provides logic one if the input voltage in the S&H stage is higher than half of the positive reference voltage. Its output defaults to zero if the input voltage does not meet this requirement. A latch-based comparator, shown in Figure 4.20, is selected in this design and it operates as follows. [20, 37] During sampling, when the latch is de-asserted, the input signal is presented to the comparator and when the latch is asserted (and the reset is low), the comparator compares the DAC output voltage to the reference input voltage to provide the output logic. The buffered output is latched to an SR latch at the last stage.
The transistors M2/M3 are switched based on the input data. When latch is high, the transistors M8/M10 and M9/M11 are in cut-off and M1 is on. The output nodes can be discharged. When latch is low during reset, the transistors M8/M10 and M9/M11 are turned on and M1 is off. The output nodes are charged to positive reference voltage.
The following timing diagram, in **Figure 4.21**, summarizes the operation of the SAR-based ADC. When the clock fires, the “Sample” signal is asserted and all registers are cleared. During the next clock cycle, the analog input is sampled and then the comparator provides the digital output for the MSB. The SAR pushes the MSB to the right, and sampling continues for the next bit positions until the end of the register. The sample signal is driven high again to start the next round of ADC conversions.

![SAR ADC timing](image)

**Figure 4.21—SAR ADC timing**

The simulation results confirmed the SAR ADC function at a supply voltage of 0.9 V at very low power of approximately 500 nA. The ADC outputs the digital data into a memory. The low-power memory design that stores the output data into memory has been described in [38].

### 4.5 Summary

The chapters up to this point covered simulated work for a sensor with a small area and ultralow power consumption. All the analog and digital circuits are optimized for ultralow power operation. Specific focus has been given to the design of the core circuit elements of the sensor for low-power and high-temperature operations. For example, reduction of the power supply voltage from the typical $V_{DD}$ of 1.5 V required by the CMOS process
technology to 0.9 V, and sub-threshold CMOS design of components, the use of low sampling frequency and selectively turning on digital blocks has enabled the core components to operate with less than 1 μA of current. As a result of the ultralow power design, it was possible to use the rechargeable micro batteries to run the sensor long enough to sample and store the required data. Also, the application of a novel circuit biasing technique for low-power and high-temperature operations has been demonstrated.

Table 4.3 summarizes the key power and area results. The sensor’s core and memory has been interfaced with two 0.3 mAhr supercapacitors.

<table>
<thead>
<tr>
<th></th>
<th>Front-End</th>
<th>Core</th>
<th>Memory</th>
</tr>
</thead>
<tbody>
<tr>
<td>Area</td>
<td>1.76 x 1.76 mm²</td>
<td>0.55 x 0.077 mm²</td>
<td>0.39 x 0.4 mm²</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>1.5 V</td>
<td>0.9 V</td>
<td>0.9 V</td>
</tr>
<tr>
<td>Speed</td>
<td>2 MHz</td>
<td>1 Hz</td>
<td>1 Hz / 2 MHz</td>
</tr>
<tr>
<td>Power @ 270°C</td>
<td>12 μW (+digital FSM)</td>
<td>1 μA</td>
<td>158 μA / 694 μA</td>
</tr>
</tbody>
</table>

The startup circuits for the current mirrors in use ensure the sensor will not begin to operate well before the minimum voltage required for correct operation is reached and unnecessary current consumption and unstable operation occurs. The capacitors in use in this design prevent an abrupt change of the power levels, especially when battery-charging using an RF source is in progress. The digital logic, described in the next section, monitors the voltage stored on the capacitor, and turns on the digital part whenever this voltage is charged to V_{DD} by incident RF, and puts the system into “Sleep” mode when the voltage drops below the reference voltage. It also provides RFID handshaking, as described in the next chapter.
Chapter 5  Digital Logic Design

5.1  Introduction

The digital logic is the brain of the sensor that drives events. It monitors the voltage stored on a capacitor and turns on the digital block whenever the capacitor gets charged enough from the reader during an RF incidence. The sensor goes through a finite state machine (FSM) loop and a power-on-reset signal gets asserted. The digital block then controls communication with the RFID reader and data is read from memory. It handles the communication with the RFID reader to receive commands and transmit sensory data wirelessly. The state machine creates control signals based on counters and commands from the RFID reader.

The digital logic puts the system in “Sleep” mode when there is no incident wave and the voltage drops below a reference voltage. When the sensor is in “Sleep” mode, it retains the contents of the sample and holds volatile memory with a power source supplied by a standby supercapacitor. The overall interface of the digital logic is shown in Figure 5.1.

Figure 5.1—Digital logic block diagram
5.2 Sensor Top Level State Machine

The sensor stays in “Power-save” mode until it is reset to change its state and start sampling temperature data after a brief three-minute delay. It remains in the food processing system, sampling once every second. The sample and store process continues a minimum of five minutes until it reaches the end of memory. When the memory is full, then it becomes ready for the reader interrogation. It stays in the “Ready for Interrogation” state until it sees an RFID reader in the range. The communication between the sensor and the RFID reader requires a proper handshaking from reader to sensor and sensor to reader to clearly identify command and data patterns.

The RFID mandatory commands are implemented in the sensor design, including the read command. The reader in the interrogation range in EPCglobal Class-2, Generation-2 Protocol [15-18] expects a 16-bit preamble and the sensor responds with the same 16-bit random number (RN) and waits for acknowledgement (“Ack”) to send its identification number. The sensor responds with data when the RFID reader issues the read command. The state changes to a “Wait” state upon incidence of an RF signal. In the “Ready” state, the sensor is ready to send data to the external reader when it is near the base station. The logic monitors the voltage stored on the capacitor, and enables the digital part whenever this voltage is charged to the reference voltage. It puts the system in “Sleep” mode when the voltage drops below a reference voltage. The FSM for the top-level design is shown in Figure 5.2.
The handshaking of the sensor with the RFID reader is presented in detail in the following sections.

5.3 Sensor to RFID Reader Communication

The digital control part of the RFID communication meets the physical and logical requirements set forth for a UHF RFID air interface in the EPCglobal Class-1, Generation-2 Protocol standard [18]. As described in chapter 2, the EPCglobal specification provides all
the details of the protocol for RFID tag (or sensor, in our case) selection, identification (singulation), and anti-collision. [18] An RFID reader emits a CW signal to continuously provide power to tags after a command has been sent and the selected tag then backscatters energy by modulating the impedance that is applied to the input to the tag antenna. [16] The FSM, depicted in Figure 5.3, decodes incoming Pulse-Interval Encoded (PIE) modulation data, responds to commands from the transmitter (reader), reads data from the internal SRAM memory, and encodes and transmits FM0 coded data to the modulator. It transmits and receives frames most significant bit (MSB) first in a binary tree fashion and uses a cycle redundancy check (CRC) for verifying the integrity of selected frames.

Figure 5.3—RFID air interface protocol block diagram

Based on the Class-1 Generation 2 protocol, the RFID reader manages the tag (or sensor) through three basic interrogator commands and the sensor has seven states that determine the sensor’s reactions in the entire operating process, as shown in Figure 5.4.
The three states of the RFID reader are the “Select” operation for choosing a tag population for inventory and access, the “Inventory” operation for identifying tags for PC, EPC, CRC16 information and the “Access” operation for reading from and/or writing to individual tags. As shown in Table 5.1, the Command parameter specifies the command. The Command parameter of Select command must be 1010. The Target parameter specifies which session or select flag the interrogator wants to select. The Action: parameter specifies how a tag changes their inventoried flag or select flag. The MemBank specifies whether mask applies to EPC, TID or User memory. The Pointer specifies the start location of mask. The Length specifies the length of mask. The Mask specifies binary string that wants to compare with tag memory. The Truncate specifies whether select flag is asserted or deserted. And finally the CRC-16 is the CRC16 parameter for checking the integrity of the data communication between the tag and the reader.
The RFID reader uses five commands namely Query commands, QueryRep commands, QueryAdjust commands, ACK and NAK commands to identify tags during “Inventory”, as shown in Table 5.2. The Command parameter specifies the command. The Command parameter of Select command must be 1000. The DR parameter sets the date rate and modulation format from tag to interrogator. The TRext specifies whether the preamble is pended with a pilot tone from tag to interrogator. The Sel parameter sets which tags respond to Query command. The Session parameter specifies which session will be selected into inventory round. The Target option specifies the value of inventoried flag. The Q is a positive number which sets the range of random numbers that tag will generate and load into slot counter. And finally the CRC-5 is CRC5 parameter.

Table 5.2—Inventory command frame [18]

<table>
<thead>
<tr>
<th># of</th>
<th>Command</th>
<th>DR</th>
<th>M</th>
<th>TRext</th>
<th>Sel</th>
<th>Session</th>
<th>Target</th>
<th>Q</th>
<th>CRC-5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bits</td>
<td>4</td>
<td>1</td>
<td>2</td>
<td>1</td>
<td>2</td>
<td>1</td>
<td>4</td>
<td>4</td>
<td>5</td>
</tr>
</tbody>
</table>

Figure 5.5 shows the reader-sensor handshaking state of the machine before the sensor is ready to send its data. This is the state of the sensor after the RFID reader has gone through “Select” and “Inventory” sessions. In the event of “Ack”, the sensor is ready to send its data if the reader transitions to “Access” mode.
Table 5.3 describes Read, Write and Kill in Access operations.

**Table 5.3—Access command frame [18]**

Defines 8 commands—Req_RN, Read, Write, Kill, Lock, Access, BlockWrite, and BlockErase.

<table>
<thead>
<tr>
<th># of Bits</th>
<th>Command</th>
<th>RN</th>
<th>CRC16</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td></td>
<td>16</td>
<td>16</td>
</tr>
</tbody>
</table>
During the reader inventory, the sensor goes through its FSM and decodes the commands from the reader and responds accordingly. The command decoding for generation-2 protocol standard supports many mandatory commands and other optional commands. All the mandatory commands have been implemented in this design.

As shown in Figure 5.6, the RFID reader always “talks” first. The sensor stays in standby in “Ready” state when the sensor is powered on, near the energized RFID field, and selected for inventory round. It picks a Q-bit random number as a slot counter value when it gets a “Query” command and counts down to “Arbitrate” state. The slot counter determines response timing. [18] This prevents two sensors from responding to the interrogator at the same time and getting involved in a collision. Only Query, QueryRep and QueryAdjust commands modify the slot counter value. The sensor waits in “Arbitrate” state and the slot count down starts every time it receives a QueryRep command until the count reaches zero, by which time the sensor transitions to “Reply” state. But the sensor will decrease its slot counter from 0000h to 7FFFh if it returns to the “Arbitrate” state from another state.

In the “Reply” state the sensor responds to the reader with a 16-bit random number (RN16). Then, if the sensor receives an acknowledgement (“Ack”), which is an RN16 parameter equal to the RN16 parameter that the sensor has backscattered, it transitions to “Acknowledge” state and sends its PC, EPC and CRC-16. The EPC protocol requires that the memory be organized into four separate memory banks, namely Reserved (for storing kill and access passwords), EPC (for protocol control bits like CRC16 in big-endian format), TID (for tag identification), and User (for user specific data storage). The digital logic performs the address processing required to map these banks to a linearly addressed memory.
The sensor returns to the “Arbitrate” state if it receives a negative acknowledgement (Nack). It then moves to the “Open” state to send a new RN16 if it has a nonzero access password and receives a ReqRN command. Otherwise it will be in the “Secured” state. No password has been implemented in our design. The “Kill” state disables the sensor permanently. The following topics cover the implementation of the main modules for RFID communication.

### 5.3.1 Controller Design

The control logic of the sensor is a state machine that is the center of the sensor’s interaction with the RFID reader. It is responsible for the interpretation (decoding) of the command that has been received from the reader when the receiver indicates that a complete frame is received.

The control logic also encodes the sensor’s data and runs the transmitter when there is data to be communicated back to the reader and waits for a control signal that indicates the
transmitter has finished sending data. The control logic of the sensor’s seven states can be condensed into the major states, as shown in Figure 5.7.

![Figure 5.7—Controller state machine](image)

The sensor stays in the “Idle” state when powered. All the control signals are reset and sensor is in a listening mode. In “Receive” state, the controller is ready to receive a command from the reader and it generates the “receive done” signal when the read operation is complete. It returns to “Idle” state if a data error is detected. The command is decoded to determine if it is for read or write and then the operation is executed. In the “Send” state, the data is encoded and transmitted to the RFID reader. The Query, QueryAdj and QueryRep commands are used to manage the number of time slots. The Query and QueryAdj commands load the slot counter with Q-bits of RN from the random number generator as the initial slot counter. Then the sensor transmits its RN if the slot counter is zero for any of the Query, QueryAdj and QueryRep commands. The QueryAdj adjusts stored Q value as per command and takes Q-bits of RN as an initial slot counter, as in the query case. That means the slot counter is initialized for every new Query or QueryAdj based on the received Q-bits. The QueryRep decrements existing slot-counter values. The controller
provides the RN (random number), EPC (ID) and READ (data) data sources to a sequencer. The sensor has a unique ID hardwired externally.

The controller waits for a data from the encoder, in the “Wait” state, until the end of the transition, by which time it goes back to the “Idle” state. The timing waveform in Figure 5.8 illustrates the basic functionality of the controller module.

![Figure 5.8—Controller timing waveform](image)

### 5.3.2 Transmitter Design

The transmit logic sends a response to the reader when the sensor receives a command from the reader. It converts a binary serial data stream to a time domain EPC Class 3 Gen 2 modulated waveform for the RFID protocol. The input clock corresponds to twice the link frequency (LF) as described in the EPC specification. [18] The transmitter sequences the preamble (RN), DATA, and CRC in time to be connected to the tag modulator. The “transmit done” command from the controller tells the sequencer that data transmission is done and instructs it to turn off the transmitter safely. It needs to wait for MAX(trcal, 10*Tpri) to stop...
transmitting gracefully after the current bit is finished. The sensor responds after a time delay of 311.5 μs. The read and write packet, including delimiters for start and end of frame, is as follows in Table 5.4 and Table 5.5.

<table>
<thead>
<tr>
<th>Table 5.4—Read Single Block Response</th>
</tr>
</thead>
<tbody>
<tr>
<td>Response SOF</td>
</tr>
<tr>
<td>packet delimiters</td>
</tr>
</tbody>
</table>

The transmitter uses a state machine for the generation of data sequences, flags, and CRC, RN, SOF (tx_load) and EOF (tx_done) fields before the response packet. The timing waveform in Figure 5.9 illustrates the functionality of the transmitter module, where tx_data is the serial data and tx_buf is the buffered vector data.

Figure 5.9—Transmitter timing waveform
5.3.3 Receiver Design

The receiver is a state machine for decoding the received data from the reader, shown in Table 5.6. It converts RFID protocol into a serial data stream and provides TRCAL (the tx clock divider calibration). It decodes the serial bit stream and helps the controller make decisions. The TRcal measurements provide transmit clock calibration (and the RTcal for debugging purposes). The read frame, in Table 5.5, contains 40 bits of data which include the calculated CRC for error detection, block number and flag bits. The packet delimiters for start and end of frame are also included.

<table>
<thead>
<tr>
<th>Request SOF</th>
<th>Request Flags</th>
<th>Read Single Block</th>
<th>Block number</th>
<th>CRC 16</th>
<th>Request EOF</th>
</tr>
</thead>
<tbody>
<tr>
<td>packet delimiters</td>
<td>8 bits</td>
<td>0x20</td>
<td>8 bits</td>
<td>16 bits</td>
<td>packet delimiters</td>
</tr>
</tbody>
</table>

Table 5.5—Read Single Block Response

A write frame packet contains 72 bits of data which includes the calculated CRC for error detection, flag bits, block numbers and data to be written. The packet delimiters for start and end of frame are also included.
Table 5.6—RFID Mandatory Reader Commands decoded

<table>
<thead>
<tr>
<th>Command</th>
<th>Code</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>QueryRep</td>
<td>00</td>
<td>Mandatory</td>
</tr>
<tr>
<td>ACK</td>
<td>01</td>
<td>Mandatory</td>
</tr>
<tr>
<td>Query</td>
<td>1000</td>
<td>Mandatory</td>
</tr>
<tr>
<td>QueryAdjust</td>
<td>1001</td>
<td>Mandatory</td>
</tr>
<tr>
<td>Select</td>
<td>1010</td>
<td>Mandatory</td>
</tr>
<tr>
<td>NAK</td>
<td>11000000</td>
<td>Mandatory</td>
</tr>
<tr>
<td>Req_RN</td>
<td>11000001</td>
<td>Mandatory</td>
</tr>
<tr>
<td>Read</td>
<td>11000010</td>
<td>Mandatory</td>
</tr>
</tbody>
</table>

The digital logic is implemented in Verilog HDL. The sample verilog codes for the key modules are presented in Appendix A.

5.4 Physical Design of the Sensor

As indicated in the previous sections, the sensor has been implemented in 0.13 μm Tezzaron 3D CMOS process in custom-level & standard cell design in the top die for logic (WTOP). The bottom die (WBOTTOM) in the 3D integration houses the capacitor. This capacitance is not large enough to replace the external supercapacitor but absorbs short power cycles and stabilizes Vdd. The top tier of the layout encompasses the sensor, ADC, SRAM, on-chip coil, power interfaces to supercapacitor and RFID power-harvesting circuits and the digital logic. The components in the top die were physically isolated for improved signal integrity. The sub-circuits that have sensitive signals including the front-end power scavenging components were isolated from sensitive clock sources to make sure no noise is coupled into the circuits. The low frequency (and slow edge rate) components that have noise tolerance were placed in
between the sensitive components. Also the on-chip coil is isolated from the circuit components to minimize RF coupling into the rest of the circuits. 

**Figure 5.10** shows the high-level floor plan of the chip.

![Figure 5.10—WTOP on-chip floor planning](image)

The physical layout has been done in Virtuoso. The parasitics for routing traces for the individual design blocks have been extracted and post-layout simulations done. The bottom tier for the capacitor has also been laid out. The GDS for the top and bottom tier have been generated in 2D in Virtuoso and the two tiers have been merged in 3D with WTOP turned over from left-to-right to mirror WBOTTOM.
Figure 5.11 shows the overall design flow.

![EDA design process](image)

Figure 5.11—EDA design process

The Tezzaron process has six metal layers to route per tier with metal 6 (top metal) for die face-2-face routing. The metal layers 1 and 2 have been used for power and ground planes and the metal layer 3 to layer 5 for signal routing. The 3D process recommends the maximum possible TSV density to improve yield. Also the maximum numbers of vias were employed to lower resistance when multiple-layers routings is involved.

The differential input and output signal traces have been routed in symmetry with matched etch lengths to minimize skew between differential pairs. This is very critical, especially in
the comparators layout. The traces that carry faster edge rate signals have also been routed in the same layer from the source circuit to the destination circuit (or a pad) to avoid via stubs. The power distribution network (PDN) routings use wide traces to minimize IR drop. Signal traces are routed with the same width point-to-point (except in a narrow trace breakouts) to maintain the same impedance and avoid discontinuity. The design uses multiple finger CMOS transistors to reduce drain capacitance parasitics, especially in rectifier layout. The n-wells of the diodes in a single charge pumping stage are separated, since the two share different power supply domains in one point. In the ADC design, the DAC capacitors did not follow common centroid and inter-digitization techniques to mitigate symmetric mismatch issues in this design, due to their low sampling frequency. [39] The clock circuit block is shielded with a ground plane. It was placed closer to the bonding pads, so the routes to the external crystal resonator can be shorter etches. These routes were decoupled from any other signals. The large length devices were used in the core part of the circuits, including the clock circuits that need to operate in low power. The Tezzaron process provides only MOS capacitors. The capacitance values for the MOS cap design has been derived from the area of the MOS based on the correlated capacitance versus gate voltage curves provided in the design guide, Figure 5.12.
The DFF in a SAR has been designed to have a compact layout with short data and clock route. The input and output signals and the power that are shared in the 9-bit SAR, in Figure 5.13, are routed to meet at the junctions. The heights for each bit level are matched to simplify signal and power sharing. This block occupies a small area of 148 µm by 38 µm.

The digital logic block has been designed in Verilog HDL using standard cells library and integrated into the rest of the design interfaces. The block has been synthesized in Design Compiler for static timing closure, and automatically places and routes, including the clock trees, in SoC Encounter, based on the analysis of the logic during the synthesis. The digital logic layout, Figure 5.14, takes approximately 673 µm by 655 µm area, but this could be compressed further if there were die area constraints.

Figure 5.12—MOS cap CV curves [32]
The design DRC and LVS has been done for each sub-circuit. All the sub-circuit components are placed and routed and final LVS performed.

In summary, the 3D IC design of the CMOS temperature sensor chip that scavenges power wirelessly and gathers temperature history in extreme temperature ranges (with the potential to multiplex additional sensors) inside a food processing system is demonstrated. The sensor and associated core circuitry has been implemented in Tezzaron’s 0.13 μm 3D CMOS process, reducing the overall area of the sensor. The core circuit in the custom design
occupies an area of just 0.55 mm x 0.077 mm and the SRAM has an area of 0.39 mm x 0.4 mm. A key problem with previous designs is the significant loss of power due to rectifier inefficiency when implemented in a standard CMOS A significant portion of power is lost due to rectifier inefficiency during CMOS RF-to-DC conversions. A bias control, phase offset and reduction of the input RF signal is implemented to demonstrate a rectifier design with more than 10% CMOS power conversion efficiency. The power conversion efficiency improves with an increase in the aspect ratio of the diode and starts to decrease as the device size of the diode continues to increases.

All the analog and digital circuits are optimized for ultralow power operation. The on-chip integration of components, reduction of the power supply voltage from the typical power required by the CMOS process, subthreshold CMOS design of subcomponents, use of low sampling frequency, and selective activation of design blocks have enabled power optimization. Specific focus has been given to the design of the core circuit elements of the sensor for low-power and high-temperature operations. The main core components operate in 0.9 V with less than 1 \( \mu A \) of current. The SRAM runs from an independent 0.9 V source with 158 \( \mu A \) and 694 \( \mu A \) write and read power and the rest of the circuits operate at 1.5 V. The power optimization has enabled the sensor to run long enough to sample and store the required data powered from a very tiny rechargeable supercapacitors. The sensor’s core and memory has been interfaced with two 0.3 mAhr supercapacitors. The final fabricated chip with all the sub-circuits for the logic in the top tier and capacitor array in the bottom die with 2:1 aspect ratio is shown in Figure 5.15.
Figure 5.15—Chip layout of the top and bottom tiers (not to scale) and the fabricated chip
Chapter 6  Test and Results

This section covers the measurement setup and test of the sensor.

6.1  Introduction

The 3D sensor test chip, described in chapters 3 through 5, has probe points for checking its functionality. It has debugging features for power, data and the clock. The probe points are for the temperature sensor; the ADC; the modulator and demodulator; the clocks; the power conditioning circuits, including the outputs from the voltage limiter and the DC-DC converter that charges the supercapacitor; and an input switch that turns on/off the rectified RF power. The chip has been mounted on a printed circuit board (PCB) to integrate with the micro batteries, antenna matching network and probing loads and test points to debug power and signal interfaces. The RF interface has been tested using two PCBs: one with an on-chip inductor and another for the external antenna to test power scavenging and the ability to modulate/demodulate using RFID reader carrier wave (CW).

The debug interfaces are shown in more detail, in Figure 6.1, with an output debug port for the two voltage levels, reference voltage, analog/RF readout, digital data output from ADC and temperature sensor output. A switch has been placed between the rectified output and the power supply. In the event the charge pump circuit fails to provide enough power to the rest of the circuits, an external DC voltage can be supplied through the batteries or directly from the power supply to continue with the test process for the rest of the circuits. The output from the on-chip inductor coil has been implemented as a port through metal pads to be connected back to the input/output RF port after verifying that coil resonates in the right frequency and bandwidth. The external antenna interface has been designed as an alternate to the on-chip coil in the event the coil fails to resonate in the UHF band. The goal is to get the sensor operational with the on-chip coil to avoid the significant system area increase due to an external chip antenna. The ID for the individual sensor is hardwired off-chip by tying individual bits of the ID to the required reference rails.
6.2 Chip Test Setup and Measurement

A PCB has been designed to test the sensor interfaces. The first iteration of the PCB design uses a 40-pin dual inline package (DIP) socket to quickly verify the basic functions of the chip and determine if there was a yield issue. The PCB design has layers for power plane, ground plane and signal. The component and pin headers are placed and routed and power decoupling capacitors are also part of the design. The board layout has been created in Eagle design tool. The die pads have been wire-bonded to the package pads, as in the bonding diagram in Figure 6.2, using Westbond 7476E wedge-wedge wire bonder. The use of a DIP package helps to do quick measurements by mounting the test chip attached to the DIP package on the PCB socket. The two supercapacitors have been attached to the power sources and all the DC interfaces have been connected to a digital meter. The measurement, as shown in Table 6.1, confirms correct DC readings in all internal nodes.
Table 6.1—Coupling/RF to DC/DC Power

<table>
<thead>
<tr>
<th>Test signal description</th>
<th>Signal CAD name (test pin #)</th>
<th>Anticipated voltage (Vexp), v or behavior</th>
</tr>
</thead>
<tbody>
<tr>
<td>Limiter output voltage</td>
<td>Vreg_probe (17)</td>
<td>Limiter output power charging the big capacitor in 1.5V range.</td>
</tr>
<tr>
<td>External control input voltage at the limiter</td>
<td>vin_ext (18)</td>
<td>1.5V Enable transmission gate switch when RF power is in use</td>
</tr>
<tr>
<td>Core circuit VDD</td>
<td>VDDS (39)</td>
<td>0.9V from DC to DC conversion at nominal 3V of a coin battery input</td>
</tr>
<tr>
<td>Regulated output voltage</td>
<td>VDD (14)</td>
<td>1.5V (expected to discharge with an increase in inductive/RF power range)</td>
</tr>
<tr>
<td>Reference voltage</td>
<td>VSS (2, 10, 15, 32)</td>
<td>References</td>
</tr>
<tr>
<td>Sensor External DC voltage</td>
<td>Vbatp_TS (19)</td>
<td>3.0(used 1.5 Vddmax so far for fear of breakdown limit)</td>
</tr>
<tr>
<td>Memory External/battery DC voltage</td>
<td>Vbatp_mem (1)</td>
<td>3.0(1.5 when power source used)</td>
</tr>
<tr>
<td>Enable external data input</td>
<td>Vin_ext_dig (8)</td>
<td>1.5</td>
</tr>
</tbody>
</table>

The table shows the measurement and the predicted node voltages based on Spice simulations. The results show a reasonable correlation between measurement and simulation. But a probe on the RF front-end signal pins revealed a degraded performance with the main resonance shifting outside the UHF band due to the added parasitics of the DIP package on the on-chip coil output. An effort was made to design another iteration of a custom board to test the rest of the interfaces and to try to get good data for the RF front-end.
Figure 6.2—40-pins DIP package bonding diagram and magnified view of the bond picture

The second iteration of the board, with custom bonding pads on the PCB, has been designed. The header pins are included to probe some of the debug interfaces, as appropriate. The clock and the RF interfaces, for example, don’t use header pins due to the negative effect of the added parasitics of the header pins on the sensitive signals. The center of the board is cut out for wire-bonding the test chip. All interfaces of the chip have a break-out to exposed metal pads. The pads are designed with enough pitch for wire-bonding and they are made large enough so they can have good contact with the probe, but small enough not to create additional loading on the debug or input/output interface signals. The probe pads for power (and ground), data, and clock are isolated. The enlarged view of the prototype test board design is shown in Figure 6.3.
The sensor’s RF I/O pins are routed as closely to the antenna as possible. A ground reference plane is cutout under the antenna part and no other components are placed nearby because the range and performance of the antenna can be affected by the coupling of the antenna radiation to a ground plane or other components closer to the antenna. A 50-ohm matching trace has been routed from the RF output/input of the chip to the input of the antenna feed to minimize impedance discontinuity. The matching passive circuits in the antenna feedline path are used to tune the antenna, decouple DC, connect the antenna to the RF chip interfaces and suppress harmonic contents. All the antenna interface signals are routed in a single layer to avoid vias and the associated parasitics. No connector test pins are used in these RF interfaces to avoid parasitics and hence the potential RF degradation. The probing for the RF pins is done directly off the pads. Two dies have been wire-bonded to the two variants of this same board: one that uses an on-chip coil and one that uses an external antenna. The bonding diagram is shown in Figure 6.4.
The testing on the second board started with power. A PS2520G power supply has been used to power the device under test (DUT) for programmable power and a longer hour-testing procedure. The appropriate input voltage and current has been programmed to the power supply. The output clock signals were connected to a Tektronix TDS684B oscilloscope. The output from the oscilloscope helps to monitor not only the amplitude but also the phase, duty cycle and frequency of the clock signs. The RFID reader has been connected to its host computer. The reader antenna has been connected to the host computer in order to transmit and receive through the transmit / receive antenna.

The overall test setup is shown in Figure 6.5. This setup does not show the separate test environments, including the vector network analyzer (VNA) that was used to characterize the internal coil (and antenna), time domain reflectometer (TDR) used to characterize impedance.
of the transmission linefeed to the internal coil (and antenna), and a programmable oven used for temperature characterization of the sensor.

![Figure 6.5—DUT setup](image)

### 6.3 Detailed Test Results and Conclusions

The impedance of the transmission linefeed to the antenna was characterized using TDR to fix off-chip impedance discontinuities. A Tektronix CSA8000B communications signal analyzer has been used to characterize the impedance of the transmission line feed to the RF port. The TDR initially showed a 25 ohm as opposed to 50 ohm feed due to an etch breakout between the antenna and the on-chip coil feed, and this has initially caused confusion. This
has been solved by using separate boards for on-coil and external antenna. The TDR also show 377 ohm for a small time duration due to the reference plane cutout around the antenna. The networks for the chip antenna and the on-chip coil have been probed and the data collected using Agilent E8364B PNA vector network analyzer (VNA). The external antenna has been probed for return loss (S11) in UHF range as a baseline.

A programmable oven provided temperature characterization of the sensor. The DUT is placed inside a 550 Vulcan programmable oven to sweep the temperature from room temperature to 140 degrees C. High-temperature-resistant ribbon cables have been extended to an external oscilloscope to capture the data. An in-house developed system programmed in C has been customized to communicate with the oven and the oscilloscope over GPIB interface to keep the DUT running and automatically record data over high resolution temperature sweeps in the form of listing text file. The system also displayed the output waveform from the DUT on the scope. The clock signals were probed by connecting them to the Tektronix TDS684B oscilloscope before putting the DUT in the oven.

The RF front-end includes an antenna and coil, and interfaces for power and data modulation and demodulation. The s-parameter of the external antenna exported from the VNA measurement is plotted in Agilent Design System (ADS) for the reflection coefficient (or return loss s-parameter S11), as shown in Figure 6.6. The reflection coefficient plot shows that all the power is reflected at lower frequencies and the antenna will not radiate or modulate signals at these frequencies. However, in the UHF range (860 MHz-960 MHz), the antenna shows a resonance and the RF power can be delivered to the sensor or transmitted from it.

Similarly, the return loss of the on-chip coil from the exported s-parameter is plotted, as shown in Figure 6.7. The center frequency has been shifted to the higher frequency by adding an approximated small capacitor in series. The on-chip coil experiences more reflection in the UHF range, especially when compared to the antenna at the center frequency. The plot shows that the coil can still scavenge power and modulate the reader CW with a reduced performance.
Figure 6.6—Measured return loss of the external UHF antenna
Once the performances of the boards with an antenna and on-chip coil are characterized, the voltage output at the rectifier is measured at different ranges of the base station. The efficiency is recorded at different antenna matching loads by comparing the incident CW with the rectifier output. Figure 6.8 depicts the power conversion efficiency of the implemented system. The measurement using an external antenna for similar aspect ratio CMOS diode implementation matches the simulation. The plot also demonstrates matching to the input RF power is critical to obtain higher power conversion efficiency.

Figure 6.7— Measured return loss of the on-chip antenna
Figure 6.8—Rectifier Power Conversion Efficiency

The observations for RF interface signals based on VNA data has been tabulated in Table 6.2.
Table 6.2—RF Interface

<table>
<thead>
<tr>
<th>Test signal description</th>
<th>Signal CAD name (test pin #)</th>
<th>Anticipated voltage (Vexp), v or behavior</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output from the on-chip inductor coil</td>
<td>coil_p (9)</td>
<td>Resonates at 900 MHz</td>
</tr>
<tr>
<td>Input/output RF port; connect output from the on-chip coil or external antenna</td>
<td>RF_in (11)</td>
<td>Communication through UHF antenna</td>
</tr>
<tr>
<td>Backscatter data output</td>
<td>varp_mod (13)</td>
<td>TX Data that starts with sensor ID as a preamble</td>
</tr>
<tr>
<td>Backscatter data ref</td>
<td>varn_mod (12)</td>
<td></td>
</tr>
</tbody>
</table>

The voltage at the limiter output is measured. The limiter output voltage for the antenna board is shown in Figure 6.9. The multimeter plot confirms a proper functionality of the power scavenging system. The ripple on the output voltage improves with additional on-board decoupling capacitors in the next stages of the design. However, the power delivery using a coil is poorer but still above the threshold voltage for this technology, as shown in Figure 6.10. The limiter provides approximately 50% less power than the simulated output power when using a coil, possibly due to impedance discontinuities and a poorer quality factor of the on-chip coil.
The limiter output plots are reproducible when the base station is moved closer to the sensor. This has proved that the limiter output is insensitive to reader antenna range in both antenna and on-chip coil cases, which is the anticipated behavior. The DC-to-DC converter converts a
higher DC voltage to a lower level voltage as expected. The voltage output after DC-to-DC conversion using an antenna matches about 72% of simulations. The input power matches 100% to the power at the chip power rail. The voltage probe, for example, for the reference voltage is temperature independent. The plot in Figure 6.11 shows the output of the listing file plotted in Matlab from the bandgap probe point of DUT’s reference voltage. The test results confirm a bandgap response to an increase in temperature.

![Figure 6.11—Voltage reference plot–bandgap response](image)

The data logger includes circuits for temperature sensor, the ADC, clock generation, and memory. Like the output reference voltage case, the temperature sensor analog output, which is voltage representation over temperature, is probed in the oven. The plot of the listing file from the temperature sensor shows a linear operation for temperatures up to 100 degrees C, as shown in Figure 6.12.
The prediction model of the calibration of the measured output of the sensor is obtained by the third-order regression of the temperature data. **Figure 6.13** shows the calibration fit and the sensor output in the same plot. The minimum residual error between the predicted calibration data and the measurement in most regions of the plot indicate a good fit.
The next critical signals tested were clocks. Testing for the clock signals focused on the crucial frequency reference used by the ADC to sample an analog data from the sensor. The output waveform from the oscilloscope, probed before the final division flip-flop, help to monitor not only the amplitude but also the phase, duty cycle and frequency of the clock signals. Depending on how much current is provided to the sensor, the output frequency from the probe point for the clock was in 100s of KHz range. The clock at this stage, shown in Figure 6.14, has a much higher frequency than originally designed. The clock also does not have a 50% duty cycle (or it has a high duty cycle), which would mean sampling at the rising edge is slower than the anticipated rate, and power utilization is higher as the clock is ON rather than OFF during most of the cycles.

![Figure 6.14—Internal node probe of the sampling clock](image_url)
To ensure the crystal in use has no issues, a separate clock generation breadboard experimental circuit similar to Figure 4.11 has been built using a FET and a CMOS inverter. The test circuit provides the type of output we expected to see, as in Figure 6.15.

![Image](image.png)

**Figure 6.15—Crystal breadboard test using CMOS inverter and FET**

The tests on the analog-to-digital converter showed a very poor resolution during variation in temperature in the heating oven due to the use of higher sampling clock frequencies than originally designed. As a result of the higher sampling frequency, the resolution of the ADC was very poor. The ADC bits toggle at coarse temperature sweeps. The clock signals didn’t exhibit the kind of frequency and duty cycle signals predicted in the simulations. It appears the voltage-controlled oscillator may not have large enough feedback resistance due to process corners or other yield issues and that the buffer in the oscillator core was unable to drive the crystal resonator. It has caused the desired frequency to be defined by the voltage-controlled oscillator used in the frequency division. This has been the major failure that prevented the testing of the remaining interfaces. Therefore the
whole system was not tested over a range of temperature. A Focused Ion Beam (FIB) has been used as an additional debug effort to adjust a feedback resistor of the oscillator core to provide an external resistor through a potentiometer and tune the sample frequency. The traces in layers M4 and M5 are buried deep in the wafer with backmetal, fill, TSVs, active, M1, M2, M3, M4, M5 and top metal (M6) stackup, making the traces inaccessible and the FIB exercise unrealistic.

As described in the previous sections, the sensor has been designed to sample data every second until it reaches the end of memory, and to then respond with data when interrogated by an external industry standard RFID reader in the 860-960 MHz frequency range. The supercapacitors power the sensor and its memory during the sampling phase. In the presence of an RFID, the incident RF signal is used to charge the supercapacitors, power the digital block of the sensor, and transmit data back to the reader.

The following tables, Table 6.3 and Table 6.4, provide the observations recorded for the core signals and the clocks.

### Table 6.3—Core signals

<table>
<thead>
<tr>
<th>Test signal description</th>
<th>Signal CAD name (test pin #)</th>
<th>Anticipated voltage (Vexp), v or behavior</th>
</tr>
</thead>
<tbody>
<tr>
<td>Digital data output from ADC</td>
<td>D8-D0 (24-31)</td>
<td>8-bit temp readout to be calibrated (expected to change with change in temperature)</td>
</tr>
<tr>
<td>CTAT output from the temperature sensor</td>
<td>Ctat (16)</td>
<td>Analog voltage output as a function of change in temp</td>
</tr>
<tr>
<td>ID for the sensor; tie to vdd or gnd</td>
<td>ID_ext7- ID_ext0 (33-38, 40)</td>
<td>Sensor ID defined by the switches thrown to on/OFF positions</td>
</tr>
</tbody>
</table>
Table 6.4—Clocks

<table>
<thead>
<tr>
<th>Test signal description</th>
<th>Signal CAD name (test pin #)</th>
<th>Anticipated voltage (V_{exp}), v or behavior</th>
</tr>
</thead>
<tbody>
<tr>
<td>Crystal clock +</td>
<td>crystal_p (21)</td>
<td>32KHz 50% duty cycle clock @ Osc core</td>
</tr>
<tr>
<td>Crystal clock -</td>
<td>crystal_n (22)</td>
<td>32KHz 50% duty cycle clock (180 deg off phase)</td>
</tr>
<tr>
<td>Temperature sensor clock</td>
<td>CLK_TS (23)</td>
<td>In HZ range before final division, 50% duty cycle clock (High frequency in kHz range depending on supplied power)</td>
</tr>
<tr>
<td>ASIC clock</td>
<td>CLK ASIC (3)</td>
<td>MHz 50% duty cycle clock</td>
</tr>
</tbody>
</table>

In summary, the test on the RF front-end of the sensor proved a good correlation of simulation to hardware. The power scavenging and biasing for insensitivity to PVT (process, voltage and temperature) variations performed as expected. The measurements on the data logger also show a functioning biasing and temperature sensor. The linearity of the temperature sensor at high temperatures is poorer but could be converted to digital data with a higher resolution ADC.
Chapter 7  Conclusions

7.1 Summary

The design, implementation and testing of a new type of fully integrated, ultralow power, low density, small area, and high temperature operation smart telemetry system has been demonstrated in this dissertation. We have presented inexpensive wireless CMOS sensor that stores temperature history in the 27-140 degree C range and interfaces with an industry standard RFID system.

The application of novel circuit biasing techniques for ultralow power and high temperature operations and improved CMOS RF-DC rectification for the front-end design was achieved. An improved RF-to-DC power conversion efficiency, using threshold compensation techniques, for charging the backup power sources from the scavenged RF power, has been demonstrated. Improved rectifier efficiency by more than 10% and an increased output DC voltage was accomplished by static basing to compensate for the CMOS diode threshold voltage and the use of low-threshold transistors of the CMOS process.

The core circuit elements, including low frequency reference clocks, ADC, and temperature sensor were designed for ultralow power and extreme temperature operations. The use of lower supply voltage from the typical VDD required by the CMOS process technology, leveraging sub-threshold CMOS design of components, clock gating and selectively turning on digital blocks has enabled the core components to operate with less than 1 μA of current. The digital logic has been designed to monitor the voltage stored on the capacitor, and turn on the digital part whenever the voltage is charged to Vdd by incident RF in UHF band (860-960 MHz), and put the system into sleep mode when the voltage drops below the reference voltage. Most of the components, including an on-chip coil, have been implemented on-chip, increasing the level of integration and decreasing the overall power usage and cost.

The successful implementation of the RF front-end circuits, power conditioning and the operations of the core subcomponents in ultralow power and extreme temperatures have demonstrated the potential to commission battery-assisted sensors for food processes and
other applications. The sensor could be powered wirelessly when the sensing occurs within the RF read range closer to the RFID reader and could also be placed in isolated locations to gather sensory data, powered from a small supercapacitor.

### 7.2 Future Work

The future design of sensors in the 3D IC processes could include a detailed study of the pros and cons of stacking components vertically. It requires more feasibility study work to explore if additional benefits can be harnessed in 3D—for example in memory design. It would be interesting to see if the memory power can be further optimized in 3D even at such low data rate designs. The feasibility study could also include thermal issues in 3D and the effect on the performance of circuits. In 3D IC CMOS processes that provide higher density capacitor, the possibility of making even higher density power storage supercapacitor on-chip by using additional wafer as capacitor array can be investigated. Also, a small part of this work has been exploring the possibility of powering these sensors directly from an RF (AC) source, if charging a battery with a DC power source were not part of a requirement. A baseline chip was fabricated to show the possibility of powering sub-components, including inverters, sensors, and ring oscillators, directly from an RF source. The preliminary results have shown that making complex designs powered directly from an RF power source is a challenge. It requires more work to demonstrate that advanced circuits can be operated directly from an RF source. The next phase work should also include off-chip interfaces to calibrate critical design interfaces—for example tuning designs that have feedback systems that are critical to stability. The feedback resistor in the oscillator core of the clock generation system can be designed to be tuned to an optimum value off-chip.
REFERENCES


APPENDICES
Appendix A: Sensor Top Level Logic
module ASIC_top(/*AUTOARG*/)
  // Outputs
  sample, tx_data,
  // Inputs
  vdd, clk, rst, idExtern, data_in, rx_data
);

input vdd;
input clk; // 1.6 MHz clock
input clk_1Hz; // 1 Hz clock
input rst; // reset corresponding to 1.6 MHz
input reset_n; // reset corresponding to 1Hz
input [3:0] idExtern;
input [7:0] data_in;
input rx_data;

output sample;
output tx_data;

wire [15:0] id_fsm;
wire [2:0] fsm_state;
wire read_done;
wire write_done;
wire [7:0] data_out;
wire [9:0] read_address;

fsm u_fsm(
  // outputs
  .id (id_fsm),
  .fsmState (fsm_state),

  // inputs
  .clk(clk_1Hz),
  .rst (reset_n),
  .rfPresent(vdd),
  .write_done(write_done),
  .read_done(read_done),
)
.idExtern(idExtern)
);

mem_interface u_mem_interface(
  // outputs
  .sample (sample),
  .write_done (write_done),
  .read_done (read_done),
  .data_out (data_out), // data to go to the RFID module

  // inputs
  .clk (clk),
  .reset (rst),
  .clk_1Hz (clk_1Hz),
  .reset_1Hz (reset_n),
  .fsm_state (fsm_state),
  .read_address (read_address[8:0]), // from RFID
  .data_in (data_in) // data from A-D converter
);

top u_top(
  // outputs
  .tx_data (tx_data),
  .data ()
  .CRC(),
  .pointer(),
  .RN16(),
  .length(),
  .mask(),
  .tx_load(),
  .tx_buf(),
  .read_address(read_address),

  // Inputs
  .clk(clk),
  .reset(rst),
  .rx_data(rx_data),
  .mem_data (data_out),
  .id_in(id_fsm),
  .ce (vdd)
);
endmodule // ASIC_top
Appendix B: Top Level of the RFID Protocol
module top (clk, reset, rx_data, tx_data, data, CRC, pointer, RN16, length, mask, tx_load, tx_buf, mem_data, id_in, ce);

  `include "epc_tag.v"
  //top level of the whole architecture
  // Log2(clock cycles for 10 maximum TARI value) (def: Log2(490) = 9 @Tck=520ns)
  parameter LOG2_10_TARI_CK_CYC = 9;
  // Min Clock cycles for 12,5 us delimitier
  parameter DELIMITIER_TIME_CK_CYC_MIN = 22;
  // Max Clock cycles for 12,5 us delimitier
  parameter DELIMITIER_TIME_CK_CYC_MAX = 24;
  parameter WordsRSV = 8;
  parameter WordsEPC = 16;
  parameter WordsTID = 8;
  parameter WordsUSR = 256;
  // 1/2 memory address pins
  parameter AddrRSV = 2;
  // 1/2 memory address pins
  parameter AddrEPC = 3;
  // 1/2 memory address pins
  parameter AddrTID = 2;
  // 1/2 memory address pins (maximum)
  parameter AddrUSR = 5;
  parameter Data = 16;

input clk;
input reset;
input rx_data;
input [15:0]id_in;
input [7:0]DTO;
input [15:0]mem_data;
input ce;

output tx_data;
output[31:0] data;
output[15:0] CRC;
output[15:0] pointer;
output[15:0] RN16;
output[7:0] length;
output[MASKLENGTH - 1:0] mask;
output[2:0] tx_load;
output[15:0] tx_buf;
output[9:0] read_address;

wire tx_data;
wire[31:0] data;
wire[15:0] CRC;
wire[15:0] pointer;
wire[15:0] RN16;
wire[7:0] length;
wire[MASKLENGTH - 1:0] mask;
wire[2:0] tx_load;
wire[15:0] tx_buf;
wire[31:0] Data_ri;
wire[15:0] CRC_ri;
wire[15:0] Pointer_ri;
wire[15:0] RN16_ri;
wire[7:0] Length_ri;
wire[MASKLENGTH - 1:0] Mask_ri;
wire rec_en;
wire[3:0] rx_done;
wire[2:0] tx_load_i;
wire[15:0] tx_buf_i;

// Enabling signals
assign rec_en = ce;

// Output signals
assign data = Data_ri;
assign CRC = CRC_ri;
assign pointer = Pointer_ri;
assign RN16 = RN16_ri;
assign length = Length_ri;
assign mask = Mask_ri;
assign tx_load = tx_load_i;
assign tx_buf = tx_buf_i;

receiver receiver_i(.clk(clk), .reset(reset), .rx_data(rx_data), .enable(rec_en), .rx_done(rx_done), .data(Data_ri), .CRC(CRC_ri), .pointer(Pointer_ri), .RN16(RN16_ri), .length(Length_ri), .mask(Mask_ri));
TagCtrl TagCtrl_i(.clk(clk), .reset(reset), .mem_DTO(mem_data), rx_done(rx_done),
.data(Data_ri), .pointer(Pointer_ri), .RN16(RN16_ri), .length(Length_ri), .mask(Mask_ri),
.tx_load(tx_load_i), .tx_buf(tx_buf_i), .addr_mem(read_address), .id_in(id_in));
transmitter transmitter_i (.clk(clk), .reset(reset), .tx_load(tx_load_i), .tx_buf(tx_buf_i),
.tx_data(tx_data));
endmodule
Appendix C: Memory Control Module
module mem_interface /*AUTOARG*/
//generates addresses for sequenabletial read and write and genableerates additional control
//signals for interfacing
//with the rest of the design and the main FSM.
  // Outputs
  sample, write_done, read_done, data_out,
  // Inputs
  clk, reset, clk_1Hz, reset_1Hz, fsm_state, read_address, data_in
 );
// Inputs main clock that is module runs off of 1Hz for Write
// 2MHZ for Read
input clk;
// Reset synchronized with clk, active low
input reset;

// this is the 1HZ clock to be used for write
input clk_1Hz;
input reset_1Hz;
input [2:0] fsm_state;
// input address for read
input [8:0] read_address;
// write data input
input [7:0] data_in;

// Outputs
// Control signal to trigger next sampling round
output sample;
// Control signal indicating all memory locations
// have beenable wrienablenable to
output write_done;
// Control signal indicating all memory locations have
// been able read from
output read_done;
// Read data output
output [7:0] data_out;
// Registers and Wires
wire sample;
wire read;
wire write;
wire [8:0] address;

reg [3:0] sample_reg;
reg [3:0] next_sample_reg;
reg [8:0] write_address;
reg [8:0] next_write_address;
reg [8:0] int_read_address;
reg [8:0] next_int_read_address;
reg write_done;
reg next_write_done;
reg read_done;
reg next_read_done;

`ifdef DEBUG
parameter max_address = 9'd16;
`else
parameter max_address = 9'd300;
`endif

// generate control signals based on the state machine states

// Write when enable state machine is in Data capture mode
assign write = (fsm_state == 3'd2);

// Read when enable state machine is in transmit data mode
assign read = (fsm_state == 3'd4);

// Multiplex read and write address to memory
assign (read) ? (int_read_address) : ((write) ? write_address : 9'b0);

// Logic for generating address for read and write
always @ (*AUTOSENSE*/int_read_address or read or read_address or sample or write or write_address or write_done)
begin
    next_write_address = write_address;
    next_int_read_address = int_read_address;
end
case({write,read})
  2'b10:
    begin
      if(sample)
        begin
          if(!write_done) && (write_address < max_address))
            begin
              next_write_address = write_address + 1'b1;
            enabled
          else
            begin
              next_write_address = 9'b0;
            enabled
        enabled // if (sample)
      enabled // case: 2'b10
    2'b01:
      begin
        next_int_read_address = read_address;
      enabled // case: 2'b10
    default:
      begin
        next_write_address = 9'b0;
        next_int_read_address = 9'b0;
      enabled
      enabled // case ({write,read})
    enabled // always @ (...)

always @ (/*AUTOSENSE*/address or read or sample or write or write_done)
begin
  next_write_done = write_done;

if(read)
  begin
    next_write_done = 1'b0;
  enabled
else
  begin
    if(write_done || (write && sample && (address == max_address)))
      begin
        next_write_done = 1'b1;
  end
end
enabled
enabled // else: !if(read)
enabled // always @ (...)

always @ (*AUTOSENSE*/address or read_done or write)
begin
    next_read_done = read_done;
    if(write)
        begin
            next_read_done = 1'b0;
            enabled
        else
            begin
                if(read_done || (address == max_address))
                    begin
                        next_read_done = 1'b1;
                        enabled
                    enabled // else: !if(write)
                enabled // always @ (...)
        always @ (posedge clk or negedge reset)
        begin
            if(!reset)
                begin
                    read_done <= 1'b0;
                    int_read_address <= 9'b0;
                    enabled
                else
                    begin
                        read_done <= next_read_done;
                        int_read_address <= next_int_read_address;
                        enabled
                    enabled // always @ (posedge clk or negedge reset)
                // logic for genableerating sample signale
                assign sample = sample_reg[3];
            always @ (*AUTOSENSE*/sample or sample_reg or write or write_done)
            begin
                next_sample_reg = sample_reg;
                if(write && !write_done)
                    begin

if(sample)
  begin
    next_sample_reg = 4'b0;
  enabled
else
  begin
    next_sample_reg = sample_reg + 4'b1;
  enabled // if (write)
else
  begin
    next_sample_reg = 4'b0;
  enabled // else: !if(write)

  enabled // always @ (...)

always @ (posedge clk_1Hz or negedge reset_1Hz)
begin
  if(!reset_1Hz)
    begin
      sample_reg <= 4'b0;
      write_done <= 1'b0;
      write_address <= 9'b0;
    enabled
  else
    begin
      sample_reg <= next_sample_reg;
      write_done <= next_write_done;
      write_address <= next_write_address;
    enabled
    enabled // always @ (posedge clk or negedge reset)
  // Instantiate the memory model here
  // To be replaced by the SRAM in the actual design

mem_model uMem(
  //outputs
  .data_out (data_out),
  // Inputs
  .address (address),
Table A.1—3D process dielectric layer stackup [32]

<table>
<thead>
<tr>
<th>Layer</th>
<th>Thickness (microns)</th>
<th>Dielectric Constant</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Typical Capacitance</td>
<td>Best Capacitance</td>
</tr>
<tr>
<td>TM IDM4 (TEOS)</td>
<td>0.78</td>
<td>0.897</td>
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<tr>
<td>TM IDM3 (SiN)</td>
<td>0.05</td>
<td>0.0575</td>
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<tr>
<td>TM IDM2 (TEOS)</td>
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<td>0.667</td>
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<tr>
<td>TM IDM1 (SiN)</td>
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<td>0.0575</td>
</tr>
<tr>
<td>M5 IDM4 (FTEOS)</td>
<td>0.34</td>
<td>0.391</td>
</tr>
<tr>
<td>M5 IDM3 (SiN)</td>
<td>0.05</td>
<td>0.0575</td>
</tr>
<tr>
<td>M5 IDM2 (FTEOS)</td>
<td>0.4</td>
<td>0.46</td>
</tr>
<tr>
<td>M5 IDM1 (SiN)</td>
<td>0.05</td>
<td>0.0575</td>
</tr>
<tr>
<td>M4 IDM4 (FTEOS)</td>
<td>0.34</td>
<td>0.391</td>
</tr>
<tr>
<td>M4 IDM3 (SiN)</td>
<td>0.05</td>
<td>0.0575</td>
</tr>
<tr>
<td>M4 IDM2 (FTEOS)</td>
<td>0.4</td>
<td>0.46</td>
</tr>
<tr>
<td>M4 IDM1 (SiN)</td>
<td>0.05</td>
<td>0.0575</td>
</tr>
<tr>
<td>M3 IDM4 (FTEOS)</td>
<td>0.34</td>
<td>0.391</td>
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### Table A.1 Continued

<table>
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<th>Layer</th>
<th>Thickness (microns)</th>
<th>Dielectric Constant</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Typical Capacitance</td>
<td>Best Capacitance</td>
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<tr>
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<td>0.0575</td>
</tr>
<tr>
<td>M3 IDM2 (FTEOS)</td>
<td>0.4</td>
<td>0.46</td>
</tr>
<tr>
<td>M3 IDM1 (SiN)</td>
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<td>0.0575</td>
</tr>
<tr>
<td>M2 IDM4 (FTEOS)</td>
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<td>0.391</td>
</tr>
<tr>
<td>M2 IDM3 (SiN)</td>
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<td>0.0575</td>
</tr>
<tr>
<td>M2 IDM2 (FTEOS)</td>
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<td>0.46</td>
</tr>
<tr>
<td>M2 IDM1 (SiN)</td>
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<tr>
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</tr>
<tr>
<td>STI</td>
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<td>0.46</td>
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<tr>
<td>BS ILD1</td>
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<tr>
<td>BS ILD2</td>
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