# ABSTRACT

WANG, GANGYAO. Design, Development and Control of >13 kV Silicon-Carbide MOSFET based Solid State Transformer (SST). (Under the direction of Dr. Alex Huang.)

Within the advent of the smart grid system, the solid state transformer (SST) will replace the traditional 60 Hz transformer formed by silicon steel core and copper windings and provides the interface between the high distribution voltage and low utility voltage. Other than the smaller size and less weight, SST also brings many more functionalities including voltage regulation, reactive power compensation, power management and renewable energy integration. The motivation of this research is to design a solid state transformer based on the wide band-gap Silicon Carbide (SiC) power MOSFETs and compare it with the silicon IGBT based SST.

With wider band-gap and higher critical electrical field, the high voltage SiC power device has advantages over silicon power device for both conduction and switching. An extensive study and characterization of the SiC MOSFET was first carried out. It has been found that the MOSFET parasitic capacitors store significant amount of energy and the MOSFET turn on loss is high but turn off loss is virtually zero with small enough turn on gate resistor. A method for estimating the MOSFET parasitic capacitances has been proposed and explained in detail. A PLECS loss simulation model has been developed for the >13 kV SiC MOSFET which has been verified through a boost converter with the SiC MOSFET switches under 40 kHz for both soft switching and hard switching conditions separately.

Widely used full bridge circuit has been chosen as the topology for the SST rectifier for its simple structure and bidirectional power transfer capability. Form three different SPWM modulation methods, the bipolar single frequency SPWM method has been

identified as the most suitable control algorithm for the >13 kV SiC MOSFET base rectifier. With such modulation method, the generated PWM voltage frequency equals to the switching frequency, the each MOSFET equivalent switching frequency under hard switching conditions is only 1/4 of the PWM voltage frequency. The SST rectifier efficiency has been simulated and measured for 6 kHz and 12 kHz switching frequency with 6 kV dc bus voltage and 3.6 kV ac voltage, which is 99.2% for 6 kHz with 8.8 kW load and 98.5% for 12 kHz with 8.3 kW load.

The SST DC-DC stage utilize the dual active half bridge (DHB) as the topology, its zero voltage switching (ZVS) turn on range has been analyzed and it is concluded that the dead-time and device parasitic capacitances will reduce the ZVS range while the magnetizing current will increase the ZVS range. Since the SiC MOSFET has very high turn on loss, it is desired to have ZVS for the full load range. The high frequency transformer with integrated leakage inductance for the DHB operation has been designed, the magnetizing inductance has been decreased for increasing the ZVS range. The DC-DC stage efficiency has been measured as 96.9% for 10 kHz switching frequency and 10 kW load, and the peak efficiency is 97.5% for 10 kHz switching frequency and 5 kW load.

The SST inverter stage is similar to many other PV inverters or motor drives. The research in this thesis is focus on characterizing the newly released 1200 V 100 A SiC MOSFET, evaluating its performance and comparing it with the same rating Si IGBT. It has been found that the SiC MOSFET based inverter efficiency will increase from 98% to 99% for 20 kHz switching frequency, and from 96.5% to 98.5% for 40 kHz switching frequency.

In summary, both the >13 kV and 1200 V SiC MOSFET has been fully characterized and studied, based on which the three stage SST has been designed and tested.

# Design, Development and Control of >13 kV Silicon-Carbide MOSFET based Solid State Transformer (SST)

by
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# DEDICATION

To my parents

Gongcheng Wang and Chengmiao Chu

# BIOGRAPHY

Gangyao Wang was born in Yuexi, Anhui province, China. He received his B.S. degree in electrical engineering from the Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2004. From 2005 to 2007, he was an Electrical Engineer with Delta Electronics Shanghai Design Center, Shanghai, China. Since 2007 he has been working toward the Ph.D. degree at the Future Renewable Electric Energy Delivery and Management (FREEDM) Systems Center, Department of Electrical and Computer Engineering, North Carolina State University, Raleigh. His research interests include power converter topology and control, solid-state transformer design, SiC power device characterization, modeling and application.

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# TABLE OF CONTENTS

# LIST OF TABLES

# LIST OF FIGURES

# CHAPTER 1

# Introduction

## 1.1 Introduction of SST Concept

The Solid State Transformer (SST) is one of the key elements in the Future Renewable Electric Energy Delivery and Management (FREEDM) Systems Figure 1.1. It acts as an energy router to enable active management of Distributed Renewable Energy Resources (DRER), Distributed Energy Storage Device (DESD) and loads, rather than a 60 Hz conventional transformer. The SST has the features of instantaneous voltage regulation, voltage sag compensation, fault isolation, power factor correction, harmonic isolation and DC output.[47, 6, 25].

In the SST the 60 Hz transformer is replaced by a high frequency transformer to provide isolation and step up/down function in addition to the power electronics

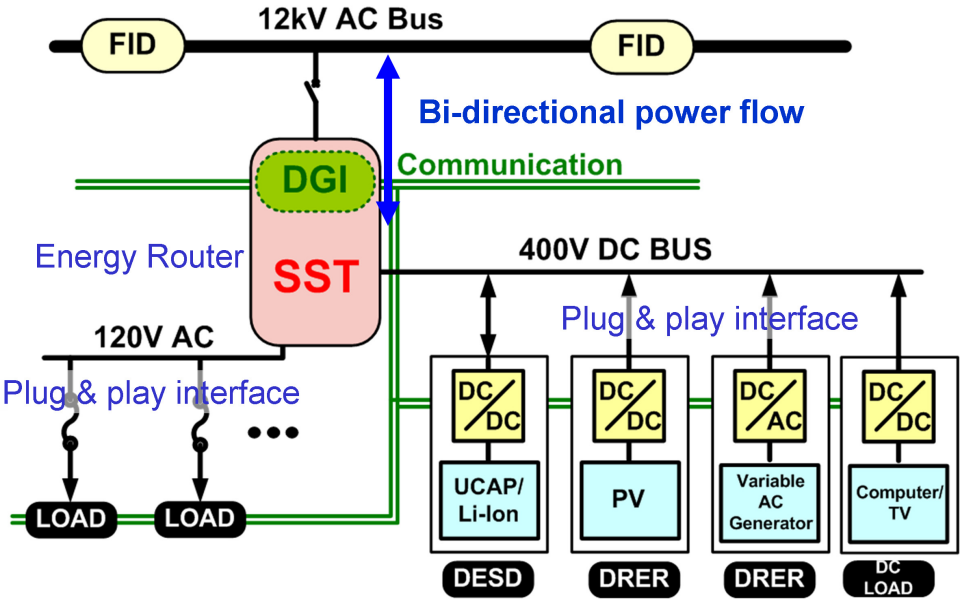



Figure 1.1: Role of Solid State Transformer (SST) under FREEDM Systems

converters, which are key to achieve size and weight reduction and the power quality improvement.

The SST will also have a 400 V DC port that will facilitate connection of the DRERs and DESDs. With the intelligent controller (Figure 1.2), each SST will have bi-directional energy flow control capability allowing it to control active and reactive power flow and manage to limit the fault currents on both the low voltage and high voltage sides. Its large control bandwidth provides the plug-and-play feature for distributed resources to rapidly identify and respond to changes in the system. With the integrated distributed grid intelligence(DGI) hardware platform, the SST can be monitored and controlled remotely through Ethernet.

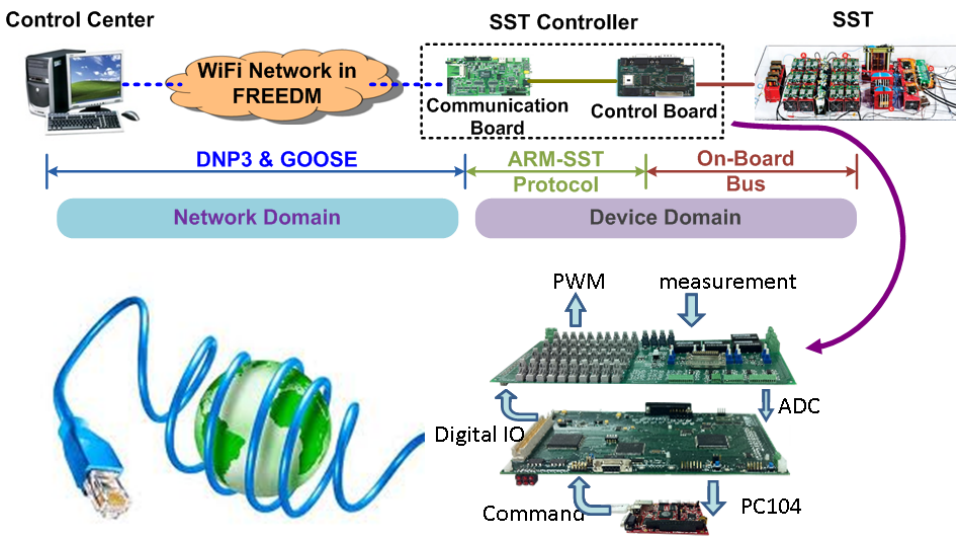



Figure 1.2: SST Enabled Energy Internet

## 1.2 Silicon IGBT based SST

The application of replacing 60 Hz transformer with high frequency power converters has been discussed in many publications [38, 58, 13, 27]. There are several project for developing the solid state transformer including UNIFLEX [8],EPRI IUT [32], GE solid substation [20]. In 2008, FREEDM System Center has started to develop the 6.5 kV IGBT based solid state transformer (Figure 1.3). It has been rated as single phase input voltage 7.2 kV, 60 Hz, output voltage 240/120 V, 60 Hz, 1 phase/3 wires. The SST consists of a cascaded high voltage high frequency AC/DC rectifier that converts 60 Hz, 7.2 kV AC to three 3.8 kV DC buses, three high voltage high frequency DC-DC converters that convert 3.8 kV to 400 V DC bus and a voltage source inverter (VSI) that inverts 400V DC to 60 Hz, 240/120 V, 1 phase/3 wires. The switching devices in high voltage H-bridge and low voltage H-bridges in (Figure 1.3) are 6.5 kV silicon IGBT and 600V silicon IGBT respectively. The switching frequency of the high voltage silicon

IGBT devices is 1080 Hz for the rectifier, and 3.6kHz for the DC/DC stage. The low voltage IGBT in the VSI switches at 10.8 kHz. The silicon IGBT based SST prototype is shown as (Figure 1.4). Due to the complexity of the topology, the control the silicon IGBT based SST is very challenging which has been discussed in [57, 41, 56, 42, 43, 46]

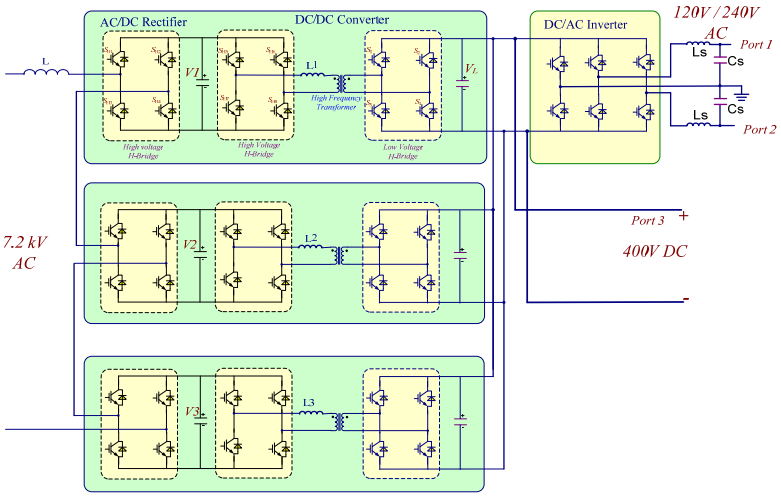



Figure 1.3: 6.5 kV IGBT based Solid State Transformer Topology

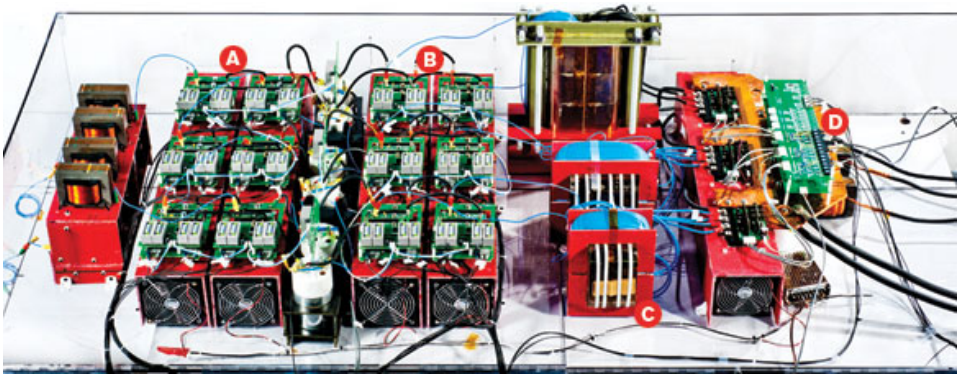



Figure 1.4: 6.5 kV IGBT based Solid State Transformer Prototype

## 1.3 SiC Power Device based SST

With a large quantity of power devices and three cascaded stages structure for the silicon IGBT based SST, it suffers from low efficiency and large size. With the development of 15 kV level SiC power MOSFET, the SST topology can be simplified as in Figure 1.5 while still provides the interface between the existing 12 kVac (7.2 kVac L-N) istribution system and 120/240 Vac utility voltage with an extra 400 Vdc bus. Due to SiC power MOSFET's low loss and high switching capability, the new SST will have reduced the size, weight and improved the efficiency. The 10A high voltage SiC MOSFET developed by Cree Inc. has a 150um epitaxial layer which is target for blocking 15kV. The prototype samples have been tested up to 13.5 kV, and it will be referred to as >13 kV MOSFET in this dissertation.

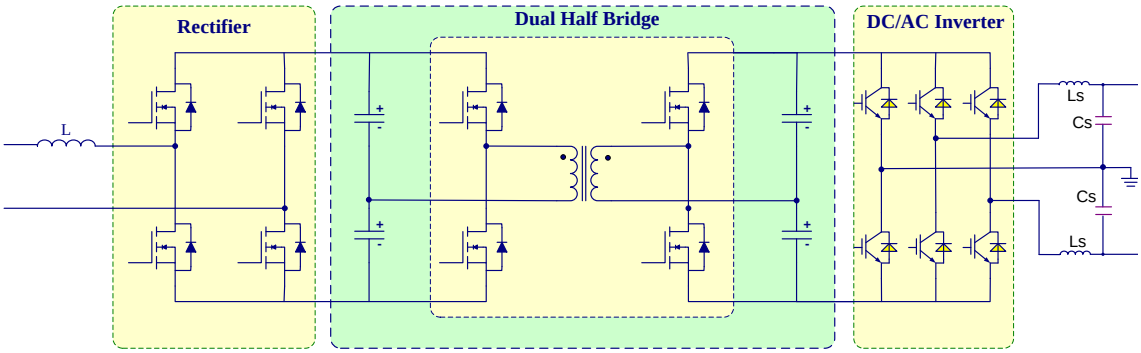
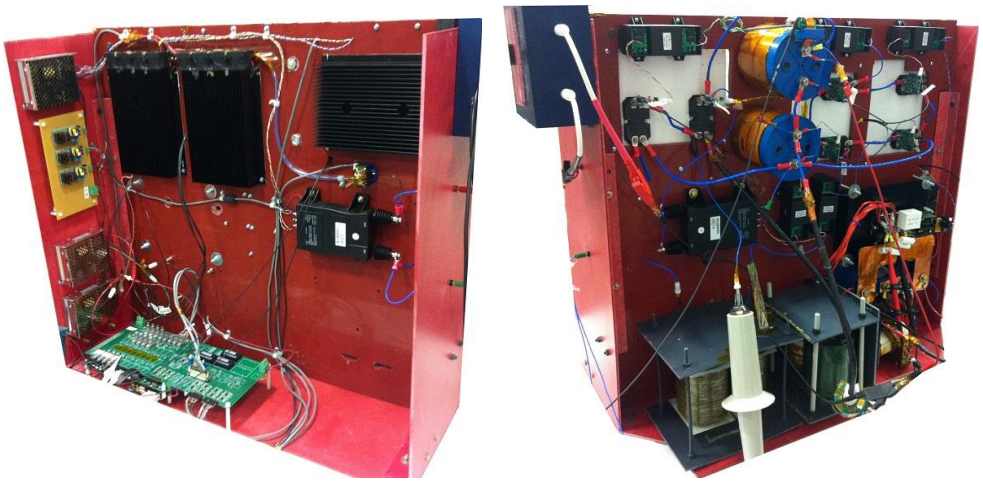



Figure 1.5: High Voltage SiC MOSFET based Solid State Transformer Topology

The main challenges for designing the high voltage SiC MOSFET based SST are: (a) The power device is new and its performance has not been fully characterized. High dv/dt generated during the switching transient may go up to 100 kV/us. For any 10 pF parasitic coupled capacitance, 1 A current will be generated. Small coupling

capacitance will make the system packaging very difficult as well as the auxiliary power supply design for the MOSFET gate drivers. (b) The high input voltage and insulation voltage for the high frequency transformer will generate high electric field, and cause partial discharge. The coupling capacitance must also be minimized because of the high dv/dt transient of the primary terminals.

The >13 kV SiC MOSFET based SST prototype has been developed as shown in Figure 1.6. With the limitation of the MOSFET blocking voltage, the high voltage DC bus has been conservatively chosen as 6 kV. The new designed SST ratings are 3.6 kVac input voltage, 6kV high voltage DC bus, 400 V low voltage DC bus and 240 Vac output with 10 kVA power rating.



(a) (b)

Figure 1.6: High Voltage SiC MOSFET based Solid State Transformer Prototype Front View (a) and Back View (b)

## 1.4 Outline of This Dissertation

Chapter 1 introduces the solid state transformer(SST) concept and described its function. The silicon IGBT based SST topology has been reviewed and the new proposed SST topology based on high voltage SiC power devices is presented.

In Chapter 2, the methodology for characterizing power devices has been discussed, followed by the characterization results of the >13 kV SiC MOSFET. It has been identified that MOSFET's parasitic capacitances play an important role in determining its switching loss. A MOSFET parasitic capacitance estimation method comprising of dynamic switching measurement and static measurement has been proposed. A PLECS loss model has been developed and verified by the a boost converter prototype experiment.

In Chapter 3, three different SPWM modulation methods for the full bridge rectifier has been reviewed and the bipolar single frequency SPWM method has been identified as the most suitable control algorithm for the >13 kV SiC MOSFET based rectifier. With such modulation method, the generated PWM voltage frequency equals to the switching frequency and each MOSFET equivalent switching frequency under hard switching conditions is only 1/4 of the PWM voltage frequency. The SST rectifier efficiency has been simulated and measured for 6 kHz and 12 kHz switching frequency with 6 kV dc bus voltage and 3.6 kV ac voltage, which is 99.2% for 6 kHz with 8.8 kW load and 98.5% for 12 kHz with 8.3 kW load.

In Chapter 4, The SST DC-DC stage has been designed which utilizes the dual active half bridge (DHB) as the topology. Its zero voltage switching (ZVS) turn on range has been analyzed and it is concluded that the dead-time and device parasitic capacitances will reduce the ZVS range while the magnetizing current will increase the ZVS range.

For achieving ZVS operation from no load to full load, variable frequency control has been proposed and the magnetizing inductance has been optimally designed. The DC-DC stage efficiency has been measured as 96.9% for 10 kHz switching frequency and 10 kW load, and the peak efficiency is 97.5% for 10 kHz switching frequency and 5 kW load.

In Chapter 5, The 1200 V 100 A SiC MOSFET module has been characterized and compared with the same rating silicon IGBT, the PLECS loss models has been developed for both of the devices.The inverter loss has been simulated and measured for different switching frequency and different load.

In chapter 6, conclusions are made and future work are listed.

# CHAPTER 2

# Characterization of the High Voltage Power Semiconductor Devices

## 2.1 Introduction

As the prerequisite for the SST circuit design, the electrical characteristics of the power devices have to be carefully studied. These characteristics include static performance like leakage current, forward conduction as well as dynamic performance like switching on and off. The high voltage SiC MOSFET is a new device with the state of the art technology. It can be switched much faster than the traditional Si IGBT. There some previous research on the 10kV SiC MOSFET [50, 51, 52, 53, 39, 40, 24, 21, 11] and 10kV SiC JBS [15, 49]. For the >13 kV SiC MOSFET its characteristics have never been fully studied and its application is seldom discussed. This chapter will first give a review of

power device general characterization approach, and then the performance of the >13 kV SiC MOSFET module will be studied in detail, and will be compared with the 6.5 kV Si IGBT. In the last part, a short comparison for different high voltage SiC devices will be given.

## 2.2 General Approaches for Power Device Characterization

### 2.2.1 Leakage Current Measurement

For power semiconductor device, static performance can be separate as DC characteristics and AC characteristics. DC characteristics include blocking capability (leakage current), output and transfer curve, on-state resistance which can all be measured by Tektronix 370 A or 371 A curve tracer. The AC characteristic mainly means nonlinear junction capacitances in this work which can be measured through LCR meter. Since these characteristics are all temperature dependent, multiple measurements have to be done under different temperature.

Since the maxim supply voltage for Tektronix 370 A curve tracer is 2 kV, the leakage current can not be measured for voltage higher than that. Typically, the leakage current is very small which makes it difficult to measure directly. The following circuit (Figure 2.1) measures voltage and then calculate the current, so it can be used for the leakage current measurement. $R2$ is the input impedance which is 10 MΩ for Fluke when doing voltage measurement, $R1$ is used for protection once the DUT

break down, the R1 value can be hundreds of MΩ which depends on the DUT voltage rating. The leakage current can be calculated by (Eq. 2.1), and at the time the DUT blocked voltage will be as in (Eq. 2.2)

$$I_{leakage} = V_{measured} / R_2 \tag{2.1}$$

$$V_{DUT} = V_{DC} - I_{leakage} \cdot (R_1 + R_2) \tag{2.2}$$

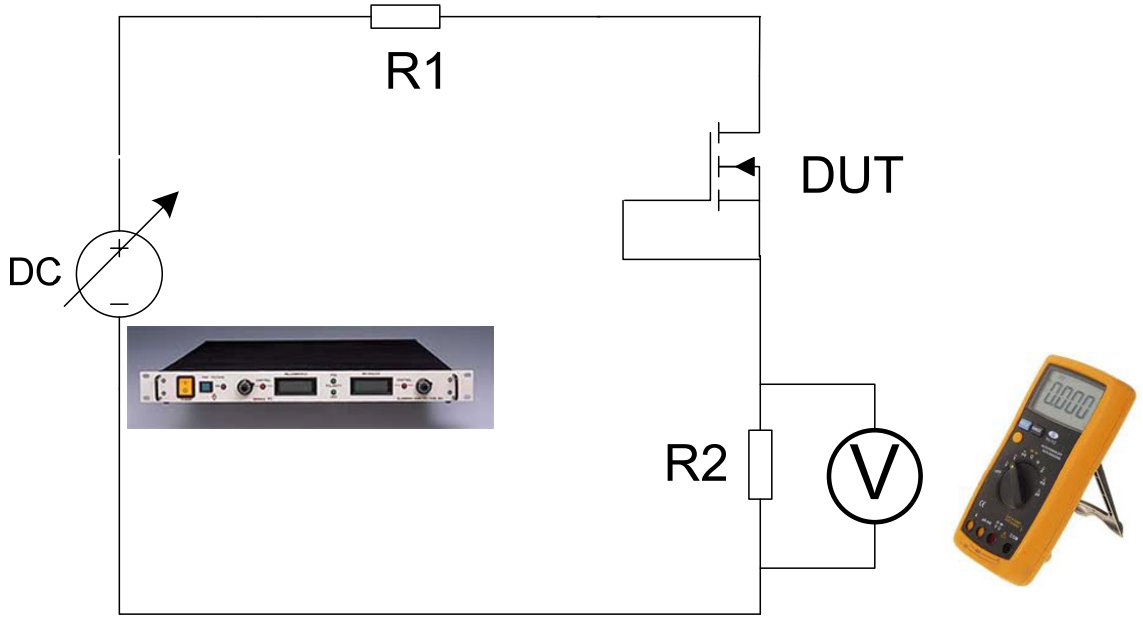



Figure 2.1: Circuit for High Voltage Power Device Leakage Current Measurement

### 2.2.2 Dynamic Switching Test

The power device switching characteristics can be tested by an inductive load double pulses tester shown as Figure 2.2[2, 9, 44], which includes a DC power supply, an inductor, a fly wheel diode, the device under test (MOSFET for example here) and the auxiliary circuit for providing gating signal.

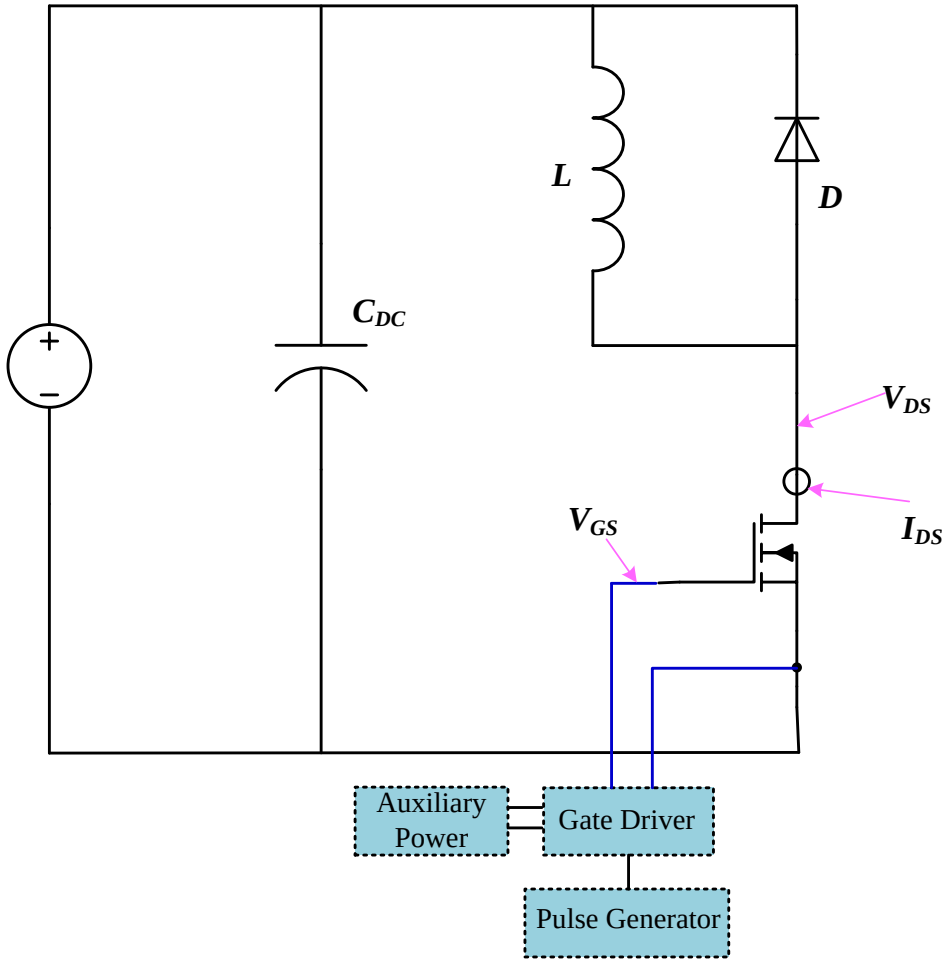



Figure 2.2: Double Pulses Tester

Figure 2.3 displays the typical double pulse waveform, during the first gating

pulse, the MOSFET drain source current will increase linearly since the power supply dc voltage is totally applied on the $L_1$. By controlling the pulse width, a pre-set drain current can be reached at the end of this pulse and the turn off transient can be captured at this moment. Right after the first pulse, the fly wheel diode $D_1$ will carry all the inductor current which will keep constant if ignoring wiring resistance. The turn on transient happens at the beginning second pulse, during which the current of diode $D_1$ will decrease to 0 A and become reverse biased, the MOSFET carries all the inductor current. With the variable DC voltage and first pulse width, the MOSFET can be switched under any desired voltage and current stress.

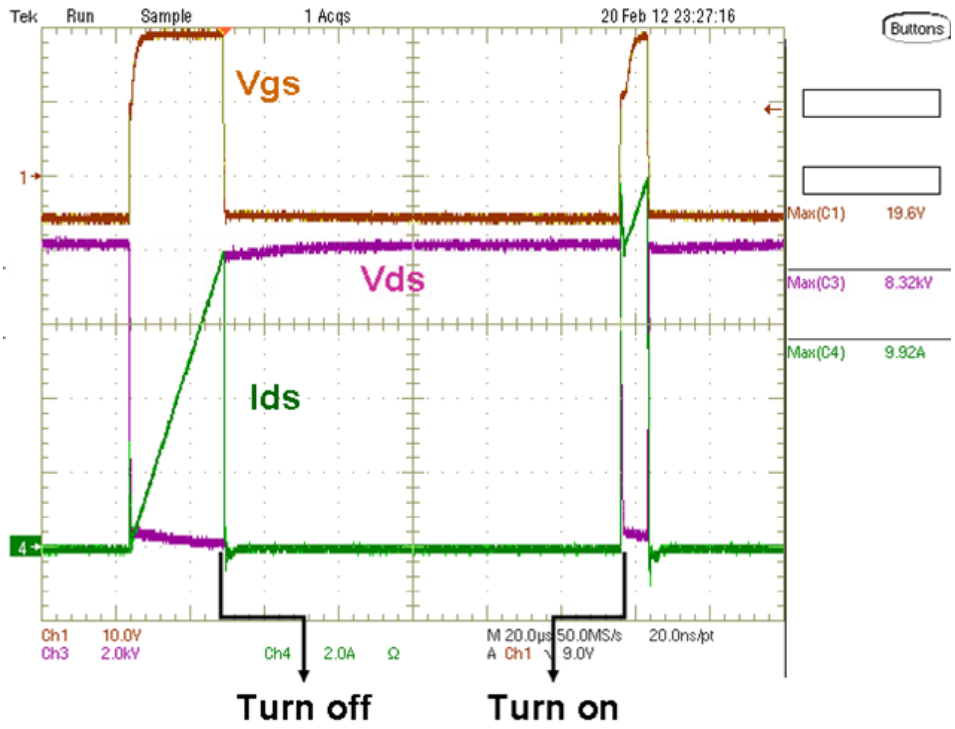



Figure 2.3: Double Pulses Test Typical Switching Waveforms

## 2.3 Characterization of 6.5 kV 25 A IGBT

### 2.3.1 Introduction

For the given 20 kVA rating, SST requires high voltage, low current and fast switching power devices. The commercial ABB 6.5 kV IGBT module is the best option but it has a 200 A minimum current rating. A 6.5 kV IGBT dual module with anti-parallel diode has been re-packaged by using ABB 6.5 kV 25 A IGBT chip and 6.5 kV 50 A diode chip.

Figure 2.4 shows the chips layout on DCB, it contains two 25 A IGBT chips and two 50 A diode chips. Figure 2.5 shows all module subassemblies. Figure 2.6 shows the final prototype, for this package design, the minimum clearance distance in air is 19mm and creepage distance is 78mm which complies with IEC-60077-1 standard.

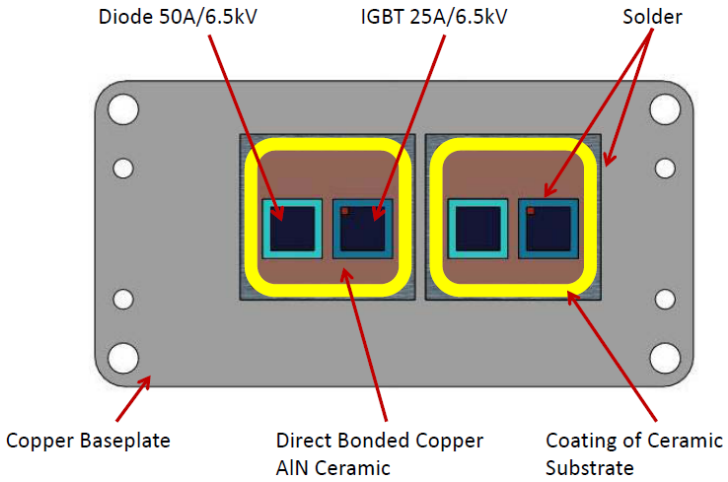



Figure 2.4: 6.5 kV 25 A IGBT Dual Module Layout

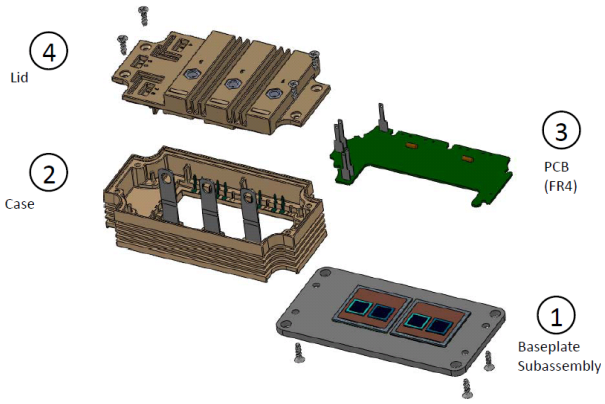



Figure 2.5: 6.5 kV 25 A IGBT Dual Module Sub-assemblies

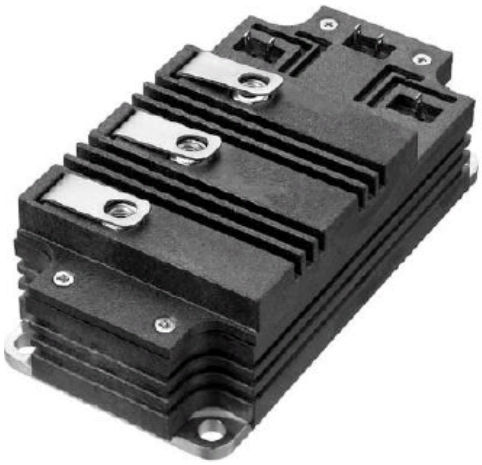


Figure 2.6: 6.5 kV 25 A IGBT Dual Module Prototype

### 2.3.2 Static Performance

The forward characteristics for IGBT and its parallel diode are plotted in Figure 2.7. The leakage current for IGBT is less than 4 mA and less than 6 mA for diode.

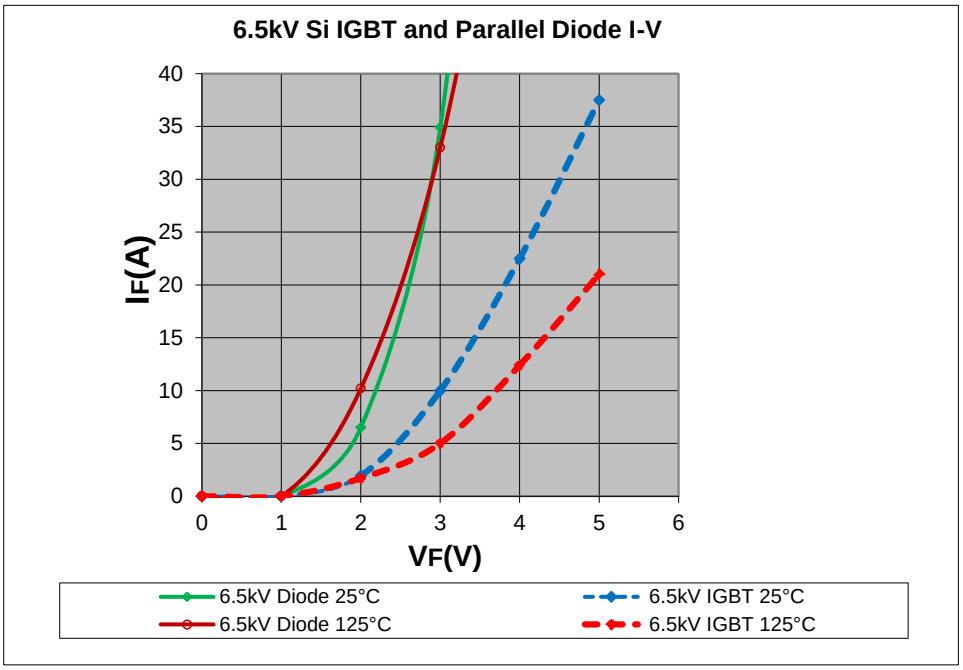



Figure 2.7: 6.5 kV 25 A IGBT and 6.5 kV 50 A Diode I-V Curve

### 2.3.3 Switching Performance

The switching characteristics of this low current IGBT module have been tested with 36 mH inductive load and 100 Ω gate resistor. Figure 2.8 gives the 10 A turn on waveform with 3.8 kV bus under 125 °C. The Turn on loss is 64.4 mJ.

Figure 2.9 shows the 5 A turn off waveform with 3 kV bus under 125 °C. The Turn off loss is 32.7 mJ.

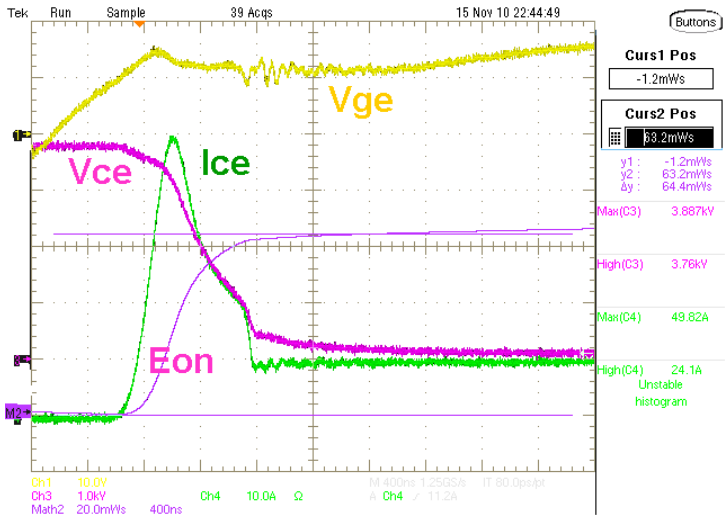



Figure 2.8: 6.5 kV 25 A IGBT 3.8 kV 10 A Turn on

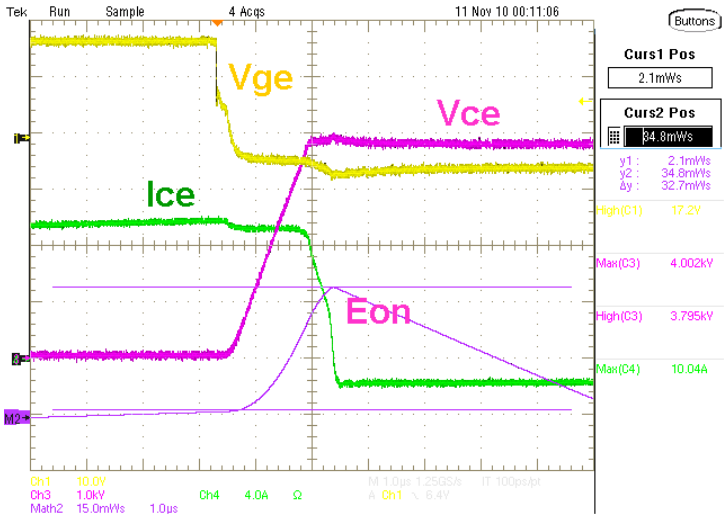



Figure 2.9: 6.5 kV 25 A IGBT 3.8 kV 10 A Turn off

The test results under different voltage, current and temperature conditions are plotted through Figure 2.12. Based on these test results, for 3800 V 5 A hard switching, the total switching loss for one device under 125 °C for 1 kHz will approximately be:

$$P_{loss} = (E_{on} + E_{off} + E_{rec}) \times f = (46.8mJ + 34.9mJ + 42.3mJ) \times 1000 = 123.9(W) \tag{2.3}$$

Compromising between the system efficiency, size and thermal management requirements, 1080 Hz has been chosen for the SST rectifier. For the DAB stage, 3 kHz has been chosen since it is capable of ZVS under rated load.

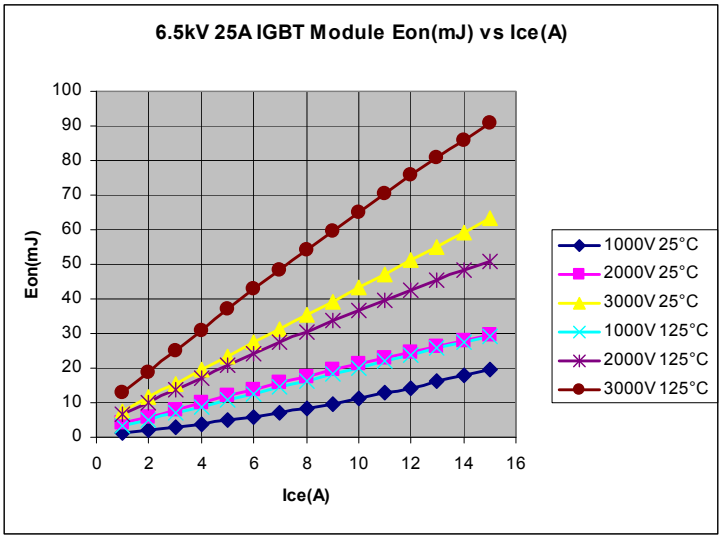



Figure 2.10: 6.5 kV 25 A IGBT $E_{on}$ (mJ) under Different Voltages and Currents

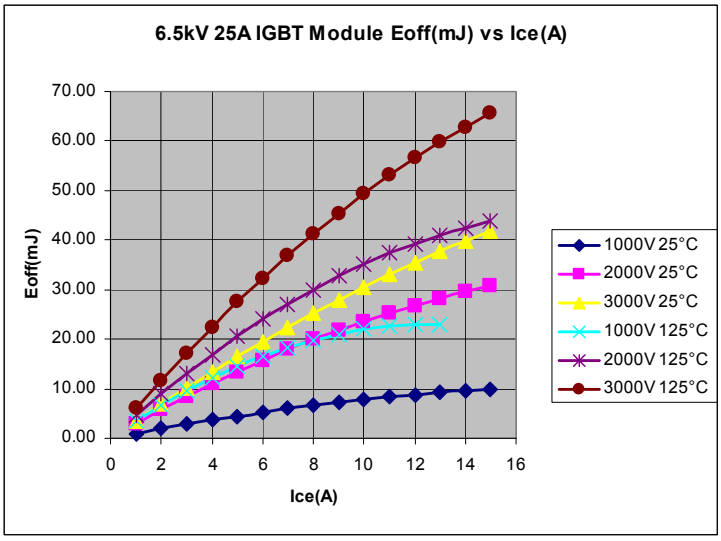



Figure 2.11: 6.5 kV 25 A IGBT $E_{off}$(mJ) under Different Voltages and Currents

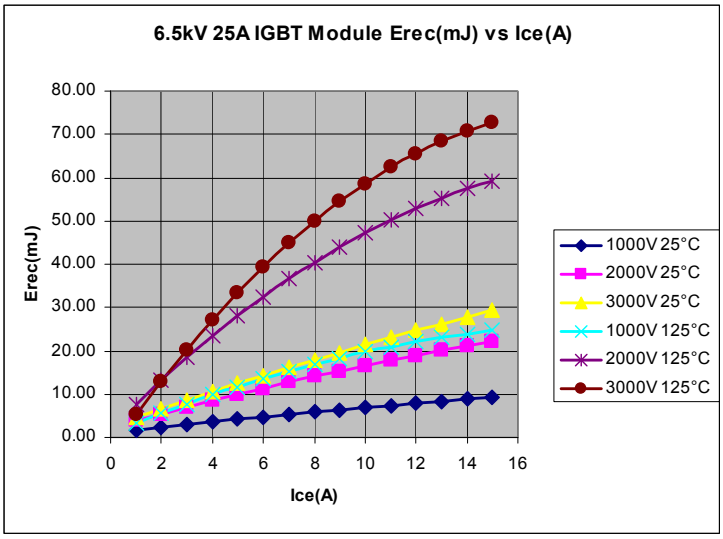



Figure 2.12: 6.5 kV 25 A IGBT Module Parallel Diode $E_{rec}$(mJ) under Different Voltages and Currents

## 2.4 IGBT Gate Driver Design Consideration

A half bridge formed by two IGBT modules is widely used for switch characterization. As Figure 2.13 shows, when switch $S_2$ turns on, the diode $D_1$ will change from forward conduction to reverse biased, and the reverse recovery current will be observed.

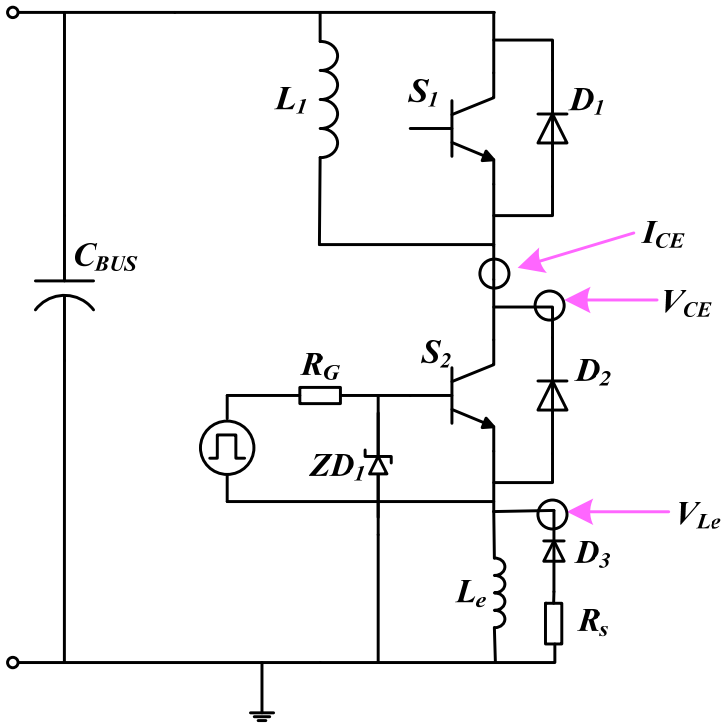



Figure 2.13: IGBT Switching Test Circuit

Then turn on transient can be divided into five phases as shown in Figure 2.14:

$[t_0, t_1]$: $V_ge$ increase from 0 V to the IGBT threshold voltage; $[t_1, t_2]$: IGBT start to conduct and the load current transferred from $D_1$ to $S_2$; $[t_2, t_3]$: Due to the reverse recovery of $D_1$, this reverse recovery current will be added to the load current and pass through IGBT $S_2$; $[t_3, t_4]$: $V_{ce2}$ decreases near to 0 V, and $V_{ce1}$ increases to $V_{bus}$ $[t_4,$

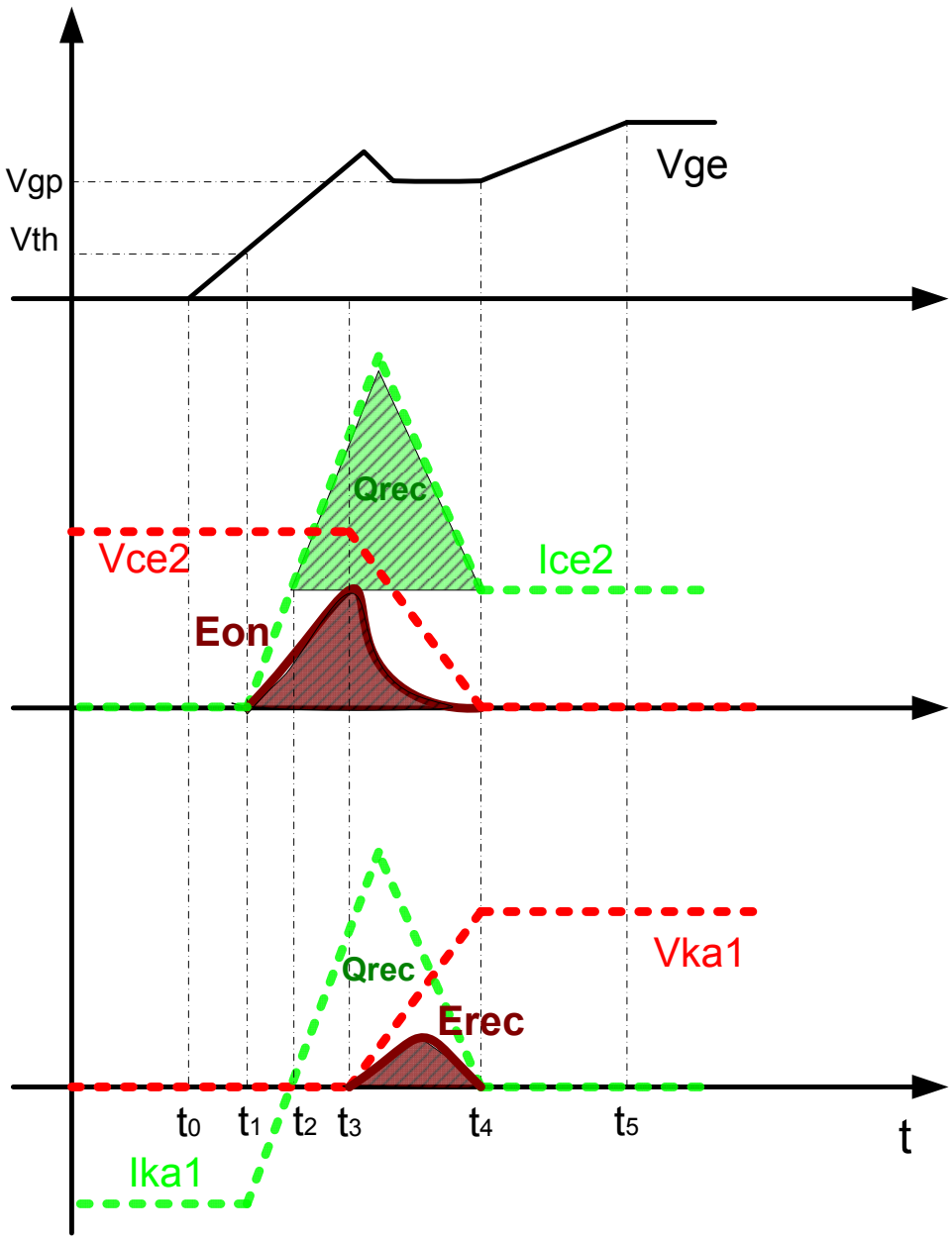



Figure 2.14: IGBT Turn On Process

$t_5$]: $V_{ge}$ increase until the preset $V_{ge}$ high voltage When considering the total loss of the $S_1$ turn on loss and $D_1$ recovery loss, it can be estimated as (Eq. 2.4):

$$Eon + Erec \approx Qrr \cdot Vce + \frac{3}{2}\frac{Vce \cdot Ice^2}{(di/dt)} + \frac{1}{2}\frac{Vce^2 \cdot Ice}{(dv/dt)} \tag{2.4}$$

According to the above equation, the loss can be reduced by increasing either $di/dt$ or $dv/dt$ , which both can be achieved via reduce $R_g$ value. However, due to the EMI consideration, in many cases a low $di/dt$ is preferred but high $dv/dt$ is acceptable. In other words, $di/dt$ has to be reduced and $dv/dt$ can be increased for the loss minimization purpose. A circuit has been proposed as in Figure 2.13, An extra inductor has been put in series with the IGBT emitter, when there is a positive $di/dt$ the inductor induced voltage will pull out current from the IGBT gate which will reduce $V_{ge}$, consequently decrease $di/dt$.

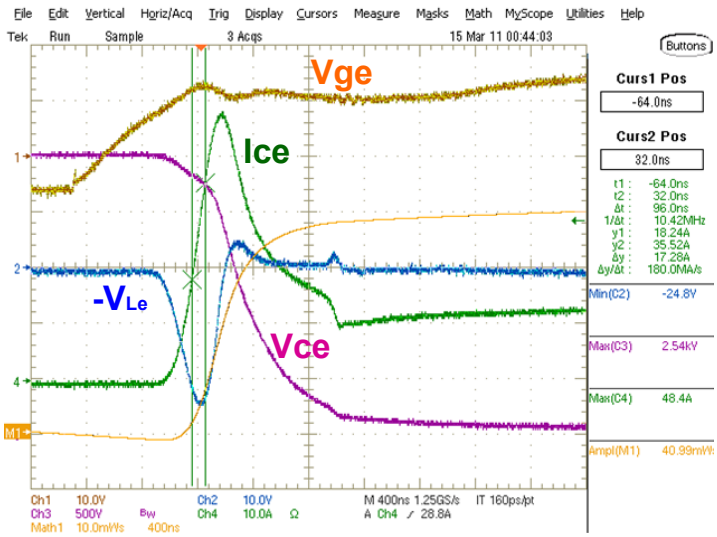



Figure 2.15: IGBT Turn On ($R_g$=100 ohm, $L_e$=100 nH, without Zener)

Figure 2.15 gives the turn on waveform when disconnect the $ZD_1$, the $L_e$ voltage is proportional to the $I_{ce}$ slope.

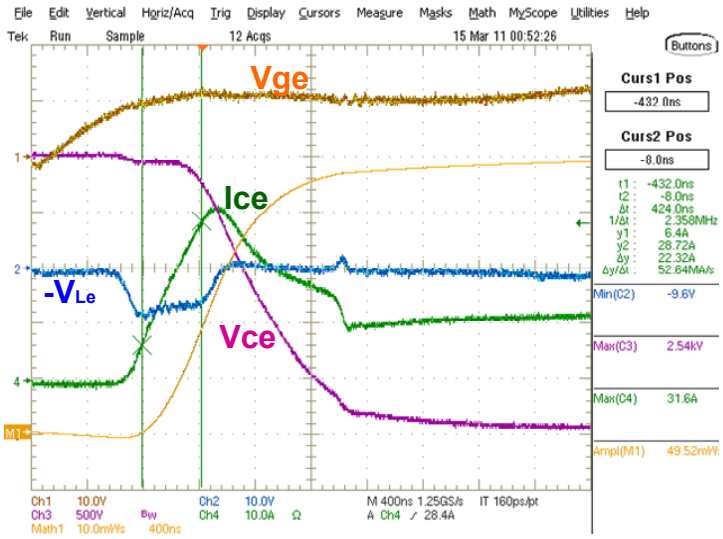



Figure 2.16: IGBT Turn On ($R_g$=100 ohm, $L_e$=100 nH, with Zener)

Figure 2.16 gives the turn on waveform when connect the $ZD_1$, the $di/dt$ has been reduced from 180 A/us to 52.6 A/us compared with Figure 2.15.

Figure 2.17 gives the turn on waveform when change Rg from 100Ω to 10Ω, the $di/dt$ is about the same as Figure 2.16, but $dv/dt$ has increased about two times, and the loss decreased to 37.1 mJ from 49.5 mJ.

Based on above analysis, IGBT turn on transient speed is dependent on the gating voltage and current, for the IGBT turn off transient speed, it is determined by the IGBT itself. The turn off transient can be divided as voltage increase phase and current falling phase, there time periods are given by equation Eq. 2.5 and Eq. 2.6

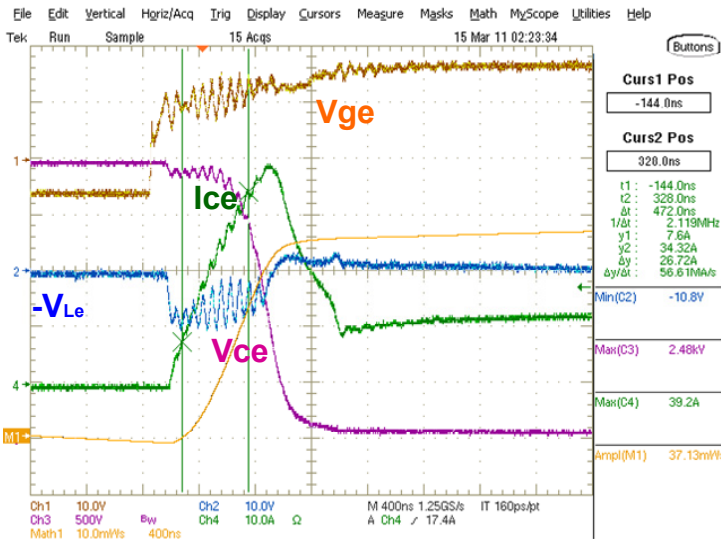



Figure 2.17: IGBT Turn On ($R_g$=10 ohm, $L_e$=100 nH, with Zener)

$$t_{V,OFF} = \frac{\varepsilon_s \cdot p_{WNB+} \cdot V_{CS}}{W_N \cdot (N_D + p_{SC}) \cdot J_{C,ON}} \tag{2.5}$$

$$\tau_{I,OFF} = \tau_{P0,NB} \cdot \ln(10) = 2.3\tau_{P0,NB} \tag{2.6}$$

The test waveforms in Figure 2.18 and Figure 2.19 prove the $R_g$ has little impact on the IGBT turn off speed.

In conclusion, the 6.5 kV silicon IGBT turn on loss can be reduced by proper design of the gate driver while the turn off loss is determined by the IGBT internal parameters.

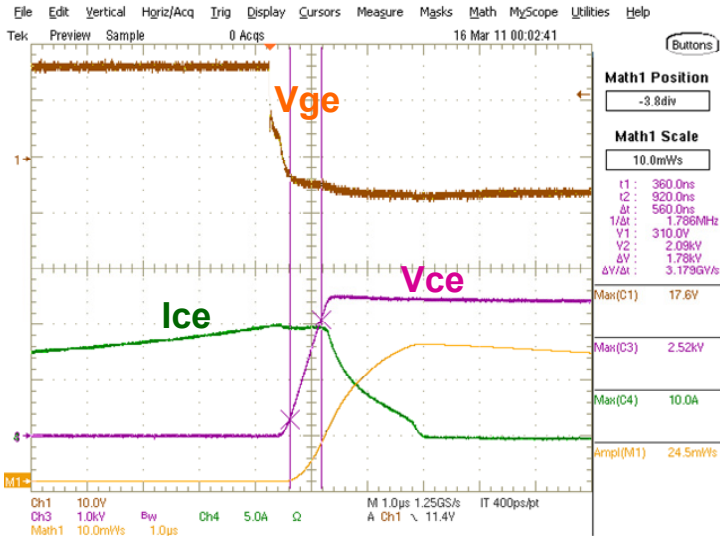



Figure 2.18: IGBT Turn Off ($R_g$=10 ohm, $dv/dt$=3.18 kV/us, $E_{on}$=24.5 mJ)

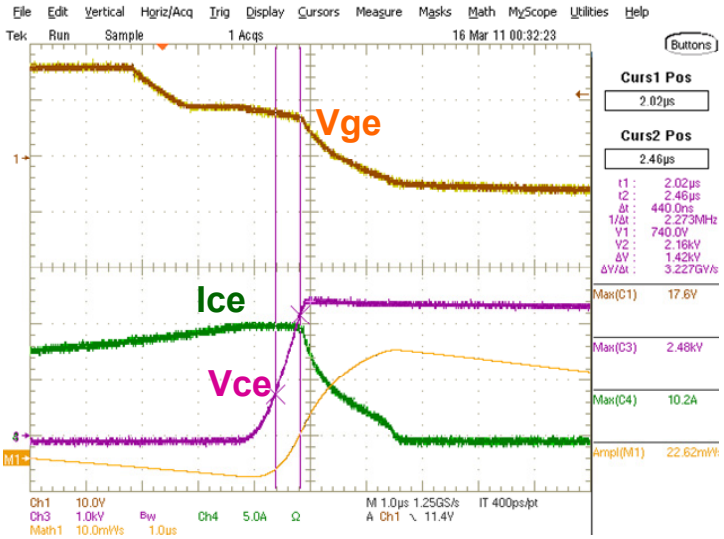



Figure 2.19: IGBT Turn Off ($R_g$=220 ohm, $dv/dt$=3.23 kV/us, $E_{on}$=22.6 mJ)

## 2.5 Characterization and Modeling of 13 kV 10 A SiC MOSFET

### 2.5.1 Introduction

The >13 kV SiC MOSFET and JBS developed by Cree Inc. has a 150um n-type SiC epilayer as the drift layer to support the high voltage as shown in Figure 2.20. The designed voltage blocking capability is higher than 15 kV, but the blocking voltage has only been tested up to 13.5 kV with 20 uA leakage current (Figure 2.22) for the safety concern. The MOSFET has a die size of $8.1mm \times 8.1mm$, and the JBS has a die size of $8.1mm \times 10.0mm$.

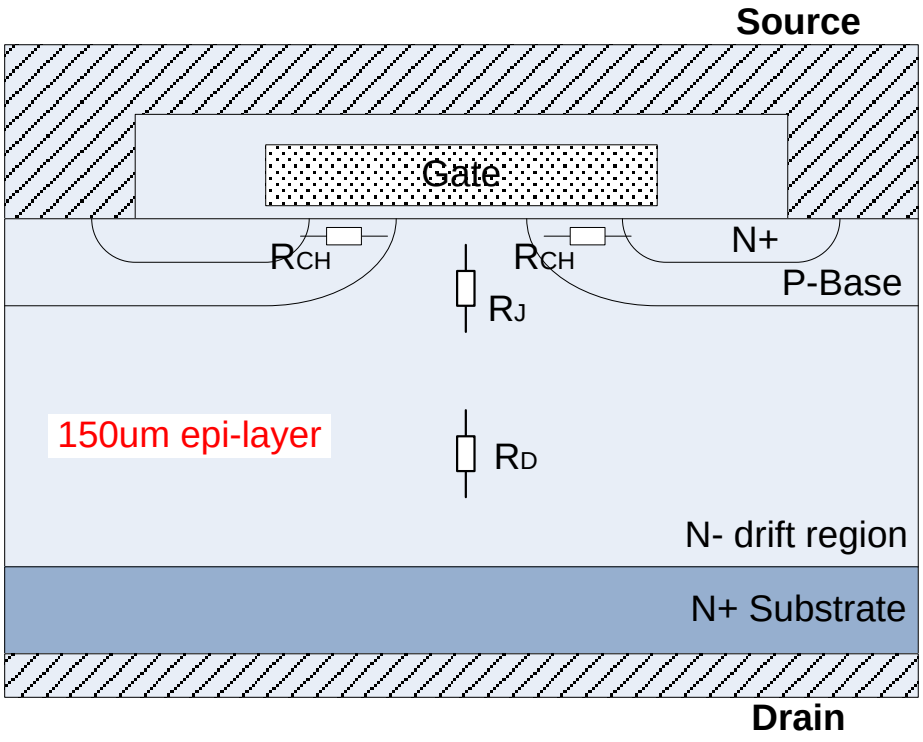
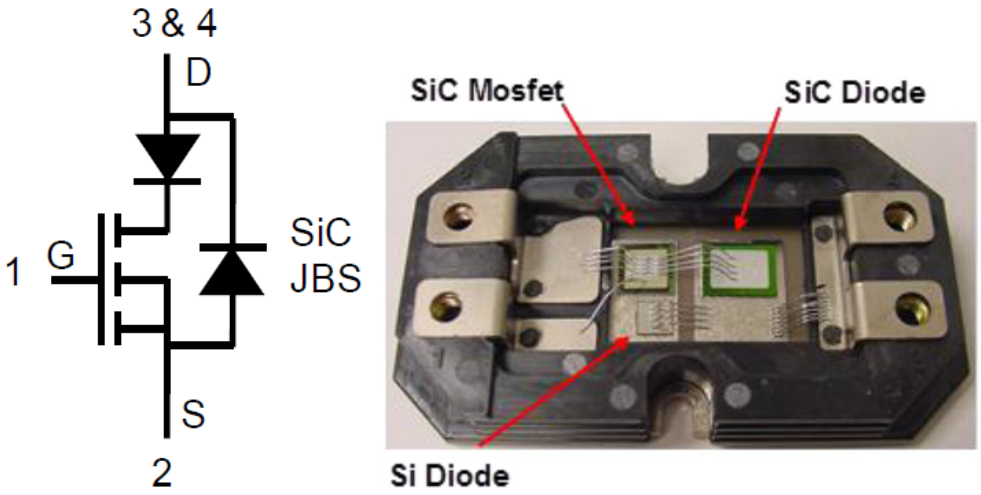



Figure 2.20: Simplified >13 kV SiC MOSFET Cross Section

One MOSFET chip and one JBS chip has been packaged together as a module. Because of the poor performance of the MOSFET body diode, a silicon diode has been put in series with the MOSFET in order to block the conduction of the SiC MOSFET body diode. Fig shows the schematic and package layout. The final module has a size of $80mm \times 43mm \times 15.8mm$.




(a) (b)

Figure 2.21: >13 kV SiC 10 A MOSFET Module Schematic and Prototype

### 2.5.2 Static Characteristics

The blocking characteristics of the >13 kV MOSFET as in Figure 2.22, measured at room temperature with 0 V gate bias, shows that the leakage current is only 20 uA at 13.5 kV blocking voltage.

The typical on-state characteristics of the >13 kV SiC MOSFET measured for different temperatures and different gate voltages is shown in Figure 2.23. With 20 V

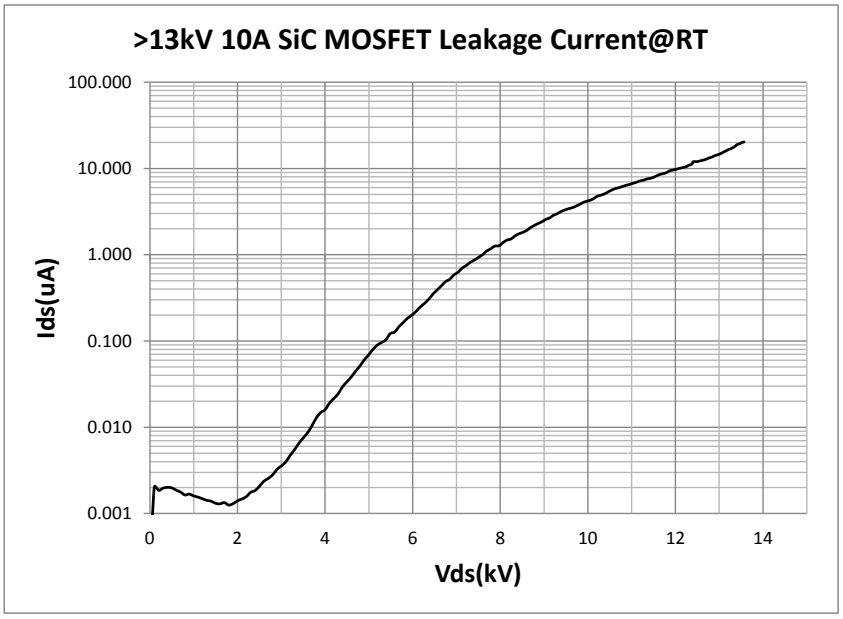



Figure 2.22: >13 kV SiC 10 A MOSFET Module Leakage Current

gate bias, the $R_{ds}(on)$ is 0.55 Ω at 25 °C and 1.7 Ω at 125 °C . It is can be found that forward on resistance is highly dependent on the gate bias for low temperature and almost keeps constant for high temperature with different gate bias.

The MOSFET on-resistance mainly contains three parts: channel resistance ($R_{ch}$), JFET region resistance ($R_{JFET}$), and drift region resistance ($R_d$). The channel resistance is determined by the gate bias and has a negative temperature coefficient (PTC), the JFET and drift region resistances will not be affected by the gate bias and both have a negative temperature coefficient (NTC). Unlike the 1200 V SiC MOSFET, >13 kV MOSFET has a very thick drift layer, the drift region resistance dominant within the total loss. Especially for the higher temperature, the channel resistance will reduce and the JFET and drift region resistance will increase, the channel resistance variance caused by gate bias will make little impact on the total on-resistance. For the power circuit applications, the MOSFET junction temperature normally around 125 °C during

operation, the conduction loss will not be reduced by having a higher gate driver voltage for the >13 kV SiC MOSFET. However, for the 1200 V MOSFET, it is suggested to apply 20 V gate bias for minimizing conduction loss.

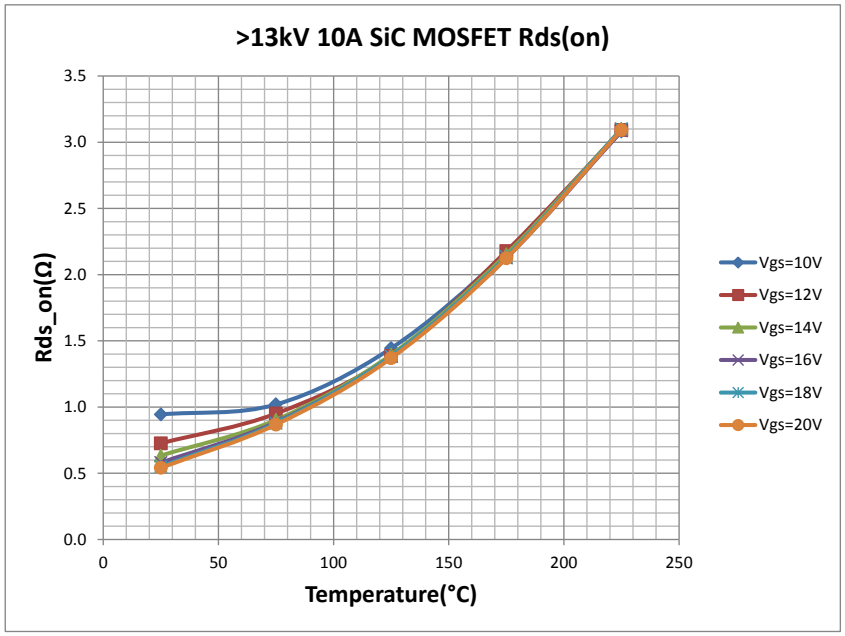



Figure 2.23: >13 kV SiC 10 A MOSFET V-I Curves

On the other hand, the gate bias voltage will determine the MOSFET saturation current, the higher gate bias voltage will have high saturation current as shown in Figure 2.24. The MOSFET short circuit capability is typically thermally limited, and the energy dissipated in the MOSFET is [26]:

$$E_{sc} = \int_{t_1}^{t_1+t_{sc}} V_{sc} \cdot I_{sc} \cdot dt \tag{2.7}$$

The MOSFET short circuit voltage usually will be the DC bus voltage. With same short circuit energy limit, the short circuit time can be longer if the short circuit current

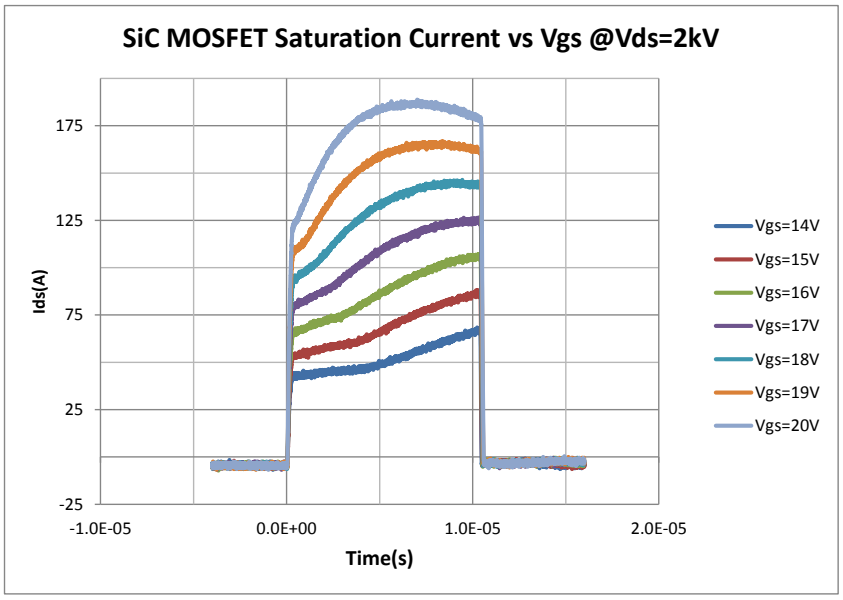



Figure 2.24: SiC MOSFET Saturation Current vs Gate Voltage

is lower. From protection point of view, a lower gate voltage bias will give a longer short circuit protection time and ease the protection circuit design.

The typical forward characteristics of the paralleled >13kV SiC JBS diode measured for different temperatures is shown in Figure 2.25, the device forward voltage at the rated current of 10 A is 5.2 V under 25 °C and 11 V under 125 °C. The I-V curve can be simply described as the Eq. 2.8 for 25 °C and Eq. 2.9 for 125 °C

$$V_F = 0.43 \times I_F + 0.95 \tag{2.8}$$

$$V_F = 1.025 \times I_F + 0.75 \tag{2.9}$$

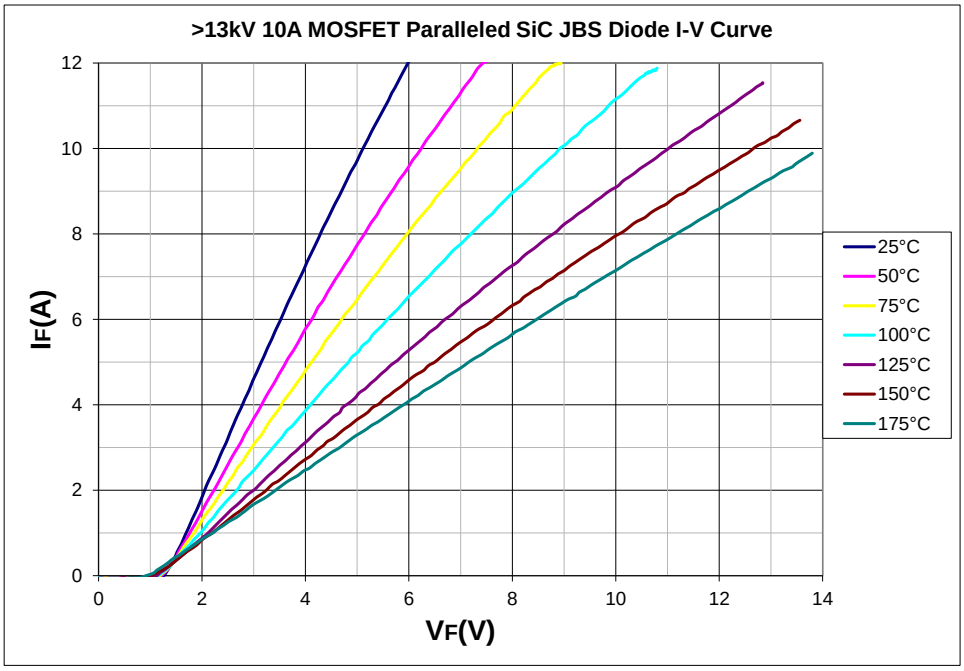



Figure 2.25: >13 kV SiC 10 A JBS Diode I-V Curves for Different Temperature

### 2.5.3 Switching Transient and Loss analysis

For the low voltage silicon MOSFET, its switching process under clamped inductive load has been analyzed in many publications [37, 54], since the energy stored by the low voltage MOSFET junction capacitor is negligible, and the current used to charge or discharge the output capacitor is small enough compared with the load current, so the MOSFET channel current can be consider approximately equal to its drain current when analyzing the switching transient. The MOSFET switching transient can be separated into four different phases for both turn on and turn off as shown in Figure 2.26

The four phases for turn on are: Phase I [$t_0$, $t_1$]: At $t_0$, the gate driver starts to charge the $C_{gs}$ and $C_{gd}$ , the MOSFET will not turn on until $t_1$ when the $V_{gs}$ reaches the threshold voltage $V_{th}$. Phase II [$t_1$, $t_2$]: At $t_1$, the MOSFET starts to turn on, drain

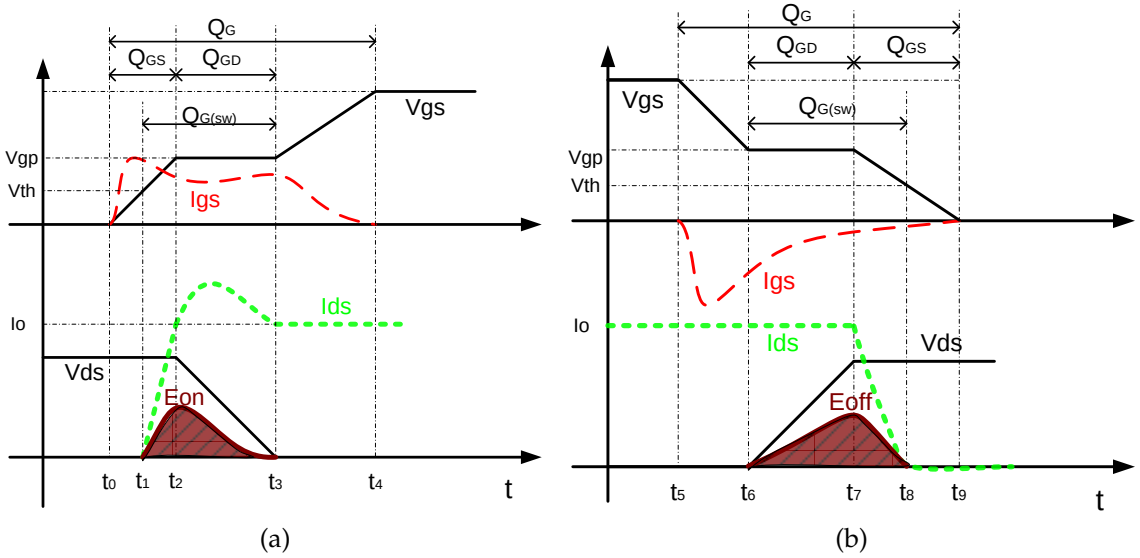



Figure 2.26: Si MOSFET Turn on and Turn off

current increases; the load current transfers from the free-wheel diode to the MOSFET, this process will finish at $t_2$ when all load current has been transferred. During this stage: $I_{ds} = g_m(V_{gs} - V_{th})$

Phase III [$t_2$, $t_3$]: At $t_2$, the MOSFET drain current has reached the inductive load current, $V_{ds}$ starts to decrease, the gate source voltage shows the miller plateau which is $V_{gs} = I_{ds}/g_m + V_{th}$, and the gate current determines the $dv/dt$ slope of the $V_{ds}$ , this phase will be ended at $t_3$ when $V_{ds}$ reached 0V Phase IV [$t_3$, $t_4$]: At $t_3$, the MOSFET has been fully turned on, with continuously increasing the $V_{ds}$ , the channel resistance can be further reduced, and finally $V_{gs}$ will be equal to the gate driver high output voltage. The total turn on loss will be:

$$E_{on} = \frac{1}{2} \cdot V_{in} \cdot I_{in} \cdot (t_{2\_1} + t_{3\_2}) \approx \frac{1}{2} \cdot V_{in} \cdot I_{in} \cdot \frac{Q_{SW}}{I_{G(L-H)}} \tag{2.10}$$

The four phases for turn off are identical as the turn on, the turn off loss can be

calculated as:

$$E_{off} = \frac{1}{2} \cdot V_{in} \cdot I_{in} \cdot (t_{7\_6} + t_{8\_7}) \approx \frac{1}{2} \cdot V_{in} \cdot I_{in} \cdot \frac{Q_{SW}}{I_{G(H-L)}} \tag{2.11}$$

The total switching loss:

$$E_{sw} = E_{off} + E_{off} \approx \frac{1}{2} \cdot V_{in} \cdot I_{in} \cdot (\frac{Q_{SW}}{I_{G(L-H)}} + \frac{Q_{SW}}{I_{G(H-L)}}) \tag{2.12}$$

However, for the high voltage low current SiC MOSFET, the parasitic capacitors store a significant amount of energy, and the required current used to charge or discharge the output capacitance is comparable to the drain current, the previous analysis method will become invalid for estimation switching loss. The MOSFET parasitic capacitances can be represented by three equivalent capacitors $C_{gs}$, $C_{gd}$ ,$C_{ds}$ and

$$C_{iss} = C_{gs} + C_{gd} \tag{2.13}$$

$$C_{rss} = C_{gd} \tag{2.14}$$

$$C_{oss} = C_{ds} + C_{gd} \tag{2.15}$$

For the high voltage SiC power devices, $C_{oss}$ will contribute a large portion of the switching loss because a large amount of energy has been stored by $C_{oss}$.

The turn on process shown in Figure 2.27 is similar as the previous case which ignores junction capacitances, the only difference is in phase III,

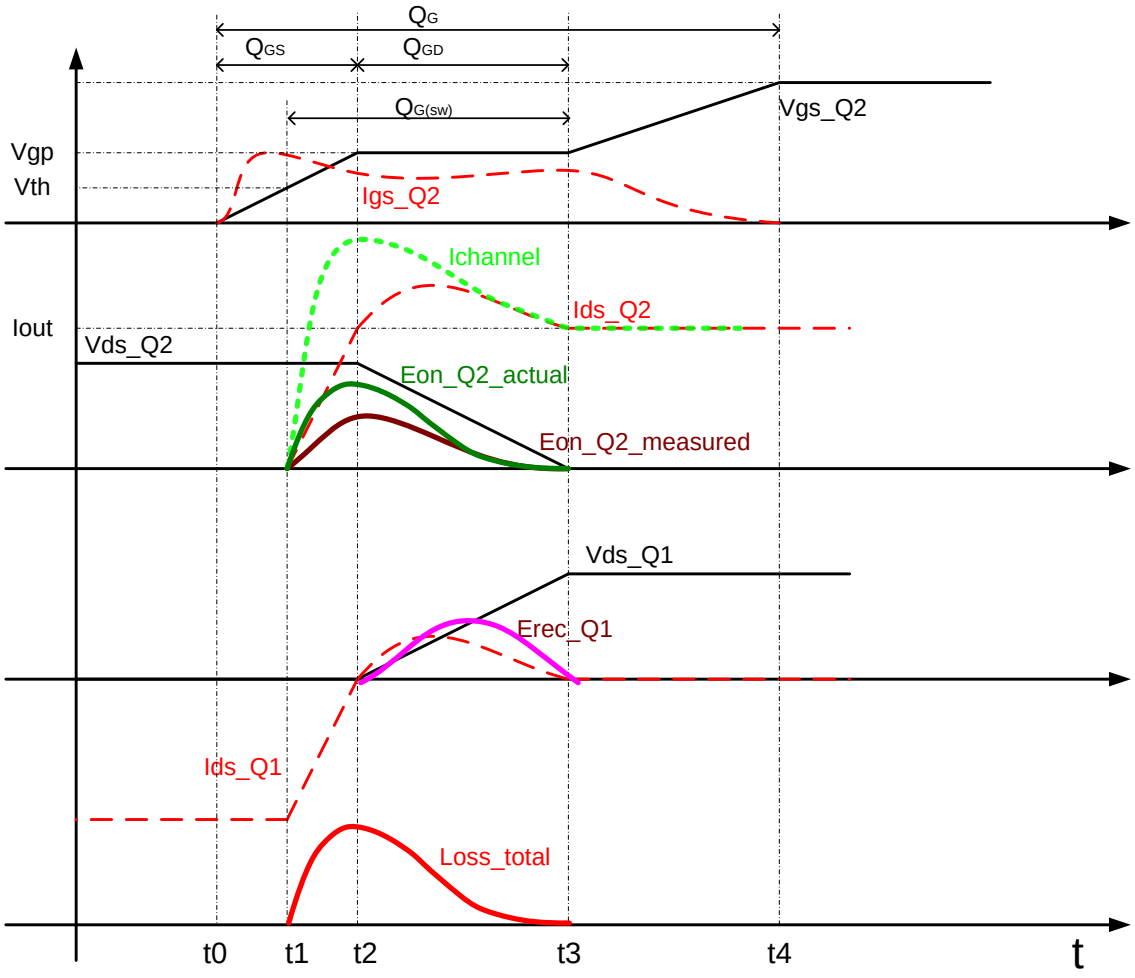
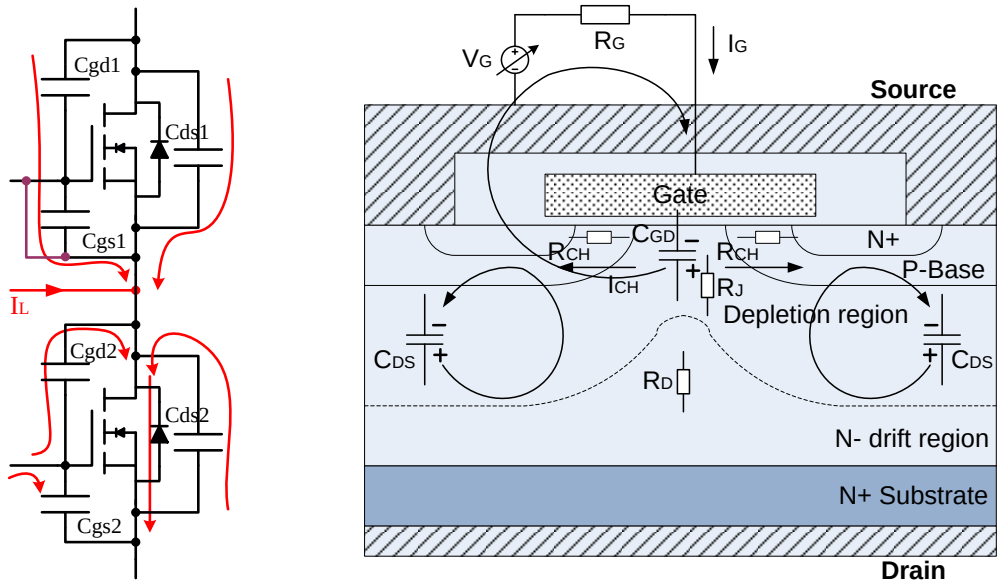



Figure 2.27: MOSFET Turn on Process

During Phase III, $V_{ds}$ drops from $V_{in}$ to 0 V, which means $C_{gd2}$, $CC_{ds2}$ is charging, However the $C_{gd2}$ and $CC_{ds2}$ discharging current will be inside the MOSFET as shown in Figure 2.28 and cannot be measured through the drain or source terminal. This part of capacitive energy loss will not be counted in the measured turn on loss.




(a) (b)

Figure 2.28: MOSFET Internal Parasitic Capacitance Discharging During Turn on

When considering a half bridge configuration of the SiC MOSFET module, the top module output capacitor

$$C_{oss1} = C_{ds1} + C_{gd1} \tag{2.16}$$

the bottom module output capacitor

$$C_{oss2} = C_{ds2} + C_{gd2} \tag{2.17}$$

$$C_{oss1} = C_{oss2} \tag{2.18}$$

Let us first consider the output capacitor related losses, it is well known that the energy stored in a linear capacitor is $E_{cap}(V) = \frac{1}{2}C \cdot V^2$ and charge $Q = C * V$, for an $RC$ circuit as in Figure 2.29(a), the energy dissipated on the resistor equals to the energy stored in the capacitor during the charging. But the MOSFET output capacitance is nonlinear and has strong bias voltage dependency. If considering the nonlinear case as shown in Figure 2.29(b),

$$C(V) = \frac{1}{\sqrt{V}} \tag{2.19}$$

Capacitor stored charge,

$$Q(V) = \int_0^V C(v)dv = \int_0^V \frac{1}{\sqrt{v}}dv = 2\sqrt{V} \tag{2.20}$$

Capacitor stored energy:

$$\begin{aligned} E_{cap}(V) = & \int_0^V V(Q)dq = V \cdot Q(V) - \int_0^V Q(v)dv \\ & = V \cdot (2\sqrt{V}) - (\frac{4}{3}V^{3}\!/2) = \frac{2}{3}V^{3}\!/2 = \frac{2}{3}[C(V)]^{-3} \end{aligned} \tag{2.21}$$

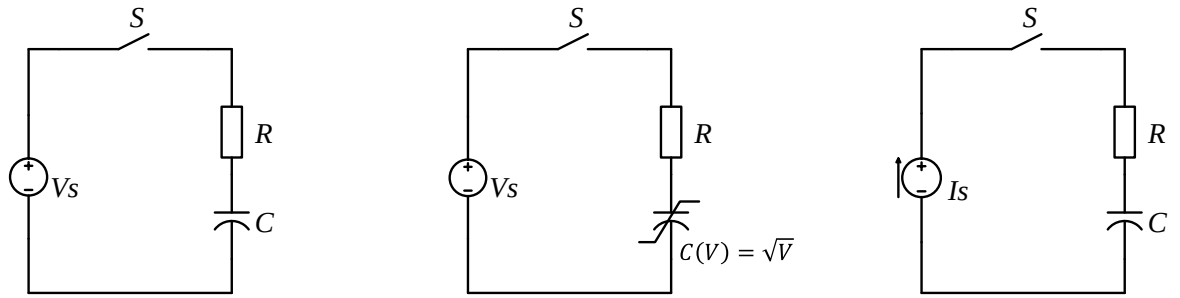
Total energy supplied by the source:

$$E_s(V) = V \cdot Q(V) \tag{2.22}$$

The energy dissipated by R will be:

$$E_R(V) = E_s(V) - E_{cap}(V) = V \cdot Q(V) - \frac{2}{3}V^{3/2} = \frac{4}{3}V^{3/2} = \frac{4}{3}[C(V)]^{-3} \tag{2.23}$$

It can found from the above equations that the energy dissipated on the resistor is two times of the energy stored in the capacitor during the charging process.




(a) (b) (c)

Figure 2.29: RC Charging Circuit

If using a current source to charge a capacitor (Figure 2.29(c)), then

$$V = \frac{I}{C} \cdot t \tag{2.24}$$

$$E_{cap}(V) = V \cdot Q(V) = (\frac{I}{C} \cdot t) \cdot (I \cdot t) = \frac{1}{C} \cdot (I \cdot t)^2 = \frac{1}{2} \cdot C \cdot V^2 \tag{2.25}$$

$$E_R(V) = I^2 \cdot R \cdot t \tag{2.26}$$

According to the above analysis, when a capacitor is charged by a voltage source,

the energy loss will be independent of the charging current, and the amount of the loss will be $V \cdot Q(V) - E(V)$, but if the capacitor is charged by a current source, the energy loss will be determined by the charging current and the series resistance.

So the above turn on loss can be separated into three parts:1) switching loss without considering $C_{oss}$ which is $V \cdot Q(V) - E(V)$, 2) the stored energy $E_{oss2}$ by $C_{oss2}$ 3) the extra current for charging $C_{oss1}$ caused loss which can be calculated as $Q_{oss1} \cdot V_{in} - E_{oss1}$

Since $E_{oss1} = E_{oss2}$, The total turn on loss will be:

$$E_{on} = \frac{1}{2} \cdot V_{in} \cdot I_{in} \cdot \frac{Q_{SW}}{I_{G(L-H)}} + Q_{oss} \cdot V_{in} \tag{2.27}$$

While the measured turn on loss will only be:

$$E_{on(measured)} = \frac{1}{2} \cdot V_{in} \cdot I_{in} \cdot \frac{Q_{SW}}{I_{G(L-H)}} + Q_{oss} \cdot V_{in} - E_{oss} \tag{2.28}$$

From the above equation, we can find the turn on loss is highly independent on the gate driver current, smaller gate resistor will have larger drive current and higher miller plateau as shown in Figure 2.30 which gives the $V_{gs}$ waveforms for a gate resistor of 10Ω, 22Ω, 56Ω so as the turn on speed shown in Figure 2.31

The measure turn on loss for 6 kV $V_{ds}$ are plotted in Figure 2.32 which shows the turn on loss dependency on the gate resistor. It can also be found the minimum turn on loss during 0 A current turn on is constant for different gate resistors, this loss is the energy caused by the MOSFET module output capacitors, the amount is about 6 mJ and can be calculated as $Q_{oss} \cdot V_{in} - E_{oss}$ without including the MOSFET internal energy loss.

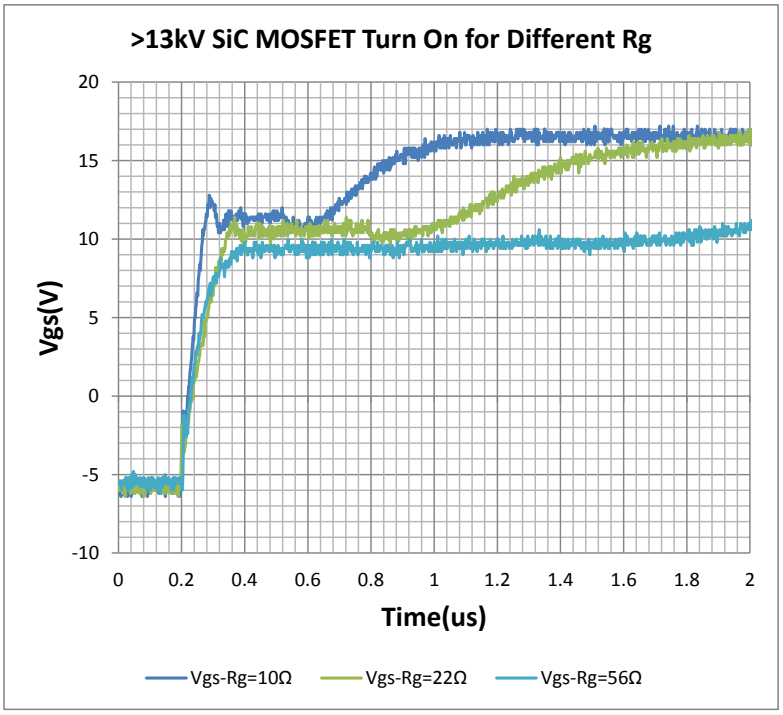



Figure 2.30: SiC MOSFET Turn on for Different $R_g$

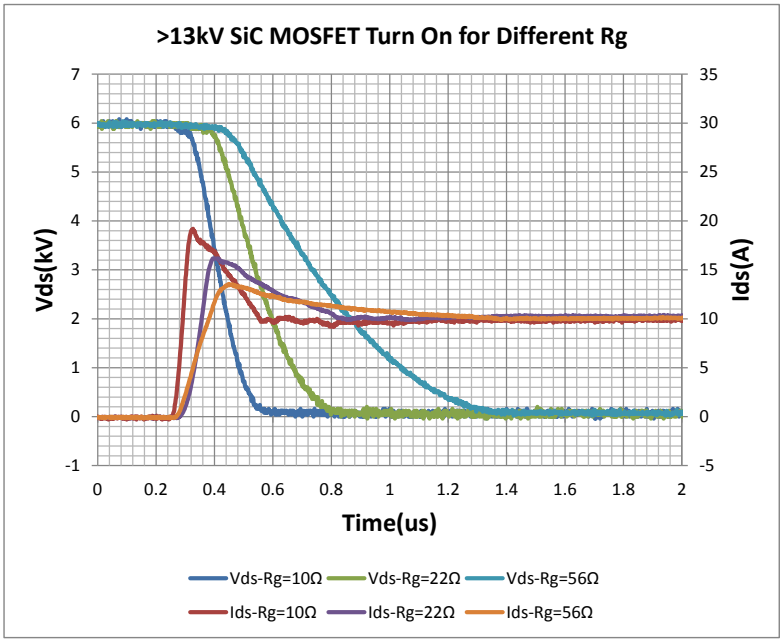



Figure 2.31: SiC MOSFET Turn on for Different $R_g$

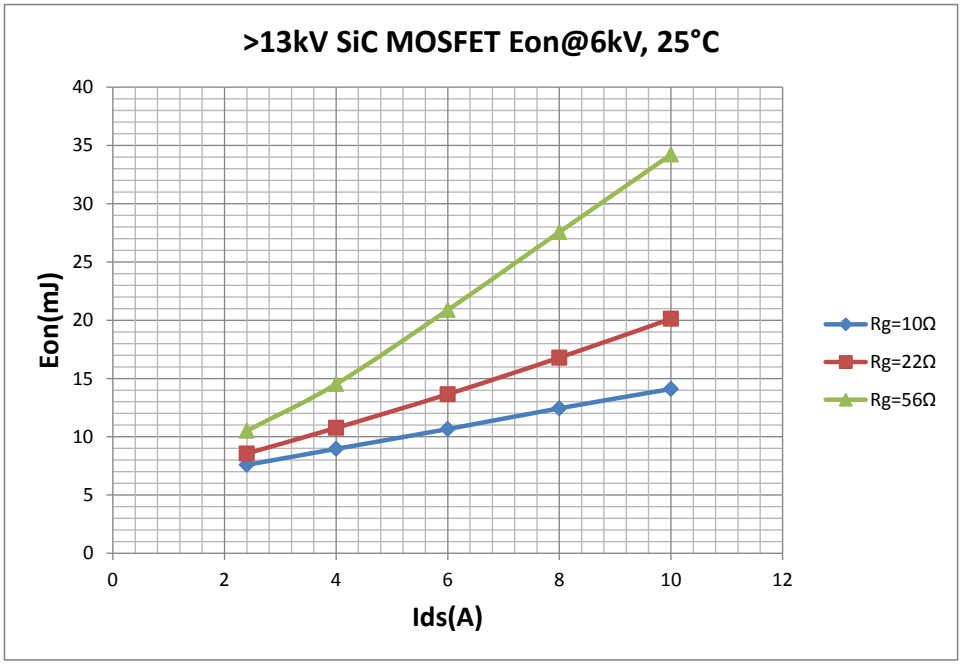



Figure 2.32: SiC MOSFET $E_{on}$

The turn off transient can also be divided into four phases as shows in Figure 2.33 which is different from the low voltage silicon MOSFET turn off transient. Phase I [$t_5$, $t_6$]: $V_{gs}$ starts to decrease at $t_5$, the MOSFET drain current will keep unchanged until $t_6$ where $V_{gs}$ reach $V_{gp}$, here $V_{gp}$ is the minimum gate voltage to maintain the drain current.

Phase II [$t_6$, $t_7$]: For low voltage MOSFET, the $V_{ds}$ will increase while the $I_{ds}$ will keep constant during this phase, while for the >13 kV SiC MOSFET, the load current will also be used for charging the output capacitance. If assuming output capacitance is constant:

$$I_L = I_{channel} + C_{oss2} \cdot \frac{dV_{ds2}}{dt} + C_{oss1} \cdot \frac{dV_{ds1}}{dt} = I_{channel} + 2 \cdot C_{oss2} \cdot \frac{dV_{ds2}}{dt} \tag{2.29}$$

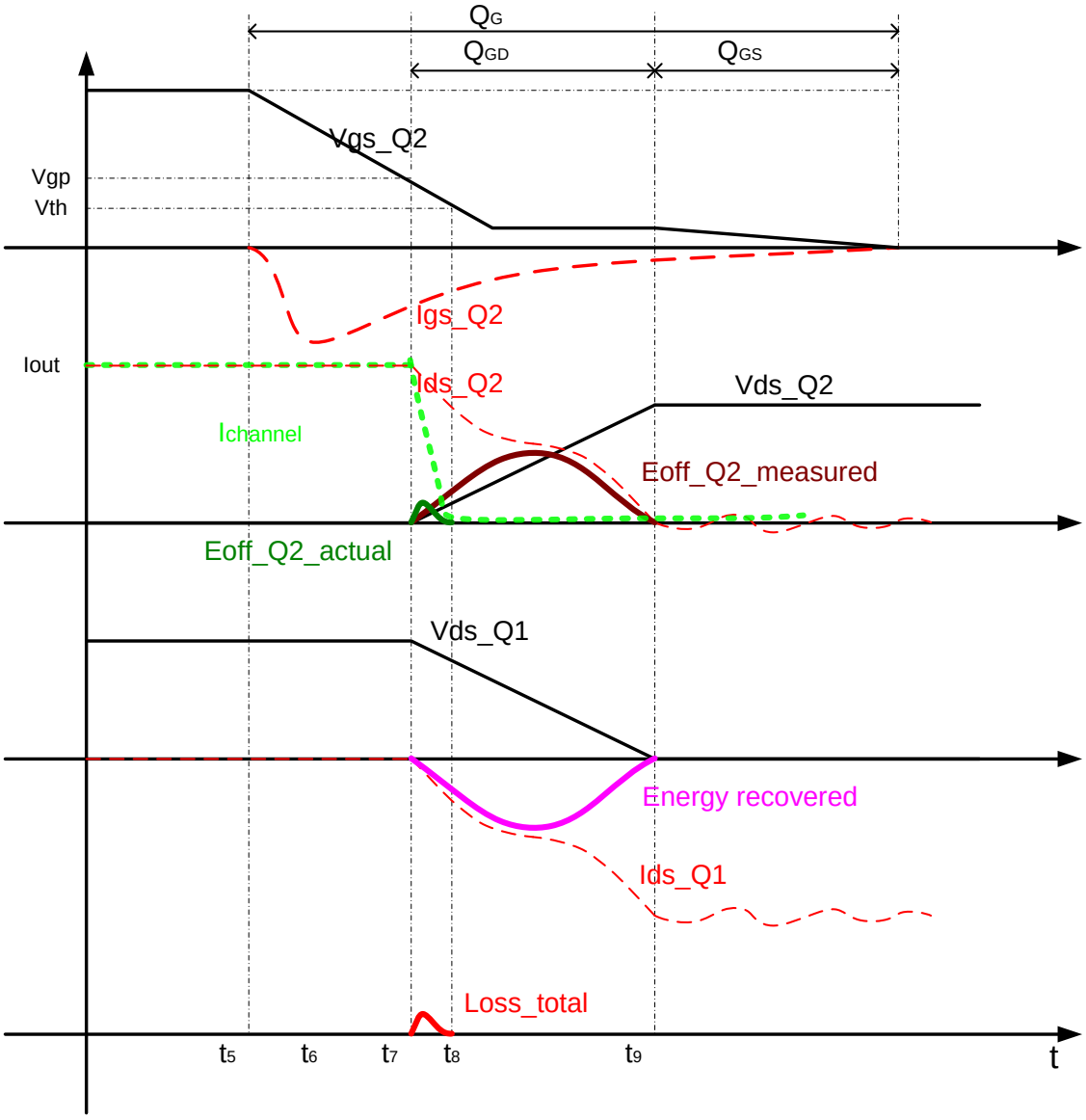



Figure 2.33: MOSFET Turn off Process

$$-I_{gd2} = C_{gd2}\frac{dV_{ds2}}{dt} = \frac{C_{gd2}}{2 \cdot C_{oss2}} \cdot (I_L - I_{channel}) \tag{2.30}$$

Since $C_{oss2}$ is typical about 10 times of $C_{gd2}$ for the SiC MOSFET, For 10A load current,

$$-I_{gd2} = \frac{C_{gd2}}{2 \cdot C_{oss2}} \cdot (I_L - I_{channel}) < \frac{1}{2 \cdot 10} \cdot (10 - 0) = 0.5A \tag{2.31}$$

The above equation indicates with no channel current and all load current is used for charging $C_{oss2}$ and discharging $C_{oss1}$, the maximum drain gate current is 0.5 A, if the gate driver sink current is higher than 0.5 A, the $V_{gs}$ will be discharged to a value less the threshold voltage, when the channel current becomes 0 A. This transient is very fast with properly chosen $R_{g(off)}$ and during this time the $V_{ds}$ is still almost zero, so $E_{off}(t_{7\_6}) \approx 0$

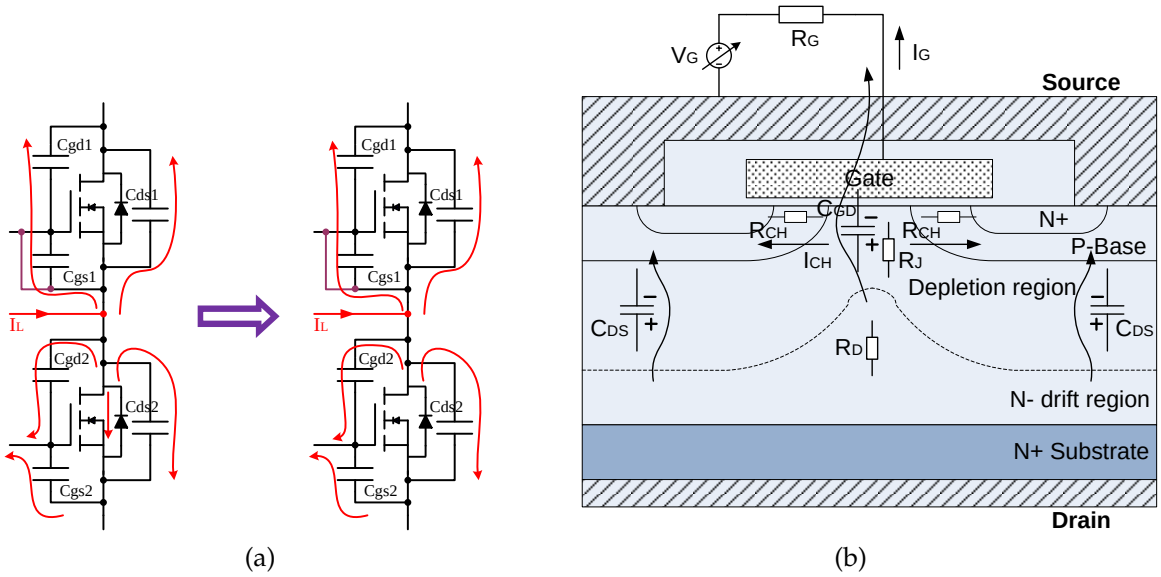
Phase III [$t_7$, $t_8$]: At $t_7$, the MOSFET channel has been reached 0, for phase 3, the load current will be divided by the parasitic capacitors as shown in Figure 2.33 and Figure 2.34

$$I_{gd2} = \frac{C_{gd2}}{C_{oss1} + C_{oss2}} \cdot I_L \tag{2.32}$$

$$I_{ds2} = \frac{C_{ds2}}{C_{oss1} + C_{oss2}} \cdot I_L \tag{2.33}$$

$$I_{oss1} = \frac{C_{oss1}}{C_{oss1} + C_{oss2}} \cdot I_L \tag{2.34}$$

$$E_{off\_measured}(t_{8\_7}) = \int_{t7}^{t8} V_{ds} \cdot I_d \cdot dt = E_{oss2} \tag{2.35}$$




(a) (b)

Figure 2.34: MOSFET Internal Parasitic Capacitance Discharging During Turn off

Phase IV [$t_8$, $t_9$]:

At $t_8$, $V_{ds}$ reach $V_{in}$, the fly-wheel diode starts to conduct, and $V_{gs}$ drops to the gate driver turn off voltage. The total measured turn off loss is $E_{oss2}$ while the actual loss which converted to heat is negligible.

$$E_{sw(measured)} = E_{on(measured)} + E_{off(measured)} = \frac{1}{2} \cdot V_{in} \cdot I_{in} \cdot \frac{Q_{SW}}{I_{G(L-H)}} + Q_{oss} \cdot V_{in} = E_{on} \tag{2.36}$$

Though the total measured loss equals the total actual loss, the loss energy has only been converted to the heat during the turn on. So for the zero voltage turn on application, the switching loss will virtually be zero.

The SiC MOSFET module turn off has been tested with a turn off gate resistance of 1Ω, 10Ω, 22Ω, 56Ω separately, the switching waveforms have been plotted in Figure 2.35 and Figure 2.36, the measured turn off loss has been plotted in Figure 2.37.

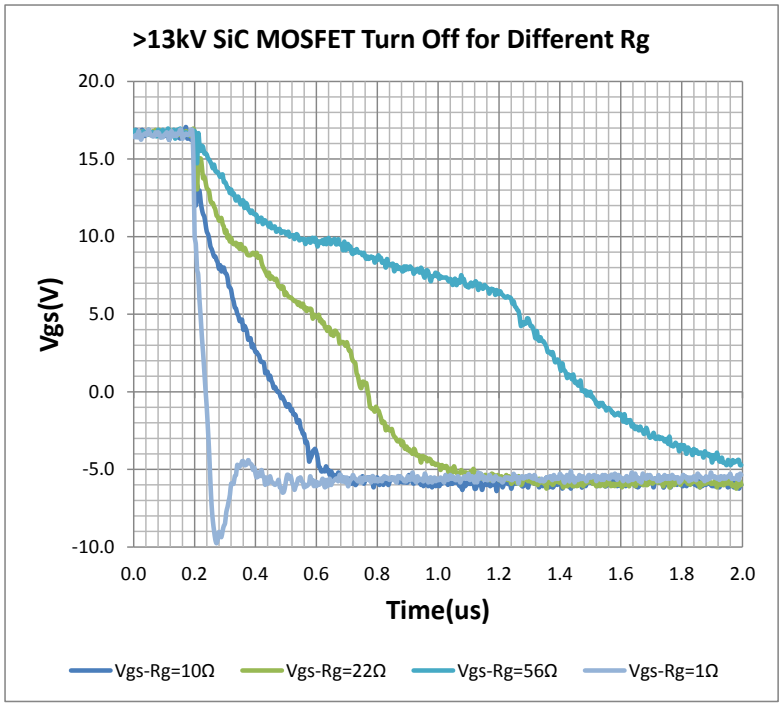



Figure 2.35: SiC MOSFET Turn off for Different $R_g$

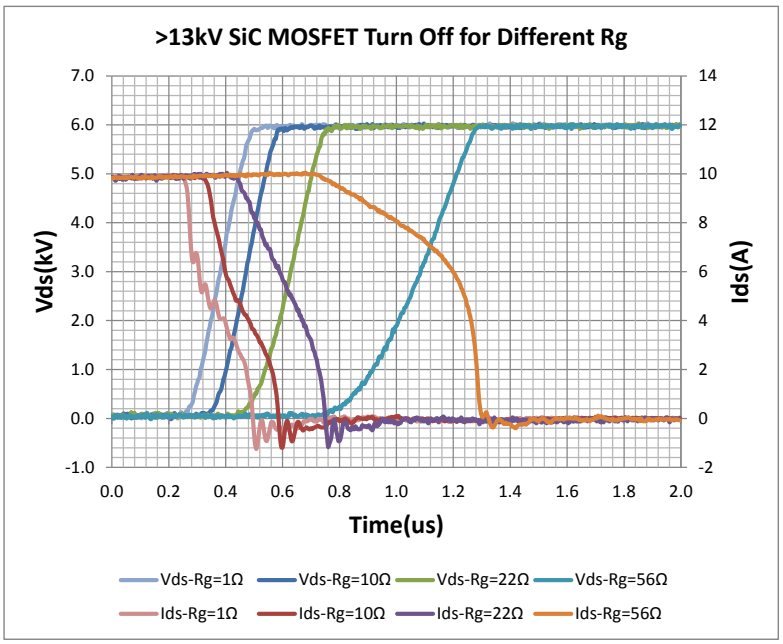



Figure 2.36: SiC MOSFET Turn off for Different $R_g$

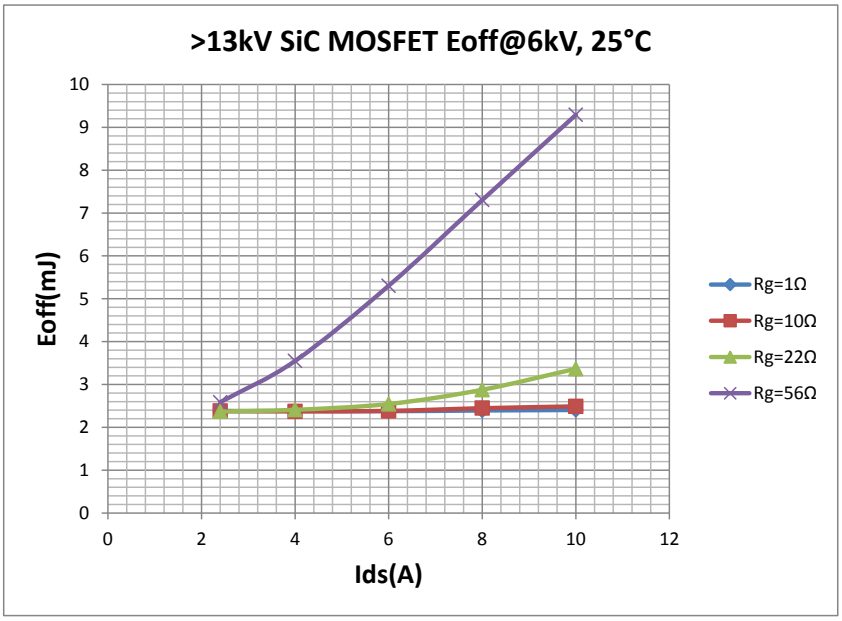



Figure 2.37: SiC MOSFET Turn off Energy for Different $R_g$

### 2.5.4 MOSFET Parasitic Capacitances Measurement

As per the analysis in the previous sections, the high voltage MOSFET output capacitance stores a significant amount of energy. Hence it is critical to have an accurate estimation of its value. Due to the nonlinear characteristic, the capacitance will be different for different voltage bias. The LCR meter or impedance analyzer usually can only generated 40 V bias which is much below the device rated voltage. For the higher voltage measurement, some methods have been proposed in [3, 36, 18], all of these solutions are based on the static measurement through impedance analysis and requires some external circuits including high voltage bias. These circuits are complex and have poor capacitance measurement accuracy.

The output and reverse transfer capacitance can also be estimated through the dynamic switching test. As shown in Figure 2.39 The top MOSFET gate source is

shorted, when the bottom MOSFET switches from off to on status, the top MOSFET $C_{gd1}$ and $C_{ds1}$ will be charged, the waveforms of $V_{ds1}$, $I_{d1}$ and $I_{gd1}$ can be captured through the oscilloscope, and then the capacitance can be calculated as:

$$C_{oss} = I_{d1}/(\frac{dV_{ds1}}{dt}) \tag{2.37}$$

$$C_{oss} = I_{d1}/(\frac{dV_{ds1}}{dt}) \tag{2.38}$$

Due to the probe's measurement resolution, the calculated capacitance will include large error when the measured drain source voltage is low. A combination method should be used which includes both the static measurement for low voltage bias and the dynamic switching test for high voltage bias. First of all, the MOSFET capacitance can be predicted by Eq. 2.39,

$$C(V) = \frac{k}{\sqrt{V + V_{bi}}} \tag{2.39}$$

Considering some packaging related capacitance , the equation becomes:

$$C(V) = \frac{k}{\sqrt{V + V_{bi}}} + C_o \tag{2.40}$$

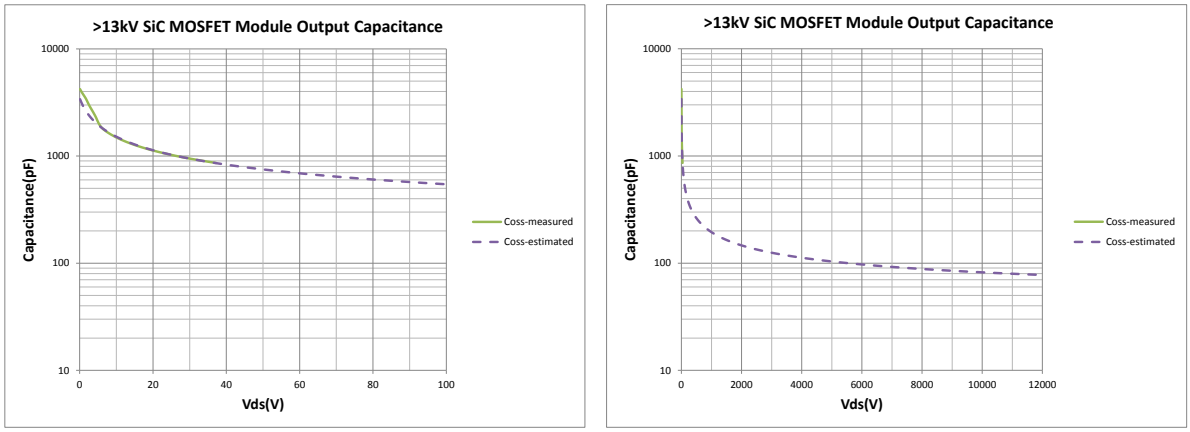
So,

$$\frac{C_{oss}(V_1) - C_o}{C_{oss}(V_2) - C_o} = \frac{\sqrt{V_2 + V_{bi}}}{\sqrt{V_1 + V_{bi}}} \tag{2.41}$$

$$C_{oss}(V_1) = \frac{\sqrt{V_2 + V_{bi}}}{\sqrt{V_1 + V_{bi}}} \cdot (C_{oss}(V_2) - C_o) + C_o \tag{2.42}$$

With all capacitances which has measured up to 40V bias, the $V_{bi}$, $C_o$ in the above equation can be solved. However, $C_o$ is much smaller than the output capacitance

with less than 40V voltage bias, its value should be calibrated by the high voltage dynamic switching test results. The finale estimations are $C_{oss}(37.3) = 859pF$, $V_{bi} = 2.3$, $C_o = 30pF$ and the output capacitance has been plotted in Figure 2.38 and accordingly the output capacitor stored charge and energy can be calculated.




(a) (b)

Figure 2.38: SiC MOSFET Output Capacitance ($C_{oss}$)

The above estimation needs to be verified by the dynamic measurement with the pulse test circuit shown in Figure 2.39. and one single gating pulse has been applied Figure 2.40. During the turn on,

$$\int I_{ds2} \cdot dt = Q_{oss1}(V_{in}) + C_p \cdot V_{in} \tag{2.43}$$

$$\int V_{ds2} \cdot I_{ds2} \cdot dt = Q_{oss1} \cdot V_{in} - E_{oss1}(V_{in}) + \frac{1}{2} \cdot C_p \cdot V_{in}^2 \tag{2.44}$$

During the turn off, if the turn off gate resistance small enough,

$$\int I_{ds2} \cdot dt = Q_{oss2}(V_{in}) \tag{2.45}$$

$$\int V_{ds2} \cdot I_{ds2} \cdot dt = E_{oss2}(V_{in}) \tag{2.46}$$

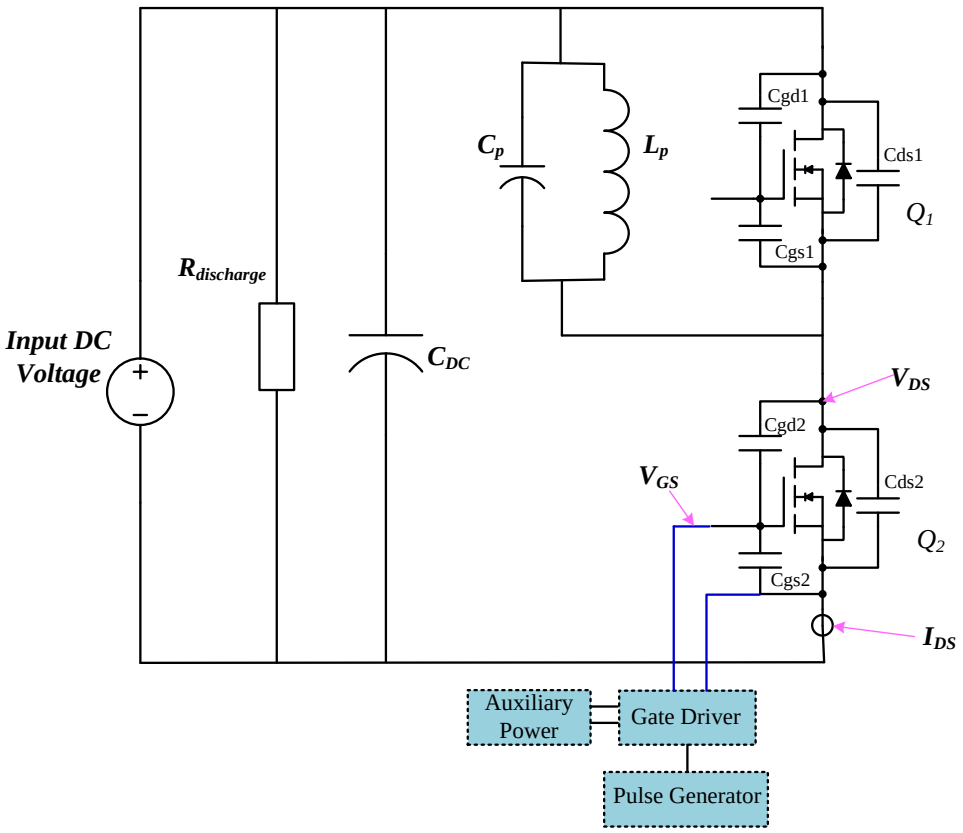



Figure 2.39: SiC MOSFET Double Pulse Test Circuit

The output capacitor energy and charge can also be calculated by its capacitance:

$$Q_{oss}(V_{in}) = \int_0^{V_{in}} C_{oss}(V) \cdot dv \tag{2.47}$$

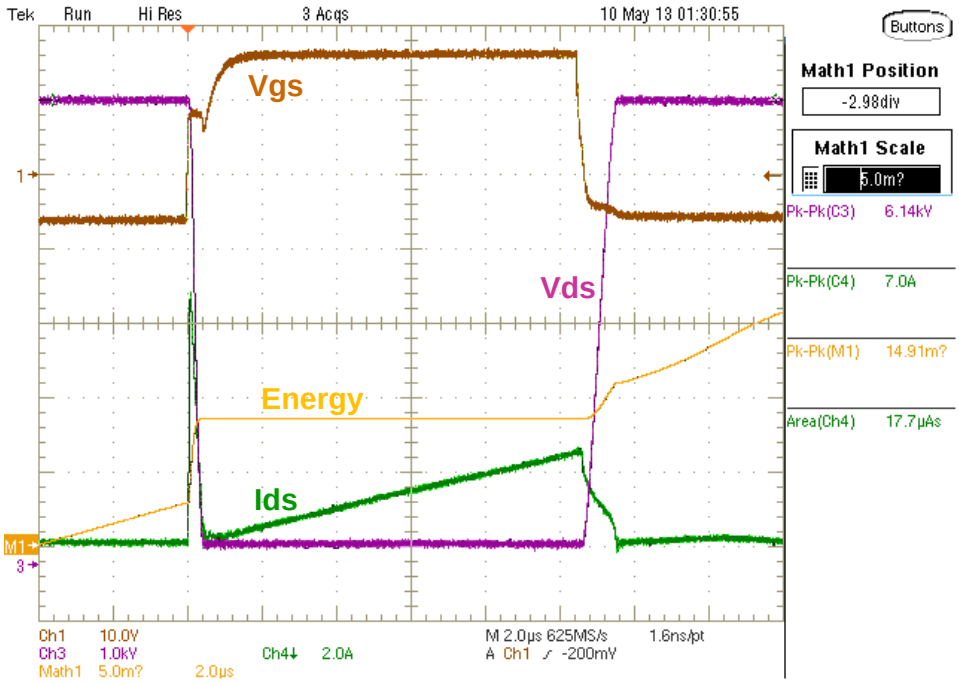



Figure 2.40: SiC MOSFET 0A Turn on and off Waveforms

$$E_{oss}(V_{in}) = \int_0^{V_{in}} V(Q)dq = V_{in} \cdot Q_{oss}(V_{in}) - \int_0^{V_{in}} Q_{oss}(v)dv \tag{2.48}$$

In Figure 2.41 the output capacitor charge has been estimated based on the output capacitance model for 1 kV to 12 kV drain voltage bias, the dynamic measurement data has been taken for the drain voltage 3 kV to 6 kV, it shows a good match.

In Figure 2.42 the output capacitor stored energy ($E_{off}$ in the figure) and the dissipated energy for charging the output capacitor($E_{on}$ in the figure) has been estimated based on the output capacitance model for 1 kV to 12 kV drain voltage, the dynamic measurement data has been taken for the drain voltage 3 kV to 6 kV, which matches with the estimated loss perfectly.

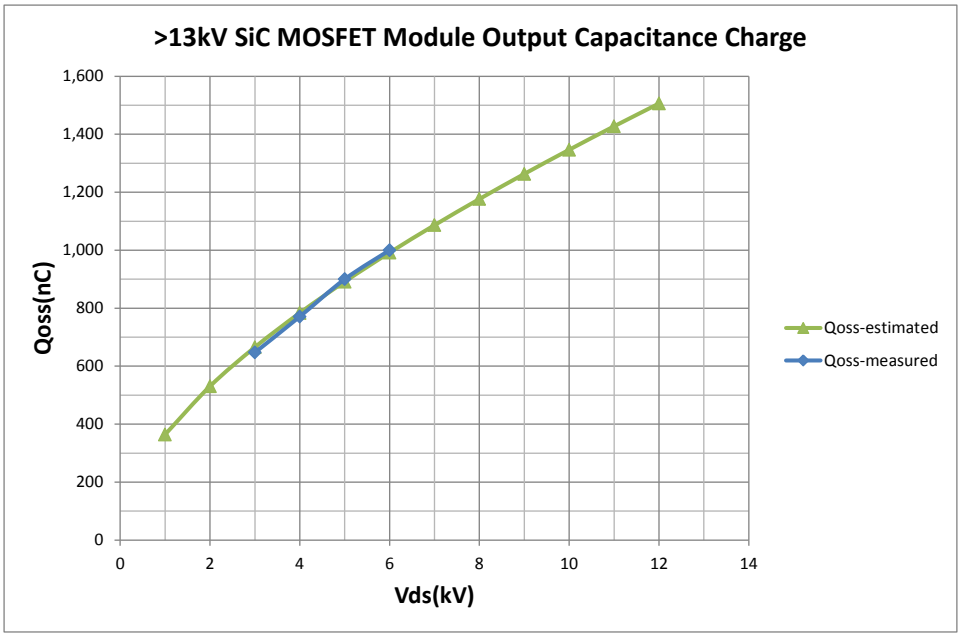



Figure 2.41: SiC MOSFET 0 A Turn on and off Waveforms

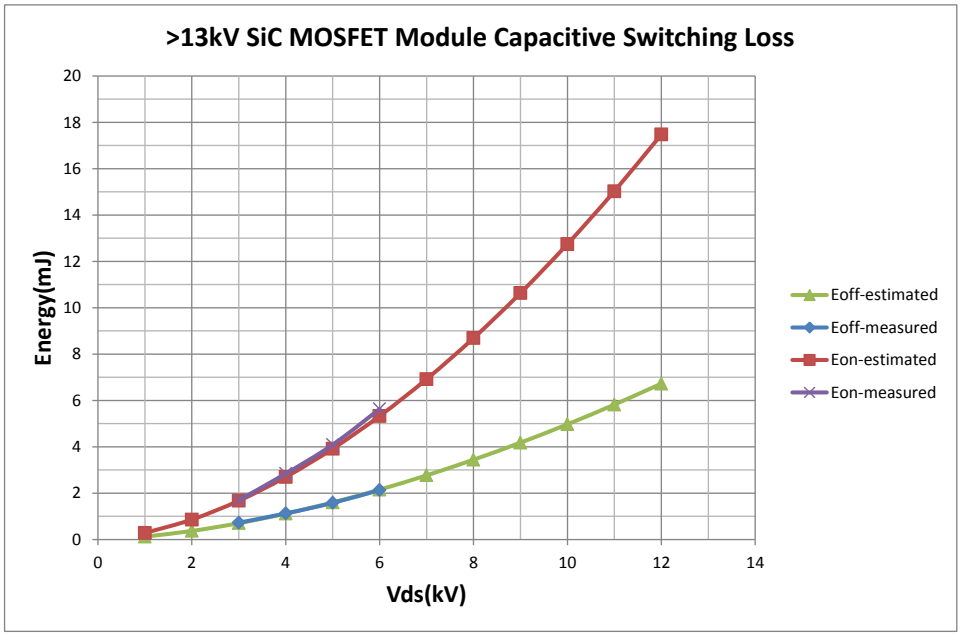



Figure 2.42: SiC MOSFET Capacitive Switching Loss

### 2.5.5 MOSFET Loss Model

The switching loss for the high voltage SiC MOSFET only contains turn on loss which can be calculated by the following equation

$$E_{on} = \frac{1}{2} \cdot V_{in} \cdot I_{in} \cdot \frac{Q_{SW}}{I_{G(L-H)}} + Q_{oss} \cdot V_{in} = \frac{1}{2} \cdot V_{in} \cdot I_{in} \cdot t_{on} + Q_{oss} \cdot V_{in} \tag{2.49}$$

The output capacitor $Q_{oss}$ has been estimated based on the output capacitance. The turn on time $t_{on}$ has been measured for the drain voltage up to 6 kV with a gate resistance of 10Ω as shown in Figure 2.43, the linear turn on time increase from 3 kV to 6 kV drain voltage has been observed for different drain current, and for the higher drain voltage, the $C_{gd}$ decrease very slightly, it is fair to estimate that the turn on time will increase linearly for voltage high than 6 kV and up to 12 kV.

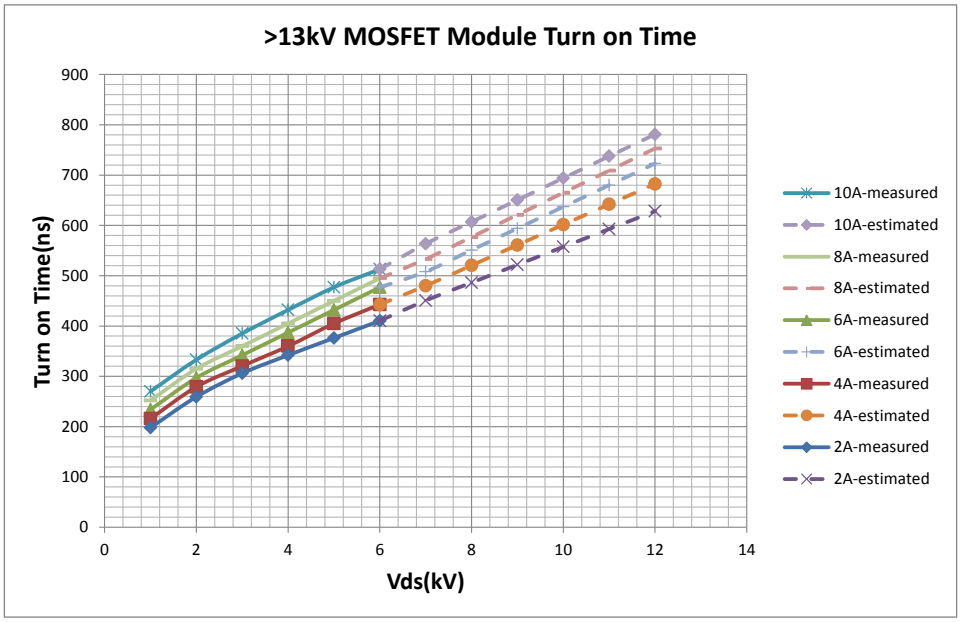



Figure 2.43: SiC MOSFET Turn on Time

With the estimated turn on time for different conditions, the switching loss can be estimated and plotted as in Figure 2.44, the measurement results for voltage less than 6 kV have also been given and matches the estimation.

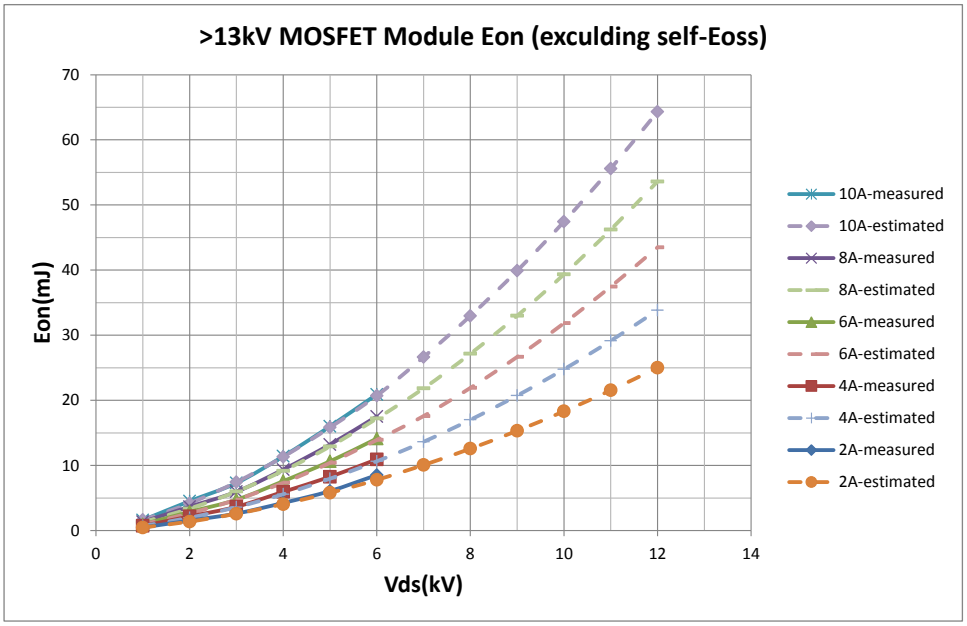



Figure 2.44: SiC MOSFET $E_{on}$ Excluding Self-$E_{oss}$

The Figure 2.45 plots the turn on loss verses drain current for different drain voltage, for 0 A drain current, the turn on loss is the minimum which is determined by the output capacitance. It has been noted that the some parasitic capacitance of the other components of the system like the inductor connected to the MOSFET will also generate losses during the turn on. When calculating the efficiency, these system capacitance has also need to be considered.

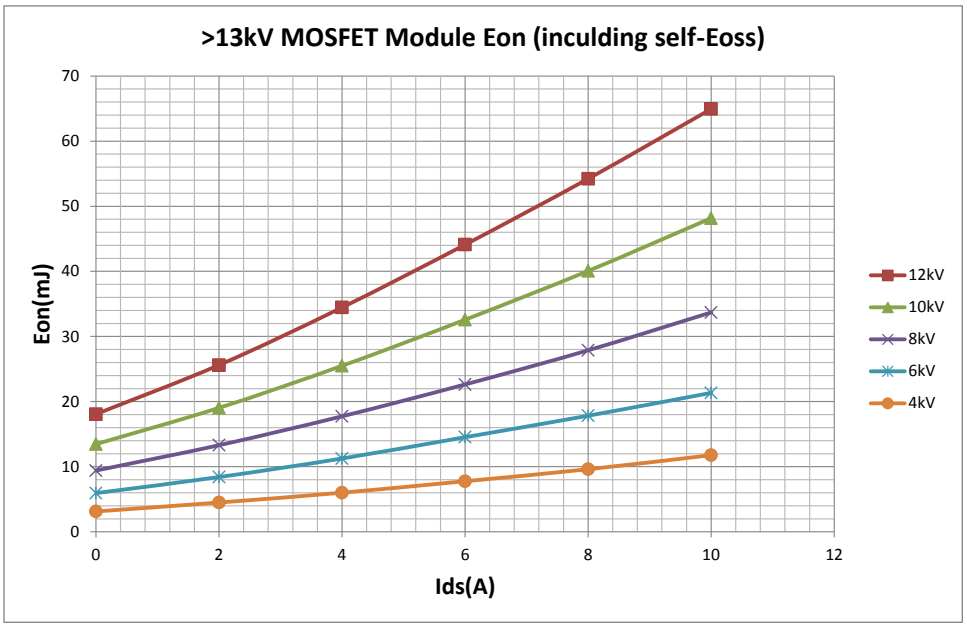



Figure 2.45: SiC MOSFET $E_{on}$ Including Self-$E_{oss}$

### 2.5.6 Experiment Verification

To validate the SiC MOSFET switching loss analysis, a boost converter (Figure 2.46 and Figure 2.49) has been built in order to test continuous operation of the above MOSFET under both soft switched and hard switched mode.

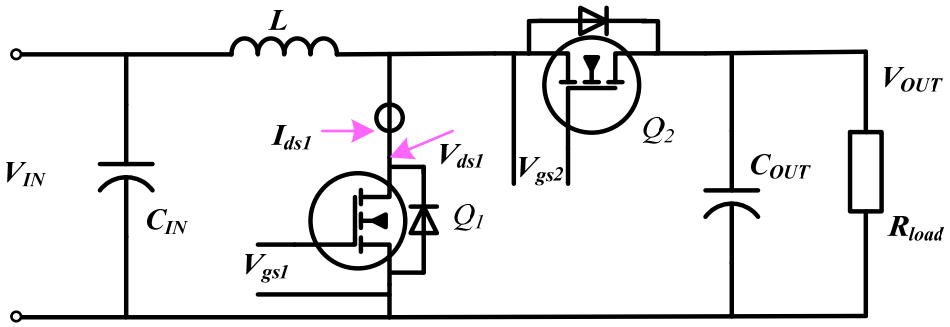



Figure 2.46: >13 kV SiC MOSFET Boost Converter Circuit

As in Figure 2.47, $Q_1$ and $Q_2$ are switched complementary, when $Q_1$ is on, the inductor current increase linearly and when $Q_2$ is on, the inductor current will decrease linearly. The duty of $Q_1$ can be adjusted in such a way the inductor has some negative current which means the $V_{ds}$ for $Q_1$ is close to 0 V the moment of its turn on.

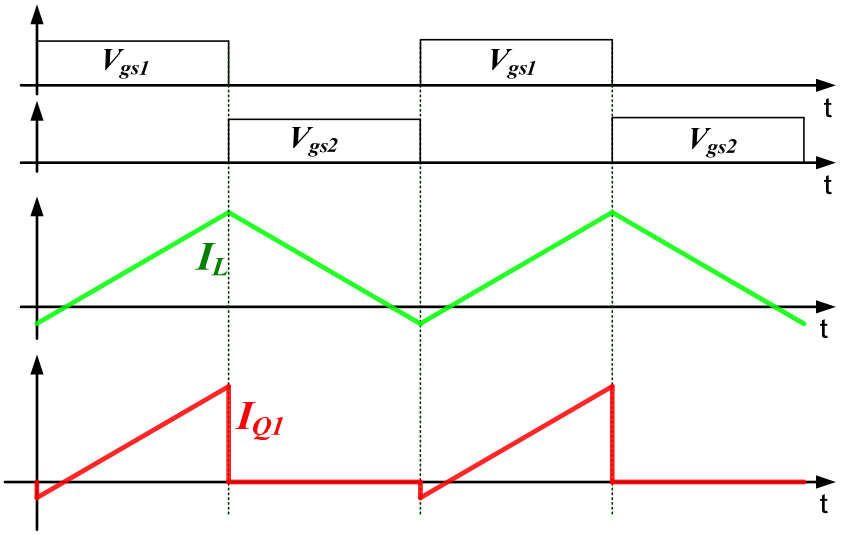



Figure 2.47: >13 kV SiC MOSFET Boost Converter Operates under CRM Mode

For the boost converter operates under CCM mode (Figure 2.48), the $Q_1$ is hard switched since at the instantaneous of its turn on, the $Q_1$ $V_{ds}$ equals $V_{out}$.

The $L_1$ is 8 mH for 20 kHz operation and 4 mH for 40 kHz operation.

The converter has been operated in three cases:1) 20 kHz soft switching (Figure 2.50); 2) 40 kHz soft switching (Figure 2.51) and 3) 40 kHz hard switching (Figure 2.52).

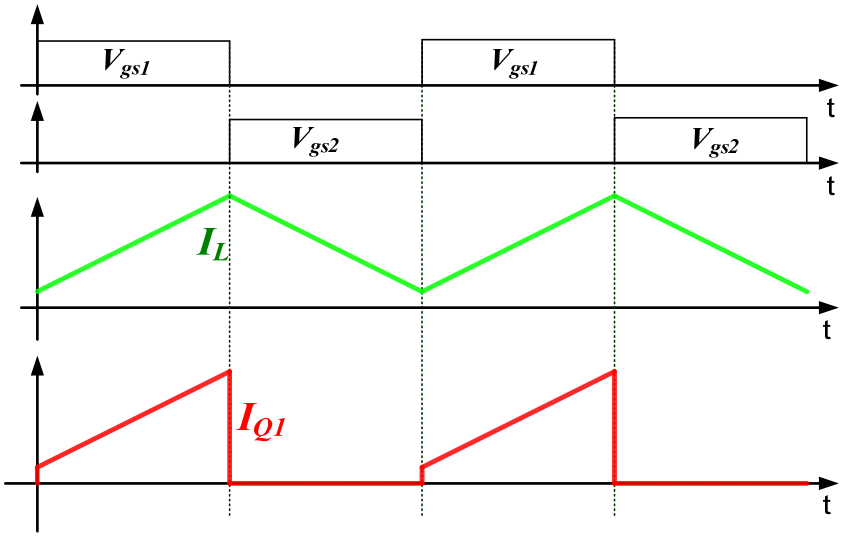



Figure 2.48: >13 kV SiC MOSFET Boost Converter Operates under CCM Mode

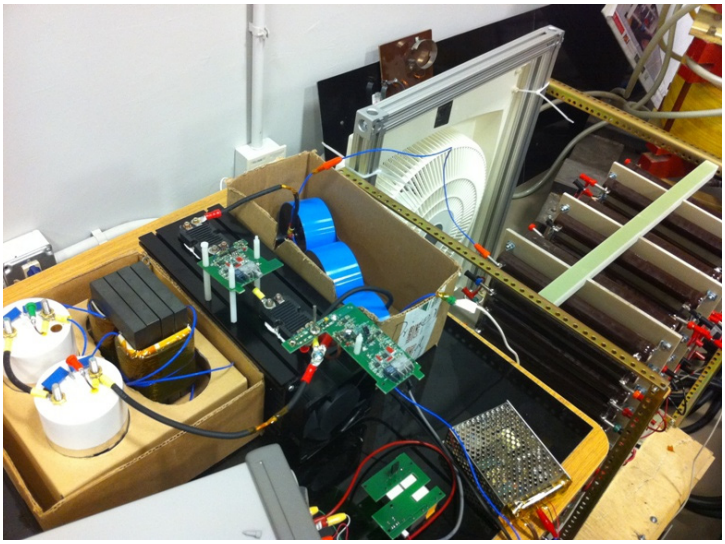


Figure 2.49: SiC MOSFET Boost Converter Circuit

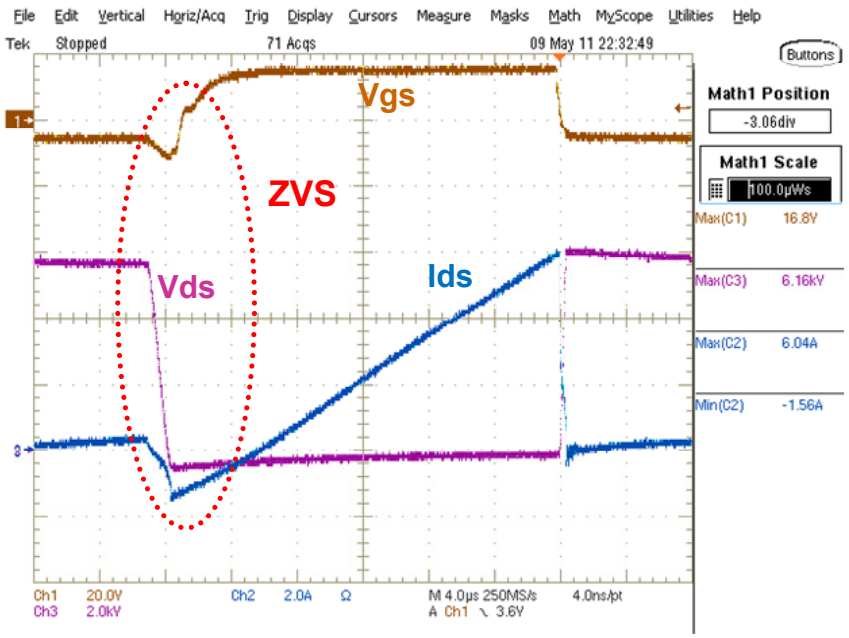



Figure 2.50: SiC MOSFET Soft Switched at 20kHz

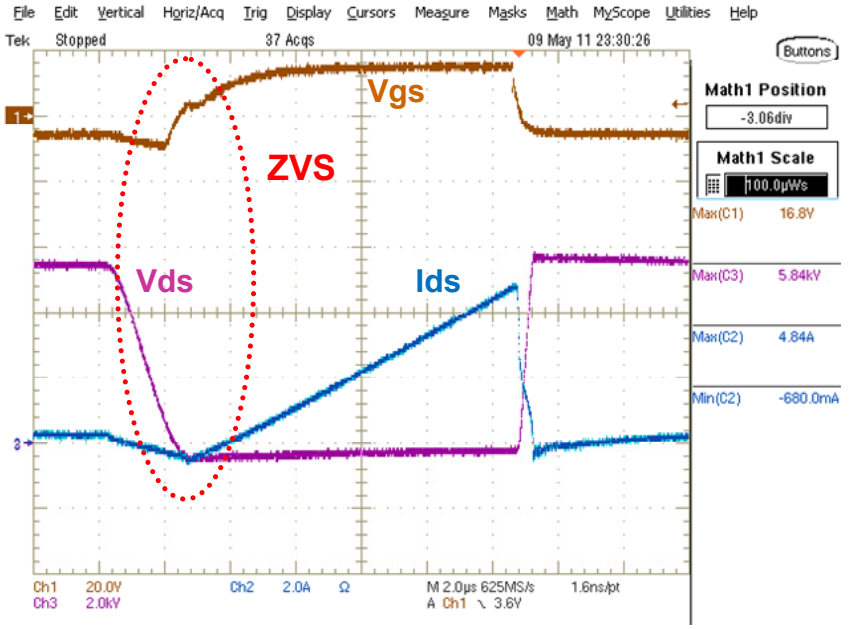



Figure 2.51: SiC MOSFET Soft Switched at 40 kHz

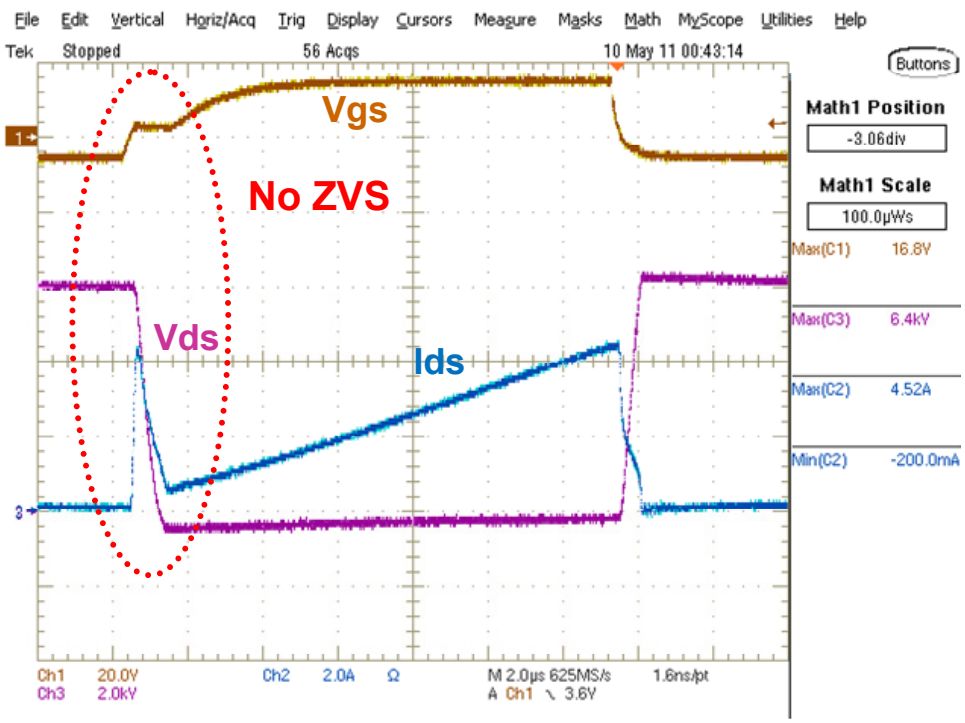



Figure 2.52: SiC MOSFET Hard Switched at 40 kHz

The efficiency and losses for three cases has been plotted as Figure 2.53 and Figure 2.54 , it can be found the loss is very close under two soft switched cases while under hard switching, the converter loss increased significantly. The blue line in Figure 2.54 is the loss that adds MOSFET turn on loss to the converter loss under soft switching, which matches the measured loss very well.

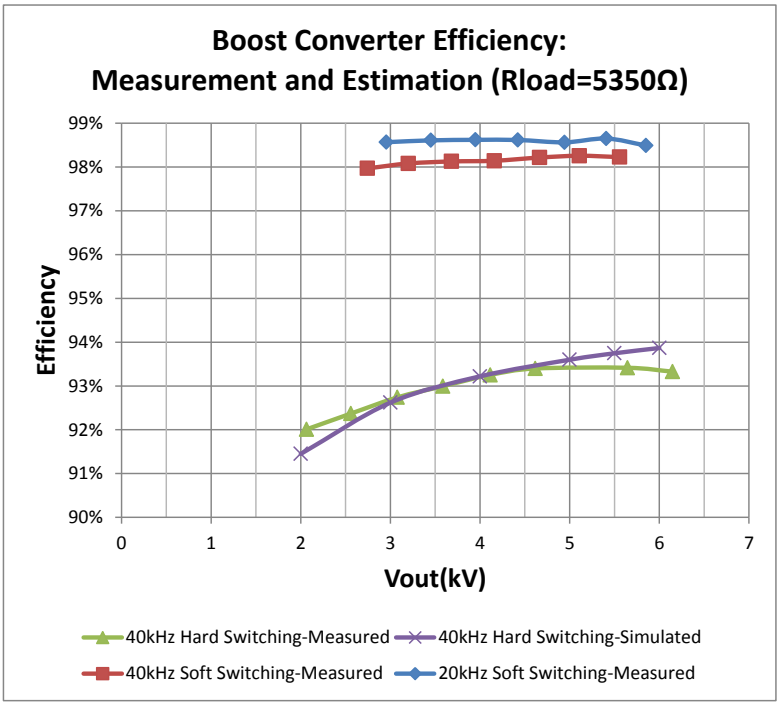



Figure 2.53: SiC MOSFET Boost Converter Efficiency

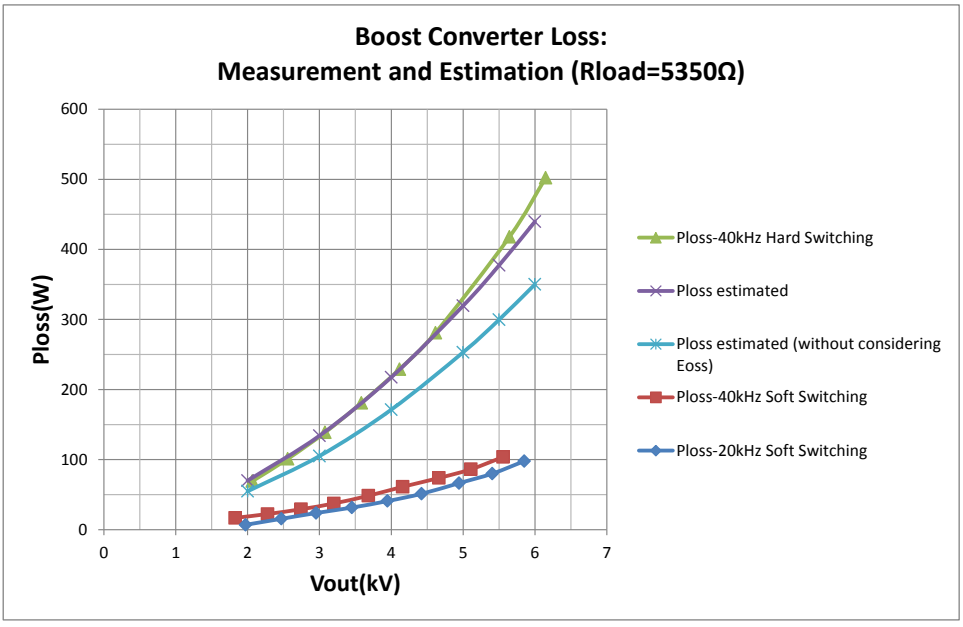



Figure 2.54: SiC MOSFET Boost Converter Loss

### 2.5.7 High Voltage SiC MOSFET Gate Driver

Due the high $V_{ds}$ voltage and high $dv/dt$ during transient, the power supply for the gate driver requires high voltage insulation and low capacitance coupling. The proposed solution is using wireless energy transfer method (Figure 2.55) which totally separates the primary from the secondary. The distance between primary and secondary coils can be adjusted to fulfill insulation requirement.

The commercial cell wireless charger has been modified as the power supply for the gate driver for saving cost and time, optical fiber is used for transmitting the PWM signal.

The whole gate driver consists of four layers: wireless energy transmitter board, insulation board, wireless energy receiver board, gate driver board. The prototype is shown as Figure 2.55.

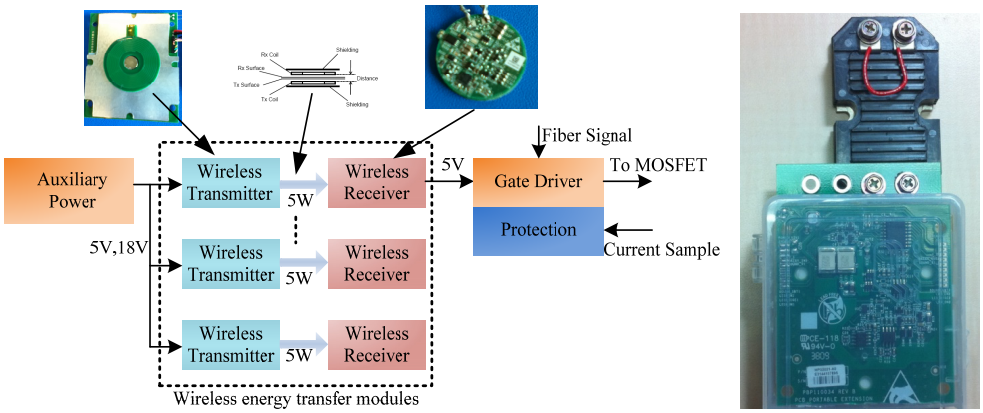



Figure 2.55: SiC MOSFET Gate Driver Power Supply (left) and Prototype (right)

### 2.5.8 Comparisons of 6.5 kV IGBT and >13 kV SiC MOSFET

The 6.5 kV IGBT and >13 kV MOSFET are compared based on their conduction and switching performance. The forward J-V curves are plotted in Figure 2.56 for 25 °C and 125 °C. Two 6.5 kV IGBTs have been put in series for an equivalent 13 kV blocking voltage, it can be seen that the MOSFET has lower forward voltage drop for $V_F$ less than about 9 V. The forward characteristic is compared based on current density. The >13 kV MOSFET has an chip area $8.1mm \times 8.1mm$ while 6.5 kV IGBT has an chip area $13.6mm \times 13.6mm$.

vspace0.2in

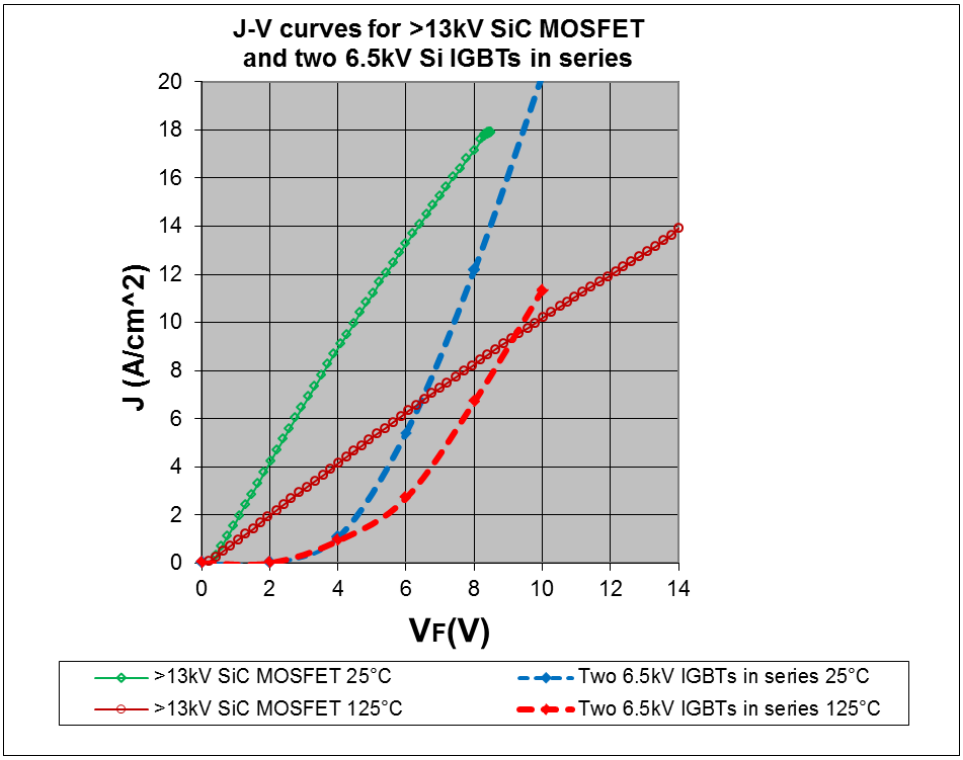



Figure 2.56: Forward I-V Curves of 6.5 kV IGBT and >13 kV SiC MOSFET

With the same DC bus voltage 4 kV, SiC MOSFET has lower turn on loss (Figure 2.57), a large portion of which is contributed by the parasitic capacitances. When the MOSFET switches at 12 kV, its turn on loss is close to the IGBT turn on at 4 kV.

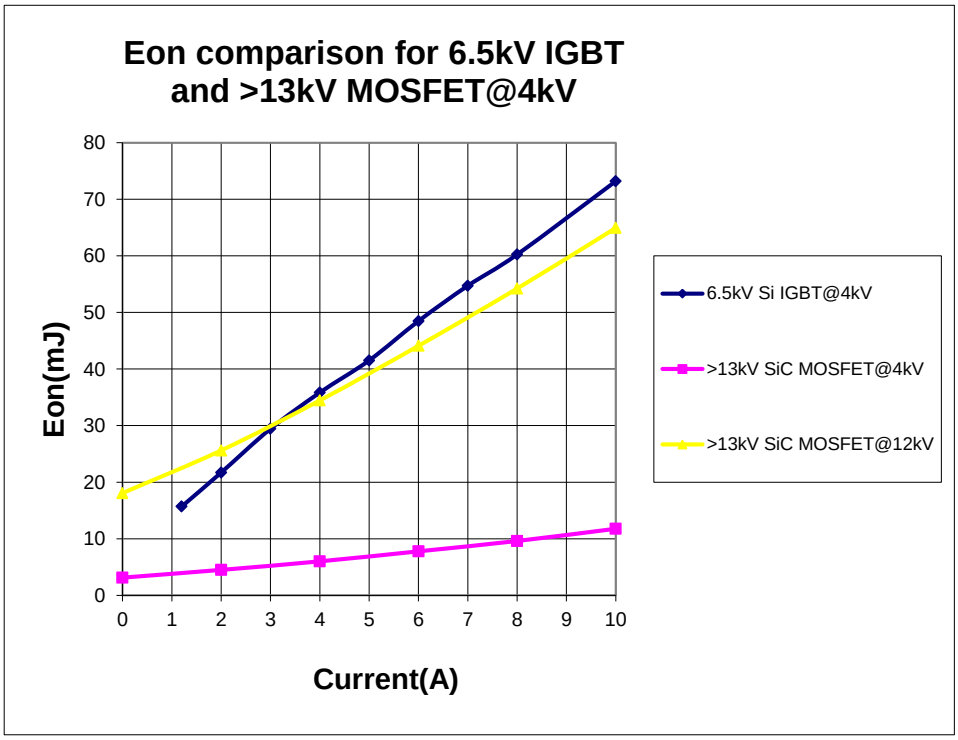



Figure 2.57: Turn-on Loss of 6.5 kV IGBT and >13 kV SiC MOSFET

For the turn off, there is no loss for the MOSFET according to the previous analysis, while turn off loss is still current dependent for IGBT as shown in Figure 2.58 which concludes that SiC MOSFET has much lower switching loss than Si IGBT.

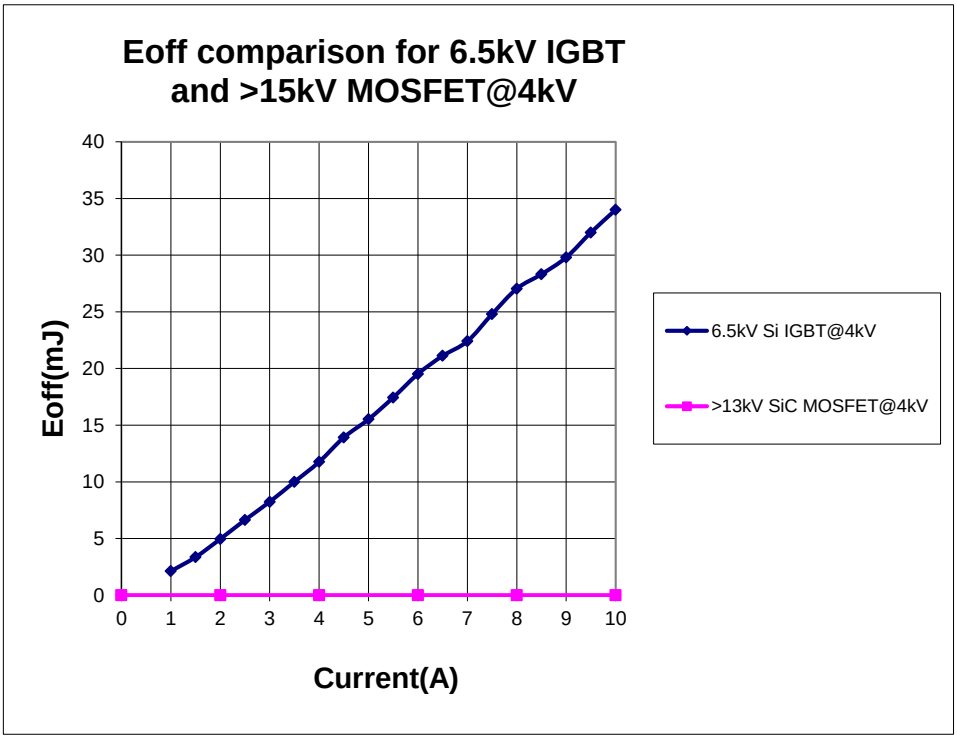



Figure 2.58: Turn-off Loss of 6.5 kV IGBT and >13 kV SiC MOSFET

## 2.6 Comparisons of High Voltage SiC IGBT and MOSFET

### 2.6.1 Introduction

With the aim to increasing current capability, researchers from Cree Inc have developed SiC nIGBT with a chip size of $8.4mm \times 8.4mm$ which can block higher than 15 kV voltage. There are two different designs, one has 2um buffer layer, the other one has 5um buffer layer. Their forward characteristics have been plotted in Figure 2.59 compared with SiC the MOSFET. It can be observed that: 1)2um buffer layer IGBT has lower forward voltage drop than 5um buffer layer IGBT; 2) IGBT forward characteristic is weak dependent on the junction temperature compared with MOSFET; 3)IGBTs have lower forward voltage then MOSFET for more than 3 A current with 125 °C junction temperature.

### 2.6.2 Switching Loss Test Setup

Since the inductor parasitic capacitance, the fly-wheel diode junction capacitance and other parasitic capacitances play an important role in determining the switching loss of the high voltage device under test, it is desired to test the two IGBTs and one MOSFET by using the same setup. Figure 2.60 shows the double pulses test circuit diagram and hardware for all the three device. The setup will be kept as the same for each test except the device under test can be replaced, a >13 kV JBS diode is used as the fly-wheel diode. The hotplate is used to heat up the device for high junction temperature test.

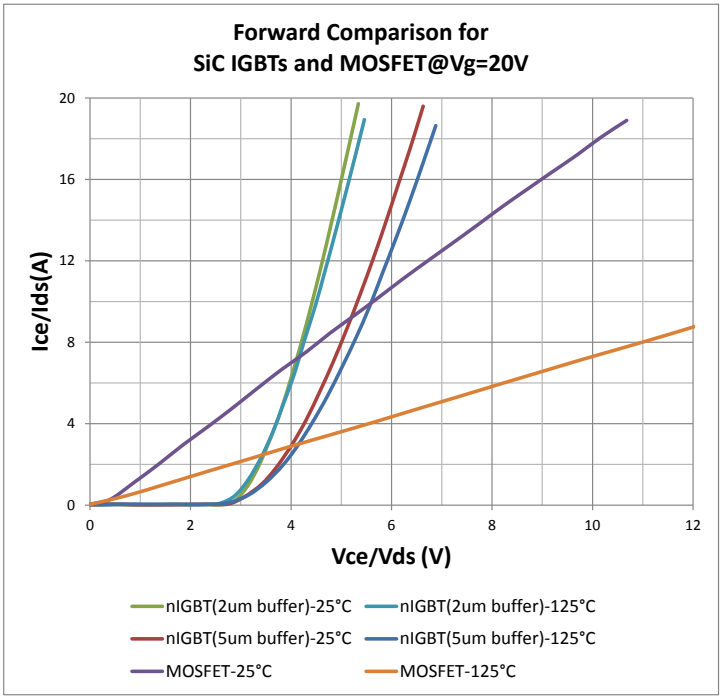



Figure 2.59: Forward Comparison of High Voltage MOSFET and IGBTs

### 2.6.3 Switching Transient under Different Temperature

The switching performance for power device is not only dependent on its physical structure, it is also affected by external parameters like gate driver voltage, gate driver resistance and temperature. In this section, sensitivity of the switching speed and loss to those parameters will be illustrated for both MOSFET and IGBTs. As a comparison, the same conditions 9 kV voltage and 10 A current have been applied for all the switching test case discussed in this section.

Figure 2.61 shows the turn on transient for the >13 kV SiC MOSFET as in the double pulses test described in the above section. Five cases have been included: 1) $R_g = 0\Omega$, $T_j = 25\,^{\circ}\mathrm{C}$; 2) $R_g = 10\Omega$, $T_j = 25\,^{\circ}\mathrm{C}$;3) $R_g = 22\Omega$, $T_j = 25\,^{\circ}\mathrm{C}$; 4) $R_g = 10\Omega$, $T_j = 75\,^{\circ}\mathrm{C}$; 5)$R_g = 10\Omega$, $T_j = 125\,^{\circ}\mathrm{C}$. According to cases 1)-3), the MOSFET turn on

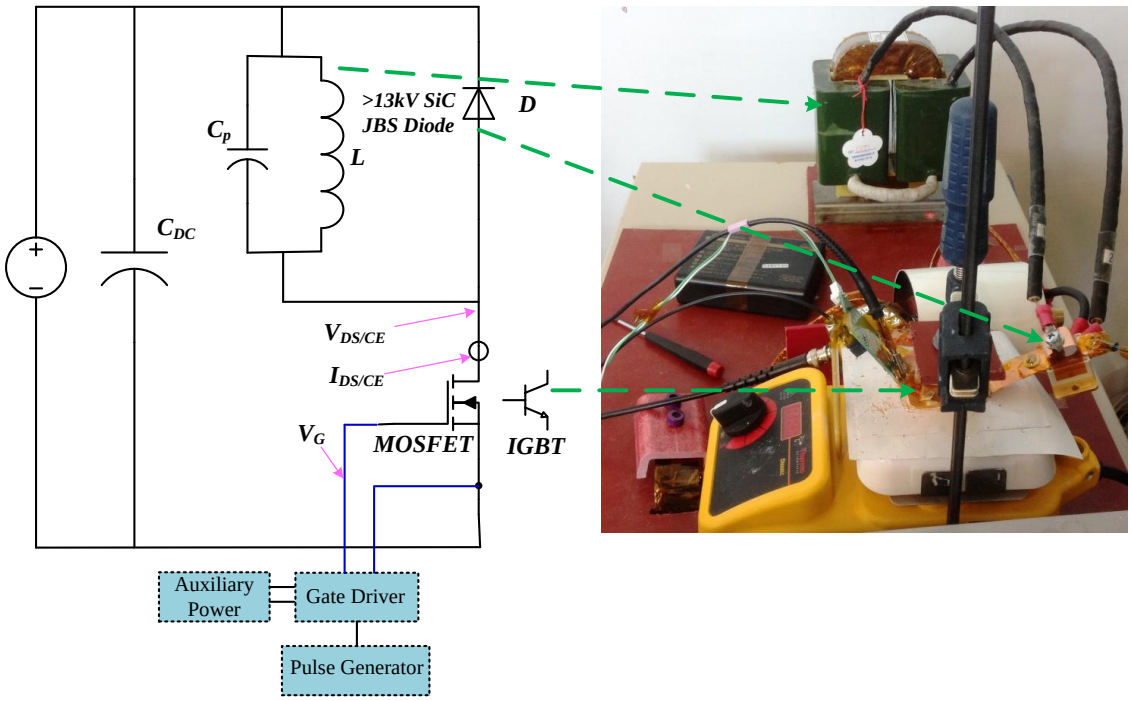



Figure 2.60: Double Pulses Test Circuit for the High Voltage MOSFET and IGBTs

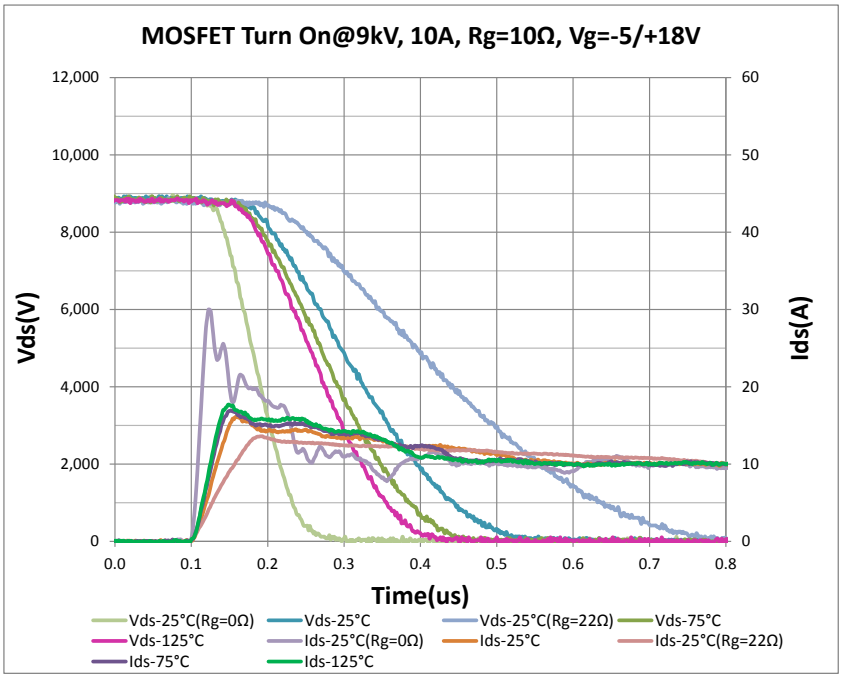



Figure 2.61: SiC MOSFET Turn on for Different Temperature

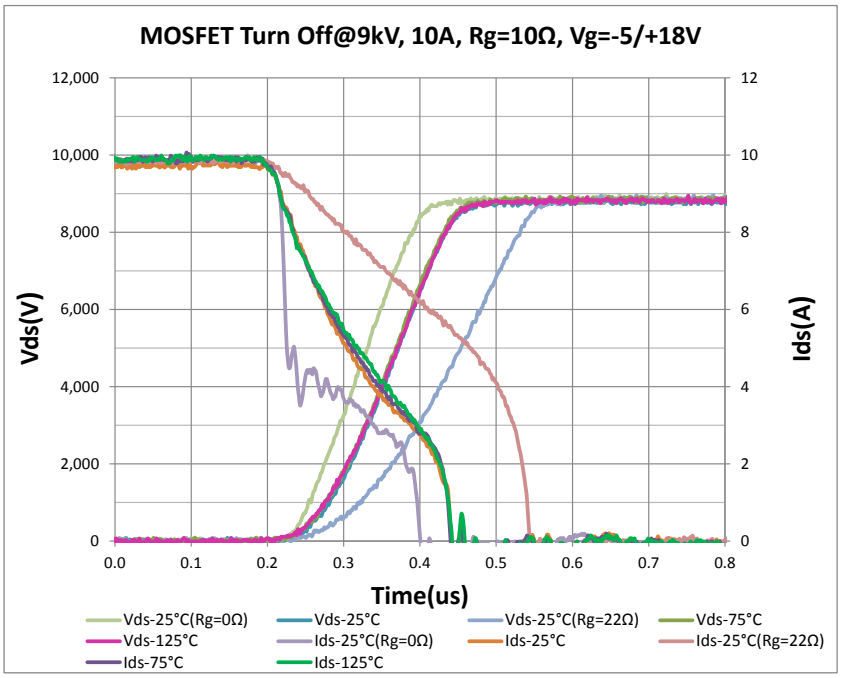



Figure 2.62: SiC MOSFET Turn off for Different Temperature

faster for smaller $R_g$; According to cases 2), 4), 5), the MOSFET turn on faster with higher junction temperature which is due to decreased threshold voltage caused by the temperature rise. Similarly for the turn off shown in Figure 2.62, smaller $R_g$ can speed up the turn off transient while it is less affected by the junction temperature.

For the 2um buffer layer SiC IGBT, there are four test cases for both turn on Figure 2.63 and turn off Figure 2.64: 1) $R_g = 10\Omega$, $T_j = 25\,^{\circ}\mathrm{C}$; 2) $R_g = 22\Omega$, $T_j = 25\,^{\circ}\mathrm{C}$; 3) $R_g = 10\Omega$, $T_j = 75\,^{\circ}\mathrm{C}$; 4) $R_g = 10\Omega$, $T_j = 125\,^{\circ}\mathrm{C}$. During turn on, the temperature difference almost has no impact on the switching speed; higher gate resistance will slow down the voltage decreasing speed when the collector emitter voltage lower than the IGBT punch through voltage, then the turn on loss will increase. While for the turn off in Figure 2.62, its speed is highly dependent on the junction temperature, the voltage rise speed is much slower with higher junction temperature especially when the collector emitter voltage lower than the IGBT punch through voltage. The turn off time ranges from 0.6 us for $25\,^{\circ}\mathrm{C}$ to 1.6 us for $125\,^{\circ}\mathrm{C}$.

The switching characteristics for the 5um buffer layer SiC IGBT are very similar to the 2um buffer layer SiC IGBT, except its turn off speed is faster, Figure 2.65 and Figure 2.66 show the turn on and turn off transient separately.

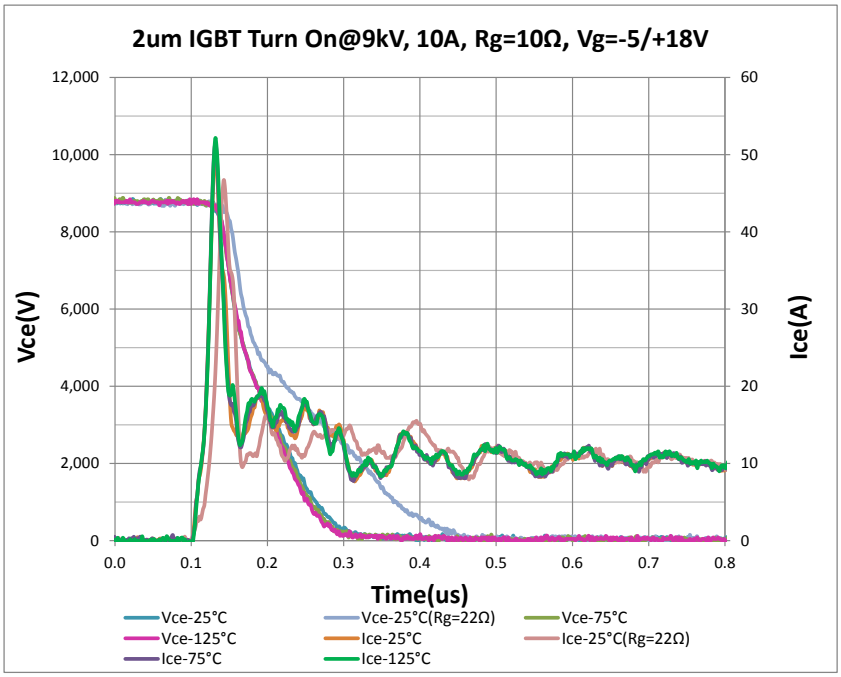



Figure 2.63: SiC IGBT with 2um Buffer Layer Turn on for Different Temperature

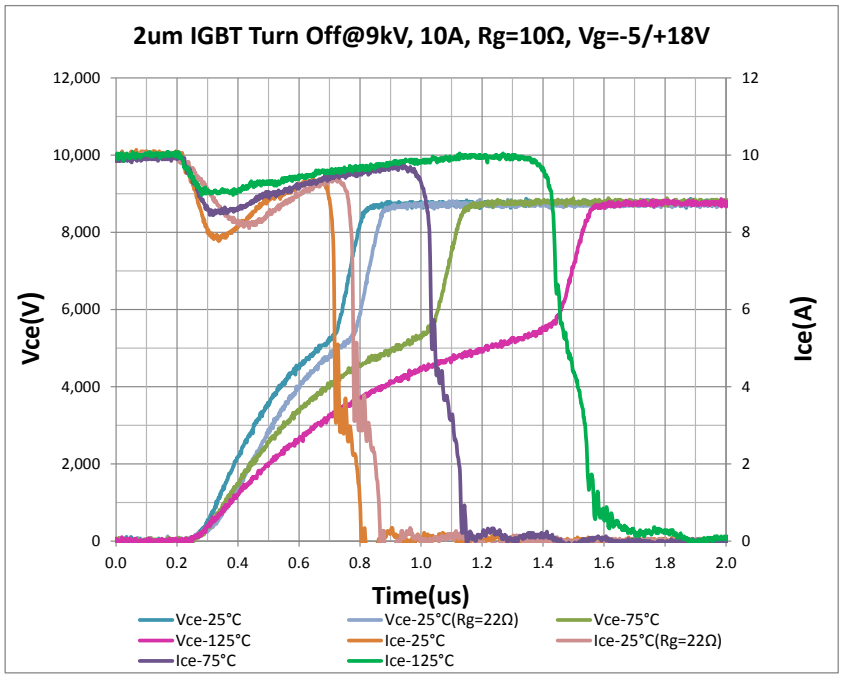



Figure 2.64: SiC IGBT with 2um Buffer Layer Turn off for Different Temperature

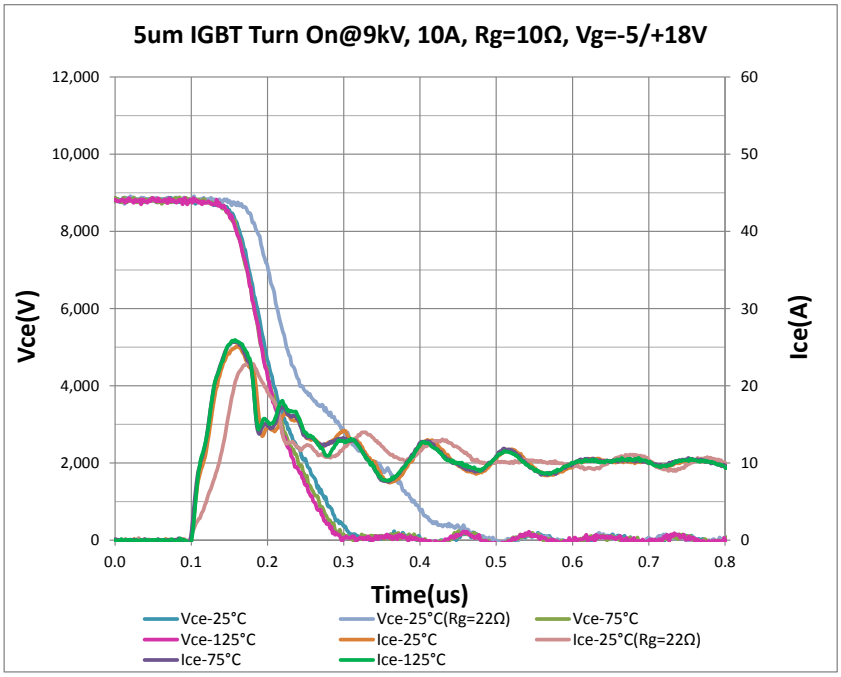



Figure 2.65: SiC IGBT with 5um Buffer Layer Turn on for Different Temperature

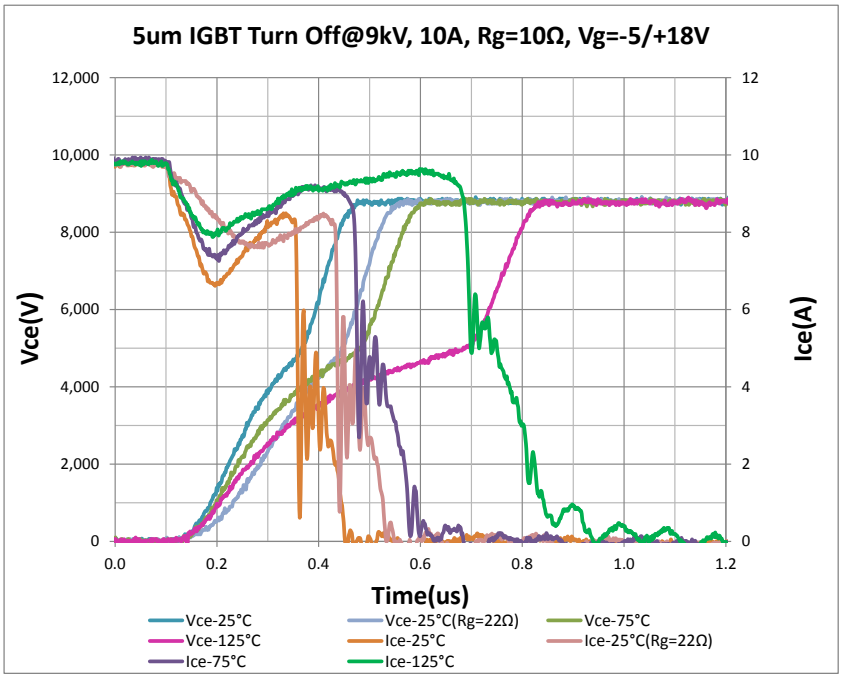



Figure 2.66: SiC IGBT with 5um Buffer Layer Turn off for Different Temperature

### 2.6.4 Switching Loss and Frequency Capability

Since the switching speed is different, the switching loss will be different for SiC MOSFET and SiC IGBTs. For the real application, the power devices usually operate under high junction temperature, it will be more reasonable to compare the switching transient for different devices under high junction temperature Figure 2.67 shows MOSFET and two IGBTs 9 kV 10 A turn on at 125 °C with the same gate driver circuit. It can be found that 2um buffer layer IGBT turns on faster then the other two, it has highest $di/dt$ as 2486 $A/us$, the $di/dt$ is 844 $A/us$ for the 5um buffer layer IGBT, and 479 $A/us$ for the MOSFET. The $dv/dt$ for these three devices are $-125kV/us$, $-92kV/us$, $-44kV/us$ respectively.

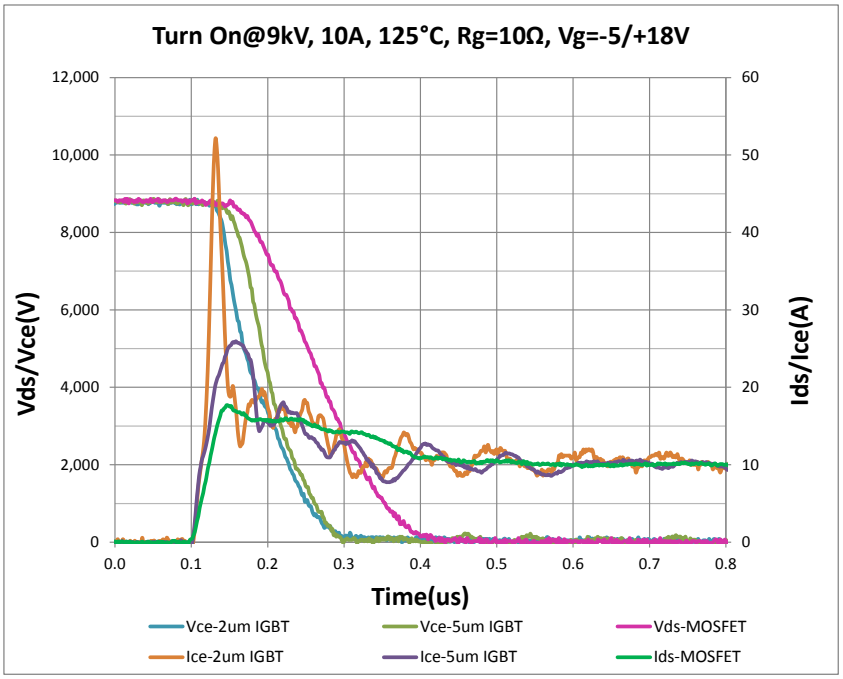



Figure 2.67: SiC IGBTs and MOSFET Turn on @ 125 °C

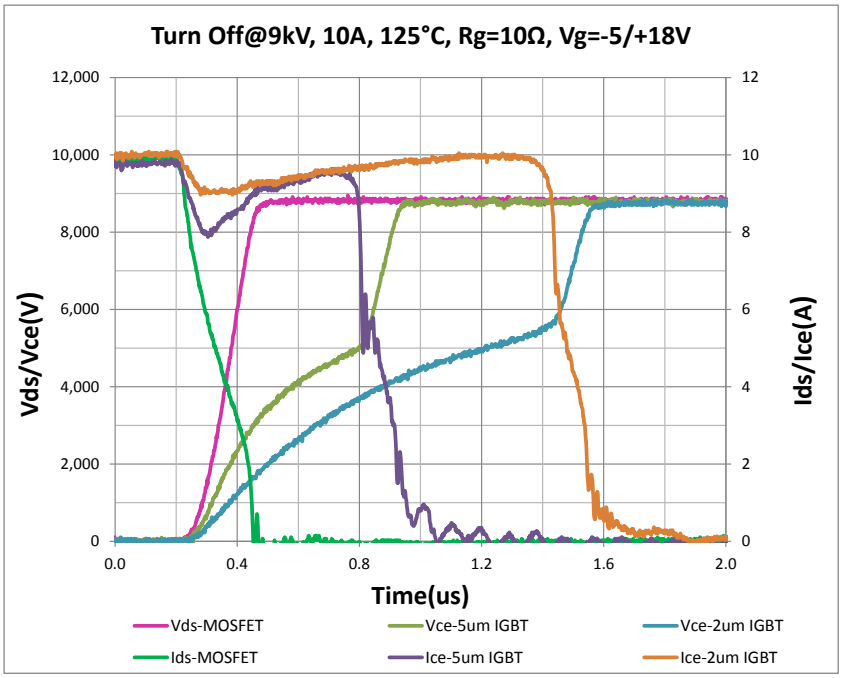



Figure 2.68: SiC IGBTs and MOSFET Turn off @ 125 °C

Figure 2.68 shows the 9 kV 10 A turn off for the three devices under 125 °C junction temperature. It is obviously that the MOSFET turns off much faster than the other two. Although the three device have almost the same $di/dt$, but the $dv/dt$ varies a lot from each other especially for the voltage lower than 5 kV.

Then turn on loss, turn off loss and total switching loss for the three devices under different current and different junction temperature have been plotted as Figure 2.69, Figure 2.70, Figure 2.71 respectively. As can be seen from Figure 2.69, both 5um buffer layer IGBT and 2um buffer layer IGBT have similar turn on loss which is also almost constant for the three temperatures 25 °C, 75 °C, and 125 °C. The MOSFET has more turn on loss than the two IGBTs, and the loss decreases as the junction temperature increases.

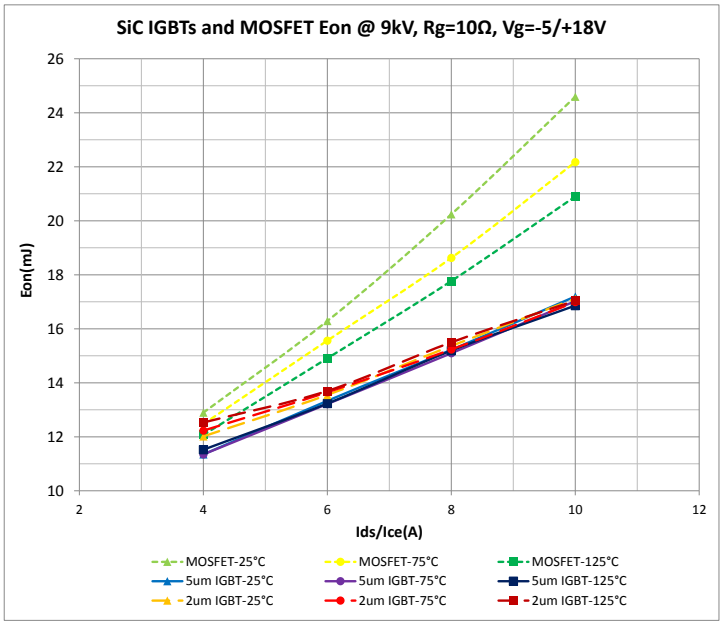



Figure 2.69: SiC IGBTs and MOSFET Turn on Loss

In Figure 2.70, the turn off loss for both 5um buffer layer IGBT and 2um buffer layer IGBT shows strong dependency on the junction temperature. the 2um buffer layer IGBT has highest switching.With 10 A current and 125 °C junction temperature, the loss is $45mJ$ compared with $21mJ$ for the 5um layer buffer IGBT and $2.5mJ$ for the MOSFET.

According to Figure 2.69 and Figure 2.70, the MOSFET has the higher turn on loss and lower turn off loss. The total switching for the three devices has been shown and compared in Figure 2.71. The total loss under 25 °C is close to each other for the three devices, while the difference is significant for 125 °C junction temperature. The MOSFET has the lowest total switching loss.

Based on the above analysis, SiC MOSFET has lower switching loss while SiC IGBTs have lower conduction loss for more than 3 A current with assumed 125 °C junction temperature, it should be valuable to investigate the switching frequency

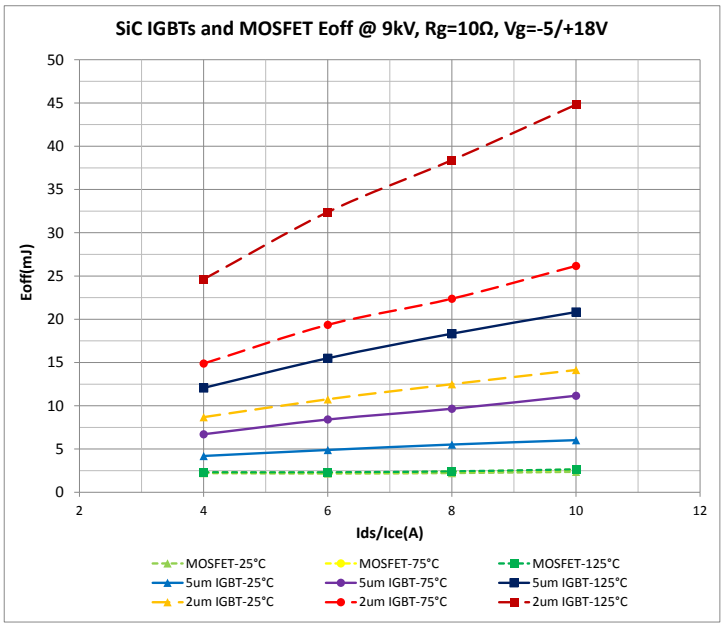



Figure 2.70: SiC IGBTs and MOSFET Turn off Loss

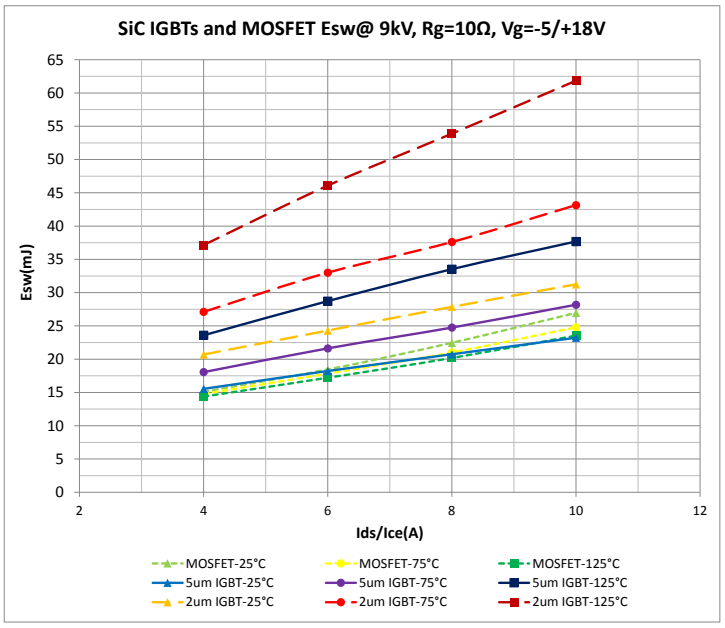



Figure 2.71: SiC IGBTs and MOSFET Total Switching Loss

capability for these devices under different load conditions. Considering a boost converter application with 4.5 kV input voltage and 9 kV output voltage, assume the inductor is large enough so the current ripple is negligible which means the power switch has a approximately square current waveform with 50% duty cycle. Assume the power dissipation capability is 100 W for all the three devices which gives about $300W/cm^2$ in term of power density for the active area. For a maximum junction temperature of 125 °C, the switching frequency capability of the SiC MOSFET and IGBTs has been plotted in Figure 2.72, the "x" axis current is the power device switching current which should be two times of the load current since the duty cycle is 50%. It can seen that SiC MOSFET has higher switching capability for current less than 9 A and 5um buffer layer IGBT has better performance than 2um buffer layer IGBT for the experiment case discussed above. The SiC MOSFET can switch at about 10 kHz with 1 A current under the hard switching conditions.

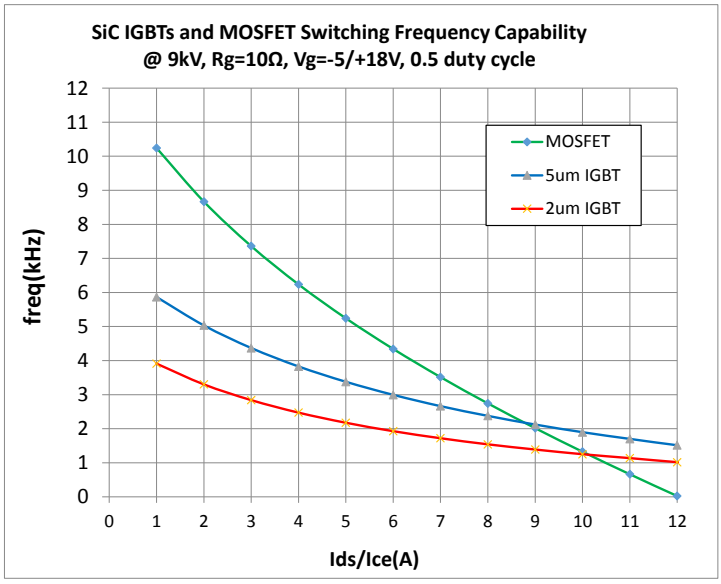



Figure 2.72: SiC IGBTs and MOSFET Switching Frequency Capability

# CHAPTER 3

# SST Rectifier Stage Design

## 3.1 Introduction

SST rectifier stage provides the front end interface with the distribution grid, which converts the sinusoidal AC voltage to DC voltage. In order to provide bidirectional power transfer capability, the SST rectifier stage has a full bridge configuration with four active power switches, so it can control the angle between the AC voltage and AC current. In other words, any combination of the active power and reactive power within the power rating limit can be transferred. Figure 3.1 shows the rectifier circuit consists of the for >13 kV SiC MOSFET. The first part of this chapter discuss the modulation methods for the full bridge rectifier and identify the most suitable one for the SST application, then the power device loss of the rectifier stage will be analyzed

and simulated with the MOSFET loss model given in chapter two. The experiment results will be given and compared with the simulation results. The simulation results for the 12 kV DC bus case has also been given.

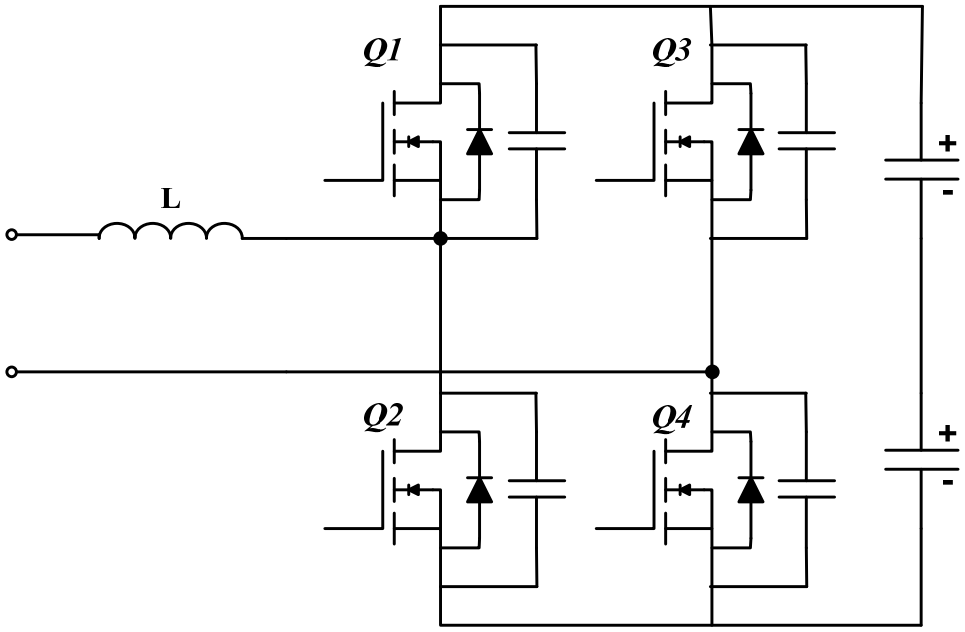



Figure 3.1: SST Rectifier Topology

## 3.2 Design of the Rectifier Stage

### 3.2.1 Continuous Current Mode (CCM) Rectifier Control

The sinusoidal pulse width modulation (SPWM) is the widely used control method of the full bridge rectifier or inverter, its basic principle can be divided as bipolar mode and unipolar mode. For the bipolar mode, the PWM voltage across the two midpoints of the full bridge will have both positive and negative values over half sinusoidal cycle

as shown in Figure 3.2, The diagonal switch $Q_1$ and $Q_4$ will have the same signal, and the other two will have the complementary signal. The basic control logic is: when the reference voltage is higher the carrier voltage, turn on the $Q_1$ and $Q_4$, otherwise turn them off. There are two drawbacks for this modulation method. One is the DC bus voltage utilization is low due to the negative voltage for the positive half sinusoidal cycle. The other one is switching loss is high, the PWM voltage frequency is only equals to device switching frequency.

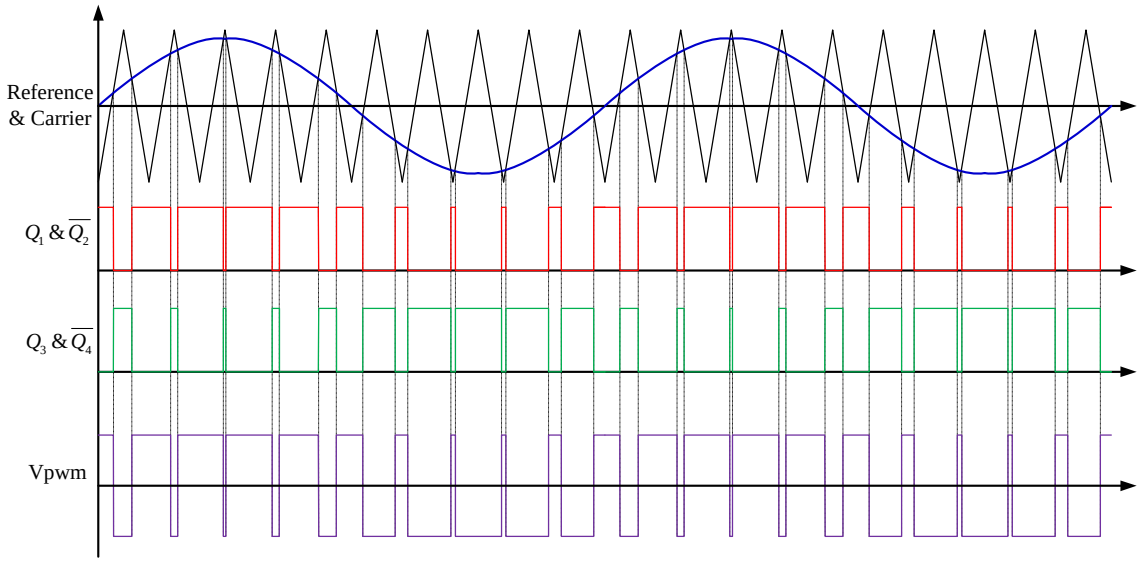



Figure 3.2: SST Rectifier Bipolar Pulse Width Modulation

For the unipolar modulation method, there are only two levels PWM voltage over one switching cycle, zero voltage and either positive or negative voltage. The unipolar double frequency modulation (Figure 3.3) has two references with 180° phase shift for the two half bridge legs separately, when the reference is higher than the triangle carrier, turn on the top device of the corresponded leg. The PWM voltage switching

frequency is two times of the power device switching frequency. The input voltage and current harmonic will be much lower compared with the bipolar modulation method. For each reference voltage cycle, the power device switches under hard switching condition for a half cycle, while switches under soft switching condition for the another half cycle where current flows from the source terminal to the drain terminal.

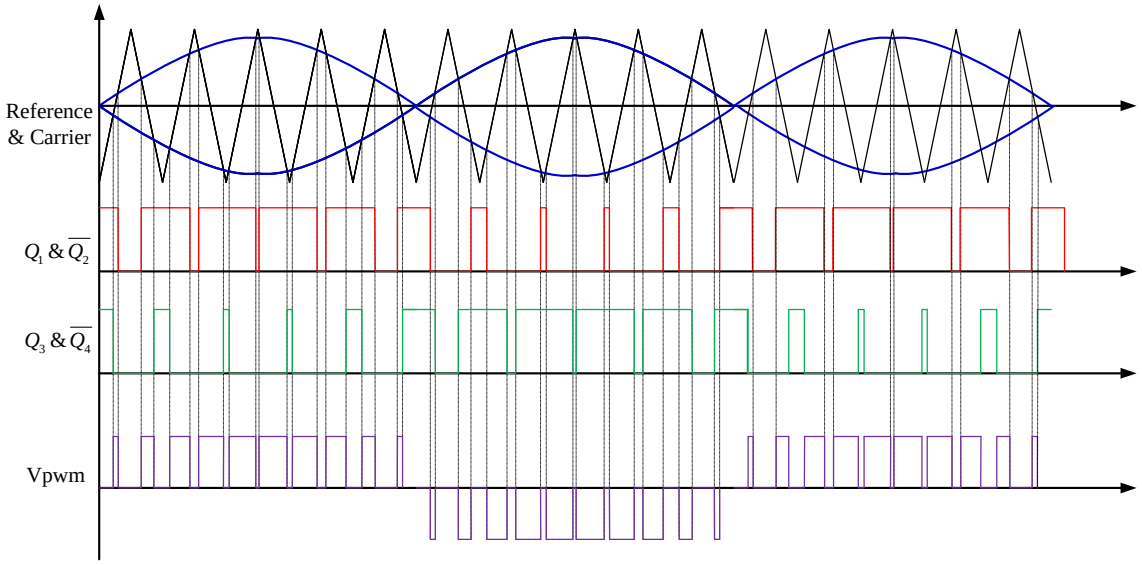



Figure 3.3: SST Rectifier Unipolar Double Frequency Pulse Width Modulation

The unipolar single frequency modulation method has only one voltage reference and control one high frequency switched leg, the other leg will be switched at the voltage reference frequency as show in Figure 3.4. In this case, the PWM voltage switching frequency equals to the high frequency switched power device switching frequency. The high frequency switched leg will rotate for each voltage reference cycle.

For the high voltage SiC MOSFET based rectifier, the unipolar single frequency

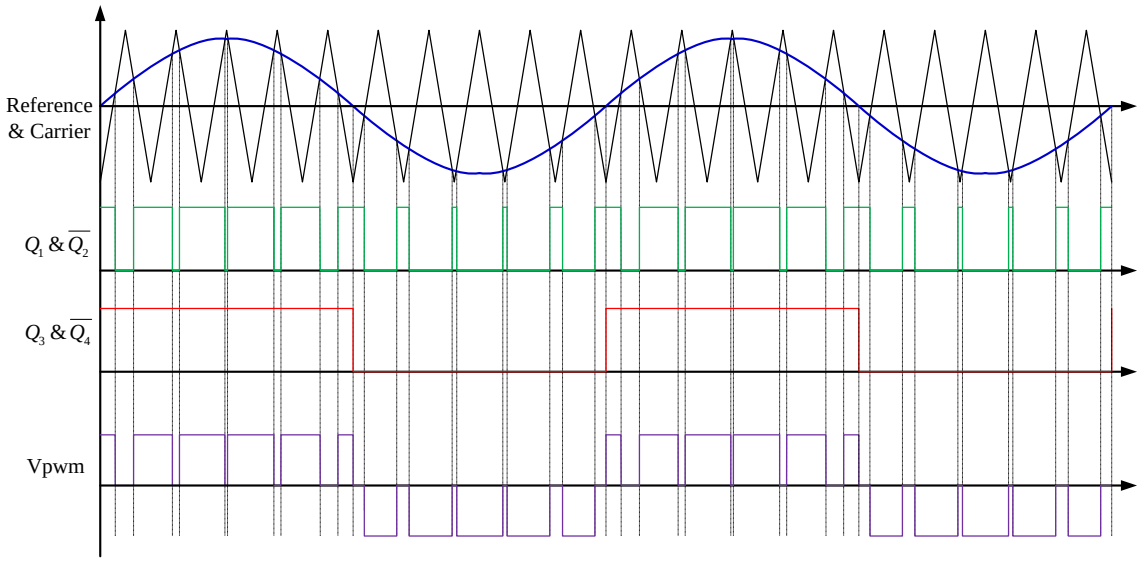
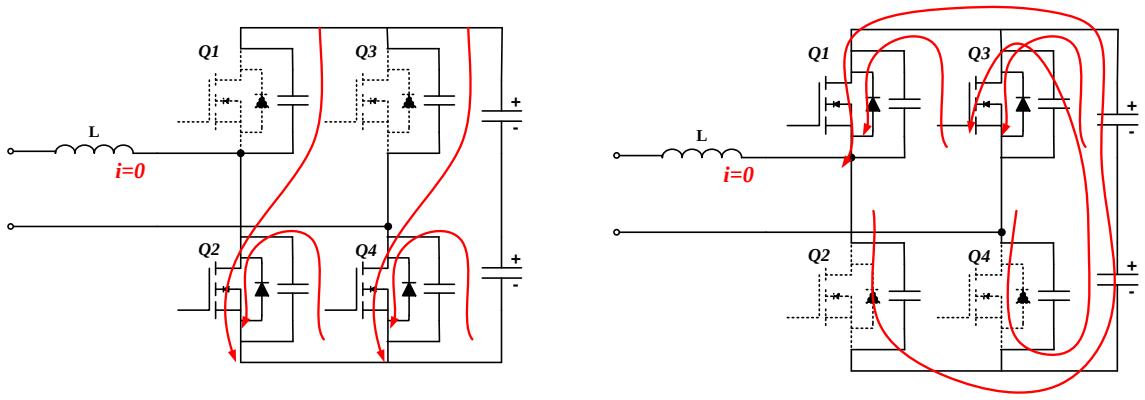



Figure 3.4: SST Rectifier Unipolar Single Frequency Pulse Width Modulation

modulation is the most suitable control method. Due to the MOSFETs output capacitance, which requires a large amount of energy to charge and dischange. However, the inductor current is very low when the input current is close to the zero crossing, and the output PWM voltage should be zero. There are two switch status cases for generating a zero PWM voltage: 1) Q1, Q3 are off and Q2, Q4 are on; 2) Q2, Q4 are off and Q1, Q3 are on. During zero voltage crossing, the power devices will switch between these two cases as shown in Figure 3.5, then capacitive switching loss will be generated.

When applying the unipolar single frequency method, the minimum on time control can be added in order to reduce the switching cycles where the reference voltage is close to the zero crossing.




(a) (b)

Figure 3.5: MOSFET Switching During Current Zero Crossing for Unipolar Double Frequency Pulse Width Modulation

### 3.2.2 Power Device Loss for the Rectifier

For the unipolar single frequency SPWM modulated rectifier which operates under continuous current mode, the SiC MOSFET will be switched under hard switching condition for only one fourth of the PWM voltage equivalent frequency. With a 12 kHz PWM voltage, the MOSFET switches 3000 cycles for hard switching, and 3000 cycles for soft switching. It will be kept on or off status for the other half time period (6000 cycles equivalent) synchronized with the line frequency.

$$t_n = \frac{T}{2} \times \frac{n}{N_{sw}}, N_{sw} = \frac{f_{sw}}{f_{grid}}, n = 1, 2, ..., (N_{sw} - 1) \tag{3.1}$$

$$P_{total} = \frac{1}{4} \cdot (\sum_{n=1}^{N_{sw}-1} E_{on,n}) \cdot f_{grid} \tag{3.2}$$

With the >13 kV SiC MOSFET loss model discussed in Chapter 2, the SST rectifier stage power devices loss has been simulated for both the 6 kHz (Figure 3.6) and 12

kHz (Figure 3.7) switching frequency under different load, it can be seen that the conduction loss is proportional to the load, while The switching loss is proportional to the switching frequency. The switching loss is high even for the light condition which is caused by the high energy loss of the MOSFET output capacitor. The conduction loss will not be affected by the different switching frequency but only determined by the load.

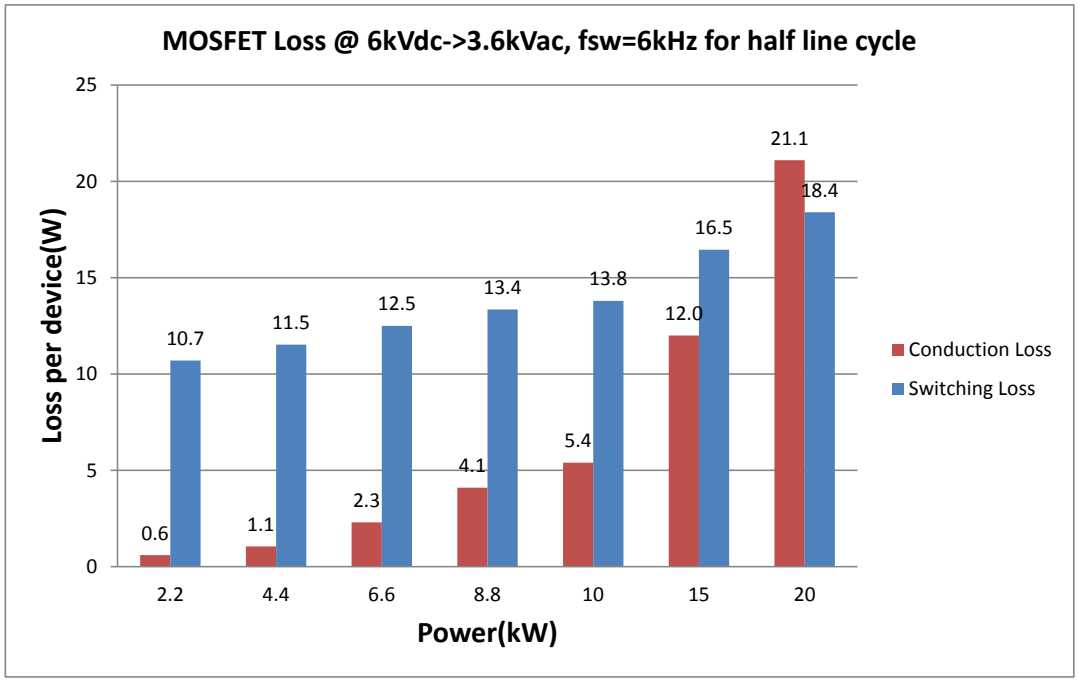



Figure 3.6: Rectifier MOSFET Loss with Unipolar Single Frequency Pulse Width Modulation (6 kHz)

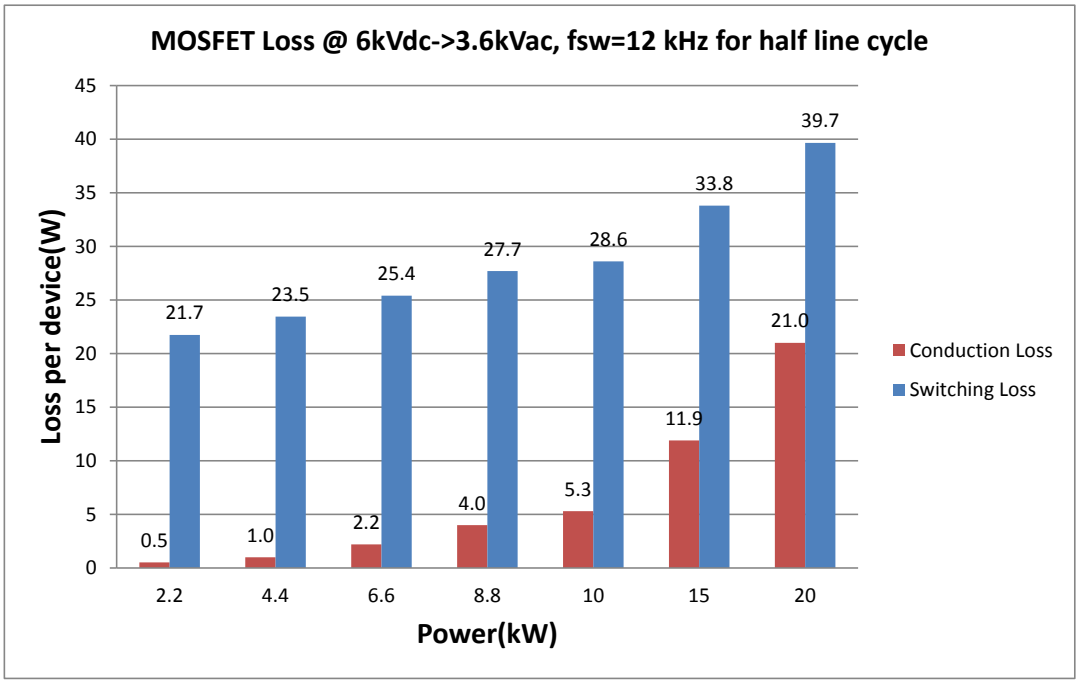



Figure 3.7: Rectifier MOSFET Loss with Unipolar Single Frequency Pulse Width Modulation (12 kHz)

### 3.2.3 Rectifier Filter Design

1. Harmonics of PWM

The current from grid is limited by IEEE 1547, as show in Table 3.1. The low order harmonic is decided by many factors, such as control scheme, grid voltage distortion, dead-time of PWM and filter. However the high order harmonic is mainly decided by the filter and PWM scheme.

As shown in Figure 3.8, grid current $i_g$ is presented by:

$$i_g(s) = (u_g(s) - u_r(s))H_f(s) \tag{3.3}$$

Where $H_f(s)$ is the transfer function of filter. $u_g$ can be neglected when we consider

Table 3.1: Harmonic Limitation for Grid Connected Inverter in IEEE 1547

| Individual harmonic order h (odd harmonics)[b] | h < 11 | 11 ≤ h < 17 | 17 ≤ h < 23 | 23 ≤ h < 35 | 35 ≤ h | Total demand distortion (TDD) |
|---|---|---|---|---|---|---|
| Percent (%) | 4.0 | 2.0 | 1.5 | 0.6 | 0.3 | 5.0 |

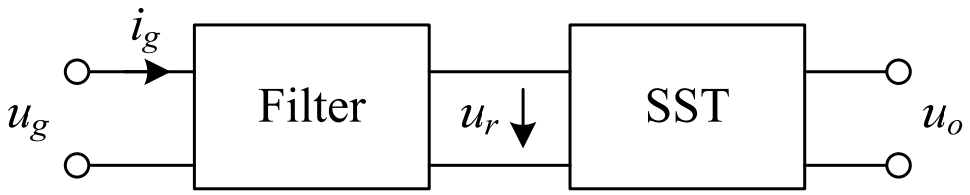



Figure 3.8: Diagram of the Input Filter for SST

high order harmonics. So frequency response if $i_g$ is:

$$i_g(j\omega) = u_r(j\omega)H_f(j\omega) \tag{3.4}$$

$u_r$ is the voltage of rectifier side, which is difficult to represent mathematically but it is possible to estimate by simulation. Based on the SST topology and the corresponding control scheme, the wave of $u_r$ $u_g$ and $i_g$ are shown in Figure 3.9, and the FFT of $u_r$ is show in Figure 3.10. Here switching frequency is 6 kHz, DC voltage is 6 kV, grid voltage is 3600 V.

Estimate the total harmonics of $u_r$ from 5700Hz 630000Hz

$$u_{rh1} = u_{r1}\sqrt{2 * 0.34^2 + 2 * 0.19^2 + 2 * 0.019^2} = 3600 * 0.551 = 1983.6V \tag{3.5}$$

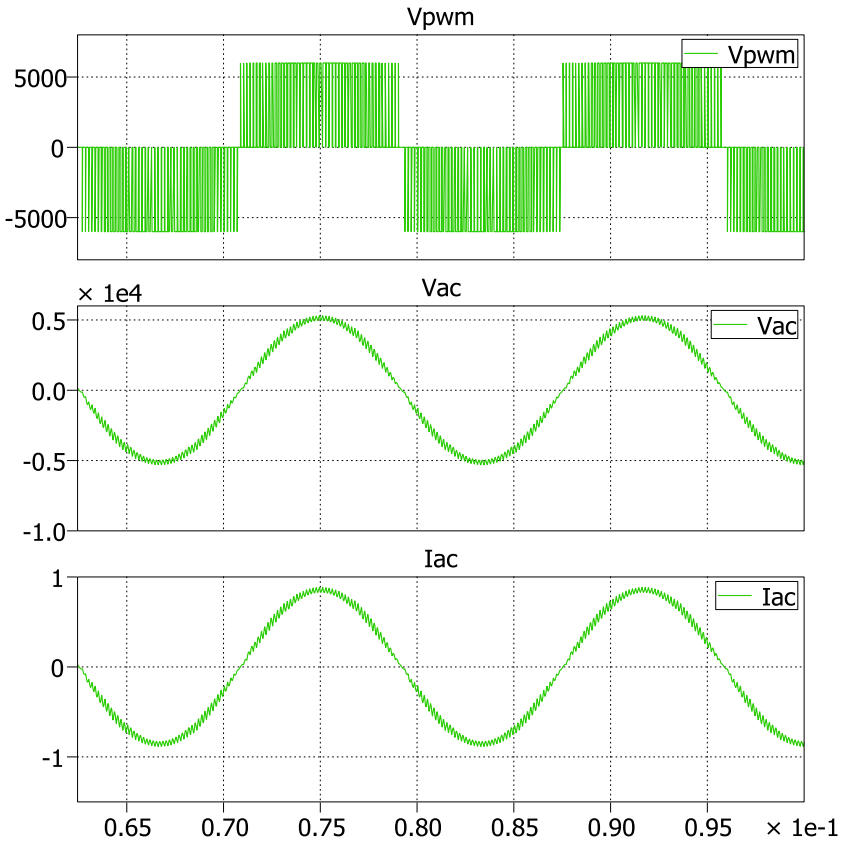



Figure 3.9: Simulation Waveforms of the CCM Rectifier

The grid current for 20 kW SST is:

$$i_{g1} = P/\eta u_{g1} = 10000/(0.95 * 3600) = 2.93A \tag{3.6}$$

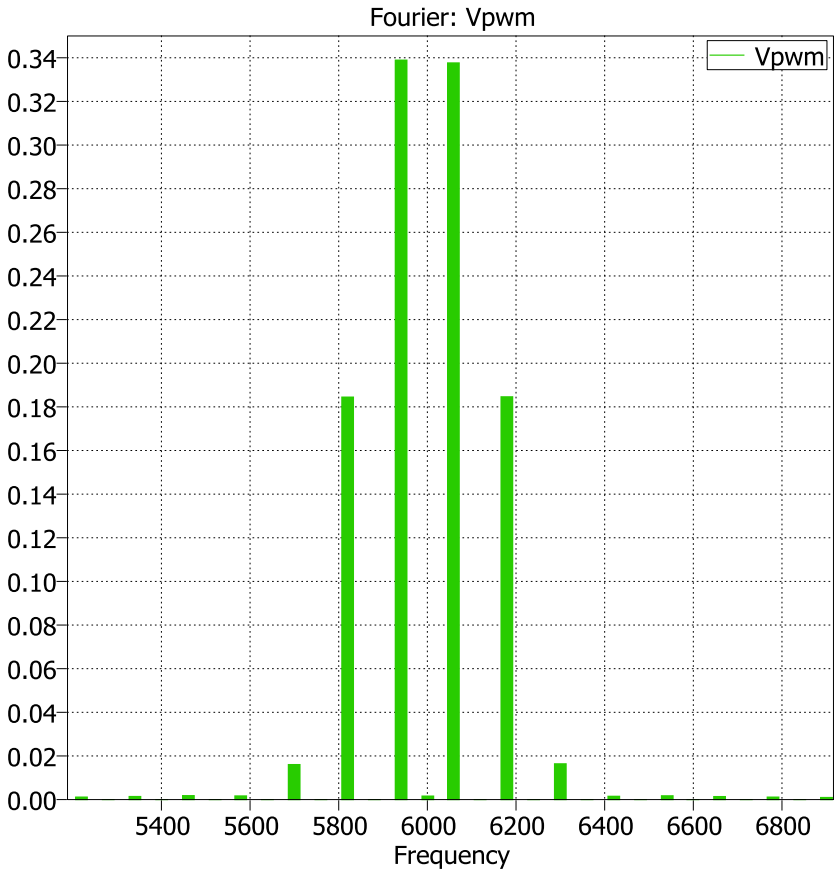



Figure 3.10: FFT Spectrum of the PWM Voltage $u_r$

To meet the IEEE 1547, the current harmonics from 6000 7000 are limited in 0.3%, it is:

$$i_{gh1} < 0.003 * i_{g1} = 0.003 * 2.93A = 0.0088 \tag{3.7}$$

So the average attenuation of filter in 5700 Hz 6300 Hz should be:

$$H_{fh1} < 0.0088/1983.6 = 1/225409 = -107dB \tag{3.8}$$

2. Single L filter design

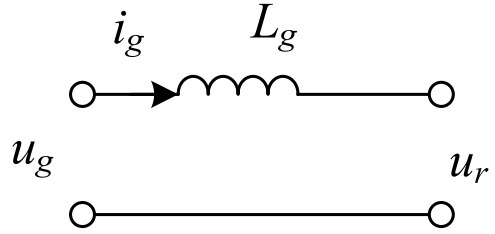



Figure 3.11: L Filter

The transfer function is

$$H_l(s) = \frac{1}{sL_g} \tag{3.9}$$

The attenuation of L- filter is

$$H_l(j\omega) = \frac{1}{j\omega L_g} \tag{3.10}$$

So,

$$|H_l(2 \cdot \pi \cdot f)| = |\frac{1}{j2 \cdot 3.14 \cdot 6000 \cdot L_g}| < \frac{1}{225409} \tag{3.11}$$

Then $L_g > 5.982H$

3. LCL filter design

The rules of LCL design are:

a) Peak-peak current of switching frequency in $L_r$ is 20% of maxim current;

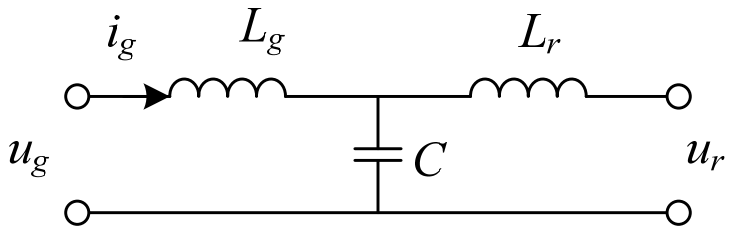



Figure 3.12: LCL Filter

b) Passive current in $C$ is small than 5% of nominal current;

c) Grid current, $i_g = 2.93A$ (max:4.14 A).

So the inductor in rectifier side $L_r$ can be calculated as:

$$L_r = \frac{U_L D}{2 \cdot \Delta I_p} = \frac{(U_{dh}/2)(T_s/2)}{2 \cdot \Delta I_p} = \frac{3000 \times 0.0005}{2 \times 6 \times 0.83} = 0.15H \tag{3.12}$$

Let $L_r = 0.3H$ $Ip$ is the peak-peak current of switching frequency in $L_r$. $Ip = 20\% of 4.14 = 0.83A$

Filter Capacitor $C$ will be:

$$C_l = \frac{i_q}{2\pi f_b u_s} = \frac{2.93 \times 5\%}{2 \times 3.14 \times 60 \times 3600} = 110.4nF \tag{3.13}$$

Where $i_q$ is passive current, $i_q = 5\% * 2.93 = 0.15$ Inductor in grid side $L_g$ To meet the attenuation of filter: $H_{fh1} < 1/409090 - 112DB$ The transfer function of LCL is

$$H_{lcl}(s) = \frac{1}{s^3 L_r L_g C + s(L_r + L_g)} \tag{3.14}$$

Let $L_g = 0.27H$, the frequency response is shown in Figure 3.13, it is -107 db at 6000Hz. So the parameters of LCL filter are: $L_g = 0.15H$, $L_r = 0.27H$, $C = 110.4nF$. The total inductance is reduced from $6H$ to $0.42H$ to meet IEEE 1547.

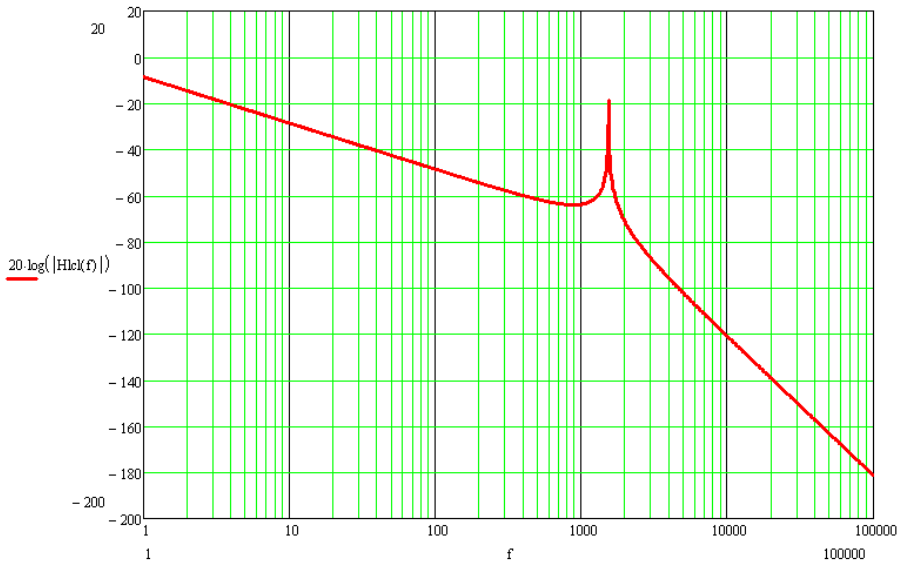



Figure 3.13: Frequency Response of the LCL Filter

## 3.3 Experiment Results

The rectifier stage has been operated under inverter mode or the energy injection mode for the SST, it has been supplied from the DC side and the output is AC voltage. Figure 3.14 shows a typical waveform for 6 kW load, 6 kVdc input and 3.6 kVac output, the switching frequency is 6 kHz with the unipolar single frequency modulation method.

The efficiency has been measured for different load conditions and two different switching frequency 6 kHz and 12 kHz. Base on the SiC MOSFET loss developed in Chapter 2, the rectifier efficiency has also been simulated for the same conditions as the experiment. Both the results have been plotted in Figure 3.15. It shows a good match between the experiment and simulation.

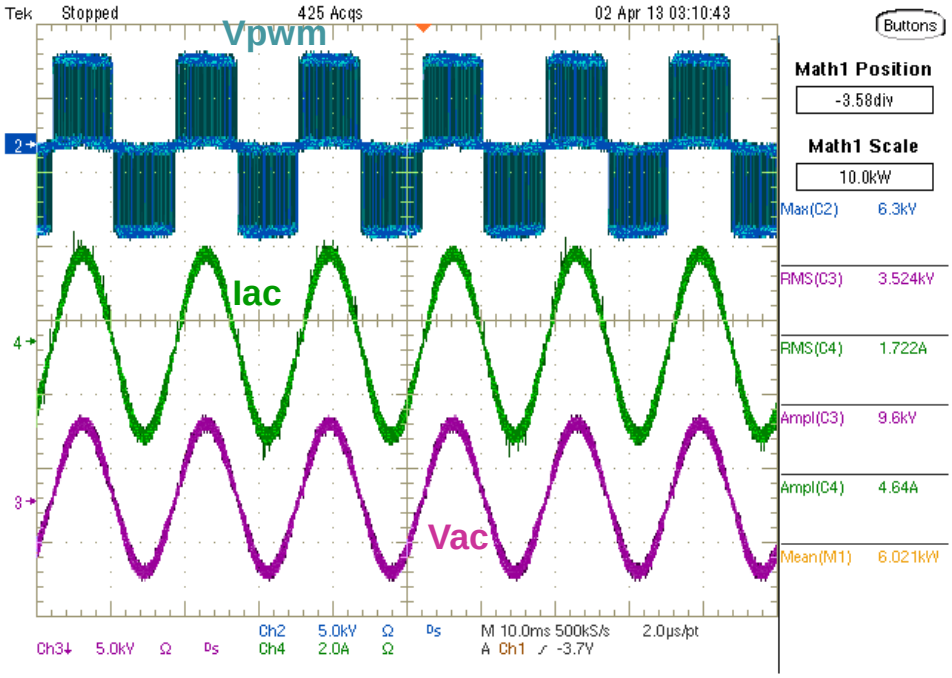



Figure 3.14: Rectifier Stage Steady State Waveforms

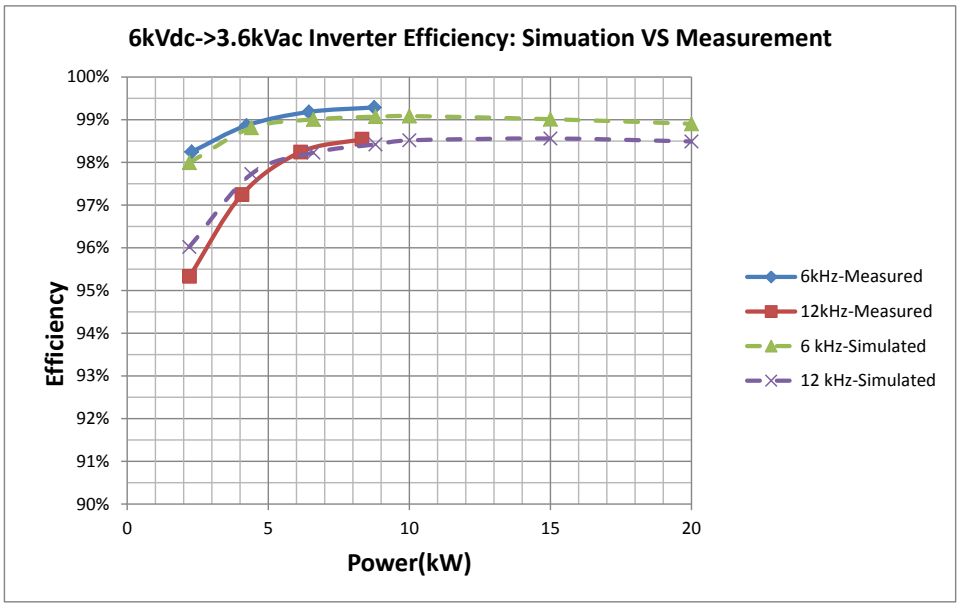



Figure 3.15: Rectifier Stage Efficiency: Measurement vs Simulation

## 3.4 Rectifier Loss Simulation for 12 kV DC bus

Due to the safety concern, the rectifier stage has not been tested up to 12 kV DC bus voltage. With the SiC MOSFET loss model, the rectifier loss and efficiency can still be estimated based on the simulation by using Simulink/PLECS. Figure 3.16 shows the simulated efficiency for both 6 kHz and 12 kHz switching frequency. The efficiency is more than 99% for heavy load with 6 kHz switching frequency, while the efficiency will drop to 99% for 5 kW load. The simulated loss breakdown has been plotted in Figure 3.17 for 6 kHz and in Figure 3.18 for 12 kHz. It can be found that the switching loss dominates the total loss.

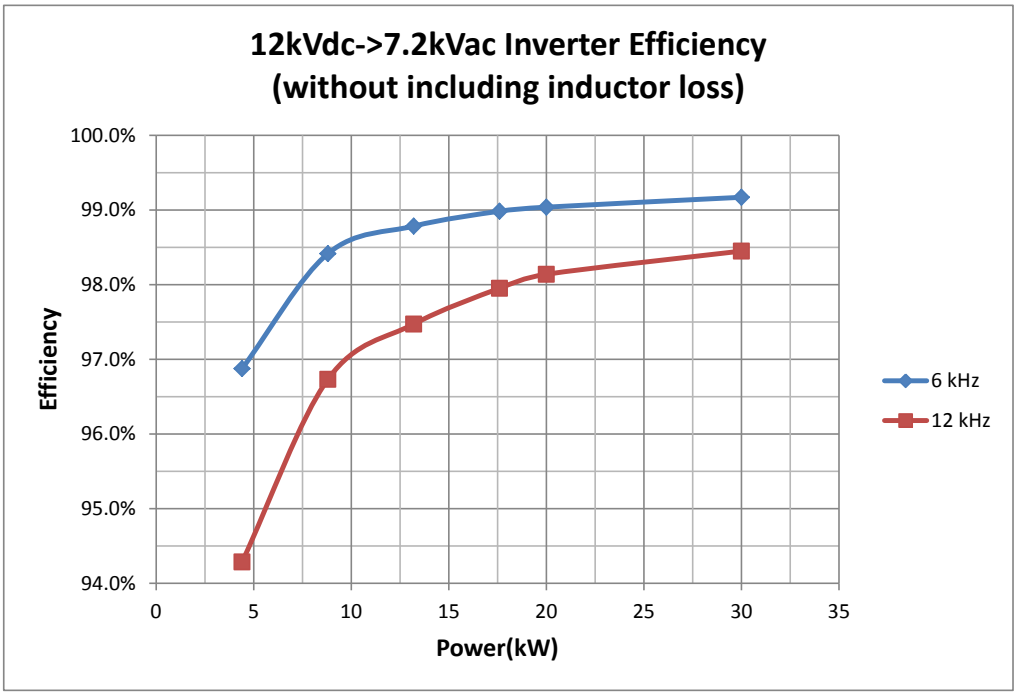



Figure 3.16: Rectifier Simulated Efficiency for 12 kV DC bus (Without Including Inductor Loss)

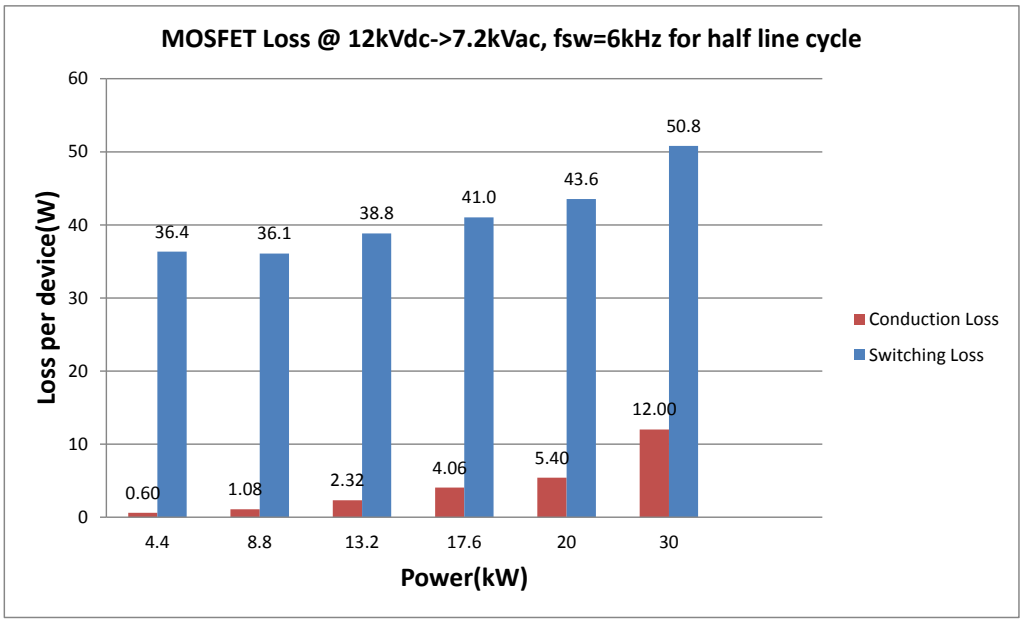



Figure 3.17: Rectifier Simulated Loss Breakdown for 12 kV DC bus, 6 kHz Switching Frequency

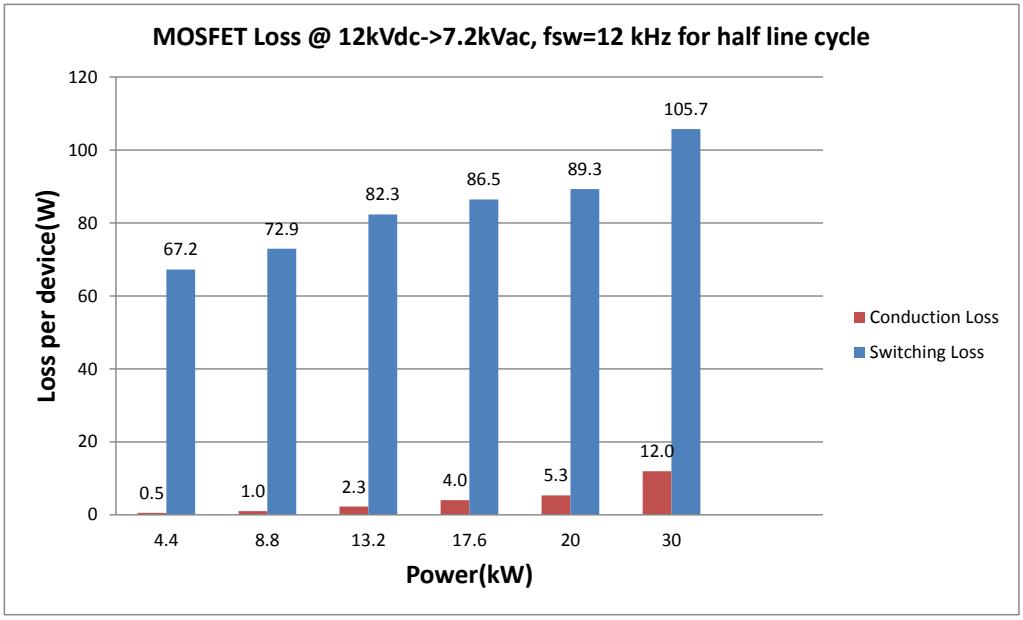



Figure 3.18: Rectifier Simulated Loss Breakdown for 12 kV DC bus, 12 kHz Switching Frequency

# CHAPTER 4

# SST DC-DC Stage Design

## 4.1 Introduction

The SST DC-DC stage steps down the high DC voltage to low DC voltage and required bidirectional power transfer capability. Dual active bridge (DAB) is a good candidate topology for its symmetric structure and the zero voltage turn on for all power device, it utilizes the transformer leakage inductance L as a buck or boost inductor to step up or step down the input voltage. For the SST application which has high input voltage and low input current, the full bridge can be changed as half bridge considering the current capability of the >13 kV SiC MOSFET. The dual half bridge (DHB) (Figure 4.1) will have automatic transformer flux balance characteristic since the split capacitor bridge can block the DC component of the magnetizing current and also has less

power devices. There are several different control method for the DAB as discussed in [30, 29, 1, 31, 5, 16, 4, 23], but for the DHB, the both input and output have a fixed 50% duty cycle, the only controllable parameter is the phase shift angle between the two legs [48, 17]. Two >13 kV SiC MOSFETs will be used for the high voltage side and 1200 V 100 A SiC MOSFET module will be used for the low voltage side. In this chapter, the soft switching ranges will be analyzed at first followed by the high frequency transformer design. The method to extend the zero voltage switching (ZVS) range under light load will be proposed. For the high voltage application, the parasitic capacitance will play an importer role on the power device switching transient. The transformer parasitic capacitance will be measured and its impact will be considered. Finally, the simulation and experiment results will be given.

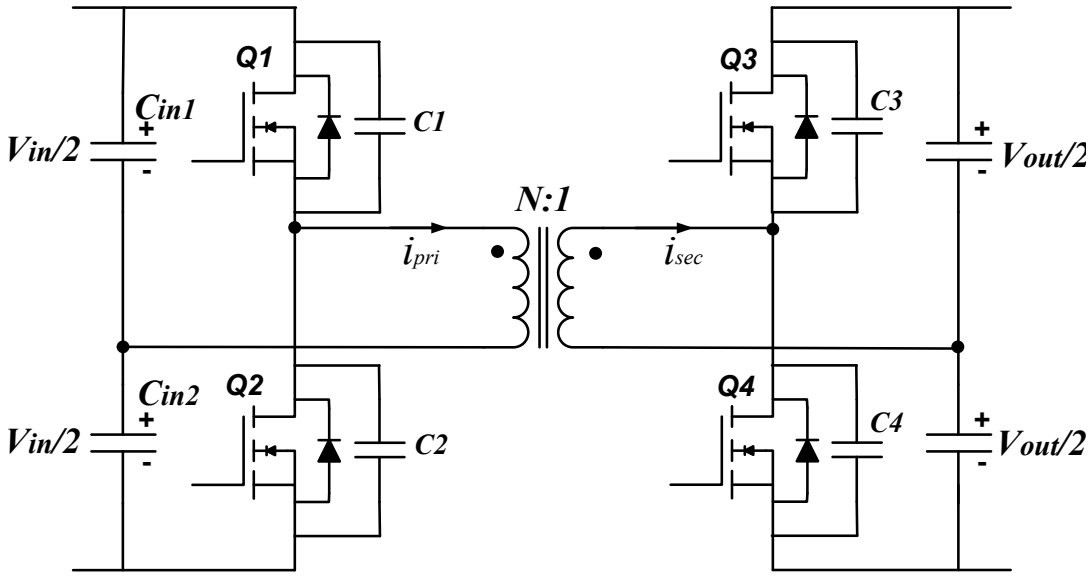



Figure 4.1: DHB Topology

## 4.2 Dual Active Half Bridge (DHB) ZVS Range Analysis and Extension Method

The Dual Active Half Bridge (DHB) (Figure 4.1) is operated under soft switching to minimize the turn on losses similar as DAB. The transformer can be transformed as the equivalent circuit shown in Figure 4.2, all secondary parameters are reflected to the primary, and $C_1$, $C_2$, $C_2$, $C_2$ stands for equivalent output capacitance for each power device.

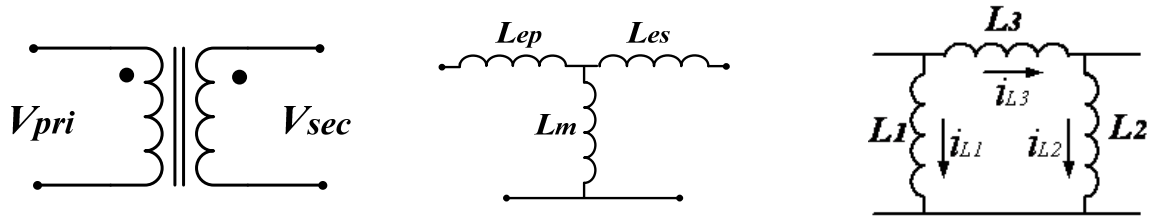



Figure 4.2: Transformer Equivalent Circuit

The current and the voltage waveforms through the transformer are shown in Figure 4.3 and the operation of the DHB can be divided into 12 stages:

[t0, t1]: $Q_1$, $Q_3$ is on, energy transferred from primary to secondary;

[t1, t2]: $Q_1$ turn off at t1, the resonant between $C_1$, $C_2$, $L_1$, $L_3$ will pull the $V_{ds}$ for Q2 to 0V;

[t2, t3]: at t2, the anti-parallel diode for $Q_2$ will conduct until $Q_2$ turn on at t3;

[t3, t4]: $Q_2$, $Q_3$ is on; the primary current will decrease from positive to negative;

[t4, t5]: $Q_3$ turn off at t4, the resonant between $C_3$, $C_4$, $L_2$, $L_3$ will pull the $V_{ds}$ for $Q_4$ to 0V;

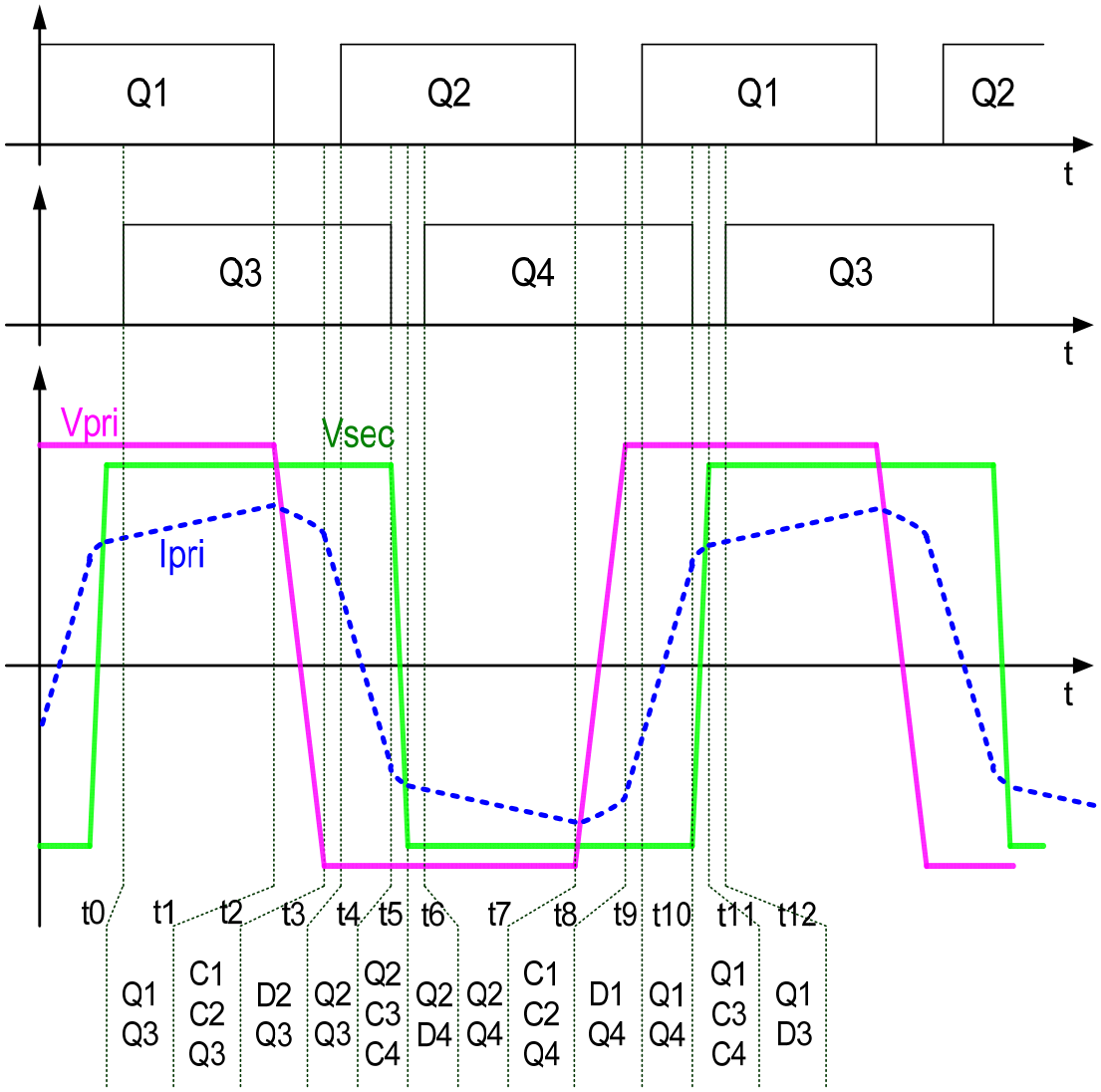



Figure 4.3: DHB Steady State Operation Waveforms

[t5, t6]: at t5, the anti-parallel diode for $Q_4$ will conduct until $Q_4$ turn on at t6;

[t6, t7]: $Q_2$, $Q_4$ is on, energy transferred from primary to secondary;

[t7, t8]: $Q_2$ turn off at t7, the resonant between $C_1$, $C_2$, $L_1$, $L_3$ will pull the $V_{ds}$;

[t8, t9]: at t8, the anti-parallel diode for $Q_1$ will conduct until $Q_1$ turn on at t9;

[t9, t10]: $Q_1$, $Q_4$ is on; the primary current will increase from negative to positive;

[t10, t11]: $Q_4$ turn off at t10, the resonant between $C_3$, $C_4$, $L_2$, $L_3$ will pull the $V_{ds}$ for $Q_3$ to 0V;

[t11, t12]: at t11, the anti-parallel diode for $Q_3$ will conduct until $Q_3$ turn on at t6;

Without considering the deadtime, transformer magnetizing inductance and device switching time, the DHB output power can be expressed as:

$$Po = \frac{V_{in} \cdot n \cdot V_{out}}{4 \cdot \pi \cdot f \cdot Le} \cdot \varphi \cdot (1 - \frac{|\varphi|}{\pi}) \tag{4.1}$$

Where $V_{in}$ , $V_{out}$ is the input and output voltages separately, $f$ is the switching frequency, $L_e$ is the transformer leakage inductance, $\varphi$ is the phase shift angle between the input and output half bridge legs. The current waveform is given by the following equation:

$$i_p(\theta) = \frac{\left[v_p(\theta) - v_s(\theta)\right]}{\omega L} (\theta - \theta_i) + i_p(\theta_i) \tag{4.2}$$

Using this equation, we enforce ZVS condition for the input and output bridges:

And, we get the following constraints given $d = n \cdot V_{out}/V_{in}$:

The ZVS range boundary can be plotted as in Figure 4.4 under different shift angle and output power. However, the deadtime between power switches will reduce the ZVS range as the Figure 4.4 shows, which considers 2 us deadtime for the high voltage side and 1 us for the low voltage side. On the other hand, the transformer magnetizing

current can help increase the ZVS range

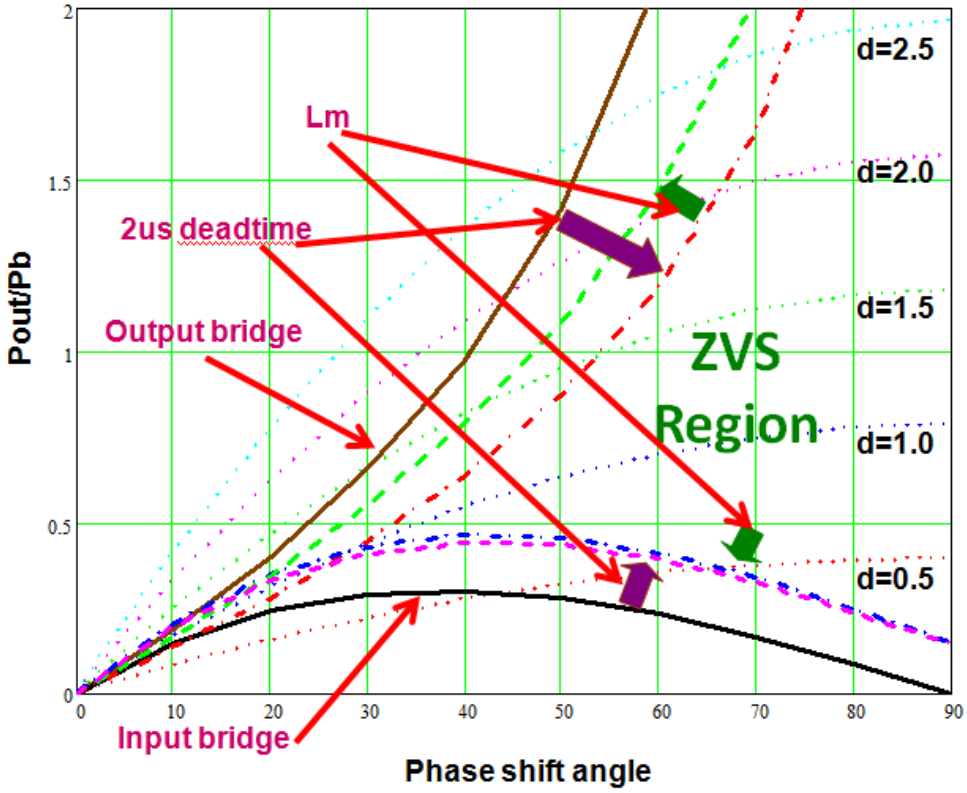



Figure 4.4: DHB ZVS Range

The resonance between magnetizing inductor, leakage inductor and $C_1$ - $C_4$ during the transient [t1, t2], [t4, t5], [t7, t8], [t10, t11] determines the MOSFET turn on voltage. Take mode [t1, t2] for example. $Q_1$ turn off at t1, the resonant between inductors and capacitors will start and the Vds(t) for $Q_2$ can be solved through Laplace Transforms, the result is :

$$V_{ds\_Q2}(t) = V_{in} - (i_{L1} + i_{L3})\frac{L_1 \cdot L_3}{(L_1 + L_3)}\sqrt{k} \cdot \sin(\sqrt{k} \cdot t) - \frac{L_3 \cdot V_{in}}{2 \cdot (L_1 + L_3)} \cdot (1 - \cos(\sqrt{k} \cdot t)) \tag{4.3}$$

Where $k = \sqrt{\frac{L_1+L_3}{(L_1 \cdot L_3)\cdot(C_1+C_2)}}$. Assume $i_{L3}(t1) \approx 0$ for DHB under no load condition, $L_1$ current at t1 can be estimated:

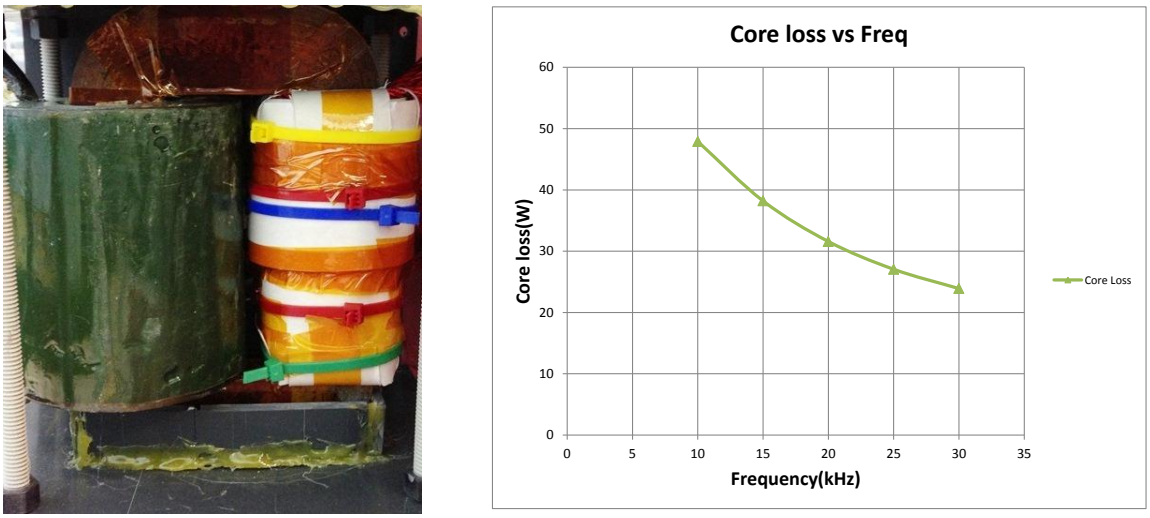
$$i_{L1}(t_1) \approx \frac{V_{in}}{8 \cdot f \cdot L_1} \tag{4.4}$$

According to Eq. 4.1, Eq. 4.3, and Eq. 4.4, $L_1$ and $L_3$ can be chosen through a try and trial method so that the inductor current can pull down the $Q_2$ $V_{ds}$ to 0V during the deadtime. Similarly, the $L_2$ can be chosen by analyzing the resonant transient for $Q_3$ and $Q_4$ during [t10, t11].

## 4.3 High Frequency Transformer Design

The high frequency transformer in the DC-DC stage in solid state transformer plays an important role for the performance and overall efficiency of the SST system. There are two challenges for the SST DHB transformer design, one is the high voltage insulation, and the other one is the integration of the leakage inductor as the resonant inductor which determines the power transfer capability[14]. The leakage and magnetizing inductance depends on the transformer geometry, turns and winding method. Considering a relative large leakage inductance is desired and the high voltage insulation between primary and secondary, a U core with the two winding on each leg has been chosen as the base transformer geometry. There are several types of magnetic core material usually considered for the high frequency transformer including amorphous alloy, nanocrystalline and ferrite. Amorphous alloy has lowest price, but its core loss will increase significantly for frequency more than 10 kHz. Ferrite core can operates under very high frequency but its saturation flux density is low. Nanocrystalline core

has both high saturation flux density and low core loss for high frequency, it is the most suitable core the SST DHB application which has a switching frequency range from 10 kHz to 20 kHz. Flux density and core loss is the key trade-offs to design transformers. With high flux density can reduce size, weight and the number of turns, but it also leads to high core loss. The final maximum flux density has been chosen as 0.3T with 20 kHz switching frequency for reducing the core loss. The Table 4.1 summaries the design results and Figure 4.5 (a) shows the prototype. The core loss has been measured for different frequency with 50% duty cycle square wave voltage input from the low voltage side, the voltage amplitude is 400V and the result is plotted in Figure 4.5 (b).




(a) (b)

Figure 4.5: DHB High Frequency and High Voltage Transformer Prototype (a) and Core Loss (b)

Table 4.1: DHB Transformer Design Parameters

| | 10kHz | 15kHz | 20kHz |
|---|---|---|---|
| Bac | 0.6 | 0.45 | 0.3 |
| Cross-section Area, Ac (cm^2) | 10.9 | | |
| Effective Cross-section Area, Ae (cm^2) | 8.93 | | |
| Window Area, Wa (cm^2) | 56.6 | | |
| # of turns on HVS | 150 | | |
| # of turns on LVS | 10 | | |
| HV winding Rac (ohm) | 0.786 | 0.974 | 1.137 |
| LV winding Rac (mohm) | 4.11 | 4.23 | 4.4 |
| Magnetizing Inductance (mH) | 228 | | |
| Leakage Inductance(reflected to HVS)(mH) | 7.4 | | |

## 4.4 Simulation Verification of the ZVS Range

The DHB design has been validated through the simulation which proves soft switching can be achieved for full load as shown in Figure 4.6 and Figure 4.8, and for no load cases shown in Figure 4.7 and Figure 4.9.

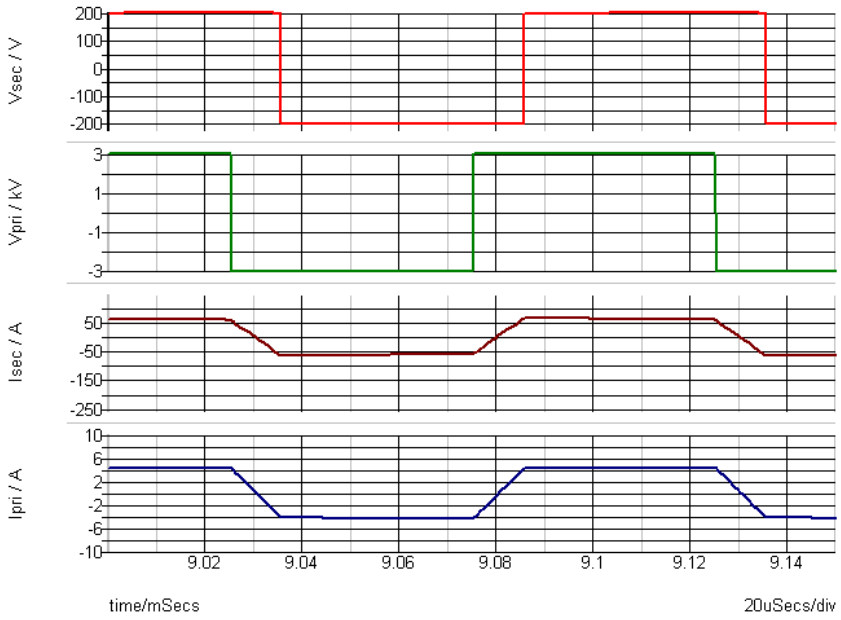



Figure 4.6: Transformer Voltage and Current for 10 kW Full Load with 228 mH Magnetizing Inductance

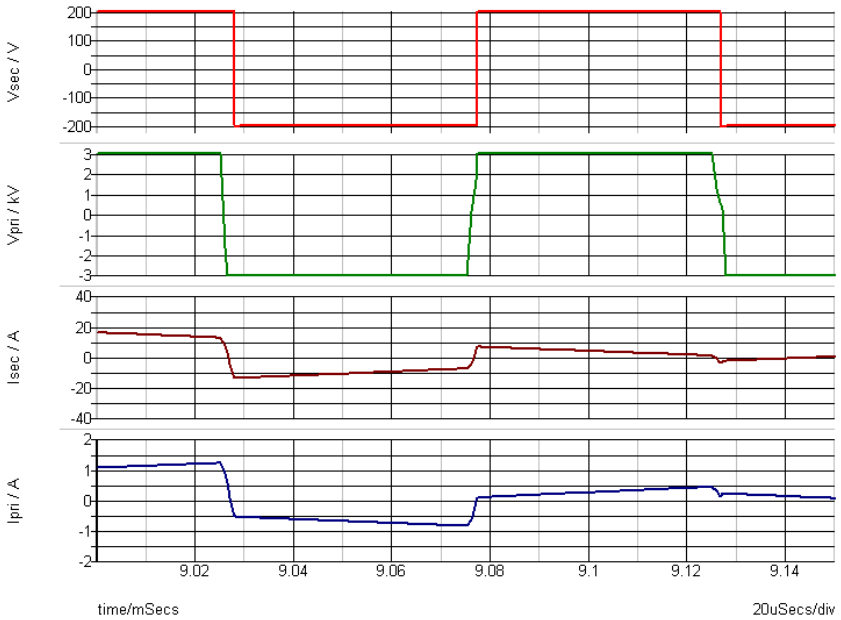



Figure 4.7: Transformer Voltage and Current for No Load with 228 mH Magnetizing Inductance

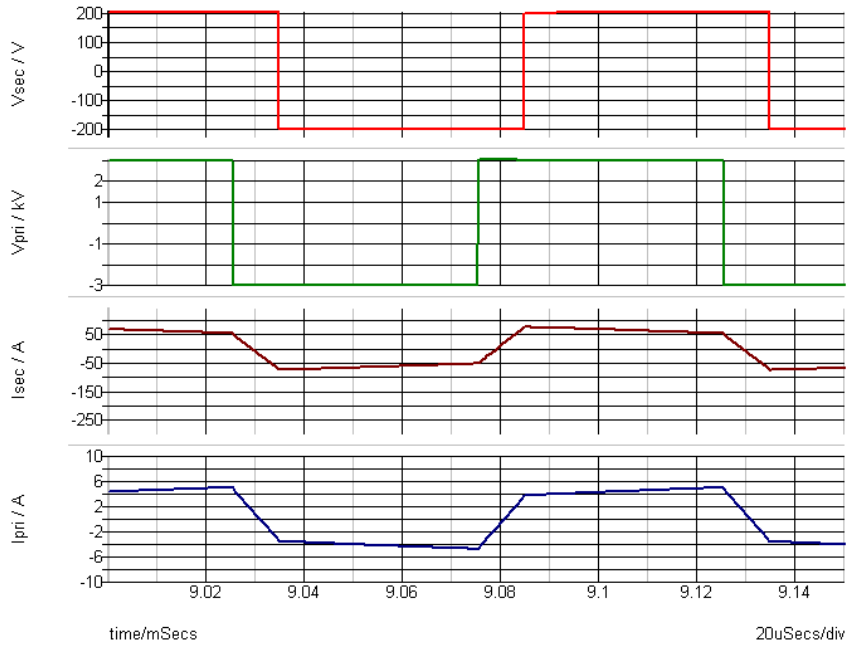



Figure 4.8: Transformer Voltage and Current for 10 kW Full Load with 44 mH Magnetizing Inductance

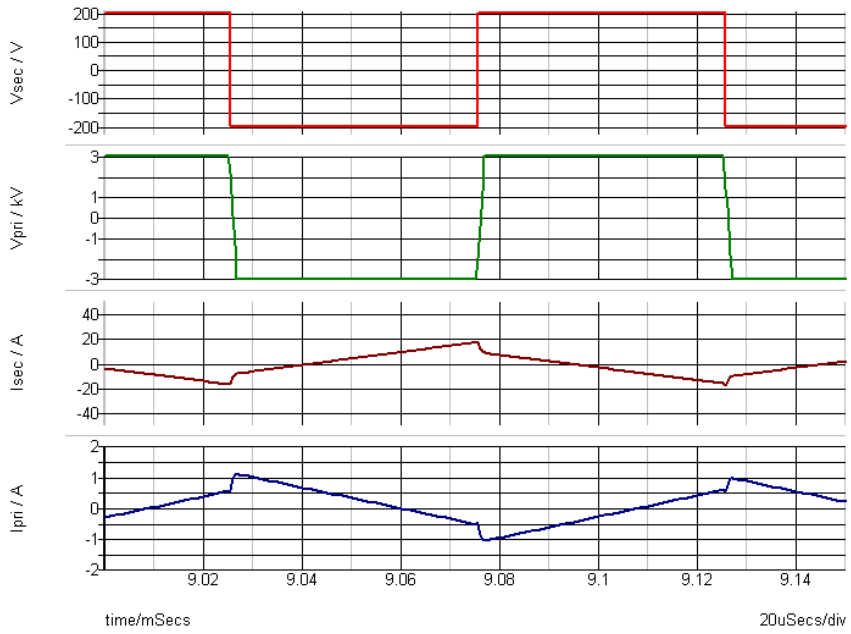



Figure 4.9: Transformer Voltage and Current for No Load with 44 mH Magnetizing Inductance

## 4.5 Variable Frequency Control and Experiment Results

It can be seen from Figure 4.5(b) that core loss will be less for higher frequency, but it can also operates safely under lower frequency 10 kHz with less than 20 W extra loss compared with 20 kHz. Since the leakage inductance will be fixed if the transformer geometry is fixed. While for the DHB converter, more energy can be transferred for the same phase shift angle if decreasing the switching frequency. Moreover, the transformer copper loss can also be reduced due to the smaller winding AC resistance for the lower frequency. The DHB converter has been tested for 3 different switching frequency 10 kHz, 15 kHz, and 20 kHz. The efficiency result is shown in Figure 4.10. The peak efficiency is 97.5% at 5.5 kW load for 10 kHz switching frequency.

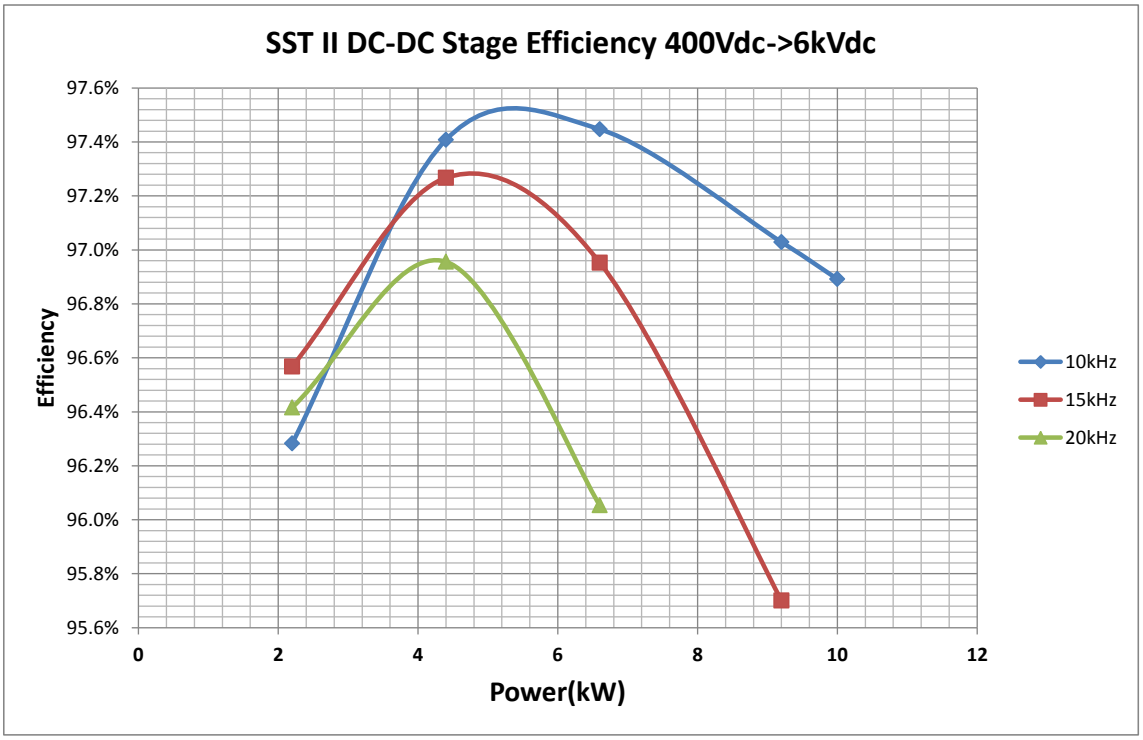



Figure 4.10: DHB Efficiency for Different Switching Frequency

Figure 4.11 and Figure 4.12 show the DHB transformer voltage and current waveforms for 10 kW and 2.2 kW load separately with 10 kHz switching frequency. It can be seen from Figure 4.12 that a large portion of the measured current is the magnetizing current.

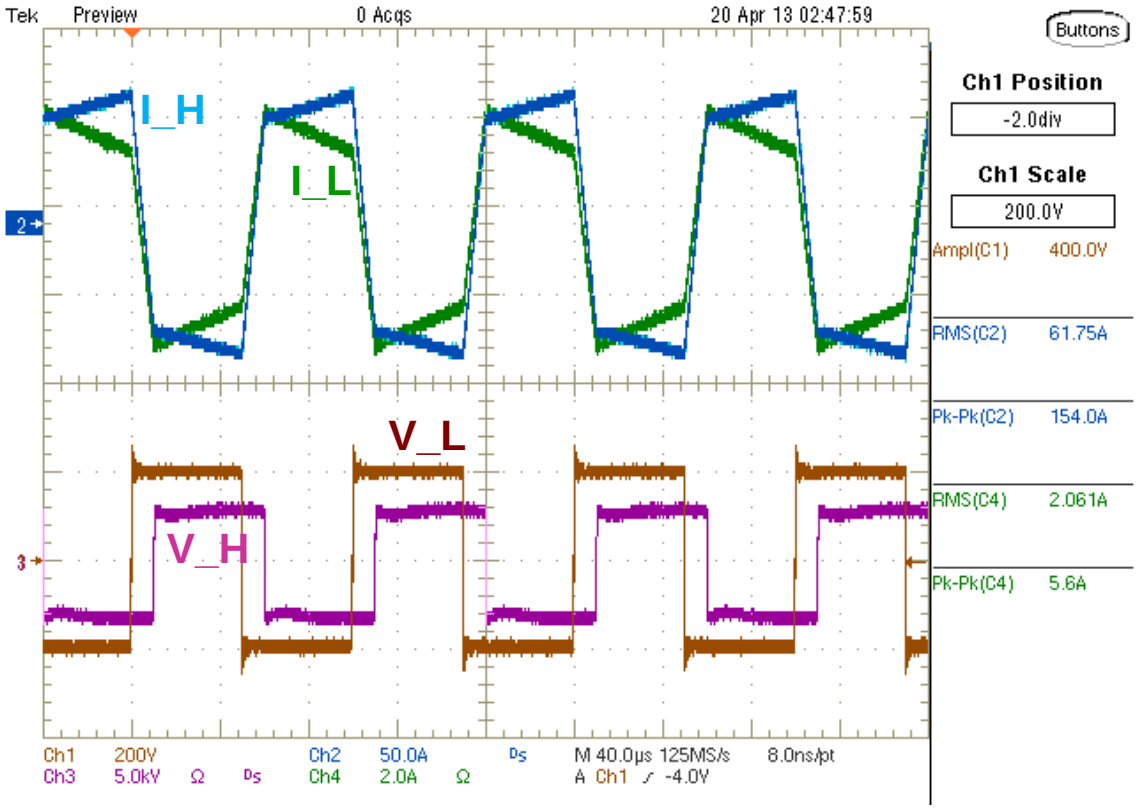



Figure 4.11: DHB Experiment Waveforms for 10 kHz, 10 kW Load

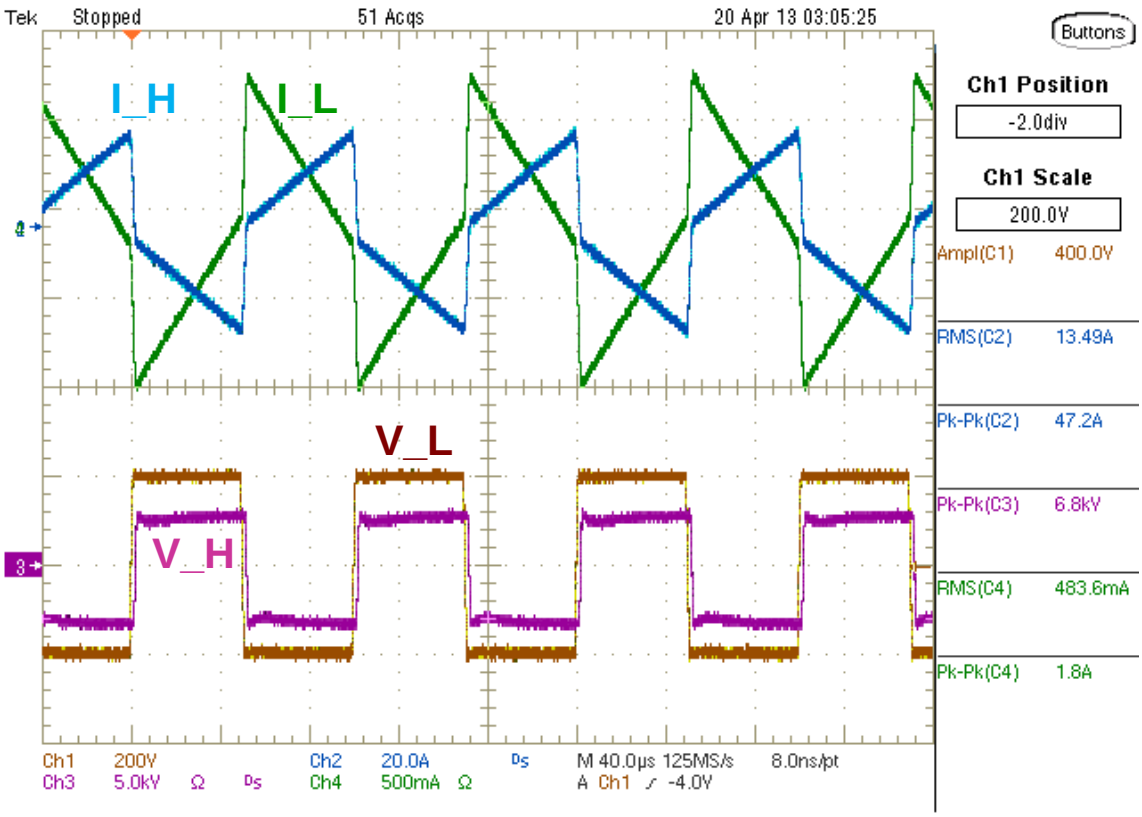



Figure 4.12: DHB Experiment Waveforms for 10 kHz, 2.2 kW Load

# CHAPTER 5

# SST Inverter Stage Design

## 5.1 Introduction

The SiC power devices has been evaluated and compared with silicon devices in many publications [19, 33, 34, 10, 7, 22, 28, 55, 45, 35, 12]. The 1200 V 100 A SiC MOSFET module (CAS100H12AM1) becomes available on the market in 2012, which potentially can be used for the PV inverters, motor drivers and other power converter applications to boost the converter efficiency and reduce the system volume. In this section, the performance of the 1200 V 100A SiC MOSFET module from Cree Inc will be investigated and compared with the same rating Infineon silicon IGBT (FF100R12RT4), particularly from the efficiency point of view. Loss dissipated in both conduction and switching transient is considered for the comparison. The SST inverter

stage without neutral leg (Figure 5.1) has been built based on these two types devices for the efficiency comparison. This section will first discuss the characteristics of both SiC MOSFET and Si IGBT under static conduction and dynamic switching. Simulation results developed with PLECS thermal model will also be compared with test results to show the validity of the loss breakdown on both devices.

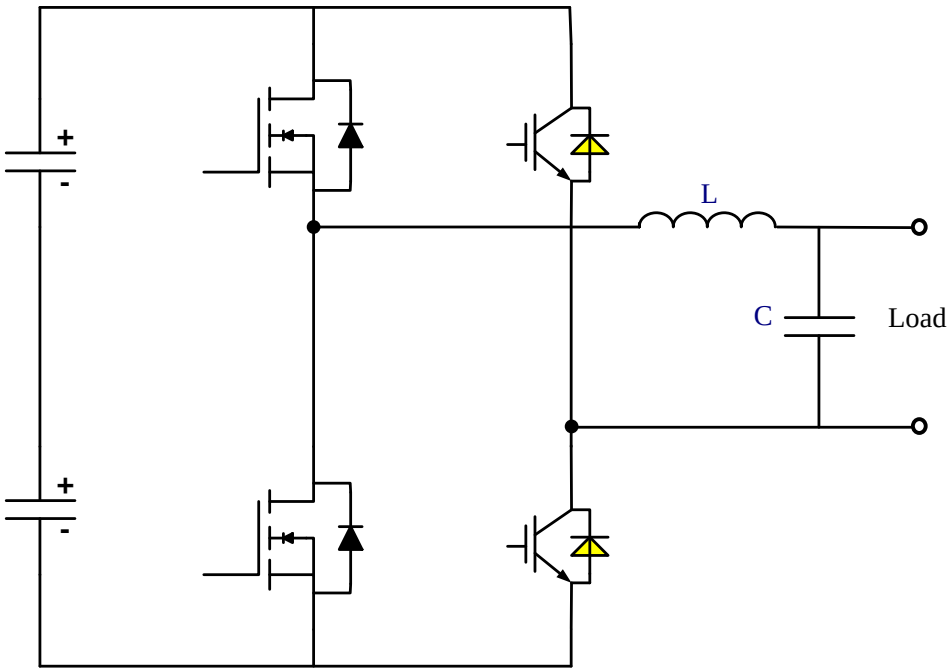



Figure 5.1: SST Inverter Stage Topology Without Neutral Leg

## 5.2 Comprehensive Performance Evaluation of the 1200 V 100 A SiC MOSFET and Silicon IGBT

### 5.2.1 Forward Characteristics Comparison

The conduction I-V characteristics of the two devices have been measured for both 25 °C and 125 °C. Figure 5.2 shows the forward I-V curves of both, it can be seen that the MOSFET has lower forward voltage drop under 90 A current. This feature enables that for single device, MOSFET has much less conduction loss than IGBT for low current situations. Moreover, SiC MOSFET displays a almost constant on resistance $R_{ds(on)}$ for a fixed temperature whereas silicon IGBT has a nonlinear I-V curve. Together with its positive temperature coefficient of ON resistance (higher temperature leads to a smaller $R_{ds(on)}$) as shown in Figure 5.2, the MOSFET is suitable for parallel operation when higher current capability is required.

Figure 5.3 shows the I-V curves with the reversed conducting current through the anti-paralleling diodes. With zero volt gate bias, the voltage drop of the SiC diodes (SiC JBS together with the MOSFET body diode) is greater than the IGBT paralleled diode. However, the MOSFET can be turned on and operated as the synchronous rectifier mode, so the reverse current will also go through the channel together the anti-paralleling SiC JBS diode. The combined voltage drop (SiC JBS diod plus MOSFET channel) will therefore be lower than the IGBT as shown in Figure 5.3.

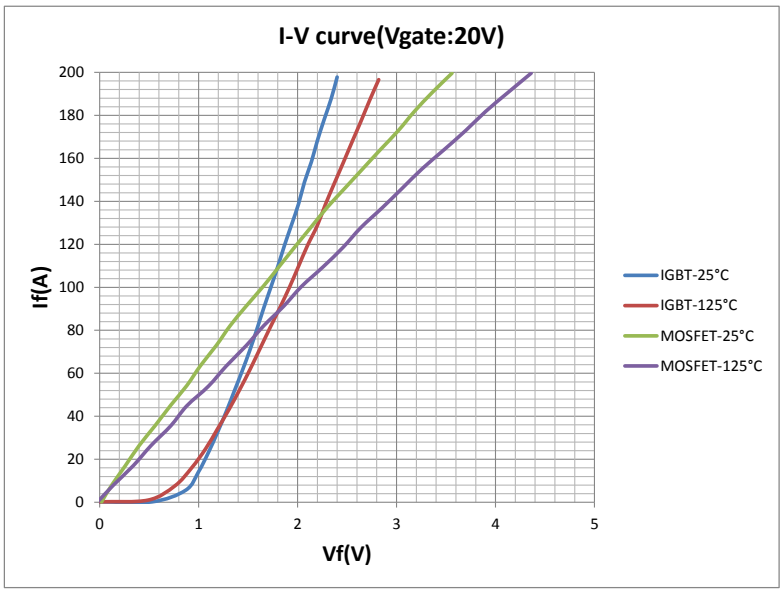



Figure 5.2: Forward I-V Curves of the Si IGBT and SiC MOSFET

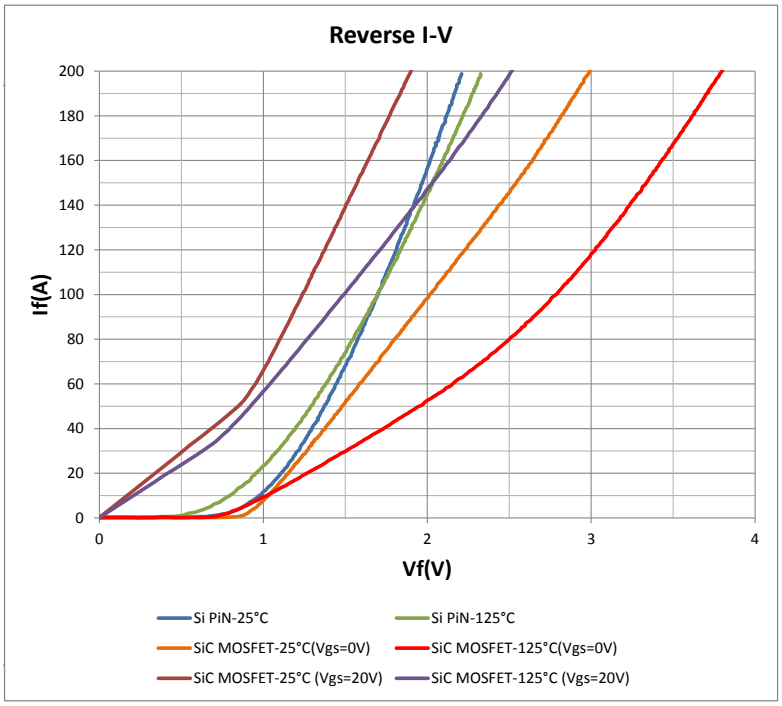



Figure 5.3: Reverse I-V Curves of the Si IGBT and SiC MOSFET

### 5.2.2 Switching Characteristics Comparison

A great portion of loss is contributed by the switching transients when the switching frequency is high. To compare the switching loss for the two devices, the dynamic switching performance has been characterized through an inductive load double pulses tester (Figure 5.4 and Figure 5.5). Special attention has been paid to minimize the loop inductance for a cleaner switching waveform with more accurate loss measurement. The loop inductance for the DC capacitor bus bar is around 30nH, and the stray inductance for the MOSFET terminals and internal wire bonding is less than 15nH per device according to the SiC MOSFET module datasheet.

Switching energy losses including $E_{on}$, $E_{off}$, and $E_{rec}$ have been measured for both Si IGBT and SiC MOSFET with the same test circuit and parameters, the results are plotted in Figure 5.6, Figure 5.7 and Figure 5.8 separately. It can be observed that the Si IGBT loss is highly dependent on the operation temperature and increases when temperature rises; while for the SiC MOSFET, the loss doesn't change much with the temperature variations, the turn on loss is even lower for the higher temperature which is caused by the negative temperature coefficient of the MOSFET threshold voltage, the switching losses under 125 °C for both devices have been listed in Table 5.1, it shows SiC MOSFET has significant lower loss than Si IGBT.

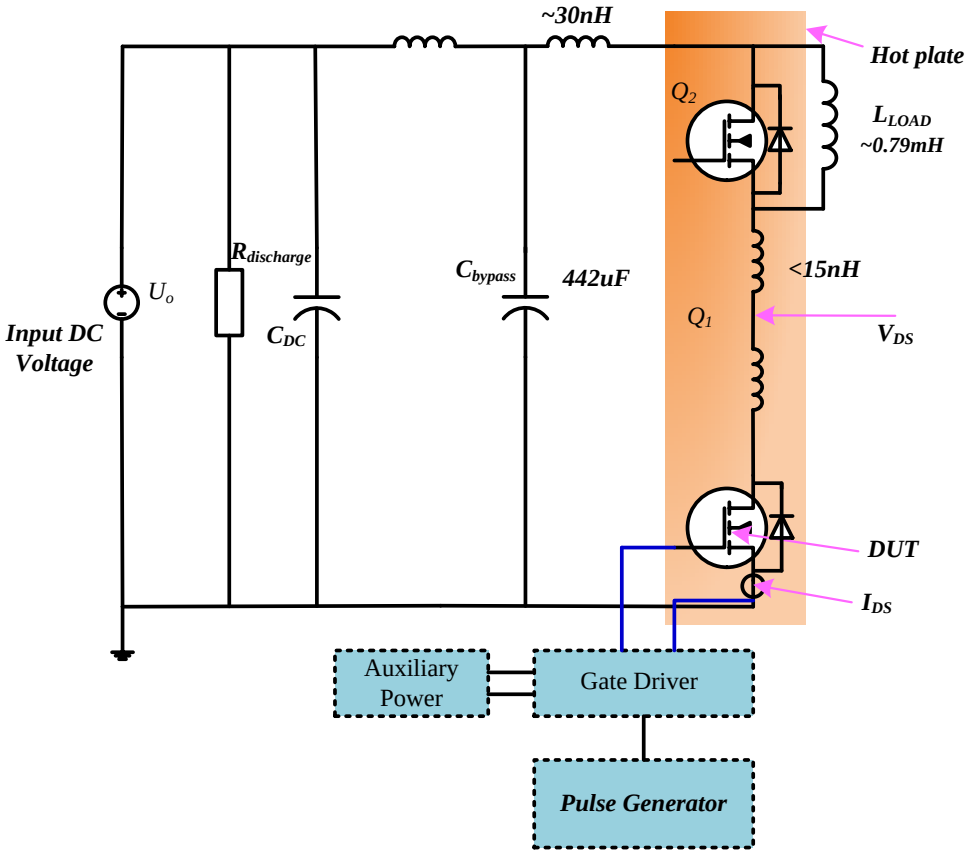



Figure 5.4: 1200V MOSFET Module Double Pulse Tester Circuit Diagram

Table 5.1: MOSFET vs IGBT Switching Loss Comparison Summary

| Conditions: Vdc=600V; Ids=100A; Rg=5Ω; Vgs=-5V~20V; Tj=125° C | | | |
|---|---|---|---|
| Loss(mJ) | Cree SiC MOSFET | Infineon Si IGBT | Times of improvement |
| Eon | 2.47 | 8.78 | 3.6X |
| Eoff | 1.28 | 8.78 | 6.8X |
| Erec | 0.53 | 5.93 | 11.2X |

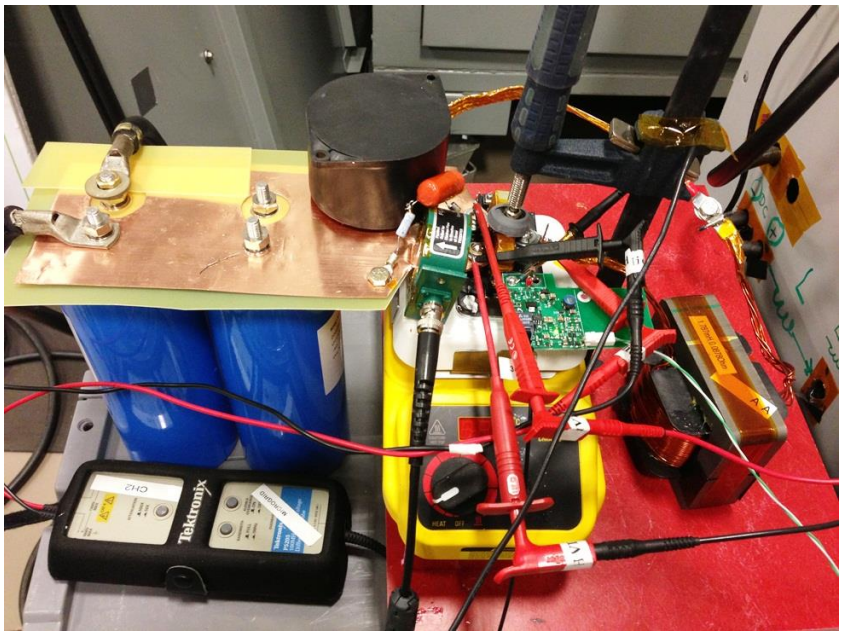



Figure 5.5: 1200V MOSFET Module Double Pulse Tester Hardware

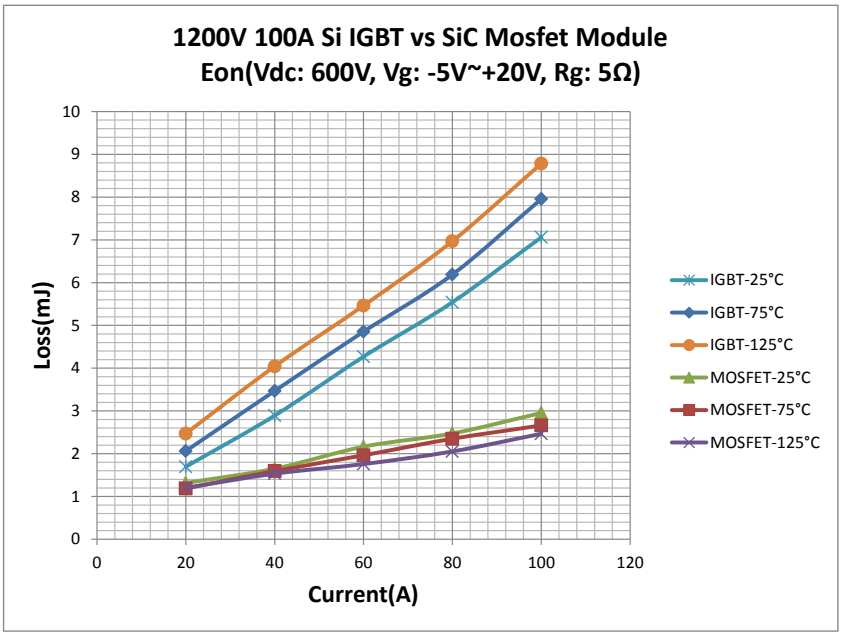



Figure 5.6: $E_{on}$ Comparison of Si IGBT and SiC MOSFET Under Different Temperatures

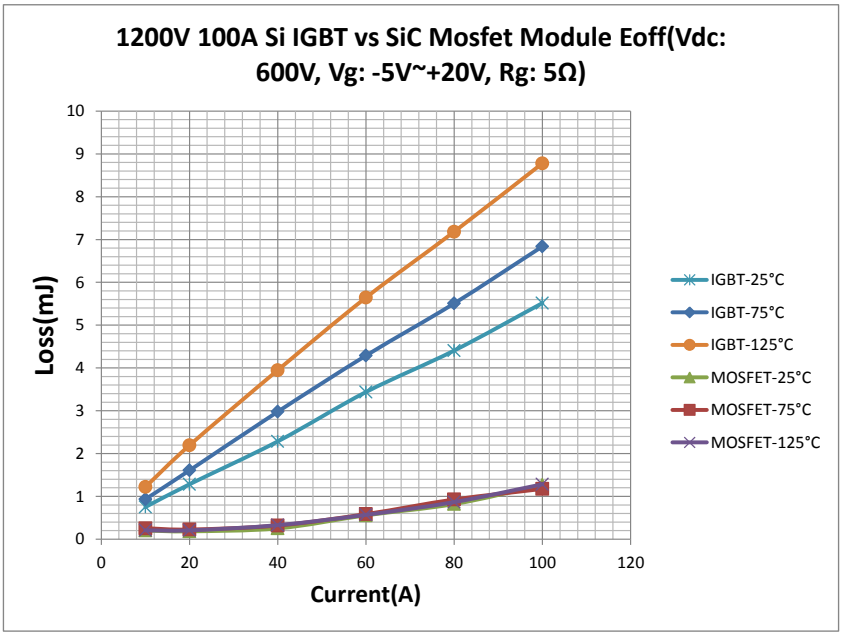



Figure 5.7: $E_{off}$ Comparison of Si IGBT and SiC MOSFET Under Different Temperatures

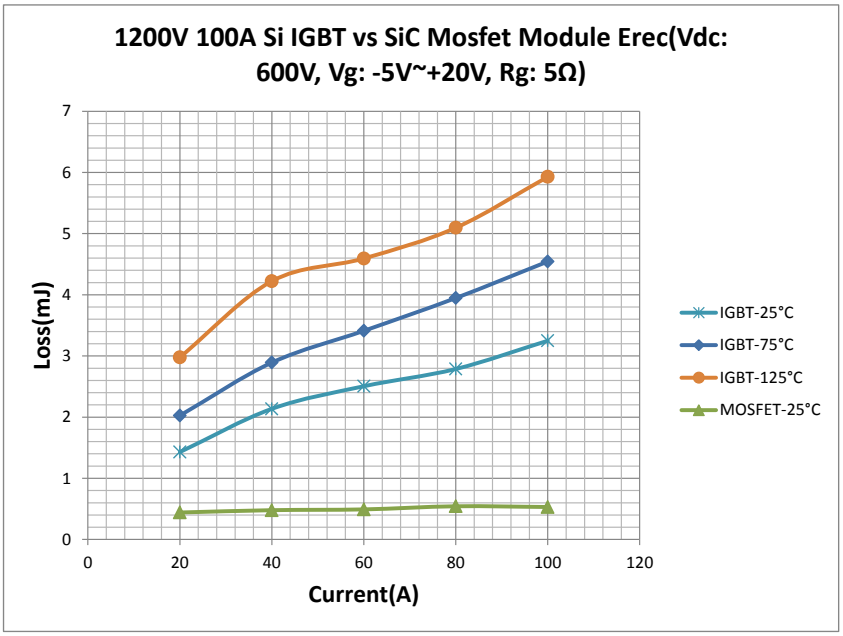



Figure 5.8: $E_{rec}$ Comparison of both Si IGBT and SiC MOSFET Under Different Temperatures

## 5.3 Prototype Design, Experiment and Loss Simulation

Full bridge inverter is one of the major applications for the 1200 V 100 A level devices. In order to evaluate the two devices for such application, an 11 kW full bridge inverter has been built (Figure 5.9). One leg is SiC MOSFET half bridge module and the other leg is Si IGBT half bridge module, the modulation method is unipolar single frequency SPWM as discussed in chapter 3, only one leg is switched at high frequency while the other one is switched at output AC voltage frequency which is 60 Hz for this test. With such configuration, we can choose either the MOSFET leg or the IGBT leg to be operated at high frequency, the advantage of this arrangement is that the hardware setup will not be changed for evaluating the two devices. Since the conduction loss will be almost the same when the device has been switched either at high frequency or at 60 Hz. The loss difference for different cases will be almost entirely caused by the difference of the switching loss. The nanocrysline core and litz wire has been used for building the filter inductor with the objective to minimize the inductor loss and its variations over different switching frequencies.

Figure 5.10 shows a typical inverter operation waveform, and the inverter efficiency has been measured for the 9 cases as listed in Table 5.2. It has been estimated that the other loss except for power devices loss is about 43 W which includes the inductor loss and DC bus capacitors paralleled resistors loss for all cases.

For cases 1-3, only the IGBT leg has been switched at high frequency. Figure 5.11 gives the measured total device loss and compares it with the simulation results. The loss simulation is based on the MOSFET and IGBT Simulink/PLECS loss model which combines the characterization data given in the above section. It shows a good match between the measured and simulated loss which validates the loss model. The

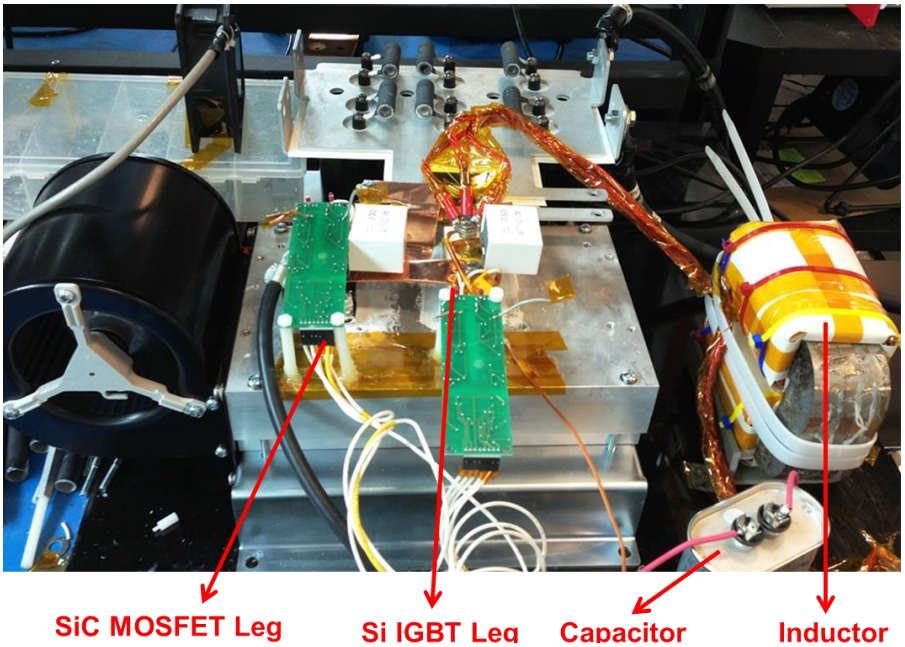



Figure 5.9: Inverter Prototype

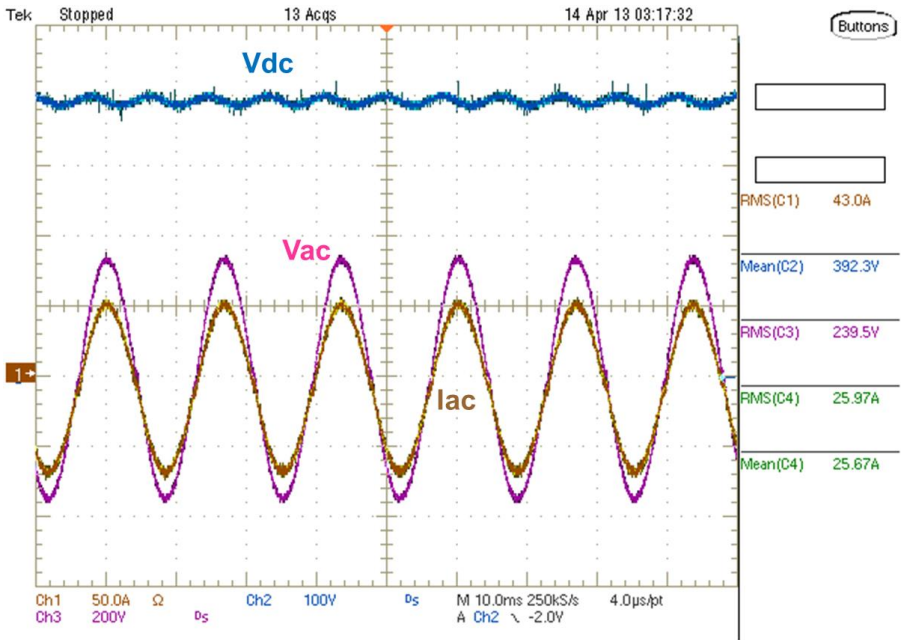



Figure 5.10: Inverter Waveforms

Table 5.2: Inverter Stage Test Cases

| Cases | IGBT Leg | MOSFET Leg | Results |
|---|---|---|---|
| 1 | 20 kHz | 60 Hz | Figure 5.11,Figure 5.12,Figure 5.15 |
| 2 | 30 kHz | 60 Hz | |
| 3 | 40 kHz | 60 Hz | |
| 4 | 60 Hz | 20 kHz | Figure 5.13,Figure 5.14,Figure 5.15 |
| 5 | 60 Hz | 30 kHz | |
| 6 | 60 Hz | 40 kHz | |
| 7 | 10 kHz | 10 kHz | Figure 5.15 |
| 8 | 15 kHz | 15 kHz | |
| 9 | 20 kHz | 20 kHz | |

simulated loss breakdown has been given in Figure 5.12 where it can be found that the major loss is the IGBT switching loss.

Figure 5.13 and Figure 5.14 show the results for cases 4-6, the conduction loss is almost the same for different switching frequency, the MOSFET switching loss is proportional to the switching frequency.

For Cases 7-9, the inverter is switched under unipolar double frequency SPWM scheme (Figure 3.3). Both legs are switched at high frequency.

The inverter efficiency for all 9 cases has been plotted in Figure 5.15. As can be seen, for each operation mode, the efficiency decreases with higher switching frequency, indicating increased switching losses. Also can be seen is that the highest efficiency occurs when only SiC devices is utilized for high frequency switching, reaching 98.6% at its peak value. This shows that SiC MOSFET has lower switching losses compared with Si IGBT. Figure 5.16 gives efficiency for the SST inverter stage.

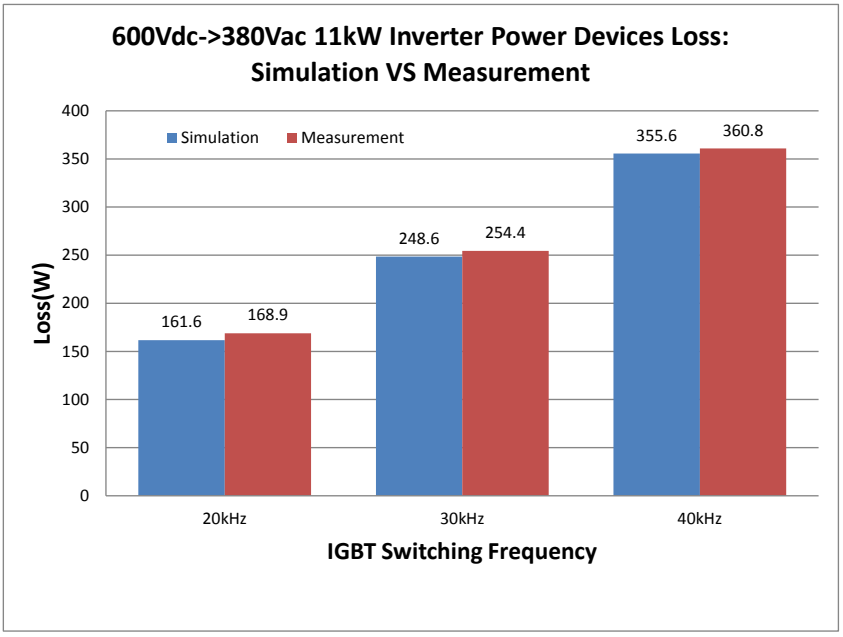



Figure 5.11: IGBT switching Loss Comparison Between Experiment and Simulation

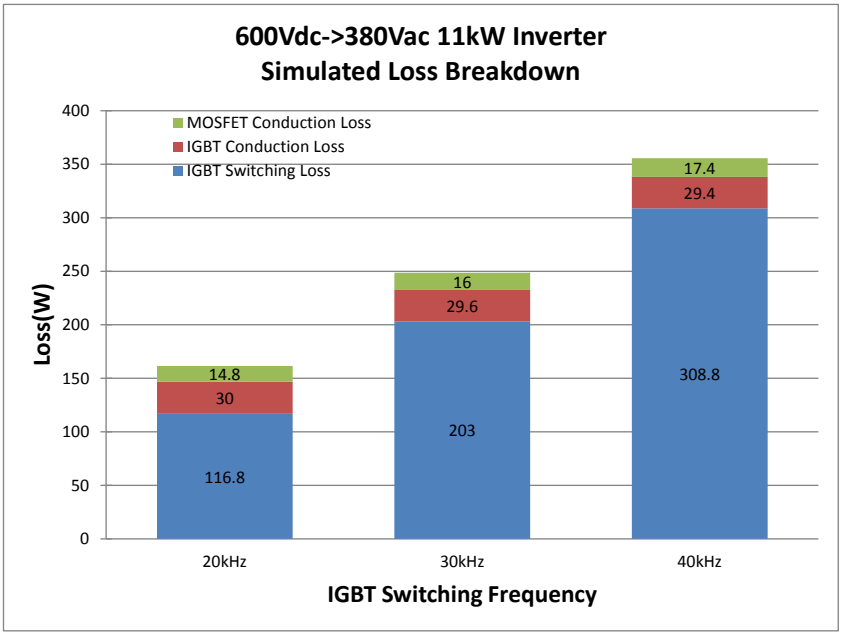



Figure 5.12: Inverter Loss Breakdown when the IGBT Leg is Switched at High Frequency

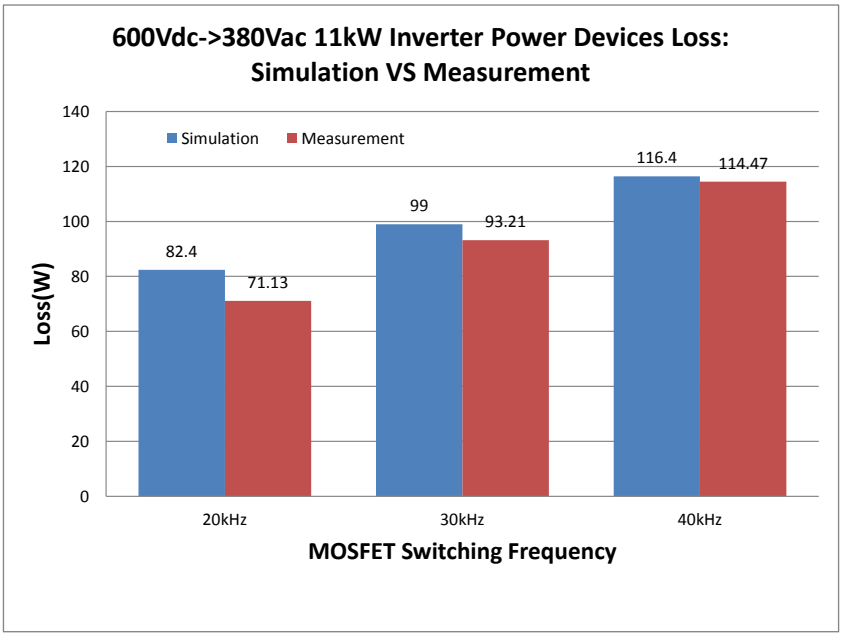



Figure 5.13: MOSFET Switching Loss Comparison Between Experiment and Simulation

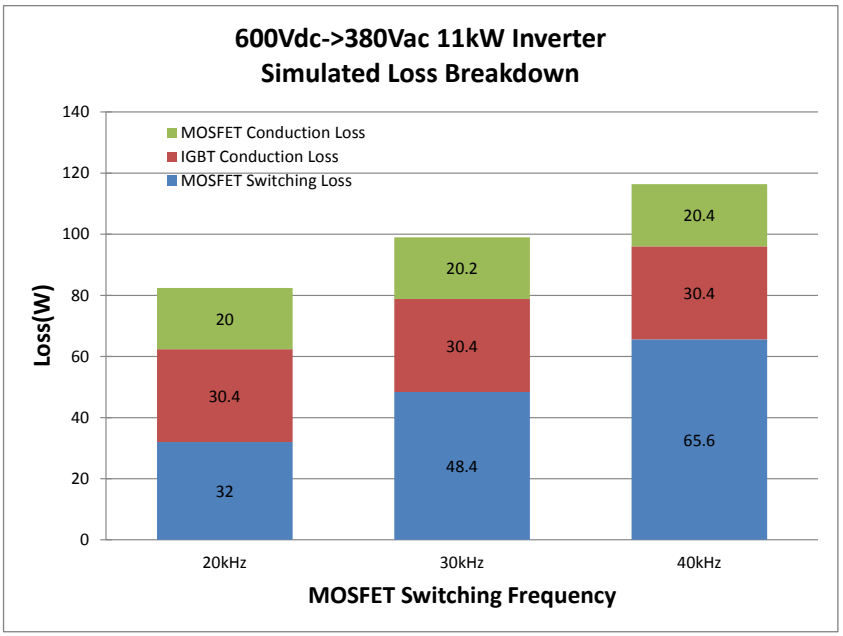



Figure 5.14: Inverter Loss Breakdown when MOSFET leg is Switched at High Frequency.

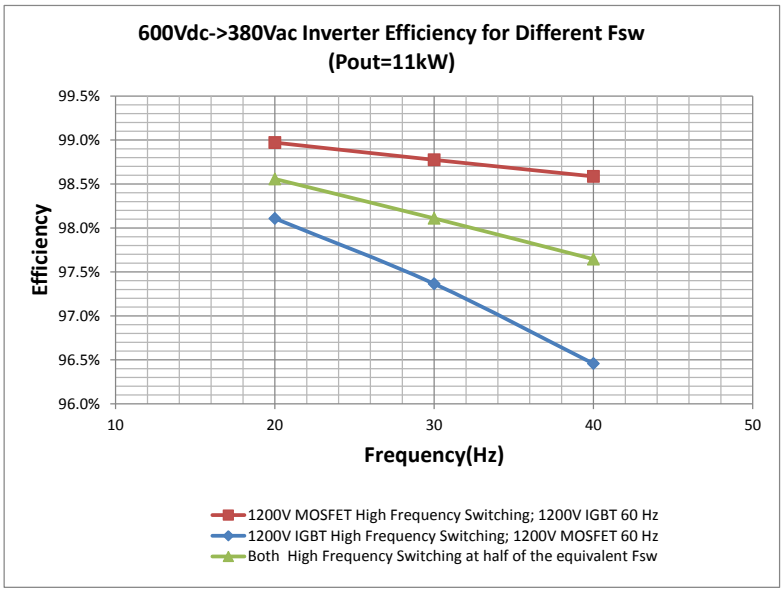



Figure 5.15: Inverter Efficiency with (1) Only Switches MOSFET; (2) Only Switches IGBT; (3) Switch both MOSFET and IGBT, at 20 kHz, 30 kHz and 40 kHz Respectively

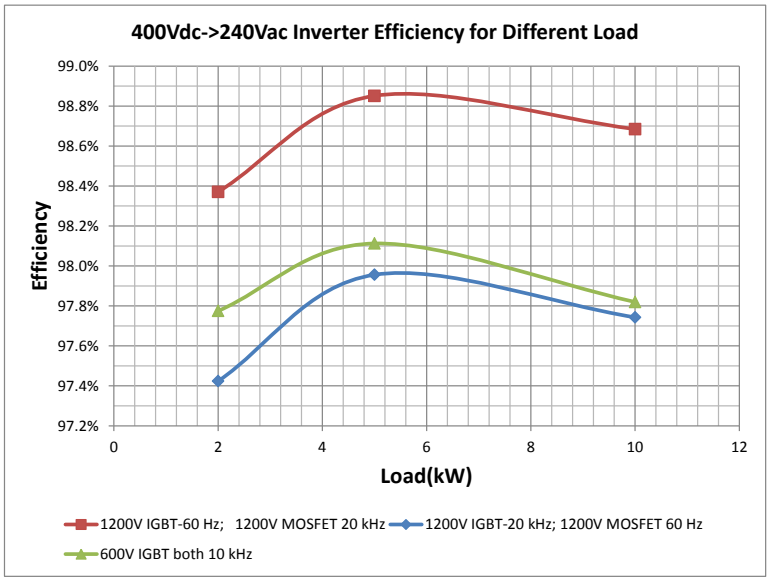



Figure 5.16: SST Rectifier Stage Efficiency for Three Cases

# CHAPTER 6

# Conclusions and Future Work

With the demand of developing a smart and robust electrical grid, there are increasing driving force to explore high efficiency and more compact solid state transformer design. This dissertation studied the performance of the emerging high voltage SiC MOSFET and designed a 10kVA solid state transformer based on all SiC devices. The switch characteristics have been fully tested with experimental setup and PLECS simulation loss models have been developed. The switching off transient is different for high voltage MOSFET and low voltage MOSFET. It is concluded that the MOSFET parasitic capacitors store significant amount of energy and the MOSFET turn on loss is high but turn off loss is virtually zero with small enough turn off gate resistor. A method for estimating the MOSFET parasitic capacitances has been proposed and explained in detail.

The SiC MOSFET based SST topology has been proposed which includes AC/DC full bridge rectifier, Dual Active Half Bridge (DHB) DC/DC and DC/AC inverter stage. In order to minimizing the MOSFET switching loss during AC current zero crossing period, the unipolar single frequency SPWM has been implemented for the rectifier stage.

The ZVS range of the DC/DC stage has been analyzed and solutions has been proposed to extend the range under light load. With reduced magnetizing inductance and variable frequency control, full load range ZVS can be achieved and has been verified through simulation.

The inverter stage has been designed based both on 1200 V SiC MOSFET and silicon IGBT, it serves as the benchmark for comparing the two devices. The results show that the SiC device has much lower switching loss compared with silicon IGBT.

The three stages' prototype has been developed and tested and the peak efficiency for each stage is 99%, 97.5%, 98.9% separately.

The future work of this research includes:

1) System level integration of the SST with the grid, which includes the bidirectional power flow, reactive power generation capability, and etc.

2) Develop the gate drivers for the high voltage SiC power devices, which requires high voltage isolation and has to be immune to the high $dv/dt$.

3) Research on the series connection of the SiC MOSFET for supporting higher voltage.

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