ABSTRACT

HUANG, XING. Design and Fabrication of High Voltage Silicon Carbide Symmetric Blocking Switch for FREEDM Smart Grid. (Under the direction of Alex Q. Huang and B. Jayant Baliga.)

This research focuses on the development of symmetric blocking Silicon Carbide (SiC) power device for fault interruption devices (FID) of FREEDM smart grid. The high voltage SiC symmetric blocking bipolar switches can greatly simplify the power circuits and provide low forward voltages.

One of the most challenging aspects in developing a symmetric blocking device is to design an feasible edge termination technique for the SiC material. The Orthogonal Positive Bevel (OPB) termination formed by blade sawing was proposed to overcome all the fabrication difficulties in SiC processing. This concept has been experimentally verified by the fabrication of a 1kV symmetric blocking NPN structure that used conventional single-zone junction termination extension (JTE) for forward blocking and the OPB termination for reverse blocking.

As the power switches in the FID may need to withstand the short-circuit current for tens of microseconds, their current saturation capabilities are very important. In order to understand the limitations of SiC devices at short-circuit operation, the short-circuit behaviors of commercial 1200V class SiC MOSFET and normally-off SiC JFET have been studied and analyzed. It was found that the JFET gate structure is much more robust and more suitable for FID application due to preferably needed current saturation capability.

A 10kV Symmetric Blocking Field Controlled Diode has been designed using parameters based on the available 150µm P-epi wafer with TCAD tools. A novel buried 3-zone JTE was designed for forward blocking and the OPB termination for reverse blocking.
A cascode configuration of the FCD with low voltage MOSFETs has been proposed to operate the FCD in two different modes: the low $V_F$ thyristor mode and the FCD mode with current saturation.

The related SiC processes have been developed and the fabrication has been carried out to demonstrate the principles of FCD. 8kV symmetric blocking has been achieved using the developed edge terminations. The best FCD sample had a blocking gain of 75X and could conduct 5A at 10V forward bias due to wafer bowing and low carrier lifetime.
Design and Fabrication of High Voltage Silicon Carbide Symmetric Blocking Switch for FREEDM Smart Grid

by

Xing Huang

A dissertation submitted to the Graduate Faculty of North Carolina State University in partial fulfillment of the requirements for the Degree of Doctor of Philosophy

Electrical Engineering

Raleigh, North Carolina

2014

APPROVED BY:

______________________________  ________________________________
Alex Q. Huang               B. Jayant Baliga
Co-chair of Advisory Committee Co-chair of Advisory Committee

______________________________  ________________________________
Lin Cheng                   Mehmet C. Ozturk

______________________________
Veena Misra
DEDICATION

To my parents: Qiguí Huang and Yingfang
Xing Huang was born in Chongqing, China. He received his B.S. degree in electrical engineering at University of Electronic Science and Technology of China, in 2009. He was then recruited as a graduate student at North Carolina State University and became a research assistant at the Future Renewable Electric Energy Delivery and Management (FREEDM) Systems Center. From 2009 to 2011, his research activity was focused on reliability of SiC Schottky diodes under surge/avalanche conditions. Since August 2011, he started working on the 10kV-class high voltage SiC devices for fault interruption devices on the smart grid transmission line. His research interests include the design, fabrication, application and reliability study of power semiconductor devices.

He has coauthored more than 10 papers and is patent holder of the orthogonal positive bevel termination.
ACKNOWLEDGEMENTS

First of all, I would like to thank my advisers, Dr. Alex Q. Huang and Dr. B. Jayant Baliga, for their guidance, support and encouragement over the course of my graduate study and research at North Carolina State University. I have been benefited much from Dr. Huang’s versatile knowledge, critical thinking and practical attitude on researches and innovations, as well as his broad professional networks. I am very grateful to Dr. Baliga’s great ideas, visions and discreet supervision on my research. His expertise from decades of experience has been invaluable resource to me. His virtue of patience and diligent attitude has set a model for me as a scholar.

I am indebted to Dr. Anant Agarwal of Department of Energy and Dr. Lin Cheng of Cree Inc for their significant support on the fabrication of SiC devices and playing important roles in the completion of this work. I am also grateful to Dr. Mehmet C. Ozturk and Dr. Veena Misra for serving in my committee and for the support they have provided directly and indirectly. Their courses and cleanroom facilities have been indispensable resources for my research.

It has been a great pleasure to work with the excellent staffs of FREEDM and NNF. I extend my special thanks to Marcio Cerullo, Nicole Hedges, Henry Taylor, Bruce Sprague, David Vellenga, Joe Matthews, Karen Autry, and Colleen Reid for their great help in technical and administrative issues.

I also give my great thanks to my friends for being supportive and a source of inspiration and learning. Specially thank Jun Wang, Gangyao Wang, Yu Du, Edward Van Brunt, Woongje Sung, Bongmook Lee, In Hwan Ji, YoungHwan Choi, Meng-chia Lee, Sizhen Wang, Yalin Wang, Francisco Suarez, Xiangyu Yang, Narayanan Ramanan, Xingchen Yang, Xu She, Dong Chen, Haotao Ke, Chang Peng and Jing Yao for many enlightening
discussions.

Finally, I would like to thank my family and my girlfriend Jing Yao for their love and support during my course of Ph.D..
# TABLE OF CONTENTS

LIST OF TABLES ................................................................. ix

LIST OF FIGURES ................................................................. x

Chapter 1 Introduction ......................................................... 1
  1.1 The Benefits of SiC Power Devices ................................. 1
    1.1.1 The Efficiency Performance ................................ 1
    1.1.2 The Reliability Performances ............................... 8
    1.1.3 Status of Commercialized SiC Power Devices ............... 16
  1.2 FREEDM System and SiC Power Devices ......................... 17
  1.3 Fault Interruption Devices ........................................ 19
    1.3.1 Mechanical and Solid-State Circuit Breakers ............. 19
    1.3.2 Silicon Solutions ........................................... 21
    1.3.3 Silicon Carbide Solution .................................. 21
  1.4 Outline of This Work ............................................... 22

Chapter 2 Orthogonal Positive Bevel Termination .................. 24
  2.1 Review of Symmetric Blocking Technologies .................... 24
    2.1.1 Solution for Wafer-Size Devices .......................... 24
    2.1.2 Solution for Si Chip-Size Devices ........................ 27
  2.2 Simulation of Orthogonal Positive Bevels ....................... 29
  2.3 Process Development of the Bevel Dicing ....................... 32
    2.3.1 Surface Roughness ......................................... 32
    2.3.2 Limitation of Dicing ...................................... 33
  2.4 Experimental Demonstration ....................................... 36
    2.4.1 Fabrication Processes .................................... 36
    2.4.2 Results and Discussions .................................. 38
  2.5 Conclusions ......................................................... 43

Chapter 3 Current Saturation Capabilities of SiC Gate Structures 44
  3.1 DC Characterization ............................................... 46
    3.1.1 DC Characteristics of SiC MOSFET ........................ 46
    3.1.2 DC Characteristics of SiC JFET ........................... 49
  3.2 Short-Circuit Test Results and Discussions .................... 51
    3.2.1 Short-Circuit Operations of SiC MOSFET .................. 51
    3.2.2 Short-Circuit Operations of SiC JFET .................... 55
  3.3 Conclusion ......................................................... 56

Chapter 4 Design of Symmetric Blocking FCD ........................ 58
4.1 Introduction to the P-type FCD .......................... 59
4.2 Design Trade-offs of the P-type FCD ....................... 60
  4.2.1 Design of Breakdown ............................. 60
  4.2.2 Saturation Current and Forward Voltage .............. 64
4.3 FCD Cascode Configuration and Use in FID .................. 68
4.4 Design of Edge Terminations ............................. 71
  4.4.1 Forward Blocking JTE Termination .................. 71
4.5 Conclusions ........................................ 74

Chapter 5 Process Development and Fabrication of FCD ........... 75
  5.1 Process Flow ...................................... 76
  5.2 Layout Design and Device Variations ..................... 77
  5.3 Unit Process Development ............................. 79
    5.3.1 Implantation and Impurity Activation ............... 79
    5.3.2 RIE of Oxide as Hard Mask for Implantation ......... 82
    5.3.3 SiC Reactive Ion Etch ........................... 85
    5.3.4 Ohmic Contact to N- and P-Type SiC ................ 85
    5.3.5 Backend Process: Thick Metal ..................... 88
    5.3.6 Beveling with Dicing Blade ...................... 92

Chapter 6 Characterization and Analysis of FCD .................... 95
  6.1 Carrier Lifetime and Diode Characteristics .............. 95
    6.1.1 OCVD measurement of Epi Lifetime ................ 95
    6.1.2 Diode Forward I-V ................................ 99
    6.1.3 Diode Reverse Blocking .......................... 101
  6.2 FCD Forward I-V .................................... 105
    6.2.1 Impact of Lifetime ................................ 105
    6.2.2 Dependence on Structural Parameters ............... 105
  6.3 FCD Blocking Characteristics ........................... 110
    6.3.1 Symmetric Blocking Characteristics ............... 110
    6.3.2 Breakover and Blocking Gain ........................ 112
  6.4 Summary and Discussions .............................. 117

Chapter 7 Conclusions and Future Work .......................... 121
  7.1 Contributions ...................................... 121
  7.2 Future Work ...................................... 122

REFERENCE ........................................... 123

APPENDIX ............................................. 133
  Appendix A Parameters for SiC Simulation .................. 134
LIST OF TABLES

Table 1.1  FOM’s of Various Semiconductor Materials (Normalized Against Silicon)  7
Table 2.1  Si reverse blocking edge termination structures ........................................ 28
Table 2.2  Implantation schedules for N-, N+ and P+ implantation .............................. 37
Table 4.1  The impact of N$_{ch}$ to device performance .............................................. 66
Table 5.1  The Process Flow of 8kV RB-FCD ............................................................ 78
Table 5.2  Oxide RIE Recipe ....................................................................................... 83
Table 5.3  SiC RIE Recipe ......................................................................................... 85
Table 5.4  Aluminum RIE DOE with fixed 300W ICP and 200W RIE power at 15mTorr ............................................................................................................. 92
Table 6.1  Lifetime Distribution on Wafer ................................................................. 97
Table 6.2  The 4H-SiC Lifetime Enhancement Processes ........................................ 119
Table A.1  The simulation models and parameters ...................................................... 135
# LIST OF FIGURES

<table>
<thead>
<tr>
<th>Figure</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.1</td>
<td>Super-junction Structure</td>
<td>3</td>
</tr>
<tr>
<td>1.2</td>
<td>BV-Ron_sp trade off: Si Super-junction vs. SiC</td>
<td>5</td>
</tr>
<tr>
<td>1.3</td>
<td>Comparison of Switching Loss of 6.5kV Si IGBT and 10kV SiC MOSFET</td>
<td>7</td>
</tr>
<tr>
<td>1.4</td>
<td>Comparing critical temperature of Si and SiC p-n junctions</td>
<td>9</td>
</tr>
<tr>
<td>1.5</td>
<td>The I-V trajectory of a 600V SiC Schottky diode</td>
<td>11</td>
</tr>
<tr>
<td>1.6</td>
<td>The I-V trajectory of a 600V SiC JBS diode</td>
<td>11</td>
</tr>
<tr>
<td>1.7</td>
<td>Typical avalanche failure waveform of a SiC diode</td>
<td>12</td>
</tr>
<tr>
<td>1.8</td>
<td>Energy tolerances of 600V 8A SiC devices that avalanche at active area vs. edge termination</td>
<td>13</td>
</tr>
<tr>
<td>1.9</td>
<td>The maximum allowed power density vs. pulse width for SiC and Si devices</td>
<td>15</td>
</tr>
<tr>
<td>1.10</td>
<td>Electric grid diagram of FREEDM system</td>
<td>18</td>
</tr>
<tr>
<td>1.11</td>
<td>Simplified diagram of FID on a single phase distribution line</td>
<td>19</td>
</tr>
<tr>
<td>1.12</td>
<td>The bulky mechanical circuit breaker for transmission line</td>
<td>20</td>
</tr>
<tr>
<td>1.13</td>
<td>Schematics for Gen-I Silicon Based FID</td>
<td>21</td>
</tr>
<tr>
<td>1.14</td>
<td>Schematics for Gen-II Silicon Carbide Based FID</td>
<td>22</td>
</tr>
<tr>
<td>2.1</td>
<td>Conventional composite bevels for symmetric blocking Si wafer-size thyristors</td>
<td>25</td>
</tr>
<tr>
<td>2.2</td>
<td>The negative bevel process</td>
<td>26</td>
</tr>
<tr>
<td>2.3</td>
<td>Theoretical analysis of positive bevel termination: surface electric field vs. bevel angle</td>
<td>30</td>
</tr>
<tr>
<td>2.4</td>
<td>TCAD 3-D simulation of orthogonal joint of two 45° bevels at 1100V</td>
<td>31</td>
</tr>
<tr>
<td>2.5</td>
<td>The dicing saw and the diamond blade</td>
<td>33</td>
</tr>
<tr>
<td>2.6</td>
<td>SEM Picture of diced (a) SiC and (b) Silicon substrates</td>
<td>34</td>
</tr>
<tr>
<td>2.7</td>
<td>Feasibility of dicing through a Si wafer vs. a SiC wafer</td>
<td>35</td>
</tr>
<tr>
<td>2.8</td>
<td>Test for safe dicing</td>
<td>35</td>
</tr>
<tr>
<td>2.9</td>
<td>The NPN symmetric blocking structure (a) and P⁺P⁻N⁺ diode (b)</td>
<td>36</td>
</tr>
<tr>
<td>2.10</td>
<td>The leakage current reduction of a typical sample after RIE treatment</td>
<td>39</td>
</tr>
<tr>
<td>2.11</td>
<td>The histogram of leakage current before and after RIE treatment</td>
<td>39</td>
</tr>
<tr>
<td>2.12</td>
<td>SEM Picture of SiC OPBs (a) before and (b) after RIE</td>
<td>40</td>
</tr>
<tr>
<td>2.13</td>
<td>The I-V characteristics of symmetric blocking NPN structure</td>
<td>41</td>
</tr>
<tr>
<td>2.14</td>
<td>The I-V characteristics of P⁺P⁻N⁺ diode</td>
<td>42</td>
</tr>
<tr>
<td>3.1</td>
<td>Fault management at different node of transmission line</td>
<td>45</td>
</tr>
<tr>
<td>3.2</td>
<td>On-state characteristics of SiC MOSFET</td>
<td>48</td>
</tr>
<tr>
<td>3.3</td>
<td>Transfer characteristics of SiC MOSFET</td>
<td>48</td>
</tr>
<tr>
<td>3.4</td>
<td>The SiC MOS gate energy band diagram</td>
<td>49</td>
</tr>
<tr>
<td>3.5</td>
<td>Saturation characteristics of SiC JFET</td>
<td>50</td>
</tr>
</tbody>
</table>
Figure 3.6 Transfer characteristics of SiC JFET ........................................... 51
Figure 3.7 Short-circuit behavior of 1200V SiC MOSFET at $V_g=10V$ ....... 52
Figure 3.8 Short-circuit behavior of 1200V SiC MOSFET at $V_g=15V$ ....... 53
Figure 3.9 Simulated junction temperature and measured power density ...... 54
Figure 3.10 Simulated temperature profile at failure ................................. 55
Figure 3.11 Short-circuit behavior of 1200V normally-off SiC JFET .......... 56
Figure 3.12 Simulated JFET realtime junction temperature (top) and temperature profiles at 1/4, 1/2, 3/4 and the end of $t_{fail}$ (bottom) ...... 57

Figure 4.1 The schematics of FCD structure .............................................. 60
Figure 4.2 Calculation of BV limitation for wafers with 150µm and 200µm epitaxial layers ............................................................. 63
Figure 4.3 TCAD simulation of 150µm $5\times10^{14}$cm$^{-3}$ P-type doped SiC epitaxial wafer: NPN open-base transistor breakdown ....................... 63
Figure 4.4 (a) the impact of $N_{ch}$ and $V_{ga}$ on $V_F$ and (b) the $N_{ch}$ on $I_{sat}\left|V_{ga}=0\right.$ . 65
Figure 4.5 Diffusing of holes across the buried gate ................................. 67
Figure 4.6 The equivalent circuit model for P-type FCD ............................. 68
Figure 4.7 The cascode configuration of FCD controlled by two LV P-type MOSFETs ................................................................. 69
Figure 4.8 Simulated thyristor mode turn-off of cascode configuration ...... 70
Figure 4.9 Simulated FCD mode turn-off with saturation current ............... 71
Figure 4.10 The schematic of the FCD with edge terminations: forward blocking 3-zone JTE and reverse blocking OPB .......................... 72
Figure 4.11 The stable performance of Buried Three-Zone JTE against CEL process variations ......................................................... 73
Figure 4.12 The potential contour mapping with $N_{ch} = 4\times10^{16}$cm$^{-3}$ ..... 73

Figure 5.1 SRIM implantation profiles of (a) JTE Zone-1, (b) Buried Gate and (c) Gate Plug ................................................................. 81
Figure 5.2 Oxide RIE: (a) with and (b) without micro-masking .................... 84
Figure 5.3 Plasma Etch of SiC: (a) 323nm after 8.5min and (b) 0.9µm after 3 cycles of 8.5min run ..................................................... 86
Figure 5.4 Microscopy of Anode Mesa .................................................. 87
Figure 5.5 The folding line of wafer bowing. The line is farthest place from mask during lithography .............................................. 87
Figure 5.6 TLM measurement for N+ SiC Ohmic contact ........................... 89
Figure 5.7 Metal surface morphology at different annealing conditions: (a) room temperature, (b) 800°C, (c) 900°C and (d) 1000°C ......... 90
Figure 5.8 The P+ specific contact resistance on annealing temperature ...... 90
Figure 5.9 RIE of Al: (a) S1 sample, (b) S2 sample, (c) S3 sample and (d) S4 sample .......................................................... 93
Figure 5.10 Experiment of Al RIE process ...................................................... 94
Figure 5.11 SiC substrate with bevel edge termination ................................. 94

Figure 6.1 Schematic of OCVD test circuit ..................................................... 96
Figure 6.2 The waveform of lifetime measurement ......................................... 97
Figure 6.3 Simulated carrier profile of P⁺P⁻N⁺ diode ................................. 100
Figure 6.4 Comparison of measured and simulated diode forward I-V characteristics 102
Figure 6.5 The simulated 13kV breakdown of PiN diode ............................. 103
Figure 6.6 PiN reverse blocking ................................................................. 104
Figure 6.7 PiN BV vs. oxide interface charge ............................................. 104
Figure 6.8 Comparison of hole density in the buried gate with lifetime of (a) 1µs and (b) 182ns ................................................................................. 106
Figure 6.9 The simulated carrier profile and voltage drop at different lifetime .. 107
Figure 6.10 Forward IV dependence on W_{j fet} and L_{ch} ............................ 108
Figure 6.11 Current capabilities of different structures at 10V_{ak} and -3V_{ga} .. 109
Figure 6.12 Simulated trend of device conductivity on L_{ch} ......................... 110
Figure 6.13 The high voltage probe station .................................................... 111
Figure 6.14 The measured blocking gain ...................................................... 111
Figure 6.15 The simulated \( \alpha \) of FCD with \( L_{ch}=3\mu m \) and \( W_{j fet}=3\mu m \) ................................. 113
Figure 6.16 The simulated \( \beta \) of FCD with \( L_{ch}=3\mu m \) and \( W_{j fet}=3\mu m \) ................................. 114
Figure 6.17 Forward current pinch off at \( V_{ga}=10V \) ................................. 115
Figure 6.18 The measured blocking gain ...................................................... 116
Figure 6.19 I_k vs. \( V_{ga} \) at -20V, -100V, -200V cathode bias ......................... 116
Figure 6.20 The dependence of BV on lithography bias ................................. 117
Figure 6.21 Revised p-FCD structure ........................................................... 120
Chapter 1

Introduction

1.1 The Benefits of SiC Power Devices

4H-Silicon Carbide (SiC), because of its large band gap (3.26eV), high critical electric field (2.7MV/cm at a doping of 1e16cm\(^{-3}\)), high electron mobility (900cm\(^2\)/V·s), and high thermal conductivity (3.7W/cm·K), has been widely recognized as the future semiconductor material for high power, high frequency, and high temperature applications[1, 2].

1.1.1 The Efficiency Performance

Trade-off between Breakdown Voltage and On-Resistance

For unipolar power semiconductor devices, both the device breakdown voltage, BV, and the specific on-resistance \( R_{on,sp} \) are determined by the doping concentration of the drift region, \( N_d \). The BV decreases with increased \( N_d \) due to reduced depletion width \( W_D \), whose relation is determined by 1-D Poisson equation:
\[ \frac{\partial^2 \phi}{\partial x^2} = -\frac{N_d q}{\varepsilon} \]  

(1.1)

where \( \varepsilon \) is the permittivity of the semiconductor and \( q \) is the unit electron charge.

For non-punch-through (NPT) drift region, the electric field has a triangle shape and the boundary condition is \( \partial \phi / \partial x \mid_{x=0} = E_C \) and \( \partial \phi / \partial x \mid_{x=W_D} = 0 \), where \( E_C \) is the critical electric field of avalanche limit. Thus the dependence of BV on \( N_d \) can be expressed as:

\[ BV = \frac{\varepsilon E_C^2}{2N_d q} \]  

(1.2)

Considering \( R_{on} = l/\mu N_d q \), where \( \mu \) is the electron mobility, and \( BV = 0.5E_C W_D \), we have

\[ R_{on,sp} = \frac{4BV^2}{\varepsilon \mu E_C^3} \]  

(1.3)

In 1983, Dr. Jayant B. Baliga proposed the figure-of-merit (FOM) using the denominator of equation above to describe semiconductor’s ability to support high voltage while having low conduction loss. The FOM is expressed as[3]:

\[ BFOM = \varepsilon \mu E_C^3 \]  

(1.4)

This means that the \( BV^2 / R_{on,sp} \) is a constant for a specified unipolar semiconductor device due to its material properties without considering any minor effect about the dependence of \( \mu \) or \( E_C \) on \( N_d \) etc. Based on BFOM, the use of the wide band gap (WBG) semiconductor materials, like SiC and GaN, that have much higher breakdown electric field was projected to be very promising twenty years ago because their BFOM is usually hundreds of times higher than Si.
However, this comparison for unipolar switches is not fair when comparing conventional drift region structure with super-junction technologies such as CoolMOS\textsuperscript{TM}[4, 5]. The super-junction is a drift region design that incorporates multiple P and N type columns. For the vertical super-junction structure shown in Figure 1.1, the depletion of P and N columns in lateral direction happens very fast due to their thin widths W. After the lateral depletion completes, the whole drift region supports the voltage just like a capacitor with fixed thickness. As long as the charge is balanced, the doping concentration within the columns can be as high as possible if it does not induce immature breakdown in the lateral direction. Therefore, the breakdown voltage can be independent from the doping concentration in the drift region and only dependent on the thickness and designed column width.

\begin{figure}[h]
\centering
\includegraphics[width=0.3\textwidth]{super-junction_structure.png}
\caption{Super-junction Structure}
\end{figure}

Assuming the lateral and vertical critical fields are the same $E_C$, the maximum allowed doping in either P or N column is $N_d = \varepsilon E_C / q W$. The thickness of drift region can be given by $T_d = B V / E_C$, thus the specific on resistance can by given by:
Therefore, $R_{on,sp}$ only linearly increases with BV instead of parabolically. With assumption of Si $\mu=1000\text{cm}^2/\text{Vs}$, $E_C=0.25\text{MV/cm}$ and SiC $\mu=800\text{cm}^2/\text{Vs}$, $E_C=2.7\text{MV/cm}$, a comparison of Si Super-junction device and SiC device are shown in Figure 1.2. The $R_{on,sp}$ of super-junction can be $<10X$ larger than SiC’s at 600V range. Due to process limitations that the super-junction has to be fabricated with multiple steps of implantation and epi-regrowth, super-junction devices are very hard to exceed 900V. Therefore, the use of SiC active switches is not very attractive when the voltage is lower than 1.2kV when considering the cheap cost of Si. For diode applications, SiC has become a competitive solution compared with Si fast switching diodes due to the simple structure and zero reverse recovery charge of high voltage SiC Schottky devices. The application of SiC diodes with CoolMOS switches becomes widely accepted approach to minimized the 600V-class system losses[6].

**Frequency Capability**

Besides BV and $R_{on,sp}$, the frequency capability of devices are also important as higher frequencies are usually desired in power electronic systems to reduce the size of the passive components. However, the conduction loss and switching losses of the power switches are negatively correlated with each other. Because the switching losses are generally limited by voltage fall time that can be determined by $t_f = Q_{gd}/i_{g,av}$, the total loss of a switching unipolar device can be given by:

$$P_{loss} = \frac{I_{\text{rms}}^2 R_{on,sp}}{A} + V_D I_D \frac{Q_{gd,sp}A}{i_{g,av}} f$$  \hspace{1cm} (1.6)
where the first term stands for the conduction loss, the second term for switching loss, $A$ is chip area, $Q_{gd,sp}$ is the specific gate-drain charge and $i_{g,av}$ is the average gate driving current. When $P_{loss}$ is minimized at $\partial P_{loss}/\partial A = 0$,

$$P_{loss} = \{2I_{rms}\sqrt{V_D I_D f/i_{g,av}}\} \sqrt{R_{on,sp}Q_{gd,sp}}$$

(1.7)

Based on Eq. 1.7, Dr. Alex Q. Huang proposed a device FOM in 2004 that can be used to evaluate the total loss performance of the various unipolar devices[7]. This FOM is expressed as:

$$HDFOM = \sqrt{R_{on,sp}Q_{gd,sp}} = \sqrt{R_{on}Q_{gd}}$$

(1.8)

Because $Q_{gd,sp} = k\varepsilon E_C \sqrt{V_D/BV}$ according to Gauss’s law, the minimized $P_{loss}$ can further expressed as:
\[
    P_{\text{loss}} = \frac{4I_{\text{rms}}(V_D BV)^{\frac{3}{2}} \sqrt{k_{Df}}_{\text{ig,av}}}{E_C\sqrt{\mu}}
\]  

(1.9)

where the denominator is material determined parameters and the nominator is the operation condition determined terms. The denominator is recognized as a FOM for the total switching loss of devices:

\[
    HMFOM = E_C\sqrt{\mu}
\]

(1.10)

The optimum chip area at minimized power loss also has a denominator of material determined parameters expressed as:

\[
    HCAFOM = \varepsilon E_C^2\sqrt{\mu}
\]

(1.11)

If the FOM’s of different materials are normalized against silicon, the corresponding performances of new material power semiconductor devices can be easily compared in Table 1.1. According to BFOM, the SiC device can also have 484X reduction in \( R_{\text{on,sp}} \) compared with Si device with the same breakdown. The SiC unipolar switch can have a factor of 8X reduction in the total loss, and 60X reduction in chip sizes when compared with Si counterparts with same voltage and current ratings.

As the voltage level goes higher, it would not be fair to compare the Si and SiC unipolar devices. For high voltage Si device (>1kV), unipolar device design is impractical due to the forbiddingly high resistance and self-heating. Bipolar design like PiN diode, IGBT or thyristors has to be used. However, the removal of excess carriers in the drift region also introduces big amount of losses during switching.

A comparative experimental study of turn-on and turn-off losses of 10kV SiC MOS-
Table 1.1: FOM’s of Various Semiconductor Materials (Normalized Against Silicon)

<table>
<thead>
<tr>
<th>Material</th>
<th>$\mu_n$ (cm$^2$/V·s)</th>
<th>$\varepsilon$</th>
<th>$E_C$ (kV/cm)</th>
<th>BFOM $\epsilon\mu E_C^3$</th>
<th>HMFOM $E_C\sqrt{\mu}$</th>
<th>HCAFOM $\epsilon E_C^2\sqrt{\mu}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>1,000</td>
<td>11.7</td>
<td>300</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>GaAs</td>
<td>8,500</td>
<td>13.1</td>
<td>400</td>
<td>22.6</td>
<td>3.9</td>
<td>6</td>
</tr>
<tr>
<td>4H-SiC</td>
<td>800</td>
<td>9.7</td>
<td>2,700</td>
<td>484</td>
<td>8</td>
<td>60</td>
</tr>
<tr>
<td>GaN</td>
<td>900</td>
<td>9</td>
<td>3,200</td>
<td>840</td>
<td>10</td>
<td>83</td>
</tr>
<tr>
<td>Diamond</td>
<td>2200</td>
<td>5.7</td>
<td>5,700</td>
<td>7351</td>
<td>28</td>
<td>261</td>
</tr>
</tbody>
</table>

FET and 6.5kV Si IGBT at 3kV DC bus voltage is shown in the Figure 1.3. The switching losses of the SiC MOSFET are around 10X higher than those of Si IGBT’s. The estimated switching frequency of 10kV SiC MOSFET can be 7-10X higher than Si IGBTs for Dual-Active-Bridge or Rectifier applications[8].

![Figure 1.3: Comparison of Switching Loss of 6.5kV Si IGBT and 10kV SiC MOSFET](image)
1.1.2 The Reliability Performances

Due to the wide band gap of SiC and small thermal generation of intrinsic carriers at high temperature, the SiC power devices are extremely temperature stable. Its high breakdown electric field and high thermal conductivity also improve the power handling capability at the transient operations at extreme conditions such as surge current and unclamped inductive switching (UIS).

Theoretically, the critical temperature that disrupts the semiconductor devices is usually defined as one where the device junction barrier becomes zero [9] or the intrinsic carrier density $n_i$ is higher than drift region doping[10]. Considering a typical P+/N junction that has doping of 1e19 cm$^{-3}$ and 2e13 cm$^{-3}$, the built-in potential can be estimated by the following equation:

$$\Phi_{bi} = \frac{k_B T}{q} \ln \left( \frac{N_A N_D}{n_i^2} \right)$$  \hspace{1cm} (1.12)

The variation of $\Phi_{bi}$ at elevated temperature is shown in Figure 1.4. The Si p-n junction has a critical temperature of around 650K while the critical temperature of SiC p-n junction is 1800K. Due to the high critical temperature of SiC p-n junction, the failure temperature of a SiC power device is usually limited by other factors like aluminum metallization or gate oxide.

Surge Current Capabilities

Power semiconductor devices, especially diodes, are usually surge current rated for reliable operations. For Si diodes, the failure mechanism is usually limited by high intrinsic carrier generation that leads to thermal runaway. For SiC diodes, the failure mechanism is different and the surge current capability is limited by mobility degradation at ele-
vated temperature. The on-resistance of a unipolar device at high temperature can be estimated by

$$R_{on} = R_{on,300K} \left( \frac{T}{300} \right)^\alpha$$  \hspace{1cm} (1.13)

where $R_{on,300K}$ is the resistance at room temperature and $\alpha$ is the temperature coefficient of mobility degradation usually around 2.4. The maximum junction temperature rise can be expressed as:

$$\Delta T_j = I_{rms}^2 R_{on}\theta_{ja} = I_{rms}^2 R_{on,300K}\theta_{ja} \left( \frac{300 + \Delta T_j}{300} \right)^\alpha$$  \hspace{1cm} (1.14)

where $\theta_{ja}$ is the junction-to-ambient thermal impedance. The positive feedback loop can be observed from this equation: the junction temperature rise leads to increased resistance that further produces joule heating at constant RMS current and leads to higher temperature. When $\partial I_{rms}/\partial \Delta T_j = 0$ in Eq. 1.14, a finite current load would lead
to infinite temperature rise, indicating a thermal runaway kick-off temperature\cite{11}:

\[ \Delta T_{\text{max}} = \frac{300}{\alpha - 1} = 214 \ (K) \quad (1.15) \]

This temperature is a critical temperature, beyond which the load current cannot increase any more. The I-V trajectory of a 600V SiC Schottky diode at an 8.3ms half sinusoidal voltage pulse shows in Figure 1.5. The current peaked slightly below 4000 A/cm\(^2\) and started to fall even though the voltage was still increasing. If a high inductive current pulse was applied, e.g. in the start operation of an electric motor, very high forward voltage would be induced and thermal runaway would happen.

This issue was solved by introducing bipolar current conduction within the device, e.g. using SiC Junction-Barrier-Schottky (JBS) or Merged-PiN-Schottky (MPS) structure that includes an active p-n junction. Because the ambipolar lifetime increases at high temperature, the bipolar conductivity gets enhanced at surge current. The total device resistance becomes a result of competition of reducing drift region resistance and increasing substrate resistance where there is lack of conductivity modulation. A typical experimental I-V trajectory of SiC JBS diode at an 8.3ms half sinusoidal voltage pulse is shown in Figure 1.6. The device could withstand 140J/cm\(^2\) energy at the surge current.

The failure in these conditions are all thermal related and limited by metallization material instead of the SiC itself. The melting of the metallization or electromigration at wire-bonding site/edge termination can disrupt the device or seriously degrade its performance\cite{12}. Because the metallization failure in single surge event require temperature at near 1000K, much higher than the critical temperature of Si at 650K, the single surge capabilities of SiC devices are much better than Si counterparts.
Figure 1.5: The I-V trajectory of a 600V SiC Schottky diode

Figure 1.6: The I-V trajectory of a 600V SiC JBS diode
Avalanche Capability

Avalanche is a common stress for power devices in hard switching circuits and can happen at some fault conditions like unclamped inductive switching. Figure 1.7 shows a typical avalanche waveform for a 600V SiC JBS diode. At the transient of avalanche operation, the device was stressed at very high power and became conductive in reverse direction after failure (lost blocking capability). Its capability to survive the avalanche energy is highly dependent on device design and material properties.

![Avalanche Waveform](image)

Figure 1.7: Typical avalanche failure waveform of a SiC diode

Because the avalanche current goes through the weakest point first, the external inductive load can force current crowding at a local area within the chip and result in a small energy tolerance. Therefore, the breakdown of the device’s active cells and edge termination have to be carefully designed. It is desired to design lower BV for active cells and higher BV for edge termination in order to have the avalanche energy shared uniformly at active cells that usually have larger area than edge termination structure.
Take 600V SiC JBS diodes for example, the device whose breakdown initiated at active area could tolerate 5X higher single avalanche energy than one failed at the corner of edge termination[13], as shown in Figure 1.8.

Figure 1.8: Energy tolerances of 600V 8A SiC devices that avalanche at active area vs. edge termination

Besides the device design, the avalanche capabilities of power devices is also very dependent on the material properties. Because the critical temperature of SiC p-n junction is as 3X as that of Si, SiC devices can tolerate much higher transient power. The 1D heat equation is shown below:

$$\frac{\partial T}{\partial t} = \lambda \left( \frac{\partial^2 T}{\partial x^2} \right) \tag{1.16}$$

where $\lambda$ is the heat diffusivity given by:

$$\lambda = \frac{\kappa}{c_p \rho} \tag{1.17}$$

$\kappa$ is thermal conductivity (W/(cm-K)), $\rho$ is mass density (g/cm$^3$), $c_p$ is specific heat
capacity \((J/(g-K))\). At a high power transient, the heat diffuses from junction to case and causes temperature rise along the path. An good estimated solution for this equation can be derived in a lumped distance given by:

\[
l_T = \sqrt{\lambda \tau}
\]  

where \(\tau\) is the duration of the high power transient. The Eq. 1.18 gives an estimated range that the heat can diffuse during the short pulse. The maximum temperature rise in the device can be then given by:

\[
\Delta T_{max} = \frac{E}{c_p \rho l_T A_{eff}}
\]  

where \(E\) is the total energy of the pulse and the \(A_{eff}\) is the effective area that swallowed the energy. Assuming the edge termination area is 1/10 of active area, the maximum temperature rise for the device with avalanche initiated at edge termination would be 10X of that for a device of the same size with avalanche initiated at active area.

For well designed Si and SiC devices whose avalanche energies are uniformly shared, the maximum power density versus pulse duration limited by their critical junction temperature (1800K for SiC and 650K for Si) can be plotted in Figure 1.9. It is predicted that the maximum transient power density of SiC limited by thermal breakdown is around 10X of Si.

**Safe Operating Area**

The safe operating areas (SOA) of power semiconductor switches are very important operational boundaries on the I-V plane. Depending on the gate biases, the SOA’s are usually divided into Forward Biased SOA (FBSOA) and Reverse Biased SOA (RBSOA).
Figure 1.9: The maximum allowed power density vs. pulse width for SiC and Si devices

FBSOA is the operational limits of the device when the gate is forward biased and RBSOA is, in contrary, limits when the gate is reverse biased.

The failure mechanisms outside of these SOA boundaries, in most case, are due to reduced breakdown voltage at high current, which is called dynamic breakdown. Because of the high current and high field, the carriers are moving at saturated velocity in the drift region, the effective space charge can be given by:

\[ N_{\text{eff}} = N_d + \frac{J_p}{v_{p,\text{sat}} q} - \frac{J_n}{v_{n,\text{sat}} q} \]

where \( J_p \) is hole current density, \( J_n \) is electron current density, \( v_{p,\text{sat}} \) and \( v_{n,\text{sat}} \) are the saturation velocities of holes and electrons. The dynamic breakdown voltage can be estimated from:
The actual dynamic BV will be even smaller if the avalanche current is amplified by the transistor gains within the device or the electric field is not evenly distributed. Because SiC has 10X higher $E_C$ and comparable carrier saturation velocities to those of Si, the dynamic avalanche voltage of SiC is approximately 100X better than Si.

The Si power BJT was replaced by Si MOSFETs and IGBTs in 1970s due to the major issue of narrow RBSOA that can be described in Eq. 1.20 and Eq. 1.21. However, the SiC power BJTs have been reported to have a near square SOA and could handle as high as $3.7\text{MW/cm}^2$ during turn off [14].

SOA issues can also occur when parasitic devices are turned on by fault. In the N-type power MOSFET or IGBT, failure may occur when the parasitic NPN transistor or PNPN thyristor is turned on due to the debiased P-body at high current. For Si CoolMOS, the reduced FBSOA due to parasitic transistors have been reported[15]. However, similar issue has never been reported for SiC MOSFETs. A theoretical explanation can be that the built-in potential of the parasitic SiC NPN transistor is 3X higher than Si and it requires much higher current to forward bias the P-body/N$^+$ source junction.

### 1.1.3 Status of Commercialized SiC Power Devices

The first commercially available SiC device was the Schottky diode introduced in 2001 by Infineon Technologies and followed by introduction of Schottky diodes from CREE and ST Microelectronics. In March, 2006, Infineon Technology introduced its second generation thinQ! SiC Schottky diodes based on Junction Barrier Schottky (JBS) structure that can conduct bipolar current at surge operations.
It was observed that a special kind of defects, the Stacking Faults (SF), would grow within the epitaxial layer of SiC device at presence of bipolar current[16–18]. The SF defects increase the device forward voltage no matter it is in unipolar operation or bipolar operation[12, 13, 19]. Many efforts in epitaxial technologies have been done to successfully reduce the root cause of the bipolar degradation that is the basil plane defect (BPD) at the interface between epi-layer and substrate[20–22]. Up to date, the SF degradation issue has been solved and non-drifting GTO thyristors have been demonstrated[23].

The SiC wafer size has been continuously growing in the last decade. In May 2007, Cree Inc. commercialized a 4-inch Zero-Micropipe 4H-SiC substrate and, later in Aug. 2010, demonstrated high quality 6-inch 4H-SiC substrate. At the time of this thesis, the 6-inch 4H-SiC wafer has become commercially available and related companies are actively upgrading their production lines to process these wafers. As the wafer size becomes larger and larger, the prices of the SiC devices have been cut to price ranges of high-end silicon devices. In 2013, large area SiC power devices up to 2cm$^2$ have been demonstrated[24].

Due to the improvement of the MOS channel mobility[25–27], 1200V class SiC MOSFETs have become commercially available from Cree and Rohm. 1200V class SiC JFETs and BJTs have also become available from other game players like Fairchild, UnitedSiC and GeneSiC, adding diversity to this industry.

1.2 FREEDM System and SiC Power Devices

The Future Renewable Electric Energy Distribution & Management (FREEDM) system is a new and paradigm shifting power grid infrastructure that integrate the legacy grid, the Distributed Renewable Energy Resources (DRER), and the Distributed Energy Storage Devices (DESD)[28].
As is shown in the Figure 1.10, the 120V low voltage residential class DRER and DESD loads are connected to the 12kV bus through the intelligent energy management (IEM) subsystem whose core is the solid-state transformer (SST) based on post-silicon devices (both SiC and GaN power devices). An intelligent fault management (IFM) subsystem will be used to isolate potential faults. IEMs and IFMs will communicate with each other by a Reliable and Secured Communication (RSC) network. The brain of the FREEDM system will be provided by the Distributed Grid Intelligence (DGI) software embedded in each IEM and IFM.

The goal of the IFM system is to execute command from DGI to interrupt the fault on the 12kV AC bus as fast as possible so as to minimize damages. A schematic view of a single phase power distribution system is shown in Figure 1.11. The fault interruption devices (FID), as the major hardware of the IFM system, are made of solid-state switches that can be turned off much faster than the conventional bulky mechanical breakers.

The main solid-state switches are required to blocking 10kV peak phase voltage and
1.3 Fault Interruption Devices

1.3.1 Mechanical and Solid-State Circuit Breakers

Conventional solutions in legacy power grid dealing with short-circuit protection are the bulky mechanical circuit breakers (in Figure 1.12). After having detected a short-circuit or an over-load situation, several periods elapses prior to open the switches mechanically. Subsequently, an arc occurs and the fault current continues. The current can only be quenched at its natural zero-crossing assuming that the plasma is significantly cooled down to avoid reignition. As a result, turning off a short-circuit relies on the mechanical movement and will take several line periods and more than 100ms. The main drawbacks of these classical solutions are the following[29]:

1) The peak current cannot be influenced. Therefore, all network components have to withstand the peak current during the switching period. This current reaches peak values, which are typically 20 times higher than the maximum operating current. After this peak, the current drops to the thermal (steady state) short-circuit current. This current is below the transient peak current value but can still reach values up to ten times the nominal value. This high current puts the components in the grid both mechanically and thermally under stress, which leads to oversizing, resulting in an increase of costs.
2) Mechanical circuit breakers have a maximum short-circuit current rating. This current limit forces the grid designers to limit the short-circuit power of the grid, e.g., by using additional line inductances. However, these measures also reduce the maximum transferable power and the stiffness of the grid, leading to an increase of voltage distortions.

3) The number of high-current short-circuit clearances is limited to about 10 to 15 times for mechanical devices.

4) During the short-circuit time, the voltage on the complete medium-voltage grid is significantly reduced. Due to the long turn-off delay of the breaker, sensitive loads require UPS support to survive this sag, which is costly and might not be feasible for a complete factory plant.

Solid-state circuit breakers based on high power semiconductors potentially offer enormous advantages when compared to conventional solutions, since a solid-state breaker is
able to switch in a few microseconds.

### 1.3.2 Silicon Solutions

As shown in Figure 1.13, the concept of the solid-state FID for FREEDM system center was demonstrated using six 6.5kV IGBT modules in series\[30\]. A lot of complicated circuit design were made: in each unit, two 6.5kV silicon IGBTs with freewheeling diodes were placed back-to-back to achieve symmetric blocking; in order to block 15kV safely, balancing resistors and capacitors were installed in each unit and were customly tuned to ensure synchronous switching of the three units in series. Besides the circuit complexity, the total forward voltage, $V_F$, of the FID is more than 18V due to the 3 levels of high voltage silicon devices in series.

### 1.3.3 Silicon Carbide Solution

The Gen-II FID has been demonstrated in FREEDM using SiC Emitter-Turn-Off (ETO) thyristors. Because the SiC ETO can only block high voltage in one direction, two SiC ETO/diode modules are connected in series and back-to-back for conducting and blocking the AC current bidirectional (Figure 1.14). More than 75% size reduction compared to
Figure 1.14: Schematics for Gen-II Silicon Carbide Based FID

Gen-I FID has been achieved. The forward voltage becomes around 10V with 6V from ETO and 4V from the anti-parallel diode, which is around half of Gen-I FID.

Further improvement is possible if using symmetric blocking SiC switches that may block high voltage in third quadrant operation and two of these switches antiparalled can realize conducting and blocking in both directions. Thus, the original two antiparalleled diodes in Gen-II FID can be omitted, which reduces the total forward voltage drop.

1.4 Outline of This Work

In this work, symmetric blocking SiC switches are proposed as the solid-state switching device for the Gen-III FID in order to reduce the conduction loss and simplify the system.

In chapter 2, a novel reverse blocking edge termination for SiC chip-size devices is proposed and experimentally demonstrate for the first time. The revere blocking edge termination reduces the forward voltage drop of the FID and simplifies its complexity.

In chapter 3, the state-of-art commercial SiC MOSFET and normally-off SiC JFET are test and their short-circuit current saturating capabilities are studied. A conclusion was made according to the results and analysis that the SiC JFET channel has better current saturating capability than that of SiC MOS gate channel. Therefore, the semi-
conductor switches in FID is desired to have a JFET channel due to its application conditions.

In chapter 4, the SiC field-controlled diode (FCD) is designed using TCAD simulation. A topology using the FCD in a cascode configuration with low voltage MOSFETs is proposed to optimize the conduction loss and simplify the gate driver.

Chapter 5 summarizes the process flow of the FCD fabrication and development of unit processes. The measurement results of the fabricated devices are presented and discussed in Chapter 6.

The future work is proposed in Chapter 7.
Chapter 2

Orthogonal Positive Bevel Termination

2.1 Review of Symmetric Blocking Technologies

2.1.1 Solution for Wafer-Size Devices

For high power silicon devices, such as thyristors, a common technique to realize high voltage blocking edge termination is the composite positive and negative bevels. As shown in Figure 2.1, the dot line is the depletion boundary when forward blocking junction \( J_1 \) is supporting voltage in the first quadrant operation. The bevel is defined as Negative Bevel since more material is removed on the highly doped side so that the depletion on the surface extends faster than at the bulk. The negative bevel is desired to be small in order to minimize the surface electric field. The maximum electric field on the bevel surface can be estimated from\([2]\):
Figure 2.1: Conventional composite bevels for symmetric blocking Si wafer-size thyristors

\[ E_{mNB} = E_{mB} \frac{W_N}{W_P} \sin(\theta_1) \]  

(2.1)

where \( E_{mB} \) is the maximum field in the bulk drift region, \( \theta_1 \) is the bevel angle of \( J_1 \), \( W_N \) and \( W_P \) are depletion widths on the two sides of \( J_1 \), whose ratio \( W_N/W_P \) is mainly dependent on the doping concentrations of N-drift region and P-base.

The dashed line is the depletion boundary when reverse blocking junction \( J_2 \) is supporting voltage in the third quadrant operation. The bevel is called Positive Bevel as more material is removed on the lightly doped side, resulting in greater extension of the depletion layer along the bevel surface when compared with the bulk [31]. The positive bevel does not require a very small angle to reduce the surface field, e.g. typical of 45° can reduce the surface field to only 41% of the maximum bulk field. The analytical model describing the dependence of maximum surface field on the bevel angle \( \theta_2 \) is given by:

\[ E_{mPB} = E_{mB} \frac{\sin(\theta_2)}{1 + \cos(\theta_2)} \]  

(2.2)
The manufacturing process of this composite bevel edge termination can be done in a two-step way. The reverse blocking positive bevel is usually formed by grit blasting the periphery of a spinning Si wafer [32][2]. The angle can be controlled by the gun tilt. The forward blocking negative bevel can be formed by abrasion of the wafer against a concave grinder to achieve very small angle, as shown in Figure 2.2. The small angle can be determined by the ratio of wafer radius to the radius of the concave curvature. The mechanical damages on the surface can be removed by the following wet etching of a thin layer of silicon.

![Figure 2.2: The negative bevel process](image)

However, this approach is not practical for SiC power devices because that the wafer-size SiC device can not be realized at the moment due to high wafer cost and lack of defect free SiC wafers. The high-yield device areas are limited to 0.1-0.5 cm² [33][34]. High
current SiC devices still require paralleling devices in module or on-wafer[35].

2.1.2 Solution for Si Chip-Size Devices

For silicon chip-size devices, the forward blocking edge termination can be formed by Junction-Terminations-Extension (JTE), Floating Field Rings (FFR) or other similar technologies. For reverse blocking edge termination, the available techniques are mainly trench isolation, deep diffusion isolation or deep wet-etched positive bevel[36], as shown in Table 2.1. The mechanism of isolation techniques including trench isolation and diffusion isolation is to extend the substrate junction up to the front side surface and enclose the bulk drift region so that the depletion at the edge of the deep substrate junction happens faster due to assisted depletion from the isolation p-n junction. The Si mesa etching technique is effectively a positive bevel edge termination that utilizes the curved etching profile.

The process compatibilities of these techniques for SiC power devices are also compared in Table 2.1. The trench isolation technique has been consider as most area efficient edge termination for commercial devices due to the high aspect ratio trench with more than 100µm depth and less than 15µm width[37]. The trench sidewall is doped in diffusion furnace and a shallow junction is formed so that the N-type bulk is enclosed by P-type Si. Compared with trench isolation, the diffusion isolation structure is much simpler, though sacrificing larger area, and can be easily fabricated by aggressive diffusion doping.

Though feasible processes for Si, these techniques become, unfortunately, impractical for SiC due to fabrication challenges such as virtually no dopant diffusion in SiC [38] and lack of an efficient deep reactive-ion-etching (deep RIE) process. If one fabricated a SiC trench isolation structure, the slow RIE rate of SiC would lead to a long process-
Table 2.1: Si reverse blocking edge termination structures

<table>
<thead>
<tr>
<th>Technology</th>
<th>Silicon Structure</th>
<th>Silicon Process</th>
<th>SiC Process Compatibility</th>
</tr>
</thead>
<tbody>
<tr>
<td>Trench Isolation</td>
<td>&lt; 15 μm</td>
<td>Deep RIE &gt;110 μm + Diffuse Doping</td>
<td>Hard lithography Wafer breakage during annealing</td>
</tr>
<tr>
<td>Diffusion Isolation</td>
<td>~ 350 μm</td>
<td>Deep Dopant Diffusion ~120 μm</td>
<td>Virtually no dopant diffusion</td>
</tr>
<tr>
<td>Si Mesa Etching</td>
<td>~ 300 μm</td>
<td>Wet Etch ~160 μm</td>
<td>No available Process</td>
</tr>
</tbody>
</table>
ing time\[39\]. Besides, the sidewall of the trench would have to be implanted and wafer 
breakage might happen during >1600°C activation anneal with deep trenches on the 
wafer. Even if the trench sidewall could be successfully doped without wafer breakage,
the following lithography processes would become difficult due to a non-flat surface and
require special photoresist coating techniques like spray coating\[40\].

The wet etch technique is also infeasible because the SiC wet etch is very slow and
leaves an SiO$_2$ layer on the surface that prevent from further reaction\[41\]. Although
30° to 80° bevels have been obtained on SiC by SF$_6$ / O$_2$ plasma etching with a wet-
etched SiO$_2$ layer as the mask \[42\], the etching selectivity of up to 6.5 is still not practical
for high voltage SiC devices with thick epitaxial layer.

2.2 Simulation of Orthogonal Positive Bevels

As discussed previously, conventional Si reverse blocking techniques are very hard to
be integrated to a SiC device fabrication process. Therefore, a new fabrication method
is needed for SiC reverse blocking power devices\[43\]. As it is common to fabricate a
wafer-size Si bevel edge termination using mechanical processes, it should also work if a
chip-size bevel edge termination is fabricated by dicing.

A 350\(\mu\)m thick N\(^+\) 4H-SiC substrate with 15.8\(\mu\)m thick 6.1\(\times\)10\(^{15}\) cm\(^{-3}\) P-type doped
epitaxial layer was available for experiment. In order to analyze the impact of the positive
bevel termination to SiC devices, two-dimensional numerical simulations of a NPN struc-
ture based the wafer specification were performed. As expected, the electric field on the
beveled surface was found to decrease with smaller bevel angles as shown in Figure 2.3
(a). The peak surface fields of 30°, 45° and 60° bevels are respectively reduced to only
31.5%, 42.5% and 54.1% of the maximum bulk electric field (which is given as 90° angle).
Figure 2.3: Theoretical analysis of positive bevel termination: surface electric field vs. bevel angle
Figure 2.4: TCAD 3-D simulation of orthogonal joint of two 45° bevels at 1100V

The 2-D simulations of all bevel angles predict the on-set of hard breakdowns at around 1050V due to field reach-through. The predictions of the analytical model described in Eq. 2.2 are in good agreement with the results of the 2-D numerical simulations as shown in Fig. 2.3 (b).

If the bevel termination is formed by the dicing process, the V-shaped trenches can only be straight lines and rectangular corners will be expected at the chip corners. In the case of most edge terminations, the breakdown could be initiated at the corners of the chip due to high junction curvature. For the proposed positive bevel termination, the corners of the chip are sharp right angles formed by two orthogonal saw cuts. In order to understand the impact of this structure, 3-D numerical simulations were performed for the case of 45° bevels. As shown in Figure 2.4, it was found that the extension of depletion layer at the corner of the two orthogonal bevels is even larger and the surface electric...
field is less. This is because that more drift region material is removed and the effective bevel angle is lower at the corner. This means that breakdown of the SiC devices at the corners of the chips can be even better protected than the edges by using the proposed orthogonal positive bevel termination and the maximum electric field is securely confined within the bulk.

2.3 Process Development of the Bevel Dicing

Dicing is widely used for both Si and SiC industry to separate the chips fabricated on a wafer. In most cases, the dicing streets are desired to be as narrow as possible to minimize the area loss while the roughness of the diced surface is not a big concern. In some special applications, dicing can be used to fabricate very smooth beveled surface for optical devices like beam splitters[44] or to make electromechanical devices like piezoelectric ultrasonic transducers[45].

The angle of a diced bevel is dependent on the shape of the diamond blade. The best available dicing saw and blade for this process is Disco™ DAD321 Automatic Dicing Saw and a 1mm thick 45° V-shaped diamond blade with 56mm outer diameter(Figure 2.5).

2.3.1 Surface Roughness

The surface of as-saw SiC and Si substrates are compared at Figure 2.6. The blade tip was 200µm below the sample surface (380µm wafer thickness) and 45° bevels were created on both sides. The SiC surface looked much smoother than Si. It is believed that the higher hardness of the SiC material (9.5 vs. 7 in Mohs scale) contributes to smoother surface in this grinding process.
2.3.2 Limitation of Dicing

In some situations, beveled surface across the whole wafer thickness is desired, e.g. fabrication a positive bevel as an alternative for shallow junction edge terminations like JTE or FFR. It was experimentally proven that dicing a 45° bevel through a Si wafer is feasible while not feasible for SiC wafers. The SiC wafer would shatter very badly during the dicing because SiC is much harder material and is very brittle. Figure 2.7 shows a comparison of diced Si chip and SiC chips. The corner of a SiC chip is lost after dicing.

In order to find the range of safe dicing depth that would not shatter the SiC wafer, a test has been carried out on a 380µm SiC sample. As shown in Figure 2.8, it was found that the SiC sample would not shatter if the substrate had only 50µm SiC left below the blade tip. Because dicing more close to the bottom surface is hard to be controlled precisely, it is believed that the SiC chip would not shatter if it was not diced through.
Figure 2.6: SEM Picture of diced (a) SiC and (b) Silicon substrates
Figure 2.7: Feasibility of dicing through a Si wafer vs. a SiC wafer

Figure 2.8: Test for safe dicing
2.4 Experimental Demonstration

2.4.1 Fabrication Processes

A 350µm thick N+ 4H-SiC substrate with 15.8µm thick $6.1 \times 10^{15} \text{ cm}^{-3}$ P-type doped epitaxial layer was used for experiment. Two test structures have been fabricated: a NPN symmetric blocking structure with forward blocking Junction-Termination-Extension (JTE) and a P$^+P^−N^+$ diode. Both structures use the OPB termination for their reverse blocking (Figure 2.9).

The alignment marks were first etched in plasma. Three implantation steps that form the P$^+$ anode, N$^+$ contact and N$^−$ JTE were carried out at room temperature using photoresist as the masks. The implantation schedules are listed in Table 2.2.

After the implantation processes, an activation anneal with graphite encapsulation at
Table 2.2: Implantation schedules for N-, N+ and P+ implantation

<table>
<thead>
<tr>
<th>Implantation</th>
<th>Implant Energy (keV) / Dose (cm(^{-2}))</th>
<th>Peak Concentration (cm(^3)) / Junction Depth (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>N-</td>
<td>40, 100, 200, 350 / 1, 2, 2.5, 3.5 (\times 10^{12})</td>
<td>(1.5 \times 10^{11}) / 0.66</td>
</tr>
<tr>
<td>N+</td>
<td>20, 40, 65, 120 / 80, 3, 5, 12 (\times 10^{13})</td>
<td>(2 \times 10^{20}) / 0.36</td>
</tr>
<tr>
<td>P+</td>
<td>30, 70, 140 / 80, 5, 12 (\times 10^{13})</td>
<td>(2.5 \times 10^{20}) / 0.33</td>
</tr>
</tbody>
</table>

1700°C for 30 minutes was performed at Cree Inc. and followed by the thermal growth of 50nm gate oxide as the surface passivation. The wafer was further passivated with 1µm of PECVD SiO\(_2\) at Duke University.

After the contact openings were etched by buffered-oxide-etch (BOE), 70nm of Nickel was sputtered and patterned for the N-type ohmic contact on both sides of the wafer. The wafer was then annealed at 1000°C for 2 minutes to form Ohmic contact. Nickel of the same thickness was also used for P-type ohmic contact and was annealed at 660°C for 5 minutes. The 0.5µm Ti/Ni/Au deposited by E-beam evaporator was used for metallization on both sides of the wafer. The front side metal was patterned by lift-off process with 3µm negative photo.

Thereafter, the positive bevel edge termination was formed by sawing 100 microns deep V-shaped trenches into the SiC wafer using the diamond coated blade with a 45° angle. The SiC wafer was cut into 3 mm × 3 mm squares.

A reactive-ion-etch (RIE) of SiC was performed to remove the surface damages introduced by the sawing.
2.4.2 Results and Discussions

The breakdown voltage of the p-n junction was measured on a probe station at room temperature. The wafer was put in a chuck filled with Fluorinert liquid. The blocking voltages of NPN structure were measured up to 1100V with Keithley 2400 and the BV of the \( \text{P}^+\text{P}^-\text{N}^+ \) diode was measured with Tektronix 371B curve tracer.

Symmetric Blocking NPN Test Structure

The as-sawed OPB termination supports 1kV as limited by field reach-through predicted by the simulation. Even without removal of the surface damage from sawing, the leakage currents were around 10\( \mu \)A/cm\(^2\). It was observed that the leakage current got reduced after a RIE treatment that remove 0.3\( \mu \)m of the bevel surface. As shown in Figure 2.10, the leakage current of the same die was reduced by around two orders of magnitude, which was widely observed for almost all the samples. A histogram of leakage current reduction of all the NPN structures is provided in Figure 2.11.

The surface morphologies of SiC substrate before and after RIE treatment are shown in (a) and (b) of Figure 2.12. Small white particles were left on the surface of as-saw SiC substrate, which were believed to be diamond dusts introduced from the blade due to the comparable hardness of SiC and diamond. Scratched lines were also formed due to the finite mesh size of the diamond grits on the blade. After RIE, these particles are removed and surface become smoother.

The forward breakdown voltage provided by JTE edge termination was measured to be the same as the reverse since it was also determined by the field reach-through. The I-V characteristics of a RIE treated sample including blocking states in both directions are given in Figure 2.13. The leakage current introduced by the OPB termination at
Figure 2.10: The leakage current reduction of a typical sample after RIE treatment

Figure 2.11: The histogram of leakage current before and after RIE treatment
Figure 2.12: SEM Picture of SiC OPBs (a) before and (b) after RIE
reverse bias is in the same range of that at forward bias.

![Figure 2.13: The I-V characteristics of symmetric blocking NPN structure](image)

**P⁺P⁻N⁺ Diode**

Though the intended application of the proposed OPB termination is to make reverse blocking SiC switches, the wafer could realize higher $BV$ if a punch-through design was used as the avalanche field ($>2$MV/cm) is higher than the field at NPN transistor breakdown (around 1.6MV/cm). Therefore, the OPB termination can also be applied to P⁺P⁻N⁺ punch-through diodes for pulsed power applications. The pulsed power generator desires a "snappy" diode with high reverse peak current and hard reverse recovery in order to shape the high power pulse[46].

The blocking characteristics of the P⁺P⁻N⁺ diode is shown in Figure 2.14. According to the Synopsys TCAD numerical simulation, the P⁺P⁻N⁺ diode has a parallel-plane breakdown of 1932V and a critical electric field of 2.1MV/cm based on the impact ion-
The avalanche breakdown was measured to be 1610V, 83.3% of ideal parallel plane breakdown given by simulation. The result indicates that the OPB termination is able to support the high electric field at avalanche operation.

Area Efficiency and Extended Applications

The OPB edge termination is very area efficient comparing with other edge termination technologies. In most edge termination technologies, the length of edge termination is usually at lease as 3X as the drift region thickness[49] and commercial devices sometimes can require the edge termination length as 10X as the drift region thickness (Figure 1.8). In contrast, the area consumption of the OPB termination is only 1X of the drift region thickness. Therefore, it is seding to apply this technology to asymmetric blocking devices as edge termination for front-side shallow junctions. However, it cannot be eas-
ily adopted for shallow junctions due to wafer shattering when cutting it through from bottom. Therefore, it is envisioned that, when making an OPB termination for shallow junctions on the front side of wafer, dicing the V-trench to a certain depth and finishing the rest of SiC with RIE process can safely separate the chips without shattering them.

2.5 Conclusions

The Orthogonal Positive Bevel (OPB) termination formed by dicing was timely proposed for the SiC symmetric blocking switches. The OPB concept has been experimentally demonstrated on a 1kV symmetric NPN structure and a 1.6kV P⁺P⁻N⁺ diode. The proposed OPB termination is formed by orthogonal dicing using a V-shaped diamond blade followed by removal of the surface damage with RIE. The as-sawed positive bevel termination can support 1000V with a leakage current of 15µA/cm². After dry etching 0.3µm of SiC on the surface, the leakage current was reduced to 0.15µA/cm².

It has to be noticed that the presence of a deep V-groove degrades photoresist coverage and patterning during device fabrication. Wafer breakage can occur due to the mechanical stresses introduced by the V-groove. Therefore, in order to integrate this process in SiC device fabrication, the bevel termination should be done in the end of the process flow as is common practice for fabrication of silicon thyristors. This technique can be used for any chip-size symmetric blocking devices such as IGBTs and thyristors. It is also suitable for P⁺P⁻N⁺ diodes for pulsed power applications.
Chapter 3

Current Saturation Capabilities of SiC Gate Structures

For solid-state switches (SSS) in fault interruption devices, the current saturation capability may bring extra benefits on fault management and device robustness at extreme conditions. When a short-circuit fault takes place at the load, the line current increases dramatically, leading to huge self-heating that can disrupt the SSS.

In conventional power electronic circuits, switches are desired to have low saturation current so that they can withstand the short-circuit operation. When there is a short-circuit, the high voltage and high current at drain or anode of a MOSFET or IGBT is detected and the controller clears the fault within 10µs . For silicon IGBTs, the short-circuit performance is usually limited by the junction failure temperature around 650K and the critical power density is around 2000kW/cm$^2$[9]. To improve the short-circuit performance, the saturation current of power switches are usually desired to be low to prevent excess self-heating[50].

Similar protection approaches can be applied to the SSS in FID and multi-segment
fault management can be done by having different saturation current at different node of the transmission line[51]. In Figure 3.1, the line current gets higher and higher when it becomes closer to the source ($I_3 > I_2 > I_1$). When there is a fault at the R1, FID1 is supposed to be triggered rather than FID2 and FID3 so that normal loads R2 and R3 are not affected by the fault. The operation can be realized by using a device with lower saturation current in FID1 and devices with higher saturation currents in FID2 and FID3, thus FID2 and FID3 would not need to react because the current is not high for them and FID1 can interrupt the fault by detecting its saturation mode operation.

![Figure 3.1: Fault management at different node of transmission line](image)

Therefore, good short-circuit capability is strongly desired for the FID application. The SiC devices are very promising in this application because they have shown significantly higher short-circuit capability compared to the silicon counterparts [52][53]. In order to understand the impact of gate structure on the short-circuit performance, two commercially available SiC MOSFET and normally-off SiC JFET rated at 1200V/0.1Ω were characterized from room temperature up to 125°C and their short-circuit capabilities were studied and compared under a 400V DC bus.
3.1 DC Characterization

The SiC MOSFET has an active area of 3.5mm × 3.5mm and the and that of SiC JFET is 2mm × 2mm. The samples were heated to 25°C, 50°C, 75°C, 100°C, and 125°C on a hot plate when their DC characteristics were measured with Tektronix 371A curve tracer. The pulsed current test has a pulse width of 250µs and a repetition frequency of 15Hz.

3.1.1 DC Characteristics of SiC MOSFET

The 1200V SiC MOSFET has a specific resistance of 11mΩ·cm² with $V_g = 20V$ at room temperature. As is shown in Fig. 3.2, the SiC MOSFET current saturates very slowly with a gate bias from 10V to 20V. An interesting phenomenon has to be noted that the drain current at $V_g = 10V$ increases at elevated temperature but it decrease with the temperature at $V_g = 20V$. This was caused by the competition between the channel resistance, $R_{ch}$, with negative temperature coefficient and the drift region resistance, $R_{drift}$, with positive temperature coefficient [54],[55]. At lower gate bias of 10V, the low inversion charge in the channel resulted in a high $R_{ch}$ and limited the total $R_{on,sp}$. When temperature was increased, the effective channel mobility improved and reduced the $R_{ch}$ as well as the total $R_{on,sp}$. When the device gate was biased at a higher voltage of 20V, there is enough inversion charge induced in the channel and the device resistance is limited by $R_{drift}$ that increases with rising temperature.

Although $R_{drift}$ could reduce the on-state current at higher temperature, this part of resistance cannot contribute to current saturation because any carriers in the drift region would be quickly swept away by the high electric field and its differential resistance would become virtually zero. Therefore, the MOS gate channel has to limit the $I_{sat}$ of SiC MOSFET during the short-circuit and the temperature dependence of its mobility.
and the threshold voltage, $V_t$, are key properties for the survival of the device. Though we could not measure the mobility directly, the increased device transconductance and reduced threshold voltage were observed at elevated temperature (Fig. 3.3). According to the ideal long-channel model, the drain saturation current can be written as:

$$I_{d,\text{sat}} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_g - V_t)^2 = \frac{1}{2} \beta (V_g - V_t)^2$$

thus, the transconductance, $g_m$ can be given as

$$g_m = \frac{\partial I_d}{\partial V_g} = \beta (V_g - V_t) = \sqrt{2\beta I_d}$$

This means at a fixed gate bias or saturation current, the higher $g_m$ indicates higher channel mobility. As is shown in Fig. 3.3, $g_m$ increased from 12.2A/V·cm$^2$ to 15.6A/V·cm$^2$ while the $V_t$ decreased at a very fast rate of $\sim$0.5V per 25°C. The changes in $g_m$ and $V_t$ are usually resulted by the oxide/SiC interface states or traps. Both of these changes lead to a higher saturation current, which is not desired for short-circuit operations.

The temperature dependence of SiC MOS gate has something to do with the interface states. As is shown in Figure 3.4, the interface states has to be filled by electrons before inversion happens[27]. The threshold at this circumstances can be expressed as:

$$V_t = V_{FB} + 2\phi_B + \frac{1}{C_{ox}} \left\{ \sqrt{2\varepsilon q N_A (2\phi_B)} + q \int_{E_i}^{E_i + \phi_B} D_{it}(E)dE \right\}$$

where $V_{FB}$ is the flatband voltage (including fixed charge effect), $\phi_B$ is bulk potential, $C_{ox}$ is the oxide capacitance, and $D_{it}$ is the interface-state density as a function of energy in the bandgap. The $V_t$ is shifted positively by the presence of the negatively-charged interface-states, assumed to be acceptor-like states above intrinsic energy level $E_i$. The
Figure 3.2: On-state characteristics of SiC MOSFET

Figure 3.3: Transfer characteristics of SiC MOSFET
interface states act as Coulomb scattering sites to reduce the channel mobility (lowering $g_m$) and cause negative shift in $V_t$ at elevated temperature[56].

\[
\text{ Figure 3.4: The SiC MOS gate energy band diagram}
\]

3.1.2 DC Characteristics of SiC JFET

The $R_{on,sp}$ of the SiC JFET is $3 \text{m}\Omega \cdot \text{cm}^2$ when $V_g$ is no less than $3 \text{V}$ at room temperature. Its DC characteristics are presented in Fig. 3.5 and Fig. 3.6. In Fig. 3.5, the $I_{sat}$ dropped lower as the drain voltage increased beyond $5 \text{V}$. This was because the curve tracer sweeps the current from zero voltage to $25 \text{V}$ with a pulse width of $250\mu\text{s}$ and repetition rate of $15 \text{Hz}$, the later measured points actually had higher junction temperature and higher resistance. Thanks to homogenous JFET channel and the significantly negative temperature coefficient of SiC bulk mobility, the drain current can saturate at a lower level as
the temperature goes higher, which would become very important in the short-circuit operation.

As stated previously, the $I_{sat}$ is mainly determined by channel mobility, threshold voltage and the gate bias. The reduced channel mobility can be further proved from Fig. 3.6, which shows the reduced $g_m$ of SiC JFET at rising temperature without any obvious change in the threshold voltage. It is worth noticing that the $g_m$ of SiC JFET is much higher than that of SiC MOSFET at any temperature. This is caused by the much higher bulk mobility than the MOS channel mobility, which is also the reason of the lower $R_{on,sp}$ of SiC JFET compared to the SiC MOSFET.

![Figure 3.5: Saturation characteristics of SiC JFET](image-url)

Figure 3.5: Saturation characteristics of SiC JFET
3.2 Short-Circuit Test Results and Discussions

The short-circuit capabilities were measured at gate driver voltages of 10V, 15V for SiC MOSFET and 10V for SiC JFET (though the gate bias was clamped to \( \sim 3V \) due to the built-in potential of the SiC pn junction). After each short-circuit test, there was a wait long enough to let the device cool back down to the room temperature before the next test.

3.2.1 Short-Circuit Operations of SiC MOSFET

As is shown in Fig. 3.7, when the SiC MOSFET gate was biased at 10V, the \( I_{\text{sat}} \) kept increasing in the first 15µs of the short-circuit operation due to the rising channel mobility with raised temperature. The current peaked at 530A/cm² and began to decrease afterwards. This was caused by the channel mobility change due to the dominant carrier scattering mechanisms at difference temperature. The electron channel mobility is limited
by Coulomb scattering at the interface traps whose effect reduces with increased temperature. The channel mobility increases even up to 600K according to previous report [54]. As temperature continued increasing, other scattering mechanisms with increased impedance on electron mobility (acoustic scattering, e.g.) would become dominant and reduce $I_{\text{sat}}$. With higher gate bias, it takes less time before $I_{\text{sat}}$ decrease because the device heats up faster. The $I_{\text{sat}}$ with 15V $V_g$ reached its peak, 1200A/cm$^2$, at 4μs from the beginning and then gradually decreased.

![Figure 3.7: Short-circuit behavior of 1200V SiC MOSFET at $V_g=10$V](image)

A 1-D numerical thermal dynamic simulation has been carried out to accurately estimate the junction temperature during the short-circuit operation. A 360μm thick 4H-SiC chip is simulated with an arbitrary power flow applied to the thermode on the front side of the chip and the backside grounded to 300K through a small thermal resistance representing that of the soldering pad and the plate. The thermal properties of 4H-SiC were calibrated and the temperature dependence of its thermal conductivity can be
described as:

$$\kappa = 4517 \times T^{-1.29}$$

where temperature T is Kelvins and the thermal conductivity \(\kappa\) in W/(cm·K)[57, 58]. Furthermore, according to Ref [59], the volumetric heat capacity can be expressed as:

$$C_v = 4.10 \times 10^{-9} \times T^3 - 1.22 \times 10^{-5} \times T^2 + 1.29 \times 10^{-2} - 0.685$$

where T is in Kelvins and \(C_v\) is in J/(K·cm³).

By applying the measured power density to the front thermode, the simulated junction temperatures and the measured short-circuit power density of SiC MOSFET at \(V_g\)=10V and 15V are presented in the Fig. 3.9. Though the short-circuit current peaks at 15µs and 4µs for \(V_g\)=10V and 15V respectively, the peak temperature at the peak is 620K for both cases. It agrees with the measured mobility increase at temperatures
up to 600K in the previous report [54]. As no measurement result has been reported at higher temperature, we assume the 620K is the critical temperature beyond which the channel mobility decreases with temperature.

Before destructed, the two SiC MOSFET samples tested at \( V_g = 10\text{V} \) and 15V withstood 13.3J/cm\(^2\) and 13.7J/cm\(^2\) of short-circuit energy respectively. The temperature profiles of them at moments of their failures are plotted in Fig. 3.10. As one can observe, the heat barely diffused beyond 150\(\mu\text{m} \). The melting temperature of aluminum, the main contact metal on the front side of the chip, is also marked in the plot. At this high temperature in the junction, the aluminum contact could be melted and result in the failure.

![Simulated junction temperature and measured power density](image)

Figure 3.9: Simulated junction temperature and measured power density
3.2.2 Short-Circuit Operations of SiC JFET

The short-circuit operation of SiC JFET is plotted in Fig. 3.11 with the current in log scale. Because no additional scattering mechanisms exist other than those in the bulk SiC material, $I_{\text{sat}}$ of SiC JFET reduced drastically by one order of magnitude from 1680A/cm$^2$ to 158A/cm$^2$ within 200$\mu$s. The device failed after 1.44msec of short-circuit operation and withstood 44.6J/cm$^2$ the energy. Right before the moment of failure, $I_{\text{sat}}$ was reduced to 50A/cm$^2$ by the high temperature.

A similar numerical analysis was done for the SiC JFET by adding a 1.1K/W thermal resistance to the chip’s backside as the same as the junction-to-case thermal resistance on the datasheet. The total time to failure, $t_{\text{fail}}$, is 1.44msec and the simulated maximum temperature during this period is plotted to the top x-axis of Fig. 3.12 and the temperature distributions at different times are plotted to the bottom x-axis in the same figure. The temperature increased to 650K within the first quarter of $t_{\text{fail}}$ but only increased by 100K during the rest time due to the reduced power density absorbed, which further
allowed the heat to diffuse deeper and be shared by a larger volume within the chip. Because of this, the junction temperature at the moment of disruption was much lower than that of the SiC MOSFET.

### 3.3 Conclusion

The SiC MOSFET can withstand a short-circuit time of 80µs at $V_g=10V$ and 50µs at $V_g=15V$. The saturation current of SiC MOSFET increases with temperature until the junction temperature get beyond 620K. For either case of the gate biases, the SiC MOSFET withstood around 13.5J/cm² and the junction heated up so quickly that the heat could not diffuse more than 150µm from the junction, which led to a local temperature exceeding the melting point of aluminum and resulted in the failure. In contrast, it took 1.44msec of short-circuit operation and 44.6J/cm² of energy density to disrupt the SiC JFET. Due to the significant decrease in $I_{sat}$ of SiC JFET, the temperature rise became
Figure 3.12: Simulated JFET realtime junction temperature (top) and temperature profiles at 1/4, 1/2, 3/4 and the end of $t_{\text{fail}}$ (bottom)

very slow beyond 650K and the heat could diffuse deeper to be absorbed by a larger volume within the chip. To sum up, due to the high mobility of JFET channel and its negative temperature coefficient, the $R_{\text{on,sp}}$ and $I_{\text{sat}}$ of SiC JFET are more optimized than SiC MOSFET for FID applications.
Chapter 4

Design of Symmetric Blocking FCD

As is concluded in the previous chapters, the JFET gate structure is more robust than MOS structure due to the negative temperature coefficient of the channel mobility and the more robust SiC p-n junction compared with SiC/SiO$_2$ interface. Therefore, a JFET channel switch with symmetric blocking and current saturation capabilities is desired. The device satisfying these requirements is the field-controlled diode (FCD). The FCD can operate like thyristor as well so is also known as field-controlled thyristor or static-induction thyristor[60]. Due to the high injection efficiency at the epitaxy/substrate p-n junction, the device is able to carry high current with low voltage drop but suffers from the high switching losses, thus it has been considered only suitable for low frequency power applications[61]. However, the FCD can be a good candidate for FID application since the switching frequency is only once per fault event.

In this chapter, a symmetric blocking FCD with lateral JFET gate structure is designed based on the specs of a 150µm P-type epitaxial wafer donated by Cree Inc.
4.1 Introduction to the P-type FCD

The FCD was first described by Houston et al. in 1976 [62] and was then extensively studied and improved by Dr. Baliga et al.[63–72]. The Si-based FCD has a vertical gate structure that is formed by diffusion. The blocking voltage is very dependent on the gate bias due to barrier lowering effect.

Figure 4.1 shows the proposed P-type SiC FCD: the cathode is the N$^+$ SiC substrate; P-type drift region is a thick epitaxy layer; and it has a P-type channel that is controlled by the N$^+$ gate close to the anode side. As a P-type depletion-mode device, the anode is usually the reference for gate voltage and it requires positive gate bias to turn off the device.

At on state operation, the device conducts bipolar current like a diode with holes coming from anode and electrons from cathode. To switch it off, a large gate current needs to be applied at the gate so that the electron-hole plasma at the drift region can be completely removed and the depletion region can build up under the gate.

At forward blocking state, the maximum blocking voltage between anode and cathode is dependent on the gate-anode bias $V_{ga}$. The ratio of blocking voltage to gate bias is called blocking gain. The blocking gain is mainly determined by the aspect ratio of the channel, $a=L_{ch}/T_{ch}$, doping concentration, $N_{ch}$, and the direction and strength of electric field. In this particular device structure, the aspect ratio can be high due to the process dimensions and the lateral JFET channel can be less subject to the barrier lowering effect from the strong vertical electric field. Therefore, the gate structure can obtain a very high blocking gain. A blocking around 500X has been previously demonstrated on 10kV SiC JFET using the same gate structure[73]. At reverse bias, the depletion starts at the cathode p-n junction and blocking is realized by OPB termination.
4.2 Design Trade-offs of the P-type FCD

A complete design flow of the P-type FCD is presented in this section. The simulation parameters are listed in the Appendix. According to the requirement of FID, the goal of optimization is to ensure the symmetric blocking voltage and minimize the forward voltage $V_F$. The current saturation capability of this structure is also discussed.

4.2.1 Design of Breakdown

The first step of designing a vertical power device is to properly choose the doping concentration and the thickness of the epitaxial layer of the SiC wafer to support the high blocking voltage. Generally, the avalanche breakdown can happen at the high electric field. It is usually defined as the avalanche multiplication factor, $M$, becomes infinite.
or, equivalently, the impact ionization integral equals to one. The critical electric field for avalanche breakdown can be given by [47]:

\[ E_C = \frac{2.49 \times 10^6}{1 - 0.25 \times \log_{10}(N_D/10^{16})} \] (4.1)

However, the breakdown for the proposed symmetric blocking device is limited by the open-base transistor breakdown that happens before impact ionization integral becomes unity[2]. Take a P-type FCD at forward blocking for example, the relation of the gate current and cathode current when anode is open can be expressed as below:

\[ I_G = \alpha_{NPN} I_C + I_L = I_C \] (4.2)

\[ I_G = I_C = \frac{I_L}{1 - \alpha_{NPN}} \] (4.3)

where \( I_L \) stands for the leakage current generated within the space charge region; \( \alpha_{NPN} \) is the open-base transistor gain, which is the product of cathode injection efficiency \( \gamma_C \), base transport factor \( \alpha_T \), and pre-avalanche multiplication coefficient \( M \):

\[ \alpha_{NPN} = \gamma_C \alpha_T M \] (4.4)

According to Eq. 4.3, the current could soar to infinite when \( \alpha_{NPN} \) equals to one. As \( M \) only needs to be a finite value for breakdown to happen, the open base breakdown voltage, \( BV_{CEO} \), is usually much lower than that of the avalanche limit and is a very common case for silicon BJTs and IGBTs.

For SiC NPN structure, the degradation of breakdown due to the transistor gain is a little different from silicon. The leakage current \( I_L \) comes from the space charge generation
current and can be expressed as:

\[ I_L = \frac{qn_i}{\tau_{SC}} \sqrt{\frac{2q\varepsilon V_r}{N_d}} \]  

(4.5)

where \( n_i \) is intrinsic carrier density, \( \tau_{SC} \) is space charge generation lifetime, \( q \) is electron charge, \( \varepsilon \) is semiconductor permittivity, \( V_r \) is the reverse bias voltage and \( N_d \) is drift region doping. Due to the large band gap of SiC, the intrinsic carrier concentration, \( n_i \), around \( 10^{-11} \) could mean that there is virtually no intrinsic carriers within the small volume of the device that is far smaller than \( 0.1cm^3 \). Thus, the \( BV_{ceo} \) is very close to the open emitter breakdown voltage \( BV_{cbo} \) as reported in many SiC BJTs[14, 74].

A over design is usually needed because the BV is lower than that calculated from ideal parallel plane after adding edge termination and active cells. A 20\% of over design is often needed. The calculation of device BV limitation for 150\( \mu \)m and 200\( \mu \)m epitaxial wafers are presented in Figure 4.2. When the drift region doping concentration, \( N_d \), is high, the device BV is limited by avalanche; when \( N_d \) is low, the BV is limited by field reach-through. To achieve a 20\% over design of a 15kV device, a \( BV_{pp} \) of around 18.5kV is needed. However, even with 200\( \mu \)m thick drift region, only a narrow range of \( N_d \) can achieve 18.5kV according to Figure 4.2. The thick drift region also brings challenges to epi-growth, such as controlling of doping and wafer bowing.

A 150\( \mu \)m \( 5\times10^{14}\text{cm}^{-3} \) P-type doped SiC epitaxial wafer was delivered for fabrication. A numerical simulation of the \( BV_{ceo} \) of the parallel-plane NPN structure on this wafer is shown in Figure 4.3 and the simulation parameters could be found in Table A.1. The leakage current increases with reduced lifetime as is predicted by the SRH recombination model. The breakdown happens at around 10kV for all cases because of the field reach-through.
Figure 4.2: Calculation of BV limitation for wafers with 150µm and 200µm epitaxial layers

Figure 4.3: TCAD simulation of 150µm $5 \times 10^{14} \text{cm}^{-3}$ P-type doped SiC epitaxial wafer: NPN open-base transistor breakdown
4.2.2 Saturation Current and Forward Voltage

The degree of freedom when designing the lateral JFET gate structure is mainly limited by the process feasibility. The buried gate (BG) is selectively doped using ion implantation and is followed by epi-regrowth of the P-layer and P\(^+\) layer on top. A anode can be then formed by a mesa etch. The BG is designed to be a box profile of 5\(\times\)10\(^{18}\) cm\(^{-3}\) and 0.5\(\mu\)m deep based on the implantation range of nitrogen at a maximum implantation energy of 350keV. The total dose of around 2.5\(\times\)10\(^{14}\) cm\(^{-2}\) is not only more than enough to stop the breakdown field and ensure high conductivity in the gate, but also well below the critical dose 1\(\times\)10\(^{15}\) cm\(^{-2}\) that can cause amorphization of the SiC crystal[75]. Because implantation damages can be caused by channeling ions at deep places below the junction[76, 77], it is assumed that 20ns of ambipolar lifetime in the region within 3\(\mu\)m below the buried gate is used to take into account the impact of these damages.

The channel doping concentration, N\(_{ch}\), and lateral channel length, L\(_{ch}\), determine many device specifications such as V\(_F\) and V\(_{cut-off}\) as well as I\(_{sat}\). Due to the lithography resolution and desired high aspect ratio, L\(_{ch}\)=2\(\mu\)m is chosen to study the impact of N\(_{ch}\) on these specifications. By assuming the bulk ambipolar carrier lifetime, \(\tau_a=1\mu s\), the simulated influence of N\(_{ch}\) on the V\(_F\), V\(_{cut-off}\) and I\(_{sat}\) is plotted in Figure 4.4 and listed in Table 4.1, where V\(_F\) is forward voltage at 300W/cm\(^2\) with V\(_{ga}\)=0 or -2.7V, V\(_{cut-off}\) is minimum gate bias required to block 9kV, and I\(_{sat}\) is the saturation current at 5kV forward anode-cathode bias. It was interesting to find that the V\(_F\) is independent of the channel doping when the gate-anode junction is floating or forward biased.

When V\(_{ga}\)=0, the gate pn junction is reverse biased at its built-in potential and the holes can only flow via the lateral channel. Therefore, higher N\(_{ch}\) enhances hole current from anode and improves conductivity modulation, reducing V\(_F\). However, because the
Figure 4.4: (a) the impact of $N_{ch}$ and $V_{ga}$ on $V_F$ and (b) the $N_{ch}$ on $I_{sat}$ at $V_{ga}=0$
Table 4.1: The impact of $N_{\text{ch}}$ to device performance

<table>
<thead>
<tr>
<th>$N_{\text{ch}}$ [cm$^{-3}$]</th>
<th>$V_F$[1] [V], $V_g=0$</th>
<th>$V_F$[1] [V], $V_g=-2.7V$</th>
<th>$V_{\text{cut-off}}$[2]</th>
<th>$I_{\text{sat}}$[3] [A/cm$^2$]</th>
</tr>
</thead>
<tbody>
<tr>
<td>$4 \times 10^{16}$</td>
<td>36.2</td>
<td>4.1</td>
<td>3.9</td>
<td>47.7</td>
</tr>
<tr>
<td>$7 \times 10^{16}$</td>
<td>6.0</td>
<td>4.1</td>
<td>7.6</td>
<td>636</td>
</tr>
<tr>
<td>$1 \times 10^{17}$</td>
<td>5.5</td>
<td>4.1</td>
<td>11.5</td>
<td>N/A</td>
</tr>
</tbody>
</table>

[1] $V_F$ was read at 300W/cm$^2$
[2] $V_{\text{cut-off}}$ is required gate bias to block 9kV [V]
[3] $I_{\text{sat}}$ was read at 5kV$_{ak}$, 0V$_{ga}$.

Gate control is weakened at higher $N_{\text{ch}}$, it requires higher voltage to cut-off the channel at blocking state. The saturation current at $V_{ga}=0$ also increases dramatically with $N_{\text{ch}}$, and the channel saturation capability is lost when $N_{\text{ch}}$ is more than $1e17$cm$^{-3}$.

On the other hand, if the gate is floating ($I_g=0$) or the anode-gate junction is forward biased ($V_{ga}=-2.7V$), the $N^+/P$ junction has no barrier for holes and allows holes to transport from $P^+$ anode to drift region directly via $N^+$ gate, equivalently putting the internal PNPN thyristor into operation (Figure 4.5). Thus, $V_F$ pins to 4.1V due to thyristor latch-up and become independent on $N_{\text{ch}}$. In this case, the device loses current saturation capability completely.

The mechanism can also be explained using the equivalent circuit model of this device (Figure 4.6). The P-type FCD incorporates a gate-cathode NPN transistor, an anode-drift PNP parasitic transistor and a P-type JFET. When the thyristor kicks-in, the channel is shorted and has no control over the current. When the thyristor is suppressed, the channel current limits the device conductivity and provides current saturation capability.

To sum up, the FCD can work in two mode: one is FCD mode, in which the lateral JFET channel controls the hole current injection and the device can have current saturation capability; the other is thyristor mode, in which the holes inject directly via buried
Figure 4.5: Diffusing of holes across the buried gate
gate and the internal PNPN thyristor latches up.

4.3 FCD Cascode Configuration and Use in FID

One possible approach to keep both $V_F$ and $I_{sat}$ low and to easily drive the device is using external switches to shift the operation modes. Two switches, e.g. low voltage (LV) P-type MOSFETs, are connected to the anode and the gate of the P-type FCD (Figure 4.7). It is possible to put the FCD into thyristor mode by turning off the gate switch and keep the anode switch at on-state. The FCD can be turned off by the opposite operation: turning on the gate switch and turning off the anode switch.

A non-isothermal simulation of thyristor mode turn-off has been done to evaluate
the turn-off of the configuration. As shown in Figure 4.8, the cascode configuration of a 1cm² FCD is in parallel with an MOV (Metal-Oxide-Varistor) that is used to absorb excess energy from the transmission line. The configuration usually operates at $V_F=4.1V$ and nominal current of 50A/cm². After a fault and the current surged to 3X of the nominal current, it turned off the fault current with only $60{^\circ}C$ temperature rise at the device junction. To let the FCD work in FCD mode, both LV MOSFETs are turned on and the configuration may have current saturation capability (Figure 4.9). Therefore, this configuration uniquely combines the advantages of FCD and GTO and adds another degree of freedom in fault control of FID.
Figure 4.8: Simulated thyristor mode turn-off of cascode configuration
4.4 Design of Edge Terminations

The device cannot block the high voltage without proper design of edge termination. The proposed symmetric blocking edge terminations and the device structure are plotted in Figure 4.10. The forward blocking edge termination is 3-zone Junction Termination Extension (JTE) and the reverse blocking edge termination is Orthogonal Positive Bevel proposed in Chapter 2.

4.4.1 Forward Blocking JTE Termination

A buried three-zone JTE has been proposed to serve as the forward blocking edge termination. The schematic of the JTE is shown in Figure 4.10. Every zone has an equal length of 150µm and the total JTE length is 450µm. The first zone (the closest one to the active area), the second zone and the last zone have triple, twice and once of the base implantation dose respectively. The base dose of $4 \times 10^{12} \text{cm}^{-2}$ was selected as the triple
of it is around the critical dose, $1.2 \times 10^{13} \text{cm}^{-2}$, for breakdown.

Because the P-layer is epi-regrown, its doping concentration could change due to the process variability. The performance of the proposed JTE termination has been simulated with different doping concentration in the P-layer. Figure 4.11 shows that the depletion in the 3-zone JTE would adapt to the variation of P-layer doping between each zone. The inner zones would support more voltage at higher doping of P-layer and the outer zones would support more voltage at lower doping. According to the simulation, the BV of the termination can tolerate ± 50% doping variation in the regrown layer and stay at 10kV as limited by field reach-through.
Figure 4.11: The stable performance of Buried Three-Zone JTE against CEL process variations

Figure 4.12: The potential contour mapping with $N_{ch} = 4 \times 10^{16} \text{cm}^{-3}$
4.5 Conclusions

In this chapter, the principles of FCD has been presented and the structural parameter are optimized based on the 150µm P-epi SiC wafer. The FCD is capable to operate in either FCD mode or thyristor mode depending on the gate bias. A cascode configuration with two LV switches respectively connected to the gate and the anode have been proposed to change the operation mode of the FCD.
Chapter 5

Process Development and Fabrication of FCD

In the previous chapters, the following work has been elaborate about developing a 10kV FCD: a 1100V reverse blocking Orthogonal Positive Bevel termination has been proposed and experimentally demonstrated on a thin SiC wafer; the short-circuit behaviors of the SiC MOS gate structure and SiC JFET structure are experimentally studied and it was concluded that the JFET channel is more temperature stable; a FCD with Buried Gate have been proposed and designed with numerical simulation tools. The next step would be fabricate this device using a 150µm SiC wafer donated by Cree Inc.

Due to the complexity of the FCD with CEL design, the fabrication demonstration is focused on FCD without CEL. In this chapter, process flow and test modules will be discussed in detail.
5.1 Process Flow

The process flow is shown in Table 5.1.

Unlike silicon devices whose alignment mark can be formed by etching oxide passivation, the SiC device’s alignment mark usually need to be done by etching SiC substrate because conventional passivation materials, even oxide or nitride, can not withstand the very high temperature (>1600°C) during implantation activation. The alignment mark is very desired at the first step of fabrication.

The following steps are Nitrogen implantation for buried gate and 3-zone JTE edge termination. Due to the low dose of implantation, 3µm thick photoresist was used for room temperature implant.

These implantation steps were followed by epi-regrowth of channel layer and anode layer. The P-type channel layer was designed to be epi-grown instead of implanting compensating ions into buried gate region. It is because that the implantation mask, either SiO₂ or photoresist polymers, can not have a perfectly straight edge and will introduce implanted ions to the surface under the sloped sidewall of the mask. Also because the buried gate is doped at 5×10¹⁸cm⁻³ and channel doping should be much lower so that it can be fully depleted, therefore, it is hard to counter-dope a highly doped region into 20X lower doping concentration using the charge compensation principle.

In addition, The P⁺ anode can also be epi-grown in the same step so that implantation damage and extra process steps can be avoided. Because the thickness of P-type channel layer Tch is limited by the implantation process of the plug that brings the buried gate to the surface contact. A 0.3µm Tch is chosen due to the ion implantation range of established process that uses up to 350keV implantation energy.

The first two implantation steps were done with Phosphorus instead of Nitrogen be-
cause the Phosphorus is easier to occupy silicon vacancies during silicidation and enhance active doping concentration that is good for ohmic contact[78, 79]. The implantation was done from lower energies to higher energies so as to reduce ion channeling and minimize crystal damages in the deeper area. After anode mesa, gate plug was formed by ion implantation at high temperature to serve electrical connection to the buried gate.

After activation anneal, initial passivation was formed using 50nm of gate oxide and additional PECVD oxide was deposited. Two layers of aluminum interconnect were patterned for gate and anode. The anode metal pad covers most of the chip region to reduce the resistance.

Due to convenience of photoresist patterning and mechanical strength, beveling the reverse blocking edge termination is desired to be done after all the major orthographical steps as stated before. In order to introduce passivation on the beveled surface, 1μm PECVD oxide was deposited and patterned using plasma etch with a plastic shadow mask.

### 5.2 Layout Design and Device Variations

In order to show the design variables in this device, lateral channel length $L_{ch}$ and JFET window width $W_{JFET}$ are varied from 1.5μm to 3μm and from 2μm to 5μm respectively.

Some test structures are also fabricated on the same wafer to extract process parameters. These include transfer length measurement (TLM) structures, resolution bars and anode-gate surface diodes, etc.
Table 5.1: The Process Flow of 8kV RB-FCD

<table>
<thead>
<tr>
<th>Step #</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PECVD 30nm oxide</td>
</tr>
<tr>
<td>2</td>
<td>Etch Alignment Mark (Mask.1)</td>
</tr>
<tr>
<td>3</td>
<td>Buried Gate implant (Mask.2) at room temperature:</td>
</tr>
<tr>
<td></td>
<td>Nitrogen, 5e13/5e13/8e13/1e14cm$^{-2}$@50/110/200/350keV</td>
</tr>
<tr>
<td>4</td>
<td>3-zone JTE implant (Mask.3-5) at room temperature:</td>
</tr>
<tr>
<td></td>
<td>Nitrogen, 6e11/9e11/1e12/1.5e12cm$^{-2}$@80/140/225/350keV</td>
</tr>
<tr>
<td>5</td>
<td>Epi re-growth: 350nm, 4e16cm$^{-3}$ P layer and 250nm, 2e19cm$^{-3}$ P+ layer</td>
</tr>
<tr>
<td>6</td>
<td>Anode Mesa (Mask.6)</td>
</tr>
<tr>
<td>7</td>
<td>Implant with 1.8µm oxide hard-mask (Mask.7) at 600°C:</td>
</tr>
<tr>
<td></td>
<td>Phosphorus, 1.5e15/2.5e15cm$^{-2}$@20/50keV</td>
</tr>
<tr>
<td></td>
<td>Nitrogen, 7e13/1e14/1.5e14cm$^{-2}$@50/110/200keV</td>
</tr>
<tr>
<td>8</td>
<td>Activation Anneal, 50nm thermal oxide, and 1µm PECVD oxide passivation</td>
</tr>
<tr>
<td>9</td>
<td>Deposit 100nm Ni on backside and 1000°C, 2min anneal</td>
</tr>
<tr>
<td>10</td>
<td>Pattern Gate (Mask.8), etch opening, lift-off Ni and 1000°C, 2min anneal</td>
</tr>
<tr>
<td>11</td>
<td>Pattern Anode (Mask.9), etch opening, lift-off Ti/Al and 900°C, 2min anneal</td>
</tr>
<tr>
<td>12</td>
<td>Pattern 1µm Al (Mask.10)</td>
</tr>
<tr>
<td>13</td>
<td>Deposit 1.5µm PECVD oxide</td>
</tr>
<tr>
<td>14</td>
<td>Pattern via (Mask.11)</td>
</tr>
<tr>
<td>15</td>
<td>Pattern 4µm Al (Mask.12)</td>
</tr>
<tr>
<td>16</td>
<td>Pattern Polyimide (Mask.13)</td>
</tr>
<tr>
<td>17</td>
<td>Reverse blocking bevel dicing and surface treatment</td>
</tr>
<tr>
<td>18</td>
<td>PECVD 1µm oxide and RIE pad opening with shadow mask</td>
</tr>
</tbody>
</table>
5.3 Unit Process Development

In this section, the process details for fabricating this SiC device is discussed.

5.3.1 Implantation and Impurity Activation

One of the most different processes of SiC from those of silicon is implant doping. Due to very small diffusion rate of dopant in SiC, the implant doping technique becomes that major doping method of SiC devices. However, implanted impurities in SiC require very high temperature above 1500°C to be activated. For P-type dopant like aluminum, the activation ratio is far from 100% even after annealed at 1700°C [80]. Luckily, this challenge is less a issue for p-type switches because the N-type doping that is usually desired in this case can be realized with Nitrogen, a dopant with high activation ratio close to 100%.

Estimation of Implantation Profile

A very accurate implantation profile can be calculated with Pearson IV model as shown in the following equation[81]:

$$P_{IV} = \frac{1}{M} \exp[-n \times \arctan(\frac{x - R_p}{A} - \frac{n}{r})] \times [1 + (\frac{x - R_p}{A} - \frac{n}{r})^2]^{-m} \quad (5.1)$$

where r, n, m, A are parameters related to species and implantation energy, and M is a fitting parameter related to the dopant dose. This model takes into account the channeling effect of implanted ions within the anisotropic crystal[81]. In the normal direction of 8° off-axis wafer, the channeling ions can shoot more than one fold deeper than normal ions and significantly push the junction depth further. These high-energy ions also introduce
lifetime-killing crystal damages down to deep ranges below the junction\cite{76}. This can greatly affect the forward characteristics due to change of doping gradient and lifetime.

However, the channeling ‘tail’ of the implantation profile does little matter if it is only active when depleted. The reason is that the specific charge density is predominate rather than the profile when estimating depletion or breakdown. If ignoring the channeling effect that introduce a low-doping “tail” at the end of the profile, the implanted ion profiles can be easily estimated with Gaussian distribution using parameters given by SRIM (Stopping and Range of Ions in Matter) Monte Carlo simulation.

The the first zone of JTE implantation is shown in (a) of Figure 5.1.

The buried gate and gate plug implant profiles are shown in (b) and (c) of Figure 5.1.

**Annealing During and After Implantation**

Due to the damage accumulation during the ion implantation process, a significant concentration of defects and lattice disorder are generated and inevitably lead to a regrowth of secondary defects or other polytype structures during postimplantation annealing. Also, defect-stimulated amorphization is the primary amorphization mechanism in SiC, which lead to high leakage, poor minority-carrier injection, and premature breakdown\cite{75, 82}.

Furthermore, because only the activated impurities can be ionized and taken into account in the Poisson equation, partially activated dopant with unknown ratio may add a lot of variability to the breakdown design when the blocking characteristics is highly dependent on charge coupling. This is a common difficulty when designing the Aluminum-implanted JTE edge termination\cite{49}.

These issues can be eased or completely solved by high temperature annealing during implantation. Ion implantation at high temperature was reported to significantly
Figure 5.1: SRIM implantation profiles of (a) JTE Zone-1, (b) Buried Gate and (c) Gate Plug

81
reduce amorphization and increase dopant activation rate[80, 83]. Considering the trade-off between time, cost and throughput, high temperature implantation around 600 °C is desired for high dose implantation steps, especially those for charge-sensitive doping, minority-carrier injectors/emitters and Ohmic contact areas.

After the implantation, a post-anneal is due in order to activate the dopant. Because of the forbiddingly high temperature of the anneal, graphite- or AlN-capsulation is needed to prevent sublime of SiC atoms from the substrate[38]. Or else, silane overpressure is preferred to anneal the “capless” wafer[84]. The post-anneal usually lasts for 30min at 1650-1750 °C.

5.3.2 RIE of Oxide as Hard Mask for Implantation

Due to the previously stated reason about high temperature implantation, a hard mask process is needed for this process because photoresist cannot stand the high temperature. PECVD oxide is a common option because it is thermally stable up to 1000 °C and easy to pattern (typically 33nm/min of deposition rate and similar speed of etching). In order to pattern the deposited oxide, an oxide RIE process was developed in-house using Semigroup RIE tool.

Plasma etching of SiO$_2$ is usually done by Fluorine-based chemistries. The overall reaction is given by:

$$4F + SiO_2 \rightarrow SiF_4 + O_2$$

Widely used carriers are CF$_4$ and CHF$_3$. CHF$_3$ leads to more straight sidewall profile compared with CF$_4$ because of the inhibitor deposition. In order to avoid enlarging implantation area, CHF$_3$ was chosen as the main etchant. Adding argon in the plasma can
Table 5.2: Oxide RIE Recipe

<table>
<thead>
<tr>
<th>Ar (sccm)</th>
<th>CHF$_3$ (sccm)</th>
<th>O$_2$ (sccm)</th>
<th>Power (Watt)</th>
<th>Pressure (mTorr)</th>
<th>SiO$_2$ etch (nm/min)</th>
<th>PR etch (nm/min)</th>
<th>SiC etch (nm/min)</th>
</tr>
</thead>
<tbody>
<tr>
<td>89</td>
<td>32.5</td>
<td>5</td>
<td>200</td>
<td>70</td>
<td>20</td>
<td>35.5</td>
<td>15</td>
</tr>
<tr>
<td>0</td>
<td>42.5</td>
<td>1</td>
<td>200</td>
<td>30</td>
<td>15</td>
<td>5</td>
<td>6</td>
</tr>
</tbody>
</table>

speed up the etching process due to physical etching from bombardment. Two etching recipe with and without argon is shown in Table 5.2. Be noticed that Fluorine-based chemistries also attack SiC because both Si and C atoms can react with the plasma and form volatile materials. Therefore, two steps are needed: the first RIE step does 90% of the etching and the second step is to use Buffered-Oxide-Etch to remove the residual. The lateral etching bias can be controlled within 20% of the total oxide thickness.

Because Semigroup RIE tool was designed for 8” wafer processing. When used to smaller sample, it develops a problem of micro-masking. Because the cathode metal, made of Aluminum that cannot form volatile compound in the plasma, can be sputtered up and re-deposit on the sample, these aluminum particles mask oxide areas to be etched and leave sharp cones on the etched surface (Figure 5.2). Although Hydrogen radicals can theoretically form volatile compound with Al, the micro-masking effect is still very bad due to relatively large area of cathode exposure (8” circle compared to 3” circle). Because of this, the whole cathode should be covered with materials that forms volatile compound in the plasma. It was found that 8” silicon wafer, for example, can serve this purpose very well and the thickness or resistivity of the silicon wafer does not affect the etching rate of the target SiO$_2$ or photoresist.
Figure 5.2: Oxide RIE: (a) with and (b) without micro-masking
Table 5.3: SiC RIE Recipe

<table>
<thead>
<tr>
<th>SF$_6$ (sccm)</th>
<th>O$_2$ (sccm)</th>
<th>Power (Watt)</th>
<th>Pressure (mTorr)</th>
<th>SiC etch (nm/min)</th>
<th>PR etch (nm/min)</th>
</tr>
</thead>
<tbody>
<tr>
<td>26</td>
<td>6</td>
<td>200</td>
<td>30</td>
<td>35.3</td>
<td>60</td>
</tr>
</tbody>
</table>

5.3.3 SiC Reactive Ion Etch

SiC RIE were used in three steps of this fabrication: the alignment mark, the anode mesa etch and the surface damage removal for bevel edge termination. The RIE recipe is shown in Table 5.3 and the equipment used was also Semigroup RIE tool. Like oxide RIE, SiC RIE in this tool also requires a cover material for the aluminum electrode of the tool to avoid micro-masking. This process has been proved to be repeatable. 8.5min of RIE delivers 300nm of SiC consumption and running 3 times of 8.5min RIE cycle with thicker photoresist can provide 0.9µm etch depth Figure 5.3. A microscopy view of anode mesa after RIE is shown in Figure 5.4.

5.3.4 Ohmic Contact to N- and P-Type SiC

The contact metal was patterned by lift-off process. Due to the wafer bowing, half of the wafer has around 20µm air gap from the mask even hard contact mode is used during lithography. The folding line was distinctly revealed during a failure in metal lift-off as shown in Figure 5.5. The lithography dose had to be tuned in order to lift off the metal across the whole wafer but some area was over-exposed and some under-exposed.

Popular Ohmic contact is either Nickel based or Al/Ti based system. For Nickel based Ohmic contact system, the optimized temperature for P-type and N-type SiC is usually around 800 and 1000 °C respectively. Because of the temperature difference, one
Figure 5.3: Plasma Etch of SiC: (a) 323nm after 8.5min and (b) 0.9µm after 3 cycles of 8.5min run
Figure 5.4: Microscopy of Anode Mesa

Figure 5.5: The folding line of wafer bowing. The line is farthest place from mask during lithography
metallization and annealing step cannot form both types of contact at once. In most cases, N-type Ohmic contact is very stable and repeatable using Nickel. Annealing at 1000 °C in low vacuum forming gas environment can provide $5.59 \times 10^{-5} \ \Omega \cdot \text{cm}^2$ as shown in Figure 5.6.

However, the P-type Ohmic contact is very sensitive to many variables and hard to reproduce. SiC samples patterned with 50/500nm Ti/Al in lift-off process were annealed for 2min at 800 °C, 900 °C and 1000 °C. The metal surface morphology looks very different after anneal Figure 5.7. Compared to mirror-smooth surface of as-deposited metal contact, the higher annealing temperature, the rougher surface and the more black compound is formed. The specific contact resistance reach a minimum value of $4.82 \times 10^{-5} \ \Omega \cdot \text{cm}^2$ around 900 °C Figure 5.8.

### 5.3.5 Backend Process: Thick Metal

Due the high current density of the bipolar device, thick metal is preferred to reduce the wire distribution resistance. As mentioned in previous chapter, the self-debias can be suppressed with lower gate resistance. The most common metals used in power devices is either gold or aluminum. Gold can be patterned with lift-off process up to 1µm using 3µm negative photoresist. For thicker metallization, gold could be too expensive. Therefore, aluminum thick metallization was developed for this purpose.

**Thick Aluminum Deposition**

In most cases, the metal deposition is done with sputtering or e-beam evaporation. However, the deposition rate is usually less than 0.5nm/s in order to prevent the equipment from serious self-heating. It would be very time-consuming to deposit 4µm of Al. Also, as
Figure 5.6: TLM measurement for N+ SiC Ohmic contact
Figure 5.7: Metal surface morphology at different annealing conditions: (a) room temperature, (b) 800 °C, (c) 900 °C and (d) 1000 °C

Figure 5.8: The P+ specific contact resistance on annealing temperature
the temperature goes up, the vacuum pressure increases and adversely affects the quality of the aluminum film because of its high reactivity of being oxidized. Furthermore, the metal source is likely to run out during the deposition and need be replaced. This may result in break of vacuum and would be very bad for the film quality, too. Therefore, a resistive-heated evaporator inside of a highly controlled nitrogen glovebox is used for this process. In the glovebox, the nominal moisture and oxygen are controlled to less than 0.1ppm. The evaporator has three source locations to allow for up to three metals. With all the three source locations fully loaded with aluminum, a total 4.5µm aluminum film can be deposited at a rate of more than 3nm/s.

Reactive-Ion-Etch of Aluminum

Usually metal is patterned by lift-off process that is to deposit metal on substrate prepared with patterned photoresist and then strip the photoresist in organic solvent. However, the patternable metal thickness is limited by the thickness of photoresist. The preferable photoresist thickness is at least as twice as the metal film thickness for easy process. If making 4µm thick metal, the photoresist would be more than 8µm. This thick photoresist will add a big difficulty in the lithography to resolve 2µm because of the high aspect ratio. Therefore, an RIE process of aluminum is very needed.

The widely used aluminum etchant is BCl$_3$/Cl$_2$ gas. The BCl$_3$ does more bombardment and effectively removes the hard Al$_2$O$_3$ layer on the surface. The Cl$_2$ provides more chemical etching. The Trion RIE tool with inductive coupled power (ICP) is used in this process. A DOE has been carried out to calibrate the process. 4µm of Al was deposited on silicon substrate covered with 2µm SiO$_2$. Comparing sample S1, S2 and S4 in Figure 5.9, the more lateral undercut in aluminum is formed with higher the Cl$_2$ concentration because of more reactive etching. Argon was reported to improve the selectivity
Table 5.4: Aluminum RIE DOE with fixed 300W ICP and 200W RIE power at 15mTorr

<table>
<thead>
<tr>
<th>Sample #</th>
<th>Cl₂ (sccm)</th>
<th>BCl₃ (sccm)</th>
<th>Ar (sccm)</th>
<th>Time (s)</th>
<th>Al etch (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>S1</td>
<td>5</td>
<td>15</td>
<td>0</td>
<td>120 + 120</td>
<td>4</td>
</tr>
<tr>
<td>S2</td>
<td>10</td>
<td>10</td>
<td>0</td>
<td>120 + 40 + 40</td>
<td>4</td>
</tr>
<tr>
<td>S3</td>
<td>10</td>
<td>10</td>
<td>5</td>
<td>100 + 100 + 120</td>
<td>N/A</td>
</tr>
<tr>
<td>S4</td>
<td>15</td>
<td>10</td>
<td>0</td>
<td>100 + 100</td>
<td>4</td>
</tr>
</tbody>
</table>

and anisotropic etching but the photoresist were seriously etcha, forming porous arrays, and failed to serve as mask due to constant sputtering and redeposition of polymers over the whole sample (Figure 5.10).

5.3.6 Beveling with Dicing Blade

The same type of blade and dicing machine Disco DAD321 were used in this process. To avoid cracking of the wafer, the dicing depth was programmed to be 275µm from the surface while the total wafer thickness is around 510-530µm. The sprocket spins at 4000RPM and the feeding speed is as slow as 0.2mm/s. The surface repairing process is the same as it is reported in Chapter 2. The bevel-cut wafer looks smooth under microscopy (Figure 5.11).

A 1µm PECVD passivation was done on the substrate after dicing and surface treatment. The pad windows were then opened with RIE of oxide using a shadow mask made with thick plastic plate.
Figure 5.9: RIE of Al: (a) S1 sample, (b) S2 sample, (c) S3 sample and (d) S4 sample
Figure 5.10: Experiment of Al RIE process

Figure 5.11: SiC substrate with bevel edge termination
Chapter 6

Characterization and Analysis of FCD

The previous chapter elaborates the process details of the experimental fabrication of the FCD. In this chapter, the electrical measurement results of the fabricated diodes and FCDs are presented. The deviation of measurement from simulation is extensively discussed and process variabilities are analyzed.

6.1 Carrier Lifetime and Diode Characteristics

6.1.1 OCVD measurement of Epi Lifetime

The minority lifetime of the epitaxial wafer is the most critical parameter for bipolar devices, which affects not only forward voltage but also switching loss. In the case of fault protection applications, because the device does not switch in normal operation, the forward voltage is the most concern. Therefore, the lifetime is desired to be high to minimize the conduction loss. The lifetime of the SiC epitaxy is a great challenge
due to defects. The reported lifetime is only around 1µs for P-type SiC epitaxy after enhancement process [85].

One of the most convenient way to measure the SiC lifetime is to use Open-Circuit-Voltage-Decay (OCVD)[86, 87]. The test circuit schematic is shown in Figure 6.1. The diode under test was driven by a pulsed power supply and put into open-circuit state abruptly. During open-circuit state, any series resistance would not contribute to the terminal voltage difference and this voltage is only determined by the carrier concentration according to Law of Junction. The left y-axis of Figure 6.2 shows the decaying voltage during a typical OCVD measurement and the right one is the scale its derivative. As the OCVD process is governed by the equation below, the average peak $\partial V/\partial t$ is around $2.75\times10^5$V/s and gives the corresponding OCVD lifetime of 188ns. The Table 6.1 shows the measured lifetime at different sites of the wafer. These values are very close to the previously reported lifetime on as-grown epitaxy [85, 86].

$$\frac{\partial V}{\partial t} = -2\frac{kT}{q} \frac{1}{\tau_{ocvd}}$$  \hspace{1cm} (6.1)

![Figure 6.1: Schematic of OCVD test circuit](image_url)
Figure 6.2: The waveform of lifetime measurement

Table 6.1: Lifetime Distribution on Wafer

<table>
<thead>
<tr>
<th>Left</th>
<th>Top</th>
<th>Right</th>
<th>Bottom</th>
<th>Average</th>
</tr>
</thead>
<tbody>
<tr>
<td>180ns</td>
<td>188ns</td>
<td>187ns</td>
<td>174ns</td>
<td>182ns</td>
</tr>
</tbody>
</table>
The relation of OCVD lifetime can be derived from the forward voltage expression of PiN diode:

\[ V_F = V_{P+} + V_M + V_{N+} \]  

(6.2)

where \( V_{P+} \) is the anode/drift junction voltage drop, \( V_M \) is the drift region voltage drop, \( V_{N+} \) is the cathode/drift junction voltage drop. \( V_M \) at steady state is a constant determined by drift region length and carrier lifetime[2]. According to the Law of Junction at high level injection:

\[ np = n_i^2 e^{qV/kT} \]  

(6.3)

\[ n \approx p = n_i e^{qV/2kT} \]  

(6.4)

\[ V = \frac{2kT}{q} \ln(\frac{n}{n_i}) \]  

(6.5)

Let the zero of x-coordinate at the middle point of drift region and the drift region length is 2d, the \( V_{P+} \) and \( V_{N+} \) can be given as:

\[ V_{P+} = \frac{2kT}{q} \ln(\frac{n(-d)}{n_i}) \]  

(6.6)

\[ V_{P+} = \frac{2kT}{q} \ln(\frac{n(-d)}{n_i}) \]  

(6.7)

Considering the recombination equation:

\[ \frac{\partial n}{\partial t} = \frac{n}{\tau_a} \]  

(6.8)

and also \( V_M \) is a constant, we have
\[
\frac{\partial V_F}{\partial t} = \frac{\partial V_{P+}}{\partial t} + \frac{\partial P_{N+}}{\partial t} = 2kT\left(\frac{1}{\tau_{P+}} + \frac{1}{\tau_{N+}}\right) \quad (6.9)
\]

where \(\tau_{P+}\) and \(\tau_{N+}\) are high-level injection lifetimes of drift region close to anode and cathode junctions. Therefore,

\[
\frac{1}{\tau_{ocvd}} = \frac{1}{\tau_{P+}} + \frac{1}{\tau_{N+}} \quad (6.11)
\]

In some case that \(\tau_{P+}\) is far smaller than \(\tau_{N+}\), such as an implanted anode, \(\tau_{ocvd} = \tau_{P+}\) and the measured lifetime is the drift region lifetime close to the anode junction.

In this experiment, because the anode is epi-grown, we assume \(\tau_{P+} = \tau_{N+} = \tau_a\) and have

\[
\tau_a = 2\tau_{ocvd} \quad (6.12)
\]

### 6.1.2 Diode Forward I-V

Due to the low lifetime of the epitaxy, the devices fabricated on this wafer were expected to work only partially at high-level injection mode. The calculated ambipolar diffusion length based on the following equation gives only 10\(\mu\)m.

\[
L_a = \sqrt{\frac{2\mu_n\mu_p kT}{\mu_n + \mu_p} \times \tau_a} \quad (6.13)
\]

At the main injecting junction of \(P^-/N^+\) epi/substrate interface, the injection efficiency is very close to unity due to the large \(\mu_n/\mu_p\) ratio\[88\] and the maximum minority concentration can be estimated the expression of total current below:
\[ J_t = 2qD_n \frac{\partial n}{\partial x} \bigg|_{x=150^{-}} = \frac{2qD_n n_{x=150^{-}}}{L_a} \]  

(6.14)

When \( J_t = 50 \text{A/cm}^2 \), the peak electron density at the cathode side of the drift region is around \( 6.6 \times 10^{15} \text{cm}^{-3} \). As a comparison, the simulated carrier profile with 182ns lifetime is shown in Figure 6.3 and the carrier concentration at \( x=150 \mu\text{m} \), the epi/substrate junction, agrees well with the hand calculation assuming high-level injection. At the \( \text{P}^+/\text{P}^- \) junction, high-level injection is also valid. Though the conductivity modulation is very limited due to the reduced injection efficiency at this junction due to lower hole mobility and limited thickness/lifetime of \( \text{P}^+ \) anode, significant slower potential change can be observed from the right axis of Figure 6.3. However, at the middle of the drift region, the minority electrons decay to lower than drift region doping concentration of \( 5 \times 10^{14} \text{cm}^{-3} \) and the high-level injection does not apply. A large amount of voltage drop was allocated at this place.

Figure 6.3: Simulated carrier profile of \( \text{P}^+\text{P}^-\text{N}^+ \) diode
The forward I-V measurements of P⁺P⁻N⁺ diode were done with Tektronix Curve Tracer and hot chuck probe station (Figure 6.4 (a)). The dependence of the device conductivity on temperature is a result of the competing mechanism of the decreasing mobility and the increasing carrier lifetime at elevated temperatures. Because the device just partially works at high-level injection condition and the lifetime increase at high temperature is very limited (τ_{ocvd}=312ns at 100°C), therefore, the enhancement of conductivity at high temperature was not observed like other bipolar devices. Very good match of simulated and measured forward I-V curves of the diodes have been achieved, as shown in Figure 6.4 (b), using the assumption of Eq. 6.12 and τₙ:τₚ=5:1 where τₐ=τₙ+τₚ=2τ_{ocvd}.

6.1.3 Diode Reverse Blocking

The theoretical breakdown of the diode structure is 13kV shown in Figure 6.5. The breakdown initiates at the bulk due to the high field.

As shown in Figure 6.6, the fabricated diode with OPB edge termination has a breakdown of 10kV, which is 77% of simulated result. The lower breakdown of measured result could be caused by the negative PECVD oxide charge and acceptor-like interface traps[89–91]. In Figure 6.7, the simulated breakdown voltage of the PiN structure with 45° bevel reduces to below 10kV when the interface charge is more than -2.5e12cm².
Figure 6.4: Comparison of measured and simulated diode forward I-V characteristics
Figure 6.5: The simulated 13kV breakdown of PiN diode
Figure 6.6: PiN reverse blocking

Figure 6.7: PiN BV vs. oxide interface charge
6.2 FCD Forward I-V

6.2.1 Impact of Lifetime

As stated in chapter 4, the lowest $V_F$ of FCD can be achieved with gate floating or forward biased to anode because the floating or forward biased $N^+/P^-$ junction does not force the minority carrier to zero and allows hole injection from anode via the buried gate. However, a simulation based on extracted lifetime of 182ns shows that the conductivity with forward biased gate improves little due to very small lifetime near the anode region. The simulated hole distribution of the FCD with $L_{ch}=3\mu m$ and $W_{jfe}=3\mu m$ at 50A/cm$^2$ is shown in Figure 6.8. The low lifetime does not allow the hole to diffuse across the buried gate and significantly kills the minority carriers near anode and the voltage drop increases dramatically due to higher resistance (Figure 6.9).

Therefore, the fabricated device cannot work in thyristor mode due to the low lifetime.

6.2.2 Dependence on Structural Parameters

When designing layout, the device structural parameters are varied to explore their influence on device performances. The main parameters are length of the lateral channel, $L_{ch}$, and width of the vertical JFET opening between the gates, $W_{jfe}$. The combinations of $[W_{jfe},L_{ch}]$ are $[2,2]$, $[3,1.5]$, $[3,2]$, $[3,2.5]$, $[3,3]$, $[4,2]$ and $[5,2]$ with unit in microns.

Comparing the devices with same $L_{ch}$ of 2$\mu m$ (Figure 6.10 (a)), the forward I-V curves at $V_{ga}=-3V$ show increased resistance with wider $W_{jfe}$. Though channel density is increased with wider $W_{jfe}$, the high-level injection depends more on the area of anode because the holes can transport via the buried gate at this condition. Therefore, larger $W_{jfe}$ means bigger cells and relatively smaller anode area.
Figure 6.8: Comparison of hole density in the buried gate with lifetime of (a) 1µs and (b) 182ns
Figure 6.9: The simulated carrier profile and voltage drop at different lifetime
Figure 6.10: Forward IV dependence on $W_{\text{jfet}}$ and $L_{\text{ch}}$
The aspect ratio of JFET channel is usually very critical for the trade-off between threshold voltage and device resistance. As plotted in Figure 6.10 (b), the devices with longer channel show much higher resistances. A summarizing plot of current capabilities of different structures at 10V forward bias and -3V gate bias are presented in Figure 6.11. The device conductivity was dramatically affected by $L_{ch}$ and got reduced by 8X when $L_{ch}$ increases from 1.5$\mu$m to 3$\mu$m. However, the simulated changes of current at the same conditions were less than 2X. This means that some other mechanisms, besides the channel, were affecting the conductivity. A good of the simulated device conductivity could only be found when scanning $L_{ch}$ near zero with assumption of 1ns lifetime near the implanted gate, as shown in Figure 6.12.

Figure 6.11: Current capabilities of different structures at $10V_{ak}$ and -$3V_{ga}$
6.3 FCD Blocking Characteristics

High voltage measurement can induce sparkling and arcing in the air due to its low breakdown electric field $\sim 5\text{V/\mu m}$ depending on the humidity and distance. Therefore, Fluorinert liquid has to be used during measurement. The probe station with liquid chuck is shown in Figure 6.13. The blocking capability of the device in forward and reverse direction have been evaluated using Glassman power supply that can source 30kV or 10mA.

6.3.1 Symmetric Blocking Characteristics

The forward edge termination is a 3-zone buried JTE edge termination that has been designed in Chapter 4. A circle-shaped test structure with $600\mu m$ radius for the buried JTE termination could block 8kV as shown on positive side of axis of Figure 6.14. The reverse blocking provided the OPB termination is shown on the negative side of the axis.
The edge terminations can block 8kV in both directions but with high leakage current. One possible cause for the high leakage is the generation current from the top re-grown epi-layer due to its bad quality. Also, due to lack of buffer layers between the P-type epitaxy and the N-type substrate, the basal plane defects might also cause high leakage current at the epitaxy/substrate junction.

![Figure 6.13: The high voltage probe station](image)

![Figure 6.14: The measured blocking gain](image)

The measured blocking gain
6.3.2 Breakover and Blocking Gain

The blocking gain and breakover phenomena were first studied and modeled by Dr. Baliga in 1982[92]. The breakover occurs due to gate current flow which causes a debiasing of the gate potential in the presence of any series gate resistance. The breakover and blocking gain of the fabricated FCD are studied and model.

Analytical Model for FCD Blocking Characteristics

A analytical model that describe the dependence of the cathode leakage current on the barrier is described as:

\[ I_k = I_0 \exp\left( -\frac{q}{kT} V_b \right) \] \hspace{1cm} (6.15)

where \( I_0 \) is junction leakage current, \( q \) is electron charge, \( k \) is Boltzmann constant, \( T \) is temperature and \( V_B \) is the effective barrier height. \( V_B \) can be empirically given by:

\[ V_b = \alpha (V_{ga} - \gamma I_k R_g) - \beta V_k^n \] \hspace{1cm} (6.16)

where \( V_{ga} \) is the gate-anode bias, \( R_g \) is gate resistance, \( V_k \) is cathode bias, \( \alpha \) is channel-controlling factor, \( \beta \) is barrier lowering factor, \( n \) is a fitting parameter in range of 0.2-1.0[66, 92], and \( \gamma = I_g/I_k = \alpha_{NPN} \) is the NPN transistor gain from cathode to gate. Plugging Eq. 6.16 into Eq. 6.17,

\[ I_k = I_0 \exp \left\{ -\frac{q}{kT} \left[ \alpha (V_{ga} - \gamma I_k R_g) - \beta V_k^n \right] \right\} \] \hspace{1cm} (6.17)

When device current breaks over, the differential resistance is zero and \( \partial V_k/\partial I_k = 0 \) in Eq. 6.17. By assuming \( n=1 \), the breakover current can be given by:
\[ I_{k,bo} = I_k|_{\partial V_k/\partial V_g=0} = kT \frac{1}{q} R_g \alpha \gamma \] 

(6.18)

According to the equation above, the breakover current of the FCD is a constant current. Similarly, the blocking gain of the device can be derived from Eq. 6.17:

\[ G = \frac{\partial V_k}{\partial V_g} = \frac{\alpha}{\beta} \]

(6.19)

Therefore, the better channel control and higher resistance to barrier lowering can result in a very good blocking gain. The extraction of \( \alpha \) can be done by sweeping gate bias at low current level with constant cathode bias. Figure 6.15 shows the simulated \( I_k-V_{ga} \) curve whose slope indicates the value of \( \alpha \). The extracted swing is 0.1V/decade and \( \alpha=23 \).

Figure 6.15: The simulated \( \alpha \) of FCD with \( L_{ch}=3\mu m \) and \( W_{jfel}=3\mu m \)

The parameter \( \beta \) can be extracted in similar way. Figure 6.16 shows the simulated \( I_k-V_{ak} \) characteristics of the FCD at various gate bias. The slopes of curves are the
corresponding $\beta$ value. However, the slope is not a constant value like in the vertical channel silicon FCDs reported in Ref.[92]. $\beta$ becomes very small when $V_g$ is 2V or larger. The reason is that the lateral channel stops to be affected by cathode bias when the channel is completely pitched off. A more reasonable way to extract $\beta$ is calculating the current increment with various cathode bias from Figure 6.15. At $V_{ga}=2V$, the current increases with cathode bias at a rate around 5kV/decade and the corresponding $\beta$ is only $\sim 0.00046$. Thus, the theoretical blocking gain of this structure is as high as 50,000.

![Figure 6.16: The simulated $\beta$ of FCD with $L_{ch}=3\mu m$ and $W_{jfet}=3\mu m$](image)

**Results and Analysis**

At a gate-anode bias of 10V, the forward current of 3\mu m channel device can be cut off while devices with shorter channel remain conductive (Figure 6.17). The blocking voltage of a 3\mu m channel device was measured at 5, 10, 15V gate-anode as shown in Figure 6.18. The chuck, on which the cathode substrate sat, could only biased to -1100V (or $V_{ak}=1100V$) due to breakdown of the chuck in the air and measurement capability.
The measured blocking gain at 15V is around 75X. The breakover current $I_{k,bo}$ is around 50mA/cm$^2$.

![Graph showing forward current pinch off at $V_{ga}=10V$](image)

Figure 6.17: Forward current pinch off at $V_{ga}=10V$

The dependence of $I_k$ on $V_{ga}$ with fixed cathode bias is shown in Figure 6.19. The average current swing is around 4V/decade and $\alpha=0.575$, which is only 1/40 of the simulated value.

According to Eq. 6.18, the actual effective gate resistance $R_g$ is around 0.576$\Omega$cm$^2$ with the extracted $\alpha=0.575$ and assumption of $\gamma=0.9$. Therefore, the low blocking gain mainly comes from the weak channel control. Because the channel doping concentration were designed with 300% of variation tolerance, the major process variation that weakens the channel control is lithography bias.

As mentioned in the last chapter, both buried gate implantation and anode mesa etch were defined with 3µm thick negative photoresist. Therefore, significant lithography bias was created when defining the buried gate and anode mesa: the implanted area becomes smaller and the anode mesa is enlarged. Assuming 1µm bias at the buried gate and anode
Figure 6.18: The measured blocking gain

Figure 6.19: $I_k$ vs. $V_{ga}$ at -20V, -100V, -200V cathode bias
Figure 6.20: The dependence of BV on lithography bias

mesa, the FCD originally designed with \( L_{ch}=2 \mu m \) and \( W_{jfe}=3 \mu m \) would become a FCD with \( L_{ch}=0 \mu m \) and \( W_{jfe}=5 \mu m \) and the blocking gain greatly reduces to less than 100X (see Figure 6.20).

### 6.4 Summary and Discussions

In summary, the fabricated symmetric blocking FCD shows 8kV breakdown in both direction but suffers from low \( V_F \) due to very low ambipolar lifetime. The FCD shows a blocking gain of 75X because of weak channel control caused by lithography bias that was introduced by wafer bowing.

Unlike silicon devices whose carrier lifetimes can easily reach tens of microseconds, the lifetime of as-grown SiC epitaxy is usually below 1\( \mu s \). This makes it difficult to get low \( V_F \) from the conductivity modulation within the high voltage SiC bipolar device. The dominant carrier lifetime killers in 4H-SiC epitaxy are the \( Z_{1/2} \) (\( E_C-0.65eV \)) centers and \( EH_{6/7} \) (\( E_C-1.55eV \)), which might come from the carbon vacancies\[93–98\]. The \( Z_{1/2} \) defects concentration of as-grown epi-layers is more than \( 1 \times 10^{13} \text{ cm}^{-3} \) and can be reduced below \( 1 \times 10^{11} \text{ cm}^{-3} \) by annealing with extra carbon introduced\[77, 99, 100\].
Though successful attempts have been made to improve the carrier lifetimes of N-type epitaxial layers and very long lifetime of N-type SiC epilayer up to 19.2μs has been reported[101], the lifetime of thick P-type SiC epi-layer is less understood and little reported[85].

There are mainly two methods to improve the P-type epitaxy lifetimes: the thermal oxidation and the Carbon implant/anneal method. According to the reports of Hayashi et. al.[85, 100], the lifetime of P-type SiC epitaxy could be improved from 0.9μs to 2.6μs by thermal oxidation technique and to 1.6μs by Carbon implant/anneal. The detailed processes are listed in Table 6.2.

Besides the defects from epitaxy process, the ion implantation can introduce extra \( \frac{Z_{1/2}}{2} \) and \( \frac{EH_{6/7}}{7} \) defects in the implanted area and also in deeper region due to channeling effect[81]. According to K. Kawahara’s report[76], after applying several steps of ion implantation with energies up to 700keV to make a junction depth of 0.8μm, the extra \( Z_{1/2} \) was introduced from the implant damage. The concentration of \( Z_{1/2} \) centers were measured to be decreasing with the increasing depth and it reached the as-grown value until a depth of 1.7-1.8μm.

Therefore, to improve the conductivity modulation and reduce conduction losses, the lifetime enhancing process is strongly desired for most of the SiC bipolar devices due to the low lifetime of as-grown epi-layer. Also, the implantation processes should be carefully designed to minimize the impact to carrier lifetime.

Besides the need to improve carrier lifetime of wafer, the gate implantation needs to be avoid and the fabrication of the p-FCD has to be improved for better tolerance of process variabilities. Therefore, a revised structure is proposed as shown in Figure 6.21. Both gate and anode should be formed by epi regrowth in order to avoid any damage that leads to reduced carrier lifetime. It is suggested that the negative bevel edge termination formed
Table 6.2: The 4H-SiC Lifetime Enhancement Processes

<table>
<thead>
<tr>
<th>Technique</th>
<th>Process Steps</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal Oxidation</td>
<td>⦿ Thermal oxidation at 1350°C for 10hr</td>
</tr>
<tr>
<td></td>
<td>⦿ Strip SiO$_2$ with hydrofluoric (HF) acid etching</td>
</tr>
<tr>
<td></td>
<td>⦿ Carbon capped annealing at 1550°C in Ar atmosphere for 30min</td>
</tr>
<tr>
<td></td>
<td>⦿ Deposition of SiO$_2$ and apply NO annealing to reduce traps from oxidation</td>
</tr>
<tr>
<td>Implantation/Anneal</td>
<td>⦿ Carbon implant at 600°C to form a 5×10$^{20}$ cm$^{-3}$ × 0.3µm box profile</td>
</tr>
<tr>
<td></td>
<td>⦿ Capped Anneal at 1600-1800°C in Ar atmosphere for 30min</td>
</tr>
<tr>
<td></td>
<td>⦿ 3µm of damaged surface removed by RIE</td>
</tr>
<tr>
<td></td>
<td>⦿ Ar anneal at 1000°C for 2min to repair RIE damage</td>
</tr>
</tbody>
</table>

by multiple RIE should be used for forward blocking in order to avoid implantation process[102]. N$^+$ buffer layer should be grown as the first epitaxy in order to shield the defects in the substrate and improve injection efficiency. A stepper lithography tool should be preferred in future in order to reduce the lithography bias caused by wafer bowing because the stepper can automatically focus on the wafer when the surface altitude changes within a reasonable range.
Figure 6.21: Revised p-FCD structure
Chapter 7

Conclusions and Future Work

7.1 Contributions

In this work, the symmetric blocking capabilities of SiC power devices have been demonstrated for the first time. The reverse blocking edge termination, Orthogonal Positive Bevels, has been developed and experimentally proven to be not only scalable from 1kV to 8kV but also compatible to the SiC device fabrication processes.

The first trial to fabricate one symmetric blocking SiC bipolar switch using OPB for reverse blocking and buried 3-zone JTE for forward blocking has been presented. The fabricated switch, Field Controlled Diode, is also a novel structure that has a lateral JFET controlled channel with 75X blocking gain. 80% of ideal symmetrical blocking capability has been achieved.

A novel cascode configuration using the FCD and two low-voltage MOSFETs controlling the near-ground electrodes has been proposed. The proposed structure does not need any current drive in the gate to operate in on-state and has capability to work in either high conduction mode or current limiting mode. The unique feature combines
the advantages of conventional FCD and GTO and may be beneficial to optimize the performance and reliability in applications.

### 7.2 Future Work

The following work would be interesting as successive activities:

1. Lifetime enhancement experiment. The controlling of the lifetime in SiC is the main challenge for future bipolar SiC power devices.
2. Develop of N-type Field Controlled Diode for complimentary operation.
3. Demonstrate the cascode configuration of the FCD as a normally off switch.
4. Develop more reliable passivation for the bevel surface.
5. Develop a reliable way to make bevel edge termination for surface junction devices and exploit the area efficiency of the structure.
REFERENCE


Appendix A

Parameters for SiC Simulation

A.1 4H-SiC Material Parameters and Models
<table>
<thead>
<tr>
<th>Physical Properties</th>
<th>Models and Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>Energy Bandgap</td>
<td>$E_g = 3.265 - \frac{6.5 \times 10^{-4} T^2}{1300 + T}$</td>
</tr>
<tr>
<td>Bandgap Narrowing</td>
<td>$\Delta E_g = 9 \times 10^{-3} (\ln \frac{N}{10^{17}} + \sqrt{(\ln \frac{N}{10^{17}})^2 + 0.5})$</td>
</tr>
<tr>
<td>Intrinsic Carrier Density</td>
<td>$n_i = \sqrt{N_C(T)N_V(T)} \times e^{-E_g/2kT}$</td>
</tr>
<tr>
<td></td>
<td>$N_C(T) = 1.689 \times 10^{19} (T/300)^{3/2}$</td>
</tr>
<tr>
<td></td>
<td>$N_V(T) = 2.494 \times 10^{19} (T/300)^{3/2}$</td>
</tr>
<tr>
<td>Electron Mobility</td>
<td>$\mu_n = \frac{947(T/300)^{-2.4}}{1 + (\frac{N_D + N_A}{3 \times 10^{17}})^{0.61}}$</td>
</tr>
<tr>
<td>Hole Mobility</td>
<td>$\mu_p = \frac{124(T/300)^{-2.4}}{1 + (\frac{N_D + N_A}{3 \times 10^{17}})^{0.34}}$</td>
</tr>
<tr>
<td>High Field Mobility</td>
<td>$\mu_{HF} = \mu_{LF}\frac{E}{(1 + (E \times \mu_{LF} v_{sat})(T/300)^{300/T})}$</td>
</tr>
<tr>
<td>SRH Recombination Lifetime</td>
<td>$\tau_{n, p} = \tau_{max}(T/300)^{3.2} \frac{1}{1 + (\frac{N_D + N_A}{3 \times 10^{17}})^{0.3}}$</td>
</tr>
<tr>
<td>Auger Recombination</td>
<td>$R_A = (5 \times 10^{-31} n + 2 \times 10^{-31} p)(np - n_i^2 e_{eff})$</td>
</tr>
<tr>
<td>Impact Ionization Coefficient</td>
<td>$\alpha = 1.69 \times 10^6 e^{-\left(\frac{9.69 \times 10^6}{E}\right)^{1.6}}$</td>
</tr>
<tr>
<td></td>
<td>$\beta = 3.32 \times 10^6 e^{-\left(\frac{1.07 \times 10^7}{E}\right)^{1.4}}$</td>
</tr>
<tr>
<td>Incomplete Ionization</td>
<td>$N_A^- = \frac{N_A}{1 + \left(\frac{E}{k_B T}\right)} p_I = N_V e^{-\frac{0.191 - 3.1 \times 10^{-8} N_A^{1/3}}{k_B T}}$</td>
</tr>
<tr>
<td></td>
<td>$N_D^+ = \frac{N_D}{1 + \left(\frac{E}{k_B T}\right)} n_I = N_C e^{-\frac{0.666 - 3.1 \times 10^{-8} N_D^{1/3}}{k_B T}}$</td>
</tr>
</tbody>
</table>