ABSTRACT

GOSWAMI, ARUNESH. Gate Leakage Current in Nitride-Based HFETs. (Under the direction of Dr. Robert J. Trew and Dr. Griff L. Bilbro).

Reliability issues like the gate leakage current, drain current collapse and breakdown limit the performance of the GaN based HFETs. In this work, the physics of the reliability issues in GaN HFETs is discussed. A new comprehensive physics based model of the gate leakage current in nitride-based HFETs is demonstrated and used to explain leakage currents in these devices when under high field operation. The model explains for the first time the physics of the gate leakage current in AlGaN/GaN HFETs by considering two paths of the leakage current flow: (1) surface layer conduction, and (2) conduction from the gate to the two-dimensional electron gas (2DEG) channel. The current transport mechanism through the surface of the device is modeled using space charge limited (SCL) transport in the presence of traps. Trap assisted tunneling (TAT) is considered for the evaluation of the electrons tunneling from the Schottky gate contact (on the drain side) to the 2DEG channel. The model adequately explains the measured gate leakage current and, predicts accurately the experimentally observed change in slope of the gate leakage current versus the gate to drain voltage. The trap levels extracted from the model are consistent with the reports presented in the literature. The gate leakage current in N-polar InAlN/GaN HFETs is modeled by considering space charge limited current flow in the presence of deep traps in the InAlN layer. The drain current collapse phenomenon in AlGaN/GaN HFETs is explained using circuit based simulation. TCAD simulation of GaN HFETs is performed to conceptually show the experimental observation of the gate to drain spacing dependence on the device breakdown voltage.
Gate Leakage Current in Nitride-Based HFETs

by
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DEDICATION

Dedicated to the ever beauteous, mysterious, the kindest spirit who is in me, in you, its sublime presence is everywhere; it remains invisible and silently it performs all the acts with ease and perfection and bestows the results to us; we then by claiming them foolishly as ours instill unwanted misery.
BIOGRAPHY

Arunesh Goswami was born at Kokrajhar, Assam, India on 20th August 1984. He did his schooling at Halflong, Dipu, Kokrajhar and Guwahati. He graduated with a Bachelor of Technology degree in Electrical Engineering from National Institute of Technology, Silchar, India in May 2006. He started working at IBM from June 2006 in Bangalore, India. He joined North Carolina State University, Raleigh, NC in January 2009 and started working towards his Ph.D program in April 2009 under the guidance of Dr. Robert J. Trew and Dr. Griff L. Bilbro. He completed his Master of Science degree in Electrical Engineering from North Carolina State University, Raleigh, NC in May 2011. He had a device modeling intern experience at RF Micro Devices in Greensboro, NC in 2012. His research is centered on the physics based modeling of the gate leakage current in GaN HFETs.
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Chapter 1: Introduction

GaN based HFETs are the future for the high power RF applications. The potential of GaN HFETs in the power RF sector enormously exceeds than that of the conventional GaAs and SiC devices. The excellent performance of the GaN HFETs which results from the superior material properties of GaN makes them an obvious choice for high power and high frequency applications [1]. The large band gap of GaN facilitates a large breakdown field and the superior thermal conductivity, and high sheet charge density enable exceptional high operating power density over the conventional GaAs and SiC devices [2]. GaN HFETs deliver RF power densities as high as 30 W/mm [3]. Due to high channel mobility and high saturation velocity, GaN HFETs achieve high channel current and high operating frequency making them an outstanding choice for RF power amplifiers in commercial, military and consumer sectors [4]. However, the performance and reliability of GaN HFETs are degraded due to the presence of electrically active defects. The high trap density at the surface and in the AlGaN barrier layer leads to the detrimental effects like gate leakage [5], drain current collapse [6], gate lag [7], and frequency dispersion [8] which adversely affect the output characteristics of the GaN based devices. Gate leakage is an important reliability issue which limits the device performance by reducing the ON/OFF drain current ratio [9] and causing variation in the minimum noise figure [10]. Understanding the physics of the trapping effects is very essential for the improvement of the reliability and performance of the GaN based devices.
1.1. Motivation

GaN HFETs are excellent candidates for high power and high frequency applications. GaN HFETs show great promise to deliver extremely improved performance at high voltage and at RF frequencies. Wide band gap of AlGaN/GaN offers high breakdown field and high electron confinement in the two dimensional electron gas (2DEG) channel facilitates in high

![Figure 1.1: Structure of a typical AlGaN/GaN device showing the polarization charges at the different interfaces, traps and the two paths for the gate leakage current- surface layer and the 2DEG channel.](image)

output current. However, the lattice mismatch of GaN and AlGaN which is about 2.5%, introduces electrically active defects and dislocations which limit the reliability and
performance of the GaN HFETs. Due to the trapping of electrons in the surface and in the AlGaN barrier, a phenomenon called virtual gate [6] originates which degrades the device performance by drain current collapse, gate lag and frequency dispersion mechanisms. Other reliability major issues include the non-linear source resistance [11] which degrades the device performance under high RF drive and DC/RF breakdown due to impact ionization in the 2DEG channel. The non-linear source resistance is modeled by considering the space charge limited effects in the source access region and has been implemented in the compact GaN HFET model [12]. The channel avalanche breakdown mechanism is modeled by considering impact ionization of the carriers at high electric field in the 2DEG channel [13].

Gate leakage is an important reliability issue which limits the device performance by affecting the DC characteristics of the device. The surface of the device in the drain access region facilitates leakage current flow due to the presence of shallow traps [14]. The traps in the AlGaN barrier assist in the trap assisted tunneling mechanism from the gate to the 2DEG which forms a secondary path for the gate leakage current flow [15]. The gate leakage current degrades the performance of the device by increasing the pinchoff current and by degrading the sub-threshold characteristic. Comprehensive modeling of the gate leakage current is essential to predict the device performance accurately. The mechanism of the gate leakage current is crucial to understand from the device physics point of view. A comprehensive model of the gate leakage current has not been reported yet. This thesis will be an effort to comprehensively explain the physics of the gate leakage current flow by considering the effects of traps in GaN HFETs.
1.2. Polarization Charges and its Effect on Transport Properties of AlGaN/GaN HFETs

AlGaN and GaN are polar materials. Due to the polarization effects charges are induced at the semiconductor interfaces which create strong electric field inside the device. The polarization induced electric field attributes exciting properties to the GaN based devices which make them unique and advantageous in the high power and high frequency applications. In fact due to the uniqueness of the polarization effects, the GaN based devices stand apart from its counterparts like the conventional SiC, GaAs devices.

Group-III nitrides AlN, GaN and InGaN are essentially ionic solids with a strong charge transfer between the very electronegative nitrogen atoms and the less electronegative metal atoms (In, Ga, or Al). The wurtzite structure of III-nitrides has a polar axis parallel to the c-direction of the crystal lattice. Due to the non-centro-symmetric nature of the Wurtzite structure, a nonzero volume dipole moment exists in the nitride crystal even when there is no external strain or electric field, which gives rise to a macroscopic spontaneous polarization ‘P’ in the III-nitrides, which can reach values up to 0.1 C/m$^2$ [16]. A large internal electric field is resulted from this large macroscopic polarization and the corresponding fixed surface charges which is given by:

\[
E = \frac{P}{\varepsilon_o (\varepsilon - 1)}
\]  

[1.1]
The value of the polarization induced electric field in the case of AlN with $P = 0.09 \text{ C/cm}^2$ can reach values of up to $10^7 \text{ V/cm}$. Corresponding values for spontaneous polarization in GaN and InN are 0.034 and 0.042 C/cm², respectively [16]. Due to the higher lattice symmetry in the zincblende structure of III-nitrides, this spontaneous polarization is absent.

The group III nitrides grown on heterosubstrate can have two in-equivalent orientations as shown in figure 1.2. These two orientations are referred to as Ga-face and N-face polarity in the case of GaN depending on whether the Ga or the N atoms forming the crystal are facing towards the sample surface. In Ga-face samples, the internal electric field point away from the substrate towards the surface, whereas the polarization has the opposite direction as shown in figure 1.2. The polarization-induced fixed lattice charges are negative at the surface and positive at the substrate interface. For N-face GaN, all charges and directions are inverted.

The GaN HFET device is shown in figure 1.1. A thin layer (~30Å) of GaN forms the top surface of the device followed by an AlGaN layer of 220Å and a thick GaN buffer layer. The built-in electric fields due to polarization charges play an important role in the electrical properties of the nitride heterostructures. In the nitride layers of the device shown in figure 1.1, besides spontaneous polarization, piezoelectric polarization is also present. Piezoelectric polarization results when Wurtzite-structure nitride materials are stressed along the [0001] direction [16]. Stress is formed due to the difference of lattice constants between GaN and AlGaN. For 30% Al composition, the value of piezoelectric polarization becomes
comparable to that of spontaneous polarization. These piezoelectric effects and the difference in spontaneous polarization between AlGaN and GaN cause polarization charges and fields in AlGaN/GaN HFETs. In Ga-face structures, these polarization effects induce negative charges at the surface and at the GaN_cap/AlGaN interface and positive charges at the AlGaN/GaN interface and at the bottom of the device. The charges are induced across the interfaces so that the net charge across a vertical slab of the device is zero. The net contribution of the polarization induced charges to the total space charge is zero.

Because of the polarization charges and the band bending of the heterostructure, a large concentration of electrons (~1x10^{13} cm^{-2}) accumulates at the GaN side of the AlGaN/GaN interface forming the 2DEG conducting channel. The carrier confinement and the carrier mobility in the 2DEG channel are very high and this is the main merit of the GaN based heterojunction devices over the conventional devices. The electron density in the 2DEG channel is a strong function of the Al content of the barrier and a weaker function of the AlGaN layer thickness [17] [18]. Since there is no intentional doping in the AlGaN/GaN HFETs, the source of electrons in the 2DEG is mysterious.

J. P. Ibbetson et al. [19] have suggested that the source of electrons in the 2DEG is the surface donors in the AlGaN barrier. The donors like states are neutral when occupied and positive when empty. So the occupancy of the surface donors determines the built in electric field in the semiconductor and hence the 2DEG density depends on it. If the state is sufficiently deep and lies below the Fermi level (E_F), there is no 2DEG formation (n_s=0) since the surface charge due to the donor states is zero.
However, since $n_s=0$, due to the unscreened polarization dipole there exists a constant electric field, and as the polarization induced electric field increases with the increasing
AlGaN barrier thickness, $E_F - E_D$ decreases and for a critical thickness the donor energy reaches the Fermi level as shown in figure 1.3. Electrons are then able to transfer from the donor states to the 2DEG leaving behind positive charge in the surface. $n_s$ increases rapidly once the critical AlGaN barrier thickness (~30Å) is exceeded. When the AlGaN barrier is much more than the critical thickness, the electron concentration in the 2DEG increases which screens the polarization induced electric field and the 2DEG density no longer increases with the increasing AlGaN barrier thickness. Larger Al composition in the barrier results in larger polarization fields and more rapid increase in the donor concentrations above the Fermi level which results in larger transfer of electrons to the 2DEG [18]. Figures 1.4 and 1.5 illustrate the 2DEG density as a function of barrier Al composition and barrier thickness respectively. The 2DEG electron density has been found to be a stronger function of the Al content in the barrier and a weaker function of the barrier thickness.

![Diagram](image)

Figure 1.3: Schematic band diagram illustrating the surface donor model with the undoped AlGaN barrier thickness a) less than, and b) greater than the critical thickness for the formation of the 2DEG [19].
The mobility of the AlGaN/GaN heterostructure is found to be less than that of the AlGaAs/GaAs heterostructure mainly because of the higher electron effective mass in GaN [17] and stronger alloy scattering in the AlGaN/GaN heterostructure which results from the much higher 2DEG density, larger conduction band offsets and relatively high levels of residual impurities in the nitride layers.

![Figure 1.4: 2DEG densities as functions of AlGaN barrier Al composition [18].](image)

The dominant scattering mechanisms which reduces the electron mobility in the AlGaN/GaN heterostructure are acoustic phonons, coulomb scattering both from the donor defects on the surface of the AlGaN barrier and unintentional dopants in the GaN well, alloy
disorder scattering, interface roughness scattering and the scattering due to the spontaneous and piezoelectric dipoles in the AlGaN barrier. Figure 1.6 shows the 2DEG mobility of the AlGaN/GaN heterostructure versus the AlGaN barrier thickness.

![Figure 1.6: 2DEG mobility vs. AlGaN barrier thickness](image)

For small thickness of the AlGaN barrier, the electron concentration in the 2DEG is less, in this region the Coulomb scattering from charged impurities in both the GaN well and the AlGaN barrier is very effective in keeping the mobility low. As the AlGaN thickness increases, the larger electron concentration of 2DEG screens the charged impurities which reduces the effectiveness of Coulomb scattering resulting in the increase of the electron mobility in the 2DEG. Finally, when the 2DEG density becomes high enough alloy disorder
scattering dominates and the electron mobility starts decreasing with increasing 2DEG density.

Figure 1.6: Low temperature 2DEG mobilities as a function of barrier thickness for four different AlGaN/GaN heterostructures with different Al barrier compositions [18].

1.3. Excellent Performance of GaN HFETs

The wide band gap semiconductors have dielectric constants about 20% lower than the conventional materials [2]. This permits a wide band gap semiconductor device to be about 20% larger in area for a given impedance. Increased area permits larger RF currents and higher RF power to be generated. GaN base devices can be operated at higher voltages due to the wide band gap of GaN. Commercial GaAs devices operate at 28 V whereas GaN based devices have the potential to operate above 42 V [1]. The high operating voltage of GaN
HFETs eliminates the requirement of voltage conversion. The higher efficiency which results from the high voltage feature reduces power requirements and simplifies cooling which lowers the overall cost and weight of the system. Another attractive material property of GaN is its higher power density which facilitates extraction of much higher power per unit width from the GaN based devices; this feature favors reduction of device size. The smaller devices are not only easier to fabricate but they also offer high impedance which makes them easier to match with the system which is often a complex and expensive task with conventional GaAs devices. GaN HEMTs have one order higher power density and power efficiency than the commercially available SiC and GaAs devices. Thus for the same output power a ten times reduction in device size can be realized using GaN based devices in place of commercial devices. GaN HFETs also achieve 3 to 10 times better Rds-ON per mm$^2$ than the conventional devices. AlGaN/GaN HFETs have higher linearity because of higher electric field to achieve saturation velocity. Overall, GaN HFETs achieve impressive device performance: output power of 30 W/mm, current gain cutoff frequency of 190 GHz and power gain cutoff frequency of 230 GHz [1].
Figure 1.7: Current-voltage characteristics simulated by MWO™ for the HFET model (blue lines), along with experimental measurements (red lines) for a HFET with 0.8µ gate length and 400µ width. Each of the six curves corresponds to a $V_{gs}$ value from -4V to 1V. All curves sweep $V_{ds}$ from 0V to 20V [20].

The measured and modeled DC I-V characteristic of an AlGaN/GaN HFET is shown in figure 1.7. A maximum current of ~ 2A/mm is routinely obtained experimentally in AlGaN/GaN HFETs. The measured and simulated of RF performance including output power, power gain and power-added efficiency, for two S-Band amplifiers fabricated using AlGaN/GaN HFETs is shown in figure 1.8. The amplifier was biased at a drain voltage of $V_{ds} = 28$V and operated in class AB at a fundamental frequency of $f = 2.14$ GHz. Due to the
conduction of extremely high current the temperature of the device rises, and at elevated temperature scattering of the carries increases which reduces the performance of the device.

Figure 1.8: Large signal simulation results including output power, power gain and PAE obtained from the HFET model comparison to the measurement data for the W=400µ, Lg=0.8µ, transistor under consideration, with and without (insertion graph) channel breakdown model. (“Red” is measurement data,”Blue” is simulation results.) [20]

The high thermal resistance in the channel operating at elevated temperature limits the channel current. The gate leakage current increases at higher temperature, at 150°C the gate leakage current increases by almost 20% than its value at room temperature [15]. The transconductance and maximum current as a function of temperature of an AlGaN/GaN HFET is shown in figure 1.9. The RF performance of the device reduces at higher operating temperature. The output power, gain and PAE drastically deteriorate at elevated temperature.
as shown in figure 1.10. This indicates the importance of thermal design for the improved performance of microwave power amplifiers for the GaN based device. Thermal design is more difficult for GaN HFETs as compared to the conventional GaAs devices, since the GaN based devices are operated at much higher voltage and power levels which tremendously increases the operating temperature.

Figure 1.9: Thermal performance of an AlGaN/GaN HFET (Lg = 0.7µ, W = 50µ) [2].
Figure 1.10: Thermal performance at 10 GHz of an AlGaN/GaN HFET class A/B amplifier (Lg = 0.7 um, W = 100 um) [2].

1.4. Modifications in GaN HFETs to Enhance Performance

Since the AlGaN/GaN devices are fabricated using unintentionally doped AlGaN and GaN, any trap-related change in the surface space charge can have a major impact on the density of the 2DEG. Doping in the AlGaN layer can screen the effects of the surface charges. However, without such screening, the channel current collapses and saturates prematurely by the high density of surface charging states especially in the gate-drain access region that could deplete or modulate the carrier in the 2DEG channel. The surface states have a major and significant effect on the operation of the GaN based devices and SiN passivation considerably reduces the effects of the surface states. SiN passivation reduces the response of the surface traps by mitigating the effects of the dangling bonds on the surface and hence
suppresses the effect of current collapse [21]. SiN passivation increases maximum drain current and maximum transconductance due to change of surface pinning level. Current gain and power density at higher drain bias is also improved by SiN passivation. Current gain cut off frequency ($f_T$) increases with SiN passivation but maximum oscillation frequency ($f_{\text{max}}$) decreases with SiN passivation. Decrease of $f_{\text{max}}$ is attributed to increase in the contribution of the feedback capacitances. Since the effects of surface traps is reduced with SiN passivation, the electric field at the drain side gate edge cannot spread out in the access region and focuses at the narrow depletion region in the 2DEG channel which results in reducing the breakdown voltage of the GaN HFETs. The trade-off relationship between the current collapse and breakdown characteristics is the main concern for using GaN HFETs in high power condition. A field modulating plate (FP) is applied to improve the breakdown voltage and to minimize the surface trap effects. The suppression of the drain current dispersion observed for the FP-HFET suggests that the field modulating plate effectively controls the depletion layer in the gate drain access region under large signal operation, which results in the removal of the effects of surface traps on the carrier concentration of the 2DEG channel. Improvement of the breakdown voltage is due spreading of the electric field under the field plate region from the gate edge in the drain access region. With the spreading of the depletion layer under the field plate electrode, the strength of the electric field at the drain side gate edge reduces and so the breakdown voltage increases. But with the increasing FP length, the breakdown voltage (BV) decreases due to reduced spacing between the FP and the drain electrode. Better modulation of the carrier density between the gate and the drain results in reduction of current collapse even in the presence of traps in a field plated device.
Figure 1.11 shows the variation of breakdown voltage and maximum drain current ($I_{\text{max}}$) with the increasing length of gate field plate. Both $f_T$ and $f_{\text{max}}$ decrease for FP devices at lower drain voltages due to the increase in the feedback capacitances. However, at higher drain voltages, the influence of FP on the feedback capacitances becomes less significant because of the extension of the depletion layer towards the drain end. Hence the FP devices exhibit drastic improvement of $f_{\text{max}}$ at higher drain voltages. The device gain drops due to the increase of the feedback capacitances at lower drain voltages; at higher drain bias this problem is mitigated. Improvement of saturated power in FP devices is attributed to the suppression of current collapse and increase in $f_{\text{max}}$.

![Graph showing $I_{\text{max}}$ and BV versus FP length (W = 50 um; L = 2.5 um)](image)

Figure 1.11: $I_{\text{max}}$ and BV versus FP length (W = 50 um; L = 2.5 um) [22].
The use of a thin ~10 Å AlN interlayer between the AlGaN barrier and GaN channel is demonstrated to reduce the sheet resistance by increasing the mobility and sheet density of the HFET device [23]. The increase in mobility is attributed to the reduction in alloy scattering and the increase in the sheet charge is due to the larger conduction band discontinuity at the AlGaN/GaN interface. The confinement of the carriers in the 2DEG increases with the incorporation of the AlN layer. Figure 1.12 shows the band structure of the AlGaN/GaN heterostructure with the AlN layer between the AlGaN barrier and GaN.

Figure 1.12: Schematic conduction band diagram of AlGaN/AlN/GaN HFET with a thin AlN layer at the AlGaN/GaN interface [23].
The gate length of the GaN HFET devices has to decrease as the required frequency of operation increases. However, devices with short gate lengths (below 300nm) exhibit short channel effects like soft pinch-off, high output conductance, threshold voltage shift and high substreshold current. These problems arise because of the poor confinement of electrons in the 2DEG channel. The performance of the GaN HFETs is enhanced by improving the carrier confinement in the 2DEG channel. Double heterostructure is used to increase the electrostatic confinement potential (to 1-2 eV) which improves the confinement of carriers in the 2DEG channel by the polarization fields [24]. Due to higher carrier confinement, the electrons do not slip out of the 2DEG into the GaN buffer at higher drain voltages, so the output conductance increases with increasing drain current. Double heterostructure deteriorates the surface morphology and creates an additional parasitic secondary channel which deteriorates the device transconductance [25]. To overcome the issues of using double heterostructure, InGaN back barrier is used to increase the carrier confinement in the 2DEG channel. The polarization induced electric field in the InGaN layer raise the conduction band in the GaN buffer with respect to the 2DEG channel, hence increasing the confinement of the carriers in the channel [26]. As a result of the improved carrier confinement, a significant improvement in the output conductance and pinchoff characteristic is observed. Increase of $f_t$ and $f_{max}$ have also been observed due to the improved carrier confinement. Figure 1.13 shows the band structure of the AlGaN/GaN HFET with the InGaN layer acting as a back barrier.
1.5. Reliability Issues in AlGaN/GaN HFETs

Although AlGaN/GaN HFETs are promising and suitable candidates for high power and high frequency applications but there are many factors which limit the device performance and reliability and consequently the commercialization of these devices have been limited. Gate leakage is an important reliability issue which limits the device performance by reducing the ON/OFF drain current ratio and causing variation in the minimum noise figure. Gate leakage is also responsible for the reduced output signal at higher frequency which leads to a downward dispersion at around 1 kHz [8]. The subthreshold characteristic of GaN devices are key to assure good PAE, reliability, linearity, and noise figure in power amplifiers [10]. The subthreshold slope in GaN HFETs has traditionally been much higher (>300 mV/dec) than the theoretical limit of 60 mV/dec [27] [28]. Figure 1.14 shows the drain current characteristics of AlGaN/GaN HFETs as a function of gate voltage in transistors with and without O₂ plasma treatment.
Figure 1.13: Effect of the insertion of an ultrathin layer of InGaN in the conduction band diagram of a GaN buffer. Due to the extremely thin InGaN layer, the conduction band discontinuity, $\Delta E_C$, of one side of the heterostructure is canceled by the $\Delta E_C$ in the other side and it can be neglected, resulting in an effective band discontinuity equal to $\Delta E_p$. In the figure, the polarization-induced sheet charges at the heterointerfaces are also shown. (b) Schematic and conduction band diagram of the InGaN back-barrier [26].
The gate leakage current is also plotted to show its effect on subthreshold slope in figure 1.14. The reduction of the gate leakage current for the AlGaN/GaN HFET with O₂ plasma treatment is clearly observed in the figure 1.14. The O₂ plasma treatment creates a thin layer of Ga₂O₃ which has high dielectric constant (~10). The Ga₂O₃ layer acts as a dielectric between the gate and the AlGaN layer. The thin layer of Ga₂O₃ effectively reduces leakage current through two mechanisms: (1) suppressing vertical tunneling by increasing barrier thickness and (2) by reducing Trap Assisted Tunneling (TAT) through the passivation of surface traps underneath and near the gate contacts [29]. From figure 1.14, it is obvious that the gate leakage current affects the DC characteristics of the device by reducing the ON/OFF drain current ratio and degrading the subthreshold slope. With increasing gate leakage current, the I₉₀/I₉₀ ratio decreases linearly. The effect of gate leakage current on the I₉₀/I₉₀ ratio is shown in figure 1.15.
Figure 1.14: Transfer characteristics and gate leakage current of AlGaN/GaN HFETs with and without O\textsubscript{2} plasma treatment at $V_{DS} = 5$ V. Subthreshold slope nearly changes (less than 5%) with $V_{DS} = 0.5 \sim 20$ V. The slight increase in the gate-to-channel separation due to the gate oxide layer (< 4 nm) is responsible for the threshold voltage shift of 0.3 V [9].

Figure 1.16 shows the correlation between subthreshold slope and the gate leakage current of AlGaN/GaN HFETs. The subthreshold slope degrades linearly with the increasing gate leakage current in a logarithmic scale. The subthreshold slope of the AlGaN/GaN HFETs with O\textsubscript{2} plasma treatment is found to be 64 mV/dec which is very close to the theoretical limit of 60 mV/dec.
Figure 1.15: Linear dependence between the ON/OFF drain–current ratio ($I_{ON}/I_{OFF}$) and the gate leakage current ($I_G$) [9].

Figure 1.16: Linear dependence between subthreshold slope and the gate leakage current ($I_G$) with and without O$_2$ plasma treatment [9].
The gate leakage current affects the noise figure of the AlGaN/GaN HFETs. The gate leakage limits the device performance by causing more than 1dB of variation in the minimum noise figure [10]. A plot of minimum noise figure versus gate leakage current is shown in figure 1.17. From figure 1.17, it is observed that the minimum noise figure increases rapidly for gate leakage current greater than 10 μA.

![Figure 1.17: Simulated effect of gate leakage (line) on NF_{min} at 10 GHz for a device with a bias of V_{DS} = 5 V and I_{DS} = 10 mA. The circle is from a different sample. Inset: Simulated (line) NF_{min} versus frequency for a device biased at V_{DS} = 5V and I_{DS} = 10mA with a gate leakage of I_{GS} = 140 μA/mm [10].](image-url)

Surface states are responsible for the detrimental effects like drain current collapse- a reduction in the DC-drain current and distortion of DC current-voltage characteristics [6]. As
shown in the figure 1.18, a significant drain current collapse is evident in the gate turn-on pulsing mode. Drain current collapse reduces the output power of the device.

The surface states result in degraded device performance by the phenomenon called gate-lag, a delayed response of the channel current to modulation of the gate potential. The charging and discharging of the traps in the device structure is reflected in gate lag. Charge temporarily trapped in the vicinity of the transistor channel reduces the drain current by considerable amount. The trapping centers are located on the surface of the device, in the AlGaN layer and in the GaN buffer. The AlGaN layer contains a large concentration of donor ions which aid the process of forming the 2DEG channel, the high density of the donor ions in the AlGaN barrier attributes to the gate lag. Figure 1.19 shows the channel current response for two devices: one of the devices shows an instantaneous recovery while the other exhibits gate lag.
Figure 1.18: Experimental $I$-$V$ characteristics obtained in dc and in gate turn-on mode, by pulsing $V_{GS}$ from -5 V to the quoted $V_{GS}$ (10 us pulse width, 0.01% duty cycle) [8].

For the device with gate lag, the channel current requires considerable amount of time to recover to the steady state level thus degrading the performance of the device. The rate of current recovery increases at elevated temperature. The reduction of the device output power by the phenomenon like drain current collapse and gate lag effects the high frequency operation which is referred as frequency dispersion.
Figure 1.19: Normalized channel current response to the gate pulse $V_G(0 < t < 10 \, \mu s) = 0$ V, after the off state $V_G = -10$ V. The devices are continuously biased at $V_D = 10$ V. The drain current is measured with the low-insertion impedance current probe. Two traces show devices with and without gate lag [7].

Figure 1.20 shows the output characteristics of AlGaN/GaN device at $V_{gs}=0$ for different pulse width values. The channel current decreases for shorter pulse width. This observed pulse behavior reflects into the curves of transconductance as a function of frequency. Figure 1.21 shows a downward dispersion at around 1 kHz i.e., the output signal is lower at higher frequencies which is in agreement with the pulsed characteristics.
Figure 1.20: Experimental $I_D-V_{DS}$ characteristics at $V_{GS}=0$ V obtained in dc and in gate turn-on mode by pulsing $V_{GS}$ from -5 V to 0 V. The pulse width is varied from 1 ms to 1 μs with a 100-ms period. Pulsed $I_D$ values are obtained by averaging the $I_D(t)$ samples over the final, stable portion of the pulse width [8].

Figure 1.21: Experimental $g_m(f)$ low-frequency dispersion curve measured at the following bias point: $V_{DS}=2$ V, $V_{GS}=-4$ V [8].
These detrimental effects are predominantly caused by charging and discharging of the traps in the surface and in the AlGaN layer and the current conduction in the drain access region in the presence of surface traps. The physics of the trapping mechanism in GaN HFETs is very essential to understand to increase the performance and the reliability of the devices.

1.6. Outline of Thesis

This thesis reports on the physics of the reliability issues in GaN based devices. The formulation of physics based model of the gate leakage current in GaN HFETs is extensively elucidated in this thesis. The thesis is divided into three sections:

Chapter 2 elucidates the formulation of the gate leakage current through the surface of the AlGaN/GaN device by considering the surface as an insulator. Firstly, the formulation of the space charge limited (SCL) current flow in the presence of deep traps in an insulator is discussed. Next, the formulation of the SCL current in the presence of shallow traps in an insulator is discussed. Finally, the physics based gate leakage model is formulated for AlGaN/GaN HFETs by considering SCL current flow through the AlGaN surface layer in the presence of two levels of shallow traps. The modeled results are compared against measurement data.

Chapter 3 establishes the comprehensive model of the gate leakage current flow in the GaN based HFETs. In the first section, an analytical model of gate leakage current in AlGaN/GaN
HFETs is derived by considering, for the first time, two paths for the gate leakage current flow: (1) the surface of the device establishes the primary path and the current transport mechanism is modeled using space charge limited transport in the presence of shallow traps; and (2) the traps in the AlGaN layer assist in the tunneling of electrons from the gate to the two dimensional electron gas (2DEG) which flows to the drain electrode constituting the second path for the leakage current. A model for the tunneling of the gate electrons to the 2DEG is incorporated in the formulation. Trap assisted tunneling (TAT) mechanism is considered for the tunneling of the gate electrons to the 2DEG channel. Due to the abundance of shallow traps in the device surface, TAT rate is much higher at the surface region, so for the formulation of the current transport mechanism through the surface, the gate electrode can be assumed as an infinite reservoir of electrons and the conduction through the surface is transport limited. The model predicts accurately the gate-leakage current for a wide range of gate-drain voltage. The trap levels extracted from the model are consistent with the reports presented in the literature. The model appropriately explains the gate leakage current of the AlGaN/GaN HFETs for drain voltages up to 170 V and is verified by comparing the model results with the measured gate leakage data of industrial devices. The model is also shown to accurately predict the gate leakage data at elevated operating temperature. In the second section, the modeling of the gate leakage current of N-polar InAlN/GaN HFETs is discussed. The gate leakage current for the InAlN/GaN HFETs is modeled using the SCL current transport in the presence of deep traps through the InAlN surface layer. The TAT from the gate to the 2DEG channel is found to be negligible in the presence of deep traps; the gate leakage current flowing through the surface layer dominates the current flow through the
2DEG channel in InAlN/GaN devices. The modeled results are compared with the measurement data.

Chapter 4 discusses the circuit based simulation of the drain current collapse phenomenon using Advanced Design System (ADS) simulator in the first section. In the second section, I briefly described the work which I had accomplished during my internship at RFMD. TCAD breakdown simulation of GaN HFETs using Silvaco Atlas simulator is performed to conceptually explain the experimental observation of the gate to drain spacing dependence on the device breakdown voltage. The simulated results of the TCAD model are compared against the measured DC $I$-$V$, Pulsed $I$-$V$, and capacitance data of AlGaN/GaN HFETs.

The dissertation is concluded by reporting on the future work required to improve the gate leakage model in Chapter 5.
REFERENCES


Chapter 2 : Physics Based Modeling of the Gate Leakage Current in GaN HFETs

2.1. Introduction

Semiconductors having wide band gap are appealing for applications ranging from power conditioning to microwave transmitters. Of the various materials and device technologies, the AlGaN/GaN HFETs are promising and suitable candidates for high power and high frequency applications such as cellular base stations, satellite communications, and radar transmitters. However, issues like gate leakage, current collapse and dispersion effects which are predominantly caused by the presence of surface traps limit the device reliability and performance. Consequently, the commercialization of these devices has thus far been limited, although commercial devices are available. Gate leakage is an important reliability issue in these devices. The gate leakage phenomenon is caused by conduction through surface traps which results in time-dependent performance degradation. Many groups have been investigating the physics of the trapping effects [1] [2] and the gate leakage mechanism [3] [4], reliability issues [5] [6], and several different methods including surface passivation and treatment [7] [8], field-plates [9], deep gate recesses [10], and other techniques to reduce the gate leakage current and to alleviate the reliability of the device have been studied. Though much effort has been put into investigating the issue, the physics of the trapping mechanism
in the AlGaN/GaN HFETs has not been completely understood and reliability still remains a major concern, especially for long term usage.

A model that adequately and accurately explains the gate leakage phenomenon due to traps has not been reported, although a generalized trap-assisted tunneling model has been reported to explain the reverse gate leakage current in AlGaN/GaN HFETs [11]. The model considered the gate electrons tunneling to the 2DEG channel through trap assisted tunneling mechanism. Figure 2.1 shows a trapezoid barrier between the metal and the semiconductor and the traps present in the barrier assist in the tunneling of electrons from the metal to the semiconductor. This model completely ignores the leakage current conduction through the surface of the device. Also, the influence of the drain voltage on the $I$-$V$ characteristic of the leakage current is not considered in the model and it predicts the leakage current through MIS structures only at low fields. The model fails to explain the gate leakage data at higher gate-drain voltages. The measurement data indicates that the $I$-$V$ profile of the gate leakage considerably changes with the changing drain voltage. A theory that explains the gate leakage current for a wide range of gate-drain voltages is required for accurately predicting the device performance. Miller et al. [12] reported on the vertical and lateral tunneling of electrons from the gate metal to the semiconductor in an AlGaN/GaN HFET (figure 2.2), but the transport mechanism of the injected electrons to the drain end of the device was not elucidated in the formulation. The lateral tunneling of the electrons from the gate to the surface layer has been suggested but not considered in the formulation of the model. Pérez-Tomás et al. [13] reported a frequency dependent conductance analysis to characterize the
gate traps and demonstrated an abundance of surface states and interface traps in the Schottky gate AlGaN/GaN HEMTs.

Figure 2.1: Device structure and energy band diagrams of reverse biased Schottky diode. TT denotes the existing model of trap-assisted tunneling only through a triangular barrier. $\Phi_t$ is the trap ionization energy and $\Phi_B$ is the barrier height [11].
An electron-hopping model which uses the Eyring’s reaction rate formulation [14] to describe the gate leakage current due to the surface traps in the AlGaN layer has been reported [15]. The electron hopping model considers the thermionic emission frequency from trap to trap to explain the gate leakage current. The usage of the Eyring’s equation to describe the flow of electrons from trap to trap is not convincing as it leads to inconsistent predictions of gate leakage with measurement data. The electron hopping mechanism dominates the current flow in an insulator or semiconductor at lower temperatures (1 and 20°K) when the thermal energy of the electrons is not sufficient to cause emission of the trapped electrons to the conduction band.
The AlGaN/GaN HFETs are not operated at such low temperatures. At higher temperatures the (shallow) traps emit the electrons to the conduction band and the free electrons in the conduction band contribute to the gate leakage current.

In this chapter, we present a physics based model of the behavior of the trapping effects in GaN HFETs which results in the gate leakage current. The new model uses the physics of space charge limited current to explain the flow of the injected electrons from the gate to the drain terminal through the AlGaN layer in the presence of traps. It is demonstrated that the new model accurately predicts the measured gate leakage of a particular AlGaN/GaN HFET.
resulting from current conduction through the surface layer in the presence of shallow trap levels at 0.57 eV and 0.75 eV below the conduction band.

The analysis of numerous gate leakage measurement data of AlGaN/GaN HFETs indicates the presence of two paths for the gate leakage current flow: (1) the surface of the device and (2) the 2DEG channel. The formulation of the gate leakage current model considering both the current paths will be considered in the next chapter. In this chapter, only the surface of the device is considered for the formulation of the gate leakage model. The experimental device consists of the Schottky AlGaN barrier which forms the surface of the device. The 2DEG is located in the GaN side of the AlGaN/GaN interface as shown in figure 2.4. The gate leakage model is formulated by considering space charge limited (SCL) current flow through the surface in the presence of shallow traps.

![Figure 2.4: Surface traps in AlGaN/GaN HFET.](image)
The undoped AlGaN layer is considered as a slab of insulator for the formulation of the gate leakage model. In the following section, the physics of the trapping effects on the SCL current flow in an insulator will be discussed.

2.2. Current Flow in an Insulator

Before the advent of quantum mechanics, insulators were simply considered a non-conduction material in which under an extremely high field, a negligible current flows. With the application of quantum mechanics to the electronic structure of solids by Bloch in 1928, the energy band picture of solids emerged which laid the foundation of the theoretical formulation of the current flow mechanism in insulators and semiconductors. On the basis of the energy band structure of solids, it became possible to theoretically explain the injection of electrons from metal contacts to insulator or semiconductor by considering the transport mechanisms like tunneling and thermionic emission. Electron flow in the conduction band of the insulator is dominated by the frequent collisions with the impurities, thermal lattice vibrations, structural imperfection and interface roughness which results in decreasing the low-field mobility in an insulator. Due to the poor mobility in an insulator, the charge carriers cannot traverse freely which results in the space charge effects. This necessitates the consideration of space charge effects in the formulation of current flow in an insulator. The presence of traps in an insulator is an inevitable attribute of a real insulator. Traps will influence the current conduction in the insulator. In the following section we will discuss how the traps affect the space charge limited current flow in an insulator.
In a trap free insulator, all injected electrons remain free, i.e., in the conduction band and all contribute to the space charge and current conduction. The current density and Poisson’s equations are given by:

\[ J = \rho v \]  \hspace{1cm} 2.1

\[ \frac{dE}{dx} = \frac{\rho}{\varepsilon} \]  \hspace{1cm} 2.2

where, \( \rho \) is the average injected free charge concentration, \( v \) is the average drift velocity.

The total injected charge per unit area in the insulator is given by:

\[ Q = \rho L = CV \]  \hspace{1cm} 2.3

Where, \( L \) is the distance between the metal electrodes and \( C \) is the capacitance.

The role of the diffusion current is neglected in the formulation of the current flow in an insulator since its magnitude is very low as compared to the drift current. Diffusion currents are sizable only in the thin region in the vicinity of metal contacts.

The presence of traps in an insulator will generally result in greatly reduced current at lower injection levels, since those traps initially empty will capture, and thereby immobilized most of the injected charge at a given voltage. However, the amount of excess charge that can be supported by the insulator at an applied voltage is the same whether the excess charges are
free or trapped. The trapped charges will not contribute to the current flow but will affect the background electric field. Thus,

\[ Q = (\rho + \rho_t) L \]  

Where, \( \rho_t \) is the average, injected, trapped charge concentration. The Poisson’s equation is given as:

\[ \frac{dE}{dx} = \frac{\rho + \rho_t}{\varepsilon} \]  

Only the free electrons in the conduction band contribute to the current flow, the current density equation is given by,

\[ J = \rho v \]  

For non-degenerate semiconductors or insulators, the thermal equilibrium free electron concentration is given by the Fermi-Dirac statistics:

\[ n_o = N_c \exp \left( \frac{F_o - E_c}{kT} \right) \]  

Where, \( N_c \) is the effective density of states in the conduction band, \( E_c \) is the energy of the bottom edge of the conduction band, \( k \) is the Boltzmann’s constant, \( F_o \) is the Fermi level at thermal equilibrium, and \( T \) is the temperature. The thermal equilibrium concentration of
trapped electrons $n_{to}$, at trap level $E_t$ is related to the trap concentration $N_t$ by the Fermi-Dirac expression [16]:

$$n_{to} = \frac{N_t}{1 + \frac{1}{g} \exp\left(\frac{E_t - F_o}{kT}\right)} = \frac{N_t}{1 + \frac{1}{g} \frac{N}{n_o}}$$ \hspace{1cm} 2.8$$

$$N = N_c \exp\left(\frac{E_t - E_c}{kT}\right)$$ \hspace{1cm} 2.9$$

Where, $g$ is the degeneracy factor for traps.

This equilibrium trap occupancy results from a balance between capture of electrons into the traps, and their thermal re-emission into the conduction band. In the presence of an applied field, the balance between free and trapped electrons is altered due to the change of free electron concentration because of carrier injection. Under electron injection the Fermi level will raise to a higher level called the quasi Fermi level. The free electron concentration is given by,

$$n = n_i + n_o = N_c \exp\left(\frac{F - E_c}{kT}\right)$$ \hspace{1cm} 2.10$$

where, $n_i$ is the average excess free electron concentration and $F$ is the Fermi level.

The trapped electron concentration under injection is given by,
\[ n_t = n_{ii} + n_{io} = \frac{N_t}{1 + \frac{1}{g} \exp \left( \frac{E_t - F}{kT} \right)} = \frac{N_t}{1 + \frac{1}{g} n} \]  

where, \( n_{ii} \) is the average, injected, excess trapped electron concentration.

In the subsequent sections the mathematical formulation of the current-voltage characteristics in an insulator in the presence of deep traps and shallow traps will be elucidated.

Figure 2.5: Energy band diagram of an insulator in thermal equilibrium. Both shallow trap and deep trap levels are shown.

\[ \text{E}_C \]

\[ \text{E}_V \]

\[ \text{F}_0 \]

\[ \text{Shallow trap level} \]

\[ \text{Deep trap level} \]
2.3. Current-Voltage Characteristic of Insulator in Presence of Deep Traps

The traps whose energy level lies below the Fermi level are termed as deep traps. Let us consider the situation where there is a single set of traps of concentration \( N_t \) at an energy level \( E_t \) below \( F_0 \). In thermal equilibrium, the concentration of traps not occupied by electrons is given by [17]:

\[
p_{to} = N_t - n_{to} = \frac{N_t}{1 + g \exp \left( \frac{F_0 - E_t}{K T} \right)} \approx \frac{N_t}{g} \exp \left( \frac{E_t - F_0}{K T} \right)
\]

The last expression is a valid approximation when \((F_0 - E_t)/kT > 1\). Where, \(n_{to}\) = concentration of trapped electrons in thermal equilibrium, \(N_t\) = concentration of deep traps, and \(E_t\) = deep trap energy level.

The trap filled limit voltage \(V_{TFL}\) is the voltage for the onset of space charge limited current injection required to fill the set of traps and is given by,

\[
V_{TFL} \approx \frac{ep_{to}L^2}{\varepsilon}
\]

where, \(L\) = spacing between the electrodes, \(\varepsilon\) = dielectric constant of the insulator layer.

The equilibrium trap occupancy results from a balance between capture of electrons into the traps, and their thermal re-emission into the conduction band. The electrons in the conduction
band will contribute to the current flow through the insulator. The Poisson’s equation in an insulator in the presence of deep traps is given by:

$$\frac{dE}{dx} = \frac{e}{\varepsilon} \left( (n - n_0) + (n_t - n_{t_0}) \right)$$  \hspace{1cm} 2.14$$

where, \( n = \) concentration of free carriers, \( n_0 = \) concentration of free carriers in thermal equilibrium far removed from the surface and contacts, \( n_t = \) concentration of trapped electrons, and \( n_{t_0} = \) concentration of trapped electrons in thermal equilibrium.

Using the current density equation and after some algebra we can derive the following differential equation:

$$\frac{dE}{dx} - \frac{J}{\varepsilon\mu} E^{-1} - \frac{e}{\varepsilon} \left( n_t - n_{t_0} - n_0 \right) = 0$$  \hspace{1cm} 2.15$$

We can derive the exact solution to the above differential equation in terms of the LambertW function [18] given by,
where, \( V(x) \) is the potential difference between the terminals.

The solution is too complicated for robust implementation in commercial software. However, the problem can be simplified by application of a regional approximation. We treat the device as different regions where the regions are defined so that the physics can be simplified in each. The insulator layer is divided into three regions on the basis of the dominance of different charge carriers in the regions. As shown in the figure 2.6, the injected free carrier concentration \( n_i \) decreases monotonically from \( \infty \) at \( x=0 \). At low injection level, there will be a plane \( x_2 \) inside the insulator where the concentration of free carriers is equal to the thermal
carrier concentration, \( n_i(x_2) = n_o \); to the left of plane \( x_2 \), \( n_i > n_o \) and \( n_o \) can be neglected. To the right of plane \( x_2 \), \( n_o > n_i \) and \( n_i \) can be ignored. To the left of plane \( x_2 \), the effect of traps will dominate over the injected carrier concentration and the thermal equilibrium concentration. Finally, there will be a plane \( x_1 \), where \( n_i(x_1) = p_{to} \), and to the left of plane \( x_1 \), the injected carriers will dominate and \( p_{to} \) can be neglected.

![Figure 2.6: Regional approximation diagram; schematic energy band of SCL current injection into an insulator in the presence of single set of deep traps.](image)

The current density and Poisson’s equations for region I are expressed as:

\[
J = en\mu E \\
\frac{dE}{dx} = \frac{e}{\varepsilon} n
\]
\[ n(x_1) = N_t \] 2.19

Where, \( N_t \) is the concentration of deep traps.

The current density and Poisson’s equations for region II are expressed as:

\[ J = e n \mu E \] 2.20

\[ \frac{dE}{dx} = \frac{e}{\varepsilon} N_t \] 2.21

\[ n(x_2) = n_o \] 2.22

The current density and Poisson’s equations for region II are expressed as:

\[ J = e n \mu E \] 2.23

\[ \frac{dE}{dx} = 0 \] 2.24

In the region 1, the injected carriers dominate the current flow. The current-voltage characteristic of the insulator in region 1 follow the trap free law or the Child’s law and is given by,

\[ J = \frac{9}{8} \varepsilon \mu V^2 \] 2.25
In the region 2, the deep traps dominate the current-voltage characteristics. This region corresponds to the TFL regime, the current-voltage relationship is given by:

\[ J = 2en_0\mu\alpha \left( 3en_0\alpha L - \sqrt{12e^2n_0^2A^2L^2 - 6\varepsilon en_0\alpha V} \right) \frac{\varepsilon}{\varepsilon} \] 2.26

Where, \( \alpha \) is the ratio of the density of the unfilled deep traps to the thermal carrier concentration.

At lower injection level, the thermal carriers dominate the current flow. This corresponds to the Ohm’s law region; the current-voltage relationship in this region is given by:

\[ J = en_0\mu \left( en_0\alpha L - \sqrt{e^2n_0^2\alpha^2L^2 - 2\varepsilon en_0\alpha V} \right) \frac{\varepsilon}{\varepsilon} \] 2.27

The cross-over voltage from the Ohm’s law region to the TFL region is given by:

\[ V_{cr1} = \frac{1}{2} \frac{en_0\alpha L^2}{\varepsilon} \] 2.28

The cross-over voltage from the TFL region to the Child’s law region is given by:

\[ V_{cr2} = \frac{4}{3} \frac{en_0\alpha L^2}{\varepsilon} \] 2.29

The \( J-V \) plot of a typical slab of insulator in the presence of deep traps is shown in figure 2.7.
2.4. Current-Voltage Characteristic of Insulator in Presence of Shallow Traps

An electron trap at level $E_t$ is said to be shallow if the Fermi level lies below $E_t$, $(E_t-F)/kT > 1$. From equation 2.11, we have,

$$\frac{n}{n_t} = \frac{p}{p_t} = \frac{N}{gN_t} = \frac{N_c}{gN_t} \exp\left(\frac{E_t - E_c}{kT}\right) = \theta$$  \hspace{1cm} 2.30

Where $\theta$ is a constant, independent of injection level, so long as the trap level remains shallow. The shallow traps of concentration $N_t$ at energy $E_t$ will substantially affect the space charge limited injection current if $\theta < 1$.

For the formulation of the shallow traps, the insulator layer is divided into four regions. The energy level of the shallow traps lie above the Fermi level but at higher injection level, the Fermi level rises above the trap energy level and the shallow traps start behaving as deep traps. To take account of this transition, we need to incorporate one extra region.

As shown in the figure 2.8, similar to the deep trap case, there will be a region from the cathode (x=0) to plane $x_1$ where the injected carriers dominate the current flow. In this region, the Poisson’s equation and the current density equation are given by:

$$J = en\mu E$$  \hspace{1cm} 2.31

$$\frac{dE}{dx} = \frac{e}{\varepsilon} n$$  \hspace{1cm} 2.32
Figure 2.7: Family of J-V curves of the current flow in an insulator for different concentration of deep traps. With the increasing concentration of traps, the $V_{TFL}$ voltage increases.
Figure 2.8: Schematic energy band of SCL current injection into an insulator in the presence of single set of shallow traps.

In the region between the planes $x_1$ and $x_2$, the quasi Fermi level is above the trap level as shown in the figure 2.8. The traps in this region behave as deep traps, the current density and the Poisson’s equation are given by:

$$J = en\mu E$$

$$\frac{dE}{dx} = \frac{e}{\varepsilon} N_t$$

$$n(x_2) = \frac{N}{g} = \frac{N}{g} \exp\left(\frac{E_t - E_c}{kT}\right)$$
At $x_2$, the quasi Fermi level is at the same level as the trap level. To the right of $x_2$, the quasi Fermi level goes below the trap level and the traps start behaving as shallow traps. Since the shallow traps cannot be filled at room temperature, the charges due to both the mobile electrons in the conduction band and the trapped electrons need to be considered in the Poisson’s equation. The shallow traps capture the free electrons and thermally emit the electrons to the conduction band and in the steady state this process will be repeated. In this region, the current density and the Poisson’s equations are given by:

$$J = en\mu E$$  \hspace{1cm} 2.37

$$\frac{dE}{dx} = e \frac{n}{\varepsilon \theta}$$  \hspace{1cm} 2.38

$$\frac{1}{\theta} = 1 + \frac{gN_i}{N}, \quad \theta < 1$$  \hspace{1cm} 2.39

$$n(x_3) = n_o$$  \hspace{1cm} 2.40

Finally, at low injection level, there will be a plane $x_3$ inside the insulator where the concentration of free carriers is equal to the thermal carrier concentration. To the right of $x_3$, the thermal carriers dominate the current flow. The current density and the Poisson’s equations in this region are given by:

$$J = en\mu E$$  \hspace{1cm} 2.41

$$\frac{dE}{dx} = 0$$  \hspace{1cm} 2.42
Considering the continuity of the current and the electric field in crossing the boundary between two adjacent regions, the current density and the Poisson’s equations are solved for each of the regions and we obtain the solutions by imposing the boundary conditions.

The solution to Region 1 is given by:

\[ J = \frac{9 \varepsilon \mu V^2}{8 L^3} \]  \hspace{1cm} 2.43

Equation 2.43 is the trap free square law or the Child’s law.

The solution to Region 2 is given by:

\[ J = \left( \frac{2en_o \mu A}{\varepsilon} \right) \left( 3en_o \alpha L - \sqrt{12e^2 n_o^2 \alpha^2 L^2 - 6en_o \alpha V} \right) \]  \hspace{1cm} 2.44

The cross over voltage between Regions 1 and 2 is given by:

\[ V = \frac{4 en_o \alpha L^2}{3 \varepsilon} \]  \hspace{1cm} 2.45

The current voltage relationship in Region 3 is given by:
\[
J = \sqrt{6e_n\mu\alpha} \sqrt{\frac{\varepsilon}{3g + 2\mu^3\theta \left( \frac{g(g\theta - 2e)}{e^2 n_o^2 \mu^2 \theta \alpha^2} \right)^{3/2} e^3 n_o^3 \alpha^3}} e_n\alpha V
\]

2.46

The cross over voltage between Regions 2 and 3 is given by:

\[
V = \frac{1}{2} \frac{e_n\alpha L^2}{\varepsilon} + \frac{1}{3} \frac{e\alpha^2\theta n_o g L^2}{\varepsilon} - \frac{1}{3} \frac{\alpha\theta g L}{\varepsilon}
\]

2.47

In region 4, the thermal carriers dominate; the current-voltage relationship is Ohmic. The solution to region 4 is given by:

\[
J = \frac{e_n\mu \left( 3e_n L - \sqrt{9e^2 n_o^2 L^2 - 6\varepsilon e_n V} \right)}{\theta \varepsilon}
\]

2.48

The cross over voltage between Regions 3 and 4 is given by:

\[
V = \frac{4}{3} \frac{e_n L^2}{\theta \varepsilon}
\]

2.49
Figure 2.9: Comparison of the $J$-$V$ profiles of SCL current flow through an insulator in the presence of deep traps (blue curves) and shallow traps (red curves). $V_{TFL}$ voltages of the SCL current in the presence of shallow traps are higher than that of the SCL current in the presence of deep traps.

Figure 2.9 shows the comparison between the $J$-$V$ characteristics of the insulator in the presence of deep traps and shallow traps. We observe that the $V_{TFL}$ voltage is higher for shallow traps than that for the deep traps which indicates that more deep the trap is, its effect on the current transport mechanism is minimum.
2.5. Mechanism of the Gate Leakage Current in AlGaN/GaN HFETs

The gate leakage measurement data of AlGaN/GaN HFETs do not show the effect of deep traps. In the $I-V$ profile of the gate leakage measurement data, we do not observe a sharp rise in the current which is the signature of the $V_{TFL}$ voltage being crossed. We can assume that however large the injection might be, the Fermi level never crosses the trap level and so the trap free square law or the Child’s law does not come to play. The requirement for the initiation of space charge effects in an insulator or semiconductor is that the injected carrier concentration must be comparable to the background doping concentration. As the AlGaN layer is undoped, any injection from an external source will create a local imbalance in the internal electric field resulting in space charge effects. We derive a physics based model which demonstrates the gate leakage in AlGaN/GaN HFETs by considering SCL current flow through the surface of the AlGaN layer. The undoped AlGaN surface layer is considered as a slab of insulator and the SCL current flow is evaluated through the insulator in the presence of traps. We have devised the gate leakage model by incorporating two levels of shallow traps in the AlGaN surface layer between the gate and the drain electrodes. The new model uses the physics of SCL current to explain the flow of the injected electrons from the gate terminal to the drain end. It is demonstrated that the gate leakage model accurately predicts the measured gate leakage of one particular AlGaN/GaN device resulting from the current conduction through the AlGaN surface layer in the presence of shallow trap levels having activation energy of 0.57 eV and 0.75 eV below the conduction band.
Traps around 0.57 eV with respect to the conduction band edge in AlGaN is widely observed in DLTS and other transient techniques [19] [20] [21]. Traps having activation energy between 0.62 and 0.90 eV have also been observed in AlGaN in the ON-state experiments; additionally, trap level of 0.74 eV is measured in the $V_{DS}=0$ state where device self-heating is negligible [22]. Closely spaced shallow traps of 0.57 eV and 0.75 eV below the conduction band in AlGaN/GaN HFETs are found to have the major impact on device degradation, as reported from DLOS/DLTS and related electronic optical local measurements [23].

As shown in figure 2.10, 0.57 eV and 0.75 eV trap levels have the most significant impact on $R_D$ in the access region. The Arrhenius plots show these levels of two resolvable traps common to four samples as depicted in figure 2.11.

For the model formulation, the AlGaN layer in the drain access region is divided into three regions on the basis of the dominance of different charge carriers in the regions. The Poisson’s and the current density equations are defined for each of the regions and the solutions are obtained by imposing the boundary conditions.
Figure 2.10: Drain controlled CID-DLTS of AlGaN/GaN HFET showing two dominant levels of traps [23].

Figure 2.11: Arrhenius plot shows two resolvable traps of AlGaN/GaN HFETs [23].
For the formulation of the gate leakage model, the AlGaN surface layer is divided into three regions as shown in the figure 2.12. At relatively low currents there will be a plane at distance $x_2$ from the gate to the right of which the thermal carrier concentration is higher than the injected free carrier concentration and the current–voltage relationship is Ohmic. To the left of this plane, we observe the first shallow trap region where the current flow is affected by the traps at level $E_{t1}$, which dominates up to the point $x_1$. At still higher voltage we observe the second shallow trap region which extends to the left of $x_1$ where the flow of the electrons travelling at the saturated velocity is being affected by the shallow traps at level $E_{t2}$. As AlGaN is a wide band gap semiconductor, the probability of the Fermi level crossing the trap level is low and the shallow traps dominate the trap induced current flow. This situation is observed in the measurement data. Also, for any injection level the Fermi level does not cross the trap level, with the result that the $V_{TFL}$ voltage is never reached and the trap free square law is not observed. For the formulation of this model, the gate is considered as an infinite reservoir of electrons.

The current density and the Poisson’s equations for the Region 1 in the AlGaN surface layer are given as:

$$J = en\mu E$$

2.50
Figure 2.12: Schematic of energy band structure. Regional Approximation diagram for the problem of SCL current injection into the AlGaN surface layer with two levels of surface traps, $F_0$ is the Fermi level at thermal equilibrium.

\[
\frac{dE}{dx} = \frac{en}{\varepsilon\theta_2} \quad 2.51
\]

Where,

\[
\frac{1}{\theta_2} = 1 + \frac{gN_{t2}}{N_2} \quad 2.52
\]

\[N_2 = N_t \exp \left[ \frac{(E_{t2} - E_t)}{KT} \right] \quad 2.53\]

The current density and the Possion’s equations in the Region 2 are given by:

\[J = en\mu E \quad 2.54\]
\[
\frac{dE}{dx} = \frac{en}{\varepsilon \theta_1}
\]

Where,

\[
\frac{1}{\theta_1} = 1 + \frac{gN_{t1}}{N_1}
\]

\[
N_1 = N_e \exp \left[ \frac{(E_{t1} - E_c)}{K T} \right]
\]

Where, where, \( N_{t1} \) and \( N_{t2} \) are the trap densities at level \( E_{t1} \) and \( E_{t2} \) respectively, \( g \) is the degeneracy factor (here it is assumed as 1).

The current density and the Poisson’s equation in region 3 are given by:

\[
J = en \mu E
\]

\[
\frac{dE}{dx} = 0
\]

The current density and the Poisson’s equations are solved for each region, and voltage and electric field continuity is enforced at the boundaries of the different regions to obtain the solutions. In region I, the voltage level is high and so is the electric field. In a semiconductor when the magnitude of the electric field exceeds the saturation electric field value, the electron velocity is no longer a linear function of the electric field. In the current density
equation, in region 1, saturation velocity term is incorporated instead of constant low field mobility. When velocity saturation is considered, instead of square law dependence, we observe a linear relationship between the SCL current and the applied voltage. The solutions for the regions 1, 2 and 3 are given below:

\[ J_I = \frac{2\varepsilon \theta_2 v_{sat} V}{L^2} \]  
2.60

\[ J_{II} = \frac{9 \varepsilon \mu \theta_1 V^2}{8 L^3} \]  
2.61

\[ J_{III} = \frac{(3L n_0 e - \sqrt{9 L^2 n_0 e^2 - 6\varepsilon \varepsilon \theta_1 n_0 V}) e \mu n_0}{\varepsilon \theta_1} \]  
2.62

The cross-over voltage from the Ohm’s law region to the first shallow trap region is:

\[ V_1 = \frac{4}{3} \frac{en_0 L^2}{\varepsilon \theta_1} \]  
2.63

And the cross-over voltage from the first shallow trap region to the second shallow trap region (velocity saturation region) is:
where, \( \mu \) is the low field mobility, \( v_{sat} \) is the saturated velocity, and \( L \) is the gate to drain spacing.

2.6. Comparison with Experimental Data

The modeled and measured gate leakage current densities versus the gate-drain voltage are shown in figure 2.13. Excellent agreement of the modeled and measured data is clearly seen for all the three regions in the \( J-V \) characteristic. The model predicts for the first time the change in the slope of the gate current as function of the gate-drain voltage in agreement with the measurement data [24]. The measured industrial device is a 400 micron HFET with Al composition of 23.5%. The DC measurement is done using Cascade Microtech probe station and Agilent E5270A 8-Slot Parametric Measurement Mainframe. Referred to figure 2.13, three distinctive regions have been observed in the gate leakage current density versus gate-drain voltage plot: the ohmic region; the shallow trap regime; and the velocity saturation region. The cross-over voltages, which separate the three regions, depend on the concentration of the traps, the depth of the trap levels, the material properties and dimensions of the device. As predicted earlier, the Fermi level lies below the trap level and so a very steep current rise is not observed as the \( V_{TFL} \) voltage is never reached. Electron velocity saturates after a certain voltage when the 2nd level of trap starts affecting the space charge.
limited current, and instead of the trap induced square law, a linear trap induced $J-V$
relationship is observed. As indicated in equations 2.60 - 2.64 and figure 2.13, the Ohm’s
law region and the shallow trap region are affected by the first level of shallow trap. Ohm’s
law will dominate up to voltage $V_1$ where the injected free-electron concentration becomes
comparable to the thermal electron concentration $n_o$. The cross-over voltage $V_1$ depends on
the depth and concentration of the first level of trap, the thermal electron concentration, and
other material properties. The 2nd level of trap affects the velocity saturation region. The
cross-over voltage $V_2$ depends on the depth and concentration of both the 1st and 2nd levels
of traps, and other material properties.

Figure 2.13 shows the agreement of the simulation data with the measured data of an
industrial device. As shown in the plot, Ohm’s law dominates until $V= V_1$ (6.256 V), then the
first level of the shallow traps at 0.75 eV below the conduction band dominates until $V=V_2$
(31.986 V) when the electron velocity saturates, and the effect of the next level of traps at
0.57 eV below the conduction band starts affecting the space charge limited current flow.
The cross-over voltages $V_1$ and $V_2$ are calculated from the equations 2.63 and 2.64, and using
the parameter values given in Table 2.1. The activation energies of both the 1st and 2nd
levels of traps are consistent with the measured data [22].

Figure 2.14 shows agreement between the modeled and measured data of an identical device
from a different wafer with the first and second levels of trap at 0.75 eV and 0.57 eV below
the conduction band, respectively. The model accurately predicts all three different regions of
the $J$-$V$ characteristic of the measurement data. Table 2.1 shows the parameter values used in the model simulation. The cross-over voltages are $V_1=4.301$ V and $V_2=18.720$ V. The trap densities, low field mobility, and saturation velocity are used to fit the model to experimental data. The trap densities are consistent with the measured data [25].

Table 2.1: Parameter values used in the gate leakage formulation.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Values used in Figure 2.13</th>
<th>Values used in Figure 2.14</th>
</tr>
</thead>
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</table>
Figure 2.13: Measured and modeled gate leakage current density versus gate-drain voltage for AlGaN/GaN HFET, $V_1=6.256$ V and $V_2=31.986$ V.
Figure 2.14: Measured and modeled gate leakage current density versus gate-drain voltage for AlGaN/GaN HFET, $V_{1}=4.301$ V and $V_{2}=18.720$ V.
2.7. Conclusion

A new model of the gate leakage in AlGaN/GaN HFETs by considering only the surface of the device as the conducting path is presented. The model is based on the space charge limited current in the presence of traps. We have formulated each of the three regions by a local governing differential equation, with associated boundary conditions. The model is entirely physics based and requires only the physical dimensions and the material properties of the device. We have demonstrated the model by comparison of model simulation results with measurements of an industrial AlGaN/GaN device and obtain excellent agreement for the modeled and measured gate leakage data. Two levels of shallow traps are found to dominate the gate leakage current. The model, for the first time, predicts accurately the experimentally observed change of slope of the gate leakage current versus the gate to drain voltage. Velocity saturation is found to affect the third region of the $J-V$ characteristic. Although the model accurately matches the gate leakage measurement data of one particular AlGaN/GaN device, the model only considers the surface as the conducting path and completely ignores the tunneling of the electrons from the gate to the 2DEG channel which constitutes the secondary path of the leakage current. The model does not give a quantitative explanation of considering the gate as an infinite reservoir of electrons. In the following chapter a comprehensive model of the gate leakage current by considering both the surface and the 2DEG as the conducting paths for the gate leakage current will be presented.
REFERENCES


2003.


Chapter 3: Comprehensive Modeling of the Gate Leakage Current in GaN HFETs

3.1 Introduction

A comprehensive physics based model of the gate leakage current in nitride-based HFETs is demonstrated and used to explain leakage currents in these devices when under high field operation. In the first section, the gate leakage current in AlGaN/GaN HFETs is explained by considering, for the first time, two paths for the leakage current flow from the gate electrode to the drain: surface layer conduction, and conduction from the gate to the two-dimensional electron gas (2DEG) channel. The current transport mechanism through the surface of the device is modeled using space charge limited (SCL) transport in the presence of shallow traps. Trap assisted tunneling (TAT) is considered for the evaluation of the electrons tunneling from the Schottky gate contact (on the drain side) to the 2DEG channel. The model appropriately explains the gate leakage current of AlGaN/GaN HFETs for drain voltages up to 170 V and is verified by comparing the model results with the measured gate leakage data of industrial devices. The trap levels extracted from the model are consistent with the reports presented in the literature. In the second section, the gate leakage current of N-polar InAlN/GaN HFETs is modeled by considering the SCL current flow through the surface layer in the presence of deep traps.
The gate leakage model considering only the surface as the conducting path accurately explained the gate leakage mechanism of one particular AlGaN/GaN device but it could not explain the gate leakage data of a wide range of devices. All the gate leakage data of industrial and UCSB devices have similar $I$-$V$ characteristics as shown in figure 3.1. Unlike the previous set of gate leakage data shown in Chapter 2, we observe that the extrapolation of the velocity saturation region of the gate leakage $I$-$V$ plot does not pass through the origin. If we extra-plot the velocity saturation region of the measurement data, it projects an offset in current axis.

In the earlier formulation of the gate leakage current considering only the surface as the conduction path, the current density voltage relationship in the velocity saturation region is given by:

$$J = \frac{2\varepsilon \theta^2_{sat} V}{L^2}$$  \hspace{1cm} 3.1

In the velocity saturation region, the current is a linear function of voltage in the presence of space charge effects. From equation 3.1, we observe that at ‘$V$’ equals to zero, ‘$J$’ is equal to zero.
In the current scenario, the measurement data demands the addition of a constant term in the expression of the current voltage relationship in the velocity saturation region to take account of the offset term. The offset term cannot be explained by the current flowing through the path where there are space charge effects. In the velocity saturation region, the current flowing in the 2DEG is constant and is not a function of the voltage since there are no space
charge effects in the 2DEG channel in the drain access region. So, the gate leakage current flow through the 2DEG represents the offset in the measurement data and the linear rise of current with voltage in the velocity saturation region indicates the flow of SCL current through the surface of the device. Hence, the gate leakage measurement data indicates two paths for the gate leakage current flow.

3.2 Comprehensive Modeling of the Gate Leakage Current in AlGaN/GaN HFETs

3.2.1 Theory

We derive an analytical model of the gate leakage current in AlGaN/GaN HFETs by considering two current paths for the gate leakage current flow: (1) current through the surface layer from the gate to the drain, and (2) current flow from the gate to the 2DEG channel at the AlGaN/GaN interface. The GaN HFET device is shown in figure 3.2. A thin layer (~30Å) of GaN forms the top surface of the device followed by an AlGaN layer of 220Å and a thick GaN buffer layer. Due to the polarization effects, negative charges are induced at the surface and at the GaN_cap/AlGaN interface and positive charges are induced at the AlGaN/GaN interface and at the bottom of the device [1]. The net contribution of the polarization induced charges to the total space charge is zero. Because of the polarization charges and the band bending of the heterostructure, a large concentration of electrons (~1x10^{13} cm^{-2}) accumulates at the GaN side of the AlGaN/GaN interface forming the 2DEG conducting channel.
Figure 3.2: Structure of a typical AlGaN/GaN HFET showing the polarization charges at the different interfaces, traps and the two paths for the gate leakage current- surface layer and the 2DEG channel.

The TCAD simulation using the 2-D numerical device simulator Silvaco™ Atlas of the energy band profile of the AlGaN/GaN HFET is shown in figure 3.3. We observe that there are two regions for the formation of an electron channel- the surface and the 2DEG. The electrons tunneling from the gate electrode will accumulate at the surface and at the 2DEG forming two channels for the gate leakage current. The trap assisted tunneling (TAT) and Fowler-Nordheim (FN) tunneling current versus the vertical electric field is shown in figure 3.5. Due to the abundance of traps in the surface and in the AlGaN layer at the gate edge
drain side, the trap assisted tunneling rate will be much higher than the conventional Fowler-Nordheim tunneling rate (as shown in figure 3.5) and so the FN tunneling mechanism can be ignored in the formulation of the gate leakage model. Also, the thermionic emission of electrons from the gate metal to the semiconductor is negligible [2]. At the AlGaN layer traps around 0.57 eV below the conduction band edge are widely observed using DLTS and other transient techniques [3] [4] [5] [6]. This level of trap will be responsible for the TAT mechanism from the gate electrode to the 2DEG channel. At the surface layer of the device shallower traps are in abundance. The TAT rate is higher in case of shallow traps than the deep traps (as confirmed from the figure 3.5), so for the formulation of the current transport mechanism through the surface, the gate electrode can be assumed as an infinite reservoir of electrons and the conduction is considered as transport limited. Due to the polarization charges and the band bending there exists a strong vertical electric field at the surface and at the AlGaN/GaN interface. In a field-plated device, the vertical electrical field is not significantly affected by the changing drain voltage, as verified by the atlas simulations shown in figure 3.4. Since with the increasing drain voltage the vertical electric field beneath the gate region remains nearly at a fixed value, the variation of drain voltage imposes minimum effect on the tunneling rate of the electrons from the gate electrode to the surface and to the 2DEG channel.
Figure 3.3: TCAD simulation of the energy band profile along a vertical cutline of an AlGaN/GaN HFET. The polarization charges at the different interfaces highly impact the band structure of the heterojunction device.

The Fowler-Nordheim tunneling current density is given by the expression [7],

\[
J = \left( \frac{q^3 E^2}{8 \pi h \phi} \right) \exp \left( - \frac{4 (2m_0)^{1/2} \phi_m^{3/2}}{3hqE} \right)
\]  \hspace{1cm} (3.2)

Where, \( h \)= Planck’s constant, \( q \)= electronic charge, \( E \)= electric field, \( \phi_m \)= barrier height, and \( m_0 \)= free-electron mass.

The expression for the trap-assisted tunneling current density is given by:
Where,

\[
J_t = \frac{C_t q N_t}{3} \left( \frac{\frac{3}{2} \psi^2}{E} \right) e^{\left( \frac{3}{2} \psi^2 \right)} \left( 1 - 1 \ln \left( 1 + e^{\left( \frac{3}{2} \psi^2 \right)} \times e^{\left( \frac{3}{2} \psi^2 t \right)} \right) \right)
\]

3.3

Where,

\[
A = \frac{4 \sqrt{2 q m_0}}{3 h}
\]

3.4

\[
C_t = \left( \frac{m_M}{m_0} \right)^{5/2} \frac{8 E_e^2}{3 h \sqrt{\psi - E_e}}
\]

3.5

\[C_t \text{ depends on the trap energy [8].}\]

\[\psi = \text{trap energy level, } E_e = \text{electron energy (0.2 eV [8]), } t = \text{barrier thickness, } N_t = \text{trap density.}\]

The concentration of the electrons that tunnel from the gate electrode can be expressed as:

\[
n_s = \frac{J_t}{q v_R} = \frac{J_t}{q \sqrt{\frac{kT}{2\pi m}}}
\]

3.6

Where, \( v_R = \text{Richardson velocity, } k = \text{Boltzmann constant, } T = \text{Temperature.}\)
Figure 3.4: TCAD simulation of the vertical electrical field ($E_y$) along a vertical cutline at the gate edge drain side of a field-plated AlGaN/GaN HFET for different drain voltages with gate voltage fixed at -4 V (pinch-off voltage). For drain voltages higher than 10 V, $E_y$ remains at a fixed value with the increasing drain voltage.

Due to the presence of high electric field and much shallower traps at the surface, the tunneling rate is higher as shown in figure 3.5, and the gate electrode can be considered as an infinite reservoir of electrons in the formulation of the leakage current through the surface. The slightly deeper traps in the AlGaN layer result in a reduced injection of electrons through TAT from the gate electrode to the 2DEG.
The electrons that tunnel from the gate electrode flow to the drain end through the surface layer establishing a path for the gate-leakage current. Due to the accumulation of the tunnel electrons in the surface layer, space charge will affect the current conduction through the surface. The undoped GaN surface layer is considered as an insulator and the current flow through the surface is modeled by incorporating space charge effects in the presence of traps. The presence of electron traps in an insulator will generally impede the current flow, since those traps, which are initially empty, will capture and thereby immobilize most of the injected carriers. The equilibrium trap occupancy results from a balance between capture of electrons into the traps, and their thermal re-emission into the conduction band. The electrons in the conduction band will contribute to the current flow through the GaN surface layer.

To evaluate the SCL current flowing through the surface, the Poisson’s and current density equations are solved for different gate-drain voltage ranges and the solutions for each region are obtained by imposing the boundary conditions. At low drain-gate voltages, the electron velocity increases linearly with the electric field. The current density and Poisson’s equations for this region are expressed as:

\[ J = qn \mu E \]  \hspace{1cm} (3.7)

\[ \frac{dE}{dx} = \frac{qn}{\varepsilon \theta_1} \]  \hspace{1cm} (3.8)
Figure 3.5: Injected carriers concentration at the surface (blue curve), and at the 2DEG channel (red curve) by the trap assisted tunneling (TAT) process from the gate electrode versus the electric field across the tunnel barrier. 0.57 eV of trap level in the AlGaN layer is considered for the TAT of gate electrons to the 2DEG and 0.32 eV level of traps is considered for TAT from the gate electrode to the surface. Fowler-Nordheim (FN) tunneling carrier injection concentration versus the electric field across the barrier is indicated by the green curve for a barrier height of \(~1.2\text{eV}\) [9].

Where,

\[
\frac{1}{\theta} = 1 + \frac{gN_{\parallel}}{N_1}
\]

\(3.9\)
\[ N_1 = N_e \exp \left[ \frac{(E_{t1} - E_c)}{KT} \right] \]  \hspace{1cm} 3.10

Where, \( N_{t1} \) is the trap density at level \( E_{t1} \), \( g \) is the degeneracy factor (here it is assumed as 1), \( \varepsilon \) is the permittivity of the surface layer, \( \mu \) is the electron mobility at the surface.

For slightly higher voltages, when the lateral electric field is near the saturation electric field, the electron velocity does not vary linearly with the electric field but is a square root function of the electric field \([10]\). In this region, the 2nd level of traps starts effecting the SCL current flowing through the surface. The current density and Poisson’s equations for this region are given by:

\[ J = qnE_s^{\frac{1}{2}} \mu E^{\frac{1}{2}} \]  \hspace{1cm} 3.11

\[ \frac{dE}{dx} = \frac{qn}{\varepsilon \theta_2} \]  \hspace{1cm} 3.12

Where,

\[ \frac{1}{\theta_2} = 1 + \frac{gN_{t2}}{N_2} \]  \hspace{1cm} 3.13

\[ N_2 = N_e \exp \left[ \frac{(E_{t2} - E_c)}{KT} \right] \]  \hspace{1cm} 3.14

Where, \( N_{t2} \) is the trap density at level \( E_{t2} \), \( E_s \) is the saturation electric field.
For higher voltages, when the electric field exceeds the value of the saturation electric field of GaN, the electron velocity saturates and is no longer a function of the electric field. The 3\textsuperscript{rd} level of traps effects the SCL current flowing through the surface in this region. The current density and the Poisson’s equations are expressed as:

\[ J = qn v_{sat} \]  

\[ \frac{dE}{dx} = \frac{qn}{\varepsilon\theta_3} \]  

Where,

\[ \frac{1}{\theta_3} = 1 + \frac{gN_{t3}}{N_3} \]  

\[ N_3 = N_c \exp \left[ \frac{(E_{t3} - E_c)}{KT} \right] \]  

Where, \( N_{t3} \) is the trap density at level \( E_{t3} \), \( v_{sat} \) is the saturation velocity at the surface.

The current density and the Poisson’s equations are solved for each region, and voltage and electric field continuity is enforced at the boundaries of the different regions to derive the solutions for all the regions. For the first region, we observe the current through the surface is a function of the square of the voltage; the SCL current-density voltage relationship is given as:
\[ J = \frac{9 \epsilon \mu \theta V^2}{8 L^3} \]  \hspace{1cm} (3.19)

The expression for the current flowing through the surface in this region is:

\[ I_{\text{Surface}} = A \times J = A \times \frac{9 \epsilon \mu \theta V^2}{8 L} \]  \hspace{1cm} (3.20)

where, \( L \) = gate-drain spacing and \( A \) = surface area.

In the second region, when the lateral electric field approaches the saturation electric field value, the SCL current-density is a function of the \( 3/2 \) power of the voltage,

\[ J = \frac{5\sqrt{60}}{27} \epsilon \theta_2 E_s \mu V^2 \frac{1}{L^2} \]  \hspace{1cm} (3.21)

The current flowing through the surface in this region is given by,

\[ I_{\text{Surface}} = A \times \frac{5\sqrt{60}}{27} \epsilon \theta_2 E_s \mu V^2 \frac{1}{L^2} \]  \hspace{1cm} (3.22)

In the third region, the electron velocity saturates at the surface and we observe a linear relationship between the SCL current-density and voltage, expressed as
The saturated current flowing through the surface in this region is expressed as:

\[ J = \frac{2 \varepsilon \theta_3 v_{sat} V}{L^2} \] \hspace{1cm} 3.23

The electrons tunneling from the gate electrode to the 2DEG channel and flowing to the drain electrode forms the second path for the gate leakage current. At or near the pinch off voltage, the depletion region of the gate will extend to the channel and the electrons will be spilled out of the 2DEG. At lower drain-gate voltages, we observe a linear relationship between the current and voltage as the current flowing through the 2DEG depends on the mobility of the electrons in the channel, which is a linear function of the electric field across the channel. The current voltage relationship is expressed as:

\[ I_{Surface} = A \times \frac{2 \varepsilon \theta_3 v_{sat} V}{L^2} \] \hspace{1cm} 3.24

\[ I_{2DEG} = \frac{W q n_s \mu_s V}{L} \] \hspace{1cm} 3.25

where, \( W \) is the width of the device, \( n_s \) is the concentration of the injected electrons tunneled from the gate electrode to the 2DEG channel, and \( \mu_s \) is the low-field electron mobility in the 2DEG. After a certain value of the drain voltage when the electric field across the channel is
close to the saturation electric field of GaN, the mobility will not be a linear function of the electric field. The velocity-field curve of electrons is modeled as [11]:

\[ v(E) = \frac{\mu_s E}{\left(1 + \left(\frac{E}{E_s}\right)^\beta \right)^{1/\beta}} \]  

where, \( E \) is the magnitude of the lateral electric field, \( E_s \) is the saturation electrical field in the 2DEG channel, and \( \beta \geq 1 \) is a real, phenomenological constant that controls the sharpness of the transition of measured velocity from its low field linear response to its high field region. The current flowing through the channel is given as:

\[ I_{2\text{DEG}} = \frac{W q n_s \mu_s \left(\frac{V}{L}\right)}{\left(1 + \left(\frac{V}{E_s L}\right)^\beta \right)^{1/\beta}} \]  

For higher gate-drain voltages when the electric field exceeds \( E_s \), the electron velocity saturates and we observe a constant current with the increasing drain voltage expressed as:

\[ I_{2\text{DEG}} = W q n_s v_{sat} \]  

where, \( v_{sat} \) is the electron saturation velocity in the 2DEG channel.
The total leakage current flowing between the gate and the drain electrodes for each of the regions is given by the summation of the SCL current flowing through the surface and the current flowing through the 2DEG channel.

\[ I_{Total} = I_{Surface} + I_{2DEG} \]

3.2.2 Model Verification

The model is verified by matching the model results with three sets of measured gate leakage data from industrial AlGaN/GaN HFETs. The simulation is performed using Maple. The measured industrial devices are 2x100, 2x700 and 2x200 micron HFETs with Al composition of 23.5%. All three devices contain a thin GaN region (~30Å) at the top which constitutes the surface of the HFET. The thickness of the AlGaN layer is 220Å. The DC gate-drain leakage measurement is made using a Cascade Microtech probe station and Agilent E5270A 8-Slot Parametric Measurement Mainframe. The source terminal is kept floating and a voltage is applied between the gate and the drain electrodes. The voltage at the gate electrode is kept fixed at the pinch-off voltage of the device and the voltage at the drain is ramped from 0-170 V. For the same set of test devices when the source terminal is connected, the gate leakage current remains the same as the two-terminal measurement indicating that the source-drain leakage is negligible. The gate leakage measurement data of 2x100 micron AlGaN/GaN HFET is shown in figure 3.6. From figure 3.6, we observe that the gate leakage current for the first measurement is much higher than the second (measured after 2-3 minutes after the first measurement) or subsequent measurements. Also, the I-V profile of the gate leakage
current for the first measurement does not show the SCL current-voltage characteristics. The gate leakage $I$-$V$ plot for the first measurement is similar to the typical $I$-$V$ characteristics of GaN HFETs in ‘ON’ state. This indicates that the most of the current of the gate leakage for the first measurement flows through the 2DEG channel. When the device is in dormant or ‘ON’ state the 2DEG is populated from the AlGaN donor states and the metal electrodes which act as sources of electrons for the 2DEG channel. When the first measurement of the gate leakage current is performed by keeping the gate electrode below the pinch-off voltage, the electrons in the 2DEG in the drain access region are pumped out of the drain end. This results in the observed higher current for the first measurement of the gate leakage data, even though the gate is below the pinch-off voltage and the source end is disconnected. The sources of electrons in this case are the metal electrodes and the AlGaN donor traps; the electron tunneling from the gate electrode is insignificant as the 2DEG is already filled, so the first measurement of the gate leakage data does not depict the actual gate leakage mechanism of the AlGaN/GaN devices. When the measurement is repeated (after a minute or two) a lower leakage current is detected with SCL current characteristics and we observed consistent $I$-$V$ profiles for the subsequent measurements of the gate leakage current. The source of the electrons of the gate leakage current for the second measurement is the Schottky gate from which electrons tunnel to the surface and the 2DEG channel. The second measurement illustrates the actual mechanism of the gate leakage current of GaN HFETs.

The modeled and the measured gate leakage current are shown in figure 3.7 for the 2x100 micron device. As we can see in the figure, excellent agreement is achieved between the
simulated and measured data. In the $I$-$V$ characteristic, we observe three distinctive regions: (1) A low field region, for gate-drain voltage range of 0- 71.05 V. In this region, the first level of traps effects the SCL current through the surface, the current flowing through the surface is proportional to the squared of the voltage and the current flowing through the 2DEG is linearly proportional to the gate-drain voltage; (2) A high-field region, for voltages between 71.05 V and 121.15 V. When the lateral electric field approaches the saturation electric field, the second level of traps are excited, affecting the SCL current through the surface, which is a function of 3/2 power of the gate-drain voltage, and the current voltage relationship through the 2DEG is given by the equation 3.27; and (3) a velocity saturation region- for gate-drain voltages higher than 121.15 V. When the magnitude of the lateral electric field exceeds the saturation electric field value, the electron velocity saturates both at the surface and at the 2DEG channel, the current flowing through the surface is linearly proportional to the voltage in the velocity saturation region and the $3^{rd}$ level of traps affects the surface current. The $I$-$V$ relationship in the 2DEG is defined by equation 3.28. The model reveals that for the 2x100 micron device, 36.81% of the gate leakage current flows through the surface layer and 63.19% flows through the 2DEG channel. The trap levels and trap densities extracted from the model are listed in Table 3.1.
Figure 3.6: Comparison of the gate leakage measurement data of the first (green curve) and second (red curve) measurement for 2x100 micron AlGaN/GaN HFET.

Figure 3.8 shows the comparison of the measured and simulated gate leakage data for the 2x700 micron device. Again excellent agreement is achieved between the modeled and the measured data. The three distinctive regions, the low field region, the high field region, and the velocity saturation region, are observed in gate-leakage $I$-$V$ characteristic. The cross-over voltages are: 52.20 V and 80.41 V. It is determined from the model that 57.71% and
42.29% of the gate leakage current flows through the surface and the 2DEG respectively for the 2x700 micron device. The parameter values used in the model simulation are given in Table 3.1.

Figure 3.9 shows the modeled and measured gate leakage data for the 2x200 micron device. The cross-over voltages are: 83.49 V and 121.12 V. Table 3.1 lists the parameter values used to fit the model and the measurement data. The model indicates that 53.06% and 46.94% of the gate leakage current flows through the surface and the 2DEG respectively for the 2x200 micron device.

The extracted trap levels from the model are consistent with the values presented in the literature. Traps with activation energy around 200 meV have been observed using backgating current deep level transient spectroscopy and by Fourier transform deep level transient spectroscopy [12] [13]. Traps having activation energy of around 0.32 eV and 0.53 eV in GaN have also been reported [14].
Figure 3.7: Modeled (blue dots) versus measured (red curve) gate-leakage data of 2x100 micron AlGaN/GaN HFET at temperature T=300K. The gate-drain spacing of the device is 19 micron and the length of the source field plate is 4 micron. The voltage at the gate terminal is kept below the pinch-off voltage of the device (-4V).
Figure 3.8: Modeled (blue dots) versus measured gate-leakage (red curve) data of 2x700 micron AlGaN/GaN HFET at temperature T=300K. The gate-drain spacing of the device is 19 micron and the length of the source field plate is 2 micron. The voltage at the gate terminal is kept below the pinch-off voltage of the device (-4V).
Figure 3.9: Modeled (blue dots) versus measured (red curve) gate-leakage data of 2x100 micron AlGaN/GaN HFET at temperature T=300K. The gate-drain spacing of the device is 19 micron and the length of the source field plate is 4 micron. The voltage at the gate terminal is kept below the pinch-off voltage of the device (-4V).
Table 3.1: Parameters used in the model to fit the gate leakage data of industrial 2x100 µ, 2x700 µ, 2x200 µ at room temperature and 2x100 µ at 150°C AlGaN/GaN HFETs.

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<td>Low field mobility (cm(^2)/V·s)</td>
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</tr>
<tr>
<td>Surface</td>
<td>2.9x10(^6)</td>
<td>7.2x10(^6)</td>
<td>8.0x10(^6)</td>
<td>7.3x10(^6)</td>
</tr>
<tr>
<td>2DEG</td>
<td>2.5x10(^7)</td>
<td>2.5x10(^7)</td>
<td>2.5x10(^7)</td>
<td>2.5x10(^7)</td>
</tr>
<tr>
<td>Beta</td>
<td>1.0</td>
<td>1.9</td>
<td>5.5</td>
<td>1.9</td>
</tr>
</tbody>
</table>


The modeled and the measured gate leakage data for the 2x100 micron device at 150°C are shown in figure 3.10. At high temperature the gate leakage current is predicted to increase by the model since the rate of thermal emission of electrons from the traps increases with increasing temperature. The measurement data shows approximately 20 times increase in the gate leakage current for the 2x100 micron device at 150°C as compared to the leakage current at room temperature. The model is used to fit the measured gate leakage data by considering the SCL current flowing through both the GaN-cap (30Å) and AlGaN (220Å) layers. At 150°C because of the high thermal energy, the electrons will thermionically overcome the GaN cap/AlGaN barrier (figure 3.3) and penetrate into the AlGaN region which results in the SCL current flow to the drain electrode through both the AlGaN and GaN-cap layers. The cross-over voltages are: 32.57 V and 41.02 V. The model reveals that for the 2x100 micron device at 150°C, 59.16% of the gate leakage current flows through the GaN_cap and AlGaN layers and 40.84% flows through the 2DEG channel. The extracted values of the model parameters are listed in Table 3.1. Traps having activation energy of around 0.44 eV and 0.59 eV in AlGaN/GaN HFETs have been observed experimentally [15] [16] [17].
Figure 3.10: Modeled (blue dots) versus measured (red curve) gate-leakage data of 2x100 micron AlGaN/GaN HFET at temperature T=423K. The gate-drain spacing of the device is 19 micron and the length of the source field plate is 4 micron. The voltage at the gate terminal is kept below the pinch-off voltage of the device (-4V).
The parameters mentioned in Table 3.1 are extracted by fitting the modeled and measured data. The magnitude and the slope of gate leakage current versus gate-drain voltage and the cross-over voltages play vital role in the parameter extraction. The slope of the first and the second regions of the gate leakage $I-V$ characteristic is highly sensitive to the first and second levels of trap ($E_{t1}$, $E_{t2}$) at the surface, trap level at the AlGaN layer; the slope of the third region of the gate leakage $I-V$ characteristic is sensitive to the third level of trap ($E_{t3}$) at the surface and the trap level in the AlGaN layer. For a 2% change in the value of surface trap level and trap concentration, roughly around 22% and 1.1% change in the gate leakage current is observed respectively; for a 2% variation of the trap level and trap concentration in the AlGaN layer, 76% and 3.5% change in the current is observed respectively; 1.64% and 0.89% change in the gate leakage current is observed for a change of 2% in the value of low field mobility and saturation velocity respectively. The value of the saturation velocity at the surface for the 2x700 and 2x200 micron devices varies 2.5 and 2.7 times than the 2x100 micron device respectively. The saturation velocity at the surface depends on the surface roughness, presence of dislocation and traps which are difficult to control during the growth process. Therefore the value of velocity saturation at the surface differs to some degree for each of the devices. The value of $\beta$, the curvature parameter, which controls the sharpness of the knee of the $v-E$ curves, varies for the different HFETs as shown in Table 3.1. The knee of the $v-E$ curve becomes sharper as $\beta$ increases, the curve is close to the two piece $v-E$ model for larger values of $\beta$ [18]. The gate leakage model is also implemented in commercial circuit simulator AWR Microwave Office using Verilog-A code.
3.3 Modeling of the Gate Leakage Current in N-polar InAlN/GaN HFETs

A physics based model of the gate leakage current in N-polar InAlN/GaN HFETs is demonstrated. The model is based on the space charge limited current flow dominated by the effects of deep traps in the InAlN surface layer. The model predicts accurately the gate-leakage measurement data of the InAlN/GaN HFET. In the pinch-off state, the gate leakage current conduction through the surface of the device in the drain access region dominates the current flow through the two dimensional electron gas channel. One deep trap level and two levels of shallow traps are extracted by fitting the model results with measurement data.

The ability to form heterojunction in InN, AlN, GaN offers different configurations of heterostructures to be formed and allow playing with the polarity of the heterostructures which determine the 2DEG densities. Of the various heterostructures, AlGaN/GaN configuration is the most popular. AlGaN/GaN HFETs demonstrate outstanding performances yielding in the highest output power (30W/mm) of all solid state devices [19]. But due to the lattice mismatch of AlGaN and GaN, the AlGaN layer is under tensile strain which degrades the reliability of the AlGaN/GaN devices. By replacing AlGaN with InAlN the device performance, stability and reliability can be improved as InAlN can be grown lattice matched to GaN [20]. Due to the high value of spontaneous polarization in InAlN, the 2DEG sheet charge density is much higher, even without piezo-polarization, for the InAlN/GaN devices than that of AlGaN/GaN [21]. InAlN/GaN HFETs also display a higher chemical and thermal stability than their AlGaN/GaN counterparts. Due to the high value of
spontaneous polarization in InAlN, it is possible to implement thinner barrier which improves the gate control of the channel current. High aspect ratio and improved electron confinement mitigate the short channel effects in N-polar GaN HFETs [22].

Although the lattice matched N-polar InAlN/GaN heterojunction improves the performance and stability of the device, the gate leakage current of the InAlN/GaN HFETs is comparable or in fact higher than their AlGaN/GaN counterparts. The $I-V$ profile of the gate leakage current of InAlN/GaN HFETs is different from that of AlGaN/GaN HFETs which is characterized by three regions in the $I-V$ plot: shallow trap region, high field region and velocity saturation region [23]. The $I-V$ characteristics of the InAlN/GaN HFET gate leakage indicate a threshold voltage after which the leakage current abruptly increases with the increase in gate-drain voltage. The gate leakage current of the AlGaN/GaN HFETs is dominated by the presence of shallow traps in the surface layer of the device. The contrasting $I-V$ characteristics of the gate leakage current of InAlN/GaN HFETs can be explained by considering the effect of deep traps in the space charge limited (SCL) current flow through the InAlN surface layer. In this paper we present a physics based model considering space charge limited (SCL) current flow through the surface of the device in the presence of deep traps in the InAlN cap layer to demonstrate the gate leakage current in the N-polar InAlN/GaN devices.
3.3.1 Theory

In a typical GaN HFET, the gate leakage current flows through two paths: the surface of the device and the 2DEG channel [23]. Due to the presence of deep traps in the InAlN cap layer, the trap assisted tunneling (TAT) [8] rate from the gate to the 2DEG channel is reduced and the SCL current flowing through the InAlN surface layer plays the dominant role in the gate leakage current in InAlN/GaN HFETs. For the formulation of the gate leakage model, the undoped InAlN layer is considered as an insulator and the SCL current flow is evaluated through the insulator in the presence of traps. In a typical insulator there exist both deep and shallow traps. Traps having its energy level below the Fermi level are called deep traps and those having its energy level above the Fermi level are called shallow traps. In a trap free insulator, all injected electrons remain free, i.e., in the conduction band and all contribute to the space charge and current conduction. The presence of traps in an insulator will impede the current flow at lower injection levels, since those traps initially empty will capture, and thereby immobilized most of the injected charge. However, the amount of excess charge that can be supported by the insulator at an applied voltage is the same whether the excess charges are free or trapped. The trapped charges will not contribute to the current flow but will affect the background electric field.
Figure 3.11: N-polar InAlN/GaN HFET with 20Å InAlN cap layer. The back barrier consists of AlN, InAlN and AlGaN layers.

The N-polar InAlN/GaN HFET is shown in figure 3.11. The device is grown on a sapphire heterosubstrate. The 20 Å InAlN cap layer forms the surface of the device. The indium composition in the InAlN layer of the device is 17.5 percent to achieve lattice match between InAlN and GaN layers. The 2DEG is formed at GaN side of the GaN/AlN interface. The back-barrier is used to increase the 2DEG confinement. The TCAD simulation using the 2-D numerical device simulator Silvaco Atlas of the energy band profile of the InAlN/GaN HFET at the gate edge in the drain access region is shown in figure 3.12. Two regions of electron accumulation in the drain access region can be observed in figure 3.12: the surface layer and the 2DEG channel. The accumulated electrons at the surface and the 2DEG form two paths for the gate leakage current flow. The electric field along the vertical slab of the device is
shown in figure 3.13. Due to lattice matched InAlN and GaN layers there is no additional piezoelectric field across the interface due to the absence of tensile or compressive strain in the InAlN cap layer. Figure 3.14 shows the TAT rate of electrons from the gate versus the vertical electric field for shallow and deep traps levels. It is observed from figure 3.14 that the TAT rate is higher in case of shallow traps (~0.30 eV) than the deep traps (~2.41 eV). The deep traps require high magnitude of electric field to start conducting through the TAT mechanism than the shallow traps. The presence of shallow traps at the surface of InAlN layer at the gate edge in the drain access region facilitates in the high electron injection due to TAT mechanism from the gate to the surface layer. For the formulation of the SCL current through the surface the gate is considered an infinite reservoir of electrons and the current flow through the surface is conduction limited. The gate metal extends into the InAlN layer and the deep traps in the InAlN layer aids in the TAT of electrons from the gate vertically to the InAlN layer which fall in the 2DEG establishing a gate leakage current path to the drain electrode.

But due to the presence of deep trap levels in the InAlN cap layer the TAT injection of electrons from the gate surface to the 2DEG is highly reduced. The vertical electric field across the InAlN cap layer is not high enough to cause appreciable carrier injection from the gate to the 2DEG through TAT mechanism as confirmed from figures 3.13 and 3.14. The tunneling of electrons due to the conventional Fowler-Nordheim (FN) is negligible compared to the TAT mechanism [23] and is ignored in the formulation of the gate leakage current.
The injected electrons from the gate accumulate in the InAlN layer and create a space charge. Most of the injected carriers will be captured by the deep traps in the InAlN layer and for gate-drain voltage less than the trap filled limit voltage ($V_{TFL}$) [24] the surface current will be zero. At $V_{gd}=V_{TFL}$, all the deep traps in the drain access region are filled and the flow of the injected carriers in the InAlN conduction band is affected by the shallow traps. The shallow

![Figure 3.12: TCAD simulation of the energy band profile along a vertical cutline of an InAlN/GaN HFET in the drain access region. The electrons tunneling from the gate accumulate at the surface and the 2DEG due to the band bending resulting from the polarization electric field.](image)
traps cannot be completely filled at room temperature [25]. The equilibrium trap occupancy results from a balance between capture of electrons into the traps, and their thermal remission into the conduction band. The SCL current flowing through the InAlN layer constitutes the primary path for the gate leakage current between the gate and the drain electrodes. The current voltage relationship of the SCL current flowing through the InAlN layer is evaluated by solving the Poisson’s and current density equations. Poisson’s equation in an insulator in the presence of trapped electrons is given by:

\[
\frac{dE}{dx} = \frac{e}{\varepsilon}( (n - n_o) + (n_t - n_{to}) )
\]

where, \( n \) = concentration of free carriers, \( n_o \) = concentration of free carriers in thermal equilibrium, \( n_t \) = concentration of trapped electrons, and \( n_{to} \) = concentration of trapped electrons in thermal equilibrium.

Using the current density equation and after simplification we can derive the following differential equation:

\[
\frac{dE}{dx} - \frac{J}{\varepsilon \mu} E^{-1} - \frac{e}{\varepsilon} (n_t - n_{to} - n_o) = 0
\]

We can derive the exact solution to the above differential equation in terms of the LambertW function [26]. The solution is too complicated for robust implementation in commercial software. However, the problem can be simplified by application of regional approximation:
the InAlN layer is divided into three regions on the basis of the dominance of different charge carriers in the regions.

Figure 3.13: TCAD simulation of the vertical electrical field (E_y) along a vertical cutline at the gate edge of an InAlN/GaN HFET for increasing gate voltage.

As shown in figure 3.15, the injected free carrier concentration n_i decreases monotonically from \( \infty \) at x=0. At low injection level, there will be a plane x_3 where the concentration of free carriers is equal to the thermal carrier concentration, the SCL current in this region is
dominated by the thermal carriers. In the region to the left of $x_3$ the deep traps start filling up, and the inception of the SCL current through the InAlN layer is affected by the shallow traps at level $E_{t1}$. At plane $x_2$ all the deep traps are filled as the gate-drain voltage exceeds the $V_{TFL}$.

Figure 3.14: Injected carriers concentration at the surface (blue curve), and at the 2DEG channel (red curve) by the trap assisted tunneling (TAT) process from the gate electrode versus the electric field across the tunnel barrier. 2.41 eV of trap level in the InAlN layer is considered for the TAT of gate electrons to the 2DEG and 0.30 eV level of traps is considered for TAT from the gate electrode to the surface.

voltage; in this region the injected carriers will dominate the current flow and the square law dependence of the SCL current versus the voltage is affected by the 1st level of shallow traps.
At slightly higher voltage we observe the second shallow trap region which extends to the left of $x_1$ where the flow of the SCL current is affected by the shallow traps at level $E_{t2}$.

The Poisson’s equation in Region 1 where the current flow is dominated by the 2$^{nd}$ level of shallow traps in the InAlN cap layer is given by:

$$\frac{dE}{dx} = \frac{e \ n}{\varepsilon \ \theta_2}$$  \hspace{1cm} 3.32

Where,

$$\frac{1}{\theta_2} = 1 + \frac{g N_{t2}}{N_2}$$  \hspace{1cm} 3.33

$$N_2 = N_c \exp \left[ \frac{(E_{t2} - E_c)}{KT} \right]$$  \hspace{1cm} 3.34

Where, $N_{t2}$ is the trap density at level $E_{t2}$, $g$ is the degeneracy factor (here it is assumed as 1), $\varepsilon$ is the permittivity of the surface layer.

The Poisson’s equation in Region 2 where the current flow is dominated by the 1$^{st}$ level of shallow traps in the InAlN cap layer is given by:

$$\frac{dE}{dx} = \frac{e \ n}{\varepsilon \ \theta_1}$$  \hspace{1cm} 3.35
Where,

\[
\frac{1}{\theta_2} = 1 + \frac{gN_{t2}}{N_2}
\]

3.36

Figure 3.15: Schematic of energy band diagram of the InAlN cap layer in the drain access region showing the four regions signifying the dominance of the different charge carriers on the SCL current flow.

\[
N_2 = N_c \exp \left[ \frac{(E_{t2} - E_c)}{KT} \right]
\]

3.37

Where, \(N_{t1}\) is the trap density at level \(E_{t1}\).
In Region 3, the SCL current flow is dominated by the deep traps in the InAlN cap layer, the Poisson’s equation for this region is given by:

\[
\frac{dE}{dx} = \frac{e}{\varepsilon} N
\]  

3.38

Where,

\[
N = \frac{N_t}{1 + g \exp\left(\frac{F_o - E_t}{KT}\right)}
\]  

3.39

Where, \(N_t\) is the concentration of the deep traps at level \(E_t\).

The thermal carrier concentration dominate the current flow in Region 4, the Poisson’s equation is expressed as:

\[
\frac{dE}{dx} = 0
\]  

3.40

The Poisson’s equation is solved along with the current density equation for each region. The voltage and electric field continuity is enforced at the boundaries of the different regions to derive the solutions for all the regions. For the first region, we observe that the current is a function of the square of the voltage. In this region the second level of shallow traps affects
the SCL current flow through the InAlN layer; the SCL current-density voltage relationship is expressed as:

\[ J = \frac{9 \varepsilon \mu \theta^2 V^2}{8 \frac{L^3}{L^3}} \tag{3.41} \]

In the second region, we observe similar square law current-voltage dependence as the first region. In this region the first level of shallow traps dominate the SCL current flow through the surface layer; the SCL current-density voltage relationship is given by:

\[ J = \frac{9 \varepsilon \mu \theta^2 V^2}{8 \frac{L^3}{L^3}} \tag{3.42} \]

The \( V_{TFL} \) is the cross-over voltage between the second and the third region. In the third region, the deep traps start filling up, and the electron flow through the conduction band is affected by the first level of shallow traps. The current-density voltage relationship is given as:

\[ J = \frac{6q^2 \mu N^2 \theta_1 L - 12q^2 \mu N^2 L}{3\varepsilon \theta_1^2 - 4\varepsilon \theta_1} - \frac{\sqrt{36q^4 \mu^2 N^4 L^2 - 24q^4 \mu^2 N^4 \theta_1 L^2 + 18q^3 \mu^2 N^3 \varepsilon \theta_1^3 V - 24q^3 \mu^2 N^3 \varepsilon \theta_1 V}}{3\varepsilon \theta_1^2 - 4\varepsilon \theta_1} \tag{3.43} \]

The current-voltage relationship in the fourth region is linear and is dominated by the thermal carriers in the InAlN layer; the SCL current-density voltage relationship is given as:
\[ J = \frac{q^2 \mu N n_o L - \sqrt{q^4 \mu^2 N^2 n_o^2 L^2 - 2q^3 \mu^2 N n_o^2 eV}}{\varepsilon} \]

3.3.2 Model Verification

The model is verified by comparing the model results against the gate leakage measurement data of 1x150 micron InAlN/GaN HFETs with InAlN cap and AlGaN cap. The simulation is performed using Maple. The \( I-V \) profile of the gate leakage data for the InAlN/GaN device with AlGaN cap with Al composition of 30 percent shown in figure 3.16 is similar to the gate leakage characteristics of the AlGaN/GaN HFETs shown in figures 3.7 – 3.10. An excellent agreement is achieved between the modeled and the measurement data. The gate leakage current of the InAlN/GaN HFET is dominated by the SCL current in the presence of shallow traps. The cross-over voltages are: 2.0 V and 6.0 V. The extracted values of the model parameters are listed in Table 3.2.
Figure 3.16: Modeled (blue dots) versus measured (red curve) gate-leakage data of 150 micron N-polar InAlN/GaN UCSB device with AlGaN cap on top. The gate-drain spacing of the device is 0.5 micron. The voltage at the gate terminal is kept below the pinch-off voltage of the device.
Table 3.2: Model parameters of 1x150 micron N-polar InAlN/GaN HFET with AlGaN cap.

<table>
<thead>
<tr>
<th>150 micron InGaN/GaN HFET with AlGaN cap</th>
<th>Trap energy (eV)</th>
<th>Trap concentration (cm⁻³)</th>
</tr>
</thead>
<tbody>
<tr>
<td>AlGaN Surface</td>
<td>0.019</td>
<td>5x10¹⁷</td>
</tr>
<tr>
<td></td>
<td>0.232</td>
<td>1.84x10¹³</td>
</tr>
<tr>
<td></td>
<td>0.335</td>
<td>1.34x10¹⁷</td>
</tr>
<tr>
<td>AlGaN</td>
<td>0.57</td>
<td>3.0x10¹⁷</td>
</tr>
<tr>
<td>Low field mobility (cm²/V·s)</td>
<td>Surface</td>
<td>2DEG</td>
</tr>
<tr>
<td></td>
<td>150</td>
<td>1200</td>
</tr>
<tr>
<td>Velocity saturation (cm/s)</td>
<td>Surface</td>
<td>2DEG</td>
</tr>
<tr>
<td></td>
<td>1.2x10⁴</td>
<td>2.0x10⁷</td>
</tr>
<tr>
<td>Beta</td>
<td></td>
<td>1.9</td>
</tr>
</tbody>
</table>

The modeled and measured gate leakage current densities versus the gate-drain voltage of the InAlN/GaN HFET with InAlN cap later are shown in figure 3.17. Again, an excellent agreement is achieved between the modeled and the measurement data. By comparing the gate leakage I-V profile of figures 3.16 and 3.17, we observe that the gate leakage current-voltage characteristic of InAlN/GaN HFET with InAlN cap is different from that of the InAlN/GaN HFET with AlGaN cap layer. The gate leakage current is dominated by the deep traps in the InAlN cap layer for the InAlN/GaN HFET with InAlN cap. Three distinctive regions have been observed as shown in figure 3.17 in the gate leakage I-V plot: Ohmic region; TFL region; and square law region.
Figure 3.17: Modeled versus measurement data for 1x150 µ N-polar InAIN/GaN HFET with gate drain spacing of 2 µ.
Table 3.3: Model parameters of 1x150 micron N-polar InAlN/GaN HFET with InAlN cap.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Values used to fit measurement data for 150 µ InAlN/GaN HFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>Deep Trap level E_t (eV)</td>
<td>2.41</td>
</tr>
<tr>
<td>Trap concentration at level E_t (cm⁻³)</td>
<td>1.207x10^{17}</td>
</tr>
<tr>
<td>Shallow trap level E_{t2} (eV)</td>
<td>0.30</td>
</tr>
<tr>
<td>Trap concentration at level E_{t2} (cm⁻³)</td>
<td>3x10^{12}</td>
</tr>
<tr>
<td>Shallow trap level E_{t1} (eV)</td>
<td>0.197</td>
</tr>
<tr>
<td>Trap concentration at level E_{t1} (cm⁻³)</td>
<td>6.42x10^{12}</td>
</tr>
<tr>
<td>Low field mobility (cm²/V.s)</td>
<td>450</td>
</tr>
<tr>
<td>Electron energy (eV)</td>
<td>0.2</td>
</tr>
</tbody>
</table>

For gate-drain voltage (V_{gd}) of 0-3.02 V, we observe an Ohmic region due to the thermal carrier concentration in the InAlN layer, in this region all the injected electrons from the gate electrode are captured by the deep traps. For V_{gd}> 3.02 V, the deep traps start filling up and the current abruptly increases. The injected electrons from the gate which are not captured by the deep traps accumulate in the conduction band of the InAlN cap layer and flow towards the drain electrode. The SCL conduction mechanism is affected by the first level of shallow traps at the InAlN surface. This region is called the TFL region and it approaches the square law region at V_{gd}=V_{TFL}=8.09 V. In this region all the deep traps are filled and the SCL current is dominated by the first level of shallow traps. The second level of shallow traps
start dominating the SCL current flow at $V_{gd}=8.22$ V. The extracted values of the trap level and trap concentration is given in Table 3.3. The extracted deep trap level is derived in terms of $F_o-E_t$; the Fermi level of the undoped InAlN cap layer is assumed to be at the mid gap level. The average energy of electrons used in the TAT formulation is approximated as 0.2 eV [8]. The cross-over voltages, which separate the three regions, depend on the concentration of the traps, the depth of the trap level, the material properties and dimensions of the material.

### 3.4 Conclusion

A comprehensive physics based model of the gate-leakage current in AlGaN/GaN HFETs is demonstrated for the first time. The model accurately predicts the gate-leakage current for drain voltages as high as 170 V. The model gives a complete picture of the physics of the leakage current flowing from the gate to the drain electrode in these devices. The model reveals that the gate leakage current in the GaN HFETs flows through two paths: (1) through the surface layer from the gate to the drain; and (2) from the gate, through the AlGaN layer to the 2DEG channel at the AlGaN/GaN interface. The tunneling of gate electrons to the surface and the 2DEG depends on the vertical electrical field beneath the gate region, which in turn depends on the polarization charges of the GaN HFETs. Due to the abundance of shallow traps at the gate edge of the surface layer, electrons tunnel from the gate electrode to the surface by trap-assisted tunneling mechanism. The current conduction from the gate to the drain through the surface layer occurs by space-charge limited current transport. The 0.57 eV trap level in the AlGaN layer facilitates the trap-assisted tunneling of electrons from the
gate electrode to the 2DEG channel. The current transport in the 2DEG is not affected by the space charge and is modeled using the DC $I-V$ formulation of a typical GaN HFET. Electron velocity saturates when the lateral electric field exceeds the saturation electric field value of GaN, and it drastically affects the gate leakage $I-V$ characteristics.

In the case of N-polar InAlN/GaN HFETs, the gate leakage current is modeled by considering the SCL current flow through the InAlN surface layer in the presence of deep traps. It is established from the model that in the InAlN/GaN HFETs, the gate leakage current flowing through the surface layer dominates the current flow through the 2DEG channel. In the $I-V$ profile of the gate leakage for InAlN/GaN HFETs, the leakage current abruptly increases when the deep traps in the InAlN cap layer start to fill up by the electrons tunneling from the gate electrode. The shallow traps dominate the SCL current flow when the gate-drain voltage exceeds the trap filled limit voltage. The model is entirely physical and requires minimum fitting parameters. The gate-leakage model can be integrated with an existing physics based compact GaN HFET model [27] [28] and is implemented in a commercial circuit simulator AWR Microwave Office.
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[19] Y.F. Wu, Member, A. Saxler, Member, M. Moore, Member, R. P. Smith, S. Sheppard, P. M. Chavarkar, T. Wisleder, U. K. Mishra, and P. Parikh, "30-W/mm GaN HEMTs by


Chapter 4 : Drain Current Collapse and Breakdown Simulations

4.1 Circuit Based Simulation of Drain Current Collapse Phenomenon in AlGaN/GaN HFETs

AlGaN/GaN HFETs are most suitable for high power and high frequency applications for cellular base stations, satellite and radar transmitters. However, the issues like current collapse [1] [2] [3] and dispersion effects which are mostly caused by the presence of surface traps limit the device performances and reliability and thus the commercialization of these devices have been hindered. Current collapse is very important since the device output power is limited by the current collapse phenomenon. Charging up of a virtual gate in the drain access region [2], hot electron injection and trapping in the buffer [3] are the proposed causes of current collapse. Though much effort has been put to investigate the traps in such devices the physics of the trapping mechanism has not been completely understood. Current collapse- a reduction of the dc drain current and distortion of dc current-voltage characteristic occurs due to the trapping mechanism and this is the most detrimental effect of traps in an AlGaN/GaN device. The current collapse causes the increase of the knee voltage and limits the maximum drain current. The reduction of the drain current is the reason why the output power of AlGaN/GaN device is considerably low than what is expected from the I-V characteristic. When large bias voltage is applied on the device, the surface traps in the vicinity of the gate, traps electrons which act as a negatively charged virtual gate and the
maximum current available from the device is limited by the discharging of these filled traps. The trapping of charge carriers in the traps is also reflected in gate lag – a delayed response of the modulation of source to drain current by the changing gate voltage. The reduction in the device output power effects the high frequency operation, this effect is also referred as frequency dispersion.

Figure 4.1: Virtual gate formation in AlGaN/GaN HFET due to the tunneling of electrons from the gate to the traps in the AlGaN layer.

The mechanism by which a high density distribution of surface states can cause drain current collapse and gate lag is illustrated in figure 4.1. When a negative voltage is applied at the gate a depletion region is formed beneath the gate region which extends up to the 2DEG channel when the gate voltage is close to the pinch-off voltage. However, due to tunneling of
electrons from the gate to the surface traps, the charge distribution at the surface is altered. As the traps capture the electrons tunneling from the gate, they become negatively charged; the surface charge becomes more negative and the depletion region is extended towards the drain side creating a virtual gate in the drain access region as shown in figure 4.1. Now at higher frequency, the virtual gate responds according to the time characteristics of traps which leads to delayed $I_D$ switching and hence drain current collapse.

4.1.1 Drain Current Collapse Due to Traps in the Drain Access Region

In this section, we have shown the phenomenon of drain current collapse by 2D simulation of an AlGaN/GaN HFET by incorporating additional parasitic elements in the circuit which take account of the trapping effects. The simulation is done using the Nitronex device NT351009 in Advanced Design System (ADS). The ADS schematic of the model of the trapping effect resulting in current collapse in AlGaN/GaN HFET in shown in figure 4.2.

The AlGaN layer acts as a dielectric between the surface positive charge and the 2DEG to form the capacitor $C_t$; the resistance $R_1$ accounts for the tunneling mechanism from the gate to the AlGaN surface and the resistance $R_2$ limit the flow of emitted electrons from the traps to the conduction band which in turn course to the drain end. The electrons which tunnel from the gate through the barrier in the presence of extremely high electric field are captured by the surface traps leading to a reduction of net positive charge on the surface and are then emitted from the traps to the conduction band in a certain duration which strongly depends on the tunneling and recombination time constants.
The 2DEG current is indirectly affected by the change in the surface charge; the lessening of the surface positive charge decreases the 2DEG and the drain current also mitigates; this process is modeled by the non-linear voltage controlled current source which is connected in the source access region. The circuit schematic which has been used to simulate the trapping effects in ADS is shown in figure 4.3.

The $I-V$ characteristic of the AlGaN/GaN HFET in the presence of trapping effects is determined by simulating the schematic in figure 4.3. The plot of the $I-V$ characteristic of the intrinsic device and of the device incorporating the trapping effects is shown in a single plot in figure 4.4.
Instead of a voltage controlled current source in the drain access region we simulated the device by incorporating a parasitic transistor, the circuit schematic is shown in figure 4.5; the $I-V$ characteristic of the same is shown in figure 4.6.

Figure 4.3: ADS circuit schematic for the modeling of drain current collapse in AlGaN/GaN HEMTs by incorporating non-linear voltage controlled current source (VCCS) in the drain access region.
Figure 4.4: $I$-$V$ characteristic of Nitronex AlGaN/GaN HFET model with (red) and without (blue) drain current collapse phenomenon. In the ADS schematic non-linear VCCS is incorporated in the drain access region to show the effect of drain current collapse phenomenon.
Figure 4.5: ADS circuit schematic for the modeling of drain current collapse in AlGaN/GaN HEMTs by incorporating parasitic transistor in the drain access region.
Figure 4.6: The $I$-$V$ characteristic of the intrinsic AlGaN/GaN HFET Nitronex model (blue curves). The red curve shows the drain current collapse phenomenon outputted from the simulation of schematic 4.5.

### 4.1.2 Drain Current Collapse due to Traps in the Source Access Region

Drain current collapse can also result from the trapping effects in the source access region. The electric field at the gate edge in the source access region is not significant as compared to the electric field at the gate edge in the drain access region; the traps in the source access region will play a lesser effect to the drain current collapse phenomenon than the traps in the drain access region. Connecting the non-linear voltage controlled current source (VCCS)
and parasitic transistor in the source access region, the drain current collapse phenomenon is shown.

Figure 4.7: ADS circuit schematic for the modeling of drain current collapse in AlGaN/GaN HEMTs by incorporating non-linear voltage controlled current source (VCCS) in the source access region.
Figure 4.8: $I-V$ characteristic of Nitronex AlGaN/GaN HFET model with (red) and without (blue) drain current collapse phenomenon. In the ADS schematic non-linear VCCS is incorporated in the source access region to show the effect of drain current collapse phenomenon.
The drain current collapse phenomenon in the AlGaN/GaN HFETs is shown by circuit based simulation by incorporating the effects of traps in the ADS schematic. The non-linear VCCS and the parasitic transistor reduce the current in the circuit. The Nitronex device NT351009 has inherent temperature effects in its $I-V$ characteristic. The incorporation of the trapping circuit further decreases the drain current. From the plots it is obvious that in the presence of
surface traps, the drain current is substantially reduced, the mechanism is called current collapse.

Reduction of the drain current by the current collapse phenomenon reduces the output power of the device. The traps at the gate edge in the drain side region play the significant role in the drain current collapse phenomenon by forming virtual gate in the drain access region.

![I-V characteristic of Nitronex AlGaN/GaN HFET model with (red) and without (blue) drain current collapse phenomenon. In the ADS schematic parasitic transistor is incorporated in the source access region to show the effect of drain current collapse phenomenon.](image)

Figure 4.10: I-V characteristic of Nitronex AlGaN/GaN HFET model with (red) and without (blue) drain current collapse phenomenon. In the ADS schematic parasitic transistor is incorporated in the source access region to show the effect of drain current collapse phenomenon.
4.2 TCAD Silvaco Atlas Simulation of AlGaN/GaN HFETs

TCAD simulations can help us to understand device physics and operation mechanisms. An example is ATLAS, a physically-based device simulator from Silvaco [4]. It works by the creation of an appropriate mesh and defining the simulation parameters and models. During the simulation, a set of fundamental semiconductor equations, including Poisson’s equation, continuity equations, and transport equations are solved for every grid point. Numerical simulators perform excellently in predicting the device performance. Unlike empirical models, numerical simulations can be performed before any real device is processed and fabricated and this will give an advantage in designing. The cross-section of the test device is shown in figure 4.11.

The goal of the project is the show the gate to drain spacing dependence on the breakdown voltage (BV) by performing TCAD simulation of the AlGaN/GaN HEFTs using Silvaco Atlas. The example ‘Breakdown’ deck of the Atlas simulator considers the conventional gate breakdown mechanism and so the gate to drain spacing has least impact on the breakdown voltage as the electric field at the gate edge does not vary significantly with the increasing drain voltage (see figure 3.4). The breakdown measurement data indicate the gate to drain spacing dependence on the BV.

The measurement of the DC I-V and pulsed I-V data of the AlGaN/GaN HFETs is first accomplished and then the parameters—low field, mobility, saturation velocity, and the bulk value of the single interface charge in the AlGaN/GaN interface are extracted by fitting the
TCAD simulation results with the measurement data. The breakdown simulation is then performed using the extracted parameters.

Figure 4.11: Cross-section of the TCAD structure of the device.

The DC measurement data is taken using Agilent E5270 Series of Parametric Measurement Solutions across different temperatures. To avoid the temperature effects, we have taken pulsed $I-V$ measurement using DIVA and AMCAD. The plot of the DC and pulsed $I-V$ measurement data is shown in figure 4.12. Next, the TCAD device structure is simulated for the DC characteristics and the breakdown mechanism by considering charges in the...
GaN_cap/AlGaN and the AlGaN/GaN interfaces. To analyze the interface charges and the donor concentration at the surface we performed high and low frequency offset capacitance measurement of the AlGaN/GaN HFETs and match the same with the measurement data. The TCAD structure is simulated by considering charges at the three interfaces and donor concentration at the surface to analyze the DC and the breakdown characteristics of the device.

Figure 4.12: Measured DC and pulsed I-V characteristics of 2x100 micron HFET device. At higher current levels the DC curves show a downward slope due to temperature effects.
4.2.1 Device Simulations Using Charges across Single Interface

The TCAD structure of the device is first simulated for the DC characteristics considering a single interface charge of $8 \times 10^{12} \text{ c/cm}^2$ between the AlGaN/GaN layers. In the TCAD deck, the meshes along the interfaces, surface and at the contact regions of the electrodes are concentrated to improve the accuracy of the simulation. The measurements versus the simulation plots for the transfer characteristic and the DC family of curves are shown in figures 4.13 and 4.14 respectively. In the simulation deck the threshold voltage is altered by changing the values of the following parameters: 1. Work Function of gate metal electrode: Increasing the working function will move the transfer curve to the positive $x$-axis. For a given value of interface charge, increasing the work function of the gate by 1 eV increases the threshold voltage by approximately 1 V. 2. Interface charge- Increasing the interface charge will shift the transfer curve to the negative $x$-axis. 3. AlGaN thickness/ Percentage of Al composition: Increasing the AlGaN thickness or the percentage of Al composition shifts the transfer curve to the negative $x$-axis since with the increase of the AlGaN thickness or the Al composition the amount of the polarization induced interface charges increases. Decreasing the Al composition decreases the saturation region of the transfer curve. The R-ON can be altered by changing the mobility models. In the linear region of the $I-V$ plot, carrier velocity is given by $v=\mu E$. Increasing the mobility will raise the carrier velocity which in turn increases R-ON. In the current fit, Farahmand Modified Caughey Thomas (FMCT) and GaNsat Silvaco Atlas mobility models are used.
Figure 4.13: Measured and simulated DC transfer curves of 2x100 micron HFET considering single interface charge at AlGaN/GaN interface in the TCAD simulation deck.

FMCT is a composition and temperature dependent low field model. Figure 4.15 shows the velocity versus the doing concentration of the FMCT mobility model with the default and modified parameter values. This model is described by the equation \[4\]:

\[
\mu(T, N) = MUN_{FMCT} \left(\frac{T}{300}\right)^{BETAN_{FMCT}} + \frac{(MU2N_{FMCT} - MUN_{FMCT}) \left(\frac{T}{300}\right)^{DELTAN_{FMCT}}}{1 + \left(\frac{N}{NCRITN_{FMCT} \left(\frac{T}{300}\right)^{GAMMAN_{FMCT}}}ight)^{ALPHAN_{FMCT} \left(\frac{T}{300}\right)^{DELTAN_{FMCT}}}}
\]  

4.1
Figure 4.14: Measured and simulated DC family of curves of 2x100 micron HFET considering single interface charge at AlGaN/GaN interface in the TCAD simulation deck.

Table 4.1: FMCT mobility model default and modified parameter values.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Default values</th>
<th>Modified values</th>
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<tbody>
<tr>
<td>MU1N.FMCT</td>
<td>295</td>
<td>1000</td>
</tr>
<tr>
<td>BETAN.FMCT</td>
<td>-1.02</td>
<td>-1.02</td>
</tr>
<tr>
<td>MU2N.FMCT</td>
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<td>2500</td>
</tr>
<tr>
<td>DELTAN.FMCT</td>
<td>3.02</td>
<td>3.02</td>
</tr>
<tr>
<td>NCRITN.FMCT</td>
<td>1.00E17</td>
<td>1.00E22</td>
</tr>
<tr>
<td>GAMMAN.FMCT</td>
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<td>-3.84</td>
</tr>
<tr>
<td>ALPHAN.FMCT</td>
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<td>1.001</td>
</tr>
<tr>
<td>EPSP.FMCT</td>
<td>0.81</td>
<td>0.81</td>
</tr>
</tbody>
</table>
Figure 4.15: Velocity versus doping concentration for default (blue curve) and modified (red curve) FMCT mobility model parameters.

High field GANSAT Silvaco Atlas mobility model is a nitride specific field dependent mobility model is selected by specifying GANSAT.N and GANSAT.P on the MOBILITY statement in the TCAD deck. The model is described by the equation [4]:

\[
\mu_n = \frac{\mu_n_0(T, N) + VSAT_N \cdot E^{N1N.GANSAT-1}}{1 + ANN.GANSAT \left( \frac{E}{ECN.GANSAT} \right)^{N2N.GANSAT} + \left( \frac{E}{ECN.GANSAT} \right)^{N1N.GANSAT}}
\]
Table 4.2: GaNsat mobility model default parameter list.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Default value</th>
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</thead>
<tbody>
<tr>
<td>VSATN</td>
<td>1.9064e7</td>
</tr>
<tr>
<td>ECN.GANSAT</td>
<td>220.8936</td>
</tr>
<tr>
<td>N1N.GANSAT</td>
<td>7.2044</td>
</tr>
<tr>
<td>N2N.GANSAT</td>
<td>0.7857</td>
</tr>
<tr>
<td>ANN.GANSAT</td>
<td>6.1973</td>
</tr>
</tbody>
</table>

Figure 4.16: GaNsat mobility model velocity versus electric field for default parameter values.

The velocity versus the electric field for the mobility models used in the simulation is shown in figure 4.17 which is in consistent with the published data.
Figure 4.17: Electron velocity versus electric field of the TCAD simulated AlGaN/GaN device.

The breakdown simulation is performed using the single interface charge at the AlGaN/GaN interface. The breakdown plot for the devices with gate to drain spacing, Lgd=5 and 19 microns are shown in the figure 4.18. The Lgd dependence on the breakdown voltage is not achieved using single interface charge. This is because the extremely high vertical electrical between the gate and the 2DEG clamps the depletion width at the gate edge as shown in figure 4.19. The impact ionization is triggered in the region beneath the gate edge because of the high vertical electric field and instead of channel breakdown, we observe a gate breakdown in the simulation of the device using a single interface charge as shown in figure 4.20.
Figure 4.18: Breakdown plot for the simulated device structures for Lgd of 5 and 19 microns considering single interface charge of 2x100 micron AlGaN/GaN HFETs.

Figure 4.19: Potential lines across the cross-section of the simulated structure for single interface charge.
4.2.2 Device Simulations Using Charges across Two Interfaces

To achieve the \( L_{gd} \) dependence on the breakdown voltage, the depletion region at the gate edge must be spread laterally towards the drain end and this can be achieved by decreasing the vertical electric field between the top surface layer and the 2DEG by the incorporation of a negative charge at the GaNcap/AlGaN interface as shown in figure 4.21. The TCAD simulated vertical electric field versus the gate to drain spacing of AlGaN/GaN HFETs is shown in figure 4.22 for single and double interface charges. In the simulation results using double interface charge, a much reduced vertical electric field is observed.
Figure 4.21: Cross-section of the simulated TCAD device structure showing the double interface charges.

Figure 4.22: Vertical electric field versus the gate-drain spacing for the simulated device.
Two interfaces charges of magnitude of $-3.2 \times 10^{12} \text{ c/cm}^2$ and $6.6 \times 10^{12} \text{ c/cm}^2$ are applied in the GaNcap/AlGaN and AlGaN/GaN interfaces respectively. The magnitude of the charges is determined by fitting the DC simulated results with the measurement data. The breakdown plots for the devices with $L_{gd}=5$, 10 and 19 microns are shown in figure 4.24. Although we achieve $L_{gd}$ dependence on the breakdown mechanism, the breakdown voltages for the devices with $L_{gd}=10$ and 19 microns are the same. This indicates that the depletion region is not spread far enough from the gate edge as verified in figure 4.23.

![Depletion region ends](image)

Figure 4.23: Potential lines across the cross-section of the simulated structure for double interface charges.
Figure 4.24: Breakdown plot for the simulated device structures for Lgd of 5, 10 and 19 microns considering double interface charges of 2x100 micron AlGaN/GaN HFETs.

The gate to drain spacing (Lgd) dependence on the breakdown voltage is achieved by the incorporation of the negative interface charge at the GaNcap/AlGaN interface which reduces the net electric field between the gate and the 2DEG thus increasing the depletion width. The simulated DC transfer curve versus the measured data is shown in figure 4.25. Figure 4.26 shows the modeled versus the measured DC family of curves. Pulsed DC measured data are compared with the simulated data in figure 4.27.
Figure 4.25: Measured and simulated DC transfer curves of 2x100 micron HFET considering charges at the two interfaces in the TCAD simulation deck.

Figure 4.26: Measured and simulated DC family of curves of 2x100 micron HFET considering charges at the two interfaces in the TCAD simulation deck.
Figure 4.27: Simulated family of curves versus pulsed $I$-$V$ measurement of 2x100 micron HFET considering charges at the two interfaces in the TCAD simulation deck.

4.2.3 Device Simulations Using Charges across Three Interfaces

In a real device, charges exist at all the three interfaces as shown in figure 4.28. According to the polarization model, a negative charge of $6 \times 10^{12}$ c/cm$^2$ exists at the surface of the GaNcap if we assume a charge of $8 \times 10^{12}$ c/cm$^2$ and $-8 \times 10^{12}$ c/cm$^2$ at the AlGaN/GaN and GaNcap/AlGaN interfaces respectively. But normally the surface is full of dislocations and traps. So, the exact amount of charge in the surface layer cannot be clarified. The donor-like surface states at $E_D$ eV below the conduction band of the GaNcap layer are present in the device and if the energy levels of the surface states are above the Fermi level, the electrons are emptied from the surface states and transferred to the 2DEG channel, while the surface
states themselves become positively charges. We used a charge of \(-2 \times 10^{12} \text{c/cm}^2\) and a donor concentration of \(8 \times 10^{12} \text{cm}^{-2}\) at the surface of the GaNcap to fit the measured data. Fixed charges of \(-8 \times 10^{12} \text{c/cm}^2\) and \(8 \times 10^{12} \text{c/cm}^2\) are incorporated at the GaNcap/AlGaN and AlGaN/GaN interfaces respectively.

Figure 4.28: Interface charges and surface donors in AlGaN/GaN HFETs.

The interface charges and the surface donor concentration are verified by matching the simulated and the measurement capacitance data as the offset capacitances significantly depend on the charges in the device. The device output characteristics especially the breakdown characteristic is highly dependent on the charges in the drain access region. Gate-drain capacitance is the most critical parameter used to interpret the interface charges in the device. The high frequency (~GHz) capacitance data are extracted from the S-parameters.
using Agilent E5270 and PNA-X Network Analyzer N5242A. To measure the low frequency (~MHz) capacitance data, a new measurement procedure is setup to measure the capacitance of the three terminal HFETs with the two terminal LCR meter Agilent E4890A interfaced with ICCAP shown in figure 4.34. We applied voltage at the third terminal externally. The capacitance of AlGaN/GaN devices having different source field plate (SFP) and gate field plate (GFP) lengths are measured and the data from both the high frequency and low frequency measurement setups are compared as shown in figures 4.29 - 4.33.

![Graph](image.png)

Figure 4.29: Gate to drain capacitance measurement data for 1x25 micron AlGaN/GaN HFET, L_{gd}=19\mu. Red curve indicates the high frequency ~13GHz measurement data. Green curve indicates the low frequency ~30MHz measurement data. Gate voltage is kept fixed at -10V.
Figure 4.30: Gate to drain capacitance measurement data for 1x50 micron AlGaN/GaN HFET, $L_{gd}=19\mu$. Red curve indicates the high frequency ~13GHz measurement data. Blue curve indicates the low frequency ~30MHz measurement data. Gate voltage is kept fixed at -5V.

The peak value of the gate to drain capacitance, $(C_{gd})$ at $V_{drain}=0$ increases with increasing gate field plate length as shown in figure 4.31. This is because the charge content beneath the GFP region increases with the GFP length. Source to gate capacitance $(C_{gs})$ increases with increasing SFP length but $C_{gd}$ (slightly) decreases with increasing source field plate length shown in figures 4.32 and 4.33.
Figure 4.31: Gate to drain capacitance measurement data for 2x100 micron AlGaN/GaN HFET, for different GFP lengths, $L_{gd}=19\mu$. Gate voltage is kept fixed at -5V.

Figure 4.32: Gate to drain capacitance measurement data for 2x100 micron AlGaN/GaN HFET, for different SFP lengths, $L_{gd}=19\mu$. Gate voltage is kept fixed at -5V.
Figure 4.33: Gate to Source capacitance measurement data for 2x100 micron AlGaN/GaN HFET, for different SFP lengths, $L_{gd}=19\mu$. Gate voltage is kept fixed at -5V.

Figure 4.34: Cartoon of the measurement set up for the low frequency gate to drain capacitance measurement of AlGaN/GaN HFET using Agilent E4890A interfaced with ICCAP.
The simulated versus the measured gate-drain capacitance ($C_{gd}$) for different combination of charges are shown in figure 4.35. We achieved the best modeled versus the measured $C_{gd}$ fit for a surface charge of $5 \times 10^{12}$ c/cm$^2$, and interface charges of $-1 \times 10^{13}$ c/cm$^2$ and $1.15 \times 10^{13}$ c/cm$^2$ at the GaNcap/AlGaN and AlGaN/GaN interfaces respectively. But for the same combination of charge the $L_{gd}$ dependence on the breakdown voltage is not achieved. We achieve $L_{gd}$ dependence on the breakdown voltage for a combination of a fixed charge of $-2 \times 10^{12}$ c/cm$^2$ and a donor concentration of $8 \times 10^{12}$ cm$^{-2}$ at the surface of the GaNcap and fixed charges of $-8 \times 10^{12}$ c/cm$^2$ and $8 \times 10^{12}$ c/cm$^2$ at the GaNcap/AlGaN and AlGaN/GaN interfaces respectively. The modeled versus the measured DC characteristics are shown in the figures 4.36 and 4.37.

The breakdown plots for devices with $L_{gd}=5$, 10, 15 and 19 microns are shown in figure 4.38. The gate-drain spacing dependence on the breakdown voltage is achieved. The simulated breakdown voltages for devices with $L_{gd}= 5$, 10, 15 and 19 microns are 1800, 3500, 4500 and 6100 V respectively. In the breakdown curve of the device with $L_{gd}=19$, only three fixed charges have been considered and the donor concentration at the surface is not taken into consideration because of convergence issues in simulation. Although we achieve gate-drain spacing dependence on the breakdown voltage, the simulated breakdown voltages are much higher than the measured data. The impact ionizations parameters are required to be altered to match the simulated breakdown voltage to the measurement data.
Figure 4.35: C_{gd} versus drain voltage for different combination of fixed charges and surface donors for 2x100 micron AlGaN/GaN HFET, L_{gd}=19\mu.

Since the GaN cap over the AlGaN layer is only 30Å thick (<50 Å), and the surface is full of dislocations and traps, the redistribution of polarization charges at its two interfaces may not accede to the theoretical prediction. As the GaNcap is very thin (30 Å), the high negative charge (-8x10^{12} \text{c/cm}^2) at the GaNcap/AlGaN interface and the negative fixed charge at the surface of the GaNcap can be considered as a single interface charge. The measured gate-drain capacitance fits well with the modeled data if the negative charge at the surface of the GaNcap and the charge at the GaNcap/AlGaN interface are combined as single interface charge.
Figure 4.36: Measured and simulated DC transfer curves of 2x100 micron HFET considering charges at the three interfaces and surface donor concentration in the TCAD simulation deck.
Figure 4.37: Measured and simulated DC family of curves of 2x100 micron HFET considering charges at the three interfaces and surface donor concentration in the TCAD simulation deck.
Figure 4.38: Breakdown plot for the simulated device structures for Lgd of 5, 10, 15 and 19 microns considering triple interface charges and donor concentration of 2x10^0 micron AlGaN/GaN HFETs.
4.2.4 Device Simulations Using Charges across Two Interfaces and Incorporating Donors Traps at Surface

In this section, only the donor concentration of $8.7 \times 10^{12} \text{ cm}^{-2}$ at the surface of the GaNcap is considered. Fixed charges of $-8 \times 10^{12} \text{ c/cm}^2$ and $8 \times 10^{12} \text{ c/cm}^2$ are placed at the GaNcap/AlGaN and AlGaN/GaN interfaces respectively. Ignoring the surface negative charge makes the simulating device structure simpler and helps avoiding convergence issues.

The modeled versus the measured gate-drain capacitance versus gate-drain voltage for surface donor concentration of $8.7 \times 10^{12} \text{ c/cm}^2$ and interface charges of $-8 \times 10^{12} \text{ c/cm}^2$ and $8 \times 10^{12} \text{ c/cm}^2$ is shown in figure 4.39. We achieved a better fit of the hump in the capacitance curve by altering the GFP height within the process variation tolerance.
Figure 4.39: Comparison of modeled (red curve) and measured (green curve) gate-drain capacitance of 2x100 micron AlGaN/GaN HFET for double interface charges and surface donor concentration.

The Lgd dependence on the breakdown is achieved and shown in the figure 4.40. The breakdown current is in the range of 50mA/mm. From the figure we observe that the breakdown voltages of the devices with Lgd of 5, 10, 15 and 19 microns are 1500, 3500, 4900 and 5900 V respectively. The breakdown voltages are higher than the measured data. But if we set the breakdown current as $1 \times 10^8$ A/mm, we observe a much lower breakdown voltage for the same device structure. We observe a breakdown voltage of 2300 V for the device with Lgd=10 microns as shown in the figure 4.41. The comparison of the simulated
transfer curve and family of curves by considering charges at the two interfaces and surface donor concentration with the measurement data is shown in figure 4.42 and 4.43.

Figure 4.40: Breakdown plot of the simulated device structures for Lgd of 5, 10, 15 and 19 microns considering double interface charges and donor concentration of 2x100 micron AlGaN/GaN HFETs.
Figure 4.41: Breakdown plot of 2x100 micron device with Lgd=10 microns. Breakdown current is limited to $3.5 \times 10^{-8}$ A/mm.
Figure 4.42: Measured and simulated DC transfer curves of 2x100 micron HFET considering charges at the three interfaces and surface donor concentration in the TCAD simulation deck.
Figure 4.43: Measured and simulated DC family of curves of 2x100 micron HFET considering charges at the two interfaces and surface donor concentration in the TCAD simulation deck.

The gate to drain spacing dependence on the breakdown voltage is achieved by considering channel breakdown in the AlGaN/GaN HFETs. Impact ionization is triggered in the channel in the drain access region which results in the device breakdown. The TCAD example deck considers single interface charge which results in a smaller depletion width in which the maximum voltage drop occurs and hence the electric field is concentrated in the channel region at the gate edge. Due to the existence of the strong electric field in a very small region
in the channel at the gate edge, impact ionization triggers resulting in gate breakdown mechanism and the gate to drain spacing does not impact the gate breakdown voltage. By considering the charges across two interfaces and donor concentration at the surface of the device, the depletion region is extended in the drain access region which results in the spreading of the electric field from the gate edge along the channel. The breakdown down simulation of the device structure considering charges at the various interfaces and donor concentration at the surface verifies the gate to drain dependence on the breakdown voltage as indicated by the breakdown measurement data.
REFERENCES


Chapter 5 : Conclusion
“Nature works in mysterious ways”

A new comprehensive physics based model of the gate leakage current in nitride-based HFETs is demonstrated and used to explain leakage currents in these devices when under high field operation. The gate leakage model is formulated by considering, for the first time, two paths for the leakage current flow- surface and 2DEG. Trap assisted tunneling mechanism is considered for the evaluation of the electrons tunneling from the Schottky gate contact to the 2DEG channel. In AlGaN/GaN HFETs, the gate leakage current flowing through the surface is evaluated by considering the effects of shallow traps on the space charge limited current flow from the gate to the drain end. The model accurately predicts the gate leakage measurement data of AlGaN/GaN devices for gate-drain voltage in the range of 0-170 V. In the gate leakage I-V characteristics, three distinctive regions are observed: (1) low field region, (2) high-field region, and (3) velocity saturation region. In the low field region, the SCL current flowing through the surface is proportional to the squared of the voltage and the current flowing through the 2DEG is linearly proportional to the gate-drain voltage. In the high field region, the lateral electric field approaches the magnitude of the saturation electric field, the SCL current through the surface is a function of 3/2 power of the gate-drain voltage. When the magnitude of the lateral electric field exceeds the saturation electric field value, the electron velocity saturates both at the surface and at the 2DEG channel, the current flowing through the surface is linearly proportional to the voltage in the
velocity saturation region. The model is used to explain the gate leakage measurement data of AlGaN/GaN HFET at 150°C by considering the surface current flowing both through the GaN cap and the AlGaN layers. In the case of N-polar InAlN/GaN HFET, the SCL current in the drain access region is dominated by the presence of deep traps in the InAlN cap. In the $I-V$ profile of the gate leakage for InAlN/GaN HFETs, the leakage current abruptly increases when the deep traps in the InAlN cap layer start to fill up by the electrons tunneling from the gate electrode. The shallow traps dominate the SCL current flow when the gate-drain voltage exceeds the trap filled limit voltage. The model accurately explains the gate leakage measurement data of InAlN/GaN HFETs.

The circuit based modeling of the drain current collapse phenomenon due to the surface traps in AlGaN/GaN HFETs using Advanced Design System is explained in Chapter 4. In the last section of the thesis, the gate to drain spacing dependence on the breakdown voltage of AlGaN/GaN HFETs is explained by TCAD simulations.

5.1. Future Work

In the gate leakage model, the surface conduction mechanism between the gate and the drain electrodes is dominated by the SCL current flow through the conduction band of the surface layer in presence of traps. The $I-V$ characteristic of the gate leakage measurement data verifies the existence of SCL current conduction. However, there are a lot of other mechanisms which affect the gate leakage current flow in GaN based devices. In the presence of shallow donor states, at room temperature, the electrons are excited to the
conduction band which results in the current flow in a semiconductor. At low temperatures, however, the electron is still bound to its atom and if the trap density is high the wave functions of these electrons overlap because of the closer spacing of the impurities. The discrete levels of the donor electrons then become bands which broaden with increased donor densities and merges with the conduction band [1]. This merging of the bands in semiconductor then eliminates the activation energy previously needed for conduction and results in increase in current flow at low temperature. But in the case of GaN HFETs, the semiconductors are normally undoped which expunges the impurity band conduction theory. However, the presence of impurity compensation leads to a trap to trap hopping mechanism which might be the dominant gate leakage current mechanism at low temperature. The deep acceptor type impurities may provide compensation to which some of the donors lose their electrons and become ionized. This will lead to a conduction mechanism in which electron hopping occurs from neutral to ionized donors. At high electric field, the current flow due to electron hopping mechanism becomes large because the field-enhanced thermal emission of charge carriers from Coulombic traps by the Poole-Frenkel effect [2]. It is experimentally observed that the ac impurity conductivity due to hopping mechanism is appreciably higher than the dc conductivity [3]. The impurity conductivity is a function of the squared of the frequency for frequencies between $10^2$ and $10^5$ Hz and temperatures between 1 and 20°K. To determine the gate leakage conduction mechanism in the GaN based devices, a two terminal conductivity measurement between the gate and the drain electrodes can be designed to analyze the ac conductivity of the drain access region of GaN HFETs at low temperatures. If the ac impurity conductivity of the drain access region of GaN HFETs at low temperatures is
a function of the squared of the voltage, then the existence of trap to trap hopping mechanism can be verified and in the gate leakage model the electron hopping mechanism which plays the dominant role at low temperatures can be incorporated. However, the GaN HFETs are normally not operated at such low temperatures. So, ignoring the electron hopping mechanism will not significantly affect the accuracy or predictability of the gate leakage model.

In the gate leakage model of GaN HFETs, an analytical formulation of traps assisted tunneling mechanism is used to evaluate the tunneling of carrier injection from the gate to the 2DEG channel. The space charge and interface charges which might affect the tunneling mechanism are not considered in the TAT formulation. The effect of free space charge with no traps and space charge with traps on the conventional Fowler-Nordheim tunneling mechanism for the case of very low free carrier mobility in an insulator is elucidated in [4]. The space charge in the presence of high density of traps appreciably limits the tunneling current density. Space charge resists the tunnel emission of new charge carriers from the metal. The variation of the tunneling contact resistance with different amount of interface charges is studied in [5]. The effects of the interface charges due to the polarization effects in GaN HFETs and the space charge in the surface layer at the gate edge drain side on the TAT mechanism should be analyzed to improve the tunneling model in the gate leakage formulation.
The breakdown measurement data shows that the breakdown voltage of AlGaN/GaN HFETs increases with increasing gate to drain spacing. The gate to drain spacing dependence on the breakdown voltage is successfully simulated by considering channel breakdown mechanism using TCAD Silvaco Atlas. The gate leakage current analysis of GaN HFETs reveals the conduction path through the surface of the device dominated by space charge effects in the presence of traps. The initiation of the breakdown mechanism at the surface of the device which can also cause the gate to drain spacing dependence on the breakdown voltage of AlGaN/GaN HFETs should be analyzed extensively.
REFERENCES


Appendix A: Maple Code

A1: Maple Code to Determine the Gate Leakage Current of GaN HFETs

> restart;

#Parameter Values

\[ u := 7.5 \times 10^{-2} : \text{eps} := 4.737 \times 10^{-11} : q := 1.6 \times 10^{-19} : K := 8.615 \times 10^{-5} : t \]
\[ := 300 : \text{no} := 5 \times 10^{10} : L := 19 \times 10^{-6} : g := 1 : \text{vsat} := 2.9 \times 10^4 : E1 \]
\[ := 3.0e3 : \text{Nc} := 2.234e24 : \text{EA} := 0.0193 : E1B \]
\[ := 0.52852463591 : \text{EtC} := 0.33659706907 : \text{NtA} := 5 \times 10^3 : \text{NtB} \]
\[ := 5.8453e15 : \text{Nc} := 1.306491e23 : \text{Area} := (30 \times 10^{-10}) \cdot 200 \times 10^{-6} : \text{factor5} := 0.8999537321338 : E2 := 1 \times 10^7 \]

with(plots):

#Shallow Traps

\[ NC := \text{Nc} \cdot \exp \left( \frac{-E1C}{K \cdot T} \right) ; \]
\[ NB := \text{Nc} \cdot \exp \left( \frac{-E1B}{K \cdot T} \right) ; \]
\[ NA := \text{Nc} \cdot \exp \left( \frac{-E1A}{K \cdot T} \right) ; \]
\[ A := \frac{1}{1 + g \cdot NtA} ; B := \frac{1}{1 + g \cdot NtB} ; C \]
\[ := \frac{1}{1 + g \cdot NtC} \cdot \text{Nc} \]

#Cross-over Voltages

\[ V3 := \frac{4 \cdot q \cdot \text{no} \cdot L^2}{3 \cdot \text{eps} \cdot B} ; \]
\[ Jcr2 := \left( \frac{3 \cdot q \cdot \frac{1}{2} \cdot u \cdot NB}{2 \cdot \text{eps} \cdot C \cdot E1 \cdot g} \right)^2 ; \]
\[ Vcr2 := \frac{2}{5} ; \]
\[ \frac{5 \cdot \text{eps} \cdot C \cdot E1 \cdot g^2 \cdot Jcr2}{3 \cdot \text{eps}^2 \cdot C \cdot E1 \cdot g^2 \cdot \text{w}^2} ; \]
\[ Vcr1 := \frac{1}{2} \left( \frac{q \cdot NC \cdot E1 \cdot u}{\text{eps} \cdot A \cdot \text{vsat} \cdot g} \right)^2 \cdot L^2 ; \]

#Solve Differential Equations to Determine Current Density

\[ \text{sigma} := \text{solve} \left( \frac{-J \cdot L}{q \cdot u \cdot \text{no}} - \frac{\text{eps} \cdot J^2 \cdot B}{6 \cdot q^3 \cdot u^2 \cdot \text{no}^3} - V = 0, J \right) ; \]
\[ \text{psi} := \text{op}(2, [\text{sigma}]) ; \]
alpha := solve\left(\frac{2\cdot J}{3\cdot L^2} \cdot \left(\frac{J}{u \cdot \epsilon \cdot \nu \cdot B}\right)^\frac{1}{2} - V = 0, J\right);

beta := op(1, [alpha]);

\text{goma} := solve\left(\frac{2 \cdot \epsilon \cdot \nu \cdot \mu \cdot E \cdot I \cdot u}{5 \cdot J} \cdot \left(\frac{3 \cdot J \cdot L}{2 \cdot \epsilon \cdot \nu \cdot \mu \cdot E \cdot I \cdot u}\right)^\frac{5}{3} - V = 0, J\right);

\text{lamba} := op(1, [gama]);

\text{rama} := \frac{2 \cdot \epsilon \cdot \nu \cdot \mu \cdot V \cdot A}{L^2};

\#Piecewise Relationship of Gate-Drain Current and Voltage

\text{J} := \text{piecewise}\left(V < V_{Th}, \text{psi} \cdot \text{Area}, V < V_{Th} / 2, \text{beta} \cdot \text{Area} + J_{\text{nanlin}}, V < V_{Th} / 2, \text{lamda} \cdot \text{Area} + J_{\text{nanlin}}, \text{rama} \cdot \text{Area} + J_{\text{nanlin}}\right);

\begin{align*}
&1.03636096 \times 10^{-33} - 6.545280606 \times 10^{-33} \sqrt{2.506944443 \times 10^{18} - 9.166910272 \times 10^{24} V} \quad V < 2.430911429 \times 10^{-7} \\
&1.16913922 \times 10^{-10} \cdot p^2 + 1.010526316 \times 10^{-9} V \quad V < 71.056619808 \\
&2.20030583 \times 10^{12} \cdot p^{3/2} + \frac{1.34421053 \times 10^{10} V}{(1 + 0.00038866404070 \cdot p^{0.199035721338})^{1.01198235}} \quad V < 124.1520858 \\
&3.101592589 \times 10^{-9} V + 5.7600010^{-7} \quad \text{otherwise}
\end{align*}
A2: Maple Code to Determine the Injected Carrier Concentration by the Trap Assisted Tunneling Mechanism in GaN HFETs

> restart;

\[ q := 1.6 \times 10^{-19} : F := 0.2 : \psi := 2.41 : \psi l := 0.3 : heV \]
\[ := 6.582e-16 : kJ := 1.054571726e-34 : m \]
\[ := 9.10938291e-31 : mg := 0.2291.10938291e-31 : Nl \]
\[ := 1.207e23 : Nl1 := 3.0e18 : V := 10 : d := 120e-10 : dl \]
\[ := 30e-10 : K := 1.38e-23 : T := 300 : with(pplots) : \]

\[ A := \frac{4 \cdot \sqrt{2 \cdot q \cdot m}}{3 \cdot hJ} ; C := \left( \frac{mg}{m} \right)^{\frac{3}{2}} \cdot \left( \frac{8 \cdot F^{\frac{3}{2}}}{3 \cdot heV \cdot \sqrt{\psi l - F}} \right) ; Cl \]

\[ := \left( \frac{mg}{m} \right)^{\frac{3}{2}} \cdot \left( \frac{8 \cdot F^{\frac{3}{2}}}{3 \cdot heV \cdot \sqrt{\psi l - F}} \right) ; \]

> \[ Y := \frac{3}{2} \cdot y^{\frac{1}{2}} \cdot A ; p2 := \exp \left( -\frac{A \cdot y^{\frac{3}{2}}}{E} \right) ; xl := \frac{E \cdot d - \psi l}{q} \; ; Yl \]
\[ := \frac{3}{2} \cdot \psi l^{\frac{1}{2}} \cdot A ; p2l := \exp \left( -\frac{A \cdot \psi l^{\frac{3}{2}}}{E} \right) ; xll \]
\[ := \frac{(E \cdot dl - \psi l)}{E} ; \]

\#Tunneling Current Density

> \[ J := \frac{C \cdot q \cdot Nl}{Y} \cdot p2 \cdot \left( Y \cdot xl - \ln \left( \frac{(1 + p2 \cdot \exp(Y \cdot xl))}{1 + p2} \right) \right) ; \]

\#Tunneling Carrier Concentration

\[ n := \frac{J}{q \cdot \sqrt{\frac{K \cdot T}{2 \cdot \pi \cdot m}}} ; \]
A3: Verilog-A Code to Determine the Gate Leakage Current of GaN HFETs Implemented in

AWR Microwave Office

`include "disciplines.h"
`include "constants.h"

module Gate_Leakage (a,b);
inout a,b;
electrical a,b;

parameter real u=7.5e-2 from (0:inf);
parameter real eps=4.737e-11 from (0:inf);
parameter real q=1.6e-19 from (0:inf);
parameter real K=8.61e-5 from (0:inf);
parameter real T=300 from (0:inf);
parameter real no=5e10 from (0:inf);
parameter real L=19e-6 from (0:inf);
parameter real g=1 from (0:inf);
parameter real vsat=2.9e4 from (0:inf);
parameter real E1=3e3 from (0:inf);
parameter real N3=2.234e24 from (0:inf);
parameter real EtA=0.0193 from (0:inf);
parameter real EtB=0.5284246 from (0:inf);
parameter real EtC=0.336597 from (0:inf);
parameter real NtA=5e23 from (0:inf);
parameter real NtB=5.8453e15 from (0:inf);
parameter real NtC=1.306491e23 from (0:inf);
parameter real W=200e-6 from (0:inf);
parameter real h=30e-10 from (0:inf);
parameter real h_2DEG=1e-10 from (0:inf);
parameter real beta=0.8999 from (0:inf);
parameter real E2=1e7 from (0:inf);
parameter real u_2DEG=0.12 from (0:inf);
parameter real vsat_2DEG=3e5 from (0:inf);

// Tunneling carrier density determined from TCAD and Maple simulations
parameter real ns_low="a" from (0:inf);
parameter real ns_high="b" from (0:inf);
parameter real ns_sat="c" from (0:inf);

real NA,NB,NC;
real A,B,C;
real Vcr1, Vcr2, Jcr2, V3;

analog begin

NA = N3 * exp(-EtA/(K*T));
NB = N3 * exp(-EtB/(K*T));
NC = N3 * exp(-EtC/(K*T));
A = 1/(1 + g*NtA/NA);
B = 1/(1 + g*NtB/NB);
C = 1/(1 + g*NtC/NC);

V3 = 4*q*no*pow(L,2)/((3*eps*B);
Vcr2 = 1.35*pow(q*NB/(eps*C*E1*g),2)*pow(L,3);
Vcr1 = pow(L,3)*pow((q*NC*E1*u/(eps*A*vsat*g)),2)/2;

// If Begin
if (V(a,b) < Vcr2) begin
  I(a,b) <+ W*h*9*pow(V(a,b),2)*u*eps*B/(8*pow(L,3)) + W*h_2DEG*q*ns_low*u_2DEG*V(a,b)/L;
end
else if (V(a,b) < Vcr1) begin
  I(a,b) <+ W*h*5*7.74596*pow(V(a,b),3/2)*eps*C*E1*u/(27*L) + W*h_2DEG*q*ns_high*u_2DEG*V(a,b)/(L*pow((1+pow(V(a,b)/(E2*L),beta)),1/beta));
end
else
  I(a,b) <+ W*h*2*eps*vsat*V(a,b)*A/pow(L,2) + W*h_2DEG*q*ns_sat*vsat_2DEG;
end
endmodule
Appendix B: TCAD Silvaco Atlas Code

B1: TCAD Code to Simulate AC and DC Characteristics of N-polar InAlN/GaN HFETs

go atlas

#InAlN composition
set InAlNcomp= 0.825
#AlN composition
set AlNcomp=0.30
#AlGaN composition
set AlGaNcomp=0.30
#
#Set Polarization N face =-0.1
#set po=-1.0
#
#Set Device Dimensions
set AirT=0.74
set N1T=0.03
set InAlNcapT=0.002
set GaNT=0.010
set AlINT=0.0005
set InAlNT=0.0075
set AlGaNT=0.010
set AlGaNT2=0.020
set GaNT2=0.0085
#----------------------------------------
set SDL=0.15
set SGspac=0.125
set GateL=0.15
set GFPl=0.075
set GFPr=0.075
set SFP=0.1
set GDspac=0.225
set SFP_Dspac=$GDspac-$SFP-$GFPr
#
#set Mesh Parameters
set super_finer=0.001
set super_fine=0.005
set finer=0.03
set fine=0.07
set coarse_fine=0.1
set coarse=0.9
set more_coarse=1.5

#--------------------------------------
#Create Mesh (x)
x.mesh loc=-(SDL+$SGspac) spac=$coarse_fine
x.mesh loc=-(SDL*0.5+$SGspac) spac=$fine
x.mesh loc=-$SGspac spac=$finer
#x.mesh loc=-(SDL*0.5+$SGspac) spac=$coarse_fine
#x.mesh loc=-$SGspac*0.5 spac=$fine
#x.mesh loc=-$SGspac spac=$super_finer
x.mesh loc=-$GFPI-($SGspac-$GFPI)/2 spac=$coarse_fine
x.mesh loc=-$GFPI spac=$fine
x.mesh loc=-$GFPI/2 spac=$fine
x.mesh loc=0 spac=$finer
x.mesh loc=$GateL*0.5 spac=$finer
x.mesh loc=$GateL spac=$super_finer
x.mesh loc=$GateL+$GFPr/3 spac=$super_fine
x.mesh loc=$GateL+0.5*$GFPr spac=$finer
x.mesh loc=$GateL+0.55*$GFPr spac=$finer
x.mesh loc=$GateL+0.6*$GFPr spac=$finer
x.mesh loc=$GateL+$GFPr*2/3 spac=$finer
x.mesh loc=$GateL+$GFPr*3/4 spac=$finer
x.mesh loc=$GateL+$GFPr*4/5 spac=$finer
x.mesh loc=$GateL+$GFPr*6/7 spac=$finer
x.mesh loc=$GateL+$GFPr*8/9 spac=$super_fine
x.mesh loc=$GateL+$GFPr+($GDspac-$GFPr)/8 spac=$fine
x.mesh loc=$GateL+$GFPr+($GDspac-$GFPr)/6 spac=$coarse_fine
x.mesh loc=$GateL+$GFPr+($GDspac-$GFPr)/3 spac=$coarse_fine
x.mesh loc=$GateL+$GFPr+($GDspac-$GFPr)/2 spac=$coarse
x.mesh loc=$GateL+$GFPr+($GDspac-$GFPr)/1.5 spac=$coarse
x.mesh loc=$GateL+$GFPr+($GDspac-$GFPr)/1.2 spac=$coarse_fine
x.mesh loc=$GateL+$GDspac spac=$super_fine
x.mesh loc=$GateL+$GDspac +$SDL*0.5 spac=$fine
x.mesh loc=$GateL+$GDspac +$SDL spac=$coarse_fine

#--------------------------------------
#Create Mesh (y)

y.mesh loc=-$AirT spac=$more_coarse 
y.mesh loc=-$AirT*0.25 spac=$coarse 
y.mesh loc=-$AirT/2 spac=$coarse_fine 
y.mesh loc=-$AirT*0.8 spac=$more_coarse 
y.mesh loc=-$N1T spac=$coarse 
y.mesh loc=-$N1T/2 spac=$coarse_fine 
y.mesh loc=-0.01 spac=$fine 
y.mesh loc=-0.007 spac=$fine 
y.mesh loc=-0.005 spac=$fine 
y.mesh loc=-$N1T/7 spac=$fine 
y.mesh loc=-$N1T/12 spac=$super_fine 
y.mesh loc=-$N1T/20 spac=$super_finer 
y.mesh loc=-$N1T/80 spac=$super_finer 
y.mesh loc=0 spac=0.001 
y.mesh loc= 0.0001 spac=0.0001 
y.mesh loc= 0.0005 spac=0.0001 
y.mesh loc=0.001 spac=0.0001 
y.mesh loc=$ InAlNcapT *2/3 spac=$super_finer 
y.mesh loc=$ InAlNcapT /5 spac=$super_finer 
y.mesh loc=$ InAlNcapT -0.0015 spac=$super_finer 
y.mesh loc=$ InAlNcapT -0.0005 spac=$super_finer 
y.mesh loc=$ InAlNcapT -0.0001 spac=0.0001 
y.mesh loc=$ InAlNcapT spac=0.0001 
y.mesh loc=$ InAlNcapT +0.0001 spac=0.0001 
y.mesh loc=$ InAlNcapT +0.0005 spac=$super_finer 
y.mesh loc=$ InAlNcapT +0.0015 spac=$super_finer 
y.mesh loc=$ InAlNcapT +$GaNT/7 spac=$super_fine 
y.mesh loc=$ InAlNcapT +$GaNT/5 spac=$super_fine 
y.mesh loc=$ InAlNcapT +$GaNT/2 spac=$super_fine 
y.mesh loc=$ InAlNcapT +$GaNT spac=0.00001 
y.mesh loc=$ InAlNcapT +$GaNT+$AlNT spac=0.00001 
y.mesh loc=$ InAlNcapT +$GaNT+0.0001 spac=$super_finer 
y.mesh loc=$ InAlNcapT +$GaNT+$AlNT+$InAlNT/9 spac=$super_finer 
y.mesh loc=$ InAlNcapT +$GaNT+$AlNT+$InAlNT/7 spac=$super_finer 
y.mesh loc=$ InAlNcapT +$GaNT+$AlNT+$InAlNT/2 spac=$super_finer 
y.mesh loc=$ InAlNcapT +$GaNT+$AlNT+$InAlNT spac=$super_finer 
y.mesh loc=$ InAlNcapT +$GaNT+$AlNT+$InAlNT+$AlGaNT/2 spac=$fine 
y.mesh loc=$ InAlNcapT +$GaNT+$AlNT+$InAlNT+$AlGaNT spac=$super_finer 
y.mesh loc=$ InAlNcapT +$GaNT+$AlNT+$InAlNT+$AlGaNT+$AlGaNT2/2 spac=$fine
y.mesh loc=$InAlNcapT +$GaNT+$AINT+$InAlNT+$AlGaNT+$AlGaNT2 spac=$super_finer
y.mesh loc=$InAlNcapT +$GaNT+$AINT+$InAlNT+$AlGaNT+$AlGaNT2+$GaNT2/2 spac=$fine
y.mesh loc=$InAlNcapT +$GaNT+$AINT+$InAlNT+$AlGaNT+$AlGaNT2+$GaNT2 spac=$super_finer

## ELIMINATE COLUMNS
Y.MIN=$InAlNcapT +$AlGaNT+$GaNT
Y.MAX=$GaNcapT +$AlGaNT+$GaNT

# Materials Definitions

region number=1 name=Air material=Air y.min=-$AirT y.max=-$N1T
region number=2 name=top material=nitride y.min=-$N1T y.max=0.0
region number=3 name=algancap material=InAlN x.comp=$InAlNcomp x.min=-($SDL+$SGspac) x.max=$GateL+$GDspac+$SDL y.min=0.0 y.max=$InAlNcapT
region number=4 name=ganlayer material=GaN y.min=$InAlNcapT y.max=$GaNT+$InAlNcapT
region number=5 name=AlNlayer material=AlN x.comp=$AlNcomp y.min=$GaNT+$InAlNcapT y.max=$GaNT+$AlGaNT+$AINT
region number=6 name=InAlNlayer material=InAlN x.comp=$InAlNcomp y.min=$GaNT+$InAlNcapT +$AINT y.max=$GaNT+$InAlNcapT +$AINT+$InAlNT
region number=7 name=InAlNlayer material=AlGaN x.comp=$AlGaNcomp y.min=$GaNT+$InAlNcapT +$AINT+$InAlNT+$AlGaNT y.max=$GaNT+$InAlNcapT +$AINT+$InAlNT+$AlGaNT
region number=8 name=InAlNlayer material=AlGaN x.comp=$AlGaNcomp y.min=$GaNT+$InAlNcapT +$AINT+$InAlNT+$AlGaNT y.max=$GaNT+$InAlNcapT +$AINT+$InAlNT+$AlGaNT+$AlGaNT2
region number=9 name=GaNlayer material=GaN y.min=$GaNT+$InAlNcapT +$AINT+$InAlNT+$AlGaNT y.max=$GaNT+$InAlNcapT +$AINT+$InAlNT+$AlGaNT+$AlGaNT2 +$GaNT2

# region number=4 name=ganbuffer material=GaN y.min=$InAlNcapT +$AlGaNT y.max=$InAlNcapT +$AlGaNT+$GaNT
# region number=5 name=Titanium1 material=Titanium x.min=-(SDL+SGspac) x.max=SFP y.min=-N1T y.max=-N1T*3/4

# Define Electrodes

electrode name=source x.min=-(SDL+SGspac) x.max=-SGspac y.min=-0.005 y.max=AlGaNcapT+GaNT+AlNT+InAlNT+AlGaNT+AlGaNT2+GaNT2/2

electrode name=gate x.min=0.0 x.max=GateL y.min=-AirT/2 y.max=0

electrode name=drain x.min=GateL+GDspac x.max=GateL+GDspac+SDL y.min=-0.005 y.max=AlGaNcapT+GaNT+AlNT+InAlNT+AlGaNT+AlGaNT2+GaNT2/2

electrode name=GFPlate x.min=-GFPl x.max=GateL+GFPr y.min=-AirT y.max=-AirT/2

# Define Materials Properties

doping n.type concentration=1e15 uniform

# Interface Charges

interface R1NUMBER=2 R2NUMBER=3 charge=8e12 s.i

intrap R1NUMBER=3 R2NUMBER=4 e.level=1.0 acceptor density=5.0e13 degen.fac=1 sign=1.00e-16 sigp=1.00e-17 s.s

interface R1NUMBER=3 R2NUMBER=4 charge=-8e12 s.s

interface R1NUMBER=4 R2NUMBER=5 charge=4.5e13 s.s

interface R1NUMBER=5 R2NUMBER=6 charge=-1.5e13 s.s

interface R1NUMBER=6 R2NUMBER=7 charge=-1e13 s.s

interface R1NUMBER=8 R2NUMBER=9 charge=-1e13 s.s

material ni.min=1e-10 taun0=1e-9 taup0=1e-9

mobility GaNsat.n fmct.n alphan.fmct=1.001 mu2n.fmct=3000 mun0=1600 ncritn.fmct=1e15 mu1n.fmct=1500
#Define Models

models srh fermi print
#model material=GaN print evsatmod=0

#Define Contacts
contact name=gate workfunc=6.2
contact name=source
contact name=drain
#contact name=SFPlate common=source
contact name=GFPlate common=gate

#Set Outputs
output charge band.param con.band val.band polar.charge qss e.lines e.velocity e.mobility
#method climit=1e-4 itlimit=30 carriers=1 electrons
method newton trap maxtrap=20

#Solve initial
solve init
solve previous
save outfile=out_start_e1.str
#tonyplot out_start_po.str

###################CAPACITANCE SIMULATION####################
solve
solve vdrain=0 local
log outf=out_capacitance_N-polar.log
solve vstep=-0.1 vfinal=-1.0 name=gate ac freq=30e6
solve vstep=-0.1 vfinal=-4.5 name=gate ac freq=30e6

log off

###################END CAPACITANCE SIMULATION ####################
# DC SIMULATION**** Derivation of Electric Field from Structure Files********

# Solve transfer curve at Vds=0V
solve vdrain=0.0
solve vgate=0.0 vstep=0.5 vfinal=1.5 name=gate
log outfile=out_transfer_Vd0.log
#save outfile=out_Vd0_Vg1p5.str
solve vgate=1.4 vstep=-0.5 vfinal=1.0 name=gate
#save outfile=out_Vd0_Vg1p0.str
solve vgate=0.9 vstep=-0.5 vfinal=0.5 name=gate
#save outfile=out_Vd0_Vg0p5.str
solve vgate=0.4 vstep=-0.5 vfinal=0.0 name=gate
save outfile=out_Vd0_Vg0p0.str
solve vgate=-0.1 vstep=-0.5 vfinal=-0.5 name=gate
#save outfile=out_Vd0_VgN0p5.str
solve vgate=0.6 vstep=-0.5 vfinal=-1.0 name=gate
save outfile=out_Vd0_VgN1p0.str
solve vgate=-1.1 vstep=-0.5 vfinal=-1.5 name=gate
#save outfile=out_Vd0_VgN1p5.str
solve vgate=-1.6 vstep=-0.5 vfinal=-2.0 name=gate
save outfile=out_Vd0_VgN2p0.str
solve vgate=-2.1 vstep=-0.5 vfinal=-2.5 name=gate
#save outfile=out_Vd0_VgN2p5.str
solve vgate=-2.6 vstep=-0.5 vfinal=-3.0 name=gate
save outfile=out_Vd0_VgN3p0.str
solve vgate=-3.1 vstep=-0.5 vfinal=-3.5 name=gate
#save outfile=out_Vd0_VgN3p5.str
solve vgate=-3.6 vstep=-0.5 vfinal=-4.0 name=gate
save outfile=out_Vd0_VgN4p0.str
solve vgate=-4.6 vstep=-0.5 vfinal=-5.0 name=gate
save outfile=out_Vd0_VgN5p0.str
solve vgate=-5.6 vstep=-0.5 vfinal=-6.0 name=gate
save outfile=out_Vd0_VgN6p0.str
solve vgate=-6.6 vstep=-0.5 vfinal=-7.0 name=gate
save outfile=out_Vd0_VgN7p0.str
solve vgate=-7.6 vstep=-0.5 vfinal=-8.0 name=gate
save outfile=out_Vd0_VgN8p0.str
solve vgate=-8.6 vstep=-0.5 vfinal=-9.0 name=gate
save outfile=out_Vd0_VgN9p0.str
solve vgate=-9.6 vstep=-0.5 vfinal=-10.0 name=gate
save outfile=out_Vd0_VgN10p0.str
log off
#********************** DC FAMILY CURVES **************************** * 

load infile=out_Vd0_Vg0p0.str master
solve vdrain=0.0
log outfile=out_family_Vg0p0.log
solve vdrain=0.0 vstep=2 vfinal=20 name=drain previous
#save outfile=out_Vg0p0_Vd20.str
log off

load infile=out_Vd0_VgN1p0.str master
solve vdrain=0.0
log outfile=out_family_VgN1p0.log
solve vdrain=0.0 vstep=2 vfinal=20 name=drain previous
#save outfile=out_VgN1p0_Vd20.str
log off

load infile=out_Vd0_VgN2p0.str master
solve vdrain=0.0
log outfile=out_family_VgN2p0.log
solve vdrain=0.0 vstep=2 vfinal=20 name=drain previous
#save outfile=out_VgN2p0_Vd20.str
log off

load infile=out_Vd0_VgN3p0.str master
solve vdrain=0.0
log outfile=out_family_VgN3p0.log
solve vdrain=0.0 vstep=2 vfinal=20 name=drain previous
#save outfile=out_VgN3p0_Vd20.str
log off

load infile=out_Vd0_VgN4p0.str master
solve vdrain=0.0
log outfile=out_family_VgN4p0.log
solve vdrain=0.0 vstep=2 vfinal=20 name=drain previous
#save outfile=out_VgN4p0_Vd20.str
log off

quit

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