ABSTRACT

LUO, HAOJUN. Amorphous Indium Gallium Zinc Oxide Based Thin Film Transistors and Circuits. (Under the direction of Dr. John Muth.)

The goal of this dissertation is to develop high performance indium gallium zinc oxide (IGZO) based thin film transistors and circuits. Individual IGZO transistors on glass and silicon were optimized and used to form basic circuit elements including inverters, NOR and NAND gates. A novel focused ion beam (FIB) approach was also investigated, where devices were formed by milling a channel to separate the source and drain. This first report of forming IGZO transistors by focused ion beam milling with sub-micron channels is interesting since it sidesteps having to use e-beam lithography or advanced photolithography methods.

Typical IGZO TFTs on glass with an AlOx gate dielectric, at VDS = 5 V, a threshold voltage of 0.2 V, a subthreshold slope of less than 190 mV/decade, an on/off current ratio larger than 10^8, and a saturation field effect mobility μsat of 14 cm^2 V^-1 S^-1 were measured.

IGZO based logic gates including inverter, NAND and NOR gates were designed, fabricated and characterized. For a typical inverter, a peak gain magnitude of 18.4 was measured at VDD=20V for static characterization. The transfer characteristics of logic gates under different supply voltages with a variety of beta ratios were also discussed and analyzed. The NAND and NOR gates demonstrated sharp transfer characteristics and satisfactory functionality between 1 and 20 V with operating frequencies reaching 5 kHz.

Submicron IGZO TFTs formed using focused ion beam etching were successfully fabricated and demonstrated. Typical devices were fabricated on SiO2/Si substrate with a bottom gate structure. Devices with channel lengths as small as 50 nm were obtained. The
devices were unusual in that a side gate channel was formed. Optimized devices had on/off ratio of $10^8$, a threshold voltage of 0.2V and subthreshold slope of 170mV/decade were measured.

IGZO is a fascinating material with high potential to be used in a wide variety of technologies. Applications include future high-end displays, transparent electronics, flexible electronics, memories, and potentially three dimensional integrated circuits.
Amorphous Indium Gallium Zinc Oxide Based Thin Film Transistors and Circuits

by
Haojun Luo

A dissertation submitted to the Graduate Faculty of
North Carolina State University
in partial fulfillment of the
requirements for the degree of
Doctor of Philosophy

Electrical Engineering

Raleigh, North Carolina
2013

APPROVED BY:

__________________________________  ____________________________
Dr. John Muth  Dr. Leda Lunardi
Committee Chair  Co-Chair

________________________________
Dr. Robert Kolbas  Dr. Veena Misra

________________________________
Dr. Mark Johnson
DEDICATION

To my loving parents, my wife and my daughter.
BIOGRAPHY

Haojun Luo was born in a small town in Guangdong, south China. He hoped to have the chance to meet people from different areas and different cultures, so he decided to attend Nanjing University, which located in a famous historical city far from his hometown. He dreamed to make this world a little better with knowledge of science and technology, so he chose materials science and technology as his undergraduate major. After he got his Bachelor Degree, he joined the Department of Physics, Peking University, where he started research in III-V optoelectronics devices. After working in Hong Kong University of Science and Technology for one year, he joined Electrical Engineering at NCSU in Fall 2007. Since then he worked in Dr. Muth’s group. His doctoral dissertation project focused on developing amorphous oxide semiconductors based thin film transistors and circuits. He also worked on another two side projects: thermal conductivity measurement and terahertz laser switches.
ACKNOWLEDGMENTS

Looking back these 6 years in NCSU, I would like to thank my committee, my colleagues, friends and my family for all their help and support.

Firstly, I want to thank my committee for being interested in my research project and guiding me during my doctoral research:

I owe Dr. Muth a debt of gratitude, for his invaluable resources, support, and guidance. Whenever I come to him, he is always very helpful. As an advisor, he always tries to make sure the students receive good training; at the same time, he tries to take good care of every student as he can. He is a role model of mine, both in research and in daily life.

I want to thank Dr. Lunardi for being my co-chair. She took good care of me when Dr. Muth was in Iraq. She is an expert in semiconductor devices. She always gives me very good suggestions and advices. I learnt a lot by discussing with her.

I am very grateful to Dr. Misra. She is an expert in transistors and gave me a lot of very good suggestions in research. Moreover, without the ALD tool and characterization tools in Dr. Misra’s lab, this work couldn’t be made possible.

I appreciate Dr. Kolbas for his guidance when Dr. Muth was on call. He is very knowledgeable. He helped me a lot during my research work.

I would like to Thank Dr. Johnson for being my committee member. He is always eager to help whenever I needed assistance.

Joe is a vital resource for me and other students. I really appreciate his training and his help on experiments. I will remember the days I worked with him.
I want to express my thanks to Dr. Batchelor, Dr. Dieter and Jonathan from AIF for helping to carry out the FIB etching project. I want to thank Dr. Schwartz, Dane Philips and Sasha for their funding support and discussion.

I would like to thank all the former and current members in MRC112 and in our group. I met them, worked with them and became good friends with them. They are: Arun Suresh, Patrick Wellenius, Jim Simpson, Williams Cox, Yi Lou, Yan Wang, Wencong Zhu, Longju Liu, Hongguo Zhang, Kory, Kanu, Jong Boem Park, Leandra, Xiang Ji, Yifan Wang, Nishad, Bharat, Abhishek Malhotra, Benjamin Decker, Sushmit Mallik, Shravan Chintapatla, and Brandon Conover. They gave me a lot of help and support. Of course we shared a lot of fun as well. I want to express my special thanks to Arun and Patrick for their help and training me in my early years. I want to express my special thanks to Leandra for helping to check this dissertation.

Lastly, I want to thank my parents, my brothers and sister. Without their deep love and endless support, I cannot be where I am now. I want to thank my wife Yingyi. This work would have been impossible without her love, encouragement and support.
# TABLE OF CONTENTS

LIST OF TABLES ................................................................................................................. x
LIST OF FIGURES .................................................................................................................. xi

Chapter 1 INTRODUCTION ................................................................................................. 1
  1.1 Overview ......................................................................................................................... 1
  1.2 Research Objective and Dissertation Organization ...................................................... 2

Chapter 2 LITERATURE REVIEW AND BACKGROUN ...................................................... 5
  2.1 Thin Film Transistor ....................................................................................................... 5
      2.1.1 Background and History ....................................................................................... 5
      2.1.2 Thin Film Transistor Structures ......................................................................... 6
      2.1.3 Basic Device Operation ....................................................................................... 9
  2.2 Transparent Conducting Oxides (TCOs) ..................................................................... 12
  2.3 Development History of AOSs Based TFTs ................................................................. 14
  2.4 Amorphous Oxide Semiconductors ............................................................................. 15
  2.5 Indium Gallium Zinc Oxide ............................................................................................. 19
  2.6 Device Review--Individual Transistor ............................................................................ 23
  2.7 Amorphous Oxide Semiconductors Based Circuits ...................................................... 27
  2.8 P-type Amorphous Oxide Semiconductors and Devices .............................................. 31
      2.8.1 Motivation and Challenges .................................................................................. 31
      2.8.2 P-Type Conducting Oxide Materials and Their Structures ................................. 32
      2.8.3 Recent Development of Materials for p-TTFTs ................................................... 37
  2.9 Oxide Transistors for Display Applications ..................................................................... 39

Chapter 3 EXPERIMENTAL TOOLS AND DEVICE CHARACTERIZATION .................. 43
  3.1 Vacuum Deposition Techniques .................................................................................... 43
      3.1.1 Pulsed Laser Deposition ..................................................................................... 43
      3.1.2 Atomic Layer Deposition ..................................................................................... 47
      3.1.3 Plasma-Enhanced Chemical Vapor Deposition ................................................... 50
3.1.4 E-Beam Evaporation........................................................................51
3.2 Patterning Techniques........................................................................52
  3.2.1 Photolithography........................................................................52
  3.2.2 Lift Off.......................................................................................52
  3.2.3 Etching.......................................................................................54
3.3 Focused Ion Beam.............................................................................56
3.4 Device Fabrication............................................................................57
3.5 Electrical Characterization of Thin Film Transistor.........................58
  3.5.1 Thin Film Transistors Operation Equations...............................59
  3.5.2 DC Current-Voltage Measurement--Output Characteristics........60
  3.5.3 DC Current-Voltage Measurement--Transfer Characteristics.....61
    3.5.3.1 Subthreshold Swing and Drain Current On-Off Ratio..........61
    3.5.3.2 Threshold Voltage and Turn-on Voltage.............................63
    3.5.3.3 Mobility Extraction.............................................................65
3.6 Conclusions....................................................................................69

Chapter 4 INDIVIDUAL INDIUM GALLIUM ZINC OXIDE THIN FILMS
TRANSISTORS AND DEVICE STUDY......................................................71
  4.1 Overview.......................................................................................71
  4.2 Effect of Oxygen Partial Pressure................................................72
  4.3 Effect of Channel Thickness.........................................................75
  4.4 Effect of Gate Dielectric Thickness................................................76
  4.5 Effect of Channel and Source Drain Overlap Area..........................77
  4.6 Effect of Patterned Gate.................................................................79
  4.7 Stability of Devices........................................................................82
  4.8 Effect of Annealing.........................................................................83
  4.9 Effect of Channel Length.................................................................86
  4.10 Conclusions................................................................................89

Chapter 5 LOGIC GATES.........................................................................91
5.1 Abstract .................................................................91
5.2 Introduction.............................................................91
5.3 Experimental Approach ..............................................93
5.4 Discrete Transistor Characteristics ...............................94
5.5 Inverter ......................................................................95
5.6 NAND Gate ..............................................................100
5.7 NOR Gate ..................................................................107
5.8 Discussion ..................................................................111
5.9 Conclusions ...............................................................112

Chapter 6 SUBMICON OXIDE THIN FILM TRANSISTORS USING FOCUSED ION BEAM .................................................................113
6.1 Introduction ..................................................................113
6.2 Focused Ion Beam (FIB) Etching ....................................114
6.3 Devices Fabrication and Experiments .............................116
6.4 Amorphous Oxide Side Channel TFTs Etched by FIB ........118
   6.4.1 Right after FIB Etching ..............................................119
   6.4.2 After Annealing in Air at 200 ºC for 30 min .................121
   6.4.3 After Annealing in Air at 300 ºC for 30 min .................122
   6.4.4 After Annealing in Air at 350 ºC for 30 min .................124
   6.4.5 After Annealing in Air at 400 ºC for 30 min .................124
6.5 Discussion ..................................................................128
6.6 Devices with Different Etching Depth .............................131
6.7 Conclusions ...............................................................137

Chapter 7 CONCLUSIONS AND RECOMMENDATION FOR FUTURE WORKS .......138
7.1 Conclusions ...............................................................138
7.2 Recommendation of Future Research ..............................141
REFERENCES ................................................................147
LIST OF TABLES

Table 2.1: Comparison of several materials used in TFTs.................................20
Table 2.2: Optical and electrical properties of ZnMgO₄ films ..............................36
Table 4.1: Summary of devices fabricated in this work.........................................71
LIST OF FIGURES

Figure 2.1: Schematics of the four most common TFT structures, according to the position of the gate electrode and to the distribution of the electrodes relatively to the semiconductor. (a) Stagger bottom gate, (b) Coplanar bottom gate, (c) Stagger top gate, and (d) Coplanar bottom gate. ..............................................................7

Figure 2.2: The TFT structure and energy band diagram as viewed through the gate: (a) the structure of a TFT, (b) at equilibrium, $V_{GS}=0$, (c) depletion, $V_{GS}<0$, (d) accumulation, $V_{GS}>0$. .................................................................................10

Figure 2.3: Different formation mechanisms of bandgaps in semiconductors. (a) Bandgap of Si is formed of the energy splitting of levels. (b) Oxygen 2p and metal (M) ns orbital forms valence band maximum and the conduction band minimum, respectively, due to the Madelung potential. After reference [26]..................16

Figure 2.4: Schematic orbital structure of the conduction-band minimum in (a) covalent semiconductors and in (b) ionic oxide semiconductors .........................18

Figure 2.5: (a) Amorphous formation and (b) electron transport properties of In$_2$O$_3$-Ga$_2$O$_3$-ZnO thin films. The values in (b) denote the electron Hall mobility (cm$^2$/V s) with density ($10^{18}$ cm$^{-3}$) in parentheses. .........................................................21

Figure 2.6: Controllability and stability of a-IGZO and a-IZO films. (a) Relationship between carrier density and oxygen pressure during deposition. (b) Stability of film conductance after deposition.........................................................22

Figure 2.7: (a) Schematic of an inverter, (b) 5-stage ring oscillator .........................28

Figure2.8: Simplified electronic structures in oxides (A) In typical n-type TOS, conduction band minimum is composed mainly of metal s orbitals and valence band maximum (VBM) of O 2p orbitals. (B) In Cu-based p-type TOSs, VBM is made of hybridized orbitals of Cu 3d and O 2p, which raises the energy level of VBM and forms more conductive hole transport paths. (C) In oxychalcogenides, hybridization of VBM enhanced by intervention of the chalcogen p orbitals. The energy level of VBM is raised and hole effective mass is reduced as the atomic number of the chalcogenide is increased. .........................................................33

Figure 2.9: Structure of (a) delafossite structure Copper oxides [58]. (b) Structure of SrCu$_2$O$_2$ ........................................................................................................................................34

Figure 3.1: Schematic of the pulsed laser deposition system in NCSU..................46

Figure 3.2: ALD growth mechanisms at different temperatures.........................49
Figure 3.3: TFTs devices structure: (a) patterned gate, (b) common gate structure...........58

Figure 3.4: Output characteristics of an IGZO TFT (T92). Drain current (linear scale) is plotted against drain voltage for gate voltages 0-15 V in 3 V steps. Gate oxide is 100nm SiO$_2$, 50 nm IGZO grown at 25 mT oxygen partial pressure, TFT dimension, W/L=50 µm /10 µm..............................................60

Figure 3.5: Typical transfer characteristics of an IGZO TFT (N10) at 3 different V$_{DS}$, 0.1V, 2V and 10 V. Subthreshold voltage swing, drain current on-off ratio, and turn-on voltage are indicated in the figures. IGZO layer of ~45 nm was grown at 25 mTorr oxygen partial pressure. TFT dimensions, W/L = 50 µm /10 µm.............63

Figure 3.6: Threshold voltage extraction from the same device. (a) I$_{DS}$ −V$_{GS}$ extraction at the linear regime, V$_{DS}$=0.1V. (b) $\sqrt{I_{DS}}$ − V$_{GS}$ extraction at the saturation regime, V$_{DS}$=10V. This device is same as shown in Figure 3.5..............................64

Figure 4.1: (a) Comparison of transfer curves for different oxygen partial pressure. V$_{DS}$=10V, L/W=100 µm /20 µm (b) parameters extracted from (a). IGZO thicknesses are kept at 35nm..........................................................73

Figure 4.2: Comparison of saturation mobilities of TFTs with IGZO grown at different oxygen partial pressure.................................................................74

Figure 4.3: (a) Comparison of transfer curves for different channel thickness. V$_{DS}$=10V, L/W=100 µm/20 µm, oxygen partial pressure is 25mT for both deposition. (b) Comparison of saturation mobilities of TFTs with different IGZO channel thickness. Channel thicknesses are 20nm and 35nm channel, respectively......75

Figure 4.4: Comparison of devices with different Al$_2$O$_3$ dielectric thicknesses................77

Figure 4.5: The images of channel and source drain overlap--full overlap and half overlap..........................................................78

Figure 4.6: Effect of Channel and source/drain overlap (L/W=100 µm /400 µm), (a) logarithm scale, (b) linear scale..............................................................79

Figure 4.7: (a) Images of pattern gate device and un-patterned gate devices (b) Transfer curves of patterned and un-patterned gate TFTs........................................80

Figure 4.8: (a) Transfer curves of un-patterned gate devices with ITO and Ti source drain (L/W=200 µm /800 µm) (b) Transfer curves of patterned gate devices with ITO and Ti source drain, (L/W=100 µm /400 µm).................................81
Figure 4.9: Transfer curves of devices measure right after fabrication and after 3 weeks, (a) patterned TFTs with ITO source drain, (b) patterned TFTs with Ti source drain

Figure 4.10: (a) Transfer curves of devices annealed at different temperature. (b) Hysteresis window, $V_{on}$ and saturation current ($I_{DS}$) changed with different annealing temperature

Figure 4.11: Comparison of IGZO annealing before and after ITO deposition

Figure 4.12: The electrical characteristics of TFT with $L\times W=2 \, \mu m \times 25 \, \mu m$. (a) $I_{DS}~V_{GS}$ curve, (b) $I_{DS}~V_{DS}$ curve

Figure 4.13: Comparison of transfer curves for different channel lengths (a) Transfer curves. (b) The relationship of $V_{on}$, saturation current $I_{DS}$ with different channel lengths

Figure 5.1: (a) Cross section of IGZO TFTs , (b) Image of IGZO based all oxide transparent TFTs and logic gates on glass substrate

Figure 5.2: (a) Log ($I_{DS}$) – $V_{GS}$ and log($I_G$) – $V_{GS}$ at $V_{DS}=5 \, V$ for IGZO TFTs. The plot also has the gate leakage, $I_G$, as a function of the gate bias (b) Drain current- Drain voltage ($I_{DS}-V_{DS}$). The TFT has Al$_2$O$_3$ as the gate dielectric and the IGZO channel is deposited at oxygen partial pressure of 25 mTorr. TFT dimensions, $W/L= 50 \, \mu m /10 \, \mu m$

Figure 5.3: (a) A photo image of inverter, Load transistor dimension is $W/L=10 \, \mu m /10 \, \mu m$. Load transistor dimension 200/10 \, \mu m. (b) Schematic diagram of inverter

Figure 5.4: (a) Schematic diagram and voltage transfer curve of an inverter at $V=1V$, 2V, 5V,10V and 20V ($L_{drive}/W_{drive}=20 \, \mu m/400 \, \mu m$, $L_{load}/W_{load}=20 \, \mu m/20 \, \mu m$. $OL=2.5 \, \mu m$), this study, (b) Transfer curve for a transparent inverter fabricated using IGZO TFTs for different values of $V_{DD}$ ($L_{drive} /W_{drive} = 20 \, \mu m /400 \, \mu m$, $L_{load} /W_{load} =20 \, \mu m /40 \, \mu m$, $OL=2.5 \, \mu m$)

Figure 5.5: Inverter device parameters extraction from transfer curve. $L_{drive}/W_{drive}=20 \, \mu m /400 \, \mu m$, $L_{load}/W_{load}=20 \, \mu m /20 \, \mu m$. $OL=2.5 \, \mu m$

Figure 5.6: Inverters with different beta ratio. Channel length $L=20 \, \mu m$, beta ratio for these three inverters are $\beta=2.5$, $\beta=5$, and $\beta=20$

Figure 5.7: Relationship between inverter gain and supply voltage, $V=1V$, 2V, 5V,10V and 20V ($L_{drive}/W_{drive}=20 \, \mu m /400 \, \mu m$, $L_{load}/W_{load}=20 \, \mu m /20 \, \mu m$. $OL=2.5 \, \mu m$); (b)
Relationship between inverter gain and beta ratio. $V_{DD}=5V$, Channel length $L=20\ \mu m$, beta ratio $\beta=2.5$, $\beta=5$, and $\beta=20$.

Figure 5.8: (a) Optical micrographs of NAND, (b) The schematic diagram of NAND gate.

Figure 5.9: Voltage transfer characteristics for a NAND gate ($W_{drive}/L_{drive}=20\ \mu m / 200\ \mu m$, $W_{load}/L_{load}=20\ \mu m / 20\ \mu m$).

Figure 5.10: Voltage transfer characteristics at different supply voltages ($W_{drive}/L_{drive}=20\ \mu m / 200\ \mu m$, $W_{load}/L_{load}=20\ \mu m / 20\ \mu m$).

Figure 5.11: Voltage transfer characteristics of IGZO based NAND gate with different beta ratios ($L=10\ \mu m$, $\beta=2.5$, 10, 40).

Figure 5.12: Schematic of experimental set up for measuring dynamic performance of NAND and NOR gates.

Figure 5.13: Output waveforms with supply voltage of a NAND gate ($W_{drive} / L_{drive} = 400\ \mu m / 10\ \mu m$, $W_{Load} / L_{Load} = 10\ \mu m / 10\ \mu m$, overlap=2.5 $\mu m$) operating at (a) 100Hz, and (b) 5kHz. $V_{DD}=10\ \text{V}$.

Figure 5.14: (a) Optical micrographs of NOR gate, (b) The schematic diagram of NOR gate.

Figure 5.15: Voltage transfer characteristics of a NOR gate ($L/W=10\ \mu m / 25\ \mu m$, $V_{DD}=5\ \text{V}$).

Figure 5.16: Voltage transfer characteristics of IGZO based NOR gates with different beta ratios ($L=10\ \mu m$, $\beta=2.5$, 5, 10).

Figure 5.17: Dynamic waveform characterization of a NOR gate ($L_{Drive}=5\ \mu m$, $W_{Drive}=100\ \mu m$, $L_{Load}=5\ \mu m$, $W_{Load}=5\ \mu m$, 2.5 $\mu m$ overlap) operating at (a) 100Hz and (b) 5 kHz.

Figure 6.1: (a) Illumination of FIB sputtering, drawing based on [46], (b) SEM images of silicon single pixel etched by straight line scan and fitting the trench cross-section profile with a Gaussian function.

Figure 6.2: Cross section of device structure and illustration of the FIB etching process. The IGZO underneath the Ti layer is designed to be 10$\mu m$×4$\mu m$. It is wider than Ti width which is 4$\mu m$ for protecting the SiO$_2$ dielectric layer during etching.
process. The overlap of IGZO and Ti is about 2µm on source / drain for carrier injection

Figure 6.3: Device top surface SEM Images of (a) device before FIB etching, and (b) device after FIB etching (tilted angle)

Figure 6.4: (a) Illustration of current flow when the device is on state, $V_G > V_T$, $V_{DS} > 0$ (b), Cross section of a lateral TFT etched by FIB

Figure 6.5: (a) Transfer characteristics ($V_D=3V$) and (b) Output characteristics of a thin film transistor (W/L=4µm/20nm) after FIB etching

Figure 6.6: (a) Transfer characteristics ($V_{DS}=3V$) and (b) Output characteristics of a thin film transistor (W/L=4µm/20nm) etched by FIB and annealed at 200 ºC in the air for 30 min

Figure 6.7: $\sqrt{I_{DS}}$ vs. $V_{GS}$ characteristics of an IGZO TFT etched by FIB, then annealed at 200 ºC for half an hour. Biased in the saturation regime with $V_{DS}=3 V$, W/L=4µm/20nm

Figure 6.8: (a) Transfer characteristics ($V_D=3V$) and (b) Output characteristics of a thin film transistor (W/L=4µm/20nm) etched by FIB and annealing at 300 ºC in air for 30 min

Figure 6.9: $\sqrt{I_{DS}}$ vs. $V_{GS}$ characteristics of an IGZO TFT by FIB, then annealed at 300 ºC for half an hour. Biased in the saturation regime with $V_{DS}=3 V$, W/L=4 µm/20nm

Figure 6.10: (a) Transfer characteristics ($V_D=3V$) and (b) Output characteristics of a thin film transistor (W/L=4µm/20nm) etched by FIB and annealed at 350 ºC in air for 30 min

Figure 6.11: $\sqrt{I_{DS}}$ vs. $V_{GS}$ characteristics of an IGZO TFT by FIB, then annealed at 350 ºC for 30min. Biased in the saturation regime with $V_{DS}=3 V$, W/L=4µm/20nm

Figure 6.12: (a) Transfer characteristics ($V_D=3V$) and (b) Output characteristics of a TFT (W/L=4µm/20nm) etched by FIB and annealed at 400 ºC in air for 30 min

Figure 6.13: $\sqrt{I_{DS}}$ vs. $V_{GS}$ characteristics of an IGZO TFT by FIB, then annealed at 400 ºC for half an hour. Biased in the saturation regime with $V_{DS}=3 V$, W/L=4 µm/20nm
Figure 6.14: SEM image shows the IGZO damage at the corner of etching gap, after repeating high voltage, high current measurements……………………127

Figure 6.15: Comparison of TFTs with different gaps after annealing at 350 °C…………128

Figure 6.16: Simulation results from Synopsys Sentaurus, (a) electrostatic potential distribution, and (b) electron density distribution on the device. ……………129

Figure 6.17: Comparison of $V_{th}$ SS, and $I_{off}$ at different annealing temperatures, $V_{DS} = 3$ V, W/L=4μm/ 20nm……………………………………………………130

Figure 6.18: Cross section image of a TFT etched by FIB………………………………132

Figure 6.19: (a) Transfer characteristic and (b) Output characteristic of direct channel IGZO based TFTs etched by FIB, W/L=4μm/20nm. Measure right after etching at room temperature…………………………………………………………133

Figure 6.20: (a) Transfer characteristic and (b) Output characteristic of direct channel IGZO based TFTs etched by FIB and annealing at 300 °C in the air for 30 min, W/L=4μm/20nm. ………………………………………………………………………………………………………134

Figure 6.21: (a) Transfer characteristic and (b) Output characteristic of direct channel IGZO based TFTs etched by FIB and annealed at 350 °C in air for 30 min, W/L=4μm/20nm. ………………………………………………………………………………………………………135

Figure 6.22: $I_{DS}$ vs. $V_{GS}$ characteristic of an IGZO TFT by FIB, then annealed at 350 °C for half an hour. Biased in the saturation regime with $V_{DS} = 3$ V, W/L=4μm/20nm……………………………………………………………………………………………………135

Figure 6.23: Transfer characteristics of direct channel and lateral channel TFTs using by FIB……………………………………………………………………………………………………136

Figure 7.1: Image of E-beam lithography patterned IGZO based TFT, L/W=200 nm/500 nm……………………………………………………………………………………………………144
Chapter 1
INTRODUCTION

1.1 Overview

Transparent oxide semiconductors (TOSs) are a new class of inorganic oxides based on multi-component combinations of post-transition metal cations with (n-1)d^{10}ns^{0} electronic configuration (n≥5). They are usually transparent from the infrared to the visible spectrum due to a large bandgap (>3.0 eV). In addition to transparency, TOSs have high electrons mobilities even in their amorphous phases due to the special electron structures. This makes them very promising for transparent thin-film transistor (TTFTs) applications.

Compared to amorphous silicon and organic semiconductors, TOS based TFTs technology possess several advantages: the magnitude of electron mobility is one or two orders higher even in the amorphous state (>10 cm²/V s); low process temperatures for the amorphous phase including room temperature deposition makes it possible to deposit the film on flexible substrates; good transparency to visible light makes it more suitable in display applications and transparent circuits; and furthermore, they are usually non-toxic and relatively cheap to fabricate. These advantages make TOSs TFTs technology a strong candidate for the next generation large screen flat panel displays and flexible electronics.

At the system level, potential applications are discussed as below:

People are attracted to the futuristic transparent displays that have been shown in several science fiction movies like Minority Report and Avatar. Advanced touch screen displays
allow the users to manipulate data and show figures on a large transparent wall or window. The recently developed technology-- transparent oxide semiconductors (TOSs) based circuits will leads us one step closer to this futuristic technique.

Another set of emerging technologies are flexible electronic, for example, devices that can be used in wearable computers; flexible displays that can be bent [1]; and health diagnosis sensors on the skin or embedded in clothes. All these technologies look very promising and have a suitable market. One possible key technique for flexible electronics is transparent oxide amorphous semiconductor based circuits.

Current LCDs and flexible displays typically use amorphous silicon (a-Si) or organic TFTs as control circuits. However, the relatively low mobility (<1 cm²V⁻¹ s⁻¹) and inferior bias stability of a-Si and organic TFTs limit their practical applications in large area flat panel displays and flexible electronics. It is predicted that amorphous silicon will reach its “bottle neck” for the future large screen (>90 inches) at the frame rate higher than 120Hz due to the poor mobility. Amorphous oxide electronics with their superior mobility could solve this problem.

In addition to applications in LCDs and flexible electronics, many other applications for TOSs TFTs have been proposed. These TFTs show sensitivity to some specific gases or vapors, which also makes them suitable as gas sensors [2-3]. TOSs based TFTs have also been used in solar cell [4], three dimensional integrated circuits, and memory elements [5-6].
1.2 **Research Objective and Dissertation Organization**

Three primary goals are pursued in this dissertation.

The successful implementation of transparent electronics devices and applications require a thorough and comprehensive understanding of the AOS physics and chemical properties, as well as material optimization and understanding devices characteristics. The first primary goal is to optimize and develop high performance IGZO based AOS TFTs deposited by pulsed laser deposition and investigate the parameters that would affect the device performance are investigated and discussed.

The second primary goal is to develop and investigate IGZO based NAND and NOR logic gates. Research efforts in AOS have focused on materials development and the performance of discrete devices [7-9]. This thesis includes some of the first published NAND and NOR gates in IGZO [10].

The third goal is to fabricate submicron AOSs based TFTs using a new method, focused ion beam (FIB) etching. This is a quick, mask free process to fabricate submicron devices. While in the display applications, the devices need to be uniform in large area, in some other applications such as 3D IC or memory; smaller devices will enable higher integration density.

The structure of this dissertation is organized by the following.

Chapter 2 reviews the relevant literature, including the properties of AOS and IGZO, development history and AOSs based TFTs, and followed by the state of art review of current AOS based devices and circuits. Device physics and operation of thin film transistors
will also be discussed to provide background knowledge for the experimental work presented in this dissertation.

Chapter 3 provides the description of experimental tools and process flows to make AOS TFTs, including pulsed laser deposition, plasma enhanced chemical vapor deposition, atomic layer deposition, focus ion beam and photolithography, followed by a discussion on the electrical TFT characterization methodology and figures-of-merit.

Chapter 4 presents the electrical characteristics of individual IGZO transistors and will discuss the device optimization. Several parameters and effects that will affect the device performance including: overlap area, channel thickness, dielectric thickness, the short channel effect, device stability, and patterned gate and annealing will be discussed.

Chapter 5 discusses the development of the IGZO based logic gates, including inverters, NAND and NOR gates. The effect of beta ratio and other parameters that will affect the logic gate characteristics are also explored.

Chapter 6 discusses small channel length TFTs etched by focus ion beam (FIB). Process details and device performance under different annealing temperatures will be presented in this chapter.

Chapter 7 summarizes all the major results presented in the dissertation and discusses some relevant future work.
CHAPTER 2
LITERATURE REVIEW AND BACKGROUND

2.1 Thin Film Transistor

2.1.1 Background and History

The thin film transistor (TFT) is a special kind of field effect transistor [11] and is different from conventional MOS transistors, where the substrate is usually the semiconductor. In TFTs a thin film of semiconductor layer is usually deposited on another isolating support substrate. The applied gate voltage will modulate the electrical field on the channel and the bias between the source/drain will drive the current flow from drain to source if a channel is formed.

The first working TFT was demonstrated by Weimer in 1962 [12], in a top gate structure with a channel thin film of poly cadmium sulfide (CdS). Later, Weimer used cadmium selenide, which made for a better FET. Other TFT semiconductor materials such as Te, InSb and Ge were also investigated, but due to the emergence of the MOSFET based on crystalline silicon technology and the possibility to perform integrated circuits in the mid-1960s, TFT development activity declined for several years at the end of the 1960s[13].

In the 1970s, LeComber, Spear and Ghaith reported a TFT using a-Si:H as the active semiconductor material, and suggested active matrix liquid crystal displays (AMLCD) as one of the applications. Since that, TFTs have attracted a lot of attention again. The most widely used application of TFTs is as switching transistors for active matrix liquid crystal
displays (AMLCD). Later on, poly-Si was also used due to better quality and higher electron mobility. The mobilities of a-Si:H and poly-Si are in the range of 0.5–1.0 cm² V⁻¹ s⁻¹ and 10–80 cm² V⁻¹ s⁻¹, respectively. The maximum processing temperatures for these two technologies are around 300 °C and 500 – 600 °C, respectively [14].

In addition to a-Si and poly-Si TFTs, other types of TFTs use organic materials as the channel layer. Organic TFTs usually have a low mobility of ~10⁻³ cm² V⁻¹ s⁻¹, however, the advantages of this technology include low cost, and simple processing, such as spin coating and printing. Moreover, the processing temperature of these devices is typically below 300 °C. This allows plastic substrates to be used for flexible devices. A large number of these organic channel materials are p-type. However, n-type and ambipolar TFTs have been demonstrated using organic channel layers [15].

Metal oxide based TFTs attract a lot of research attention since 2003. They are thought to be a good candidate for the next generation technology for large area displays and flexible electronics. More detail about metal oxide based transistors and circuits will be discussed later this chapter. In the following subsections, a brief description about the TFT device structures and device operation principle will be presented.

2.1.2 Thin Film Transistor Structures

Figure 2.1 shows four of the most commonly used TFT structures. They are: co-planar top-gate, co-planar bottom gate, staggered top-gate, and staggered bottom-gate [16]. Depending on the source/drain electrodes placement on the device, the devices are categorized as co-planar structures and staggered structures. In the co-planar structure,
source/drain electrodes are on the same side of the semiconductor and insulator interface, while in staggered structures, source/drain electrodes are placed on opposite sides of the semiconductor-insulator interface. Depending on whether the gate electrode is on the top or bottom of the structure, they are categorized as top-gate and bottom-gate structures [11].

Different structures have their own advantages and disadvantages: while the staggered structure provides a large contact area for the source/drain contacts for charge injection, the co-planar structure leads the source/drain contacts to be in direct contact with the induced channel.

Figure 2.1: Schematics of the four most common TFT structures, according to the position of the gate electrode and to the distribution of the electrodes relatively to the semiconductor. (a) Stagger bottom gate, (b) Coplanar bottom gate, (c) Stagger top gate, and (d) Coplanar bottom gate. After reference [16].
For bottom-gate structures, the gate electrode and the gate insulator are present beneath the semiconductor. The advantage to this is that usually the dielectric layer is deposited under high power or high temperature, depositing the gate and dielectric layer first would avoid affecting the semiconductor layer. The drawback is that the surface of the semiconductor is exposed to atmosphere. Thus environmental gases like moisture or air may affect the semiconductor layer and device performance.

For top gate structures, the gate and insulator layer are present on top of the semiconductor layer. The advantage of this is that the channel layer is covered by the insulator and hence the surface is passivated. The drawback is that we need to avoid damage to the semiconductor layer and reduce the interface state when depositing the gate dielectric layer.

The process integration and fabrication parameters also play a role in determining the final TFT structure. For example, the staggered bottom-gate structure is usually used for the fabrication of a-Si:H TFTs, due to easier processing and better electrical properties. Also, when using in the LCD displays, since a-Si:H is sensitive to light, in this staggered structure, the metal gate electrode can shield the semiconductor material from backlight exposure. While a coplanar top-gate structure is normally preferred for poly-Si TFTs, the poly-Si process requires high temperatures that could degrade the properties of other materials (and their interfaces) previously deposited. And it is preferred if the ploy-Si is a flat and continuous film without any layers underneath it [16].

Figure 2.1 only shows the 4 commonly used types of structures, in reality, the structure could change in order to improve the device performance, for instance, in a-Si:H, the a-Si
underneath the source/drain regions are sometimes heavily doped to reduce contact resistance. Also some passivation layer may be added to the staggered bottom gate structure to improve the device long time reliability.

2.1.3 Basic Device Operation

TFT is a three terminal field effect device. Unlike conventional MOSFET which relies on the inversion layer to form the channel, TFT is an accumulation mode device.

In this subsection, an n channel accumulation mode TFT will be used as example to explain the operation principles of TFTs, while a similar discussion could be extended to p-channel TFTs.

Figure 2.2 shows a TFT structure and the energy band diagram of the device at different biases. Ideally it has been assumed in this discussion that: 1) the semiconductor is slightly n type; 2) there is no charge inside the semiconductor and; 3) the semiconductor and gate electrode have the same work function.

Figure 2.2(b) shows the equilibrium state, where there is no external voltage applied to the gate electrode. The energy bands are not bended. When there is a negative bias applied to the gate electrode, as shown in Figure 2.2(c), the mobile electrons in the semiconductor layer are repelled away from the interface, leaving a depletion region near the semiconductor/dielectric interface. From the band diagram of view, the conduction band in the semiconductor layer bends upwards close to the dielectric layer. This makes the semiconductor layer less conductive compared to the equilibrium state. If the magnitude of the negative gate bias is increased, the depletion region grows further into the semiconductor
layer and eventually the entire semiconductor layer can be fully depleted. In this condition, a channel is not formed, and even with a potential across the source and drain there is no current flow induced. This corresponds to the ‘off’ state.

Figure 2.2: The TFT structure and energy band diagram as viewed through the gate: (a) the structure of a TFT, (b) at equilibrium, $V_{GS}=0$, (c) depletion, $V_{GS}<0$, (d) accumulation, $V_{GS}>0$.

On the other hand, when a positive bias is applied to the gate, mobile electrons are attracted, and will accumulate close the semiconductor/ dielectric interface, forming a thin layer of “channel” near the dielectric layer. From the band diagram of view, the positive voltage drop across the dielectric and semiconductor layers, causes the conduction band in the semiconductor to bend downwards, which means that more delocalized electrons accumulated near the dielectric.

After the accumulation is established and the channel is formed, if a positive bias is applied between the drain and source ($V_{DS}>0$), the electrons would flow from the source to
the drain. There are two regimes depending on the magnitude of the $V_{DS}$. If the $V_{DS}$ is fairly small, (usually smaller than 200mV), the current between source drain is linear with drain voltage, the transistor acts like a resistor. This is the so called "linear" regime. In this regime, the charge density inside the channel is fairly uniform between the source and drain. The channel resistance depends on the channel sheet charge density, which is a function of the gate bias ($V_{GS}$).

When $V_{DS}$ increases, the accumulation near the drain decrease, and as $V_{DS}$ increase further, at some point, the region near the drain will be fully depleted. This voltage is called the pinch off voltage. Further increasing the $V_{DS}$ will not result in higher source drain current. The device enters the "saturation" regime.

In the linear regime ($V_{DS}<V_{GS}-V_T$), the "on" current $I_{DS}$ can be described by

$$I_{DS} = C_i \mu_{FE} \frac{W}{L} \left[ (V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

(2.1)

Where $C_i$ is the gate capacitance per unit area; $\mu_{FE}$ is the field-effect mobility; $W$ is the channel width and $L$ is the channel length. For very low $V_{DS}$, the quadratic term can be neglected, resulting in a linear relation between $I_{DS}$ and $V_{DS}$.

In the saturation regime ($V_{DS}>V_{GS}-V_T$), $I_{DS}$ is described by

$$I_{DS} = C_i \mu_{sat} \frac{W}{2L} (V_{GS} - V_T)^2$$

(2.2)

These equations are used for ideal TFTs. Although these equations fit quite well with most of the TFT behaviors, some of the assumptions such as $\mu_{FE}$ and $\mu_{sat}$ being independent of $V_G$ may not hold true sometimes, especially in oxide based thin film transistor, where $\mu_{FE}$
and $\mu_{\text{sat}}$ are highly dependent on the gate voltage, and $\mu_{\text{FE}}(V_G)$ and $\mu_{\text{FE}}(V_G)$ need to be used [17]. A detailed discussion on this will be present in section 3.8.

### 2.2 Transparent Conducting Oxides (TCOs)

Transparent conducting oxides (TCOs) are a class of materials which possess high electrical conductivity and optical transparency. From the electronic band structure point of view, traditionally, electrical conductivity and transparency are usually considered to be mutually exclusive [18]. This is because an insulator is a material with filled valence bands and empty conduction bands such that few states in the bandgap allow transparency. While a metallic material, the Fermi level lies inside the band with a large density of states to provide a large amount of carriers [19].

Actually TCOs are not 100% optically transparent and have lower conductivity compared to metal conductors. However, TCOs were found to have niche applications with sufficient transmission and moderate but useful electrical conductivity. For the common TCOs such as In$_2$O$_3$, ZnO SnO and CdO, undoped stoichiometric materials are insulators with band gaps larger than 3.1eV. These TCO hosts are degenerately doped to place the Fermi level up into the conduction band.

The first TCO cadmium oxide was found in 1907 and since then several other TCOs have been used for their optical and electrical properties, such as tin oxide (SnO$_2$), indium oxide (In$_2$O$_3$), indium tin oxide (ITO) and zinc oxide (ZnO). These TCOs are typically used in passive applications such as conductive windows, electrical pads for touch screens and other applications.
Most of the TCOs are n-type materials. The n-type conductivity has two origins: the creation of point defects (such as oxygen vacancies and/or metal interstitials) or extrinsic substitutional doping (typically on the cation site). The optical and electrical properties of TCOs are governed by the carrier generation mechanism.

When an oxygen atom is removed from the oxide creating a vacancy, two valence band bonds are removed, so the two electrons that would have occupied those bonds are available to occupy conduction band states. The lattice point corresponding to the oxygen vacancy can have a localized charge of 2+ (if the two free carriers are removed). The formation of the vacancy depends on the oxide free energy of formation [20].

For the metal interstitials case, a neutral metal atom residing in an interstitial site could easily be reduced to a more thermodynamically stable state in the process and donates x electrons to the conduction band. Typically x is one or two. Extrinsic doping is a traditional method to modulate carrier concentration. For example, in the ZnO: Al, an Al$^{3+}$ aluminum sits on a Zn$^{2+}$ site, resulting in one additional electron in the conduction band and a localized 1$^+$ ion on site. Similar behavior is seen in Tin-doped indium oxide [21].

Thus the point defect concentration can be modified by controlling:

- The deposition parameters during growth by changing
  - the oxygen partial pressure
  - the substrate temperature
  - the energetics of the impinging atom flux
- Post annealing in an oxidizing or reducing environment.
TCOs are used to make transparent thin film transistors (TTFTs) for two important reasons: First, TCOs are widely used in TTFTs as source, drain, and gate contacts, as well as interconnects. Due to the wide band gap of these oxide materials, it makes all oxide transparent circuits possible. Secondly, the TCOs can be used as the channel materials of TFTs. These channels can either be crystalline or amorphous. This dissertation will focus on the development of amorphous oxide semiconductors (AOSs), more specially, indium gallium zinc oxide based thin film transistors and circuits.

2.3 Development History of AOSs Based TFTs

As mentioned in section 2.1, the early exploration of TFTs were using oxide semiconductor as the channel layer. In the mid-1960s, there were two reports on TFTs fabricated using SnO$_2$ and In$_2$O$_3$ as channel materials [18,22], followed by the first proposal of a TFT fabricated using CdS in 1962 [11]. In 1968, a ZnO TFT was reported for the first time [23], which was fabricated using single crystal ZnO.

About 28 years later, the SnO$_2$: Sb TFTs combined with a ferroelectric gate was reported in 1996 [24]. The concept of transparent thin film transistors (TTFTs) was first proposed in that paper. In 2003, there were several reports of crystalline oxide TFTs using ZnO as the channel layer [7-8].

Among the TOSs, several groups selected ZnO as the first choices for transparent electronic devices in 2003. Since then ZnO TFTs have been studied intensively because ZnO is expected to exhibit better performance than a-Si:H and organic TFTs due to the large Hall mobility (200 cm$^2$ V$^{-1}$ s$^{-1}$) of single-crystal ZnO. However ZnO thin films can be very easily
crystallized during the deposition process, leading to the formation poly crystalline films with grain boundary defects. The existence of grain boundaries causes a non-uniformity problem in terms of \( \mu_{\text{FE}} \) and \( V_{\text{th}} \), decrease \( \mu_{\text{FE}} \) severely, and deteriorates the TFT performance and stability.

Another crucial problem of ZnO TFTs is that the carrier density is usually very high (typically \( \gg 10^{18} \text{ cm}^{-3} \)) even in the undoped state. This makes it difficult to control the channel conductance and the threshold voltage. It will also lead to the instability of TFT characteristics.

Therefore, it is imperative to search for other amorphous metal oxide semiconductors with device performance comparable to those of ZnO TFTs or even better. In 2004, Nomura et al. reported a new class of amorphous oxide semiconductors based on indium gallium zinc oxide (IGZO), and demonstrated that high performance transistors could be fabricated using amorphous IGZO thin film deposited even at room temperature [25]. The field effect mobility was 8.3\( \text{cm}^2 \text{V}^{-1} \text{s}^{-1} \) even in the amorphous state. This report attracted significant worldwide interest in industry and academia, because of its potential for high mobility, low process temperatures, excellent uniformity in device parameters, as well as good scalability to a large substrate size.

2.4 **Amorphous Oxide Semiconductors**

The most important feature that makes a semiconductor useful is the controllability of conductivity over a large range. For an amorphous semiconductor, it also has the advantages
of large area uniformity and low temperature process, which makes it possible to process on a wide range of rigid and flexible substrates.

The research on amorphous semiconductors started in the 1960s [19], and was highlighted by the innovation of amorphous silicon [17]. The development of amorphous semiconductors led to two new frontiers: “giant microelectronics”, (electronics based on circuits made on a large area substrate); and “flexible electronics”, (electronics devices made on soft, flexible substrates).

![Diagram](image)

**Figure 2.3**: Different formation mechanisms of bandgaps in semiconductors. (a) Bandgap of Si is formed of the energy splitting of levels. (b) Oxygen 2p and metal (M) ns orbital forms valence band maximum and the conduction band minimum, respectively, due to the Madelung potential. After reference [26].

However, for amorphous silicon, the properties of amorphous semiconductors are greatly degraded compared to their crystalline phases. While single crystalline silicon (c-Si) exhibits
an electron mobility of about 1500 cm$^2$ V$^{-1}$ s$^{-1}$, the electron mobility of hydrogenated amorphous silicon (a-Si:H) is less than 1 cm$^2$ V$^{-1}$ s$^{-1}$. This is because the carrier transport is controlled by hopping between localized tail-states and band conduction is not achieved. Thus the low mobility is associated with the intrinsic nature of the chemical bonding. Silicon is a covalent semiconductor, the conduction band minimum (CBM) and valence band maximum (VBM) are formed by anti-bonding (sp$^3$ $\sigma^*$) and bonding (sp$^3$ $\sigma$) states of Si sp$^3$ hybridized orbitals [26]. Its band gap is formed by the energy splitting of the $\sigma^*$- $\sigma$ levels, as shown in Figure 2.3(a). The sp$^3$ orbitals have strong directionality.

In amorphous Si, because the directional bonds are significantly distorted, the magnitude of the overlap between the vacant orbitals of the neighboring atoms is very sensitive to the variation in the bond angle. As a consequence, rather deep localized states would be created at somewhat high concentrations and thereby greatly degrade the drift mobility due to carrier scattering with these defects, as shown in Figure 2.4(a).

However, metal oxide semiconductors that contain post transition metal cations have very strong ionic bonds. After the charge transfer from metal atoms to oxygen atoms, the electronic structure is stabilized by the Madelung potential formed by these ions. The Madelung potential lowers the energy levels in the oxygen ions and raises those in the metal cations. Therefore, the CBM is primarily formed by the unoccupied ns orbital of the metal cations with isotropic spherical shape ($n$ is the principal quantum number, and $n$$\geq$5); and the VBM is primary dominated by the oxygen 2$p$ orbitals. The spatial spread of this vacant the $s$ orbital is so large that direct overlap between $s$ orbitals of the neighboring cations is possible in heavy metal oxides, and therefore the effective electron mass is small in these oxides.
Figure 2.4: Schematic orbital structure of the conduction-band minimum in (a) covalent semiconductors and in (b) ionic oxide semiconductors [25].

In the amorphous state of these metal oxide semiconductors, as shown in Figure 2.4 (b), direct overlap among the neighboring metal ns orbitals is still possible. The overlap is not greatly affected by the distorted metal-oxygen-metal bonds that commonly exist in an amorphous material. Therefore, AOSs exhibit very high electron mobilities even in the amorphous phase, close to the mobilities of their corresponding crystalline phases.
2.5 **Indium Gallium Zinc Oxide**

As discussed in section 2.3, after Nomura et al. reported TFTs fabricated using room temperature deposited a-IGZO as a channel layer [25], substantial research has been attracted to this area. Following the design principle discussed in section 2.4, i.e. post transition metal cations with electronic structure \((n-1)d^{10}ns^0\) would have high electron mobility even in the amorphous states. Several amorphous oxide semiconductors have been investigated, including amorphous In-Ga-Zn-O(a-IGZO), Zn-Sn-O (ZTO), In-Ga-O (IGO), In-Zn-O (IZO), Ga-Sn-Zn-O (GTZO) etc. However, among these amorphous materials, IGZO is the most commonly used in TFTs and is thought to replace a-Si for future generation displays, because it could easily achieve the desired balance between high mobility, good control of TFT and large area uniformity. Several materials that can be used to fabricate TFTs and applied in displays are compared in table 2.1.

Figure 2.5 summarizes the relationship among chemical composition, structure, mobility, and carrier density of an-IGZO film deposited at room temperature by pulsed laser deposition [27]. From figure 2.5(a), it is noticed that pure ZnO and In\(_2\)O\(_3\) can easily form crystalline films even when deposited at room temperature. (This is also observed in many other metal oxides, since they are difficult to form amorphous phases). On the other hand, the binary or multiple component oxide compounds forms amorphous phases when the oxide mixing ratio exceeds a threshold. In general, mixing of two or more cations having different ionic charges and sizes is effective for enhancing the formation of an amorphous phase and suppressing
crystallization. This is the reason why AOSs are basically multi-component systems, and this fact implies that we can find a wide variety of AOS materials.

Table 2.1: Comparison among several materials used in TFTs

<table>
<thead>
<tr>
<th>Materials</th>
<th>Mobility (cm²/Vs)</th>
<th>Transparency</th>
<th>Large area Uniformity</th>
<th>Process Temperature</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>a-Si:H</td>
<td>&lt; 2</td>
<td>Poor</td>
<td>Good</td>
<td>~250 °C</td>
<td>Low mobility, opaque, low current driving capability.</td>
</tr>
<tr>
<td>Poly-Si</td>
<td>30~100</td>
<td>Poor</td>
<td>Poor</td>
<td>&gt;250 °C</td>
<td>High mobility, high temperature process, opaque.</td>
</tr>
<tr>
<td>ZnO</td>
<td>10~50</td>
<td>Good</td>
<td>Poor</td>
<td>RT or &gt;250 °C</td>
<td>High mobility, high carrier concentration, easy to form grains.</td>
</tr>
<tr>
<td>organic materials</td>
<td>&lt;1</td>
<td>poor</td>
<td>good</td>
<td>RT</td>
<td>Low mobility, low cost, short life time.</td>
</tr>
<tr>
<td>a-IGZO</td>
<td>8~140(*)</td>
<td>Good</td>
<td>Good</td>
<td>RT</td>
<td>Transparent, high mobility, good uniformity, capable to drive high current.</td>
</tr>
</tbody>
</table>

(*)-- The mobility of IGZO also depends on In composition and deposition conditions.

In IGZO films, the high mobility is primarily defined by the fraction of In₂O₃ followed with that of ZnO. This can be proved by the fact that higher mobility samples are obtained in the In-rich a-IGZO films. This is consistent with the theory that both In³⁺ and Zn²⁺ have the
electronic configuration \((n-1)d^{10}ns^0\) \((n\geq5)\), but \(\text{In}^{3+}\) is larger than \(\text{Zn}^{2+}\), thus it plays a more dominant role.

Figure 2.5: (a) Amorphous formation and (b) electron transport properties of \(\text{In}_2\text{O}_3\)-\(\text{Ga}_2\text{O}_3\)-ZnO thin films. The values in (b) denote the electron Hall mobility \((\text{cm}^2/V \text{ s})\) with density \((10^{18} \text{ cm}^{-3})\) in parentheses. [27]

However, although the mobility of IZO could be higher, sometimes it is too conductive and hard to control the off state when it is used as the TFT channel. As shown in Figure 2.6, for the same deposition parameters, the carrier concentration and the leakage current of a-IGZO film is much lower than IZO. The incorporation of \(\text{Ga}^{3+}\) ions has two major effects: First is that the Ga-O bond is much stronger than In-O bond and Zn-O, and this would suppress generation of the free carriers (oxygen vacancies). Second, it helps to form the amorphous phase by introducing a different size cation.
Figure 2.6: Controllability and stability of a-IGZO and a-IZO films. (a) Relationship between carrier density and oxygen pressure during deposition. (b) Stability of film conductance after deposition. [28]

From Figure 2.6 (a), we can find that when deposited at different O$_2$ partial pressures, the carrier concentrations of IGZO thin films could vary from $10^{20}$ to $10^{15}$ cm$^{-3}$, which provides large controllability of the carrier concentration. Arun et al. reported that the conductivity of IGZO thin films varied with the deposition partial pressure [29]. The films grown in vacuum were metallic with a carrier concentration of $\sim10^{20}$ cm$^{-3}$. For semiconducting films grown between 5 and 80 mTorr, the conductivity decreased more than 4 orders of magnitude.

As stated earlier, transparency is an important advantage of IGZO thin film. The transmittance of IGZO thin film is usually greater than 80%. Thin film with lower carrier concentration has slightly better transparency than that with higher carrier concentration [30]. Tagaki et al. used the Tauc’s plots to determine the optical bandgap. The two IGZO bandgaps were determined to be $\sim3.1$ eV and $\sim3.3$ eV for the film with carrier concentrations
of $\sim 10^{13}$ cm$^{-3}$ and $\sim 10^{20}$ cm$^{-3}$, respectively. The absorption edge for the higher carrier concentration film was blue-shifted due to the Burstein–Moss (BM) effect, as the Fermi level in the conduction band in degenerated state rise, the optical absorption edge energy increases.

In summary, the high optical transmittance, high carrier mobility, good carrier concentration controllability, and uniformity make IGZO films useful as active material in transparent electronic devices.

### 2.6 Device Review-- Individual Transistors

In sections 2.1 and 2.3, the early development history and basic physics background of the AOSs based TFTs were briefly reviewed. In this section we will review some of the recent development of AOSs based devices with focus on the devices and circuits.

The pioneers of AOSs TFTs are Hosono’s group in Japan and Wager’s group in Oregon State University. In 2003, Nomura et al. reported the first transparent TFT using single crystalline IGO$_3$(ZnO)$_5$ annealed at 1400°C as a channel layer and 80nm amorphous hafnium oxide as a gate insulator. The device exhibited an $I_{on}/I_{off}$ ratio of $10^6$ and a field effect mobility of 80 cm$^2$ V$^{-1}$ s$^{-1}$ [9]. Following this report, the same group reported the first amorphous IGZO TFT fabricated at room temperature, (In: Ga: Zn = 1: 1: 1 atomic ratio) [25], with measured $\mu_{FE}$, $I_{on}/I_{off}$ and $V_T$ of 6-9 cm$^2$ V$^{-1}$ s$^{-1}$, $10^3$ and 1.6 V, respectively. The device characteristics were found to be stable during repetitive bending of the substrate sheet.
Since then several amorphous oxide semiconductors based TTFTs have been fabricated, employing different methods and techniques to improve the device performance. Some of these methods and techniques will be reviewed in the following section.

Research has been carried out to explore the relationship between chemical composition, the process parameters and the TFTs performance. Iwasaki et al. reported that the optimization of the atomic ratio and the oxygen particle pressure during the deposition [31]. Higher Ga content required lower O\(_2\) partial pressure; while higher In content required higher O\(_2\) partial pressure to produce functional TFTs. Mobility is observed to be strongly related to the indium content of the film. For their experiments, the best TFT performance was achieved with a compositional ratio of In : Ga : Zn = 37 : 13 : 50. This ratio resulted in a saturation mobility of 12 cm\(^2\)V\(^{-1}\)s\(^{-1}\), threshold voltage \(V_T\) of +3V and \(I_{on}/I_{off}\) ratio of 7×10\(^7\).

Some researchers made the effort to improve the ohmic contact of the oxide semiconductors [32-33]. Park et al. investigated Ar plasma treatment on the IGZO films [32]. By increasing the carrier concentration from \(10^{14}\) cm\(^{-3}\) to \(\sim10^{20}\) cm\(^{-3}\) upon Ar plasma, the contact resistance between the Pt/Ti (source/drain electrode) and a-IGZO (channel) was reduced from 1550 Ω-cm to 330 Ω-cm. Without the treatment, TFTs exhibited a moderate \(\mu_{FE}\) of 3.3 cm\(^2\)V\(^{-1}\)s\(^{-1}\), subthreshold swing of 0.25 V/decade, and \(I_{on}/I_{off}\) of 4×10\(^7\). After the Ar plasma treatment, the device performance significantly improved, an \(S\) value of 0.19 V/decade, \(I_{on}/I_{off}\) of 10\(^8\), as well as a \(\mu_{FE}\) of 9.1 cm\(^2\)V\(^{-1}\)s\(^{-1}\), were recorded. Similarly, Ahn et al. proposed a H\(_2\) plasma method to improve the contact resistance, with incorporated hydrogen acting as shallow donors. [33]
The long term stability and reliability of TFTs are the most important issues before this technology can be applied in mass production. The stability of AOSs based TFTs has been intensely studied in recent years. Some results indicated that threshold voltage $V_{th}$ under positive bias stress tests would exhibit a positive shift, which could be attributed to the trapping of positive charges in the (A) gate insulator, (B) gate/channel interface, (C) inside the bulk of channel layer, (D) back-channel surface or (E) creation of acceptor type deep traps [34-35].

The effect of bias stress and threshold voltage shift were studied by several groups. Lee et al. reported the time dependence of $\Delta V_{th}$ followed a stretched exponential law [34]. While Arun et al. reported that the time dependence $\Delta V_{th}$ followed an exponential law [35]. In his model, the threshold voltage shift is proposed as:

$$\Delta V_{th} = r_0 \log\left(\frac{t}{t_0}\right)$$

Where $r_0$ is a decay rate constant, which is proportional to the product of $N_{tr}$ (cm$^{-3}$) and $\lambda$ (cm). $N_{tr}$ is the density of traps in the dielectric, and the tunneling constant $\lambda$ is the product of the applied gate voltage and dielectric material parameters. In this model, negative charge injection induced by the positive gate bias was responsible for the positive $\Delta V_{th}$ under stress conditions.

Hsieh et al. reported the self heating effect of IGZO based TFTs [36]. They found that the threshold voltage shift is linear with the drain stress power. And they claimed that $V_T$ instability was dominated by the self-heating effect. A wider channel width can bring a more significant self heating effect because the heat generated within the channel is more difficult
to dissipate. During self heating stresses, gate bias can be considered to serve as the trapping force, and drain bias can be considered to serve as the current driver and, therefore, the heat generator.

Joeng et al. studied the effect of environmental ambient, including oxygen and water on the gate bias stability of IGZO TFTs [37-38]. They modeled the oxygen adsorption by the following simple chemical reaction:

\[ \text{O}_2 \text{(gas)} + e^- = 2\text{O}^- \text{(solid)} \]

The case is similar for the water molecule. According to the field induced adsorption/desorption model they proposed, under positive bias stress, the accumulated electron density in the channel region increased and the absorbed concentration of \([\text{O}^-]\) would also increase, which would raise the \(V_{th}\) of the transistor.

In order to improve the stability and reliability, two major methods are used: one is thermal annealing the other one passivation. For example, Kamiya et al. reported that thermal annealing could remove weak chemical bonds, especially Zn-O related bonds and form a more stable a-IGZO [39]. They also claimed that annealing is more effective in wet oxygen than in dry oxygen, which was attributed to the stronger oxidation power provided by \(\text{H}_2\text{O}\) molecules. To solve the back gate absorption, more recent papers employed a gas-tight passivation layer on top of the channel layer. These passivation layers are usually made of \(\text{SiO}_2\) [40], \(\text{SiN}_x\) [41], \(\text{Al}_2\text{O}_3\) [42] or \(\text{TiO}_x\) [43].

Solution based inorganic metal oxide TFTs have also been investigated. Compared to conventional devices fabrication methods using deposition, photolithography, etching and lift off, this method provide the advantages of low cost and a fast fabrication process.
Ohya et al. reported the first solution based ZnO TFT [44], with mobility of 0.2 cm$^2$V$^{-1}$s$^{-1}$ and the current on/off ratio of $10^7$. However, one limitation of their experiment is their process requirement for very high annealing temperature, as high as 900˚C.

Due to the excellent performance of the IGZO system, solution based IGZO TFTs have been reported after 2009 [45-47]. In order to reduce the annealing temperature, Yang et al. report nano-particle IGZO TFT using the hydrothermal method and laser annealing to improve the device performance. The solution was then heated in an autoclave at 180 °C under a pressure of 10 atm for 1 h, and the thin film was post baked at 95 °C. Illumination by a Nd:YAG (355nm) laser at a dose of 740 mJ, the IGZO thin film became poly crystallized. They got the best mobilities of 7.65 2 cm$^2$V$^{-1}$s$^{-1}$ and on/off current ratio of 2.88×10$^7$.

In 2012, Kim et al. reported using deep ultraviolet photochemical method to active the sol–gel spin coated metal oxide films formed at room temperature [48]. They found that deep-ultraviolet irradiation induced efficient condensation and densification of oxide semiconducting films. The device performance (transistor mobility and operational stability) fabricated by this method were comparable to the devices fabricated by thermally annealed thin films. The photo-annealed TFTs have shown field-effect mobilities of 8.766±0.98 cm$^2$V$^{-1}$s$^{-1}$ for IGZO, 4.436±0.59 cm$^2$V$^{-1}$s$^{-1}$ for IZO, and 11.296±1.62 cm$^2$V$^{-1}$s$^{-1}$ for In$_2$O$_3$. The gate dielectric was 35 nm thick ALD deposited Al$_2$O$_3$. These devices were very stable after bias stress. The threshold voltage shifted 1.12V after a gate-bias stress time of 10,000 s.
2.7 **Amorphous Oxide Semiconductors Based Circuits**

Most of the research on the AOSs based devices was focused on individual transistors. There are only a few reports about AOSs based circuits. That is one of the reasons we chose this area as one of the major research areas of this thesis. Most of the recent reports focused on the fabrication and characteristics of inverters and ring oscillators.

The inverter is the basic building block of circuits, in which the output is opposite to input signal. In CMOS circuit, it is constructed by a p-type TFT and a n-type TFT. However, due to the lack of p-type AOSs based TFTs, the inverter is constructed by 2 n-type TFTs, one acting as load resistor the other is the drive transistor.

A ring oscillator (RO) is used to evaluate the operation speed of the TFTs. A RO is constructed by connecting an odd number of inverters in series and tying the output of the final inverter back to the input of the first inverter as shown in Figure 2.7(b).

![Inverter and Ring Oscillator Diagrams](image)

Figure 2.7: (a) Schematic of an inverter, (b) 5-stage ring oscillator. (T_L is the loading transistor, T_D is the driving transistor.)
The 1st transparent ring oscillator was reported by Presley in 2006 [49]. It was a five-stage ring oscillator based on IGO TFTs. The gain of the inverter was measured to be ~1.5 and the maximum frequency was measured to be 2.3 kHz with a 30V supply and 9.5 kHz with 80V supply. The relative low operation speed was due to the large gate-source/gate-drain overlap of 200 µm.

Arun et al. reported a whole transparent ring oscillator based on IGZO TFTs [50]. The devices were deposited on ITO/glass substrate and ALD deposited Al₂O₃ was used as the dielectric layers. PLD deposited ITO was used as the source/drain and interconnected layers. The field-effect mobilities of the TFTs were measured to be about 15 cm² V⁻¹ s⁻¹. The maximum operation frequency of the ring oscillators was 2.1 MHz with a supply voltage of 25 V, corresponding to a propagation delay of < 48 ns/stage. It is claimed the ring oscillators they reported were the fastest all-transparent oxide semiconductor circuits up to their report date.

Zhao et al. reported 15-stage ZnO TFT ring oscillators fabricated on flexible polyimide substrates [51]. The channel layer was ZnO thin film deposited by plasma enhanced ALD (PEALD) at 200 °C. Field-effect mobility of the ZnO TFT was reported to be 20 cm² V⁻¹ s⁻¹. The maximum operation speed was > 2 MHz with a supply voltage of 18 V, corresponding to a propagation delay of < 20 ns/stage. These devices were claimed to be the fastest oxide semiconductor circuits on flexible substrates up to their report date.

Lim et al. reported an OR gate fabricated on a glass substrate based on double gate single IGZO transistors [52]. The double gate (DG) configuration was used and was reported to improve mobility and on to off current ratio compared to their bottom gate devices. The DG-
TFTs showed a saturation mobility of 16.9 cm$^2$V$^{-1}$s$^{-1}$, drain current on/off ratio of 1*10$^6$, sub-threshold gate voltage swing of 0.33 V/decade, and threshold voltage of 1.25 V. However, their OR gates operated at relatively low frequency, only about 5 Hz was demonstrated.

There have also been research efforts to realize complementary oxide circuits possible.

In 2011, Martins et al. reported complementary inverters with and on paper substrate. The p-TFTs employed non stoichiometric Tin oxide (SnO$_x$, x<2) as the channel layer [53]. The n-TFTs employed indium gallium zinc oxide (IGZO) as the channel layer. The paper was used as substrate and gate dielectric layer. The gate material indium zinc oxide was deposited on the other side of the paper. The IGZO layer was 40nm thick and the SnO$_x$ was 8 nm thick. Ni/Au was used as the source drain and contact layer. The TFTs exhibits electrons and hole mobilities higher than 21 and 0.8 cm$^2$V$^{-1}$S$^{-1}$. Even though these devices had large leakage current, the inverters did show functional inverter voltage transfer curves. The inverter exhibited a logic output swing larger than 85% of the $V_{OH}$. For the $V_{DD}$=17V, noise margin (NM) $NM_H$ was about 9.8, $NM_L$ was about 1.0V. The power consumption was 32 pW per inverter. It should be noticed that these circuits were not transparent. However, it demonstrated complementary circuits using all oxide materials. And the implementation of CMOS on paper created an opportunity for light weight, low cost, and fully recyclable complementary circuits, i.e., green electronics.

In 2011, Nomura et al. reported complementary inverters using a same channel material—SnO [54]. The devices were fabricated on a SiO$_2$/Si substrate with the maximum process temperature of 250 ºC. The saturation mobilities of p-channel TFTs and n-channel were measured to be $\sim$ 0.81 cm$^2$V$^{-1}$S$^{-1}$ and 5*10$^{-4}$ cm$^2$V$^{-1}$S$^{-1}$, respectively. The inverter
operated with a maximum voltage gain of ~ 2.5. The bandgap of SnO is 2.7eV which is not fully transparent for the visible spectrum. The double gate configuration was used. The bottom gate was a heavily doped silicon substrate. A top gate electrode was deposited on top of the channel layer to prevent the SnO oxidizing into the n-type SnO₂. A ~330nm thick Y₂O₃ layer was used as top gate dielectric layer. This is the first demonstration of an oxide-based complementary-like inverter using a single channel material, which allows simple fabrication of complementary logic circuits based on oxide TFTs.

More details about p-type oxide semiconductors and their devices research status will be reviewed in next section.

2.8 P-Type Amorphous Oxide Semiconductors and Devices

2.8.1 Motivation and Challenges

Since the emergence of n-channel transparent thin film transistors (n-TTFTs), researchers have been working hard to develop robust p-channel TTFTs. While the researches on n-TTFTs have attracted a lot of attention and the device performances of n-TTFTs has improved in the past decade, the development of robust p-channel TTFTs remains a considerable challenge. This severely limits the applications of transparent oxide semiconductors. The presence of both active layers makes circuit design more flexible and enables low power-consumption circuits similar to complementary metal-oxide-semiconductor (CMOS) technology.
In this section, the working principle of p-type conducting oxide, p-type oxide semiconductor materials and some recent developments on p-channel TFTs will be reviewed and discussed.

The key problem for developing the p-type TFTs is that developing the p-type oxide semiconductor thin film suitable for the p-TFT channel layer remains challenging. However there has been some research about the ‘bulk’ p-type transparent conducting oxides aiming to developing the p-n optoelectronic devices. It is possible that p-type oxide semiconductors thin films could be modified from these bulk p-type transparent conducting oxides (TCOs). Because p-type TCOs for optoelectronic devices require transparency (band-gap>~3.1 eV), high mobility, high carrier concentration, high conductivity, while the thin film for p-type TTFT requires transparency, high mobility, controllable or relative low carrier concentration.

For most of the n-type TOSs, the conduction band minimum (CBM) is made of a spatially spread spherical metal s orbital. Therefore, electrons in the metal oxides have small effective masses, and high electronic conduction is possible if high-density electron doping is achieved. In contrast, the valence band maximum (VBM) is made of oxygen 2p orbitals, which are rather localized, leading to small hole effective masses. Furthermore, the dispersion of the valence bands tends to be small, thus the VBM level is so deep that hole doping is difficult. That is the reason that p-type TOSs are much more difficult to attain [56].

2.8.2 P-Type Conducting Oxide Materials and Their Structures

Hosono et al. proposed [57] that the good p-TCO’s conduction could be obtained by increasing the dispersion of VBM. This could be achieved by three methods: (i) decreasing
the nearest neighboring oxygen–oxygen distance, (ii) using hybridization of metal orbitals whose energy levels are close to those of O 2p (Figure. 2.8 (B)), or (iii) employing more extended orbitals for anions (Figure. 2.8 (C)).

Later, $3d^{10}S^0$ configuration of $\text{Cu}^+$ was chosen as a candidate because it provides a large band gap and the means for the introduction of holes through partial oxidation of $\text{Cu}^+$. Up to date the most important the p-TCOs could be summarized into the following 4 categories:

Type A: Delafossite structure copper oxides: $\text{CuMO}_2$ (M=Al, Ga, In, Sc, Y, La)

The first realization of wide band gap p-type oxide is $\text{CuAlO}_2$, which was reported by Kawazoe et al. in 1997. It exhibited band gap>3eV, positive Seebeck coefficient (+183 $\mu$VK$^{-1}$), conductivity of 1Scm$^{-1}$, and carrier mobility close to 10 cm$^2$ V$^{-1}$ s$^{-1}$. However, unfortunately, this high mobility has not been reliably repeated.

Figure 2.8. Simplified electronic structures in oxides (A) In typical n-type TOS, conduction band minimum is composed mainly of metal s orbitals and valence band maximum (VBM) of O 2p orbitals. (B) In Cu-based p-type TOSs, VBM is made of hybridized orbitals of Cu 3d and O 2p, which raises the energy level of VBM and forms more conductive hole transport
paths. (C) In oxychalcogenides, hybridization of VBM enhanced by intervention of the chalcogen p orbitals. The energy level of VBM is raised and hole effective mass is reduced as the atomic number of the chalcogenide is increased. [57]

The delafossite structure consists of an alternating stack of Cu$^+$ ion layers and MO$_2$ octahedral layers along the c axis (as shown in Figure 2.9a). These O-Cu-O sticks are isolated, producing no Cu-O-Cu- linkages. The Cu-Cu separation is relatively long. In these structures with large M atoms, additional O atoms could be inserted between Cu atoms by carefully heating samples in the air, providing the Cu-O-Cu linkages. The Cu$^{1+}$ becomes locally oxidized to Cu$^{2+}$. This process will improve the conducting but also reduce the transparency.

Figure 2.9: Structure of (a) delafossite structure Copper oxides [58]. (b) Structure of SrCu$_2$O$_2$ [59]

Type B: Ternary copper oxide MCu$_2$O$_2$ (M=Ca, Ba, Mg, Sr)
The ternary copper oxide $\text{MCu}_2\text{O}_2$ ($\text{M}=\text{Ca}, \text{Ba}, \text{Mg}, \text{Sr}$) was also reported as a transparent conductor [59-60]. Undoped and K-doped polycrystalline SrCu$_2$O$_2$ films were grown by pulsed laser deposition. The band gap is 3.3 eV, conductivities are $3.9 \times 10^{-3}$ and $4.8 \times 10^{-2}$ Scm$^{-1}$, respectively. For the K-doped film, the carrier concentration is $6 \times 10^{17}$ cm$^{-3}$ and mobility is 0.5 cm$^2$ V$^{-1}$ s$^{-1}$ [59].

The structure of MCu$_2$O$_2$ is shown in Figure 2.9 (b). Compare to the delafossite structure, the conductivity is higher and the carrier mobility is higher. Zig-zag chains of $–\text{Cu-O-Cu}$ linkages extend along a axis of the tetragonal cell, providing a conduction path for holes.

Type C: Copper oxychalcogenide and Copper Fluoride chalcogenides

The oxide chalcogenides ($\text{LuCuOQ; Ln=La, Ln}=$Lanthanide, $\text{Q=S, Se, Te}$) and Fluoride chalcogenides ($\text{MCuFQ; M=Ba, Sr, Ca}$) were chosen to approach the principle (iii) as shown in Figure 2.8 (c). This structure employed chalcogenides to form VBM largely hybridized with Cu$^+$ 3d$^{10}$ orbitals. These materials are layered structures, where edge-shared CuS4 tetrahedra forms sheets in the ab plane that are widely separated by [LnO] or [MF] layers. Carrier transport is confined to the two dimensional Cu-Q sheets.

LaCuOQ exhibits good $p$-type conduction. Undoped LaCuOS have a hole concentration of $\sim 10^{19}$ cm$^{-3}$ and Hall mobility of $\sim 0.5$ cm$^2$ V$^{-1}$ s$^{-1}$ at room temperature. Mobility becomes larger as Se content increase in LaCuO(S$_1-x$Se$_x$ ) and reaches $\sim 8.0$ cm$^2$ V$^{-1}$ s$^{-1}$ in LaCuOSe [61]. This value is comparable to that of $p$-type GaN:Mg. Another important property of these materials is that degenerate $p$-type conduction is achieved in Mg-doped LaCuOSe. This is the first degenerate $p$-type conductor. The band gap of LaCuOS and LaCuOSe are 3.1eV and 2.7eV, respectively.
BaCuSF and BaCuSeF exhibit similar structures and properties. The band gaps are 3.2eV and 2.9eV respectively [62]. The room-temperature Seebeck coefficient and electrical conductivity of undoped BaCuSF pellets were 56 µV/K and 0.088 Scm⁻¹, and 32 µV/K and 0.061 Scm⁻¹ for the BaCuSeF. They also found that the conductivity could be controlled by doping. The highest conductivities were 82 Scm⁻¹ for Ba₀.₉K₀.₁CuSF and 43 Scm⁻¹ for Ba₀.₉K₀.₁CuSeF.

Type D: Spinel ZnM₂O₄ (M=Co, Rh, Ir)

The transition metal ions with 4d⁶ configurations located in an octahedral crystal field have a low-spin configuration in the ground state, which could be regarded as a “quasi-closed shell” configuration. Therefore they are expected to behave similarly to Cu⁺ ions with 3d¹⁰ closed shell configurations and to enhance the dispersion of the valence band. The p-type films of ZnM₂O₄ were reported [63]. The optical and electrical properties are summarized in table 2.2. All the films are deposited by PLD in high oxygen pressure. The problem of spinel ZnM₂O₄ is that the band gap is not large enough for optical transparency.

<table>
<thead>
<tr>
<th>ZnM₂O₄</th>
<th>T%</th>
<th>E gap (eV)</th>
<th>Conductivity (S/cm)</th>
<th>Seebeck (µV/K)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ZnCo₂O₄</td>
<td>26.1</td>
<td>2.26</td>
<td>0.39/0.61</td>
<td>+131.4</td>
</tr>
<tr>
<td>ZnRh₂O₄</td>
<td>54.8</td>
<td>2.74</td>
<td>2.75/2.83</td>
<td>63.4</td>
</tr>
<tr>
<td>ZnIr₂O₄</td>
<td>60.8</td>
<td>2.97</td>
<td>3.39/2.09</td>
<td>53.9</td>
</tr>
</tbody>
</table>
2.8.3 Recent Development of Materials for P-TTFTs

Before 2008, almost all development of the p-type transparent oxide focused on the “bulk” transparent conducting oxide for the use for optoelectronics devices like p-n junction LEDs. In those applications the p type material required transparency, high mobility and high carrier concentration. In 2008 Hosono’s group published a few papers trying to develop p-type transparent oxide thin film towards the p-channel TTFTs. This subsection will briefly review these recent developments of p-channel devices and complementary circuits.

Y. Ogo et al. [64] reported a p-type oxide semiconductor TFT using SnO as the channel layer. The single crystalline SnO was deposited on (001) yttria-stabilized zirconia (YSZ) substrates by PLD at 575°C, with a hole density of 2.5×10^{17} cm^{-3} at room temperature. The p-channel TFT exhibited field-effect mobilities of 1.3 cm^2 V^{-1} s^{-1}, on/off current ratios of 10^2, and threshold voltages of 4.8 V.

The main limitation of this material is that the band gap is not large enough, as 2.7eV is not transparent to the whole visible spectra. Also the on/off ratio is small, indicating a large off current. This is due to the large carrier concentration (>10^{17} cm^{-3}).

H. Hiramatsu et al. [65] explored the structural optical and electrical properties of copper-based chalcogenide thin films, including CuAlS₂, CuGaS₂, CuInS₂, CuAlSe₂, CuGaSe₂, CuInSe, and simple Cu₁.₆S and Cu₁.₇S. From the point of p-channel TTFT, there are several interesting points in this paper. (1) These p-type thin films were deposited by PLD at room temperature and chalcopyrites were shown to be amorphous or nanocrystalline and showed reasonable holes mobility or high conductivity. This proves transparent soft electronics are totally possible. (2) The electrical conductivities of the chalcopyrite films could be tuned...
from $<1.4 \times 10^{-2}$ S/cm to 13 S/cm by changing the flow of H$_2$S/Ar pressure. Also the hole concentration could be controlled by introducing oxygen gas and H$_2$S gas during the thin film deposition. The conductivity decreases with increasing the oxygen partial pressure, suggesting that the decrease in the conductivity originates largely from the decreased hole concentration. (3) Very high conductivities were obtained from the Cu$_{1.6}$S and Cu$_{1.7}$S thin films. The conductivity of Cu$_{1.7}$S deposited on polyethylene terephthalate (PET) could reach as high as $7.3 \times 10^3$ S/cm, which is even higher than the low temperature ITO. Therefore it may be a possible hole injection electrode in the future transparent electronics.

In their experiment, however, no TFTs show current modulation by the gate bias. They addressed the reason to sub gap states density higher than the carrier density introduced by gate voltage. However, another possible important reason might be the carrier concentration is too high, larger than $10^{22}$ cm$^{-3}$. In such a high carrier density it is almost impossible to turn off the device.

T. Mine et al. [58] showed the possibility to control the carrier concentration of CuCaO$_2$ by varying the oxygen pressure during the thin film deposition. The single crystalline CuCaO$_2$ thin film was epitaxially grown by PLD at a substrate temperature between 725$^\circ$C and 780$^\circ$C. By controlling the oxygen partial pressure from 3 Pa to 6.5Pa, the electrical conductivity of the as-deposited films could range from $3.3 \times 10^{-5}$ S/cm to $1.7 \times 10^{-2}$ S/cm, and the carrier concentration could be controlled from $10^{14}$ cm$^{-3}$ to $10^{17}$ cm$^{-3}$. They also found that annealing could help to improve the surface smoothness and increase the hole mobility. Post annealing at 1215 $^\circ$C reduces the surface root-mean-square roughness from 1.4nm to 0.56nm and increases the hole mobility from 0.2 cm$^2$V$^{-1}$s$^{-1}$ to 0.8 cm$^2$V$^{-1}$s$^{-1}$. They
tried to make a TTFT using the CuCaO$_2$ as the channel layer but the TTFT was not functional, because of low mobility.

Additionally, K. Matsuzaki et al. [66] grew high mobility Cu$_2$O thin film and fabricated TFTs. The Hall mobility of single phase epitaxial films was obtained as high as 90 cm$^2$ V$^{-1}$ S$^{-1}$. However, the maximum field effect mobility is only 0.26 cm$^2$ V$^{-1}$ S$^{-1}$, two to three orders smaller than the Hall mobility. Their results showed that the Fermi level in the channel is strongly pinned and a large amount of trap states exists in the channel and/or the channel-gate insulator interface. They attribute the extra trap states to a slight non-stoichiometry of Cu$_2$O or to the device fabrication process. Other issues include that the Cu$_2$O band gap of is only 2.17eV, not transparent for the whole visible spectrum and the on/off current ratio is very low ~6.

As reviewed in last section. Martins et al. and Nomura et al. reported complementary inverters using SnO$_x$ and SnO as the p-channel materials. And they demonstrated that complementary oxide circuits are possible. Though these early devices did not show robust device performance, these results demonstrated the possibility and further research effort may further improve the devices performance.

2.9 Oxide Transistors for Display Applications

As previously discussed, amorphous metal oxide based TFTs have a close relationship with displays, due to the inherent advantages of this technology. First of all, it is transparent, low temperature process compatible and, has good uniformity and high mobility, which makes it very suitable for next generation large screen LCDs, transparent displays and
flexible displays. Secondly, the higher mobility makes it possible to drive OLED based displays, which require high drive current.

A 6.5 inch flexible full color AMOLED display on polymer substrate driven by a-IGZO TFTs was demonstrated by J. S. Park et al from Samsung Mobile displays in 2009 [67]. The individual a-IGZO TFTs exhibited a field-effect mobility of 15.1 cm² V⁻¹ S⁻¹, a subthreshold slope of 0.25 V/decade, and a threshold voltage of 0.9 V were obtained. The gate bias stress showed that devices on PI substrates were very stable under 15V stress and high degrees of spatial uniformity. TFT samples on 10 µm thick PI substrate withstood bending down to R=3 mm under tension and compression without any performance degradation. The overall thickness of the AMOLED display panel was less than 0.1 mm. It is top-emissive OLED structure and has aperture ratio of 53%, resolution of 85 ppi. The simplest circuit includes two TFTs and one storage capacitor that drive each pixel.

In 2008, Ito et al. demonstrated the application of amorphous oxide thin film transistor (TFT) to electronic paper [68]. They proposed a low cost printing process. The source drain and electrodes (Ag) were printed onto the a-IGZO layer. The sputtered-deposited SiON film was utilized as a gate insulator and passivation layer for the bottom gate IGZO TFTs. The TFTs show an on/off ratio of more than 7 orders of magnitude and field effect mobility of 2.8 cm² V⁻¹ S⁻¹. A 4” bottom gated IGZO TFT array was integrated with an electrophoretic front plane, performing with a resolution of 200 ppi and the number of the pixel of 640 x 480.

There are several companies working on oxide TFTs for display applications. And there is new research progress in the recent years.
Thanks to the high mobility and large area uniformity of the oxide TFTs, Samsung demonstrated the high-end display— the 70” ultra-definition (UD) LCD 3DTV with a high scanning frequency (240 Hz) in 2010 [69].

In 2011, Samsung announced that it had started mass production of a 22” transparent LCD panel [70]. Instead of using a backlight, the transparent displays rely on ambient light and consume 90% less electricity than the conventional LCD panel. These displays exhibit a 1680 × 1050 resolution, a contrast ratio of 500:1 and a transparency of 15%.

In 2012, Sharp and Semiconductor Energy Laboratory (SEL) jointly developed a new IGZO structure for display applications [71]. They named this new crystalline IGZO structure as CAAC (C-Axis Aligned Crystal) structure. They claimed that the CAAC-IGZO TFT was more stable compared to conventional amorphous IGZO TFT, especially under gate bias temperature stress with light irradiation. Under 80°C, 2000 second light irradiation, +30V gate bias, only resulted in $\Delta V_{th} = +0.27V$ and -30V negative gate bias only resulted in $\Delta V_{th} = -0.23V$.

At the same time period, Sharp announced the production of IGZO based LCDs [72]. The first IGZO based LCD displays are now available in consumer devices, including two Sharp devices and the new Asus PadFone [73]. The 4.9 inch IGZO based LCD display offers a 1280x720 pixel resolution. Sharp also revealed some other sample panel specification: 32 inch- 3840x2160 (140 ppi), 10 inch- 2560x1600 (300 ppi), 7 inch- 800x1280 (217 ppi).

Wellenius et al. reported an active matrix pixel constructed by two IGZO TFTs and europium doped IGZO thin film electroluminescent (TFEL) phosphor [74]. In this design, one TFT (T1) has as inputs a row (drain) and column (gate) voltage signal. The gate of the
other TFT (T2) is connected to the source of T1, and the source of T2 is grounded. Two IGZO TFTs were used to control the row and column signal while the TFEL devices is connected to the high AC voltage source. The IGZO driving TFTs showed good transient response under 120Hz power supply, demonstrating IGZO as a viable material for active matrix backplanes. The research results indicate these IGZO TFTs, could be used in modern LCD displays operating at 120 Hz.

The transparent TFEL device used a novel amorphous Eu:IGZO wide bandgap thin film as a phosphor. This device demonstrates electroluminescence characteristic of the Eu$^{3+}$ dopant, resulting in emission comparable to that of earlier red TFEL devices. A low EL threshold voltage (~40 V) was observed. This TFEL device was successfully integrated with and modulated by TFTs under gate voltage in the range of 8 to 16V, using the TFT channel as a ground path for the TFEL. Their experiments showed that channel geometry is an important consideration for TFEL modulation as the length was observed to affect several facets of the TFEL luminance. These results indicate the viability of IGZO TFTs for active matrix display applications and also demonstrate a novel AOS EL phosphor.
Chapter 3
EXPERIMENTAL TOOLS AND DEVICES
CHARACTERIZATION

This chapter will discuss some of the important experimental tools used to fabricate devices and the device characterization. The tools that were used to deposit the thin films and fabricate devices include pulsed laser deposition (PLD), plasma-enhanced chemical vapor deposition (PECVD), atomic layer deposition (ALD), E-beam evaporation, photolithography, lift-off, etching and focused ion beam (FIB). Finally the device’s process steps, device parameter extraction and device characterization will be presented.

3.1 Vacuum Deposition Techniques

3.1.1 Pulsed Laser Deposition

The IGZO channel layer and ITO layers in this work were deposited by a high vacuum pulsed layer deposition (PLD) system at NCSU.

Pulsed laser deposition is a common technique to deposit high quality thin film materials. This technique employs a high power laser to heat, ionize and evaporate material from the surface of the target. This ablation process therefore produces luminous plasma that expands rapidly away from the target surface. The ablation material is then collected by the substrate properly placed in front of the target. Due to the high energy, the atoms and ions have large kinetic energy which improves materials quality as the surface is constructed.
There are several advantages of using PLD over other thin film deposition techniques.

1) PLD is able to transfer identical stoichiometric composition of the target to the film. The high energy from the radiation is absorbed by only a thin layer of the target surface. And the pulse is very short. The surface of the target can rise to more than one thousand degree Celsius, while the bottom of the target remains unheated. Such nonequilibrium heating produces a flash of evaporants that deposit on the substrate, producing a film with composition identical to that of the target surface.

2) PLD is an extremely clean process. Since energy source is outside the chamber, deposition could be in vacuum or reactive gases environment.

3) The use of a carousel to house several targets in the PLD system, making it is relative easy to deposit multiple layers without breaking the vacuum. At the same time, since the gases don’t affect the laser. It is also possible to deposit multiple films with different gas environments.

However, there are a couple disadvantages to PLD. First the plume is relatively small. It is difficult to get thin film uniformly over a large area, which limits its industry application. Usually PLD systems are used in research labs and sputtering is used commercially. Second, the ablated thin film may contain macroscopic globules of molten material, and form particles on the substrate.

To overcome these problems, in this study, most of the samples were deposited on the substrates of the size ~15 mm x 15 mm. Fairly uniform films were attained by controlling the deposition parameters and rotating the substrates. Also lower laser energy was used when depositing IGZO and ITO to reduce the number of particles.
The Schematic of a PLD system is shown in Figure 3.1. There are 4 major components for a basic PLD system:

1) A laser system used as the energy source to ablate ceramic targets of the desired composition.

2) The vacuum chamber containing the target holders and substrate holders.

3) Optical system that consists of a series of lens, aperture and mirrors needed to guide the laser beam into the chamber to ablate the target.

4) Pumping system and gas feedthrough to provide the high vacuum and the background gas used during the deposition. A mechanic pump is used for rough pumping and a turbo pump is for high vacuum pumping.

The PLD system at NCSU is from NEOCERA Inc. A Lambda-Physik Compex 201 KrF (248 nm) excimer laser is used as energy source. Laser power is typically between 150 and 300 mJ per 20 ns pulse, with a pulse rate of 10 Hz. The power density at the target is estimated to be ~3 J/cm². The chamber operating pressure is controllable from $10^{-8}$ Torr to 100-500 mTorr. The chamber background gases are oxygen or argon. By changing oxygen partial pressure the carrier concentration in IGZO or ITO can be controlled. The gas flows are regulated by a MKS mass flow controller and the desired chamber pressure is maintained by a variable-position gate valve. Samples are clipped onto a substrate holder that rotates during the deposition to improve the film uniformity. The targets are mounted on a carousel and are rastered and rotated to avoid pitting at the same point.
The IGZO targets are prepared in NCSU. There are different targets with different compositions, the most common used as the TFT’s channel in this study is $\text{In}_2\text{Ga}_3\text{Zn}_5\text{O}$ (In:Ga:Zn=1:1:5). The targets are prepared according to this procedure: The raw oxide powders were mixed according to desired composition. The mixed powders were calcininated at 1000 °C for 2 hours, before being ground and pressed up to 5000 psi into a 1 inch ceramic disk. Then the target is sintered at 1400 °C for 6 hours in air. The ITO target was bought from commercial vendor. All the depositions in this study are carried out at room temperature.
For a typical deposition, samples and targets are loaded into the PLD chamber which is then pumped down to a base pressure of ~5×10^{-7} Torr. The target is then pre-cleaned by 500 pulses at 5Hz and 500 pulses at 10Hz, with the shutter blocking the substrates. The laser frequency and laser power are kept at 10 Hz and 150 ~ 170mJ/pulse in this study. During the depositions, the target is rotated and rastered to avoid target pitting. The substrate holder is also rotated during the growth to improve film uniformity. The oxygen partial pressure during deposition was varied between 5 mTorr and 100 mTorr for IGZO and ITO thin films. The number of pulses was varied, depending on the desired film thickness. A typical IGZO channel layer is about ~40nm thick in this study, and requires 6,500 laser pulses. The substrate holder includes a heater, which can heat the substrate to up to 1000 °C. However, in this study, the substrate holder was kept at room temperature when depositing IGZO and ITO thin films.

3.1.2 Atomic Layer Deposition

Atomic layer deposition (ALD) has become an important technique for depositing thin films for some applications. One of the most important motivations of recent development of ALD is that it is an effective tool to deposit high quality high k dielectric thin films.

ALD is a technique that can deposit thin films on a variety of substrates in a precise way. The principle is very similar to other chemical vapor deposition (CVD). The reactions are gas phase chemical reactions. ALD breaks the CVD reaction into two half reactions, by keeping the precursor materials separate. For each reaction cycle, one precursor pulse comes in and adheres on to the substrate surface, then a purge gas (usually nitrogen or argon) removes the
excess precursor. Then another precursor comes in and reacts with the first precursor on the substrate surface. The purge gas after each precursor pulse can prevent parasitic CVD deposition.

The sequential, self-limiting deposition nature of ALD makes the precise atomic layer control possible. Film growth can be attained as fine as ~0.1Å per cycle. And the films deposited by this method show excellent film conformity and uniformity over large areas. The main drawbacks of this technique are that the deposition rate is very slow, and the materials that can be synthesized by this technique are limited compared to other CVD methods and molecular beam epitaxy technique (MBE).

In this work, the AlO₅ deposition employs two precursors: trimethylaluminum (TMA) and water. The chamber temperature is kept at 200 °C. There are 4 steps for each cycle.

1) TMA is pulsed into the reaction chamber and reacts with the surface hydroxyl groups in a saturating manner until a monolayer of TMA has been chemisorbed on the substrate.

2) The excess of the precursor is purged away by the gas N₂.

3) The second precursor H₂O is pulsed into the reactor and reacts with the chemisorbed TMA, forming an AlO₅ layer on the substrate and a byproduct gas CH₄.

4) The CH₄ gas and excess H₂O are then purged by N₂.

These 4 steps make one complete cycle. By controlling the number of cycles, the desired film thickness can be obtained. In the ideal case, a complete monolayer is formed for each cycle and no impurities are introduced into the film. In practice, however, only a fraction of a monolayer may be deposited in each cycle due to steric hindrances between bulky ligands in
the chemisorption layer or lack of active surface sites [75]. And impurities found in the films are at the 0.1-1 atom % level. [76]

In this work, a Savannah 100, Cambridge Nanotech ALD system was used to deposit aluminum oxide (AlO\textsubscript{x}) as a dielectric layer. The surface reaction during AlO\textsubscript{x} deposition could be described as [77]: (In the equation, * represents the surface species)

A) \( \text{AlOH}^* + \text{Al(CH}_3\text{)} \rightarrow \text{AlOAl(CH}_3\text{)} 2^* + \text{CH}_4 \)  \hspace{1cm} (Eq3.1a)

B) \( \text{AlCH}_3^* + \text{H}_2\text{O} \rightarrow \text{AlOH}^* + \text{CH}_4 \)  \hspace{1cm} (Eq3.1b)

Temperature is a key parameter to control the saturation mechanism of ALD. The processing temperature range for ALD to maintain self-terminating growth is called the ALD window. Figure 3.2 shows growth rate vs. process temperature with ALD window defined.

Figure 3.2: ALD growth mechanisms at different temperatures.
From Figure 3.2, only when the temperature is kept at the ALD window and nearly ideal ALD-type self-terminating growth takes place can lead to a constant growth rate. While at low process temperature, it can lead to two contradictory results: on one case, the surface reactions may not have enough thermal energy to complete the reaction and result in a very low deposition rate. Or on another situation, when the temperature is very low and cannot start the reaction at all, the deposition rate can be very high because the reactant is absorbed to the surface and condensed before reaction. While at high process temperature, there are still two contradictory possibilities. On one case, the surface species can decompose and allow additional reactant adsorption. This will result in a higher deposition rate. While on some other situations, high temperature may result in desorption the surface species needed for ALD reactions from surface and lead to a lower deposition rate [77]. The cases on low and high temperature process depend on the specific temperatures, reactant gases and pressure in the chamber.

3.1.3 Plasma-Enhanced Chemical Vapor Deposition

In this study, an Oxford Plasmalab 80Plus parallel plate PECVD system is employed to deposit both SiNx and SiOx thin films as gate dielectrics. The deposition temperature of the SiOx thin film is 300°C and 200°C for SiNx thin film. In general, the devices have better performance with ALD deposited AlOx films.

Plasma Enhanced Chemical Vapor Deposition (PECVD) is an excellent tool to deposit variety of thin films at lower temperatures compared to conventional CVD reactors. PECVD uses high voltage to generate a glow discharge, i.e. plasma. The electrical energy is then
transferred into a gas mixture. The active gas mixture is then discharged and transformed into reactive radicals, ions, neutral atoms and molecules, and other highly excited species. These atomic and molecular fragments interact with a substrate. The deposition processes or etching processes will occur on the surface of the substrate depending on the nature of these reactions. Because the formation of the reactive atoms and energetic species in the gas phase forms by collision in the gas phase, the substrate can be maintained at a relative low temperature. For example, high quality silicon dioxide thin films can be deposited at 300~350 °C while conventional CVD requires substrate temperatures up to 650 ~850 °C to deposit similar quality thin films.

3.1.4 E-Beam Evaporation

Electron beam evaporation is a type of physical vapor deposition (PVD). This technique utilizes a high energy electron beam to heat the target, transforming the target material into its gas phase. Therefore a thin layer of target material is then uniformly coated on the sample’s surface. The electron beam is usually generated from a filament, accelerated by a high voltage (5-30KeV), focused and then guided to the target crucible by magnets. The chamber is required to maintain a high vacuum when the electron beam is on. The crucibles are poor heat conductor.

There are several advantages for the Ebeam evaporation.

1) The electron beam only heats the target material but not the entire crucible. Therefore it has lower contamination level than other thermal evaporation techniques.
2) The thin films deposited by this method are dense and have good adhesion to the substrates due to the high energy process.

3) The substrate holder is usually on the top of the crucibles, which leads to a small incident angle. This makes lift off processes very easy.

4) There are several crucibles in the chamber. Multiple layer deposition is very easy for this technique.

However, one of the drawbacks for E-beam evaporation is the possible x-ray damage to the deposited thin-film from the electron beam.

In this work, an Edwards E-beam evaporation system is used to deposit source drain or interconnect metals. The acceleration voltage is 5keV.

3.2 **Patterning Techniques**

3.2.1 **Photolithography**

Photolithography is a process used to transfer patterns from photo-masks to thin films or a bulk substrate using ultraviolet (UV) light. It is an important technique for modern semiconductor and integrated circuits.

The basic steps of photolithography are as follows.

1) Sample surface must be cleaned to remove any dust or organic contamination by acetone, methonal and DI water before applying photoresist. Then the samples are put on a hotplate for dehydration to improve the adhesion.
2) A photoresist layer is then applied on the surface of the substrate in a spin-coating hood. Depending on the desired thickness, the spinning rate can range from several hundred to several thousand rpm and use between 20-120 seconds. The spinning process makes the photoresist thin and uniform.

3) The coated samples are then put on a hot plate / oven for soft bake to drive out solvents and dehydrate the film.

4) The samples are then transferred to the aligner for a UV light exposure. Alignment of the mask is very critical. By adjusting the X, Y and rotational axis, the perfect alignment with previous patterns or layers can be achieved. After alignment and raising the substrate to contact the photo mask, an exposure of UV light causes a chemical change on the photoresist.

5) The samples are then dipped into a special solution called “developer” to remove some area of photoresist, resulting in the patterns reprinted from the mask.

The critical part of photolithography is the photoresist. There are three major components of a photoresist: Resin, photoactive component (PAC), and solvent. The type of the PAC determines the type of photoresist, either positive or negative. Positive photoresist, the most common type, becomes soluble in the developer when exposed; while with negative photoresist, unexposed regions are soluble in the developer.

The photo-mask is created by a photographic process and developed onto a glass substrate. The cheap masks use ordinary photographic emulsion on soda lime glass, while chrome on quartz glass is used for the high-resolution deep UV lithography.
For this work, a MJB 360 aligner was used. The UV light source is 365nm (I-line) and the exposure energy was set to 275 mJ/cm². The AZ5214E was used as both a positive and negative photoresist in this work. When used as positive photoresist, the samples were developed after exposure. When used as negative photoresist, the samples were baked at 115 °C for 90 sec after the first exposure, followed by a flood exposure (without photo-mask) for 90 sec before the samples were developed.

### 3.2.2 Lift Off

The lift off process is a common technique in research and industry when the etching is not preferred or the selectivity between the layers and mask is poor. It is the follow up process of photolithography. After a new thin film is deposited on the patterned photoresist coated samples, the whole sample is then submerged in a solvent (usually acetone) to remove the photoresist. This will also removes the film on top of the photoresist, leaving the desired pattern of the thin film on the substrate. However, the presence of photoresist may prevent the deposition process from being high temperature. For example, the AZ5214 photoresist cannot exceed ~250 °C. Some special high temperature photoresist may sustain in higher temperature. In this process, the PLD deposition of IGZO, ITO and the source drain metal Ti, Moly are patterned using lift off process.

### 3.2.3 Etching

Etching is a common process technology in semiconductor IC fabrication. Etching processes employ acids or other active gas/plasma to engrave the samples, which are usually
covered with patterned material, called etching masks. A layer is then chemically removed from the surface for the uncovered region of the wafer.

Wet etching employs liquid phase etchants to etch the samples. The samples are immersed in a bath of etchant, which is specially designed to attack some type of materials. Wet etching usually is a quick and convenient process. However, wet etching is usually isotropic, which leads to large bias when etching thick films. It also requires the disposal of large amounts of toxic waste.

RIE is dry etching technique and is very commonly used. It uses chemically reactive plasma to remove a surface layer of the wafers. The plasma is generated under low pressure (vacuum) by an electromagnetic field. High-energy ions from the plasma attack the wafer surface and react with it. A RIE system usually consists of a cylindrical vacuum chamber. Inside the chamber there are:

1) Two electrodes to create an electric field. These two electrodes are usually two plates. One grounded and one biased at positive high voltage.

2) Component to accelerate ions. The etching gases are introduced into the chamber through a small inlet on the top of the chamber, and exits to the vacuum pump system through the bottom. The gases are then discharged into plasma and generate ions.

The advantage of RIE etching is that it is an anisotropic etching. It is a uni-directional process which is beneficial for high fidelity pattern transfer.

In this work, two RIE etch tools were used. SiN$_x$ and SiO$_x$ layers were etched in Oxford Plasmalab 80Plus parallel plate RIE system. O$_2$ and CF$_4$ are used as etching gases. ITO and
Al2O3 layers were etched in a Plasmatherm batchtop RIE tool, in which BCl3 is used as etching gas.

### 3.3 Focused Ion Beam

The focused ion beam (FIB) microscope has been widely used in fundamental material studies and semiconductor manufacturers over the last two decades. It offers high-resolution imaging and flexible micromachining in a single platform.

The operation principle of the FIB is very similar to the scanning electron microscope (SEM), except that in a FIB system, a gallium ion beam is used instead of electron beam. FIB can use this focus ion beam to mill other materials, and the scattering beam can also be used for imaging.

Modern advanced technology allows the minimum resolution of the FIB to be several nanometers when operating at low current levels. The resolution of FEI Quanta 200 3D SEM/FIB dual beam system used in this study is 7nm when operating at 10pA current. Higher beam currents would have lower resolution but higher etching speed.

The main advantages of FIB etching include etching and imaging in one system, room temperature etching processing, for allowance of flexible substrates or un-flattened substrates that are not suitable for photolithography. This can be very useful for flexible electronics or sensors.

More details about this technique and this FIB system will be presented in Chapter 6.
3.4 Device Fabrication

Several substrates have been used in this study including: p-type silicon wafers, p-type silicon with 100nm thermal silicon dioxide, corning glass coated with an ITO thin film, glass coated with ITO and ATO (Al₂O₃ and TiO₂ super lattice) thin films.

Even though the process procedures are a little bit different for different substrates, all the IGZO thin film transistors in this study are fabricated using a staggered bottom gate configuration. Here, we use the ITO on glass substrate as an example, to explain the whole process of fabricating TFT devices. Usually a four-level mask was used. The four mask levels are gate electrode level, dielectric layer, channel level and the source/drain level.

First of all, the bottom ITO gate was patterned by photolithography, followed by BCl₃ reactive ion etching (RIE) dry etching, at 100W forward power for 20 minutes. A 100 nm Al₂O₃ dielectric layer was then grown by atomic layer deposition (ALD) at 200 °C. A 35-40 nm thick amorphous IGZO channel layer was deposited by pulsed laser deposition (PLD) in oxygen pressure of 25 mTorr at room temperature. ITO source/drain contacts and interconnects were then deposited by PLD at room temperature. In some devices, titanium or Moly was used as source/drain contact. These metals were deposited in an E-beam evaporator using a conventional photolithography and lift off process. If a common gate structure was used, the dry etch of ITO bottom gate and Al₂O₃ dielectric could be skipped. The example of patterned gate structure and un-patterned gate (common gate) structured TFTs are shown in Figure3.3.
3.5 **Electrical Characterization of Thin Film Transistors**

Discrete devices and logic gates were characterized using a HP 4155B semiconductor parameter analyzer. All tests were carried out in the dark at room temperature. The inverters, NAND and NOR gates were characterized by a HP 4142B semiconductor parameter analyzer with Agilent 33220A arbitrary waveform generator and curve tracer.

Thin film transistors are evaluated using different parameters. Various figures-of-merit including the subthreshold swing, threshold voltage, drain current on-to-off ratio, turn-on voltage, and channel mobility are discussed below. While these parameters show important
characteristic of the device, each figure-of-merit has it’s own unique shortcomings. It is imperative to consider a compilation of these figures-of-merit when assessing device performance. For the logic gates, gain; noise margin, and operation speed are considered as well.

3.5.1 Thin Film Transistors Operation Equations

Because both TFTs and MOSFETs are field-effect devices, classic MOSFET drain current equations are typically employed for TFT assessment. The MOSFET equations for both the triode and saturation regions of operation are shown below:

\[
I_{DS} = \mu C_{ins} \frac{W}{L} \left[ (V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \quad \text{for } V_{DS} \leq V_{GS} - V_T, \quad (3.2a)
\]

\[
I_{DS} = \frac{1}{2} \mu C_{ins} \frac{W}{L} (V_{GS} - V_T)^2 \quad \text{for } V_{DS} > V_{GS} - V_T \quad (3.2b)
\]

However, these two equations are not so accurate in some situations when applied to thin film transistors. The modified equations are usually used for better assessment of TFTs [78]:

\[
I_{DS} = \mu(V_{GS}) C_{ins} \frac{W}{L} \left[ (V_{GS} - V_{on}) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \quad \text{for } V_{DS} \leq V_{GS} - V_{on}, \quad (3.3a)
\]

\[
I_{DS} = \frac{1}{2} \mu(V_{GS}) C_{ins} \frac{W}{L} (V_{GS} - V_{on})^2 \quad \text{for } V_{DS} > V_{GS} - V_{on} \quad (3.3b)
\]

There are two differences between Eq. (3.2) and Eq. (3.3). First, the mobility in Eq. (3.2) is constant while in Eq. (3.3) the \(V_{GS}\) dependent mobility is used, which is more accurate in thin film transistor technology. Second, \(V_T\) is replaced by \(V_{on}\) in equation (3.3), since \(V_T\) is
an ill-defined parameter. The determination of $V_T$ is quite subjective. More details about mobility $\mu$, threshold $V_T$ and $V_{on}$ will be discussed in the following section.

3.5.2 DC Current-Voltage Measurement--Output Characteristics

![Graph of Output Characteristics](image)

Figure 3.4: Output characteristics of an IGZO TFT. Drain current (linear scale) is plotted against drain voltage for gate voltages 0-15 V in 3 V steps. Gate oxide is 100nm SiO$_2$, 50 nm IGZO grown at 25 mT oxygen partial pressure, TFT dimensions are, W/L=50\mu m/10\mu m.

Output characteristics or $I_{DS}$-$V_{DS}$ are common tests for understanding the thin film transistor devices under test. The $I_{DS}$-$V_{DS}$ curves are obtained by sweeping $V_{DS}$ for different $V_{GS}$ values, which allows one to observe the pre and post pinch off regime of the transistor. A series of typical output characteristics are shown in Figure 3.4. Output characteristics provide some qualitative information about this device. For example, the decreasing
separation distance of $I_{DS}-V_{DS}$ curves for increasing $V_{GS}$ indicates that the mobility degraded for that $V_{GS}$ range. The hard saturation of these $I_{DS}-V_{DS}$ curves indicates that the channel is fully depleted for that $V_{GS}$. Good saturation is very important for a thin film transistor. The linear region of $I_{DS}-V_{DS}$ also provides information about contact resistance.

3.5.3 DC Current-Voltage Measurement--Transfer Characteristics

Transfer characteristics or $I_{DS}-V_{GS}$ characteristics could be obtained by sweeping $I_{DS}$ with increasing $V_{GS}$ at constant $V_{DS}$. These characteristics provide quantitative information about the device under test. Figure 3.5 shows typical transfer characteristics of an IGZO based TFT. Several important device parameters such as threshold voltage, turn-on voltage, subthreshold swing, current on/off ratio, mobility can be extracted from these transfer characteristics. This parameter extraction will be discussed in the following section.

3.5.3.1 Subthreshold Swing and Drain Current On-Off Ratio

The sub-threshold swing ($S$) is estimated using a semi-log plot of the transfer characteristic taken at high $V_{DS}$. $S$ is the inverse of the maximum slope in the transfer characteristic, as shown in Figure 3.5.

$$S = \left( \frac{d \log(I_D)}{dV_{GS}} \right)_{\text{max}}^{-1} \tag{3.4}$$

$S$ determines how fast it is to turn a TFT from the off state to on state.
Also, the S value provides important information about the quality of a TFT. According to Kamiya et al [27], the subthreshold voltage swing is related to the trap density in the band gap (subgap traps) at the Fermi level \( D_{sg} \) as:

\[
S = \ln 10 \left\{ \frac{k_B T}{e} \left( 1 + \frac{e D_{sg}}{C_{ins}} \right) \right\} = 59.5 \left( 1 + \frac{e D_{sg}}{C_{ins}} \right) \text{ [meV/decade at 300K]} \tag{3.5}
\]

Where \( C_{ins} \) is the gate capacitance. From Eq. (3.4) the S value should be larger than 59.5 meV/decade at 300K and a steeper transfer curve corresponds to a higher quality channel with fewer defects. This \( D_{sg} \) value includes contributions from the bulk channel region \( N_{sg} \) and the interface \( D_{it} \).

The subthreshold swing in figure 3.5 is estimated to be 190mV/decade.

Drain current on/off ratio is another useful measurement of TFT performance. It is simply the ratio of the maximum on state saturation drain current \( I_{on} \) to the minimum measured off state current \( I_{off} \). Higher saturation current a TFT, or lower gate leakage current will lead to higher drain current on/off ratio. \( I_{off} \) is also a measure of the gate leakage present in the TFTs. To reduce the leakage power consumption, a lower \( I_{off} \) is preferred. For the devices shown in the figure 3.5, an \( I_D \) on/off ratio higher than 108 is extracted. Gate leakage current \( I_{off} \) is less than 1pA.
63

Figure 3.5: Typical transfer characteristics of an IGZO TFT at 3 different $V_{DS}$, 0.1V, 2V and 10 V. Subthreshold voltage swing, drain current on-off ratio, and turn-on voltage are indicated in the figures. An IGZO layer of ~45 nm was grown at 25 mTorr oxygen partial pressure. TFT dimensions, W/L = 50 µm /10µm.

3.5.3.2 Threshold Voltage and Turn-on Voltage

Threshold voltage $V_T$ is an important parameter for transistors. In MOSFET, $V_T$ denotes the gate voltage where the inversion layer is formed at the gate dielectric and semiconductor interface. In TFTs, $V_T$ denotes the gate voltage where an accumulation layer or conductive channel is formed close to the dielectric and semiconductor interface. It is usually used to evaluate the performance of a device. However, in the case of thin film transistors, $V_T$ is quite an ambiguous parameter. The ambiguity comes from multiple sources. First of all, $V_T$ can be extracted by different methods. It can either be extracted using extrapolation of the $I_{DS}$
−V_{GS} curve (when biased in triode) or extrapolation of the $\sqrt{I_{DS}} - V_{GS}$ curve (when biased in saturation). Second, the extrapolation of curves can be quite subjective.

Figure 3.6: Threshold voltage extraction from the same device. (a) $I_{DS} - V_{GS}$ extraction at the linear regime, $V_{DS}=0.1V$. (b) $\sqrt{I_{DS}} - V_{GS}$, extraction at the saturation regime, $V_{DS}=10V$. This device is the same as shown in Figure 3.5.

Figure 3.6 shows two different methods to extract the threshold voltage for the same device. Figure 3.6(a) use the $I_{DS} - V_{GS}$ extraction method in the linear regime, i.e., with $V_{DS}=0.1V$. The $V_T$ is estimated to be ~2.9V. While Figure 3.6(b) uses the $\sqrt{I_{DS}} - V_{GS}$ extraction at the saturation regime, i.e., with $V_{DS}=10V$. The $V_T$ is estimated to be ~0.5V by this method. It is obvious that the $V_T$ is quite subjective and not unique for a device.

Therefore, another parameter, turn on voltage, $V_{on}$, is widely used in literature [78]. As shown in Figure 3.5, $V_{on}$ is determined by plotting log ($I_D$) −$V_{GS}$. The gate voltage at the onset of conduction (distinguished by a sharp increase in current) establishes $V_{on}$. $V_{on}$ is
easier to handle in device analysis and is much more stable. It usually won’t change with $V_{DS}$ if we don’t consider the drain induced barrier lowering effect. Both $V_T$ and $V_{on}$ are reported for the devices tested in this work.

3.5.3.3 Mobility Extraction

The mobility of a field-effect transistor (FET) is a very important figure-of-merit parameters. It is the average mobility of all carriers transported in the channel under all different scattering mechanisms including phonon, ionized impurity, and interface roughness. The channel mobility determines the current drive capability and maximum switching frequency of a FET. The accurate extraction and assessment of channel mobility is very important.

Even though channel mobility is a very useful and important parameter for device comparison, there are some complications in mobility extraction. First of all, similar to $V_T$ extraction, there are several different methods to extract the channel mobility. Each different method leads to slightly different result due to some approximation and different models used. Secondly, the gate leakage current is usually not accounted for in the extraction. However, it can also affect the extracted value of channel mobility.

In the following section, five types of different channel mobilities including effective mobility ($\mu_{eff}$), field effect mobility ($\mu_{FE}$) saturation mobility ($\mu_{sat}$), average mobility ($\mu_{avg}$), and incremental mobility ($\mu_{inc}$) will be discussed. The equations to extract these mobilities are also provided.
The effective mobility \( \mu_{\text{eff}} \) and field effect mobility \( \mu_{\text{FE}} \) are extracted from the triode region of device operation (below pinch off) and saturation mobility \( \mu_{\text{sat}} \) is extracted from the saturation region of device operation (above pinch off).

From the Eq.(3.2a), in the triode region, \( V_{DS} \) is small, Eq (3.2.a) could be expressed as:

\[
I_{DS} = \mu C_{\text{ins}} \frac{W}{L} [(V_{GS} - V_T) V_{DS}] 
\]  

(3.6)

Differentiating Eq. (3.6) with respect to \( V_{DS} \) and \( V_{GS} \) yields the channel conductance, \( g_d \), and the transconductance, \( g_m \), respectively:

\[
g_d = \frac{\partial I_D}{\partial V_{DS}} = \mu C_{\text{ins}} \frac{W}{L} (V_{GS} - V_T) 
\]  

(3.7)

\[
g_m = \frac{\partial I_D}{\partial V_{GS}} = \mu C_{\text{ins}} \frac{W}{L} V_{DS} 
\]  

(3.8)

Therefore, the effective mobility, \( \mu_{\text{eff}} \) and the field effect mobility \( \mu_{\text{FE}} \), can be extracted by,

\[
\mu_{\text{eff}} = \frac{g_d}{C_{\text{ins}} \frac{W}{L} (V_{GS} - V_T)} 
\]  

(3.9)

\[
\mu_{\text{FE}} = \frac{g_m}{C_{\text{ins}} \frac{W}{L} V_{DS}} 
\]  

(3.10)

From Eq. (3.9), it is obvious that \( \mu_{\text{eff}} \) is dependent with \( V_{GS} \).

Next, considering the saturation region, the drain current equation is shown in Eq. (3.2b). The saturation mobility is extracted from the saturation region of TFTs operation. Taking the square root of Eq.(3.2.b) and differentiating with respect to \( V_{GS} \), \( \mu_{\text{sat}} \) is given by
\[ \mu_{\text{sat}} = \left( \frac{d \sqrt{I_D}}{dV_{GS}} \frac{1}{\sqrt{\frac{W}{L}}} \right)^2 \]  

From Eq. (3.11), \( \mu_{\text{sat}} \) can be extracted from the slope of the extrapolation of the \( \sqrt{I_D} \sim V_{GS} \) curve, as shown in Figure 3.6(b). Thus \( \mu_{\text{sat}} \) is dependent on the threshold voltage extraction \( V_T \).

Actually, each method has its own limitations. For the \( \mu_{\text{sat}} \), may not be so accurate because the mobility extracted by this method is an average of the carrier mobility in the “channel” region and the mobility in the “pinch off” region of the channel, and the mobilities in these two regions may be quite different. In practice, it is more often employed for the case that the leakage current significantly affects the subthreshold voltage current. Since \( \mu_{\text{eff}} \) is dependent on the \( V_T \) extraction, while \( V_T \) can be ambiguous. The condition it is obtained should be specified. \( \mu_{\text{FE}} \) can be considered to be inaccurate as it doesn’t include the effect of gate bias \( V_{GS} \). In practice, \( \mu_{\text{FE}} \) is usually used because it doesn’t require the extraction of \( V_T \). However, \( \mu_{\text{sat}} \) is often used in literature to show the saturation mobilities.

These three mobility extraction methods are based on the ideal transistor operation equation and assume that that the channel mobility of TFTs is a constant independent of \( V_{GS} \). While this assumption would be valid with an ideal MOSFET, it doesn’t hold for TFTs, since TFTs may have several non-ideal factors such as carrier trapping, interface roughness scattering and velocity saturation. Therefore, Hoffman introduced another two mobility metrics, i.e., average mobility, \( \mu_{\text{avg}} \), and incremental mobility, \( \mu_{\text{inc}} \) [80]. These two new methods better suit the TFTs non-ideal factors and provides us a more physically meaningful
and quantitatively representative metric of device performance. These two new methods use basic charge transport theory and include gate bias dependent mobility. The details of these two mobility extraction methods and the derivation will be discussed below.

Average mobility $\mu_{\text{avg}}$ is the average mobility of the channel. Assume this channel carrier is drift-current dominated. The channel conductance can be defined as

$$G_d(V_{GS}) = \mu_{\text{avg}}(V_{GS}) \frac{W}{L} Q_n(V_{GS})$$  \hspace{1cm} (3.12)

In this equation, $G_d$, $\mu_{\text{avg}}$ and $Q_n$ are all dependent on $V_{GS}$. $W$ and $L$ are the channel width and channel length, respectively. $Q_n$ is the charges accumulated in the channel. It could be determined by measuring the gate to channel capacitance.

$$Q_n(V_{GS}) = C_{\text{ins}}(V_{GS} - V_{on})$$  \hspace{1cm} (3.13)

Substitute Eq. (3.13) into Eq. (3.12) and reorganize the equation, we can get the average mobility $\mu_{\text{avg}}$.

$$\mu_{\text{avg}}(V_{gs}) = \frac{G_d}{\frac{W}{L} Q_n} = \frac{G_d}{C_{\text{ins}} \frac{W}{L} (V_{GS} - V_{on})}$$  \hspace{1cm} (3.14)

The average mobility $\mu_{\text{avg}}$ is similar to $\mu_{\text{eff}}$ in Eq. (3.9), except that in $\mu_{\text{avg}}$, the $V_T$ is replaced in with $V_{on}$. This will eliminate the ambiguity of the $V_T$ extraction. However, if the subthreshold diffusion current is large, the use of $V_{on}$ will introduce bigger error in the mobility extraction. Usually for the oxide based TFTs, the contribution from diffusion current in the subthreshold regime is very small. In this study, the gate leakage is usually less than 10 pA.
The last mobility extraction method—incremental mobility $\mu_{\text{inc}}$, corresponds to the incremental mobility of carriers added to the channel when the gate voltage increases. The equations are derived below.

$$\Delta Q_n(V_{GS}) = C_{\text{ins}}\Delta V_{GS} \quad (3.15a)$$

$$\Delta G_d = \mu_{\text{inc}}(V_{GS}) \frac{W}{L} \Delta Q_n(V_{GS}) \quad (3.15b)$$

$$\mu_{\text{inc}}(V_{GS}) = \frac{\Delta G_d}{\Delta V_{GS} \frac{W}{L} C_{\text{ins}}} = \frac{G_d'(V_{GS})}{C_{\text{ins}} \frac{W}{L}} \quad (3.15c)$$

To estimate $\mu_{\text{inc}}$, the incremental induced channel charge ($\Delta Q_n(V_{GS})$) is first defined, and then the differential channel conductance is determined using Eq. (3.12). It is important to note that Eq. (3.15) is based on the assumption that the mobilities of the carriers present in the channel don’t change when additional charges are induced.

### 3.6 Conclusions

The technologies to deposit thin films used in our study were reviewed. These deposition techniques including pulsed laser deposition, atomic layer deposition, plasma enhanced
chemical vapor deposition and e-beam evaporation were presented. The working principles, structure, advantages and disadvantages of these techniques are discussed.

Basic device patterning techniques includes photolithography, lift-off, etching and focused ion beam were discussed.

Finally, an overview of device electrical characterization was presented. The TFTs operation equations, DC output characteristics and transfer characteristics were discussed. Several important parameters that will be discussed in the later chapters of this dissertation were discussed. These parameters include subthreshold swing, drain current on-off ratio, threshold voltage and turn-on voltage and five different carrier mobility estimation methods.
Chapter 4

INDIVIDUAL INDIUM GALLIUM ZINC OXIDE THIN FILMS TRANSISTORS AND DEVICE STUDY

Indium Gallium Zinc Oxide is a relatively new material system. There are many material properties and device mechanisms that need to be studied to better understand IGZO based TFTs. This chapter will discuss some affects that will have an influence on device performance and how to optimize these parameters to develop high performance IGZO based TFTs.

4.1 Overview

In this work, the devices can be categorized into transparent devices fabricated on glass substrates and opaque devices fabricated on silicon substrates. The information about devices we have fabricated is summarized in table 4.1. The cross section of both patterned gate and common gate device structures are shown in Figure 3.3. The detailed process steps are described in section 3.4.

Table 4.1: Summary of devices fabricated in this work

<table>
<thead>
<tr>
<th>Design and structures</th>
<th>Transparent TFTs</th>
<th>Opaque TFTs</th>
</tr>
</thead>
<tbody>
<tr>
<td>S/D metal</td>
<td>ITO, Ti</td>
<td>ITO, Ti</td>
</tr>
<tr>
<td>dielectric</td>
<td>Al₂O₃(ALD), ATO, SiNₓ (PECVD)</td>
<td>Al₂O₃ (ALD), thermal SiO₂, SiNₓ (PECVD)</td>
</tr>
<tr>
<td>Gate pattern</td>
<td>Patterned gate/ common gate</td>
<td>Common gate</td>
</tr>
<tr>
<td>Gate metal</td>
<td>ITO</td>
<td>Cr/Au</td>
</tr>
<tr>
<td>Substrates</td>
<td>Glass</td>
<td>Silicon</td>
</tr>
</tbody>
</table>
Several effects about the device performance and device optimization are studied and will be discussed in the following sections:

- Effect of oxygen partial pressure
- Effect of channel thickness
- Effect of dielectric thickness
- Effect of channel and source/drain overlap area
- Effect of patterned gate
- Device stability
- Effect of annealing

4.2 Effect of Oxygen Partial Pressure

Oxygen partial pressure is a key parameter to control the carrier concentration in the IGZO layer. It will also affect many devices parameters such as threshold voltage, saturation on current, subthreshold slope, and hysteresis windows.

Figure 4.1 (a) shows the transfer characteristics of TFTs deposited at different oxygen partial pressures. The oxygen partial pressures were 10mT, 25mT and 40mT, respectively. These IGZO channel layers all have the same thickness, all about 35nm thick. Because the carrier concentration of IGZO thin film mainly comes from its oxygen vacancies, the films deposited at higher oxygen partial pressures have lower carrier concentrations and therefore are more resistive. In contrast, the IGZO thin films deposited at lower oxygen partial pressures have higher carrier concentration and the films are more conductive. When comparing these devices parameters for different oxygen partial pressures, IGZO thin films
with lower oxygen partial pressure, have a higher saturation and a lower turn on voltage. The hysteresis window is also larger for the TFTs with IGZO grown at 40mT oxygen partial pressure, as shown in Figure 4.1(b).

![Comparison of transfer curves for different oxygen partial pressure. V_DS=10V, L/W=100 µm /20 µm (b) parameters extracted from (a). IGZO thicknesses are kept at 35nm.](image)

Figure 4.1: (a) Comparison of transfer curves for different oxygen partial pressure. V_{DS}=10V, L/W=100 µm /20 µm (b) parameters extracted from (a). IGZO thicknesses are kept at 35nm.

Devices with a semiconductor layers grown at different oxygen partial pressures will also have different mobilities. Figure 4.2 shows the saturation mobility of three TFTs with IGZO deposited at 10mT, 25mT and 40mT. Under V_{DS}=10V, the saturation mobility of 10mT, 25mT and 40mT are 13.8, 8.8 and 2.6 cm^2V^{-1}s^{-1}, respectively. These results show that IGZO thin films grown at lower oxygen partial pressures will result in high device mobilities. If measuring the saturation mobilities under a higher V_{DS}, the mobility value will be higher than measured at low V_{DS}.
Another interesting observation is that in these devices, the mobilities do not increase as the $V_{GS}$ increases. The mobilities reach the highest value when $V_{GS}$ is around 8-9V. Then the mobilities decrease with $V_{GS}$ when $V_{GS}$ is higher at 10V.

The subthreshold slopes of the devices do not change much when changing the oxygen partial pressure. The subthreshold slopes are all calculated to be ~200mV/decades for all values of oxygen partial pressures. However, when depositing the IGZO channel layer at partial pressure higher than 40mT, the subthreshold slopes of the devices become larger as the oxygen partial pressure is increased.

Figure 4.2: Comparison of saturation mobilities of TFTs with IGZO grown at different oxygen partial pressure.
4.3 Effect of Channel Thickness

For the IGZO based thin film transistors, channel thickness is also a parameter that will have effect on drain current, threshold voltage, hysteresis window and subthreshold voltage. Optimization of channel thickness is very critical to getting excellent device performance.

Figure 4.3: (a) Comparison of transfer curves for different channel thickness. $V_{DS}=10\,\text{V}$, $L/W=100\,\mu\text{m}/20\,\mu\text{m}$, oxygen partial pressure is 25mT for both deposition. (b) Comparison of saturation mobilities of TFTs with different IGZO channel thickness. Channel thicknesses are 20nm and 35nm channel, respectively.

Figure 4.3 (a) shows the transfer characteristics of two TFTs with different IGZO channel thickness. One is ~35nm, the other is ~20nm. From these transfer curves, one notices that the turn on voltage for thicker channel layer is smaller, and the on drain current is also higher due to the more conductive channel. One can also notice that the hysteresis window is much larger for thinner channel layer. For the TFTs with 20nm IGZO channel layer, the
hysteresis window is ~7.8V, while the hysteresis window is about 2.5V for the TFTs with a 35nm IGZO channel layer. These results indicate that the interface between the IGZO and the gate dielectric is not smooth and the interface state density is high. We speculate that the IGZO thin film quality is not very good and that the surface is rough for the 20nm thin film devices, because the deposition by PLD is island growth, rather than step flow growth atomic layer by atomic layer.

Figure 4.3(b) shows the mobility of TFTs with different channel thicknesses. The saturation mobility of TFTs with a 35nm IGZO channel layer is much higher than that of a 20nm channel layer. This also confirms that the interface between 20nm IGZO and SiO$_2$ is very rough, with high interface state density.

On the other hand, the channel thickness could not be too thick, because if it is too thick, the channel layer is too conductive. A thick channel will result in very negative turn-on voltage and it is hard to deplete the channel layer.

4.4 **Effect of Gate Dielectric Thickness**

The devices with different gate dielectric thicknesses were also evaluated. The Al$_2$O$_3$ thin films were deposited by ALD at 200°C. 250cycles, 500 cycles and 1000 cycles of Al$_2$O$_3$ thin films were deposited. The resulting thickness was about 30 nm, 60 nm, and 110 nm, respectively. Devices with these dielectrics were fabricated. The devices with 250 cycles presented high leakage current, resulting in barely working devices. The transfer curves of the TFTs with 500 and 1000 cycles Al$_2$O$_3$ are shown in Figure 4.4.
From the transfer curves, it can be noticed that the leakage current is large for the 500 cycles TFT when the gate voltage is larger than 10V. The on current of 500 cycles is also larger than the device with 1000 cycles. This is because for a thinner dielectric, the electric field on the channel layer is stronger, leading to more accumulated electrons in the channel. For similar reasons, the threshold voltage is expected to be higher for the thicker dielectrics, however, the difference is very small in our devices, $V_{th}$ of 1000 cycle TFTs is 0.2V smaller than that of devices made with 500 cycles of $\text{Al}_2\text{O}_3$.

Figure 4.4: Comparison of devices with different $\text{Al}_2\text{O}_3$ dielectric thicknesses.
4.5 **Effect of Channel and Source Drain Overlap Area**

At the early stage of our devices design, in order to ensure the carrier injection level was high enough, the source drain was deposited on top of the channel layer. Later in order to improve the device control and reduce parasitic capacitance, the patterned gate design was introduced. The overlap area between channel and source drain would affect the device performance. Figure 4.5 shows the images of full overlap device and half overlap (partial overlap) device.

![Figure 4.5: The images of channel and source drain overlap--full overlap and half overlap](image)

Comparing the transfer curves of devices with channel and source/drain full overlap and half overlap, the threshold voltage and the subthreshold voltage swing are about the same. In the linear scale, it could be found that the saturation current of the full overlap device is
slightly higher than that of half overlap device. This is because larger channel source/drain overlap area leads to a larger carrier injection area.

![Graphs showing the effect of channel and source/drain overlap.](image)

(a) (b)

Figure 4.6: Effect of Channel and source/drain overlap (L/W=100 µm /400 µm), (a) logarithm scale, (b) linear scale

### 4.6 Effect of Patterned Gate

The samples in this section were fabricated on ITO/glass substrates, with ALD growth of an Al₂O₃ dielectric. ITO and Ti were compared as the source/drain metal.

As mentioned in the previous section, the patterned gate and un-patterned gate devices were fabricated and characterized. The electrical transfer curves of patterned gate and un-patterned gate devices were shown in Figure 4.7. Both devices were using ITO as source drain material. They were fabricated at room temperature without any annealing.
Figure 4.7: (a) Images of pattern gate device and un-patterned gate devices (b) Transfer curves of patterned and un-patterned gate TFTs.

It can be noticed that there is a hysteresis window in the IV curve of the un-patterned device, this is commonly observed and it is usually interpreted to be due to the charges trapped in the interface between the semiconductor and gate dielectric. However, for the patterned gate devices, the hysteresis window is different from the un-patterned gate devices, the hysteresis window is smaller, and there is a “hump” in the sweep back curve.

To better understand the origin of the hysteresis. The ITO and Ti were used as source/drain metals. Figure 4.8 shows the transfer curves of un-patterned and patterned gates devices with ITO source drain and Ti source/drain.
Figure 4.8: (a) Transfer curves of un-patterned gate devices with ITO and Ti source drain (L/W=200/800 µm). (b) Transfer curves of patterned gate devices with ITO and Ti source drain, (L/W=100 µm /400 µm).

The un-patterned gate devices, with ITO and Ti source drain have similar shaped hysteresis windows, indicating that the majority of interface charges are trapped in the insulator and IGZO interface. Yet the hysteresis windows of Ti source drain devices tend to be smaller. This is due to the better contact interface between Ti and IGZO than that of ITO and IGZO. This implies that there are some small amount of charges trapped in the interface between ITO and IGZO. It is clear that the “hump hysteresis” is related to the patterned gate devices.

There may be three reasons for this interesting phenomenon:

a) The smaller contact area of IGZO/insulator and IGZO/source drain in patterned devices, results in fewer trap charges, which leads to the smaller hysteresis windows.
b) This may be due to interface states between the ITO gate sidewall and the IGZO, the bottom ITO gate was dry etched by RIE and about 200 nm in height. If the etched surface was not smooth enough there may be some interface states on the ITO sidewall and insulator.

c) The electric field around the gate edge is higher than other region in the channel, this non-uniform electrical field from the gate would make the channel conductivity non-uniform. The drain potential is higher than the source terminal as well, making the energy band bending complex in the channel.

4.7 Stability of Devices

The long term stability of IGZO TFTs is a critical issue for applications in flexible circuits or in displays. In this experiment, the performance of new devices measured within <24 hours after fabrication and old devices sitting in office for 3 weeks were characterized. Figure 4.9(a) shows the patterned gate TFTs with ITO source drain. Compared to new devices, the $V_{on}$ of old devices shifted about +1.2 V, and the hysteresis windows became larger. The transfer curves of new and old transistors with a Ti S/D source drain are shown in Figure 4.9 (b). The Ti S/D devices don’t have hysteresis a window after 3 weeks, but a $V_{on}$ shift of about +2V was observed. When measuring more devices including patterned gates and un-patterned gates, for both ITO and Ti source-drains, a positive $V_{on}$ shift was observed for all devices, from +0.5V to +2.5V, the hysteresis windows became a little larger, indicating a higher interface state density. The saturation current, on off ratio remained almost the same.
Figure 4.9: Transfer curves of devices measure right after fabrication and after 3 weeks, (a) patterned TFTs with ITO source drain, (b) patterned TFTs with Ti source drain.

The positive shift of the $V_{on}$ and the larger hysteresis windows is due to the $O_2$ and $H_2O$ exposure. When the devices were placed in the room atmosphere for a long time, $O_2$ and $H_2O$ molecules were adsorbed on the surface of the IGZO. The $O_2$ would become the $O^-$ ions sticking to the surface if reacting with electrons [81]:

$$O_2 (\text{gas}) + 2e^- = 2O^- (\text{solid})$$

When measuring the aged devices, extra positive charges are needed to compensate these negative ions, that is why $V_{on}$ shifts from $+0.5V$ to $+2.5V$. More charges trapped in the semiconductors results in a larger hysteresis window.

4.8 **Effect of Annealing**

The devices in this experiment were fabricated on ATO/ITO/glass substrates. A bottom gate stagger structure with common gate was used. 6500 pulses (about 40 nm) of IGZO was
deposited at 25 mT O₂ partial pressure. About 100 nm PLD deposited ITO was used as the source/drain material. After the devices were fabricated, some of the devices were annealed in the air at 200°C, 300°C, 400°C, 500°C, respectively. The electrical transfer curves of devices annealed at different temperature and as deposited are shown in Figure 4.10 (a). The important parameters including hysteresis window, saturation current and turn on voltage Vₜₜ are summarized in Figure 4.10 (b).

It was observed that annealing can reduce or eliminate the hysteresis window. The hysteresis window was eliminated when annealed at 400 °C or higher. This implied the interface density states were reduced by annealing. And at 400°C, the interface density states were almost eliminated. Vₜₜ became negative due to the removal of the charges trapped in the interface. This also implied that the charges trapped were primarily negative charges. The saturation current at V₉S=20V and V₉S=10V increased when annealing temperature increased, and reached a maximum value at 400°C annealing, then decreased as temperature further increased. This means that from room temperature to 400°C, the annealing improved the quality of the IGZO thin films and removed the interface states between the IGZO and insulator. However when annealing at temperatures higher than 400°C, the higher temperature started to deteriorate the material’s quality, leading to the decrease of the saturation current.
Further experiments showed that annealing the IGZO before ITO deposition resulted in better device performance than those annealed after ITO deposition. The transfer curves are shown in Figure 4.11. It was found that for the devices annealed before ITO deposition, 400°C annealing was still the best annealing condition, leading to a zero hysteresis window and highest saturation current. Compared to the devices annealing with ITO source drain at 400°C, the leakage current was smaller and the sub-threshold voltage slope was smaller. This was because the conductivity of the ITO source drain would decrease when annealing in the air, Annealing with ITO would lead to higher the contact resistance between the IGZO and the ITO source drain, which deteriorated the device performance.
4.9 Effect of Channel Length

There are very few reports discussing the short channel effects of IGZO based TFTs. This may be due to the fact that the majority of devices fabricated by IGZO are in relatively large dimensions. However, it is important and interesting to study the short channel effect when the devices are scaled down.

The devices in this study were fabricated on p$^+$-silicon wafers with a 100nm thermal grown SiO$_2$. About 80 nm of IGZO was deposited by PLD at 40 mTorr O$_2$ partial pressure. Titanium was deposited as source drain. The nominal channel dimensions (L×W) were 5 μm×25 μm, 10 μm×50 μm and 20 μm×100 μm. Because of over exposure during the
photolithography, the resulting dimensions became 2 µm×25 µm, 7 µm×50 µm and 17 µm×100 µm, respectively.

![Figure 4.12: The electrical characteristics of the TFTs under different drain voltages. Dimension of TFT: L×W=2 µm×25 µm. (a) I_{DS}~V_{GS} curve, (b) I_{DS}~V_{DS} curve.](image)

The electrical characteristics of the TFTs with L×W=2 µm×25 µm are shown in Figure 4.12. The on/off current ratio of $10^8$, threshold voltage of 1V, subthreshold slope of 200 mV/decade were measured. The $I_{DS}~V_{DS}$ curve shows that the devices work in enhancement mode. When comparing the transfer curves of different drain voltages, it was noticed that the $V_{on}$ reduces from -1.12V for $V_{DS}=1V$ to -1.32V for $V_{DS}=10V$. The $V_{on}$ shift of -0.2V for $V_{DS}=1V$ and 10V were also observed for devices with L=7 µm and L=17 µm. This negative threshold voltage shift is similar to drain induced barrier lowering (DIBL) in MOSFETs, but the mechanism is not exactly the same. The IGZO TFTs fabricated in our lab are n-type accumulation devices. The positive bias applied to the drain would accumulate some electrons around the drain terminal, which forms a shorter effective channel length than
nominal length, the higher drain voltage, the shorter effective channel length. Therefore the turn-on voltage is smaller with the higher drain bias than that with lower drain bias.

Figure 4.13 Comparison of transfer curves for different channel lengths (a) Transfer curves. (b) The relationship of V\text{on}, saturation current I\text{DS} with different channel lengths.

The transfer curves measured at V\text{DS}=10V of L=2 µm, 7 µm and 17 µm are shown in Figure 4.13 (a). It can be found that the V\text{on} is smaller when the channel length becomes shorter, dropping from -0.93V for L=17 µm to -1.32V for L=2 µm, which is also a typical short channel effect. The saturation current increases as the channel becomes shorter, even the channel width is smaller for the shorter channel lengths. This should be due to the increase of carrier mobility. No decay of the subthreshold slope was observed for the short channel devices, and 200 mV/decade was measured for all the three channel lengths.
The devices discussed in this section were fabricated by traditional photolithography. The smaller devices fabricated by focused ion beam (FIB) milling with channel length less than 1 µm will be discussed in Chapter 6.

4.10 Conclusions

In this chapter, first the design of different structures and different types of devices were overviewed, then several parameters to optimize the device performance were measured and discussed.

1. Oxygen partial pressure is important to control the device parameters. Lower oxygen partial pressure will result in higher on drain current, smaller threshold voltage, and higher mobility.

2. The thickness of the IGZO channel layer is also an important parameter to control device performance. Too thick of a channel layer will result in negative threshold voltages and make it hard to deplete channel layer, while too thin of a channel layer will result in a large hysteresis window and very low mobility. In our study, a 35nm channel layer deposited at 25mT oxygen partial pressure was found to be the best for TFTs applications.

3. The channel dielectric must be larger than a critical thickness to reduce the gate current. This thickness depends on the application, for $V_{GS}>15V$, a gate dielectric larger then 50nm is needed for the Al$_2$O$_3$ layer. For the larger devices, the gate dielectrics are usually around 100nm, because IGZO and other metal oxide channel layers are amorphous materials.
4. In TFTs, larger channel and source/drain overlap usually helps to inject more carriers. However, our study showed that half overlap and full overlap didn’t make a tremendous difference in the current-voltage curves.

5. Different source/drain materials were examined. Metals such as Mo and Ti have lower contact resistance than ITO.

6. A patterned gate design gives a low parasitic capacitance, while a patterned gate will lead to hump in transfer characteristics for the ITO source/drain.

7. Device stability was also examined. Leaving the device exposed to the atmosphere will result in a positive shift of threshold voltage, due to the oxygen atoms that were attracted to the IGZO channel surface.

8. Annealing is an effective way to reduce interface defect density states between the semiconductor and the dielectric. 400 °C is the best annealing condition for the IGZO channel layer.
Chapter 5
LOGIC GATES

The content of this chapter were published in condensed form in IEEE Device Letter 2012.

Transparent IGZO logic gates

Haojun Luo, Patrick Wellenius, Leda Lunardi and John Muth,

5.1 Abstract

Optically transparent indium gallium zinc oxide (IGZO) based logic gates inverters, NAND, and NOR gates were fabricated and characterized, using transistors deposited at room temperature with 5, 10 and 20 µm gate lengths and a beta ratio between 2.5 and 40. The NAND and NOR gates operation frequencies were measured up to 5 kHz. The individual transistors were measured to have saturation mobilities of 14 cm²/Vs, sub-threshold swings of 190 mV/decade, and current on/off ratios in excess of 10⁸. Logic operations were satisfactorily demonstrated for bias voltage between 1 and 20 V. These results indicate viable digital logic can be applied particularly where optical transparency or the use of novel flexible substrates is more important than the operating speeds.
5.2 Introduction

Amorphous oxide-based semiconductor thin film transistors (TFTs) have stimulated considerable industrial and academic research because of higher electron mobilities when compared to silicon and organic counterparts, transparency and potential applications on flexible substrates [82]. Most of the research has been focused on display applications due to the large potential market [83], [84] or on the performance of discrete devices [85]-[90]. Few reports have been published on inverters or ring oscillators using oxide semiconductors [49]-[51]. Presley et al. reported the first amorphous oxide semiconductor (AOS) based ring oscillator with a peak oscillation frequency of 9.5 kHz [49]. Recently IGZO-based fully transparent ring oscillators were reported with 2 MHz operating frequency [50] and OR gates at 10 Hz [52]. All oxide CMOS type inverters were reported by Nomura et al. and Martins et al. [53], [54]. Yet to our knowledge standard extensively used logic gates such as NAND and NOR gates have not been reported on AOS-based transistors. While easy to build they represent the fundamental blocks for most Boolean functions and therefore for all digital integrated circuits.

In this chapter, transparent amorphous oxide digital logic with all layers, including interconnects, composed of oxides are reported. All NAND, NOR gates and inverters, basic building blocks of digital logic, are demonstrated here, showing high gain and fast response compared to amorphous silicon or amorphous organic semiconductor devices of comparable dimensions. These results indicate that IGZO digital logic is suitable for particular applications where optical transparency or substrate flexibility could be sought.
5.3 Experimental Approach

A cross-section illustration of the device is shown in Figure 5.1 (a). The ITO (130 nm, 30 Ω/□) coated glass was used as the substrate. The bottom ITO gate electrode was formed by BCl₃ reactive ion etching (RIE), a dry etch at 100W forward power for 20 minutes. A 100 nm Al₂O₃ dielectric layer was then grown by atomic layer deposition (ALD) at 200 °C. In order to reduce the leakage current, the Al₂O₃ film went through rapid thermal annealing at 600 °C for 60 s in N₂ ambience. The Al₂O₃ dielectric layer is then patterned by conventional photolithography and etched by BCl₃ RIE. About 35 nm thick amorphous IGZO channel layer was deposited by pulsed laser deposition (10 Hz, 155 mJ/pulse) in oxygen pressure of 25 mTorr at room temperature. The composition of the IGZO layer is Ga₂O₃:In₂O₃:ZnO=1:1:10 (In:Ga:Zn=1:1:5). Preparation of the target used has been described in detail in chapter 3 (section 3.1). 100nm ITO source/drain contacts and interconnects were then deposited by pulsed laser deposition at room temperature.

Figure 5.1 (a) Cross section of IGZO TFTs. (b) Image of IGZO based all oxide transparent TFTs and logic gates on glass substrate.
An image of IGZO based all oxide transparent TFTs and logic gates on glass substrate is shown in Figure 5.1 (b). It can be seen that the sample is transparent. One can easily see through and the words underneath are very clear. The transparency of all stacks is higher than 80%.

5.4 **Discrete Transistor Characteristics**

Electrical characteristics of individual transistors were shown in the Figure 5.2(a) and (b). At $V_{DS} = 5$ V, a threshold voltage of 0.2 V, a subthreshold slope of less than 190 mV/decade, an on/off current ratio larger than $10^8$, and a saturation field effect mobility $\mu_{sat}$ of $14 \text{ cm}^2/\text{Vs}$ were measured. The off state current is less than 1 pA, mainly due to gate leakage. The TFT transfer characteristics show enhancement mode operation allowing the realization of simple circuits without the necessity of level shifting. The low threshold voltage and small value of subthreshold swing allow the device to operate as low as 1.5 V, indicating promise for low-power applications, and significant future progress in energy efficiency. The devices also operated at higher voltages, making them compatible with many current integrated circuits. The hysteresis window is very small, less than 0.1V, indicating that there is low interface states density at ITO /Al$_2$O$_3$ interface and Al$_2$O$_3$ / IGZO interface.
Figure 5.2: (a) Log $(I_{DS})$ – $V_{GS}$ and log$(I_G)$ – $V_{GS}$ at $V_{DS}=5$ V for IGZO TFTs. The plot also has the gate leakage, $I_G$, as a function of the gate bias. (b) Drain current- Drain voltage ($I_{DS}$-$V_{DS}$). The TFT has Al$_2$O$_3$ as the gate dielectric and the IGZO channel is deposited at oxygen partial pressure of 25 mTorr. TFT dimensions, W/L = 50/10 μm.

5.5 **Inverter**

Inverters, the most elementary integrated circuit investigated here, were fabricated by connecting a load transistor operating in saturation mode ($V_{GG}=V_{DD}$) to a drive transistor. Figure 5.3(a) shows a photo image of an inverter. In this work, inverters with different channel lengths have been fabricated, including L=20 μm, L=10 μm and L=5 μm, and an overlap between gate and source/ drain contact of 2.5 μm and 5 μm. Figure 5.3(b) shows the schematic diagram of the inverter. The load transistor is always on, connecting the $V_G$ to the $V_{DD}$. The size of the load transistor is much smaller comparing to the drive transistor. In this study, the W/L of the load transistor is kept at 1, i.e., L=W=20 μm or L=W=10 μm or L=W=5 μm. While the drive transistors have bigger size, W/L ratios in this study include 2.5,
5, 10, 20, and 40. Since the load transistors have the W/L ratio equal to 1 (W_{load}=L_{load}) The W/L ratios of the drive transistors are also the beta ratios of the inverters.

![Image of an inverter](image1)

**Figure 5.3:** (a) A photo image of an inverter, Load transistor dimension is W/L=10 µm /10 µm, drive transistor dimensions are 200 µm /10 µm. (b) Schematic diagram of inverter.

Figure 5.4(a) shows the voltage transfer curve of an inverter using a load transistor with L=20 µm, W=20 µm and drive transistor with L=20 µm and W=400 µm. Switching from the high to the low state was observed for V_{DD}=1, 2, 5, 10, and 20 V. Full swing of the output from near 0 V to V_{DD}-V_{th} was also observed for all voltages. Figure 5.4(b) shows the transfer curves of inverter fabricated by Arun [91]. It could be noted that the transfer curves in this study are much steeper. This indicates that the inverters in this work can switch from output high to output low in a shorter time, i.e., can be operated faster.
Figure 5.4: (a) Schematic diagram and voltage transfer curve of an inverter at V=1V, 2V, 5V,10V and 20V (L_{drive}/W_{drive}=20 µm/400 µm, L_{load}/W_{load}=20 µm/20 µm. OL=2.5 µm), this study. (b) Transfer curve for a transparent inverter fabricated using IGZO TFTs for different values of V_{DD} (L_{drive}/W_{drive} = 20 µm /400 µm, L_{load}/W_{load} =20 µm /40 µm, OL=2.5 µm) [91].

Parameters such as peak gain magnitude and noise margin are very important information to understand the operation of an inverter. Figure 5.5 shows the use of this inverter operated at V_{DD}=20 V as an example to analyze inverter parameters. Peak gain magnitude (gain=dV_{OUT}/dV_{IN}) can be extracted by taking the differential slope from the output transfer characteristic. For this inverter peak gain magnitude is as high as 18.4, which is considered high for an amorphous oxide semiconductor inverter. The noise margin in high state NM_{H} (NM_{H}= |V_{OH}-V_{IH}|) and low state NM_{L} (NM_{L} = |V_{IL}-V_{OL}|) were determined to be 18.2 V and 0.7 V, respectively. The transition width (V_{IH}-V_{IL}), which indicates the undefined logic state region, is as small as 2.2 V. These parameters show that the inverter has high output voltage for the high state and very low output for the low states.
In order to compare the device performance with different beta ratio, inverters with different beta ratio were fabricated. Figure 5.6 shows the transfer curves of inverters with channel length of 20 µm and different beta ratios. It was observed that for the same gate length, a larger beta ratio results in a sharper transfer curve. This is because the larger gate width of the drive transistor, a larger current is allowed to pass through the transistor when the gate voltage is high. Therefore the discharge process is faster. For a similar reason, the output off state voltage was lower for higher beta ratios. The larger device width results in a larger input capacitance. Thus it will take a longer time for the load transistor to charge that input capacitance when the input voltage changes from high to low.
The gain magnitude is an important parameter for an inverter. The gain of an inverter must be larger than 1 in order to be applied to ring oscillators. Figure 5.7(a) shows the relationship between supply voltage and the gain. The gain magnitudes are calculated from the transfer characteristics shown in Figure 5.3 (a). For the devices in this study, higher supply voltages will result in higher gain. Figure 5.7(b) shows an example of the relationship between gain and beta ratio at \( V_{DD} = 5 \text{V} \). The gain magnitudes are calculated from the transfer characteristics shown in Figure 5.6. From the images, it is clear that higher beta ratio will lead to higher gain. This is consistent with the theoretical prediction, and the origin of this has been explained in the previous text.
Figure 5.7: Relationship between inverter gain and supply voltage, \( V = 1 \text{V, 2V, 5V, 10V and 20V} \) \((L_{\text{drive}}/W_{\text{drive}}=20 \ \mu \text{m} /400 \ \mu \text{m}, \ L_{\text{load}}/W_{\text{load}}=20 \ \mu \text{m} /20 \ \mu \text{m}, \ OL=2.5 \ \mu \text{m})\); (b) Relationship between inverter gain and beta ratio. \( V_{\text{DD}}=5\text{V} \), Channel length \( L=20 \ \mu \text{m} \), beta ratio \( \beta=2.5 \), \( \beta=5 \), and \( \beta=20 \).

5.6 NAND Gate

In CMOS technology, the NAND gate is constructed by two PMOS transistors connected in parallel and two NMOS transistors connected in series. For the amorphous oxide based transistors, only NMOS devices are used to construct the logic gates. In this work, the NAND gate was realized by a series connection of two drive transistors and a load transistor. The load transistor was operated in saturation mode by connecting the drain and gate bias to \( V_{\text{DD}} \). An optical micrograph of a fabricated NAND gate is shown in Figure 5.8 (a). The schematic diagram of the NAND gate is shown in Figure 5.8(b).

A variety of devices with different gate lengths \((L=5 \ \mu \text{m}, 10 \ \mu \text{m}, 20 \ \mu \text{m})\), beta ratio \((\beta=2.5, 5, 10, 20, 40)\) and different gate and source/drain overlaps \((\text{overlap}=5 \ \mu \text{m}, 2.5 \ \mu \text{m})\) were fabricated.
The performance of the NAND and NOR gates under DC bias static and dynamic inputs were characterized. For the static characterization, a HP 4142 B semiconductor analyzer and two DC power supplies were used. The measurements were taken by keeping one input to either constant high DC voltage or connect to ground, and sweeping voltage from negative to positive on the other input and measuring the output.
Figure 5.9: Voltage transfer characteristics for a NAND gate (\(W_{\text{drive}}/L_{\text{drive}}=20\,\mu\text{m} / 200\,\mu\text{m}, \ W_{\text{load}}/L_{\text{load}}=20\,\mu\text{m} / 20\,\mu\text{m}\)).

Figure 5.10: Voltage transfer characteristics at different supply voltages (\(W_{\text{drive}}/L_{\text{drive}}=20\,\mu\text{m} / 200\,\mu\text{m}, \ W_{\text{load}}/L_{\text{load}}=20\,\mu\text{m} / 20\,\mu\text{m}\)).
A typical DC voltage transfer characteristic of NAND gate is shown in Figure 5.9. The dimension of the load transistor is \( W/L = 20/20 \, \mu m \), while the dimension of drive transistor is \( 200/20 \, \mu m \). The overlap between gate and the source/drain is \( 2.5 \, \mu m \). For \( V_{DD} = 5 \, V \), if the input \( V_A \) was low (0 V), the output was high, close to 4.9 V. If the input \( V_A \) was high (\( V_A = V_{DD} \)), the transistor A is on, therefore the NAND gate acted like an inverter.

When applied at different supply voltages, this NAND gate shows correct function from 1V to 10V. The output voltage is always high if one input is low, i.e., one of the drive transistors is off. The NAND gates could be operated as low as 1V, indicating that these logic gates could be used in future low power system applications. On the other hand, the NAND gates and inverters can also be operated at 10V, implying that these logic gates can be also used in high power high breakdown voltage applications.

Figure 5.11 shows voltage transfer characteristics of the NAND gate with different beta ratios. Comparing these transfer curves of NAND gates with those of same channel length and different beta ratios, the NAND gate with smaller values of \( \beta \) show shallower transfer characteristics, consistent with theory. For the NAND gate with \( \beta = 2.5 \) (\( L_{drive}/W_{drive} = 10 \, \mu m/25 \, \mu m \)) the output voltage drops from 4.9 V to less than 1 V for the input \( V_{DD} = 5 \, V \), while for the NAND gate with \( \beta = 40 \) (\( L_{drive}/W_{drive} = 10 \, \mu m/400 \, \mu m \)) the output voltage drops from 4.9 V to less than 0.1 V.
Figure 5.11: Voltage transfer characteristics of IGZO based NAND gate with different beta ratios (L=10 µm, β=2.5, 10, 40.)

The gate source/drain overlap has been designed to be 2.5 µm and 5 µm. The devices with 5 µm overlap have shallower transfer characteristics and slower response speed due to the larger input capacitance.

In order to test the dynamic performance of the logic gate, two square input signals (V_A=V_B=10 V) from two waveform generators were directly applied to the two input terminals. The supply voltage V_DD was 10V. The schematic of the experimental setup is shown in Figure 5.12.
The output waveforms of typical NAND gate operating at 100Hz, and 5 kHz are shown in Figure 5.13 (a) and (b). In this setup no level shifter or output buffer was used.

For the NAND gate, the output was low only when both inputs were high. If any of the inputs were low the output was high. From Figure 5.13, for the 100 Hz frequency, the output waveform is sharp, without any difference between the rise and fall times. At the frequency of 5 kHz, the rise and fall times of the NAND gate are 78 μs and 8 μs, respectively. The rise time is much larger than the fall time. This implies that the limitation of this circuit for operating at higher frequency is the charging time. Smaller gate source/drain overlap and reducing the resistance of interconnects could help to reduce the RC time constant and
improve operating speeds. The speed of the NAND gate was as high as 5 kHz, much faster than earlier reported OR gate results [52].

Figure 5.13: Output and input waveforms of a NAND gate \((W_{\text{drive}} / L_{\text{drive}} = 400 \, \mu m / 10 \, \mu m, W_{\text{Load}} / L_{\text{Load}} = 10 \, \mu m / 10 \, \mu m, \text{overlap} = 2.5 \, \mu m)\) operating at (a) 100Hz, and (b) 5kHz. \(V_{\text{DD}} = 10 \, V\).
5.7 **NOR Gate**

In contrast to the NAND gate, the NOR gate is constructed by two parallel drive transistors connected to a load transistor. An optical image of a NOR gate is shown in Figure 5.14(a) and the schematic diagram of the NOR gate is shown in Figure 5.14(b).

![Figure 5.14: (a) Optical micrographs of NOR gate, (b) The schematic diagram of NOR gate.](image)

A series of typical voltage transfer curves for a $\beta=2.5$ ($W_{\text{drive}} / L_{\text{drive}} = 25/10 \, \mu m$, $W_{\text{Load}} / L_{\text{Load}} = 10/10 \, \mu m$, overlap=2.5 $\mu m$) NOR gate is displayed in Figure 5.15. If one of the inputs $V_A$ was high, the output voltage was always low regardless of the voltage applied to the other input. The output voltage is lower than 0.1V, indicating a strong pull down capability of the
drive transistor. If the input $V_A$ was low, the NOR gate acted like an inverter. Similar to the NAND gate, the NOR gate displayed sharp transfer characteristics. For $V_{DD}=5$ V, the output voltage dropped from 4.9 V to less than 0.1 V when input $V_B$ is scanned from low to high.

Figure 5.15: Voltage transfer characteristics of a NOR gate (L/W=10 µm /25 µm. $V_{DD}$=5V).

DC voltage transfer characteristics of NOR gates with same channel length and different beta ratios are shown in Figure 5.16. In this example, the channel length is L=10 µm, while beta ratios range from $\beta = 2.5$ to $\beta = 10$, respectively. All the NOR gates show satisfactory function, and are very similar. The device with a larger beta ratio has sharper transfer curves, because the larger channel width enables a stronger pull down capability.
Figure 5.16: Voltage transfer characteristics of IGZO based NOR gates with different beta ratios (L=10 µm, β=2.5, 5, 10).

Similar to NAND gates, the NOR gates dynamic performance is also tested. The testing set up schematic is shown in Figure 5.12. The output waveforms of a typical NOR gate operating at 100Hz and 5 kHz are shown in Figure 5.17. The sizes of this NOR gate are $W_{\text{Drive}}/L_{\text{Drive}} = 100 \, \mu\text{m}/10 \, \mu\text{m}$, $W_{\text{Load}}/L_{\text{Load}} = 10 \, \mu\text{m}/10 \, \mu\text{m}$, overlap=2.5 µm. From the curves, for the frequency at 100 Hz, the output waveform is sharp, without a significant difference between the rise and fall times. At the frequency of 5 kHz, the rise and fall times of the NOR gate are 52 µs and 12 µs, respectively. The rise time is much larger than the fall time, implying again that the limitation of NOR and NAND gate for operating at higher frequency is the charging time.
Figure 5.17: Dynamic waveform characterization of a NOR gate ($L_{\text{Drive}} = 5 \, \mu m$, $W_{\text{Drive}} = 100 \, \mu m$, $L_{\text{Load}} = 5 \, \mu m$, $W_{\text{Load}} = 5 \, \mu m$, 2.5 $\mu m$ overlap) operating at (a) 100Hz and (b) 5 kHz.
5.8 Discussion

The operation speed of the NAND and NOR gates was as high as 5 kHz, much faster than earlier reported OR gate results [52]. However, further increasing the channel width of the load transistor or decreasing the capacitance of the drive transistor could reduce the charging time. Decreasing gate source/drain overlap and reducing the resistance of inter-connects could reduce the RC time constant and improve operating speeds.

The logic gates in this work were constructed with only n-type TFTs. The n-type circuits have a lower transistor count than complementary circuits, but tend to dissipate higher static power.

The above results indicate that amorphous oxide semiconductor based logic gates are viable as the integrated circuit technology for particular applications and transparent systems on glass or plastics. Due to the relatively low operating frequency and high capacitance compared to other high frequency integrated circuit technologies, those applications may be constrained to areas specifically not requiring fast response. However, the high electron mobility observed in amorphous IGZO films so far promises further increase in the circuit speed. By scaling down the device dimensions, optimizing the circuit design, reducing parasitic capacitance and interconnect resistance could lead to higher maximum operating frequency. The low threshold voltage and small sub-threshold swing permit stable logic operation at low voltages, indicating progress in energy efficiency. Furthermore, the logic gates were demonstrated to function over a range of voltages indicating that they can be easily integrated with a variety of current integrated circuit technologies.
5.9 Conclusions

In this chapter, transparent amorphous IGZO based NAND and NOR gates were realized. First, the individual transistors on the same mask were tested. The device parameters with a threshold voltage of 0.2 V, a subthreshold slope of less than 190 mV/decade, a current on/off ratio larger than $10^8$, a gate leakage current less than 1 pA and a saturation field effect mobility $\mu_{\text{sat}}$ of 14 cm$^2$/V·s were extracted. The operation and key parameters of IGZO based inverters were than discussed. A peak gain magnitude of 18.4 was attained. The inverter transfer characteristics under different supply voltages and with different beta ratios were also discussed and analyzed. Finally, the NAND and NOR gates constructed by IGZO based TFTs were demonstrated. These two types of logic gates demonstrated sharp transfer characteristics and satisfactory functionality between 1 and 20 V with operating frequencies reaching 5 kHz. These results are significant and indicate basic digital logic building blocks with high gain and fast response, demonstrating the viability for amorphous oxide digital logic for transparent and flexible electronic systems.
Chapter 6

SUBMICRON OXIDE THIN FILM TRANSISTOR USING
FOCUSED ION BEAM

6.1 Introduction

One of the most important applications of amorphous oxide semiconductors (AOSs) based TFTs is flat panel displays, which requires large scale uniformity. However, in applications such as transparent circuits, smaller devices are faster and enable more compact circuits. For example, for IGZO TFTs based 3-D stack memory [5], smaller devices means it is possible to integrate more devices in a unit area.

At the same time, it is important to examine electrical characteristics of amorphous oxide based TFTs when the channel is extremely short. This area has not been intensely studied but the new effects and the physics behind this need to be examined and understood.

In academic research, the conventional way to make a submicron device is using electron beam lithography. It requires coating a polymer onto the sample surface, loading the sample into a vacuum chamber, designing a mask file and converting the file into SEM, alignment under SEM, optimizing the exposure dose and exposing the pattern by the electron beam. It usually needs to test and optimize the exposure dose for different pattern sizes. Smaller feature size requires lower current and a slower scan rate. The main drawback of this technique is that it is very slow and very expensive.
In this chapter, we proposed a new method to fabricate submicron oxide thin film transistors using focused ion beam (FIB). There are several advantages for this new technology. First of all, it is photoresist free, the coating of photoresist and preparation of masks for this step can be skipped. Also any lift off or strip step can be skipped, since FIB can be directly used to dice the metal. Secondly, the process is fast compared to E-beam lithography. Depending on the thickness of the metal and the semiconductor layer, the typical etching time of each device is approximately several seconds. Thirdly, it is a room temperature process and can be applied to fabricating oxide based thin film transistors and circuits on flexible substrates. This will open a new window for fabricating small flexible electronics or transparent electronics. As far as we know, this is the first report of using FIB to etch amorphous oxide based submicron thin film transistors.

In the following sessions, the basic principle of FIB will be discussed in 6.2. The experimental detail of devices fabrication will be presented in section 6.3. Depending on the etching depth, two types of FIB etched submicron devices will be discussed in section 6.4 and 6.5, respectively, followed by the conclusion.

### 6.2 Focused Ion Beam (FIB) Etching

A focused ion beam (FIB) system is a powerful tool in nanostructure fabrication. The versatility of resist free FIB patterning allows the fabrication of a wide variety of nanostructures in the sub-micron size range.

The basic FIB instrument consists of a vacuum system and chamber, a sample stage, detectors, gas liquid metal ion source, an ion column delivery system.
FIB systems operate very similarly to scanning electron microscopes (SEM), except that rather than using electron beam in SEM, FIB systems use an electrostatically controlled ion beam that can be operated at low beam currents for imaging or high beam currents for sputtering or milling. The small probe sputtering ability of the FIB is made possible by the liquid metal ion source (LMIS). Gallium is currently the most commonly used ion source, and is used for this work.

As shown in Figure 6.1(a), when the gallium (Ga+) ion beam strikes the sample surface, many species are generated including the sputtered atoms and molecules, secondary electrons and secondary ions. Sputtering occurs as the result of a series of elastic collisions where the momentum is transferred from the incident ions to the target atoms within a collision cascade region. The signal from the sputtered ions or secondary electrons is collected to form an image.

A side effect of the ion beam milling is that the ions can be implanted into the surface of the underlying material. In the case of a gallium beam this layer can be conductive.

The beam spread is not a rectangle distribution. Gaussian distribution is usually used as the first approximation, and deviations from a Gaussian distribution can occur in the low-intensity tails. Figure 6.1(b) shows the cross-section profile of FIB etched silicon pixels, which indicate the beam shape. These profiles can be fitted very well for the central core with a Gaussian function.
Figure 6.1: (a) Illumination of FIB sputtering, drawing based on [92]. (b) SEM images of silicon single pixel etched by straight line scan and fitting the trench cross-section profile with a Gaussian function [93].

6.3 Devices Fabrication and Experiments

The devices were fabricated on a heavily doped p⁺-type silicon substrate with 100nm of thermally grown SiO₂. The silicon substrate is used as the bottom gate with a sheet resistance of Rs=0.001–0.005 Ωcm. About 40nm of IGZO was deposited by pulsed laser deposition (PLD) as a channel layer (In: Ga: Zn =1:1:5 atom ratio). The oxygen partial pressure was 25mT during deposition. A 120nm Ti layer as the source/drain and contact pads was deposited by E-beam evaporation and was patterned by a conventional photolithography process. The source / drain terminals were intentionally connected together before FIB etching.
An FEI Quanta 3D FEG with live SEM imaging and FIB milling dual beam system is used in this study. During the fabrication, the focused Ga\(^+\) beam was used to mill a narrow gap between the source and drain. This gap defines the channel length. The width of the Ti layer on top of IGZO defines the channel width. This width of W=4\(\mu\)m is kept constant for all devices in this study. The acceleration voltage of 30 KeV and beam current of 30 pA were used for this FIB milling process. Figure 6.2 shows the 3D device structure and the FIB etching process.

![Cross section of device structure and illustration of the FIB etching process.](image)

Figure 6.2: Cross section of device structure and illustration of the FIB etching process.
The IGZO underneath the Ti layer is designed to be $10\mu m \times 4\mu m$. It is wider than the Ti width which is $4\mu m$ for protecting the SiO$_2$ dielectric layer during the etching process. The overlap of IGZO and Ti is about $2\mu m$ on the source and drain for carrier injection.

Figure 6.3 shows the images of devices before and after FIB etching. Figure 6.3(a) shows the devices before FIB etch. The Ti metal is on top of the IGZO layer. After the FIB diced through the metal Ti, the source and drain were separated, and the transistor was made.

Figure 6.3: Device top surface SEM Images of (a) device before FIB etching, and (b) device after FIB etching (tilted angle).

6.4 **Amorphous Oxide Side Channel TFTs Etched by FIB**

If the focused Ga$^+$ beam etches all the IGZO in the gap, there is still IGZO side channel on each lateral side. When the gate terminal is positively biased, the electrons will accumulate near the IGZO/SiO$_2$ interface. If the source is grounded and a positive voltage is applied to
the drain terminal, the current will flow through the lateral IGZO channel to the source, as illustrated in the Figure 6.4 (a). We name this type of structure side channel thin film transistors.

6.4.1 Right after FIB Etching

Figure 6.4(b) shows a cross sectional view at the gap of a side channel TFT. It is clear that the ion beam etched away the Ti layer and the IGZO layer, and the etched profile is a Gaussian curve shape. When the nominal gate is 20nm wide, the actual gap of the IGZO is about 50nm. The SiO₂ was also etched away.

Figure 6.4: (a) Illustration of current flow when the device is on state, \( V_G > V_T, V_{DS} > 0 \), (b) cross section of a lateral TFT etched by FIB.
These amorphous oxides based lateral TFTs etched by FIB still have the advantages mentioned before, i.e., photoresist and mask free processing, ease of fabricating short channel devices compared to the E-beam lithography method, and room temperature compatibility. In the following section, we will discuss the electrical properties of this type of device.

Figure 6.5(a) shows the transfer characteristic of a 4 $\mu$m $\times$ 20nm (20nm is the nominal channel length) device right after FIB etching. The gate leakage is very high. This should be due to the gate oxide being etched through, and also that some Ga$^+$ ions residual are on the surface of the gap surface, resulting in a high gate current. This is confirmed by the negative $I_D$ when the gate bias is higher than 7V. Negative $I_D$ means that the current is flowing into the drain terminal instead of flowing out. This is due to the fact that gate bias is higher than drain bias which is 3V.

![Figure 6.5](image)

Figure 6.5: (a) Transfer characteristic ($V_D$=3V), (b) output characteristics of a thin film transistor ($W/L=4\ \mu m/20nm$) after FIB etching.
The output characteristics of this device after FIB etching are shown in Figure 6.5(b). The IV curves are similar to a resistor. The channel resistance is about 200kΩ and the gate voltage can barely modulate the source drain voltage. We speculate that there are some residual Ga\(^+\) ions on the surface of the channel, making the channel very conductive.

6.4.2 After Annealing in Air at 200 °C for 30 min

After annealing this device in air at 200 °C for 30 min, the device characteristics changed from resistor type to n-type enhancement mode transistor. Figure 6.6(a) shows the transfer characteristics of this IGZO TFT with channel lengths of 20nm and a width of 4 μm, at drain voltage of 0.1V and 3V. The on-off current ratio is larger than 10\(^4\), the on current is able to reach 5.5 μA for V\(_{DS}\)=3V. V\(_{on}\) is ~3.0V and the subthreshold swing is estimated to be 1.52V/decade. The maximum gate leakage reduces from 3.1×10\(^{-4}\) to 1.8×10\(^{-9}\)

![Figure 6.6: (a) Transfer characteristics (V\(_{DS}\)=3V), (b) output characteristics of a thin film transistor (W/L=4μm/ 20nm) etched by FIB and annealed at 200 °C in the air for 30 min.](image)
Fig. 6.6 (b) shows the output characteristics of this TFT, under various gate voltages. The IGZO TFTs show the n-type enhancement mode and exhibit a hard saturation. The drain current of 5.5 μA could be reached with drain voltages at 10 V and gate voltage of 9 V.

Figure 6.7 shows $I_{DS}^{1/2}$ vs. $V_{GS}$, from this curve in the saturation mode ($V_{DS}=3$ V), the threshold voltage was estimated to be 0.9 V.

From these observations, after 200 °C annealing, most of the Ga$^+$ ions on the surface of the channel were evaporated or oxidized by annealing in the air. The transistors started to show transistor characteristics. But we speculate that there were still a small portion of Ga$^+$ ion residual on the surface and on the edge of IGZO thin film. Therefore the performance of the transistor is not fully recovered.

Figure 6.7: $\sqrt{I_{DS}}$ vs. $V_{GS}$ characteristic of an IGZO TFT etched by FIB, followed by annealing at 200 °C for 30min. W/L=4μm/ 20nm. Bias condition $V_{DS} = 3$ V.
6.4.3 After Annealing in Air at 300 °C for 30 min

After increasing the annealing temperature and annealing this device at 300 °C in air for 30 min, the device showed better IV characteristic compared to those annealed at 200 °C.

Figure 6.8(a) shows the transfer characteristics of this IGZO TFT at drain voltage of 0.1 V and 3 V. The on-off current ratio is larger than $10^7$, the on current is able to reach 7 μ A for $V_{DS}=3$ V. $V_{on}$ is $\sim 1.6$ V and subthreshold swing is estimated to be 270 mV/decade. The maximum gate leakage further reduced from $1.8\times10^{-9}$ to $\sim 10^{-13}$, which is almost the same level with the un-etched normal process TFTs.

Figure 6.8: (a) Transfer characteristics ($V_D=3$ V), (b) output characteristics of a thin film transistor (W/L=4μm/ 20nm) etched by FIB and annealed at 300 °C in air for 30 min.

Figure 6.8(b) shows the output characteristics of this TFT under various gate voltages. The IGZO TFTs show the n-type enhancement mode and exhibited a hard saturation. The drain current increased from 5.5 μA to 8.8 μA with drain voltages at 10 V and a gate voltage of 9 V.
Figure 6.9 shows $I_{DS}^{1/2} - V_{GS}$, from the curve in the saturation mode ($V_{DS}=3$V). The threshold voltage is estimated to be +1.57V.

From these experimental results, we conclude that after 300°C annealing, almost all of the Ga$^+$ ions on the surface of the etching gap were either evaporated or oxidized or became interstitials by annealing at 300 °C. The damage due to the Ga$^+$ implantation was fully recovered and the transistor characteristics are further improved.

6.4.4 After Annealing in Air 350 °C for 30 min

After annealing at 350 °C for 30 min, the device's electrical characteristics are further improved and reach the best performance.

As shown in Figure 6.10 (a), the on-off current ratio is larger than $10^8$, the saturation on current is further increased from 7μA to 11.3 μA for $V_{DS}=3$V at $V_{GS}=15$V. $V_{on}$ is ~-1.6V, similar to annealing at 300 °C. While the subthreshold swing was reduced to 170mV/decade,
small subthreshold swing means that this device can be turned on very fast. The maximum
gate leakage remains $\sim 10^{-13}$ A, which is similar with the un-etched normal process TFTs.

Figure 6.10: (a) Transfer characteristics ($V_D=3$ V), and (b) output characteristics of a thin film transistor ($W/L=4 \mu$m/ 20nm) etched by FIB and annealed at 350 ºC in the air for 30 min.

Figure 6.11: $\sqrt{I_{DS}}$ vs. $V_{GS}$ characteristics of an IGZO TFT by FIB, then annealed at 350 ºC for 30 min. Biased in the saturation regime with $V_{DS} = 3$ V, $W/L=4 \mu$m/ 20nm.
Figure 6.11 shows $I_{DS}^{1/2}$ vs. $V_{GS}$, the $V_{th}$ is estimated to be -0.5V, reduced from +1.5V at 300 °C, due to the smaller subthreshold swing. And the drain current is further increased to 10.8 μA at $V_{DS}$=10 V and $V_{GS}$=9V.

6.4.5 After Annealing in the Air at 400 °C for 30 min

This device's performance degraded after annealing at 400 °C. The transfer characteristics and output characteristics are shown in Figure 6.12.

Although the drain current increased to 15.7 μ A at $V_{DS}$=3V and $V_{GS}$=15V. $V_{on}$ decreased to -6.2V and increased hysteresis was observed. The degraded performance was due to the oxidization of the source drain metal Ti and increased contact resistance between the Ti and the IGZO increased. Another possible reason for degradation is that the IGZO thin
film at the corner of the etching gap appeared to be damaged by the large voltage, high current measurements. This was confirmed by the SEM observation after repeated measurements of the devices, as shown in Figure 6.14.

Figure 6.13: \( \sqrt{I_{DS}} \) vs. \( V_{GS} \) characteristics of an IGZO TFT by FIB, then annealed at 400 °C for 30 min. Biased in the saturation regime with \( V_{DS} = 3 \) V, \( W/L=4\mu m/20nm \).

Figure 6.14: SEM image shows the IGZO damage at the corner of etching gap, after repeating high voltage, high current measurements.
6.5 Discussion

Besides the nominal etching gap of 20nm, other values from 50nm to 500nm were also etched. All these devices exhibited a similar trend with the nominal L=20nm devices. This implies that the FIB etching technique is repeatable.

Figure 6.15 shows the $I_D$-$V_G$ curves of the devices with different etching gaps after annealing at 350 °C. These curves are almost identical because the area of the IGZO lateral area is almost the same. Also the distance between source and drain depends on the shortest lateral path, and this distance is slightly larger than the channel gap.

Figure 6.15: Comparison of TFTs with different gaps after annealing at 350 °C.
Figure 6.16 (a) shows the simulation result of electrostatic potential distribution on the device, and figure 6.16(b) shows the simulation result of electron density distribution on the device.
device. It is clear that the corner around the etching gap has a much stronger electric field. Therefore in the side channel TFTs, most of the electrons will transport along the stronger electric field region, i.e., the majority of the electrons will flow from the source to drain along the etching corner.

Figure 6.17: Comparison of \( V_{\text{th}} \), SS, and \( I_{\text{off}} \) at different annealing temperatures, \( V_{DS} = 3 \text{ V} \), \( W/L=4\mu\text{m}/20\text{nm} \).

Figure 6.17 shows the off drain current, subthreshold swing and threshold voltage with different annealing temperature. It is evident that when annealing from 200 °C to 400 °C, the drain off current reduces from \( 1\times10^{-9}\text{A} \) at 200 °C to about \( 1\times10^{-13} \text{A} \) at 350 °C, however, the off current goes higher when annealing at 400 °C due to the degraded semiconductor quality and higher metal semiconductor contact resistance. However, from 200 °C to 350 °C, the
subthreshold slope decreases from 1.5V/decade to 170mV/decade, indicating these devices should be suitable for circuit applications.

From above discussion, the IGZO based TFTs have conductive channel and large gate leakages right after the FIB etching due to the residual Ga+ ions on the surface of the etching gap and the damage of the gate dielectric by ion implantation. After annealing at 200 °C, the TFTs started to show n type enhancement mode transistor characteristics. After annealing at 350 °C, the devices showed the best performance. The on off drain current ratio is higher than 10^8, the drain current reaches as high as 11.3 μA at V_{DS}=3V and V_{GS}=15V. SS is as small as 170mV/decade, and the threshold voltage is -0.5V.

For this type of side channel TFT devices, there are two lateral IGZO channels, one on each side. This has potential application to be used as 3-state device if we make a separate gate control on top (bottom) of each channel area to individually control each lateral channel. The current will be 0, I/2, and I.

### 6.6 Devices with Different Etching Depth

In the last section we discussed devices that the IGZO gap was etched by the FIB, leaving the lateral area IGZO to form the side channel. In those devices, the FIB etched into Si layer. After annealing, those devices etched to Si showed transistor behavior at lower annealing temperature and short annealing time. In order to investigate the devices performance under different etching depth, devices with different etching depths were fabricated.

Among different conditions, there are several devices with similar etching depth show double channel characteristics, which will be discussed below.
Figure 6.18 shows the cross section image of a TFT etched by FIB. The nominal etching gap is 20nm. From the image we can see that, the separation between IGZO the source/drain is about 80nm, because the titanium layer is 120nm, and the etching profile is Gaussian. The IGZO layer and thermal oxide layer were almost etched away. But there is a thin layer of native oxide layer underneath the thermal oxide layer.

Figure 6.18: Cross section image of a TFT etched by FIB.

Figure 6.19 shows that transfer characteristics and output characteristic of this TFT right after the FIB etching. These characteristics are very similar with the lateral TFTs right after FIB etching, because there are residual Ga$^+$ ions left on the surface of the etching gap, that
make the channel very conductive. The TFT acts like a resistor. The resistance between source and drain is about $2 \times 10^5 \ \Omega$. From the transfer characteristics, the gate leakage current is in the order of $10^{-5} \ \text{A}$. These mean that there are still some Ga$^+$ ions residual on the surface of the etched profile.

After annealing at 300 °C in air for 30 min, the gate leakage current is reduced from $10^{-5} \ \text{A}$ to $10^{-12} \ \text{A}$ as shown in Figure 6.20 (a). This means that the current path from the gate to source/drain is cut off. This may be due to the damage caused by the Ga$^+$ ion implantation has been recovery after 300 °C annealing, or the Ga$^+$ ions are oxidized into Ga$_2$O$_3$ and form a thin layer of dielectric, or both effects present at the same time.

![Figure 6.19](image_url): (a) Transfer characteristic and (b) output characteristic of direct channel IGZO based TFTs etched by FIB, W/L=4µm/20nm. Measure right after etching at room temperature.
However, the resistance between source drain remains very high, and the output characteristics are shown in Figure 6.20 (b). The transistors still act like a resistor. But, the drain current is much higher for $V_{GS}=9\text{V}$ than that for $V_{GS}=-6\text{V}$. From the transfer characteristic, the on/off drain current ratio is about $10^2$.

In our study, it is observed that for the devices with shallower etching depth, it requires high annealing temperature to reduce the source/drain current, and increase the contrast of on current and off current. While for the devices with deeper etching depth, lower annealing temperature / shorter time can change the source drain from resistor to transistor type, i.e., increase the on-off current ratio. We speculate that the Ga$^+$ ions on the surface of the etching gap form current path between source/drain. And annealing at high temperature, the Ga$^+$ ions are either evaporated or oxidized to cut off the current path between source drain.
Figure 6.21: (a) Transfer characteristic and, (b) output characteristic of direct channel IGZO based TFTs etched by FIB and annealed at 350 °C in air for 30 min, W/L=4 μm/20 nm.

Figure 6.22: \( V_{DS} \) vs. \( V_{GS} \) characteristic of an IGZO TFT by FIB, then annealed at 350 °C for 30 min. Biased in the saturation regime with \( V_{DS} = 3 \) V, W/L=4μm/20nm.

After further annealing this device at 350 °C in the air for 30 min, the device started to show transistor characteristics. Figure 6.21 (a) shows the transfer characteristics of this IGZO TFT at drain voltage of 0.1V and 3V, and the on-off current ratio is larger than \( 10^8 \), the on current is able to reach 4 \( \mu \) A for \( V_{DS}=3V \). \( V_{on} \) is \( \sim 7.6V \) and subthreshold swing is estimated
to be 170mV/decade. The maximum gate leakage further reduced to $10^{-13}$, which is almost the same level with the un-etched normal process TFTs. Figure 6.22 shows $I_{DS}^{1/2} - V_{GS}$. From this figure, it is obvious that there are two turn on points in the curve, the first threshold voltage is -6.2V and the second threshold voltage is -1.0V.

The most interesting point about this device is that two turn-ons voltages are observed in the transfer characteristics. The two turn-on voltages indicate that there are two channels in this transistor. Figure 6.23 shows the comparison of this device and a side channel TFT with same nominal etching dimension. In the transfer characteristics, the drain currents curves are perfectly overlapped for these two TFTs at higher gate bias. This implies that the side channel drain is still dominated in this device. However, there is another channel. This channel has much lower threshold voltage and turns on at -7.6V.

![Graph showing transfer characteristics of direct channel and lateral channel TFTs using by FIB.](image)

Figure 6.23: Transfer characteristics of direct channel and lateral channel TFTs using by FIB.
We speculate that this new channel is formed by the Ga\(^+\) diffusion into a thin layer of SiO\(_2\). This layer is similar to a semiconductor layer, and the gate bias will attract some carriers to accumulate and form a channel between source and drain. But this layer is more conductive than IGZO, which makes the turn on voltage much lower.

When annealing at higher temperature, the device started to degrade, similar to the lateral TFTs etched by FIB.

For the devices with shallower etching depth, leaving IGZO layer still in the channel, the channels were too conductive. And the functional operation of transistor behavior can not be achieved. Further optimization and more research need to be carried out for this target.

6.7 Conclusions

In summary, IGZO TFTs etched by focused ion beam are demonstrated here and the nominal minimum channel length is 20nm but the actual minimum channel length is \(~50\)nm due to the thick metal layer. The devices show n-type enhancement mode accumulation characteristics.

The devices are actually side channel TFTs since the IGZO thin films in the gap are etched through. The electrical characteristics after FIB etching and after different annealing temperature were studied. These devices show low leakage current and large on current after annealing at 350 °C in air. A special case, with another channel on the surface of the gap was also discussed. As far as we know, this is the first report of IGZO based TFT etched by focused ion beam. And this method enables a new method to etch submicron amorphous oxide thin film transistors in a fast, photo-resist free manner.
CHAPTER 7
CONCLUSIONS AND RECOMMENDATION FOR FUTURE WORKS

7.1 Conclusions

This goal of this dissertation is to develop high performance indium gallium zinc oxide based thin film transistors and circuits. To approach this goal, the first step is to develop and optimize the discrete transistor, and study the device physics. After optimization of the single transistors performances, several logic gates including inverters, NAND and NOR gates were designed, fabricated and characterized. IGZO based NAND and NOR gates were first reported by this work. A new method to fabricate submicron IGZO based thin film transistors using focused ion beam is also proposed and demonstrated in this work for the first time. The details of these main results are summarized below:

In order to obtain high performance IGZO based TFTs, many different devices parameters and device structures were investigated. The devices in this work can be categorized as transparent devices fabricated on glass substrates and opaque devices fabricated on silicon substrates.

As the semiconductor channel layer, indium gallium zinc oxide thin films are deposited by pulsed laser deposition in this work. Oxygen partial pressure during the deposition is an important parameter to control the devices performance: higher oxygen partial pressure will result in more resistive films and lower oxygen partial pressure will result in more conductive
IGZO thin films. Devices with an IGZO layer deposited at higher oxygen partial pressure have higher threshold voltages, smaller drain currents and smaller saturation mobilities. To make a good balance between threshold voltage and relative high mobilities and high on current, the oxygen partial pressure was optimized to be between 25mT and 40mT for standard TFTs devices. IGZO thickness is another important parameter that has influence on the device performance. Thicker films will lead to more negative threshold voltage and larger drain on current. Thinner IGZO channel layers will lead to more positive threshold voltage and smaller drain on current. If the thin film is too thin, the degradation of thin film will lead to a larger hysteresis window. The thickness of IGZO was optimized to be about 35-40 nm for standard TFTs applications in this work.

The quality of dielectric layer also plays a very important role in device performance, since the electrons are accumulated at the IGZO semiconductor layer and dielectric layer interface. The quality of this interface determines the device performance. In our study, the ATO layer and the ALD grown AlO_x were the best out of the studied dielectric layers. For the AlO_x gate dielectric, too thin a gate dielectric will lead to large gate leakage current. In our study, the thickness is kept around 100nm in most of the devices. The devices stability and annealing conditions were investigated. Annealing at 400°C for 1 hour is the best condition for annealing IGZO TFTs. The effects of channel length and drain voltage were also studied. Shorter channel length leads to a larger drain current and smaller threshold voltage. Higher drain voltage will also lead to a smaller threshold voltage. This is due to the reduction of effective channel length.
For a typical IGZO TFT on glass with AlO$_x$ gate dielectric, at $V_{DS} = 5$ V, a threshold voltage of 0.2 V, a subthreshold slope less than 190 mV/decade, an on/off current ratio larger than $10^8$, and a saturation field effect mobility $\mu_{sat}$ of 14 cm$^2$/Vs were measured.

After excellent performance of TFTs was achieved, logic gates based on IGZO discrete devices were designed and fabricated. The operation and key parameters of IGZO based inverters were then discussed. A peak gain magnitude of 18.4 was attained. The inverter transfer characteristics under different supply voltages with different beta ratios were also discussed and analyzed. IGZO based NAND and NOR gates were demonstrated and reported for the first time. The static and dynamic performance of logic gates were characterized. These two type of logic gates demonstrated sharp transfer characteristics and satisfactory functionality between 1 and 20 V with operating frequencies reaching 5 kHz. The effects of beta ratio and parasitic capacitance were also discussed. The significance of these results indicates basic digital logic building blocks with high gain and fast response and demonstrates the viability for amorphous oxide digital logic for transparent and flexible electronic systems.

The idea of using focused ion beam to fabricate submicron IGZO based TFTs was proposed in this work. Submicron IGZO TFTs were successfully fabricated and demonstrated. The devices were fabricated on SiO$_2$/Si substrate with a bottom gate structure. The nominal etch gap was 20nm but the actual channel gap is about 50nm due to the thick source drain metal. Right after etching, the current between the source and drain is high and can’t be modulated by the gate bias due to the Ga$^+$ ions residual on the surface of the etching profile. After annealing at 200°C for 30 min in air, the devices started to show transistor
behavior but still exhibited a relatively large leakage current. Further increasing the annealing temperature improves the device performance. After annealing at 350 °C for 30 min in air, an on/off ratio of $10^8$, threshold voltage of 0.2V and subthreshold slope of 170mV/decade were measured. The IGZO in the channel was etched through and these devices are side channel transistors. Different etching depths require different annealing temperatures. A special case, with another channel on the surface of the gap was also discussed.

7.2 Recommendation of Future Research

Based on the results presented in this dissertation there are several future research topics that should be worth further investigation.

1. Focused ion beam etching with He or Ar

The focused ion beam source used in this study is Ga⁺ ion. This makes the etched gap conductive. The oxidization and diffusion of Ga⁺ ions into the IGZO and SiO₂ thin films make the analysis complicated. In the future, we can try to use the FIB with a He or Ar source to etch devices. He and Ar ions are much more stable and hard to react with other elements. This will help to understand the device performance after etching.

2. Further materials and devices study

In this work several parameters that could affect the device performance have been optimized and studied. However, further study on material and devices can be done to better understand the device physics. For example, in chapter 4, a 20nm thick IGZO channel shows large hysteresis window. TEM and SEM can be done to further exam the quality of the thin
film. Also in the annealing experiment, annealing up to 400 °C reduces the hysteresis window and increases saturation current; while annealing at 500 °C decreases the saturation current. Further experiments such as TEM, SEM XRD, and Hall measurement can be performed to better understand the change of the thin film quality and carrier concentration. These information can help to better understand and mechanism and device physics.

3. Development of new indium free channel material

IGZO is one of the most popular oxide materials used in research and it does show excellent performance in devices. However, indium and gallium are increasing expensive. High volume industrial applications will potentially consume a lot of material and they are also very sensitive to price. Potentially, ZnO is a good candidate material. But at present the poly crystalline nature of ZnO limits its performance. However, further investigation on ZnO and other metal alloys should be carried out to develop channel materials that are low cost and suitable for device applications.

4. Long term stability

Long term stability is one of the most important issues before mass production. There are several methods to improve the long term stability: annealing, passivation, optimization of device structure, and choosing a better channel material. The relationship between annealing and defect density, the relationship between device passivation and device performance as well the long term stability need to be further studied and understood. Further optimization of the device structure can also improve the device stability. Finding new materials systems or material structures that will have better device stability is also very important.
To study the long-term stability, there are several conditions that can be investigated, including the device stability under higher temperatures, under various light sources, and under positive bias stress and negative bias stress. Some research about the positive bias stability and the light induced negative bias stress has been carried out [27],[42],[81]. However, more research on these areas needs to be carried out in order to better understand the mechanisms involved and to develop methods to improve the device’s long term stability.

5. Fabrication of submicron devices using E-beam lithography

In this dissertation we proposed a new method to fabricate submicron TFTs. E-beam lithography (EBL) is another useful tool to fabricate submicron small devices. The advantage of EBL is that it won’t introduce any implanted ions. It would be good to compare devices fabricated by FIB and EBL. Figure 7.1 shows the image of an EBL-patterned device. With such a short channel length, the resistance of the channel might be much smaller than the large dimension devices, making it difficult to turn off the device. Therefore the thickness of the channel layer may need to be optimized for such a short channel. Annealing is another way to change the conductivity of the channel.
6. Three Dimensional (3-D) Circuits

Three Dimensional (3-D) device stacks are attracting a lot of research attention recently because the physical scaling of devices is becoming more and more difficult. It is expected that three dimensional stacking could integrate devices more densely. It is also expected that 3D integration will enable one to put multiple functions in each pixel of flexible displays, leading to the realization of sophisticated devices like a foldable display functioned with imaging scanners and health-sensing imagers [94].

A 3D IC could also reduce the global, semi-global wires and interconnect lines, leading to a more efficient pack and wire. 3D integration has already been employed in the state-of-art large scale integrated circuits based on single-crystal Si [95]. Compared to silicon, IGZO has an intrinsic advantage over conventional silicon in 3D technology, because in the silicon
processes, it is difficult to grow high-quality epitaxial silicon over oxide and the processing temperature is high; while for IGZO, the processing temperature could be as low as room temperature and the IGZO film can easily be deposited on the dielectric.

Up to this date, there is no report on 3D circuits based on all AOSs based TFTs. It will be an interesting research project to design and fabricate 3D circuits based on all AOSs TFTs. To start with, an IGZO based 3D stacking inverter and ring oscillators can be investigated first to demonstrate the feasibility of AOSs based 3D circuits. One TFTs layer could be deposited on top of another TFT layer. The disadvantage of 3D circuits is that the processing is complicated. Especially the designs needed to avoid the cross talk between layers and reduce overall steps.

6. Development of p- type oxide based TFTs

In this dissertation, the TFT devices and logic gates are all based on n-type devices. All n-type devices limit the design for complicated circuits and tend to consume more power. The presence of both p-type and n-type devices will make circuit design more flexible and enables low power-consumption circuits similar to complementary metal-oxide-semiconductor (CMOS) technology.

There are several potential candidates for p-type semiconductors such as NiO, CuO, and SnO. The main problems with these p-type semiconductors include:

1) They have low mobility.

2) The p-type doping level is hard to control.

3) It usually requires high temperature annealing to achieve reasonable performance. Further research needs to be carried out to search more possible p-type materials suitable for
p-TFTs. Further study needs to be carried out to further improve the performance of these p-type materials and devices.
REFERENCES


