ABSTRACT

YU, XUNWEI. Power and Energy Management Strategy for Solid State Transformer Interfaced DC Microgrid. (Under the direction of Dr. Alex Q. Huang.)

As a result of more and more applications of renewable energy into our ordinary life, how to construct a microgrid (MG) based on the distributed renewable energy resources and energy storages, and then to supply a reliable and flexible power to the conventional power system are the hottest topics nowadays. Comparing to the AC microgrid (AC MG), DC microgrid (DC MG) gets more attentions, because it has its own advantages, such as high efficiency, easy to integrate the DC energy sources and energy storages, and so on. Furthermore, the interaction between DC MG system and the distribution system is also an important and practical issue. In Future Renewable Electric Energy Delivery and Management Systems Center (FREEDM), the Solid State Transformer (SST) is built, which can transform the distribution system to the low AC and DC system directly (usually home application level). Thus, the SST gives a new promising solution for low voltage level MG to interface the distribution level system instead of the traditional transformer. So a SST interfaced DC MG is proposed. However, it also brings new challenges in the design and control fields for this system because the system gets more complicated, which includes distributed energy sources and storages, load, and SST.

The purpose of this dissertation is to design a reliable and flexible SST interfaced DC MG based on the renewable energy sources and energy storages, which can operate in islanding mode and SST-enabled mode. Dual Half Bridge (DHB) is selected as the topology for DC/DC converter in DC MG. The DHB operation procedure and average model are analyzed, which is the basis for the system modeling, control and operation. Furthermore, two novel power and energy management strategies are proposed. The first one is a
distributed energy management strategy for the DC MG operating in the SST-enabled mode. In this method, the system is not only in distributed control to increase the system reliability, but the power sharing between DC MG and SST, State of Charge (SOC) for battery, are both considered in the system energy management strategy. Then the DC MG output power is controllable and the battery is autonomous charged and discharged based on its SOC and system information without communication. The system operation modes are defined, analyzed and the simulation results verify the strategy. The second power and energy management strategy is the hierarchical control. In this control strategy, three-layer control structure is presented and defined. The first layer is the primary control for the DC MG in islanding mode, which is to guarantee the DC MG system power balance without communication to increase the system reliability. The second control layer is to implement the seamless switch for DC MG system from islanding mode to SST-enabled mode. The third control layer is the tertiary control for the system energy management and the communication is also involved. The tertiary layer not only controls the whole DC MG output power, but also manages battery module charge and discharge statuses based on its SOC. The simulation and experimental results verify the methods. Some practical issues for the SST interfaced DC MG are also investigated. Power unbalance issue of SST is analyzed and a distributed control strategy is presented to solve this problem. Simulation and experimental results verify it. Furthermore, the control strategy for SST interfaced DC MG blackout is presented and the simulation results are shown to valid it. Also a plug and play SST interfaced DC MG is constructed and demonstrated. Several battery and PV modules construct a typical DC MG and a DC source is adopted to simulate the SST. The system is in distributed control and can operate in islanding mode and SST-enabled mode.
The experimental results verify that individual module can plug into and unplug from the DC MG randomly without affecting the system stability. Furthermore, the communication ports are embedded into the system and a universal communication protocol is proposed to implement the plug and play function. Specified ID is defined for individual PV and battery for system recognition. A database is built to store the whole system date for visual display, monitor and history query.
Power and Energy Management Strategy for Solid State Transformer Interfaced DC Microgrid

by
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DEDICATION

To my parents

Moqing Yu and Deyong Jian
BIOGRAPHY

The author, Xunwei Yu, was born in Fengxin, Jiangxi Province, China. He received his B.S. and M.S. degree from Anhui University of Science & Technology and Huazhong University of Science & Technology, China in 2002 and 2007, respectively, both in electrical engineering. Since fall of 2009, he started to pursue a Ph.D. degree at National Science Foundation funded Engineering Research Center: FREEDM, Department of Electrical and Computer Engineering, North Carolina State University, Raleigh.
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Chapter 1 Introduction

1.1 Research Background

The global demand for electric energy has increased continuously for the last few decades. On the other way, the shortage of energy and the problems of environment have become serious concerns in the today’s world. Alternative renewable energy sources generation, like PV, Wind, Fuel cell and tidal power, have drawn more and more attentions in last ten years [1]-[5]. Figure 1.1 shows the renewable energy source generation ratio in 2012 and it will take more and more important role in the future. In 2012, 22100 terawatt-hours (Twh) electrical power will come from the renewable energy in global electricity generation, which is 20% of the whole electrical power. Based on Siemens prediction (Figure 1.1), in 2030, the electrical power generated by renewable energy source is about 37100 Twh, which is 28% of the global electrical generation [6].

Thus, how to utilize the renewable energy sources and deliver their power into the traditional AC utility reliably based on their different features, is the hottest research topic in recent years. The microgrid (MG) is the most promising method to integrate these various renewable energy sources and interface them to the utility [7]-[10]. The basic idea of MG is using the power electronics technology to construct a sub-grid, which consists of distributed renewable energy resources (DRERs), distributed energy storage device (DESD) and the local load. Then the power generated by DRESs and DESD will supply the local load, or be delivered to the utility. Thus, the biggest feature of MG is that it can not only interface to the utility but operate by itself. Based on the Figure 1.2, the MG distributed generation market
will keep increasing and the market might be 12.7 billion at 2018, which depicts a promising future for the MG.

Figure 1.1 World Electricity Generation. (cited from Sustainable Energy Review Oct 2012)

Figure 1.2 World MG Generation Market. (Sourced from Pike Research)
Figure 1.3 Typical AC MG Diagram.

Figure 1.4 Typical DC MG Diagram.
As mentioned before, MG can be considered a sub-grid which includes multiple DRERs, DRSDs, and the load. Then, the conventional MG interfaces to the distribution system or utility by traditional transformer. All DRERs, DESDs and load share a common bus by converters and communication ports are embedded into the system to transit the MG information or instructions between the control center and the local controllers for converters. Basically, MG can be divided into two major groups based on its structure, which the first one is the AC MG (shown in Figure 1.3) [11]-[15] and the other one is DC MG (shown in Figure 1.4) [16]-[20]. The AC MG is the system which all devices (DRERs, DESD, load) share a common AC bus, while the DC MG is the system which all devices connects a common DC bus. Comparing to AC MG, DC MG has its own advantages such as:

1) higher efficiency because of elimination of multiple power conversion stages and reduction of filter requirements;
2) better to power future homes’ DC loads, like electric vehicle (EV), light-emitting diode (LED), projector, and etc, [21]- [24];
3) easier to integrate the renewable resources and energy storages, especially for some DC sources like fuel cell [25]-[28], PV [29]-[31], battery [32], and etc.;
4) no harmonic and reactive power factors.

1.2 Survey of Conventional DC MG

1.2.1 Overview of DC MG Structure

Usually, DC MG’s structure can be categorized into two major types based on the converter’s topology [33], which the first one is multiple-input converters (MIC) and the other one is single-input converters (SIC). As shown in Figure 1.5, MIC is the structure
which several DRERs and DESDs share a common converter which interfaces to DC bus, while SIC is the structure which each DRER or DESD interfaces to the DC bus by the individual converter.

Comparing to the SIC, MIC has its own advantages, such as higher efficiency and less devices. Three-port DC/DC converter is a typical application for MIC [34]-[40]. But its disadvantages are obvious, like complicated circuit and control algorithm design. The SIC which are applied in DC MG are some typical DC/DC topologies, such as buck-boost, flyback, dual active bridge (DAB), dual half bridge (DHB), and so on. These topologies are easy to implement. Furthermore, the corresponding control algorithm design is easy to accomplish since it only deals with one DESD or DRER.

(a) SIC structure  
(b) MIC structure

Figure 1.5 SIC and MIC Structure of DC MG.
1.2.2 DC MG Bus Voltage Standards

Similar to AC system, the DC MG system bus voltage can be categorized into several levels for different applications. The first major application is the DC system for data center. A 380 V DC testbed system for data center is developed by the Lawrence Berkeley National Laboratory (LBNL). Based on [41], 380 V DC system achieves an improvement of 4-6% efficiency points over well designed efficient 408-208 V AC systems available today. The second major application is the home DC appliances. In home application, the DC voltages are divided into three levels, which are 12 or 24 V, 48 V and 120 V DC. 12 or 24 V is used for low-power devices in interior spaces, such as lighting, sensors, routers and modems [42]. 48 V is the standard voltage for the telecommunications. 120 V is defined as the upper boundary of extra-low voltage (ELV), which is low risk under dry conditions [43].

1.2.3 Overview of DC MG Power and Energy Management Strategy

Comparing to the conventional utility, the MG is more complicated because of the integration of multiple DRERs and DESDs. The system information is usually changing because not only the load varies frequently, but the power generated by DRERs is not always constant. The reason is that the DRERs output power is based on their inputs. For example, the power generated by PV panels and wind turbine is depends on the sun irradiation and wind speed, respectively. Furthermore, DRERs and DESDs dynamic responds are different from each other, which is another factor needs to be considered in the system design. Also, when DC MG operates by itself, meaning it disconnects from the grid, DRERs and DRSD output power is limited by their features and power ratings. Thus the major issue for DC MG
power management is how to maintain the system’s power balance in the presence of stochastic DRERs, DESDs and loads, especially the system is in islanding mode. When the DC MG connects to the grid, usually, the grid is considered as infinite energy source. Thus, the system power balance can be always guaranteed. Then the system energy management becomes the major concern, such as how to manage the individual DRER and DESD output power based on their different features. Basically, like AC MG, there are three basic categories for DC MG power and energy management strategy: Centralized control, distributed control and hybrid control or hierarchical control.

1) Centralized control

As shown in Figure 1.6, besides the traditional power line connection, a communication line is attached between central controller and each individual local controller for DRERs, DESDs and load. The direction of the communication line is bidirectional. It conveys every device’s information in the system to the central controller and transits the instructions from the central controller to the local controller. The objective of centralized controller is to monitor the whole system operation and make the power and energy management instructions for each device in the system based on the system information, which is coming from the local controllers’ measurements [44]-[46]. For the local controllers, the operation modes or the control algorithms are pre-embedded. When they receive the instructions from central controller, the corresponding modes or the control algorithms start to operate. Since all local controllers operations are based on the central controller’s instructions, a high-bandwidth communications link is required and necessary to guarantee the whole system real-time operation.
The main advantage for this control strategy is that the system energy management can be always maintained if the communication is real time. The reason is that the instructions for local controllers are made based on the whole system information in the centralized controller. On the other side, the drawbacks of centralized control are obvious. The major one is that the reliability of the system is degraded because all system operations are all based
on the communication ports. Any malfunctions occur in the communication link might cause the whole system fail or unstable.

2) Distributed control

The basic idea of distributed control is that each local controller’s operation is only based on the local information, as shown in Figure 1.7. Different from the centralized control, the central controller is removed in the distributed control. Since all devices in the system share a common DC bus, the DC bus voltage must be some valuable information that can be used for the local controllers. Actually, in DC system, the DC bus voltage represents the whole system power information. In other word, if the system power balance achieves, this voltage will be a constant; if not, the bus voltage will vary. Thus, the bus voltage is commonly used in distributed control and DC bus voltage signal (DBS) is the most popular method [47] -[49] for DC MG distributed control.

Obviously, comparing to the centralized control, the system’s reliability gets upgrade. The operation mode or control algorithm for the local controller is based on the source characteristic and DC bus voltage instead of the instructions from communication link. When the system information changes, the local controller will automatically make faster response than centralized control, because the control algorithm bandwidth is usually faster than the communication. However, there are some shortcomings for distributed control. The first is the system energy management might be a problem because the operation for local controller only has its individual local information but missing the system information. For instance, the battery can only operate in one status in distributed control algorithm based on some fix bus voltage. Then, if it’s running in discharging mode for a long period, the battery might be
damaged, which might lead system to unstable, especially in islanding mode. If the energy management is involved, the battery can be charged with the sacrifice of some bus voltage drop. Unfortunately, it usually can’t be achieved without the system information involved into the local controller. The third problem is the system maintenance. Since the whole system monitor function is missing, the whole system has to be shut down even only one device is damaged.

Figure 1.7 DC MG Distributed Control Diagram.
3) Hierarchical control

Hierarchical control [50] [51] is a hybrid control strategy which combines the advantages for centralized control and distributed control. Its control diagram is shown in Figure 1.8. Although its structure is same as the centralized control, its operation principle is different. Same as the centralized control, the communication ports are bidirectional to deliver the system information and instructions between central controller and local controllers. Different from the centralized control, the control algorithm for power balance is embedded in individual local controller and the instructions are just for the power management. Thus the local controller still can operate by itself based on the local information liked the distributed control, when the communication ports fail or delay. Therefore, the system power balanced can be achieved by local controller and the system reliability gets increasing. Furthermore, the system optimization or energy management is guaranteed because the local controllers can also operate based on the instructions issued from the centralized controller based on the system information. Then the requirements of bandwidth for the communication link decreases because the requirement of time scale for energy management is slow.

Nowadays, more and more communication protocols are added into the MG system, such as Zigbee [52], Power Line Communication (PLC) [53], Controller Area Network (CAN) [54], and WIFI [55]. Which one is selected depends on the system design and requirement.

The major weakness of hierarchical control is hard to accomplish. Since the MG system architecture and the distributed control algorithms are complicated, adding communication
Figure 1.8 DC MG Hierarchical Control Diagram.

ports is not easy. Furthermore, the communication architecture is also need to be investigated, which has to guarantee the system stability to avoid the MG malfunction because of the communication delay or malfunction. In addition, the cooperation for the
distributed control and the instructions coming from the centralized control is another factor need to be considered.

1.3 DC MG in FREEDM Systems

The FREEDM Systems Center is a US National Science Foundation (NSF) generation-III Engineering Research Center (ERC) established in 2008 with its headquarters at North Carolina State University, US. The center’s objective is to develop the fundamental and enabling technologies for a future power distribution system called the FREEDM system [56].

Targeted as a future grid architecture suitable for large scale plug-and-play integration of distributed resources, the proposed FREEDM system is depicted in Figure 1.9 and its feasibility is based on current and future progress of power electronics technology and information technology. The medium voltage AC grid (12.45 kV) is powered by a substation SST (SST1) from the 69 kV transmission grid. Several distribution-level SSTs are connected to the medium voltage system and transform the 12.45 kV to the low voltage AC (120 V) and DC (380 V), both of which can then enable the residential AC MG and DC MG. A solid state fault isolation device (FID) is adopted to isolate the malfunction areas when the system is in abnormal condition, such as single phase or three phase faults. Bidirectional communication in the SSTs and FIDs deliver the system information to the control center and take the instructions from the control center. A completely decentralized software and communication architecture is also be researched by the center. In summary, the key features of this innovative FREEDM system are:

1. Ability to form plug-and-play AC and DC MG that integrate DRER and DESD.
2. Intelligent power management (IPM) through the use of high bandwidth SST that directly controls medium voltage and low voltage interfaces.

3. Intelligent fault management (IFM) with ultra-fast and intelligent fault isolation capability of the FID.

4. Intelligent energy management (IEM) via coordinated optimization and dispatch of distributed resources.

In FREEDM systems, besides the SST control, SST interfaced DC MG operation and control are the important factors to guarantee this huge system operation well. Basically, the system investigation of SST interfaced DC MG can be divided into four major areas (as shown in Figure 1.10). The first area is the protection section, which is for the DC system fault protection [57] [58]; the following section is the DC system stability analysis; the third
one is the intelligent energy management, including the economic optimization [59], forecasting, and so on; the last section is the system power management. This dissertation is focusing on the last two areas for a single SST interfaced DC MG system.

The three popular control strategies for DC MG, which are discussed in section 1.2.3, can all be applied to the system. One major challenge for such a system is to operate each component in a distributed fashion while maintaining system stability under all operation conditions. This is the objective of the IPM and IFM control. The instructions from the control center are too slow and can only be used for system monitoring, optimization and economic operation (the IEM functions). Therefore, IPM and IEM are the major concerns will be discussed and solved in the following chapters.

![Figure 1.10 FREEDM DC MG System Structure.](image-url)
1.4 Dissertation Outline

The dissertation has six chapters and is organized as follows:

Chapter I introduces the DC MG background and the research objectives. The DC MG prospect, structure and control algorithms are reviewed. Furthermore, a DC MG system structure in FREEDM center which needs to interface to SST is proposed. The research objective is presented.

Chapter II introduces the DHB topology, which is applied to the DC MG system for DESD and DRER, is presented. Several corresponding factors for DHB are analyzed, including 1) the large signal average model of DHB for system simulation is achieved; 2) ZVS procedure and boundary of DHB for experiment are analyzed; 3) the control algorithm for DHB is proposed; 4) the switching model for single DHB is implemented in Matlab/Simulink; 5) the experimental results verify the ZVS procedure and the control algorithm for DHB.

Chapter III proposes a novel distributed energy management strategy without communication for SST interfaced DC MG, which includes DRERs (fuel cell, PV) and DESD (battery). Furthermore, SST is firstly adopted to enable the DC MG to interface AC system and the distribution system. The proposed distributed control algorithms for SST, fuel cell, PV and battery are also presented based on their different features. In this energy management strategy, the system can seamlessly switch between charging mode and discharging mode. Also, the dynamic power sharing between SST and DC MG is analyzed and achieved. In addition, since SOC of battery is considered into the energy management strategy, the battery can intelligently and automatically switch its control algorithm based on its SOC and the system information without the communication ports. To verify the proposed
energy management strategy, the corresponding simulation model is constructed and the simulation results verify it.

In chapter IV, a hierarchical power and energy management strategy for SST interfaced DC MG is proposed, which includes primary control, secondary control and tertiary control. The primary control is based on the distributed control level to guarantee the system power balance without communication. Furthermore, some extreme cases, like load shedding and PV shedding, are considered and verified in primary control. The secondary control is adopted to eliminate the voltage difference when DC MG switches from islanding mode to SST-enabled mode and then seamless switch is achieved. Furthermore, the DC MG power flow control and battery’s SOC management are involved into the tertiary control. If the battery SOC in the predetermined range, tertiary control is to control DC MG output power. Otherwise, the tertiary control objective is to manage battery operate in charge or discharge status instead of controlling the DC MG power flow. Two tertiary control methods are presented and investigated. One is to change SST low DC output voltage and the other one is to manage battery droop curve. The advantages and disadvantages for these two methods are analyzed. The simulation and experimental results verify it.

Chapter V analyzes some practical issues for the SST interfaced DC MG. The unbalanced power issue of SST is investigated and a distributed control method is presented. Simulation and experimental results are shown to verify it. Then the control strategy for SST interfaced DC MG blackout is proposed and the simulation results valid it. Lastly, a DC MG with plug and play function is proposed. A distributed control strategy is applied to the system, which includes multiple DRERs and DESDs. The requirements for plug and play function are
proposed and a corresponding universal communication protocol is proposed. Furthermore, the wireless communication is added into the system to implement the system monitoring and plug and play function implementation. A database built in MYSQL is adopted to save the system historic data for query.

Chapter VI is the conclusion and future work.
Chapter 2 DC/DC Converter Modeling for DC MG

2.1 DC/DC Converter Selection Applied in DC MG

One mention is applied firstly that only DC/DC converters are considered in this chapter since the DRERs and DESDs in the proposed DC MG are all DC sources. There are many DC/DC converters which can be applied into the DC MG along with the power electronics technology increasing in this decade. As mentioned in Chapter I, there are two major types for MG structure, which one is SIC and the other one is the MIC. Here the SIC is selected because of its advantages mentioned in chapter I. Usually, there are several basic requirements for DC/DC converters in DC MG:

1) The converter should can be applied into both DESDs and DRERs;
2) The converter should be easy paralleled or serried since the voltage levels for input and output of DC MG are different;
3) The efficiency of the converter should be high to avoid much energy loss;
4) When the converter plugs and unplugs from system, the system stability should be guaranteed since the plug and play function is one of the import characteristic of system;
5) The control of the converter should be easy to design to alleviate the system design burden because the MG system usually consists many converters;
6) The economic factors of converters should be considered to decrease the cost;

Based on these above requirements, DHB is adopted as the DC/DC converter which applies into the DC MG. The topology of DHB is shown in Figure 2.1. DHB, which was proposed by Dr H. Li and Dr F. Peng [60],[61], is getting more and more applications in renewable
energy area and MG system because of its simplicity in structures and control algorithm implementation [62]-[65]. This topology can implement the bidirectional power flow which is necessary for the DESDs in MG. Since the DHB large signal model can equivalent to a current source, this is easy to be paralleled. Furthermore, zero voltage switch (ZVS) is easy to achieve to ensure the converter efficiency with appropriately circuit parameters design. The basic idea for DHB control is phase shift control (PSC). Comparing to the dual active bridge (DAB) topology [66]-[68], only four power electronics devices are needed. In the latter sections of this chapter, the modeling of DHB, the design for the control algorithm, the selection for the main circuit parameters and the efficiency evaluation are carried out.

![Figure 2.1 Topology of DHB.](image)

2.2 DHB Large Signal Model

Since DC MG system consists many DC/DC converters, the simulation for the system’s power and energy management is on the large signal model. Furthermore, the DC/DC
converters which are adopted for DC MG are DHB. Thus, the large signal model for DHB is critical. As shown in Figure 2.1, the AC terminals of DHB are connected by leaking inductor and high frequency transformer. Figure 2.2 shows the primary-referred equivalent circuit and its idea operation waveform in one switching cycle is depicted in Figure 2.3 [62].

Figure 2.2 Primary-referred Equivalent Circuit of DHB.

Figure 2.3 Ideal Operation Waveform of DHB in One Switching Cycle.
Based on the Figure 2.2, equation (2.1) can be concluded

\[ L \frac{di_L(t)}{dt} = v_a - v_b \]  \hspace{1cm} (2.1)

Where \( L = L_r + L_m \), \( L_r \) and \( L_m \) are the transformer leaking inductance and excitation inductance, respectively. Based on the Figure 2.3, the equations (2.2) and (2.3) can be deduced.

\[
\begin{align*}
    v_a &= \begin{cases} 
    v_1 & 0 \leq t < \varphi \\
    v_1 & \varphi \leq t < \pi \\
    -v_2 & \pi \leq t < \pi + \varphi \\
    -v_2 & \pi + \varphi \leq t < 2\pi 
    \end{cases} \\
    v_b &= \begin{cases} 
    -v_4 & 0 \leq t < \varphi \\
    v_3 & \varphi \leq t < \pi \\
    v_3 & \pi \leq t < \pi + \varphi \\
    -v_4 & \pi + \varphi \leq t < 2\pi 
    \end{cases}
\]  \hspace{1cm} (2.2)

\( \varphi \) is the phase shift angle between high frequency transformer primary side and second side drive signal. Then

\[
\begin{align*}
    L \frac{di_L(t)}{dt} &= \begin{cases} 
    v_1 + v_4 & 0 \leq t < \varphi \\
    v_1 - v_3 & \varphi \leq t < \pi \\
    -v_3 - v_2 & \pi \leq t < \pi + \varphi \\
    v_4 - v_2 & \pi + \varphi \leq t < 2\pi 
    \end{cases}
\]  \hspace{1cm} (2.4)

Transfer equation (2.4) from time domain to radian domain, equation (2.5) can be deduced
\[i_L(\alpha) = \begin{cases} 
\frac{(v_1 + v_4)\alpha}{\omega L} + i_L(0) & 0 \leq \alpha < \varphi \\
\frac{(v_1 - v_3)(\alpha - \varphi)}{\omega L} + i_L(\varphi) & \varphi \leq \alpha < \pi \\
\frac{(-v_3 - v_4)(\alpha - \pi)}{\omega L} + i_L(\pi) & \pi \leq \alpha < \pi + \varphi \\
\frac{(v_4 - v_3)(\alpha - \pi - \varphi)}{\omega L} + i_L(\pi + \varphi) & \pi + \varphi \leq \alpha < 2\pi
\end{cases} \] (2.5)

Based on the Figure 2.3, equation (2.6) is concluded.

\[
\begin{align*}
i_L(0) &= -i_L(\pi) \\
i_L(\varphi) &= -i_L(\pi + \varphi)
\end{align*} \] (2.6)

Equation (2.7) can be achieved from equations (2.5) and (2.6):

\[
\begin{align*}
i_L(0) &= \frac{-(v_1 - v_3)(\pi - \varphi) - (v_1 + v_4)\varphi}{2\omega L} \\
i_L(\varphi) &= \frac{-(v_1 - v_3)(\pi - \varphi) + (v_1 + v_4)\varphi}{2\omega L} \\
i_L(\pi) &= \frac{(v_1 - v_3)(\pi - \varphi) + (v_1 + v_4)\varphi}{2\omega L} \\
i_L(\pi + \varphi) &= \frac{(v_1 - v_3)(\pi - \varphi) - (v_1 + v_4)\varphi}{2\omega L}
\end{align*} \] (2.7)

When S3 is on, S4 is off, secondary side of high frequency transformer can be shown as Figure 2.4.
Figure 2.4 Secondary Side Equivalent Circuit when S3 is On and S4 is Off.

Then

$$i_L(\alpha) = c_3 \frac{dv_3}{dt} + c_{out} \frac{dv_{out}}{dt}$$  \hspace{1cm} (2.8)

$$c_4 \frac{dv_4}{dt} = -c_{out} \frac{dv_{out}}{dt}$$  \hspace{1cm} (2.9)

While S3 is off, S4 is on, secondary side can be shown as Figure 2.5.

Figure 2.5 Secondary Side Equivalent Circuit when S3 is Off and S4 is On.
then
\[ c_3 \frac{dv_3}{dt} = -c_{out} \frac{dv_{out}}{dt} \] (2.10)
\[ i_L(\alpha) = -(c_4 \frac{dv_4}{dt} + c_{out} \frac{dv_{out}}{dt}) \] (2.11)

Define \( S_3 = 1 \) when \( S_3 \) is on, and \( S_3 = 0 \) when \( S_3 \) is off in one cycle, the following equation can be defined based on the equations (2.8) to (2.11).

\[
\begin{cases}
    c_3 \frac{dv_3}{dt} = [i_L(\alpha) - c_{out} \frac{dv_{out}}{dt}]S_3 - c_{out} \frac{dv_{out}}{dt}(1 - S_3) \\
    c_4 \frac{dv_4}{dt} = [-i_L(\alpha) - c_{out} \frac{dv_{out}}{dt}]S_3 - c_{out} \frac{dv_{out}}{dt}(1 - S_3)
\end{cases}
\] (2.12)

Usually, the capacitor selection is as \( c_3 = c_4 = c_m \), and then \( v_{out} = v_3 + v_4 \), equation (2.13) can be concluded based on (2.12)

\[ \left( \frac{c_m}{2} + c_{out} \right) \frac{dv_{out}}{dt} = \frac{i_L(\alpha)S_3 - i_L(\alpha)(1 - S_3)}{4} \] (2.13)

Based on the waveforms for DHB,

\[
\begin{cases}
    i_L(\alpha)S_3 = \frac{[i_L(\phi) + i_L(\pi)](\pi - \phi) + [i_L(\phi + \pi) + i_L(\pi)]\phi}{2\pi} \\
    i_L(\alpha)(1 - S_3) = -i_L(\alpha)S_3
\end{cases}
\] (2.14)

Substituting (2.7) into (2.14), (2.15) can be yielded

\[
\begin{cases}
    i_L(\alpha)S_3 = \frac{\pi(\pi - \phi)(2v_1 + v_4 - v_3)}{2\pi\omega L} \\
    i_L(\alpha)(1 - S_3) = -\frac{\pi(\pi - \phi)(2v_1 + v_4 - v_3)}{2\pi\omega L}
\end{cases}
\] (2.15)
Usually, the duty cycle for DHB is 0.5, therefore, (2.16) can be concluded

\[
\begin{align*}
  v_1 &= v_2 = \frac{1}{2} v_{\text{in}} \\
  v_3 &= v_4 = \frac{1}{2} v_{\text{out}}
\end{align*}
\]  
(2.16)

Combine (2.13) (2.15) and (2.16), equation (2.17) can be produced

\[
c_{\text{eq,out}} \frac{dv_{\text{out}}}{dt} = \frac{\phi(\pi - \varphi)}{4\pi\omega L} v_{\text{in}} = \frac{\phi(\pi - \varphi)}{8\pi^2 fL} v_{\text{in}}
\]  
(2.17)

Where \( f \) is the switching frequency.

Considering the voltage turn ratio, (2.18) can be concluded from (2.17).

\[
c_{\text{eq,out}} \frac{dv_{\text{out}}}{dt} = \frac{N\phi(\pi - \varphi)}{8\pi^2 fL} v_{\text{in}}
\]  
(2.18)

Where \( c_{\text{eq,out}} = \frac{c_{m}}{2} + c_{\text{out}} \) and \( N \) is the transformer turn ratio.

Because of the symmetrical structures for primary and second side, the input voltage can be given as (2.19).

\[
c_{\text{eq,in}} \frac{dv_{\text{in}}}{dt} = \frac{N\phi(\pi - \varphi)}{8\pi^2 fL} v_{\text{out}}
\]  
(2.19)

Where \( c_{\text{eq,in}} = \frac{c_{n}}{2} + c_{\text{out}} \) and \( c_{n} = c_{1} = c_{2} \)

Thus, the large signal average model for single DHB converter can be shown as the follows figure.
Where 

$$ g = \frac{N \varphi (\pi - \varphi)}{8 \pi^2 fL} $$

As stated in the [62], the output power of DHB can be depicted as (2.20)

$$ p = \frac{nv_{in} v_{out} \varphi (\pi - \varphi)}{8 \pi^2 fL} $$ (2.20)

Figure 2.7 shows the output power versus different phase shift angle. The maximum power is delivered when phased shift angle equals to $\pi/2$. When the phase shift angle is greater than zero, the power will be delivered from the primary side to the secondary side. While the value of phase shift angle is negative, the power direction will be reversed. Thus, DHB can be considered as an inductor interfaced by two controllable square wave voltage sources, as shown in Figure 2.8.
Figure 2.7 Relationship between Power and Shift Angle.

Figure 2.8 Equivalent Model for DHB.
2.3 ZVS Operation Boundary

To guarantee the system efficiency, it should make the converter to operate in ZVS as much as possible [69]-[71]. The ZVS operation principle is analyzed as following. According to the topology symmetric characteristic, only soft switching process of S2 is shown and the same process can be applied to other switches.

The turn-on process of S2 can be divided into two statuses. The first one is that S1 is turned off from conducting and Cs2 is conducting. In this period, Cs1, Lr, and Cs2 begin to resonate. Cs1 starts to charge while Cs2 begins to discharge. The current direction is shown in Figure 2.9.

![Figure 2.9 Soft Switching Process a of S2.](image)
The second one is that $V_{ds\_ds2}$ equals to zero and D2 begins to conduct, clamping $V_{ds\_ds2}$ to zero. Thus, when S2 is turned on in this period, ZVS for S2 can be guaranteed. The current direction is shown in Figure 2.10.

![Figure 2.10 Soft Switching Process b of S2.](image)

Therefore, to achieve ZVS, a certain current must charge and discharge the snubber capacitors. Based on the analysis of S2’s turn-on process, ZVS the boundary for primary side can be drawn as equation (2.21).

$$i_L(0) \leq 0$$  \hspace{1cm} (2.21)

Combining equations (2.7) and (2.21), the primary side ZVS boundary can be defined as follows:

$$n \leq \frac{\pi}{\pi - 2\phi}$$  \hspace{1cm} (2.22)
In the same theory, the secondary side ZVS boundary can be defined as equation (2.23) because of the topology symmetry.

\[ n \geq 1 - \frac{2\varphi}{\pi} \]  
(2.23)

Where \( n \) is the transformer turn ratio.

2.4 Small Signal Modeling for DHB

As shown in Figure 2.6, the output average model of DHB can be modeled as a controllable current source, which the current value is \( \frac{N\varphi(\pi - \varphi)}{8\pi^2 fL} V_{in} \). Thus, the equivalent output circuit of DHB can be depicted as Figure 2.11 (a) [72],[73]. For a given operation condition of \( V_{in} \) and duty cycle, the transfer function from phase shift angle to output voltage can be shown as equation (2.24).

\[ \frac{\tilde{v}_{out}}{\dot{\varphi}} = \frac{N(\pi - 2\varphi)}{8\pi^2 fL} V_{in} Z_{out} \]  
(2.24)

where \( Z_{out} = \frac{1}{SC_{out} // R_o} \), the corresponding small signal of DHB can be depicted as Figure 2.11 (b). Based on equation (2.24), the small signal of DHB from phase shift to output voltage is the first order system. The Bode plot for simplified linear model is shown in Figure 2.12.
\[ i_s = \frac{N\varphi(\pi - \varphi)}{8\pi^2 fL} V_{in} \]

(a) average output model

\[ i_s = \frac{N(\pi - 2\varphi)}{8\pi^2 fL} V_{in} \bar{\phi} \]

(b) small signal output model

Figure 2.11 Average Output Model and Small Signal Output Model.

Figure 2.12 Bode Plot for Load of 100ohm.
2.5 Control Algorithm for DHB

For the DHB converter, the phase shift control is adopted while the control objective depends on the energy source or energy storage which is on the low voltage side. Here, battery is selected as an example while the other DESDs and DRERs’ control algorithms are depicted in later chapters. The battery is usually the energy buffer for DC MG, thus its control objective is to regulate its output voltage. Here, a constant voltage value (380 V) is adopted and its control diagram is shown in Figure 2.13. First the outer loop is the voltage control loop which the input is the difference between the output terminal DC voltage $V_{dc}$ and the reference voltage. Then the voltage error gets through the PI controller. In the DC system, the output power is linear to the source input current when the bus voltage is regulated as a constant if the loss is considerable small and ignored. Thus the inner loop is the current control loop which the input is the difference between the battery output current and the voltage control loop output ($I_{ref}$). The phase shift angle ($\varphi$) is achieved by the PI controller.

![Figure 2.13 DHB Control Diagram.](image)

2.6 Simulation and Experimental Results

To verify the DHB topology and the control algorithm discussed above, a 500 W DHB switching model for battery module is built in Matlab/Simulink and the correspondingly lab
testbed is constructed (Figure 2.14). The simulation and testbed parameters are listed in Table 2-1. The stable status simulation results for DHB are depicted in Figure 2.15 and the experimental waveforms for hardware testbed are shown in Figure 2.16.

Table 2-1 Simulation and Testbed Parameters.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Battery nominal voltage</td>
<td>48 V</td>
</tr>
<tr>
<td>Battery rated capacity</td>
<td>10 Ah</td>
</tr>
<tr>
<td>Vref</td>
<td>380 V</td>
</tr>
<tr>
<td>f (switching frequency)</td>
<td>50 kHz</td>
</tr>
<tr>
<td>Lr</td>
<td>3 uH</td>
</tr>
<tr>
<td>C</td>
<td>100 uF</td>
</tr>
<tr>
<td>R</td>
<td>400 ohm</td>
</tr>
<tr>
<td>C1, C2</td>
<td>10 uF</td>
</tr>
<tr>
<td>C3, C4</td>
<td>6.7 uF</td>
</tr>
<tr>
<td>Transformer turn ratio</td>
<td>1:7.91</td>
</tr>
</tbody>
</table>
Figure 2.14 DHB Testbed.

Figure 2.15 DHB Simulation Result.

(a) DHB output current, voltage & input current  (b) transformer voltage & inductor current
As shown in Figure 2.15 and 2.16, the simulation results and experimental results verify the DHB operation and control algorithm, which are critical and fundamental for the DC MG operation we will carry out in the later chapters. Furthermore, the experimental results also test the controller dynamic response when the load step changes (from 2 kohm to 650 ohm).
When the load increases, the phase shift gets large which is consistent to equation (2.20). ZVS is also verified (shown in Figure 2.16(d)) which guarantees the converter’s efficiency.

2.7 Summary

In this chapter, the DHB topology, which is applied to the DC/DC converter of DC MG system, is presented. Several corresponding factors for DHB are analyzed: 1) The large signal average model for DHB is achieved; 2) ZVS procedure and boundary for DHB are analyzed; 3) The control algorithm for battery based on DHB is proposed; 4) The switching model for single DHB battery is implemented in Matlab/Simulink; 5) The experimental results very the ZVS procedure and the control algorithm for battery based on DHB.
Chapter 3 Distributed Energy Management Strategy for SST Interfaced DC MG

3.1 Introduction and Motivation

The topology of the SST in FREEDM is illustrated in Figure 3.1[74]-[75]. The front-end stage adopted cascaded multilevel rectifier with three H-bridges. Three dual active bridge (DAB) converters are connected to each high DC link with secondary side parallel as the DC/DC stage to step down high DC voltage to the low value. In the last stage, a single phase inverter is to transform the low DC voltage to 120 V AC output.

As introduced in chapter I, SST supplies a good solution for DC MG to interface with the distribution system directly. It provides both the dc and ac interface for the residential side.
In addition, SST is also good to increase the system efficiency and interface DC and AC MG to the traditional distribution level utility. However, DC MG also faces some challenges: 1) how to supply sustainable and reliable power to the load or the utility; 2) how to intelligently control each device in the system; 3) how to maximize the utilization of DESDs and DRERs based on their different characteristics. Thus, in order to fulfill these challenges, a novel distributed energy management strategy based on SST enabled DC MG is presented. The main contribution of this chapter can be summarized as follows:

1) a SST-enabled DC MG system is envisioned;
2) a novel distributed energy management strategy is proposed for SST enabled DC MG;
3) several operation modes of battery are defined based on its SOC information and the SOC is involved into the system energy management strategy;
4) dynamic power sharing between SST and DESD is investigated.

The rest of the chapter is organized as follows: In Section 3.2, the DC MG system enabled by a single phase, three-stage SST is presented to illustrate the key feature of the proposed system, and the topology for DESD and DRER is introduced. The system energy management is proposed in Section 3.3. In Section 3.4, the corresponding control algorithms for individual DESD and DRER are introduced. Typical case studies to verify the proposed energy management are illustrated in Section 3.5. The conclusion is given in Section 3.6.

3.2 Description of DC MG Enabled by SST

The envisioned DC MG architecture enabled by SST is shown in Figure 3.2. Only DC MG system energy management is considered here. For the AC MG enabled by the SST ac output terminal, a typical RL load is adopted to represent as the AC MG. Since the islanding mode
of system is the same as the traditional DC MG, this chapter only focuses on the SST-enabled mode for better demonstration of the proposal.

PV, fuel cell and battery are selected as typical DRERs and DESD respectively to construct a DC MG, and the DC bus is connected to SST low DC output terminal. SST can be considered an interface between low voltage AC and DC systems to the distribution system. The power flow directions for DESD and DRERs are also depicted. PV and fuel cell always supply power to the system, while the battery is considered an energy buffer to balance the system power supply and demand when battery’s SOC is within the operation range; SST’s can also operate bi-directionally. When the DC MG supplies more power than the loads need,
the extra power will feed back to the utility by SST, and vice versa. More details about the power flow will be discussed in Section 3.3.

3.2.1 SST Topology

SST is one of the newest family members of flexible ac transmission (FACTs) devices [74]–[76]. The key idea for SST is to apply power electronics control technology and the state of art power device technology to increase the operating frequency of the transformer and therefore decrease its volume.

Figure 3.3 shows a simplified single phase, three-stage SST unit under the consideration. The device limitation is not considered while higher power and voltage rating SST can be composed by series and paralleled connection of this unit.

![Figure 3.3 Simplified Single Phase, Three Stage SST Topology.](image-url)
3.2.2 Converter for the PV, Fuel cell and Battery

PV, fuel cell and battery modules share a common dc bus, thus the three modules can be modeled as the dc voltage or current sources. The DHB topology is adopted and the modeling and control details of DHB are discussed in chapter II.

3.3 System Energy Management

The MG system information is very complicated and stochastic, for example: the output power of PV will change as the irradiation changes; the load is not always constant; DRERs and DESD have different dynamic responses, and so on. Therefore, to supply reliable and high quality power to the users, the system energy management strategy should consider these factors. Comparing to the AC MG, there is no frequency in the DC MG system, and the bus voltage is the only information can be utilized in distributed control. The bus voltage represents the system power information, meaning when the system has extra power, the bus voltage will rise; when the system needs more power, the bus voltage will drop. Droop control is adopted for both SST and battery (the droop control algorithm will be discussed in Section 3.4). Thus the DC bus voltage, which varies in a certain range, is regulated by the SST DC/DC stage and battery module together. In addition, to avoid DC MG operating at too high or too low voltage, the system will enter the constant bus voltage control mode when the bus voltage value is out of the limit (360V-400V).

Due to the droop control fashion [76]-[77], the power of the battery is only determined by the system operating condition. For example, when the power generated by DRERs is less than the load demand, the battery has to supply some power to the load. In some situation, the AC grid has to supply heavy load in a certain time, e.g. in summer time. Then the grid
voltage and frequency will drop. In the worst case, the grid will collapse. On the other side, the battery can’t supply its maximum power to the load because its output power is defined by its droop curve. Then, to reduce burden for AC grid and maximum the battery capacity, an adaptive droop control is proposed with operation curve shown in Figure 3.4.

![Figure 3.4 SST & Battery Droop Curves.](image)

380V is used as the boundary value between charging and discharging mode for SST and battery. Charging mode for SST means that SST absorbs extra power from DC MG and discharging mode means SST delivers extra power to the DC MG. The droop slope for SST is chosen to be smaller than that of battery because the battery’s power rating is smaller than SST. The traditional droop control can make battery achieve seamless switch between charging and discharging mode automatically. However, as discussed before, the battery
rating cannot get fully utilized because the power of battery depends on the system operating condition. To address this issue, the battery will switch to constant current control loop when the DC bus voltage reaches a predetermined critical value. For example, when the bus voltage is in charging mode and reaches 390 V, meaning the DRER’s output power is higher than the load, the battery will enter the constant current charging mode (battery trajectory jumps from point A to point B in Figure 3.4), while the SST is still in droop control. The constant current value is the battery maximum charging current. Two consequences might happen: the first one is that the output power of DRER is less than the sum of the load and battery constant charging power, then the power feeding into SST will decrease and the DC bus voltage will begin to drop until the system power reaches a new balance. For the battery curve, it will go down vertically from point B. The second one is that if the generated power of DRER is still higher than the sum of battery charging power and the load, the bus voltage will keep increasing and the battery curve will go up vertically from point B. As soon as the bus voltage reaches 400 V (point C), the SST switches to constant voltage control mode to keep DC bus voltage at 400 V, and then the extra power will feed back into SST. To avoid battery oscillating between two operating modes, battery can switch from current control loop to the droop control only when the DC bus voltage drops to the 380 V (point D).

In discharging mode, when the bus voltage reaches 370 V, it means the AC system and the battery need to supply more power to the load. But the battery’s capacity doesn’t get full utilization because it’s under droop control. To maximize the battery capacity and reduce the AC grid burden, the battery needs to enter the constant current discharging mode to supply the maximum power to the load (battery trajectory jumps from point E to point F). The
constant discharging value is the battery’s maximum discharging current. If the power generated by the battery and DRERs is larger than the load needs, the bus voltage will be recovered and the battery curve will go up vertically from point F; otherwise, the battery curve will go down vertically from point F. When the DC bus voltage reaches 360V (point G), SST will operate at constant voltage control mode to keep bus voltage at 360V, then the extra power will be supplied by SST. Battery can only switch back to droop control when the DC bus increases to 380V (point H) to avoid battery oscillating between two operation modes.

![Battery Operation Mode](image)

**Figure 3.5 Battery Operation Mode.**

In addition, the operation of battery has to be determined based on its SOC, thus the SOC has to be included in the battery control algorithm. Furthermore, due to the battery’s bidirectional power flow nature, three basic modes are defined for the battery: Mode I---battery standby (SOC out of limit), Mode II---battery charging, Mode III---battery
discharging. The battery operation should seamlessly switch among three modes (shown in Figure 3.5). The arrow in Figure 3.5 shows the mode switching direction. For example, when the battery is in the charging mode and its SOC is higher than the upper limit, the battery will enter the standby mode and stop absorbing power no matter which control mode it is operating in (from Mode II to Mode I on light green curve in Figure 3.5). Then, the only option for battery back to work is battery is to supply power to load decreases its SOC (from mode I to Mode III) when the system needs more power. In this situation, to avoid the battery oscillating between discharging and standby modes, the battery should output power to the system and keep in the constant current discharging control only when the bus voltage is lower than 370 V. The purple curve in Figure 3.5 depicts the battery mode switch direction when its SOC reaches the lower limit. Similarly, when battery SOC is less than the lower limit, battery enters standby mode. Only when the bus voltage is higher than 390 V, the battery will receive power from the system and stay in the constant current charging control.

The control objective of DRERs is to optimize the utilization of their output power optimally. To achieve this, PV always operates in maximum power point track (MPPT) mode. The fuel cell is in constant power control mode because of its slow dynamic response. The individual module control algorithm is explained in section 3.3.

3.4 Control Algorithm Design

Based on the proposed energy management strategy, the corresponding control algorithms for each module in system are discussed in this section. It is noted here that the distributed control, which only requires local information, is adopted for each module.
3.4.1 SST Control

As discussed before, the SST provides 360 V-400 V dc bus, as well as 120 V ac bus for ac system. The SST control diagrams are represented from Figure 3.6 to Figure 3.8 and the symbols are explained in Table 3-1.

The single phase d-q decoupled control is adopted for the ac/dc converter to rectify high AC voltage (7.2 kV) to high DC voltage (11.4 kV). The high voltage dc bus is controlled by a dual loop controller. The outer loop for d-axis is the voltage regulator and the inner loop for d-axis is the current control loop. The q-axis is for the reactive power control loop and its reference is set to zero for unity power factor operation (Figure 3.6). Phase shift control is adopted for DAB stage to convert high dc voltage to low dc voltage, and its control loop is shown in Figure 3.7. This phase shift between primary side and secondary side determines the power transfer between the high voltage dc side and the low dc voltage side. Previously, the low dc voltage is regulated as a constant value for SST. In order to realize distributed control, the droop control method is proposed for SST, in which the bus voltage is in the range of 360 V to 400 V, and the low dc voltage reference is concluded by the SST droop equation (3.1).

\[ V_{SST, \text{dc}} = V_{SST, \text{dcmx}} - R_{sst} I_{SST} \quad (3.1) \]

Where \( V_{SST, \text{dc}} \) is the SST low dc side output voltage reference, \( V_{SST, \text{dcmx}} \) is SST low dc side output voltage value without load and it is set as 380 V, \( R_{sst} \) is the droop slope and \( I_{SST} \) is the SST low dc side output current. To guarantee that the output low dc voltage of SST is within the desired range, the saturation limiter is added into the droop curve output, where the up-limiter is 400 V and the low-limiter is 360 V, respectively. In addition, a low-pass filter is
adopted to filter the second order harmonic component in the dc bus voltage. The inverter stage adopts the dual loop controller, in which the outer ac voltage loop and inner inductor current loop are cascaded, as shown in Figure 3.8.

![Figure 3.6 SST Rectifier Control in Single DQ Transform.](image)

![Figure 3.7 SST Low DC Voltage Side Control.](image)
Figure 3.8 SST Inverter Stage Output Control.

Table 3-1 Symbols for SST Control Diagram.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{in}$</td>
<td>AC input current</td>
</tr>
<tr>
<td>$V_{dc}$</td>
<td>d-axis voltage</td>
</tr>
<tr>
<td>$V_{ac}$</td>
<td>AC input voltage</td>
</tr>
<tr>
<td>$I_{sl}$</td>
<td>d-axis current</td>
</tr>
<tr>
<td>$V_{ref}$</td>
<td>q-axis current</td>
</tr>
<tr>
<td>$wC_s$</td>
<td>SST low dc side voltage critical value</td>
</tr>
<tr>
<td>$wL_s$</td>
<td>SST low dc side output current</td>
</tr>
<tr>
<td>$V_{SST-ref}$</td>
<td>SST low dc side output voltage reference</td>
</tr>
<tr>
<td>$V_p$</td>
<td>low ac side positive output voltage</td>
</tr>
<tr>
<td>$V_n$</td>
<td>low ac side negative output voltage</td>
</tr>
<tr>
<td>$I_{ref}$</td>
<td>ac side positive output current reference</td>
</tr>
<tr>
<td>$I_0$</td>
<td>ac side positive output current</td>
</tr>
<tr>
<td>$I_{ref}$</td>
<td>ac side negative output current reference</td>
</tr>
<tr>
<td>$I_n$</td>
<td>ac side negative output current</td>
</tr>
<tr>
<td>$\theta$</td>
<td>Phase shift</td>
</tr>
</tbody>
</table>

3.4.2 Battery Control

To implement the battery operation curve discussed in Figure 3.4 and the transition mode in Figure 3.5, the battery control algorithm has to be automatically switched between the
droop control and current control loop based on the bus voltage and SOC. The control algorithm is shown in Figure 3.9, battery control algorithm judgment flow chart is shown in Figure 3.10, and the symbols are explained by Table 3-2.

<table>
<thead>
<tr>
<th>$V_{b_out}$</th>
<th>battery converter dc bus voltage</th>
<th>$V_{b_out}$</th>
<th>battery converter dc bus critical voltage value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_b$</td>
<td>battery output current</td>
<td>$I_b_di_limit$</td>
<td>battery constant current discharge limiter</td>
</tr>
<tr>
<td>$I_b_cha_limit$</td>
<td>battery constant current charge limiter</td>
<td>$I_b_ref$</td>
<td>battery current reference</td>
</tr>
<tr>
<td>$I_{pv}$</td>
<td>PV panel output current</td>
<td>$V_{pv}$</td>
<td>PV panel output voltage</td>
</tr>
<tr>
<td>$V_{ref}$</td>
<td>PV panel output voltage reference</td>
<td>$i_{ref}$</td>
<td>PV panel output current reference</td>
</tr>
<tr>
<td>$V_{ref}$</td>
<td>Fuel cell output power reference</td>
<td>$i_{ref}$</td>
<td>Fuel cell output current reference</td>
</tr>
</tbody>
</table>

Table 3-2 Symbols for Battery, PV and Fuel Cell Control Diagrams.

Figure 3.9 Battery Control Algorithm.
The battery droop control equation is shown in equation (3.2).

\[ V_b = V_{b_{\text{max}}} - R_b I_b \]  \hspace{1cm} (3.2)

Where \( v_b \) is the reference of output voltage for the battery converter, \( v_{b_{\text{max}}} \) is its output voltage at no load and is set as 380 V, \( R_b \) is the droop slope and \( I_b \) is battery output current. To reasonably assign the power sharing between SST and battery, their droop slopes are designed based on their capacities (shown as equation (3.3)).

\[ R_b S_b = R_{\text{SST}} S_{\text{SST}} \]  \hspace{1cm} (3.3)

where \( S_b, S_{\text{SST}} \) are the power ratings for the battery and the SST respectively. Usually, the SST’s power rating is greater than battery’s, and their slope values are shown in Table 3-3.

Here, the SST’s power rating is selected ten times as the battery’s power rating considering the battery economic factor. SST’s power rating is determined by the load requirements, PV’s output power and fuel cell’s output power. The SST droop slope can be calculated if the bus voltage range and the SST output current values at minimum or maximum bus voltage are determined.

The voltage thresholds for the battery switching from droop to current control are determined by several factors, such as system power rating, load, bus voltage range, battery and SST’s droop slopes. Here, the system voltage range is defined from 360 V to 400 V. Then in the discharging area, for example, the median value in discharging range ([360 V, 380 V]), 370 V, is selected as the threshold. So in the normal irradiation, the sum of PV, battery, SST and fuel cell’s output power can supply the normal load, the bus voltage is in [370, 380]. Then when the load peak occurs (the several times of normal load) or PV generating power decreases because of the irradiation, the bus voltage will drop to less than
Figure 3.10 Battery Control Algorithm Judgment Flow Chart.
370 V and the battery will switch to current control loop. In the same way, 390 V is selected as the voltage threshold for droop to constant current control in charging area ([380 V, 400 V]).

As shown in Figure 3.9, there are four different current references for the battery current control loop. Only one reference will be selected based on the battery control algorithm judgment. In battery control algorithm judgment, the SOC of the battery is estimated initially, and then the voltage and some customer designed flags are evaluated. The judgment flow will follow the rules below:

1) If SOC is higher than or equal the upper limit (h_limit), the bus voltage will be evaluated and the critical value is 370 V.
   a. If the bus voltage is higher than 370 V, based on the mode transition criteria (shown in Figure 3.5), the battery will enter the standby mode (mode I) and the current control loop reference is zero. Both the constant current discharge flag (flag_cc) and constant current charge flag (flag_cd) are set to zero, indicating that the battery is in the standby mode.
   b. If the bus voltage is lower than 370 V, it means the battery needs to supply maximal power to the system. According to mode transition criteria (shown in Figure 3.5), the battery will enter the constant current discharging mode and the I_b_dis_limit will become the current control loop reference. In addition, flag_cd is set to 1, indicating that the battery is in the constant current discharging control mode.

2) If SOC is less than the lower limit (l_limit), the bus voltage will be evaluated and the critical value is 390 V.
a. If the bus voltage is lower than 390 V, the battery will enter the standby mode and the reference of current control loop is zero. Meanwhile, both \( \text{flag}_{\text{cc}} \) and \( \text{flag}_{\text{cd}} \) are set to zero.

b. If the bus voltage is higher than 390 V, it means the battery will receive maximal power from the system to charge. Using the same mode transition criteria shown in Figure 3.5, the battery will enter the constant current charging mode and the \( I_{b,\text{cha}\_\text{limit}} \) is the current control loop reference. In addition, \( \text{flag}_{\text{cc}} \) is will set to 1, which means the battery is in the constant current charging mode.

3) If SOC is in the operation range, the bus voltage will be evaluated and 370 V is the critical value.

a. If the voltage is lower than 370 V, based on battery operation curve in Figure 3.4, the battery will be in constant current discharging mode and the \( I_{b,\text{dis}\_\text{limit}} \) is the current control loop reference. Furthermore, \( \text{flag}_{\text{cd}} \) is set to 1, which shows the battery is in the constant current discharging mode.

b. If the bus voltage is higher than 370 V, some further judgments need to be considered. If the bus voltage is higher than 390 V, the battery will enter the constant current charging mode and the \( I_{b,\text{cha}\_\text{limit}} \) will become the current control loop reference. Furthermore, \( \text{flag}_{\text{cc}} \) is set as 1, which means the battery is in the constant current charging mode. If the bus voltage is less than 390 V, according to the battery operation curve (shown in Figure 3.4), battery might operate in the droop control, constant current charging or discharging mode. Then the \( \text{flag}_{\text{cc}} \) is evaluated firstly and two possible consequences will show as follows:
i) If flag_cc equals to 1, which indicates the battery was in the constant current charging loop in the last state, and then voltage judgment will be adopted. If the bus voltage is lower than 380 V, the battery will switch to the droop control and flag_cc is set to zero. Otherwise, the battery will stay in the constant current charging mode.

ii). If flag_cc equals to zero, the battery might be in droop mode or the constant current discharging mode, then flag_cd will be estimated. If flag_cd equals to zero, battery will be in droop control mode. Otherwise, battery is in the constant current discharging mode in the last state and the bus voltage has to be evaluated. If the voltage is lower than 380 V, battery will stay in the constant current discharging mode. In the other way, battery will switch to the droop control mode and flag_cd is set to zero.

3.4.3 PV Control

In Figure 3.11, the control diagram of MPPT mode is depicted. PV panel current and voltage are sensed for control purpose. Perturb and observe (P&O) method is implemented in order to find the optimum operating voltage and achieve MPPT [78][79][80][81][82]. Meanwhile, dual loop control scheme is adopted in order to fast track the voltage reference.
3.4.4 Fuel Cell Control

The fuel cell dynamic response is slow, thus it is usually has a power control loop [83][84]. It has a dual control loop where the outer loop is the power control loop and the inner loop is the current control loop (shown in Figure 3.12).

3.5 Case Study and Simulation Results

To verify the proposed energy management strategy of the system and the distributed control algorithm for each module, the corresponding simulation models are built in Matlab/Simulink based on the diagram shown in Figure 3.2. The average model is adopted since the large scale system operation is preferred. Some key simulation parameters are listed.
in Table 3-3. Several typical cases are carried out and the key waveform results are shown. The power of DC MG in the follows Figures is the sum of the battery, PV and fuel cell’s output power. The dc bus voltage shown in Figures is the dc bus voltage value that the second order harmonic component has been filtered. The base values for the SST input voltage and current are 10 kV and 3 A respectively. The AC load is the PQ load where the active power is 1.1 kW and reactive power is zero.

<table>
<thead>
<tr>
<th>Table 3-3 Key Parameters for the Simulation.</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{dref}$</td>
</tr>
<tr>
<td>$i_{qref}$</td>
</tr>
<tr>
<td>$V_{p_ref}$</td>
</tr>
<tr>
<td>$R_b$</td>
</tr>
<tr>
<td>$R_{SST}$</td>
</tr>
</tbody>
</table>

1) Case I
This case is to evaluate that the system can seamlessly switch between the charging mode and discharging mode when the dc load changes. The initial value of dc load is 7 ohm, it step changes to 3.5 ohm at 1.5 s, and then back to 7 ohm at 4 s. The simulation results are shown in Figure 3.13.

Figure 3.13 (a) shows the typical PV irradiation curve and the PV output power, which verifies the MPPT control. The fuel cell’s output power and current are shown in Figure 3.11 (b). Since the fuel cell is always in constant power control loop and the fuel cell terminal
voltage is constant (except a very small oscillation when load changes), the output power and current curves verify the controller for fuel cell.

Figure 3.13 (c) shows the output power of SST and DC MG, which is defined as the total power of battery, PV, and fuel cell. Figure 3.13 (d) depicts the key waveforms of battery. Initially, the output power of SST and battery is negative because the PV and fuel cell’s output power is larger than the load needs, and the dc bus voltage is higher than 380 V. Their output power is not constant because the PV’s output power varies with different irradiation. When the load increases at 1.5 s, the battery and SST has to supply more power and switch to the discharging mode, the bus voltage is less than 380 V. Therefore at this point, the DC MG output power has a step step-up change because the battery’s output power changes from negative to positive. At 4 s, when the load switches back to 7 ohm, the SST and battery change back to the charging mode, so the SST and battery output power is back to the negative and the dc MG output power has a step-down change.

Figure 3.13 (e) depicts the AC input voltage and current of SST, which shows the power reverse at 4s. Since the oscillation of dc bus voltage is very small when load changes, the AC output voltage is very smooth (Figure 3.13 (f)). Figure 3.13 (g) shows the high dc side voltage of SST tracks its reference (11.4 kV) and only has a small oscillation at 1.5 s and 4 s. Since the low DC side bus is in the droop control, its value changes in range [370 V, 390 V] when the SST’s output power varies.
Figure 3.13 Simulation Results for Case I.
2) Case II
Case II is to evaluate the energy management strategy performance when the SOC of battery reaches the upper-limit and low dc side bus voltage reaches 400 V. The upper-limit of SOC is set to 80%, meaning battery will enter standby mode when SOC reaches this value. The initial value of the DC load is 5 ohm, then step change to 30 ohm at 1 s, finally changes to 3.5 ohm at 4 s. The simulation results are summarized in Figure 3.14.

The fuel cell output power and current waveforms are depicted in Figure 3.14 (a). The control algorithm for fuel cell is also verified in this condition. The output power of SST and DC MG is shown in Figure 3.14 (b). The key waveforms of battery are shown in Figure 3.14 (c). Initially, the SST and battery are in the discharging mode to supply the power to the system when the DC load is 5 ohm. When the load value decreases at 1 s, the SST and battery enter the charging mode (output power is negative) because the output power of PV and fuel cell is larger than the dc load. The output power of DC MG has a step change at this time. Meanwhile the low DC side bus voltage is greater than 380 V, as shown in Figure 3.14 (e). As soon as this bus voltage is greater than the constant current charging voltage limit (390 V), the battery enters the constant current charging mode and the current reference is 40 A as shown in Figure 3.14 (e). When the DC bus voltage reaches 400 V, SST enters the constant voltage control mode instead of droop control mode to keep the voltage at 400 V. Once the SOC of battery reaches 80%, it enters the standby mode. Then since the battery has stopped absorbing the power at 2.5 s, the absolute values of output power for DC MG and SST increase (Figure 3.14 (b)). At 4 s, due to load increasing, the bus voltage drops to 365 V, and SST outputs power to the system. As shown in Figure 3.9, the bus voltage signal for
battery algorithm selection is filtered to eliminate the transient noise. The time for battery going back to constant current discharging mode is 4.1 s. There is 0.1 s delay comparing to the time that bus voltage drops to below 370 V. The reference for discharging current is set to 40A. After the battery supplies the power to the system, the output power of DC MG increases, while the output power of SST decreases (Figure 3.14 (b)). The spikes occur at 4s because there is a big load changes at that time. SST transits from charging mode to discharging mode and then the bus voltage drops rapidly.

As shown in Figure 3.14 (d) for SST’s input voltage and current, the power reverse at 4s, coordinating with the power direction in Figure 3.14 (b). SST high and low DC output voltage is shown in Figure 3.14 (e). The Figures for the PV’s irradiation curve, PV’s output power and SST output AC voltage waveforms are shown in Figure 3.14 (f) and (g), respectively. The irradiation is same as case I, so the PV waveform is same as case I. Since the SST’s low DC bus voltage value is enough to generate the 120 V AC, there is no effect for the inverter’s output waveform when the DC bus voltage varies.
Figure 3.14 Simulation Results for Case II.
3) Case III

Case III is to evaluate the energy management strategy when the battery SOC reaches the lower limit and bus voltage reaches the lower limiter (360 V). The lower limit of SOC is set to 20%, meaning the battery will enter standby mode. The initial value of the DC load is 6.7 ohm, and then changes to 2.8 ohm at 1 s, finally changes to 12 ohm at 4 s. The corresponding simulation results are shown in Figure 3.15.

The fuel cell output power and current waveforms are depicted in Figure 3.15 (a) and the control algorithm is verified under this condition. The output power of the SST and DC MG is shown in Figure 3.15 (b). The key waveforms of battery are shown in Figure 3.15 (c). Initially, the SST and battery are in the charging mode to supply the power to the system. When the load changes at 1 s, the SST and battery enter the discharging mode and the output power of DC MG increases because the battery output power changes to positive from negative (Figure 3.15 (b)). When the dc bus voltage reaches 360 V as shown in Figure 3.15 (e), the SST will switch from droop control mode to constant voltage control mode. Furthermore, since the value is lower than the constant current charging voltage limit (370 V), the battery will enter the constant current discharging mode and the current reference will be 40 A (Figure 3.15 (c)). When the battery SOC reaches 20%, the battery will be in standby mode. The output power of DC MG decreases, while the output power of SST increases (Figure 3.15 (b)) because the battery stops supplying the power (Figure 3.15 (c)). The dc bus voltage will remain at 360 V, because it has already reached its lower limit. At 4 s, the bus voltage will increase to 395 V, and the output power of SST will become negative (Figure 3.15 (b)) because of the load decreasing. As discussed in case II, the time for battery going
back to constant current charging mode is 4.1 s, with 0.1 s delay compared with the time that takes bus voltage to increase above 390 V. The reference for charging current is set to 40 A. After the battery is back to charging mode, both the DC MG and SST output power will decrease because the battery absorbs the power from the system. The fast spikes occur on 4s because there is a big load changes at this time. SST transits from discharging mode to charging mode and then the bus voltage increases rapidly.

SST input voltage and current is shown in Figure 3.15 (d). Figure 3.15 (e) shows the SST high DC and low dc bus voltage. When the load changes and battery mode switches, the bus voltage oscillation is pretty small and the system is still stable. The Figures for the PV’s irradiation curve, PV’s output power and SST output AC voltage waveforms are shown in Figure 3.15 (f) and (g), respectively. The irradiation is same as previous cases, so the PV waveform is same. Similar to the case II, there is no side effect for the inverter’s output waveform when the DC bus voltage varies.
Figure 3.15 Simulation Results for Case III.
3.6 Summary

In this chapter, a novel distributed energy management strategy is proposed for SST enabled DC MG, which includes SST, DRERs (fuel cell, PV) and DESD (battery). SST is firstly adopted to enable the DC MG to interface AC system and the distribution system. The proposed distributed control algorithms for SST, fuel cell, PV and battery are presented. In this energy management strategy, the system can stable switch between charging mode and discharging mode without communication. The dynamic power sharing issue between SST and DC MG is investigated. In addition, since SOC of battery is considered into the energy management strategy, the battery can be intelligently managed to charge and discharged based on its SOC and the system information (DC bus voltage). To verify the proposed energy management strategy, the corresponding simulation model is constructed in Matlab/Simulink and the simulation results verify the proposed distributed energy management strategy.
Chapter 4 Hierarchical Power and Energy Management for SST Interfaced DC MG

4.1 Review and Motivation

In previous published literatures and introduction of chapter I, power and energy management strategy for DC MG can be summarized into three categories: centralized control, distributed control, and hierarchical control[45]-[51],[85]-[86]. J. M. Guerrero et. al proposed the hierarchical control for AC/DC MG in [12], [50]. As discussed in chapter I, the hierarchical control is a hybrid method, which combines the advantages of both centralized and distributed control and can be served as the standard for MG (the principles of hierarchical control will be detailed in Section 4.2). The system control strategy frame is categorized into three basic control layers: primary control, secondary control, and tertiary control. Each control layer takes effect on different time scales and the objective is to ensure that the MG can operate in islanding mode, grid-connection mode, and seamlessly transfer between these two modes.

Therefore, a novel hierarchical power and energy management for SST interfaced DC MG is proposed in this chapter. The chapter is organized as follows: the system introduction is introduced in section 4.2; the primary control for a typical DC MG is illustrated in Section 4.3 which includes each device control algorithm in system, such as PV control algorithm, battery control algorithm, fuel cell control algorithm and load control; the secondary control for DC MG is depicted in section 4.4; and the tertiary control is illustrated in section 4.5; simulation and experimental results to verify the system performance are shown in section 4.6; and the last section is the conclusion.
4.2 System Introduction

As shown in Figure 4.1, a typical DC MG is constructed in the FREEDM system. The DC MG includes DESD such as battery and DRERs such as PV, fuel cell as well as DC loads. These devices are connected to the common DC bus by DC/DC converters. The load is divided into the critical load and non-critical load to deal with some extreme cases in islanding mode. To implement hierarchical control, the low bandwidth communication ports are embedded into the system. The communication is bidirectional and all the DC MG system information will be sent to the SST controller. Thus, the controller of SST is selected as the centralized controller for DC MG. The DC/DC converters are not only controlled by individual local controllers, but can get the instructions from the SST’s controller. The corresponding hierarchical control is proposed which the objective is to ensure the whole system power balance and energy management.

![Figure 4.1 SST-enabled DC MG Diagram.](image-url)
The basic structure of hierarchical control strategy is depicted as Figure 4.2. The primary control is the distributed control essentially which the objective is to ensure the DC MG system’s power balance (IPM) without communication. Thus, the primary control usually takes effect on microsecond level, which is basically the power converter control, such as the voltage control, current control, and e.t.c. All the local information, including the DESD, DRERs output voltage, output current, SOC for the battery and so on, are sent to the upper controller (SST controller), which implements the tertiary control and secondary control through a bidirectional communication link. The objective of secondary control is to recover the DC MG bus voltage to equal the SST output low dc voltage. Then seamless switch will be achieved when the DC MG connects to SST from islanding mode to SST-enabled mode. The time scale for the secondary control is millisecond or second level. After the DC MG enters SST-enabled mode, the DC MG system power balance can be always guaranteed if the SST can deliver enough power from or to the grid. Furthermore, SST collects all the DC MG system information as the centralized controller for the DC MG. Thus, the tertiary control is the energy management (IEM) for the SST interfaced DC MG system. Usually, the tertiary control objective is control the power common coupling (PCC) power flow between SST and DC MG. In this novel energy management strategy, the battery SOC management is also involved. The tertiary control can intelligently switch its control objective between PCC power flow control and battery’s charging or discharging control based on its SOC information. The time scale for the tertiary control is longer than the primary control and secondary control, usually in minute or hour level.
As shown in Figure 4.1, when the DC MG disconnects from the SST, MG operates in islanding mode. While the DC bus connects to the SST, the MG is in SST-enabled mode. As discussed in chapter 3, the DC MG system information is very complicated and time variable. Therefore, to supply a reliable and high quality power to the load or SST, the major control objective is to maintain the system power balance. As shown in equation (4.1),

$$P_{SST} + P_{DC\_MG} + P_{AC\_MG} = P_{Load}$$  \hspace{1cm} (4.1)

where, $P_{SST}$ is the SST output power, $P_{DC\_MG}$ is the power supplied by the DC microgrid, $P_{AC\_MG}$ is the power delivered by the sources AC microgrid, and $P_{Load}$ includes the load power in both the AC and DC microgrid. Since the AC MG is not this chapter focus, so the AC MG is represented as a typical RL load. Thus,

$$P_{DC\_MG} = P_{DREER} + P_{DESD}$$  \hspace{1cm} (4.2)

$$P_{AC\_MG} = 0$$  \hspace{1cm} (4.3)

$$P_{Load} = P_{AC\_Load} + P_{DC\_Load}$$  \hspace{1cm} (4.4)
Based on the system structure is shown as Figure 4.1, the equation (4.5) can be concluded as follows.

\[ P_{DC\_MG} = P_{Battery} + P_{Fuel\_cell} + P_{PV1} + P_{PV2} \quad (4.5) \]

Here, the battery power is defined as positive when it outputs power. For the power of battery can be concluded as follows:

\[ P_{Battery} = V_b I_b \quad (4.6) \]

Where, \( V_b \) is the battery module DC terminal output voltage and \( I_b \) is the battery module output current. SST output power can be defined as

\[ P_{SST} = V_{dc} I_{dc} \quad (4.7) \]

Where, \( V_{dc} \) is the SST DC terminal output voltage and \( I_{dc} \) is the SST dc output current.

Figure 4.3 depicts the equivalent circuit of DC bus, where the \( C_{eq} \) is the equivalent capacitor on the DC bus. Thus, the capacitor voltage dynamic can be given as follows.

\[ C_{eq} V_{dc} \frac{dV_{dc}}{dx} = (P_{SST} - P_{AC\_Load}) - (P_{DC\_Load} - P_{Battery} - P_{PV1} - P_{Fuel\_cell}) \quad (4.8) \]
Thus, the system power unbalance will cause the bus voltage change. From this perspective, the bus voltage represents the system power status.

4.3 Primary Control

4.3.1 Primary Control Method Review

As shown in Figure 4.1, when the switch interfaced SST DC output terminal and DC MG bus is off, the DC MG operates in islanding mode. This mode is common for some rural or remote areas which the distribution line can’t reach or the voltage sag occurs in the grid. Thus, the system power and energy management strategy for DC MG in islanding mode must match the follows requirements:

1) system power balance in islanding mode;
2) control algorithm is designed only on its local information without communication;
3) DRERs and DESDs characteristics should be considered in control algorithm
4) some extreme conditions should be involved in system power management

Thus, the principle purpose of primary control is to guarantee the system power balance in islanding mode. As shown in equation (4.1), when system is in islanding mode, the equations (4.9)-(4.11) can be concluded

\[ P_{DC-MG} = P_{DC-Load} \]  
\[ \sum_{i=1}^{2} P_{PVi} + P_{Fuel\_cell} + P_{battery} = P_{DC\_Load} \]  
\[ C_{eq} V_{dc} \frac{dV_{dc}}{dx} = (P_{Battery} + \sum_{i=1}^{2} P_{PVi} + P_{Fuel\_cell} - P_{DC\_Load}) \]

Based on equation (4.11), when the power generated by DRERs is greater than the load needs, the bus voltage will increases, and vice versa. So the battery is operating as a power
buffer for the system, like discussed in chapter 3. However, the battery’s ability of absorbing and supplying power is limited and based on its SOC. Thus, there are two extreme cases should be considered in islanding mode. The first one the battery and DRERs can’t supply enough power to the load, and the second one is the battery can’t absorb power from DRERs.

To make full use of this only system information (DC bus voltage) to implement the primary control, the DC bus voltage is no longer a constant value but varies in some range. DBS is adopted for the primary control. As discussed in chapter 3, the basic idea of DBS is that every device (whether it is DESD, DRER or load) in a DC MG is controlled based on its DC bus voltage to implement a power management strategy in distributed control. Some voltage thresholds are predetermined for each converter or load. As soon as the module detects its bus voltage reaching this value, the control algorithm will enter the corresponding control mode. Thus, the converter modules and load not only respond to the level of the DC bus voltage, but all of them will affect the DC bus voltage value after the modes change, thus automatically interfaces to other modules in the system. In one word, the DC bus voltage as a replacement for communication line to convey the system information among the modules in MG. Some papers [47]-[49] proposed some adaptive DBS. However, some of them just consider system operates in one mode instead of system mode switch, some of them just consider the system operates in normal conditions but ignore some critical cases.

In order to overcome these drawbacks and address the challenges discussed aforementioned, a novel primary control strategy for DC MG is presented. The main contributions of the proposed primary power management strategy can be summarized as follows:
1) power balance can be guaranteed in islanding mode;

2) the control algorithm design for local controller is only based on local information and individual module characteristic;

3) some extreme cases are studied and verified the proposed power management strategy;

4) the power management strategy is still valid in SST-enabled mode;

4.3.2 Primary Control Introduction

The DC bus voltage will be regulated by the battery’s DC/DC converter. Two PV DC/DC converters and one DC/DC converter for fuel cell transfer power generated by PVs and fuel cell to the DC bus. These PV converters power ratings are different, which PV I is greater than PV II. The DC/DC converter for the battery balances the power differences between the load and the power supplied by PVs and fuel cell. PVs and fuel cell output power is always greater than or equal to zero. When the PVs and fuel cell’s output power is greater than load, the battery will be charged and $I_b$ is negative; while the PVs and fuel cell’s output power is less than load, the battery will be discharged and $I_b$ is positive.

The system operation curve is shown in Figure 4.4, where 380 V is defined as the critical value. When the bus voltage is greater than this value, the system will be in the charging area; otherwise, the system is in discharging area. The charge and discharge areas are defined by the battery status.
The bus voltage range is from 320 V to 440 V. In islanding mode, only battery is responsible to support the DC bus voltage. Droop control is adopted for battery control (the droop equation is defined in section 4.3.3). Then when the DRERs’ (PVs and fuel cell) output power are larger than the load, the bus voltage is greater than 380 V and battery will be in charging area to absorb power. On the other way, when the DRERs’ output power is less than the load, the bus voltage is less than 380 V and battery will be in discharging area to supply power to load. Considering the battery characteristic (SOC limit) and the device’s voltage and current limit, the bus voltage can’t be too high or too low. Thus, some rules have to be made. In charging area, to avoid the bus voltage reach the high-limit value (440 V), a threshold is preset. When the bus voltage reaches 420 V, the smaller rating PV (PV I) will switch from MPPT mode to standby mode automatically, which means this PV won’t
generate power but still connect to the DC bus. Then two conditions follow: the first one is the DRERs’ power are less than load then the bus voltage will decrease; the other is the DRERs’ power are still greater than load, then the bus voltage will keep increasing. When the bus voltage reaches high-limit value (440 V), the battery will enter the constant voltage control from droop control to constant voltage control. In discharging area, battery is always to supply power to the load to support DC bus voltage. To avoid the battery deeply discharge, the load management strategy has to be included. The non-critical load will be shed from the system when the bus voltage is lower than some predefined threshold; the critical load is always connected to the system. Then the other threshold value (340 V) is preset. When the bus voltage reaches 340 V, the non-critical load is shed from the system automatically. Similar to the charging area, two consequences happen: the first one is the bus voltage recoveries if the output power of DRERs and battery is greater than load; while the other is the bus voltage keeps decreasing when the output power of DRERs and battery is still less than the load. When the bus voltage reaches 320 V, battery enters constant voltage control to keep bus voltage be constant value (320 V). To avoid system’s chattering, the voltage value for PV I back to MPPT mode from standby mode is that the bus voltage drops to 390 V; while the voltage value for non-critical load reconnects to the system is 370 V. An assumption is made that SST is considered as an infinite energy router between DC MG and distribution system. The assumption is reasonable because the SST’s power rating is much greater than the DC MG power rating, usually 10 times. The range for SST low DC output voltage is [360 V, 400V] which will be used for tertiary control. Therefore, the two extreme cases won’t occur in SST-enabled mode because of the voltage range.
4.3.3 Primary Control Diagram

Similar to the chapter 3, the droop control is adopted for the battery control strategy. The droop equation is shown in equation (4.12).

\[ V_b = V_0 - R_b I_b \]  

(4.12)

Where \( V_b \) is the reference of the battery converter output voltage, \( V_0 \) is battery converter output dc bus voltage without load and is set as 380 V, \( R_b \) is the droop slope and \( I_b \) is battery module output current. For PV I, it always operate in MPPT. While for PV II, to deal with the extreme cases, there are two modes: one is MPPT and the other one is stand-by mode. The fuel cell module is always in power control loop to supply a constant power to the system. Based on the control algorithms aforementioned for each device and load, the equivalent circuit of DC MG system in islanding mode is shown as Figure. 4.5, which the fuel cell and PVs are equivalent to current sources while the battery is a voltage source.

![System Equivalent Circuit in Islanding Mode](image.png)

(a) normal case  (b) load shedding  (c) PV II shedding

Figure 4.5 System Equivalent Circuit in Islanding Mode.
The primary control diagram for DC MG is shown in Figure 4.6. The DHB topology is selected as DC/DC converter for battery, PV and fuel cell is DHB. Thus, the controllable variable is the shifted phase angle between primary side and secondary side of the DHB. The more details for DHB control can be referred to Chapter 2. Since the DC system has no frequency component, the filter is adopted to filter the DC bus voltage dynamic noise. Thus, it can be designed as the mean value filter.
4.4 SST Control Algorithm

The modeling for SST is depicted in Chapter 3. Thus, only DAB control diagram is shown in Figure 4.7 because the only difference for SST’s control is its low DC out voltage is regulated as constant instead of in droop control. The SST’s low DC output terminal voltage reference is set as 380 V when DC MG disconnects from SST.

![Figure 4.7 SST DAB Control Diagram.](image)

4.5 Secondary Control Algorithm

Since the DC bus voltage is regulated in droop control in islanding mode, its bus voltage might have some deviations from SST DC terminal output voltage. To achieve the seamless switch from islanding mode to SST-enabled mode, the secondary control is adopted. The SST’s low DC terminal voltage is sensed and compared with the DC MG bus voltage. The error is processed by a compensator and the output is sent to the battery unit by the low bandwidth communication to restore the DC MG bus voltage (see Figure 4.8). Since the DRERs and load control don’t contribute to regulate the DC bus voltage, their control algorithm is same as shown in Figure 4.5 and is omitted here.

The controller can be represented as follows:
$V_s = k_{sp}(V_{SST_{dcout}} - V_{bus}) + k_{si}(V_{SST_{dcout}} - V_{bus})/s \quad (4.13)$

Where $k_{sp}$ and $k_{si}$ are the control parameters for the secondary control. Thus, for battery droop control, the equation (4.12) becomes:

$$V_b = V_0 - R_b I_b + V_s \quad (4.14)$$

Based on equation (4.14), the key point for secondary control is to shift the droop curve (see Figure 4.9). When the SST’s low DC output voltage is higher than DC MG bus voltage, $V_s$ is larger than zero and the droop curve is shifted above (battery operation point from a to b), and vice versa (battery operation point from c to d).

Figure 4.8 Secondary Control Diagram.

Figure 4.9 Droop Curve Shift with Secondary Control.
4.6 Tertiary Control Algorithm

Usually, the tertiary control is to control the PCC power flow [17], meaning the power flow interfaced between DC MG and SST. The DC MG PCC power flow is depicted as Figure 4.10 and defined as equation (4.15).

\[ P_{MG} = V_{ldc}i_{MG} \]  

(4.15)

![Figure 4.10 DC MG PCC Power Flow Diagram.](image)

As discussed before, since PV is in MPPT and the fuel cell is in constant power control, the essence of the PCC power flow control is to control battery output power. For example, if the desired PCC power flow increases, the battery has to output more power. However, the appropriate SOC value is beneficial for battery to support DC MG operates in islanding mode and also is good for battery health. While if the SST’s low DC output voltage is constant or the conventional droop control is applied for battery, the battery can only operate in single mode (charge, discharge or standby mode). Thus, SOC is included into the tertiary control, either. When battery SOC is in the predetermined range, the tertiary control is to control DC
MG PCC output power. On the other way, when the battery SOC is out of the range, the tertiary control is to manage the battery to charge or discharge mode. So the SOC control has a higher priority than PCC power flow control, meaning that if SOC signal is enabled, PCC power flow control signal will be disabled and the tertiary control begins to charge or discharge battery. The battery charge or discharge can be determined by the SST DC voltage and battery droop curve. Thus, there are two options for tertiary control strategy. The first one is to change SST’s low DC terminal output voltage and the secondary is to shift the battery droop curve. Since the secondary control is to make the DC MG bus voltage equal to the SST output voltage, the secondary control will be disabled when the tertiary control comes into effect.

4.6.1 PCC Power Flow Control by Changing SST Low DC Output Voltage

As depicted in Figure 4.11, SOC is evaluated and processed by the tertiary control objective selection block to determine the control objective. When SOC is in range, tertiary control is PCC power flow control. DC MG output power compared to the reference, and the controller can be represented as follows:

\[ V_{il} = k_{ilp} (P_{ref} - P_{MG}) + k_{ili} (P_{ref} - P_{MG})/s \]  

(4.16)

Where \( k_{ilp} \) and \( k_{ili} \) are the control parameters for the tertiary control of PCC’s power flow. Then, the bus voltage reference (the SST DC output voltage reference) can be shown as equation (4.17):

\[ V_{Bus\_ref} = V_{SST\_dcref} - V_{il} \]  

(4.17)
So if the $P_{ref}$ is greater than $P_{MG}$, the SST output voltage will drop and the battery will generate more power to the system, and vice versa (Figure 4.12).

Figure 4.11 Tertiary Control Diagram for DC MG Power Flow Control and Change SST DC Voltage to Manage Battery Status.

(a) $P_{ref}$ less than $P_{MG}$  
(b) $P_{ref}$ greater than $P_{MG}$

Figure 4.12 SST DC Voltage Changes for PCC Power Flow Control.
4.6.2 SOC Control by Changing SST Low DC Output Voltage

If the SOC is out of range, then the tertiary control is to charge or discharge battery instead of controlling PCC power flow. For example, if the SOC reaches the Hsoc (upper limit for SOC), $I_{ref}$ equals to $I_d$ (discharge current for battery) and the tertiary control enters battery SOC management process. The controller can be represented as follows:

$$V_{t2}=k_{t2p}(I_{ref}-I_b)+k_{t2i}(I_{ref}-I_b)/s$$  \hspace{1cm} (4.18)

Where $k_{t2p}$ and $k_{t2i}$ are the control parameters for the tertiary control of SOC. Then, the SST output voltage reference can be shown as equation (4.19):

$$V_{bus\_ref} = V_{SST\_dc\_ref} - V_{t2}$$  \hspace{1cm} (4.19)

Thus, the SST DC output voltage will decrease and the battery will be discharged (Figure 4-13 (a)), and vice versa Figure 4-13 (b)).

(a) SOC to Lsoc  
(b) SOC to Hsoc

Figure 4.13 SST DC Voltage Changes for SOC Control.
4.6.3 PCC Power Flow and SOC Management by Shifting Battery Droop Curve

Similar to the previous tertiary control strategy, SOC is evaluated and processed by the tertiary control objective selection block to determine the control objective. Different from the first tertiary control method, this tertiary method controls PCC power flow or SOC by shifting the battery droop curve. As shown in Figure 4.14, when SOC is in range, tertiary control is PCC power flow control. DC MG output power compared to the reference, and the controller can be represented as follows:

\[ V_{t3} = k_{t3p}(P_{\text{ref}}-P_{MG}) + k_{t3i}(P_{\text{ref}}-P_{MG})/s \]  \hspace{1cm} (4.20)

Where \( k_{t3p} \) and \( k_{t3i} \) are the control parameters for the tertiary control of PCC’s power flow. Then, the battery droop curve can be shown as equation (4.21):

\[ V_b = V_0 - R_b I_b + V_{t3} \]  \hspace{1cm} (4.21)

So if the \( P_{\text{ref}} \) is greater than \( P_{MG} \), the battery droop curve will shift up to generate more power to the system, and vice versa (Figure 4.15). The following battery control block is the battery voltage and current control (shown in Figure 4.6).

If the SOC is out of range, then the tertiary control is to charge or discharge battery instead of control PCC power flow. For example, if the SOC reaches the \( \text{Hsoc} \) (upper limit for SOC), \( I_{\text{ref}} \) equals to \( I_d \) (discharge current for battery). The controller can be represented as follows:

\[ V_{t4} = k_{t4p}(I_{\text{ref}}-I_b) + k_{t4i}(I_{\text{ref}}-I_b)/s \]  \hspace{1cm} (4.22)

Where \( k_{t4p} \) and \( k_{t4i} \) are the control parameters for the tertiary control of SOC. Then, the battery output voltage reference can be shown as equation (4.23):

\[ V_b = V_0 - R_b I_b + V_{t4} \]  \hspace{1cm} (4.23)
Thus, the battery droop curve will shift up and the battery will be discharged, and vice versa (Figure 4.16).

Figure 4.14 Tertiary Control Diagram for DC MG by Shifting Battery Droop Curve.

Figure 4.15 Battery Curve Shift for PCC Power Flow Control.

Figure 4.16 Battery Curve Shift for SOC Control.
4.6.4 Pros and Cons for Two Tertiary Control

Comparing these two methods for tertiary control, they both can achieve battery charge and discharge management and PCC power flow control. The advantage for first one is that the communication is excluded from the control part and the system reliability increases because there is no need to send instruction to the battery module. The disadvantages are 1) the load power which connects to the DC bus changes since the DC bus voltage changes; 2) DC bus voltage changing range is limited by the SST output voltage range. The advantages for the second one are 1) the load power which connects to the DC bus is same since there is no change in DC bus voltage; 2) the shifting range for battery droop curve is only based on battery capacity instead of the bus voltage limitation. While the disadvantage of this tertiary control is that the instructions of shifting item need to be convey from SST side to the battery and the time delay needs to be considered. The system reliability decreases by the communication. Which one is selected will be based on the trade-off their advantages and disadvantages.

4.7 Simulation and Experiment Verifications

To verify the proposed hierarchical control strategy, the simulation is carried out based on the average model built in Matlab/Simulink. The system structure is shown in Figure 4.1. Several typical cases are carried out and the key results are shown. The parameters for PVs, fuel cell and battery are listed in Table 4-1.
### Table 4-1 Key Simulation Parameters

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<th>Parameter</th>
<th>Value</th>
<th>Parameter</th>
<th>Value</th>
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</thead>
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<td>290 V</td>
<td>$I_{oc (PVI)}$</td>
<td>50 A</td>
</tr>
<tr>
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<td>40 A</td>
<td>$V_{oc (PVI)}$</td>
<td>290 V</td>
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<td>40 A</td>
<td>$I_{max (PVI)}$</td>
<td>30 A</td>
</tr>
<tr>
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<td>Rated Capacity</td>
<td>50 AH</td>
</tr>
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<td>$V_{fuel _nom}$</td>
<td>300 V</td>
<td>$I_{fuel _nom}$</td>
<td>100 A</td>
</tr>
</tbody>
</table>

#### 4.7.1 Primary Control Simulation and Experiment Verifications

**a. Simulation Verification**

**Case I: Non-critical load shedding and back**

This case is to evaluate the non-critical load shedding and back performance when the DC MG is in the islanding mode. The DC bus voltage values for load shedding and back are set as 340 V and 370 V respectively. To make sure the bus value can reach these two values, the irradiation for PV is step changes from a constant value to other constant values instead of a sine curve. The irradiation step changes from 1000 w/m$^2$ to 200 w/m$^2$ at 1s and back to 1000 w/m$^2$ at 3s. Initially, a critical load and non-critical load are connected to the DC bus, where their values are 8 Ohm and 16 Ohm respectively. At 2s, the critical load step changes to 4.8 Ohm. The simulation results are summarized in Figure 4.17.
Figure 4.17 Simulation Results for Non-critical Load Shedding and Back.

(a) PV output power & irradiation

(b) DC MG power, bus voltage & noncritical load control signal

(c) battery information

(d) fuel cell information
Figure 4.17 (a) shows the PV irradiation curve and the PV output power, which PV output power tracks the irradiation curve changes and verifies the MPPT. The fuel cell output power and current waveforms are depicted in Figure 4.17 (d). The control algorithm for fuel cell is also verified in this condition.

The DC MG output power, DC bus voltage and the control signal for non-critical load are depicted in Figure 4.17 (b). The key waveforms of battery are shown in Figure 4.17 (c). Initially, the battery is in the charging mode to absorb the power from the system and the bus voltage is greater than 380 V. When the irradiation decreases at 1 s, the battery enters the discharging mode (output power is positive) because the output power of PV and fuel cell is less than the DC load. The output power of DC MG step changes to a small value at this time. Meanwhile the DC bus voltage drops to 350 V, which is still greater than 340 V (the voltage value for load sheds). Then the non-critical load is still connected to the DC bus and the control signal for this load is still 1, which means the load isn’t shedding. At 2s, the critical load changes to a small value, then the bus voltage keeps decreasing. As soon as the filtered DC bus voltage for load control is less than 340 V, the control signal for non-critical load turns to zero, which means this non-critical load is shedding. After the load sheds, the bus voltage gets recovery (about 345 V). When the irradiation recovers to 1000w/m² at 3s, the DC bus voltage keeps increasing since the DC MG system output power increases. As soon as the filter DC bus voltage for load control is greater than 370 V, the control signal for non-critical load turns to one, which means this non-critical load is connected back to the system. As shown in Figure 4.6, the bus voltage signal for load control algorithm selection is filtered to eliminate the transient noise. The time for load sheds and back is 2.1 s and 3.1 s
respectively. There are about 0.1 s delays comparing to the times that bus voltage drops to below 340 V and increases back to 370 V because of the bus voltage filter’s time delays.

Case II: PV II shedding and back

This case is to evaluate the performance which PV II module sheds and back to the system. The DC bus voltage values for PV II shedding and back are set as 420 V and 390 V respectively. Similar to the case II, the irradiation for PV is step changes from a constant value to other constant values instead of a sine curve. The irradiation step changes from 400 w/m\(^2\) to 1000 w/m\(^2\) at 1s and changes to 700 w/m\(^2\) at 3s. The initial value of the DC load is 7.5 Ohm, and then step changes to 4.5 Ohm at 4 s. The corresponding simulation results are shown in Figure 4.18.

Figure 4.18 (a) shows the PV irradiation curve and the PV output power, which PV output power tracks the irradiation curve changes. The fuel cell output power and current waveforms are depicted in Figure 4.18 (b). The control algorithm for fuel cell is also verified in this condition. The DC MG output power, DC bus voltage and the control signal for PV II are depicted in Figure 4.18 (c). The key waveforms of battery are shown in Figure 4.18 (d). Initially, the battery is in the charging mode to absorb the power from the system and the bus voltage is greater than 380 V. When the irradiation increases at 1 s, the battery absorbs more power from the system and the bus voltage keeps increasing. As soon as the filtered DC bus voltage for PV II control is greater than 420 V, the control signal for PV II become zero which means PV II operates in stand-by status and no output power. After the PV II enters stand-by mode, the bus voltage decreases to a stable value (about 420 V). The output power of DC MG increases because the PV I output power gets large increase even the PV II has no
output power. At 3 s, the irradiation changes to 700, then PV I output power decreases and the bus voltage drop to 415 V. Meanwhile the DC bus voltage is still greater than 390 V (the voltage value for PV II reproducing power to the system). Then the PV II is still in the stand-by mode and the control signal for PV II is still 0, so PV II still has no output power. At 4s, when the load changes to a small value (4.5 Ohm), the battery module has to switch back discharging mode to supply power to the DC MG system. Correspondingly, the bus voltage is dropping. As soon as the filtered DC bus voltage for PV II is less than 390 V, the control signal for PV II turns to one, which means PV II backs to MPPT mode from stand-by mode and supplies power to the system. After PV II is back to MPPT mode, the bus voltage recoveries (about 360 V). The output power of DC MG increases since all DRERs and DESD supply power to the system. As shown in Figure 4.6, the bus voltage signal for PV II control algorithm selection is filtered to eliminate the transient noise. The time for PV II entering into stand-by mode and back to MPPT is 1.1 s and 4.1 s respectively. There are about 0.1 s delays comparing to the times that bus voltage increases to 420 V and drops back to 390 V because of the bus voltage filter time delays.
b. Experimental Verification

The experiment is carried out to verify the control algorithms. The hardware testbed is shown in Figure 4.19. The system is scaled down which consists of a 500 W battery module and a 200 W PV module. A DC source is adopted to simulate the PV. The load shedding and
Figure 4.19 PV and Battery Testbed.

Figure 4.20 Waveform for Load Shedding.

Back case result is shown in Figure 4.20 and the PV shedding and back case result is shown in Figure 4.21. The key parameters for hardware are listed in Table 4-2 and the symbol is explained in Table 4-3.
Figure 4.21 Waveform for PV Shedding and Back.

Table 4-2 Hardware key parameters.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_{\text{battery}}$</td>
<td>6 uH</td>
</tr>
<tr>
<td>$I_{\text{PV, MPPT}}$</td>
<td>2.5 A</td>
</tr>
<tr>
<td>$V_{\text{PV, shedding}}$</td>
<td>395 V</td>
</tr>
<tr>
<td>$R_{\text{critical}}$</td>
<td>2 kohm</td>
</tr>
<tr>
<td>$L_{\text{PV}}$</td>
<td>4 uH</td>
</tr>
<tr>
<td>$f$</td>
<td>50 kHz</td>
</tr>
<tr>
<td>$V_{\text{PV, back}}$</td>
<td>375 V</td>
</tr>
<tr>
<td>$R_{\text{PV, critical}}$</td>
<td>1 kohm</td>
</tr>
<tr>
<td>$V_{\text{source}}$</td>
<td>48 V</td>
</tr>
<tr>
<td>$V_{o}$</td>
<td>380 V</td>
</tr>
<tr>
<td>$V_{\text{load, shedding}}$</td>
<td>365 V</td>
</tr>
<tr>
<td>$V_{\text{PV, MPPT}}$</td>
<td>45 V</td>
</tr>
<tr>
<td>$R_{0}$</td>
<td>54</td>
</tr>
<tr>
<td>$V_{\text{load, test}}$</td>
<td>385 V</td>
</tr>
</tbody>
</table>

Table 4-3 Symbols for Hardware Testbed Parameters.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_{\text{battery}}$</td>
<td>leaking parameter for battery module</td>
</tr>
<tr>
<td>$L_{\text{PV}}$</td>
<td>leaking parameter for PV module</td>
</tr>
<tr>
<td>$V_{\text{source}}$</td>
<td>battery nominal voltage</td>
</tr>
<tr>
<td>$V_{\text{PV, MPPT}}$</td>
<td>voltage for PV at MPPT</td>
</tr>
<tr>
<td>$I_{\text{PV, MPPT}}$</td>
<td>current for PV at MPPT</td>
</tr>
<tr>
<td>$f$</td>
<td>switching frequency for PV and battery</td>
</tr>
<tr>
<td>$V_{\text{PV, shedding}}$</td>
<td>voltage threshold for PV shedding</td>
</tr>
<tr>
<td>$V_{\text{PV, back}}$</td>
<td>voltage threshold for PV back</td>
</tr>
<tr>
<td>$V_{\text{load, shedding}}$</td>
<td>voltage threshold for noncritical load shedding</td>
</tr>
<tr>
<td>$V_{\text{load, back}}$</td>
<td>voltage threshold for noncritical load back</td>
</tr>
</tbody>
</table>
The worst case for bus voltage dropping is that only battery supplies the power to the load without PV. Initially, only one battery supplies the critical load. The battery outputs power to the load. Then one PV parallels to the system and its output power is greater than load, thus the battery switches to the charging mode and bus voltage increases. Then the non-critical load connects to the system, the battery has to go back to discharge mode to output power and bus voltage droops. While the value of bus voltage is still than the threshold value for load shedding, the critical load still connects to the system. When PV has no power to the system, the battery output power increases and the bus voltage keeps decreasing. Since the time value for the bus voltage filter is 0.5 s, after 0.5 s as the bus voltage less than 365 V, the non-critical load is shedding from the system. Then bus voltage gets some recovery. When the PV is back to the system, the bus voltage increases and the battery output current decreases. Same as the load shedding, after 0.5 s as the bus voltage greater than 380 V (threshold value for load back), the non-critical load reconnects to the system. After the load back, PV output power is less than the load, so the battery is in the discharge mode.

For PV shedding case, initially, the battery supplies the critical load alone. Then PV panel connects to the bus and supply the power to the system. The bus voltage increases and the battery output current decreases. But the battery still output power to the load and the bus voltage is less than 380 V, so the PV is still on the MPPT mode. As the load decreases to zero, the bus voltage increases and the battery switches from discharging mode to the charging mode. Since the time value for the bus voltage filter is 0.5 s, after 0.5s as the bus voltage is greater than 395 V, the PV is in stand-alone mode and no output power to the system. Then the battery’s output power is almost zero and the bus voltage is
380 V. When the load is back to system, the bus voltage decreases and the battery output current increases. Different from the PV enters to standby mode, after 1.5 s as the bus voltage is less than 375 V, the PV is back to MPPT mode from standby mode because there is about 1 s for PV module soft-start time. After the PV back, the voltage gets some recovery and the battery output current decreases.

4.7.2 Secondary Control Simulation and Experiment Verifications

Case I: without secondary control

Simulation Verification

This case is to evaluate the performances when the DC MG connects to the SST without secondary control. The load in DC MG is 4ohm and the load connects to the SST DC terminal is 20 ohm, while the AC load is still the RL load which R equals 10 ohm and L equals 100 uH. The simulation results are depicted in Figure 4.22.
Figure 4.22 Simulation Results without Secondary Control.
Figure 4.22 (a) shows the DC MG and SST output power. DC MG is in islanding mode and output power to the load, thus its DC bus voltage is much less than 380 V (360 V). When the MG enters to the SST-enabled mode, there is about 20 volts difference between SST DC bus and MG DC bus. Thus, there is a huge inrush on SST output power because the SST bus capacitor has to output power to the DC MG bus capacitor. After the bus voltage reaches constant, based on the droop control, the battery won’t output power to the load because the \( V_0 \) equals DC bus voltage (380 V). This explains the DC MG output power decreases after the system enters to the SST-enabled mode. Figure 4.22 (e) also verifies it which the SOC keep constant value after 1.6 s. For the PV modules and fuel cell module, one is in MPPT control and the other one is in constant power control, which the Figure 4.22 (b) and (c) verify them respectively.

Case II: secondary control

a. Simulation Verification

This case is to evaluate the performances when the DC MG connects to the SST with secondary control. The system information is exactly same as the case I. The simulation results are depicted in Figure 4.23. The time scale for secondary control is 0.001 s. Before the secondary control operates, battery output power to the load and the DC MG bus voltage is less than 380 V, same as the case I. Then the secondary control begins to work at 1.1s. As shown in Figure 4.23 (f), the MG bus voltage begins to increases to match the SST DC output voltage. When it reaches 380 V (SST DC output voltage), it keeps constant. Based on the equation (4.14) and Figure 4.23, since the DC MG bus voltage is less than 380 V, to recovery this voltage, the droop curve has to be lifted. Thus, the battery has to output power
when the bus voltage recovers to 380 V. After the DC MG bus voltage recovers to 380 V, DC MG connects to SST at 1.6 s. Noticed that there is still a small oscillation on SST output power even the those two DC voltages equal. This is because the SST bus voltage has secondary harmonic component and the wave shown in the Figure is the filtered result. Since the droop curve is lifted, different from the case I, after the DC MG enters SST-enabled mode, battery still outputs current to the system. In the period between secondary control starts and the time connecting to SST, the output current of battery is not constant even the bus voltage keeps 380 V. This is because the PVs in MPPT control and their output power is not constant but tracking the irradiation curve.
(a). SST and DC microgrid output power

(b). PV information

(c). Fuel cell information

(d). SST AC output waveform

(e). Battery information

(f). DC voltage value

(g). Control signal

Figure 4.23 Simulation Results with Secondary Control.
b. Experimental Verification

A FPGA+DSP control platform was developed to control the SST. A laboratory prototype of a single-phase, three-stage SST (Figure 3.1) was built, as shown in Figure 4.24, cascaded multilevel rectifier with three H-bridges is adopted as the front-end stage to interface with 1.2KV grid. Three DAB converters are connected to each DC link with secondary side parallel as the DC/DC step down stage, in which 380V dc bus is enabled. In the last stage, and single phase inverter is adopted to provide 120V AC. The design and implementation of SST can be referred to [89].

Figure 4.24 A Cascaded Type Three Stage SST Prototype.
To verify the secondary control algorithm, experimental results are shown in Figure 4.25. The communication ports are not included in this chapter so a software trigger is adopted to start the secondary control and the time step for secondary control is 0.001 s.

Figure 4.25 (a) shows steady state operation waveforms of SST, including input voltage and current, high voltage dc, and output low voltage ac. The current is in phase with the voltage at high voltage side, indicating the unity power factor operation. The input voltage is not smooth because a set-up transformer is adopted to boost the input voltage of SST. The transformer has some impedance, thus the system can be considered operate in a weak grid, while this will not affect any conclusion.

Figure 4.25 (b) shows the SST waveforms, including the input voltage and current, high voltage dc of one AC/DC power stage, and low voltage dc. In Figure 4.25 (c), before the secondary control loop starts, the DC MG bus voltage is less than the 380 V because the battery and the PV have to supply power to the load. As soon as the secondary control loop begins to operate, the MG bus voltage keeps increasing with the secondary control time step until it reaches 380 V. Then the DC MG connects to the SST, and the seamless switch is achieved. Furthermore, as mentioned before, the battery droop curve is lifted because of secondary loop. Therefore, when system is in SST-enabled mode, the battery still outputs current to the load. For PV module, there is no change in its output voltage and current because it always operates in MPPT loop shown in Figure 4.25 (d).
4.7.3 Tertiary Control Simulation and Experiment Verifications

a. Changing SST DC Output Voltage Simulation Verification

This case is to verify the tertiary control algorithm by changing SST low dc output voltage and the simulation results are shown from Figure 4.26 to Figure 4.29. Since the SST input
voltage, current, low AC output voltage and current are same with secondary control, their waveforms are omitted to save space. Same as the secondary control, both PV modules are in MPPT mode. Thus, only one PV module is simulated in this control layer. The PV irradiation is set as a constant (1000w/m²) and its output power is 10 kW (Figure 4.26). The fuel cell output power is still 20 kW. Initially, the system is in SST-enabled mode with the secondary control, thus, the bus voltage (SST low dc output voltage) is 380 V. The battery outputs power for voltage recovery and DC MG doesn’t deliver power to the SST. At 0.25 s, tertiary control begins to operate and the power reference for PCC is 5 kW. Thus, based on equation (4.17), the SST low dc output voltage decreases (Figure 4.28). Then the battery’s output current increases to supply more power to SST (Figure 4.26) and its SOC decreases rapidly (Figure 4.27). This is the reason why the DC MG output power and DC MG output power to SST increase in Figure 4.26 from 0.2 s. SST output power decreases because the DC MG supplies more power to the system. The battery Lsoc is set as 25%. When battery SOC reaches this value (2.25 s), the tertiary control objective switches to SOC control to charge the battery instead of PCC power flow control. So the SST low dc output voltage increases based on equation (4.19) (Figure 4.28). The battery charge current is set as 50 A. Thus, the battery output current changes to negative and battery starts to be charged (Figure 4.29). Then the DC MG output power and DC MG output power to SST decreases, while SST output power increases at 2.25 s (Figure 4.26). Figure 4.29 depicts the corresponding control flags for secondary control, PCC power flow control and SOC control.
Figure 4.26 Power Information Simulation Results in First Tertiary Control Strategy.

Figure 4.27 Battery Current & SOC Information Simulation Results in First Tertiary Control Strategy.
Figure 4.28 SST High and Low DC Voltage Simulation Results in First Tertiary Control Strategy.

Figure 4.29 Voltage Recovery Signal, PCC Control Signal & SOC Control Signal Simulation Results in First Tertiary Control Strategy.
b. Experimental Verification

Due to the limited AD channels in SST control board, only SOC management is implemented at tertiary control. The experimental results are shown in Figure 4.30. A software trigger is adopted to start the tertiary control to simulate the SOC reaches the L_{SOH}.

Figure 4.30 shows the SST waveforms, including the input voltage and current, high voltage dc of one AC/DC power stage, and low voltage dc. When the tertiary control starts, the SST output DC bus voltage increases because the item $V_c$ in equation (4.18) is less than zero. Figure 4.31 shows the SST AC side voltage, DC MG bus voltage and the battery current. It is noted that the secondary control is disabled before the tertiary control starts. Thus, the battery module’s output current is almost zero before the tertiary control starts. When the tertiary control starts, the DC bus voltage is increasing until the battery output current reaches its current reference (-2 A). Since the PV is still on MPPT and its curve is same as previous case, shown in Figure 4.32.
tertiary control starts
1) input current 5V/1A 10 V 1 s
2) input voltage 5kV 1 s
3) VhDC 500V 1 s
4) VlDC 200V 1 s

Channel 1
Channel 2
Channel 3
Channel 4

Figure 4.30 SST Waveform with First Tertiary Control.

1) AC output voltage 500 V 1 s
2) battery output current 100mV/1A 500 mV 1 s
3) DC bus voltage 200 V 1 s

Channel 1
Channel 2
Channel 3

Figure 4.31 Battery Current, DC MG Bus Voltage and SST AC Output with First Tertiary Control.
c. Tertiary Control by Shifting Battery Droop Curve

This case is to verify the tertiary control algorithm by shifting battery droop curve and the simulation results are shown as Figure 4.33. Since the SST input voltage, current, low AC output voltage and current are same with secondary control, their waveforms are omitted to save space. The PV irradiation is set as a constant (1000w/m²) and its output power is 10 kW (Figure 4.33). The fuel cell output power is 20 kW. Initially, the system is in SST-enabled mode with the secondary control, thus, the bus voltage (SST low dc output voltage) is 380 V. The battery outputs power for voltage recovery and DC MG doesn’t deliver power to the SST. At 0.2 s, tertiary control begins to operate and the power reference for DC MG PCC is 5 kW. Thus, based on equation (4.23), the battery droop curve has shift up while the SST low dc output voltage is still 380 V (Figure 4.35). Then the battery’s output current increases to
supply more power to SST and its SOC decreases rapidly (Figure 4.34). This is the reason why the DC MG output power and DC MG output power to SST increase in Figure 4.33 from 0.2 s. SST output power decreases because the DC MG supplies more power to the system. The battery Lsoc is set as 25%. When battery SOC reaches this value (1.4 s), the tertiary control objective switches to SOC control to charge the battery instead of PCC power flow control. So the battery droop curve has to shift down based on equation (4.24), while the SST low dc output voltage is still 380 V (Figure 4.35). The battery charge current is set as 50 A. Thus, the battery output current changes to negative and battery starts to be charged (Figure 4.34). Then the DC MG output power and DC MG output power to SST decreases while SST output power increases at 1.4 s (Figure 4.33). Figure 4.34 depicts the corresponding control flags for secondary control, PCC power flow control and SOC control.

Figure 4.33 Power Information Simulation Results in Second Tertiary Control Strategy.
Figure 4.34 Battery Current & SOC Information Simulation Results in Second Tertiary Control Strategy.

Figure 4.35 SST High and Low DC Voltage Simulation Results in Second Tertiary Control Strategy.
b. Experimental Verification

Same as the first tertiary control strategy, only SOC control is involved into the tertiary control for experimental verification. The experimental results are shown from Figure 4.37 to Figure 4.39. Similarly, a software trigger is adopted to start the tertiary control to simulate the SOC reaches the $L_{SOH}$ and the time step for tertiary control is 0.1 s.

Figure 4.37 shows the SST waveforms, including the input voltage and current, high voltage dc, and low voltage dc. When the tertiary control starts, different from the previous tertiary control, the SST output DC bus voltage keeps constant as 380 V. Figure 4.38 shows the SST AC side voltage, DC MG bus voltage and the battery current. When the secondary control loop stops, and the battery output current drops to zero because the $V_o$ equals to 380 V (the SST DC output voltage) without the voltage recovery item ($V_s$ equals to zero). After

Figure 4.36 Voltage Recovery Signal, PCC Control Signal & SOC Control Signal.
the battery’s output current reaches zero, the tertiary control loop is triggered and begins to operate (the green line goes to 3.3 V). Then the battery starts to charge until the current reaches the Ic (-2 A). Same as the first tertiary control method, the PV is still on MPPT and there is no effect for its waveform whether the secondary control stops or tertiary control starts, shown in Figure 4.39.

Figure 4.37 SST Waveform with Second Tertiary Control.
Figure 4.38 Battery Current, DC MG Bus Voltage and Control Flag with Second Tertiary Control.

Figure 4.39 PV Waveform with Second Tertiary Control.
4.8 Summary

In this chapter, a hierarchical power and energy management for DC MG is proposed which includes primary control, secondary control and tertiary control. The primary control is based on the distributed control level to guarantee the system operate well without communication. Furthermore, load shedding and PV shedding is considered and verified in primary control. The secondary control is adopted to eliminate the voltage difference between SST low DC output and DC MG bus voltage when DC MG switches from islanding mode to SST-enabled mode. Then the seamless switch is achieved. Furthermore, the battery SOC management and PCC power flow control are involved into the tertiary control. Usually, the tertiary control is to supply a constant power to the SST when the battery SOC in the range. While if the battery SOC is in the defined range, the tertiary control will control the PCC power flow. If the battery SOC is out of the operation range, the tertiary control will operate the SOC management to charge or discharge the battery instead of PCC power flow control. Two tertiary control methods are presented. One is to change SST DC output voltage and the other one is to change battery droop curve. The advantages and disadvantages for these two methods are analyzed. The simulation and experimental results verify it.
Chapter 5 Practical Issues for SST Interfaced DC MG

5.1 Introduction and Motivation

In previous chapters, some power and energy management strategies for SST interfaced DC MG are introduced, which includes distributed energy management, and hierarchical power and energy management. However, in the real applications, there are still a lots of practical issues need to be considered for SST interfaced DC MG system. These issues are very important to ensure the system to operate more reliable as well as the power and energy management strategy. This chapter will introduce some of the typical issues for practical application of SST interfaced DC MG, such as power balance issue for SST, SST interfaced DC MG blackout and system’s plug and play function requirements and implementation.

Figure 5.1 SST Topology.
5.2 Power Balance Issue for SST

SST topology is redraw in Figure 5.1, which is introduced in Chapter 3. SST functions in details can be referred [87]. Based on the modularized three-stage topology, a proper controller should be developed to ensure that: 1) the voltage sharing among the high voltage DC links in the rectifier stage should be guaranteed; 2) the power flow through each DAB converter in the DC/DC stage should be the same. An equivalent block diagram of SST is depicted in Figure 5.2. If the power balance achieves, equations (5.1), (5.2) and (5.3) can be concluded.

\[ P_{\text{Rec1}} = P_{\text{Rec2}} = P_{\text{Rec3}} \]  

\[ P_{\text{DAB1}} = P_{\text{DAB2}} = P_{\text{DAB3}} \]  

\[ V_{\text{hdc1}} = V_{\text{hdc2}} = V_{\text{hdc3}} \]

![Figure 5.2 SST Equivalent Block Diagram.](image)
However, in SST topology, the power balance can’t be guarantee because of the floating structure of high voltage dc link [88],[89] and the disunity for the hardware parameters, such as leaking inductance parameters of high frequency DC/DC transformers in DC/DC stage. Some methods [89],[90] [91] were presented to address this issue. [90] presented a method which guaranteed the rectifier stage power balance, while the DC/DC stage power balance issue wasn’t included because the mismatch parameters in DC/DC stage weren’t considered. Another power balance method was presented in [91], the rectifier and DAB’s power balance can achieve, but individual DC/DC’s output power needed to be calculated. The power balance method was adopted in [89] for rectifier and DC/DC stages. However, the rectifier stage’s information (all cascaded rectifiers’ active power duties) needs to be calculated and involved in DC/DC stage control. When the SST consists multiple modules for high voltage level application, one controller might not have enough ability to handle rectifier and DC/DC stages both. An option is that one controller is responsible for rectifier stage control and the other one is for the DC/DC stage control. This option can’t work efficiently without the communication ports involved, and then the system reliability will be degraded.

Thus, in this section, a distributed control strategy for SST is presented, in which a single phase dq control strategy is adopted for the cascade rectifier stage power balance [89], and a distributed power balance strategy is adopted to mitigate the power unbalance issue of DC/DC stage. Furthermore, the control strategies for rectifier and DC/DC stages are totally independent, which can guarantee the SST to operate well even multiple controllers needed in high voltage application. The simulation and experimental results are presented to verify the proposed method.
a) Rectifier Stage Power Balance Control

A single phase dq controller is adopted [89] and the control scheme is depicted as Figure 5.3. Active and reactive power is controlled by duty $d_d$ and $d_q$ respectively. Furthermore, the voltage balance controller is to generate the extra duty ($\Delta d$) which is added to $d_d$ to guarantee the rectifier stage power balance. The more details for rectifier stage control can be referred to [89].

![Figure 5.3 Single Phase DQ Control for Rectifier](image)
b) Distributed Power Balance Control Strategy for DC/DC Stage

1) Power Unbalance Issue Analysis

As [89] discussed, the unbalanced output power of DAB will occur because of the mismatch for the hardware parameters, such as leaking inductance parameters of transformers and devices. A typical DAB topology is shown in Figure. 5.4 and its operation and control algorithm details can be referred to [66],[92],[93] [94]. By adjusting the phase-shift between the primary side H bridge and the secondary side H bridge, the power delivered by DAB can be shown as equation (5.4)

\[ P_{DAB} = \frac{V_1V_2}{2\pi fNL_i} \Phi(1 - \frac{\Phi}{\pi}) \]  

(5.4)

![Figure 5.4 Typical DAB Topology.](image)

Where \( V_1, V_2 \) are the input and output voltage, respectively, \( N \) is the transformer turn ratio, \( f \) is the switching frequency, \( L_i \) is the leaking inductor, which is equivalent to primary side, and \( \Phi \) is the phase shift between the primary and secondary side.
Thus, it is can be easily concluded that in parallelized DAB stages of SST, if the input voltages are the same and the same phase shift is explored, the power unbalance will be caused by the mismatch of the parameters, which usually are represented as equivalent inductors. Then the high dc side voltages \(V_{\text{hdc}1}, V_{\text{hdc}2}, V_{\text{hdc}3}\) aren’t equal because the three DAB’s output power is different. Thus, different phases shift have to be concluded for the individual DAB stage.

2) Distributed Control Strategy to Mitigate DC/DC Stage Unbalance Power

To increase the system reliability, droop control is a good option for parallel converters in distributed control. The conventional droop control is shown as equation (5.5). When it’s applied to the parallel DAB stage of SST, \(V_i\) is the ith DAB output voltage, \(V_{\text{imax}}\) is the ith DAB output voltage without load and \(k_i\) is virtual resistor for the ith DAB.

\[
V_i = V_{\text{imax}} - I_i k_i \quad (5.5)
\]

The equivalent circuit for two parallel DAB converters of DC/DC stages is depicted in Figure. 5.5. \(R_{\text{line}1}\) and \(R_{\text{line}2}\) are the line impedances from DAB output terminals to the load. The values of line impedances are very small comparing to the virtual resistors (\(k_1\) and \(k_2\)). Thus, the voltage drops on \(R_{\text{line}1}\) and \(R_{\text{line}2}\) can be ignored. Then equations (5.6) can be concluded as following:
Based on the equations (5.5) and (5.6), if $k_1$ and $k_2$, $V_{1\text{max}}$ and $V_{2\text{max}}$, are selected the same values, respectively, the output current of two DABs are the same and the power balance is achieved. Followed by the equation (5.4), if the leaking inductors are different, different phase shifts will be generated.

However, the major disadvantage of droop control is that the output voltage is not constant but varies with the load, meaning that the output voltage drops when the load increases. To overcome this drawback, an adaptive droop method is adopted. Comparing to the conventional droop curve, an additional PI controller is added to eliminate the voltage drop caused by the droop control. The PI controller can be represented as equation (5.7):

$$V_{si} = k_{pi} (V_{i\text{max}} - V_{\text{load}}) + k_{ii} (V_{i\text{max}} - V_{\text{load}}) / s$$

(5.7)

Where $k_{pi}$ and $k_{ii}$ are the control parameters. Thus, the DAB control equation becomes:

$$V_i = V_{i\text{max}} - I_i k_i + V_{si}$$

(5.8)
Based on the equation (5.8), the key point for adaptive droop control is to shift the droop curve (see Figure. 5.6). The shifted value is dependent on the PI’s output. For example, when the DAB output voltage is less than the reference \( V_{\text{imax}} \) of output voltage, \( V_i \) is larger than zero and the droop curve is shifted above (operation point from a to b), and vice versa (operation point from c to d). The control diagram is depicted as Figure. 5.7.

Figure 5.6 Adaptive Droop Curve.

Figure 5.7 Adaptive Droop Control Diagram.
3) Simulation & Experiment Verification

To verify the proposed method, the corresponding simulation and experiment are carried out. A 10 kVA-switching model for SST is built in Matlab/Simulink. The simulation parameters are listed in Table 5-1. The key simulation results are depicted in Figure 5.8 and 5.9.

Figure 5.8 shows the simulation result without the current balance control strategy, while the voltage balance strategy is applied on high voltage side. The input voltage and current is shown in Figure 5.8 (a), where the cascade rectifier operates in unity power factor. The high DC and low DC side voltage of SST is depicted in Figure 5.8 (b) and (c) shows the three DAB output currents. Notice that the output currents of three DAB are unbalanced even the high DC side voltages are same (the voltage ripple is caused by the grid secondary harmonics), which agrees with the analyses in section II. Figure 5.8 (d) shows the inverter’s output current and voltage.

Figure 5.9 shows the simulation result with the proposed current balance control strategy for DAB stage. The high DC side voltage balance control is still applied to guarantee the cascade rectifier output voltage balances (Vhdc1, Vhdc2 and Vhdc3 in Figure 5.9 (a)). The three parallel DAB output currents are equal (Figure 5.9 (b)), meaning the three DABs’ output power is balanced with proposed control strategy. The output voltage of DAB’s low DC voltage is shown in Figure 5.9 (a). As discussed in section III, different from the conventional droop curve, the output voltage of DAB won’t drop as the load increase, but keeps as the constant value (200V). The input voltage, current and inverter’s output voltage and current are omitted because they are the same as the previous case.
Figure 5.8 Simulation Results without Current Balance Control.
Figure 5.9 Simulation Results with Proposed Current Balance Control.

Table 5-1 Simulation Parameters.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input L filter</td>
<td>135 mH</td>
</tr>
<tr>
<td>High voltage DC link capacitor</td>
<td>38 uF</td>
</tr>
<tr>
<td>High frequency transformers</td>
<td>Turn ratio: 9.5:1</td>
</tr>
<tr>
<td></td>
<td>Leaking inductance I: 25 mH</td>
</tr>
<tr>
<td></td>
<td>Leaking inductance II: 30 mH</td>
</tr>
<tr>
<td></td>
<td>Leaking inductance III: 30 mH</td>
</tr>
<tr>
<td>Low voltage DC link capacitor</td>
<td>20 uF</td>
</tr>
<tr>
<td>Output inverter filter</td>
<td>L: 1mH; C: 30 uF</td>
</tr>
<tr>
<td>AC input</td>
<td>3600 V (RMS)</td>
</tr>
<tr>
<td>High DC voltage reference</td>
<td>3*1900 V</td>
</tr>
<tr>
<td>Low DC voltage reference</td>
<td>200 V</td>
</tr>
<tr>
<td>(k_1, k_2, k_3)</td>
<td>0.5</td>
</tr>
<tr>
<td>Voltage reference for inverter</td>
<td>120 V</td>
</tr>
<tr>
<td>Load</td>
<td>10 kW</td>
</tr>
</tbody>
</table>
A 10 kW three-stage seven-level SST prototype is constructed. The key parameters for the hardware testbed are listed in Table 5-1. The voltage is scaled down and three experiments are carried out: 1) conventional control for DAB without current balance, 2) the conventional droop control for DAB, and 3) the proposed control for DAB.

Figures 5.10 to 5.13 are the experiment results for the conventional control without applying the current balance strategy. The input voltage and current are depicted in Figure 5.10. Three high DC voltages are shown in Figure 5.11 to verify the rectifier stage controller. The voltage balance control strategy (shown in Figure 5.3) is applied to make the three voltages be equal. As shown in Table 5-1, when the leaking inductors of three high frequency transformers are different, the output currents are different (Figure 5.12). Reviewing the equation (5.4), parallel DABs output current values are inversed to their leaking inductors value as only one phase shift is generated (322mA, 358mA, 385mA, RMS value respectively). The inverter output voltage and current are depicted in Figure 5.13 to verify the inverter function.

Figure 5.14 is the result for the DAB control with conventional droop control. Since the input voltage, current, rectifier voltage, inverter output voltage and current are the same as the previous case’s results, they are omitted due to the limited space. The three DABs’ output currents are the same (380mA, 377mA, 375mA, RMS value respectively), while the low DC voltage drops to 95V when the Vmax is set as 100V. Figure 5.15 is the result of the proposed adaptive droop control. Comparing to the Figure 5.14, three DABs’ output currents are same (380mA, 383mA, 384mA, RMS value respectively), and the low DC voltage is maintained as desired value (100V), which verifies the proposed method.
Figure 5.10 Input Voltage and Current.

Figure 5.11 Individual Three High DC Voltage.
Figure 5.12 Three DAB Output Currents and Low DC Voltage without Current Balance.

Figure 5.13 Inverter Output Voltage, Current, High DC and Low DC Voltage.
Figure 5.14 Three DAB Output Currents and Low DC Voltage with Conventional Droop Control.

Figure 5.15 Three DAB Output Currents and Low DC Voltage with Adaptive Droop Control.
5.3 BlackStart and Blackout Control

5.3.1 BlackStart

SST interfaced DC MG equivalent diagram is shown in Figure 5.16. DC MG usually operates in the SST-enabled mode by hierarchical control discussed in chapter 4. Only the system meets abnormal conditions, the DC MG might disconnect from the SST and operates in islanding mode. Thus, there are two issues need to be considered, which the first one is the system blackstart and the other one is blackout. The blackstart for SST with DC MG can be referred to [96], [97].

![Figure 5.16 Equivalent System Diagram.](image)

5.3.2 Blackout

Usually, when SST and DC MG operate independently, if utility fails, the SST will be shut down. For DC MG, it will operate in islanding mode in distributed control which discussed in Chapter 4. While when DC MG connects to SST, blackout procedure will be different. Since DC MG includes DRERS and DESD, which have the ability to generate the power, DC MG might have the ability to support the inverter stage of SST operation even the utility
fails. The blackout process is depicted in Figure 5.17. When the utility fails, the rectifier and DAB stages of SST stop, then the bus voltage will be supported by DC MG. Then two consequences might occur. The first one is the DC MG can support the inverter if the DRERs and DESD has enough power to supply it. The other one is the inverter will be shut down if the DRERs and DESD can’t supply enough power to it. In the same theory as discussed in Chapter 3 and 4, the bus voltage ($V_{ldc}$) is the criterion to select the modes. To coordinate with the distributed control in Chapter 4, the critical voltage value for inverter shutting down is set as 360 V. When the bus voltage is greater than 360 V, the inverter will operate with DC MG support. However, when the bus voltage is less than 360 V, the inverter will be shut down.

\[ \text{Utility fails} \]
\[ \text{Rectifier, DAB stops} \]
\[ \text{bus($V_{ldc}$) voltage detection} \]
\[ \text{Y} \]
\[ \text{DC MG support inverter} \]
\[ \text{N} \]
\[ \text{Inverter stops DC MG in islanding} \]

Figure 5.17 SST Interfaced DC MG System Blackout Flow Chart.
This simulation is to evaluate the system performance for DC MG supporting the inverter operation when the utility fails. As shown in Figure 5.18, when the utility fails at 1.8 s (Figure 5.18 (a)), the SST’s rectifier and DAB stages stop and then the bus voltage is regulated by battery of DC MG. So the battery has to supply more power to support the inverter operation and the DC MG bus voltage drops to 370 V. Correspondingly DC MG
output power increases in Figure 5.18 (b). PV and fuel cell states are no changes and their output power is stable (Figure 5.18 (b)). Furthermore, there is no effect for the inverter’s voltage and current waveforms because the DC MG bus voltage is in the range to generate the AC output voltage (Figure 5.18 (c) and (d)). At 2.3s, there is a step change for the DC load, and then the bus voltage keeps dropping. When the bus voltage is less than 360 V, the inverter will be shut down. Since an average filter is added in the bus voltage detection for inverter, there is a delay for inverter shutting down and it stops at 2.4 s (Figure 5.18 (c)). When the inverter is shut down, the AC load of inverter is disconnected from the system. The equivalent load of DC MG decreases, then the bus voltage gets recovery. This is the reason why the output power of battery and DC MG has a sharp increase and then decreases at 2.3s to 2.4s respectively.

5.4 Plug and Play Function

For the practical DC MG applied to the future house, the plug and play function is very important and necessary. The meaning of plug and play function is when DRER, DESD or the load plugs into or unplugs from the system, the system should recognize it and display its information for the customer or the technician in controller center [55],[98]. Thus, the basic requirements for plug and play function can be described as followings:

1) Communication ports should be embedded into the individual controller for each DESD, DRER and load;

2) Distributed control strategy should be implemented into the individual controller to increase the system reliability;
3) DESD and DRER can plug into the system randomly and start to operate without communication involved;

4) DESD and DRER can unplug from the system randomly and stop without affecting the system operation;

5) Universal protocol should be designed for system center to recognize the DESD and DRER;

6) Human Machine Interface (HMI) should be built for system information display;

7) Data center should be built in system center to save historic data for system optimization.

A smart DC MG is constructed in FREEDM systems Center and a scalable distributed control strategy is adopted (shown in Figure 5.19). It includes: two DRERs (PVs) and two DESDs (batteries) which are used to simulate multiple DRERs and DESDs, local loads and a DC source, where the arrows show the modules power flow directions. Here, a DC source is adopted to simulate the SST low dc output. Two unidirectional DC/DC converters are used for PVs to transfer power generated by PVs into the system, and two bidirectional DC/DC converters are used for batteries to balance the power differences between loads and the power supplied by PVs in islanding mode. The local load and the DC source share a common dc bus. The dc bus voltage can be enabled by the DC source’s output or be regulated by the battery’s DC/DC converters. Correspondingly, when the DC source disconnects from the DC MG system, the DC MG operates in the islanding mode; while the DC source connects to the system, the DC MG enters the DC source-enable mode.
As discussed in earlier chapter, the droop control and the MPPT can fulfill the requirement 2) for both battery and PV modules. For the requirements 3) and 4), the boost converter is selected as the topology for battery and PV module. Assuming the system bus voltage is already set up, thus, the judgment for the DRER and DESD plugging operation is to measure the module’s DC/DC converter output voltage. When the DRER or DESD plugs into the system, the measured output voltage is in the predetermined DC bus voltage range (360V-400V), meaning the module has already plugged into the system, then the module starts to operate automatically with the embedded control algorithm in the local controller. Boost converter output voltage will keep increasing when the module is unplugged into the system. Thus the module’s output voltage can still be used to judge unplug function. If the module’s output voltage is greater than the voltage threshold (450 V), this module will be considered unplug and the module will be shut down.

To achieve the requirement 1) and 5), the communication ports are embedded into the system. It is to emphasize here that the communication port is used for the system to
recognize the batteries and PVs only, so the control algorithm is totally independent from the communication port. Since the batteries and PVs are all controlled by digital signal processor (DSP, TI28335), the serial communication interface (SCI) is adopted for system center to identity the module. A custom-designed communication protocol is developed for the module recognition (shown in Table 5-2). When the module plugs into the system and starts to operate, the communication begins to work and the serial data streams are sent by DSP in SCI every two seconds after the plug function is verified. A character of data with its formatting information is called a frame and is shown in Figure 5.20 [99]. The basic unit of SCI data is called a character and is one to eight bits in length. Each character of data is formatted with a start bit, one or two stop bits, and optional parity and address bits. The SCI data streams include six characters. The first character is defined as the module ID which means the module is either the battery or PV. For example, 00000001 represents PV and 00000002 represents battery, respectively. The second character is defined as the module number in the system. For example, if there are two batteries in the DC MG, then 00000001 represents battery I and 00000002 represents battery II. This number will be issued by the system center since only the system center has the information of the numbers for the battery and PV. Thus, the module’s initial number is zero when it is connected to the system at the first time before it get the second information in the data stream from the system center. The follows characters (from 3 to 6) are the module’s local information: the module output voltage, current, converter terminal voltage and SOC for the battery. When the module disconnects from system, the communication will be stopped after the unplug function is verified. Noted here, this protocol is also can be extended to apply for other
DESDs and DRERs, like fuel cell, supercapacitor, wind and so on; even it’s just verified for battery and PV in this demonstration.

<table>
<thead>
<tr>
<th>start</th>
<th>LSB</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>MSB</th>
<th>Parity</th>
<th>Stop</th>
</tr>
</thead>
</table>

Figure 5.20 Typical SCI Data Frame Format.

Table 5-2 Customer Design Communication Protocol.

<table>
<thead>
<tr>
<th>Number of Data</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Module ID</td>
</tr>
<tr>
<td>2</td>
<td>Module number</td>
</tr>
<tr>
<td>3</td>
<td>Module output voltage</td>
</tr>
<tr>
<td>4</td>
<td>Module output current</td>
</tr>
<tr>
<td>5</td>
<td>Converter terminal voltage</td>
</tr>
<tr>
<td>6</td>
<td>SOC (for battery)</td>
</tr>
</tbody>
</table>

To supervise the operation of the whole system, requirement 7), a system center is constructed and the system architecture is shown in Figure 5.21. Considering the DESD and DRER might be far from the control center, wire communication is unrealistic, thus a wireless communication port is adopted. The communication board (TS7800) [100],[101] is interfaced with the each DSP board for individual module and transforms the SCI signals into WIFI signals, then the WIFI signals are transited to the system center. As a result, the system center of the DC MG collects the whole system information and a database, requirement 6), is built to store all information. On the front-end of system center, Java [102] and JSP [103]
are used to build up the webpage which shows the real time data from each device (Figure 5.22.(b) and (c)) and device’s plug or unplug status. On the back-end of system center, a database is set up by MySQL [104] to save all system history information in the system center. This database can query the TS7800 board for the data based on the customer’s required period and then display the history data on the webpage (Figure 5.22.(d)). Furthermore, these data will automatically be stored into the database in the specified space,
based on the defined space for individual device according to their IDs. In addition, since each device has its own ID in the system center, when the device re-plugged into the system, it can be recognized by the system center automatically then its data can be saved into the corresponding space. Furthermore, the dynamic arrows are added on the webpage to show the module power flow direction and the battery arrow direction is bidirectional since it operates bidirectional. The webpage of system center is shown as Figure 5.22.

Figure 5.22 HMI and Data center.
The system’s testbed configuration is shown in Figure 5.23 where a 380V DC MG prototype is constructed. It consists of two PV panel, two batteries and one local resistor load bank, which share a common dc bus. The dc bus voltage can be regulated by batteries in the islanding. A DC power supply is adopted to supply a constant 380V dc bus in DC source-enable mode. Thus the system can operate in islanding, DC source-enable and transient modes. The batteries droop slopes are set the same values so they can share power equally.

Figure 5.23 Hardware Testbed.

Case I: PV I Unplug and Plug in Islanding Mode

Initially, two PVs and two battery modules are connected to the system in islanding mode; the batteries are in the charging mode since the power generated by PVs is greater than the load needed and the bus voltage is a little bit greater than 380V. When PV I is unplugged from the system, then the batteries have to output power to makeup the PV I’s previous
output power, so the batteries are switched from charging mode to discharging mode automatically. Since the batteries’ output power is positive, the bus voltage decreases and is less than 380V. When PV I is plugged into the system and generating power into the system, the batteries go back to charging mode and the bus voltage increases to the previous value before PV I is unplugged. When PV I unplugs and plugs, there is no side effect to the operation of PV II. PV II is always in MPPT mode to supply the maximum power to the system. Figure 5.24.(a) shows the output currents of batteries and bus voltage. PV panels’ voltages and currents are depicted in Figure 5.24.(b).
144

a. Batteries output currents and bus voltage.

b. PVs output currents and voltages.

Figure 5.24 PV I Unplug and Plug in Islanding Mode Waveform.
Case II: Battery II Unplug and Plug in Islanding Mode

The initial status of the system is exactly the same as case I, and then battery module II is unplugged from the system, finally is plugged back into the system. Figure 5.25.(a) and (b) show batteries, PV panels output voltages, currents and bus voltage. Before unplugging, both batteries are in the charging mode. After battery II is unplugged from the system, then the battery I needs to absorb extra power to keep the system power balance. So the battery I’s charging current and the DC bus voltage increase (current value steps more negative). When the battery II is re-plugged back into the system, the DC bus voltage has a small drop because battery module II is on the soft-start status, then the bus voltage will be recovered to the initial value before battery II unplugged from the system. For the two PV modules, they are always in MPPT control modes, so there are no obvious change for PVs output currents and voltages even when battery II is plugged into and unplugged from the system.
a. Batteries output currents and bus voltage.

b. PVs output currents and voltages.

Figure 5.25 Battery II Unplug and Plug in Islanding Mode Waveform.
Case III: Islanding Mode to DC Source-enable Mode

Experimental results of the transition from islanding mode to DC source-enable mode are shown in Figure 5.26.(a) and (b). Initially two PVs and two batteries modules are all connected to the system and the system is in the islanding mode. The DC bus voltage is regulated by the two batteries modules. Based on the Figure 5.26.(b), the total power of two PV modules is equals to the load needed, so the bus voltage equals 380V. Since the batteries modules are in droop control and the critical value is set to 380V, the average values of batteries output currents are almost zero, which means batteries don’t generate or absorb power. When the system switches into the DC-source enable mode, there are no obvious changes on the DC bus voltage and the battery output currents because the output voltage of DC source is 380V. The PV modules are always in MPPT control. Since the irradiation is not strong, the PVs’ output voltages keep increasing and the currents have no big changes.
a. Batteries output currents and bus voltage.

b. PVs output currents and voltages.

Figure 5.26 Islanding Mode to DC Source-enable Mode Waveform.
Case IV: DC Source-enable Mode to Islanding Mode

Figure 5.27.(a) and (b) show the experimental results of the system transited from the DC source-enable mode to islanding mode. When system is in the DC source-enable mode, the DC bus voltage is regulated by the DC source. Since the output voltage of DC source is 380V, which equals to the batteries droop control output voltages without load, the batteries are almost in stand-by status (the average values of output current are zero). When the DC source is disconnected from the DC bus, the system goes into the islanding mode and the batteries modules are responsible to support the bus voltage. Then the batteries have to generate power into the system because the power generated by PVs is less than the load needs. As analysis before, the batteries are in droop control, so the DC bus voltage in islanding mode is smaller than 380V. For PV modules, they are always in MPPT control in either mode and there are no obvious changes for their voltages and currents.
a. Batteries output currents and bus voltage.

b. PVs output currents and voltages.

Figure 5.27 DC Source-enable Mode to Islanding Mode Waveform.
5.5 Summary

In this chapter, some practical issues for SST interfaced DC MG are analyzed, including the power balance issue for SST, blackout control strategy for the system, and a plug and play DC MG construction, demonstration and function implementation.

Initially, the reason for power unbalance issue of SST is analyzed and an adaptive droop control method is proposed. The simulation and experimental results are present to verify it. Secondary, the control strategy for blackout procedure is proposed and the simulation results valid it. At the end, a plug and play DC MG with multiple DRERs and DESDs is built. The distributed power management strategy is applied to the system. Furthermore, the wireless communication is added in the system. In addition, a universal communication protocol is proposed and the plug and play function is achieved. A computer is simulated the control center and all the system data is saved in a database for system display, monitoring and history data quest, which is built with MYSQL.
Chapter 6 Conclusion and Future Work

6.1 Conclusion

In this dissertation, some power and energy management strategies for SST interfaced DC MG are proposed. The first contribution is the SST is firstly adopted to interface the DC MG with the distribution system. Furthermore, a distributed energy management strategy and a hierarchical power and energy management strategy are proposed and verified in simulation and experiments. Then unbalance power issue for SST is analyzed and a distributed control strategy is present to solve it. A practical DC MG with plug and play function is investigated and demonstrated.

In chapter II, the DHB topology, which is applied for DC/DC converter in the DC MG, is presented. Several corresponding factors for DHB are analyzed: 1) the large signal average model for DHB is achieved; 2) ZVS procedure and boundary for DHB is analyzed; 3) the control algorithm for DHB is investigated; 4) the switching model for single DHB is implemented in Matlab/Simulink; 5) the simulation and experimental results verify the ZVS procedure and the control algorithm for single DHB.

In chapter III, a novel distributed energy management strategy is proposed for SST interfaced DC MG, which includes DRERs (fuel cell, PV) and DESD (battery). Furthermore, SST is firstly adopted to enable the DC MG to interface AC system and the distribution system. The proposed distributed control algorithms for SST, fuel cell, PV and battery, are presented based on their individual characteristics. In this energy management strategy, bidirectional power flow for SST is verified. In addition, since SOC of battery is monitored, battery can intelligently and automatically switch its control algorithm based on its SOC and
the system information without the communication ports involved. Then the system reliability increases. To verify the proposed energy management strategy, the corresponding simulation model is constructed and the simulation results valid it.

In chapter IV, a hierarchical power and energy management for DC MG is proposed which includes primary control, secondary control and tertiary control. The primary control is based on the distributed control level to guarantee the system power balance without communication, which also increases the system stability and verify the IPM function. Furthermore, some extreme cases, such as load shedding and PV shedding, are considered and verified in the primary control. The secondary control is adopted to eliminate the voltage difference between SST low DC output and DC MG bus voltage when DC MG switches from islanding mode to SST-enabled mode. The seamless switch procedure is achieved. Furthermore, the battery SOC management and PCC power flow control are both involved into the tertiary control. If the battery SOC is in the defined SOC range, the tertiary control will control the PCC power flow. However, if the battery SOC is out of the operation range, the tertiary control will manage the battery SOC to charge or discharge the battery instead of PCC power flow control. Two tertiary control methods are presented. One is to change SST DC output voltage and the other one is to control battery droop curve. The advantages and disadvantages for these two methods are analyzed. The simulation and experimental results verify it.

In chapter V, some practical issues for SST interfaced DC MG are analyzed, including the power balance issue for SST, blackout control strategy for the system, plug and play DC MG demonstration and verification. Initially, the reason for power unbalance issue of SST is
analyzed and an adaptive droop control method is proposed. The simulation and experimental results are present to verify it. Secondary, the control strategy for blackout process is proposed and the simulation results valid it. At the end, a plug and play DC MG, which consists multiple DRERs and DESDs, is built. The distributed power management strategy is applied to the system. Furthermore, the wireless communication port is embedded into the system. In addition, a universal communication protocol is proposed and the plug and play function is achieved. A computer is adopted to simulate the system center and all the system data is saved in a database, which is built with MYSQL.

6.2 Future Work

There are several major future work can be investigated. The first one is developing a more comprehensive hierarchical control for DC MG. Since the communication ports are embedded, more IEM function can implement in the tertiary control layer, such as economic analysis, marketing and optimization.

The second one is to develop the co-operative power control between AC MG and DC MG. When DRERs or DESDs constitutes the AC MG instead of the RL load, how to control the AC and DC MG power flow coordinately might be an interesting topic to investigate.

The third one is to develop an autonomous control system for the FREEDM systems without communication. Since FREEDM systems (Figure 1.9) includes multiple SSTs. It brings more challenges for power and energy management strategy. The control strategy should not only guarantee single SST with MG operate in islanding mode and grid-connection mode, but make multiple SSTs operate in both modes, even in transient mode without communication.
The forth one is the DC MG stability analysis, which is another critical issue that must be addressed. The system might become unstable if it is not designed correctly, especially some converters and load plugs and unplugs. Also the interaction between the converters can result in an under damped or unstable system in the small signal sense [105], [106]. The issue of small signal stability was proposed by Middlebrook in 1976 [107]. Initially, it was used to invest the interaction between a converter and its input filter. The key point of the solution is to ensure the system’s stability by guarantee that the value of the filter’s output impedance \( Z_o \) should be much smaller than the input impedance of the converter \( Z_i \) over the entire frequency range, i.e. \( |Z_o| \ll |Z_i| \). Lots of researches are carried out to define the stable area for DC distributed system [108]-[114]. However, in the DC MG, the battery’s power is bidirectional as the energy buffer, which means the battery can be source or the load under different conditions. This might change the load and source impedance ratio, which might cause the system unstable. Thus, much work is worth investigating in this field.
REFERENCES


[56] “http://freedm.ncsu.edu.”


