ABSTRACT

WU, HONGYU. Fault Diagnosis Testbed for Plug and Play Photovoltaic System. (Under the direction of Dr. David Lubkeman.)

In recent years, the cost of energy, concerns about the environmental impacts of energy production, renewable portfolio standards requirements, and other economic factors including incentives have combined to increase consumer's interest in residential photovoltaic (PV) system. However, even though PV system hardware costs have been substantially reduced, the installed cost of a residential system is still relatively high due to "soft costs" such as customer acquisition, permitting, installation, interconnection fees, etc. A "Plug and Play" PV system approach has been suggested as a means of lowering cost, whereas the system is designed as a standardized appliance that can be installed by a residential customer. A true "Plug and Play" solution needs a number of advanced residential safety and utility grid-friendly functions, among which fault diagnosis is the backbone of these advanced features. In this thesis, a Power-Hardware-in-the-Loop (PHIL) testbed has been developed to conduct fault analysis in residential PV system. A series of tests have been conducted on the proposed system to analyze and validate the findings in some existing studies. The study has also been extended to provide a systematic study on the current protection challenges for a PV system. The first part of the thesis is devoted to implementation of an RTDS testbed for prospective PHIL tests. The second part mainly focuses on developing the fault diagnosis function of the Plug and Play PV system. The developed RSCAD platform to generate simulation plots can be modified and used for PHIL testing as well.

Fault Diagnosis Testbed for Plug and Play Photovoltaic System

by
Hongyu Wu

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APPROVED BY:

_____	_____
Dr. David Lubkeman Committee Chair	Dr. Iqbal Husain
_____	
Dr. Ning Lu	

DEDICATION

To my family and dear friends who are the biggest support of my life.

To my teachers who nourished me with knowledge throughout my entire student career.

To all the people who make a difference in my life.

BIOGRAPHY

Hongyu Wu comes from Hefei in China. He received a Bachelor's degree in Electrical Engineering and Automation from North China Electric Power University, Beijing, China in 2012. He joined NC State University since August, 2012 for his Master of Science degree in Electrical Engineering. His research interests include Distribution Automation, Real Time Power System Simulation and Photovoltaic System.

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Chapter I: Introduction

1.1 Growth of Residential PV Market

It is commonly acknowledged that high penetration and large-scale utility adoption of photovoltaics (PV), with its increasingly more cost-effective and more reliable performance, is a critical element of the future of renewable energy. In the US, solar is now the second largest source of new electricity generating capacity, exceeded only by natural gas. And during the past five years, the residential solar market in the US has been growing steadily with increasing end-market demand and declining system prices (See Fig 1.1 and Fig 1.2). The government believes that the advanced power electronics like PV inverters will make high penetrations of PV at residential level not just acceptable, but desirable. According to Shayle Kann, Senior Vice President at GTM Research, "Perhaps more important than the numbers, 2013 offered the US solar market the first real glimpse of its path toward mainstream status. The combination of rapid customer adoption, grassroots support for solar, improved financing terms and public market successes displayed clear gains for solar in the eyes of both the general population and the investment community." [7]

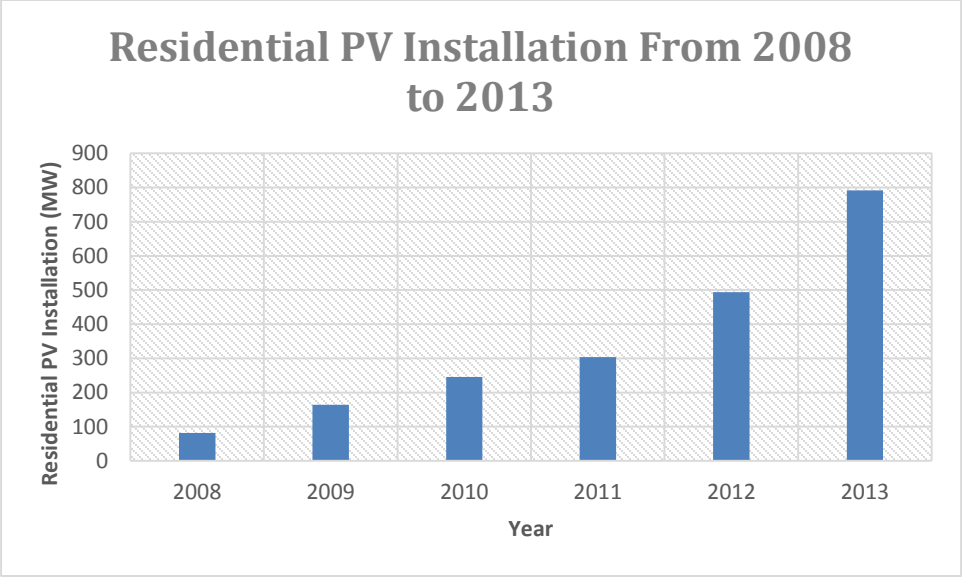

Fig 1.1 Residential PV Installation Trend from 2008 to 2014 (Source: GTM Research/SEIA U.S. Solar Market Insight: 2013 Year-in-Review)

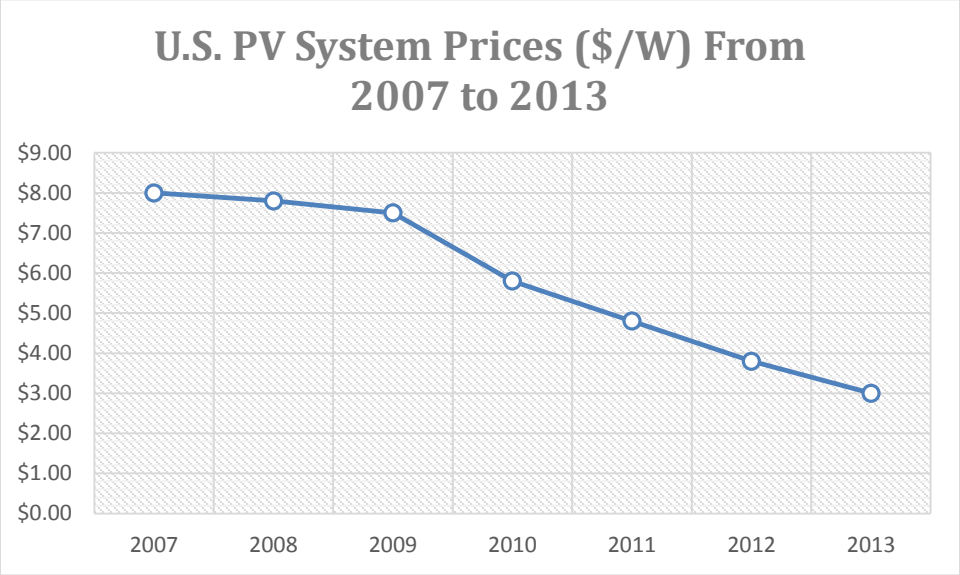

Fig 1.2 U.S. Weighted Average Systems Price ($/W) from 2007 to 2013 (Source: GTM Research/SEIA U.S. Solar Market Insight: 2013 Year-in-Review)

The main contributor of PV technology improvement—Rooftop PV industry (See Fig 1.3) has grown rapidly since the late 1990s, due in large part to gradually declining system prices, improved equipment, increased consumer concerns regarding climate change, and a proliferation of government and utility incentive programs. Until recent years the single largest obstacle for residential PV remains system cost; it will likely be more than a decade before PV can directly compete with traditional grid electricity without subsidies or incentives [1].

Fig 1.3 Residential Rooftop Systems (Source: Energy.gov)

Rooftop PV systems are often categorized into two discrete market segments—residential and commercial—based on the type of building on which they are installed. Generally, these markets are defined by electricity rates, PV system sizes, and rooftop slopes. In the United States, residential PV systems are generally 2–10 $kW_{P\ DC}$ and installed on sloped roofs, while commercial systems may be between 10 $kW_{P\ DC}$ and multi-megawatts and are most often installed on flat or low-slope roofs. In this thesis we will focus on residential rooftop PV system. A typical residential rooftop PV system consists of a linked collection of solar panels, PV mounting systems, solar trackers, solar micro inverters, monitoring and metering system and a capacitor charge controller with maximum power point tracking capability.

1.2 Need for Plug and Play

According to a recent report by US DOE SunShot Initiative, the last five year decline in installed system prices is mainly attributed to decreasing module prices, which fell by $2.6/W from 2008 through 2012. This represents roughly 80% of the drop in total PV system prices for ≤10 kW systems over the same period. However, over the longer-term, installed system prices should be expected to fall as a result of reductions in non-module costs. The non-module costs include items as inverters, mounting hardware, labor, permitting and fees, customer acquisition, overhead, taxes, and installer profit. It is predicted that new technology development in the near future will help greatly reduce soft-costs even though the hardware costs might remain about the same.

Bringing down the soft-costs of residential PV system in the next five years is the key to accomplish the 2020 SunShot Initiative goal (The SunShot Initiative aims to reduce the total installed cost of solar energy systems to $0.06 per kilowatt-hour (kWh) by 2020). For example, non-module costs for ≤10 kW systems declined by approximately $2.5/W from 1998 to 2012, constituting 38% of the reduction in total installed system prices over that period. In recent years, however, non-module costs have remained relatively flat while module prices fell rapidly, and as a result, non-module costs have grown significantly as a share of total system costs. From DOE's residential PV soft-cost reduction roadmap (See Fig 1.4), it can be seen clearly that a new approach will be needed for the next generation residential PV system development to break through the soft-costs reduction barrier.

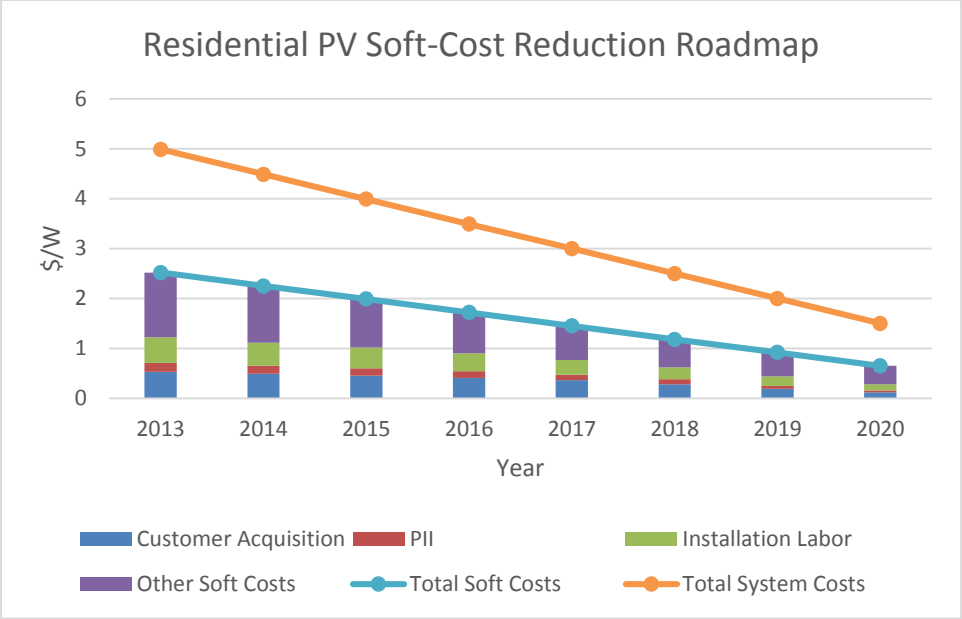

Fig 1.4 Residential PV Soft-Cost Reduction Roadmap (Source: Energy.gov)

At the heart of this new approach is the Plug and Play (PnP) concept, which has been utilized very successfully in the computer and automotive industries. DOE believes that Plug and Play technologies can be applied to the PV industry to reduce costs and simplify installations. It should be noticed that a PnP is likely to be more expensive from the hardware side, but much less expensive on the soft cost side, which serves for the ultimate target of SunShot Initiative as well as the need for developing world-wide smart grids in the long term.

By definition, a Plug and Play PV system is a commercial, off-the-shelf system that is fully inclusive with little need for individual customization. Any homeowner/consumer can buy and install (or have a contractor install) the system without the need for special training or specialized tools. The homeowner plugs the system into a "PV-ready" circuit and an automatic PV discovery process initiates communication between the system and the utility. The system and the interface to the grid are automatically configured for optimal operation. This scenario is depicted in Figure 1.5, in which a bi-directional flow of information between the home and utility via a smart grid is illustrated.

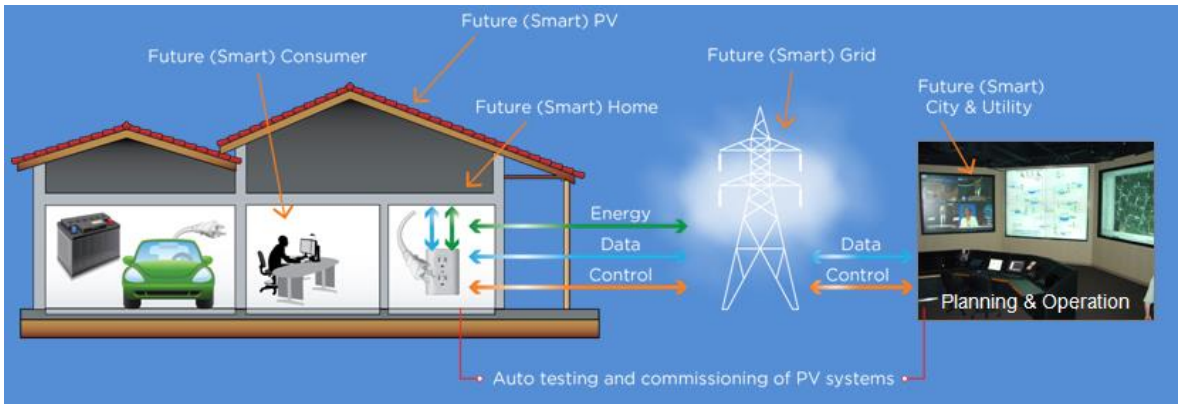

Fig 1.5 Conceptual Diagram of Future PnP System (Source: DE-EE0006036)

A complete Plug and Play PV system is expected to have the following characteristics to enable easy installation and same day commissioning of the entire system:

Table 1.1 Characteristics of PnP PV System (Source: DE-EE0006036)

Simple Installation	The PV system must be simple enough to install safely in ten man-hours of labor or less, with no special expertise or training, requiring few or no special tools.
Automatic Electrical Permitting and Inspection	To replace the need for electrical permits and inspections, one listing of the entire PnP system must be developed along with a standard PV plug at the utility meter as well as smart PV-ready circuit breakers. The PV system must have inherent electrical safety guarantees so that the electrical installation is analogous to plugging a television set into a wall outlet without having to acquire an electrical permit. Also upon connection, the system should be capable of performing self-diagnostics. The PV system should be able to automatically communicate all pertinent information (including potentially self-diagnostic results) to the electrical code officials, in lieu of inspection, to ensure that required electrical codes and standards are met.

Table 1.1 Continued

Automatic Structural Permitting and Inspection	Similarly, to replace the need for structural permits and inspections, one listing of the entire Plug and Play PV system must be developed along with the use of lightweight PV materials and innovative mounting mechanisms. Collaboration between the roofing and solar industries are critical in this effort. The structural technologies should have modularity and flexibility to enable various design options. The PV system structure should comply with all the building codes and be able to automatically communicate all the pertinent information (including potentially self-diagnostic results) to building code officials, in lieu of inspection, to ensure that the required building codes and standards are met.
Automatic Grid Interconnection	To replace the need for grid interconnection agreement, a Plug and Play PV system will most likely need to, upon connection with the grid, automatically communicate to the utility all the pertinent information required to ensure that it does not interfere with the normal operation of the grid. The PV system will also need smart grid capabilities (such as reactive power and voltage regulation) to ensure normal grid operation.
Costs	The Plug and Play PV system must meet the SunShot goal of $1.5/W installed cost for the residential market.
System Design	To ensure broad market acceptance by homeowners, the Plug and Play PV system must be designed with customer needs in mind.

1.3 Literature Review

PV power generating technology will not achieve its full potential until it ceases to be regarded by local permitting authorities and utilities as a problem or potential hazard, but instead as a safe and reliable resource that can be monitored and dispatched to contribute to the efficiency and stability of the grid. In past years there has been a large amount of work published on the study of PV system. Listed below are studies highlighted with respect to the concern of PnP residential PV system.

- PV-ready electrical circuit simulation

PSCAD models can be found and used for system-level simulation to study the impact of PV penetration under variable atmospheric conditions [5]; On the DC side of the PV system, SPICE is considered as the simulation environment because of its convenience of modelling PV modules [12]; However, both PSCAD and SPICE model need to approximate the inverter model and MPPT control as a passive component. Several MATLAB/Simulink-based simulations do utilize the complete inverter model, but the characteristics of MATLAB (non-real-time, pure software environment) leads to a limit area of application [14-15].

- System integration, planning and operation

  In general, increased PV penetration can have a either beneficial or detrimental impact on power system operation, depending on the level of penetration as well as the pertinent control scheme. To provide an assessment on voltage profiles in residential neighborhoods in the presence of PV systems, the results of PSCAD simulation based on a distribution system case study indicate that, the PV penetration level should not adversely impact the voltage profile when the distributed PV resources do not exceed 2.5 kW per household on average [4-5]. Investigations have been made on the utilization of Distributed Energy Storage (DES) to alleviate dynamic impacts of PV-DG units on power distribution system using models developed in PSCAD. Simulation results show that through proper control algorithms, DES has the potential for improving dynamic performance of distribution feeders with PV-DGs proliferations [6].

- Solar inverter testing

  Besides traditional field tests for standard commissioning, modern testing has been extended to more complicated test scenarios at the residential-level such as arcing fault [20]. It is also possible to combine a real-time simulator with hardware environment to perform fundamental testing for traditional grid-connected PV inverters [8-9]. However, the studies conducted by utilizing real-time simulation have not reached as far as testing smart-inverter functionality in real-time simulated

testbed and even more importantly, the same approach to studying micro inverter functionality seems to be nonexistent.

- Safety considerations and fault diagnosis

  Either safety issues or fault diagnostics functions are directly related to the pre-fault and fault study in PV array. Areas of study can vary based on the needs of research institutes but generally fall into two categories: 1) developing arc fault or high impedance fault degradation models and studying the resulting fault current waveform transmission in PV system for detection [13]. 2) steady state analysis for different types of faults in PV system based on SPICE Model and discussion on potential challenges for the protection system. [16]

1.4 Content of Thesis

This thesis describes validated distribution network models in RSCAD platforms. It also introduces a general approach of Power-Hardware-in-the-Loop testing to perform studies on fault diagnostics function in the proposed PnP system. This study should serve as preliminary simulation development before actual Power-Hardware-in-the-Loop test can be conducted in the future. Due to the PV system's unique output characteristics, this thesis focuses on the modeling, development, and analysis of various faults in a residential grid-connected PV system. The main contributions of the thesis are:

- Different from previous PV modelling works that are done in SPICE. A real-time simulation platform has been developed that can be used to predict the actual performance of residential PV system with different scales and different array configurations.
- The same simulation platform is modified with simplified inverter model to simulate typical PV faults, including ground faults, line-line faults, mismatch faults and others.
- The electrical behavior of PV system during DC arc faults and low voltage AC arc faults are simulated and studied. Based on the simulation results, the feasibility of developing fault detection technologies embedded in smart circuit breakers is evaluated.

- Residential-wise protection coordination issues have been investigated based on the modified RTDS testbed. The resulting system response from islanding or anti-islanding scheme is then analyzed and evaluated.
- Power-Hardware-in-the-Loop testing procedure for solar micro inverter has been introduced with the developed RTDS interface so that the PnP grid-friendly functions proposed in the previous sections can be well tested in a non-field environment.
- Advanced fault diagnostics topics like ground fault blind spot detection, fuse sizing and impact of MPPT control on fault evolution has been analyzed, which provides a guideline to be taken into consideration when designing protection system for residential PV system.

Acronyms are heavily used in this thesis. All of them can be found in Appendix D.

Chapter II: Solar Inverter Testing Using RTDS Hardware-in-the-Loop Environment

This chapter introduces a general approach to conduct solar inverter tests using RTDS Power-Hardware-in-the-Loop environment. While the solar micro inverter bears a similarity to traditional string inverter, the high reliability and easy installation make it stand out to be an ideal PnP solution for residential PV system. And for the DOE PnP project, the focus is shifting to multi-port building blocks which is a hybrid configuration between a central inverter and micro inverter.

In this chapter, a review of existing testing standards for PV inverter has been conducted. In order to better study the PnP function of solar inverters, different test scenarios are then introduced in combination with Power-Hardware-in-the-Loop approach. Finally, details of PHIL interfaces in RTDS are given to provide a complete validated platform for the PnP function testing in this thesis.

2.1 Plug and Play Solar Micro Inverter

The technical integration of solar energy, often performed by power electronics, will have an increasingly more profound impact on the grid stability, reliability and availability as the penetration of PV increases. The PnP residential PV system is of no exception. The core of the system is a solar micro inverter (See Fig 2.1), a smart DC to AC interface module with grid-friendly functions.

Fig 2.1 SOLARBRIDGE Micro Inverter

The main advantage of micro inverters over conventional central inverters is that since each micro inverter is connected to a single solar panel instead of multiple panels, the output of the entire array will not be disproportionately reduced due to small amounts of shading, debris or snow lines on any one solar panel, or even a complete panel failure. When faults occur, they are identifiable to a single point, as opposed to an entire string. This not only makes fault isolation easier, but unmasks minor problems that might not otherwise become visible – a single underperforming panel may not affect a long string's output enough to be noticed [3]. Another advantage is the simplicity to design and stock, as there is normally only a single model of inverter that can be used with any size array and a wide variety of panels [2].

Conventional two-stage solar micro inverter consists of an isolated DC-DC converter and a grid-tied DC-AC inverter. The pre-stage DC-DC converter releases the maximum solar energy from a PV panel by MPPT control and provides a high-voltage DC bus for the post-stage AC output voltage and connects with the AC-grid system [15]. Modern micro inverters are typically rated between 190W and 220 W. Because it is operated at this lower power point compared with central inverter, many design issues inherent to larger designs go away; the need for a large transformer is generally eliminated, large electrolytic capacitors can be replaced by more reliable thin-film capacitors, and cooling loads are reduced so no fans are needed [2].

The main disadvantage of the micro inverter concept has, until recently, been cost. Because each panel has to duplicate much of the complexity of a string inverter, costs are marginally greater. As of October 2010, a central inverter costs approximately $0.40 per watt, whereas a micro inverter costs approximately $0.52 per watt. However, with steadily decreasing prices, the introduction of dual micro inverters that accept DC input from two solar panels, and the advent of wider model selections to match PV module output more closely, cost is less of an obstacle so micro inverters may now spread more widely [3]. A summary of comparison between micro inverter and central-inverter is given in Table 2.1.

Table 2.1 Comparison between Micro inverter and Central-inverter

	Micro Inverter	**Central Inverter**
Power Output Level	Low	High
Solar Panel Connection	Typically one inverter to one panel in parallel connection	Typically one inverter to multiple panels in string connection
Mean Time Between Failures	Low	High
Heat Loads	Low	High
Fault Detection and Isolation	Easy	Hard
Overall Array Reliability	High	Low
Product Warranty	Typically 15-25 years	Typically 5-10 years
Average Cost	High	Low

In addition to the advantages due to inherent topology, the Plug and Play function of micro inverter also makes it one step ahead compared with conventional string inverter. The details of this function vary among different manufacturers, but generally they include simple installation and inspection process, and Internet addressability for user to monitor and detect faulty or under achieving panels.

2.2 PV System Commissioning Test

As mentioned in Chapter 1, a successful PnP system should feature simple installation as well as automatic electrical permitting and inspection. This leads to our focus on the most basic test for PV system – commissioning test.

Commissioning is a way to formalize quality control of installed PV systems. The process ensures that systems are safe and high performing. Successful commissioning leads to satisfied system owners and system operators. Seen in this light, having a rigorous commissioning

process is essential to the growth of the PV industry and to the overarching goal of installing more renewable energy systems. At the most basic level, commissioning ensures that the owner's requirements have been met. Most of the PV system commissioning will occur after installation is complete and before project closeout. It should include the following elements [11]:

- Verify that the installation is complete.
- Verify that the installation is safe.
- Verify that the installation is aesthetically acceptable.
- Verify that all components of the installation are robust and permanent.
- Document as-built conditions.
- Verify system performance.
- Verify proper system operation.
- Establish performance benchmarks.
- Complete any required acceptance documentation.
- Train the system owner on basic system operation.

PV inverters are subject to multiple safety and electromagnetic compatibility regulations. The same regulatory standards apply to micro inverters. Since PV inverters are generally grid-tied, strict guidelines have been established to ensure the presence of a multitude of grid-tied inverters do not cause disruptions on the public utility grid. Typical examples of these regulatory standards are listed in Table 2.2. For commissioning and site tests, the PV system installation shall be in compliance with UL 1741, except where modified or additional safety requirements are identified for the smart inverters. The equipment interconnecting capability shall pass IEEE 1547.1 commissioning tests and utility-specific commissioning tests if inverter is not tested to UL1741. (IEEE 1547.1 has been incorporated into UL1741 for product pre-certification.)

Table 2.2 Regulatory Standards for PV Inverter Testing

Standard	Description
IEEE 1547 / IEEE 1547.1	Standard for Conformance Test Procedures for Equipment Interconnecting Distributed Resources with Electric Power Systems
UL 1741	Standard for Inverters, Converters, Controllers and Interconnection System Equipment for Use With Distributed Energy Resources
IEC 61000-3-15	Electromagnetic immunity and emission requirements for dispersed generation in Low Voltage networks
VDE 0126-1-1 and IEC 6210	Standards for safety mechanisms needed for grid-tied solar inverters in Low Voltage networks

2.3 PV Inverter Grid-Friendly Functionality Test

Another feature of PnP inverters that differentiate them from traditional inverters is the grid-friendly functionality. Currently IEEE 1547 does not allow PV inverters to provide voltage control. However over the years many efforts have been put on filing documents on Distributed Energy Resources (DER) capabilities to upgrade the standard so that the inverters would be easier to integrate during high penetration conditions. The overall summary of existing documents can be found in Appendix A. Some conclusions we have derived regarding 'grid-friendly' smart inverter functionality are listed below in Table 2.3:

Table 2.3 Overview of Grid-Friendly Smart Inverter Functionality

1	Support anti-islanding to trip off under extended anomalous conditions
2	Provide ride-through of low/high voltage excursions beyond normal limits
3	Provide ride-through of low/high frequency excursions beyond normal limits

Table 2.3 Continued

4	Provide volt/var control through dynamic reactive power injection through autonomous responses to local voltage measurements
5	Counteract frequency excursions beyond normal limits by decreasing or increasing real power
6	Counteract voltage excursions beyond normal limits by providing dynamic current support
7	Reconnect randomly within a preset time window after grid power is restored
8	Limit maximum real power output at the PCC to a preset value
9	Modify real power output autonomously in response to local voltage variations
10	Provide reactive power by a fixed power factor
11	Set actual real power output at the PCC
12	Schedule actual or maximum real power output at specific times

The grid-friendly functionality of PV inverter is developing all the time and varies from country to country, manufacturer to manufacturer. But conceptually, it is commonly acknowledged that the grid-friendly PV inverter should serve as a controllable source for providing both active and reactive power while enhancing grid stability. Today testing grid-friendly functionality of micro inverter is considered to be optional in comparison to commissioning test, but can expect to be mandatory in the future with prospective growing PV penetration.

2.4 Overview of PnP Inverter Test Scenarios

In this thesis we divide the PnP inverter testing into two parts: commissioning test and grid-friendly function test, and seek to develop four different test scenarios with increasing scale to cover the whole PnP function of micro inverter.

2.4.1 Residential Household Commissioning Test

The first test is residential household commissioning test (See Fig 2.2). Details of testing can be found in Section 3.1. At this level DC arcing fault or low impedance faults in PV arrays are likely to be observed. Either field testing or hardware-in-the-loop testing can be utilized.

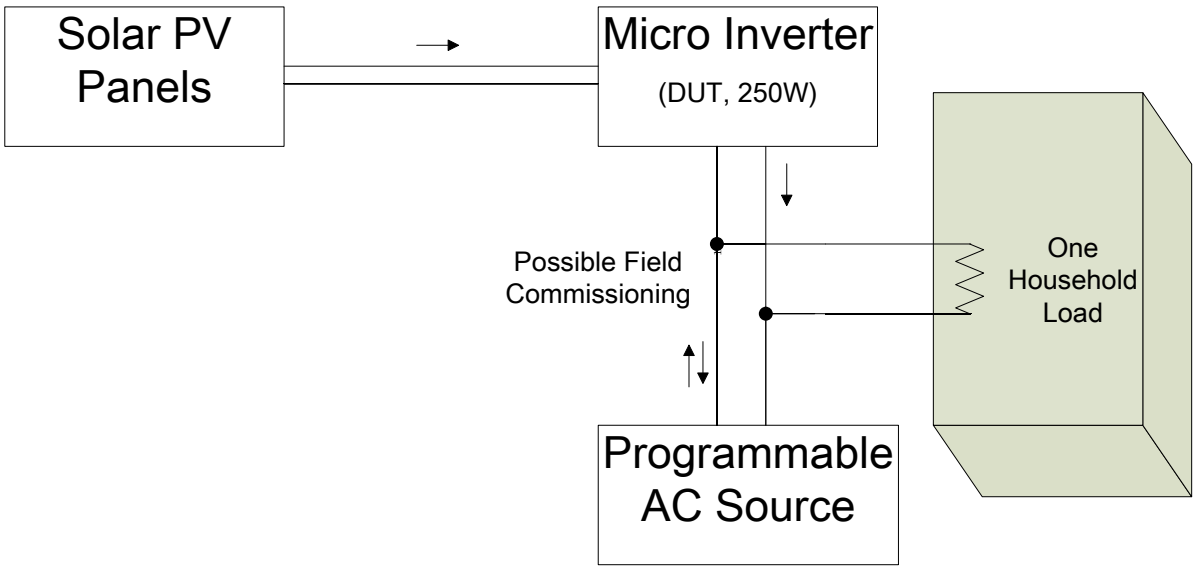

Fig 2.2 Schematic of Household-Wise Inverter Commissioning Test

2.4.2 Customer Distribution Transformer Level Grid-friendly Function Test

The second test is customer distribution transformer level grid-friendly function test. Fault diagnosis functions of micro inverter should be tested at this level. Some other grid-friendly functions of interest include:

1) Modify real power output autonomously in response to local voltage variation,
2) Set actual real power output at the PCC,
3) Counteract voltage excursions beyond normal limits by providing dynamic current support,
4) Schedule actual or maximum real power output at specific times.

The schematic for this test is shown in Fig 2.3.

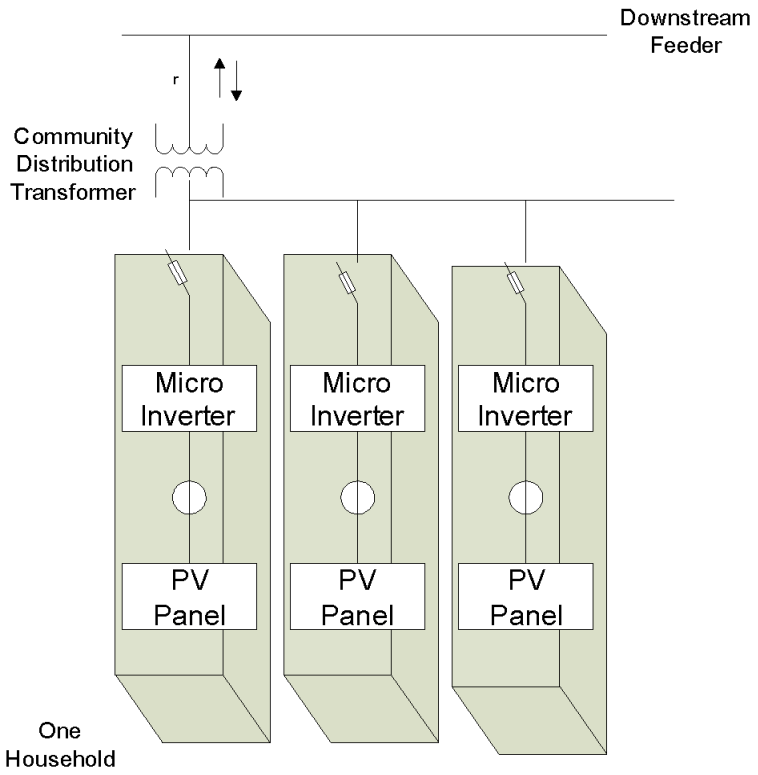

Fig 2.3 Schematic of Customer Distribution Transformer Level Grid-Friendly Function Test

2.4.3 Type I Distribution System Wide Grid-Friendly Function Test (Feeder to PV Systems Impact)

The third test is Type I distribution system wide grid-friendly function test with focus on feeder to PV systems impact. Faults at this level are likely to create low-voltage sags and cause breaker tripping that disrupts inverter operations. Interconnection functions of micro inverters including low voltage/frequency ride through and islanding schemes are most commonly tested at this level. Some of the functions to our interest are:

1) Support anti-islanding to trip off under extended anomalous conditions,
2) Provide ride-through of low/high voltage excursions beyond normal limits,
3) Provide ride-through of low/high frequency excursions beyond normal limits,
4) Reconnect randomly within a preset time window after grid power is restored.

The schematic of test is shown in Fig 2.4.

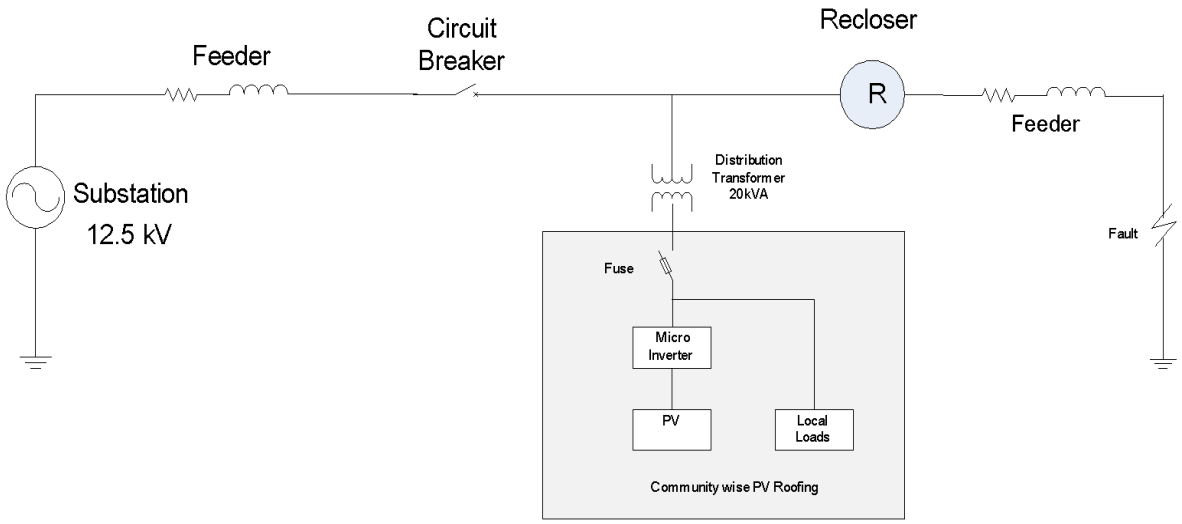

Fig 2.4 Schematic of Type I Distribution System Wide Grid-Friendly Function Test

2.4.4 Type II Distribution System Wide Grid-Friendly Function Test (PV Systems to Feeder Impact)

The last test is Type II distribution system wide grid-friendly function test with focus on PV systems to feeder impact. This test should serve as a verification or complimentary study for PV penetration case study. The schematic of test is shown in Fig 2.5 and can be utilized to verify functions such as:

1) Counteract frequency excursions beyond normal limits by decreasing or increasing real power,
2) Provide volt/var control through dynamic reactive power injection through autonomous responses to local voltage measurements,
3) Counteract voltage excursions beyond normal limits by providing dynamic current support,

4) Limit maximum real power output at the Point of Common Coupling (PCC) to a preset value,
5) Provide reactive power by a fixed power factor,
6) Set actual real power output at the PCC,
7) Schedule actual or maximum real power output at specific times.

The schematic of test is shown in Fig 2.5.

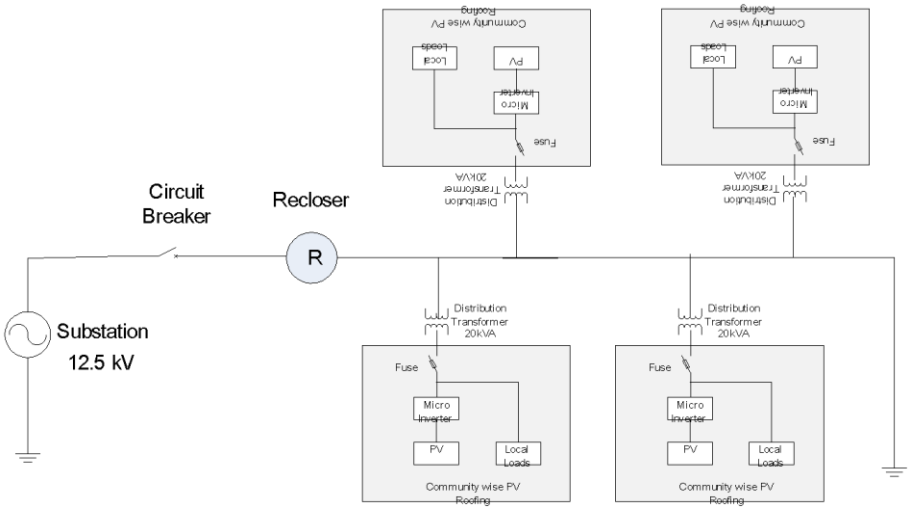

Fig 2.5 Schematic of Type II Distribution System Wide Grid-Friendly Function Test

2.5 Power-Hardware-in-the-Loop

In comparison to conventional field test, in which the actual hardware of the system is built, the approach of combining simulation with hardware experimentation known as hardware-in-the-loop (HIL) has come into sight and gained world-wide recognition these days. HIL approach is being intensively studied for many reasons, but mainly because of the economic concern of large-scale hardware implementation and the lack of accuracy for pure software simulation. Besides, the testing and validation of individual components will no longer be

sufficient on its own. For the purpose of mitigating risks in testing equipment in complex grids, the testing should include the entire system. This has a significant impact on the method of testing and the testing facility itself. The combination of simulation together with hardware experimentation will be inevitable to allow the validation of the system at the required complexity including the highly dynamic and transient power system behavior under real-time constraints [10].

The addition of power components distinguishes power HIL from control HIL. Control HIL encompasses the testing of sub-systems, such as protection relays, power converter controllers and power quality regulators, while power HIL tests complete power devices such as PV inverters. Power-Hardware-in-the-Loop (PHIL) testing allows equipment to be validated in a virtual power system under a wide range of realistic conditions, repeatedly, safely and economically. It combines the power of real-time simulation with the actual response of real power and control hardware components.

The essential part of Hardware in the Loop simulation is the Real-Time Simulator (RTS) which computes the simulation model and offer I/O capabilities. As the device under test works in real-time, the simulated system with which it will interact must be computed in real-time. Therefore, the simulation time-step of the Real-Time Simulator must be small enough to reproduce the behavior of the simulated system under dynamic conditions. Different platforms for real-time simulation are currently available for HIL applications. The two most popular platforms are Real Time Digital Simulator (RTDS) and OPAL RT:

Real Time Digital Simulator (RTDS) is a power system simulator that solves electromagnetic transient simulations in real time, mostly used for large-scale power system simulation, power system stability analysis, closed-loop testing of relays and HIL applications [17]. PSCAD models can be effortlessly migrated to RSCAD testbed so that the overall flexibility of RTDS-based simulation is increased. Specifically RTDS is the ideal simulation tool for HVDC study.

OPAL-RT is a PC/FPGA Based Real-Time Digital Simulator, Hardware-In-the-Loop (HIL) testing equipment and Rapid Control Prototyping (RCP) system [18]. Because of the capability of incorporating MATLAB/Simulink models, OPAL-RT systems are most popular in

designing, testing and optimizing control and protection systems for power electronics and motor drives.

A natural extension of the concepts of HIL leads to Power-Hardware-In-the-Loop (PHIL) simulations, in which natural couplings (nodes involving the conservation of energy) are established and a significant amount of energy can be virtually exchanged between the simulation software and the hardware being tested [10]. In electrical PHIL simulation the Hardware under Test (HuT) is a power device, more precisely the solar micro inverter in this thesis. But the virtually simulated system is electrical. Therefore, the power interface must be electrically coupled to the HuT. The power amplifier matches the power rating of HuT and accepts reference low level signals from the RTDS. High accuracy and small time-delay are very important. As the amplifier can provide or absorb power. 4 quadrant operation is normally required and a power source (e.g. the utility grid) as well as power sink (e.g. the utility grid or an external load) are needed. The conceptual diagram of the setup is shown as Fig 2.6.

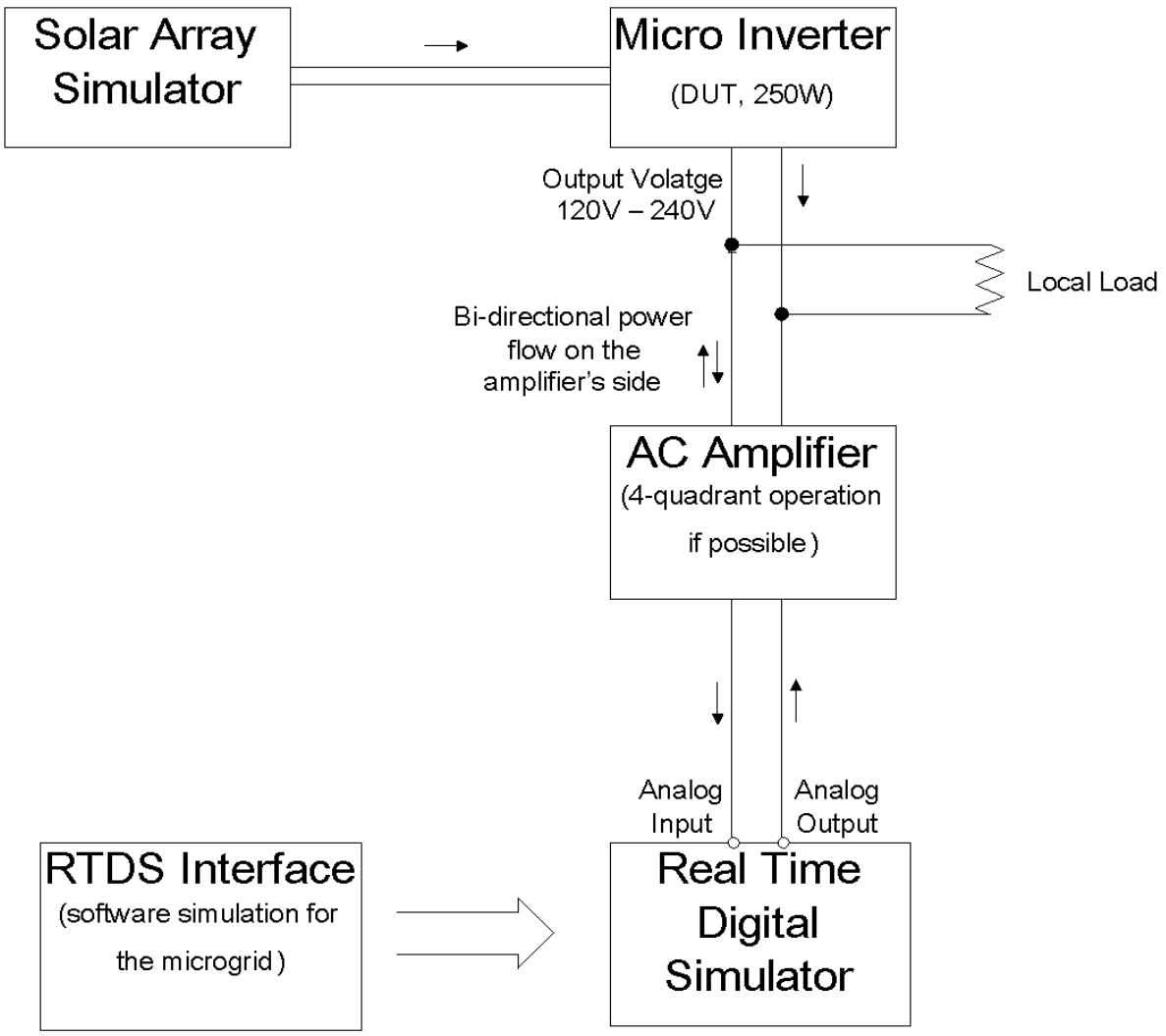

Fig 2.6 Test Setup of Micro inverter Hardware-in-the-Loop Testing

PV testing requires that we literally connect the output of one AC power source into the AC output of another. This concept is referred to as "back driving". "Back driving" current into an AC power source can cause it to shut down. To avoid shutting down, an AC power source capable of four quadrant operation, and external load or both are required. At the on-set of the test, the AC Power Source is supplying power only to the resistive load that is present. The

micro inverter will be in a high impedance state until it senses suitable DC power is available. As DC power is applied to the micro inverter DC input, the micro-controller starts to synchronize to the simulated AC utility power provided by the RTDS controlled AC power source. If the voltage and frequency sensed are within acceptable range, the micro inverter will start up. This process can take several minutes. During startup, the micro inverter will gradually ramp up the amount of current delivered until it reaches the MPP, maximum power point of the available PV panel [9].

2.6 PHIL Interfaces for RTDS

RTDS is one of the most commonly used PHIL testing platform for power system applications. Therefore, it is of great importance to understand its proprietary software RSCAD and hardware solution so that a solid PHIL interface can be built to perform the tests.

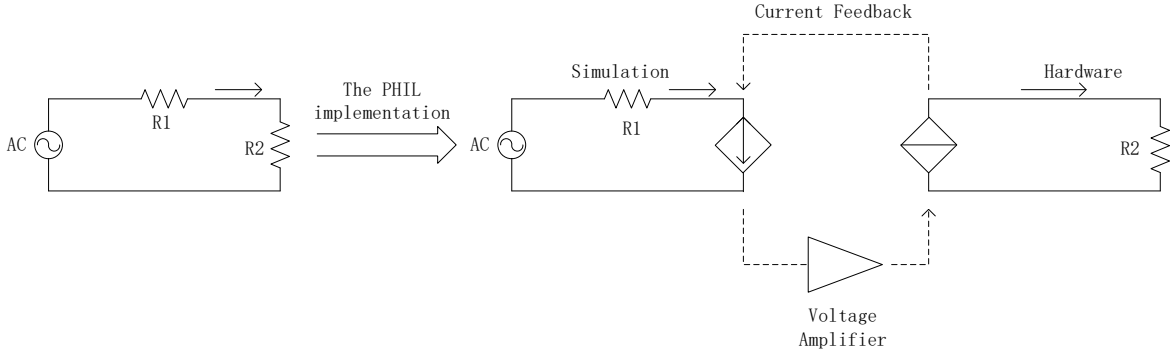

Fig 2.7 Signal Transfer Diagram of PHIL Implementation

The RTDS hardware has various interfaces to connect to the external devices. These interfaces are in the form of cards namely, GTAI/GTAO (for Analog I/O), GTDI/GTDO (for Digital I/O) and GTNET (for IEC 61850 communications).

PHIL specifically requires utilizing GTAO and GTAI cards for the data transfer. The power grid model simulated in RSCAD provides the necessary signals. In this case voltage reference

signals that are to be transferred via the PHIL loop as are shown in Fig 2.8. Similarly the RSCAD simulation also contains inputs which collect data from the external world, in this case current signal from the output of micro inverter. These interface connections are explained in detail below.

For the Analog Outputs, the CT outputs from RSCAD simulations are collected from the RTDS via the GTAO cards. Inputs to the GTAO model are IEEE−754 double precision floating point numbers. This model converts and scales input signals to 16−bit integers and writes them to the GTAO card via the GTIO interface. All the outputs signals are sent to the D to A converters on the GTAO card at the same time (aligned). The GTAO card's output range is +/− 10 volts. Inputs to the GTAO component must be scaled to produce a desired voltage on the output channels of the GTAO card, due to the limited input capability of the connected current amplifier. The scale values can be entered in the "D/A Output Scaling" menu item (See Fig 2.8). For example, an input signal of magnitude 187.79 kV L−N peak is input to the GTAO component. Entering a scale value of 187.79 will result in a 5V peak signal output of the GTAO card [17].

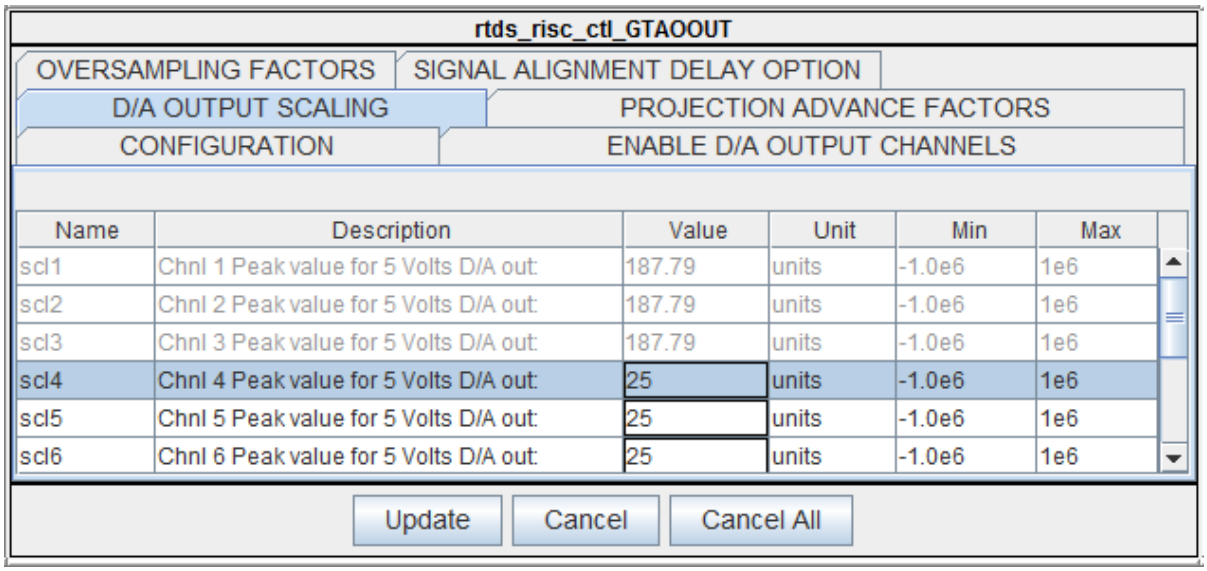

Fig 2.8 Scaling Factor Settings of GTAO/GTAI

For Analog Inputs, the current inputs for RSCAD simulations are collected from the micro inverter via the GTAI cards. Similar to the GTAO card, the GTAI reads data from up to twelve analogue input channels and converts it to digital format for use by the RTDS. A separate scale value is specified for each input signal. Scale values represent the analog signal peak voltage (in volts) which will result in a value of 1.0 to be present on the corresponding output signal wire. For example, a scale value of scl1=5.0 means that a voltage of 1 volt on the analogue input channel #1 will result in a value of 1/5 (0.2) on the output wire labelled '1'. The maximum input range of the GTAI is +/− 10 volts peak [17].

The complete RSCAD interface for PHIL micro inverter testing is show in Fig 2.9.

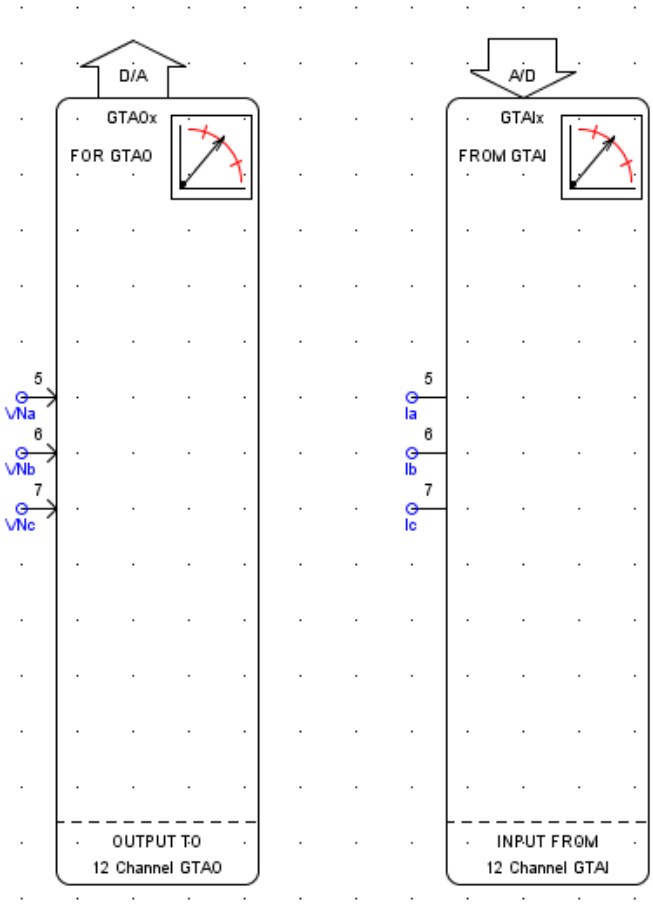

Fig 2.9 RSCAD Interface for PHIL Test

Chapter III: RSCAD Models for Residential PV System

RSCAD is the main interface with the RTDS hardware and is designed to allow the user to perform all of the necessary steps to prepare and run simulations, and to analyze simulation results. Even though there are many different models built for PV system simulation and each has its validated testing environment, RSCAD (EMPTC type simulation) modelling will be used in this thesis for the purpose of PHIL test. This chapter provides details of PV system modelling in RSCAD and introduces two types of PV system models which are suitable for all the four test scenarios mentioned in the previous chapter.

3.1 Detailed RSCAD Model for PV Array Model

The PV Array model has two power system nodes which allow it to be interfaced with the RTDS Network Solution; nodes P and N represent the positive and negative terminals respectively. The connections labeled “INSOLATION” and “TEMPERATURE” are the model’s control signal inputs. The complete model of RSCAD PV array is given in Fig 3.1.

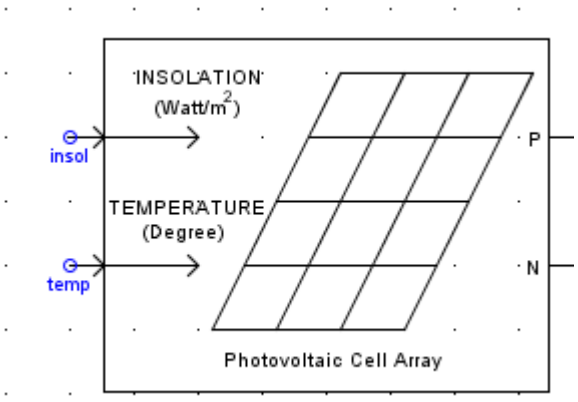

Fig 3.1 PV Array Model in RSCAD

A PV Array should normally consist of a large number of PV modules. The following figure represents the conceptual model for a PV module. The current source represents the current generated by solar radiation striking the photovoltaic cells. The diode models the characteristics of the junction between the P−type and N−type semiconductors.

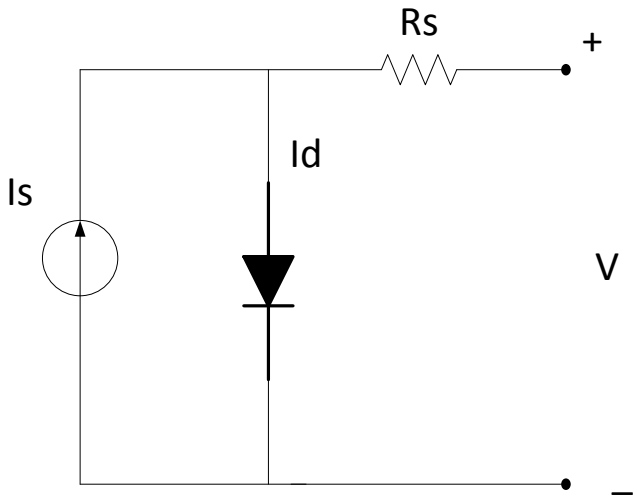

Fig 3.2 Equivalent PV Module Model in RSCAD

The voltage, V, and current, I, output from the PV array are based on the calculated outputs for each individual module. The equations used to calculate the currents and voltages of individual modules are provided; these are then scaled appropriately according to the topology of the array.

The current flowing through the internal diode representation is given by the following equation. This equation is well known and is commonly referred to as the 'diode law'.

$$I_D = I_0 \left(exp \left(\frac{V + I \cdot R_s}{n \cdot V_T} \right) - 1 \right) \quad (1)$$

Where $V + I \cdot R_s$ is the total bias voltage, n is the diode ideality factor.

The calculation of equation (1) requires that the thermal potential difference V_T, and the diode saturation current, I_0, be defined. These two quantities are given in equations below:

$$V_T = \left[(TEMP + 273) \cdot \frac{K}{q}\right] \cdot N_c \tag{2}$$

Where K is the Bolzmann constant, q is the elementary charge.

$$I_0 = A \cdot (TEMP + 273)^{\gamma} \cdot exp\left(\frac{E_g \cdot N_c}{nid \cdot V_T}\right) \tag{3}$$

Where γ is the temperature dependency factor, nid is the diode ideality factor.

Calculation of equations (2-3) again requires the intermediate calculation of other quantities. The band energy gap of the diode and the temperature dependent coefficient can be calculated using equations below:

$$E_g = 1.16 - 0.000702 \cdot \frac{(TEMP+273)^2}{(TEMP+273-1108)} \tag{4}$$

$$A = \frac{I_{oref}}{(refTEMP+273)^{\gamma} \cdot exp\left(\frac{-E_{gref} \cdot N_c}{nid \cdot V_T}\right)} \tag{5}$$

Finally, in order to calculate A, we must define the reference diode saturation current, which is given by equation:

$$I_{oref} = \frac{I_{scref}}{exp\left(\frac{V_{oref}}{nid \cdot V_{Tref}}\right)} \tag{6}$$

The following equation is used to obtain the value of the internal series resistance shown in Fig 3.1.

$$R_s = \frac{nid \cdot V_{Tref} \cdot ln\left(\frac{I_{scref} - I_{mpref}}{I_{oref}} + 1.0\right) - V_{mpref}}{I_{mpref}} \tag{7}$$

The internal current source in the PV array model can be described using the following equation:

$$I_{sc} = I_{scref} \cdot \left(\frac{INS}{1000}\right) \cdot \left(1.0 + \frac{J_{TMP}}{100} \cdot (TEMP - refTEMP)\right) \tag{8}$$

The total array current is the module current multiplied by the Np parameter. The total internal diode thermal voltage is the module thermal voltage multiplied by the Ns parameter.

3.2 Detailed Model for Grid-Connected PV Inverter and RSCAD Interface with Small Time Step Simulation

The actual inverter model used in the thesis is a conventional two-stage inverter with a Buck DC-DC stage and a two-level DC/AC converter shown in Fig 3.3. Control blocks include two triangle wave data generators for DC/DC converter and DC/AC converter, reference MI wave generator for DC/AC converter, DC/DC converter control, simple P/Q control, DC capacitor charger control and MPPT control, all of which has no difference with the proposed inverter model built in MATLAB/Simulink before.

What differentiates the RSCAD inverter model from a MATLAB/Simulink model is the interface, which is used to transfer power system signals between large and small time step simulations. Usually interface transformer components are used to transfer power system signals between large and small time step simulations. These interface transformers, however, cannot be used for the PV array because the outputs of the PV array component are effectively DC signals which cannot flow through the transformer.

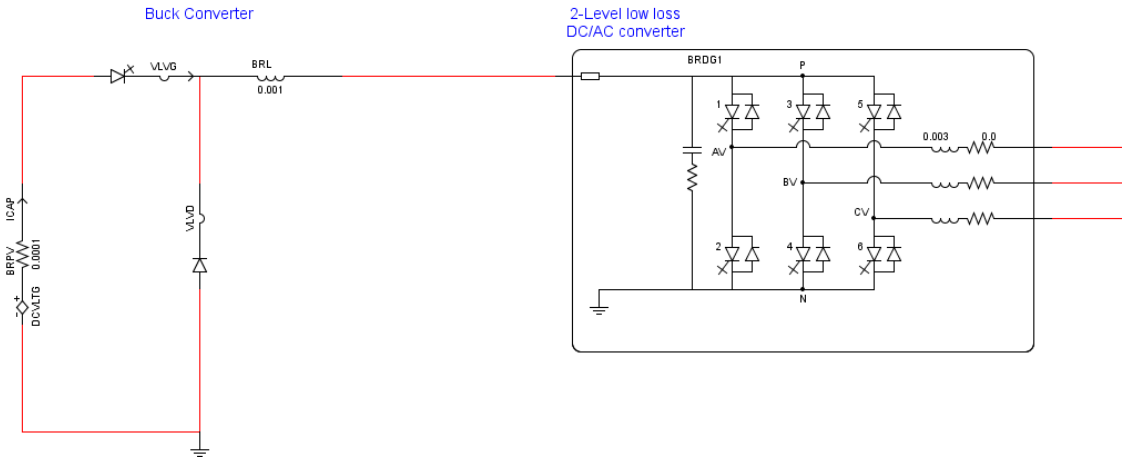

Fig 3.3 Grid-Connected PV Inverter Model in RSCAD

One solution which would bridge the large and small time step portions of the simulation is to construct the necessary interface by transferring voltage and current information between them. Voltage information from the large time step side of the simulation is transferred to the small time−step side of the simulation and current information from the small time step side is brought to the large time step side. Fig 3.4 illustrates the signals which must be interchanged between the large and small time step portions of the simulation.

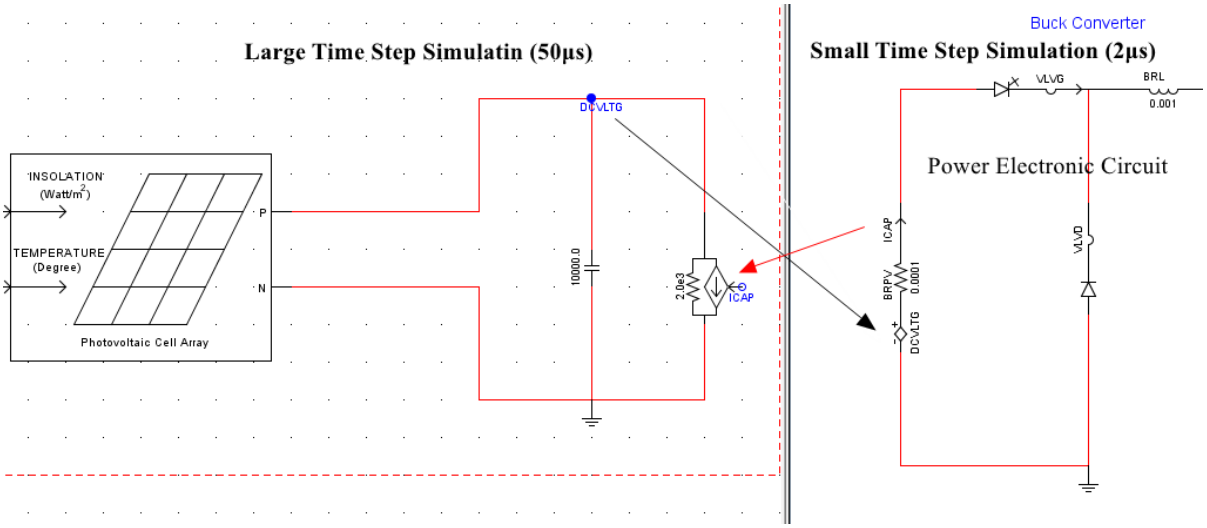

Fig 3.4 Signal Interchange between Large and Small Time Step simulation

The node voltage in the large time step side is transferred to the small time step side, driving a voltage source. The current in the small time step side is transferred back to the large time step side, driving a current source branch. In this configuration, an interface capacitor, marked with a red rectangle, contributes to the stability of the interface by smoothing the node voltage. A physical capacitor is commonly found in the power conversion system applications with PV arrays [17]. By using this interface technique, the necessary power electronics application device(s) can be accurately modeled and simulated with the PV array model. The same application in RSCAD modelling can be found in the VSC interface (See Fig 3.5) which connects the output of DC/AC converter to the power system network with large time step.

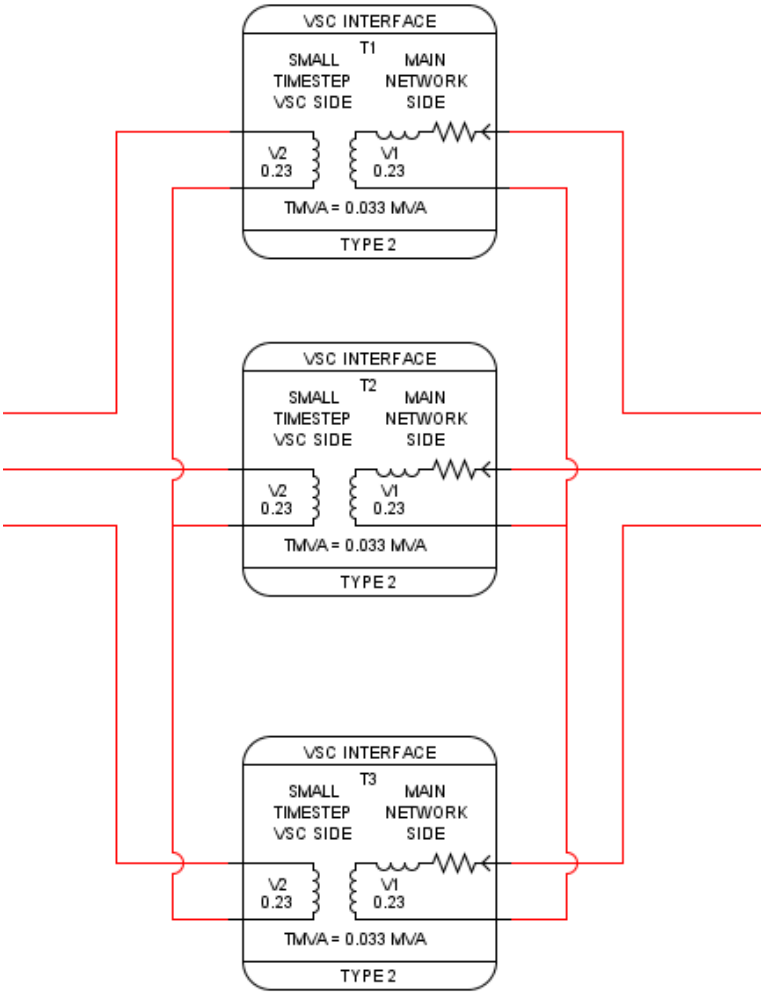

Fig 3.5 RSCAD VSC Interface

3.4 Average RSCAD Model for Distribution System Simulation

The intention of developing average model of PV system is to accommodate for the space constraints in RTDS. One of the primary modelling challenges in RTDS is to maintain computation simplicity of simulating large systems with the limited hardware. It is

recommended from RTDS technologies that for a system to replicate a real time scenario, it needs to be run at a time step close to 50 μs.

Due to the shared characteristics of EMTDC, it is relatively easy to implement the existing PSCAD model in RTDS environment compared to other inverter models built in MATLAB/Simulink or Spice. The average model of PV system in PSCAD is built on [21], in which the modelling details of PV model in PSCAD are explicitly explained. The model uses an approximate DC-DC stage, DC-AC stage, a phase lock loop, a current regulator, and a pre-designed filter.

For the purpose of study the impact of PV penetration and more importantly, PHIL testing in distribution system level, the PSCAD model has been migrated to RSCAD tool with several modifications:

1) Assume that the RSCAD models of PV panels are always operated at Maximum Power Point (MPP). This assumption will reduce the computation burdens in PHIL simulation. Details are explained in Appendix B.
2) Basic protection scheme for typical residential PV system has been adopted in the average PV inverter model.

The modified part of the RSCAD average PV system model is shown in Fig 3.6.

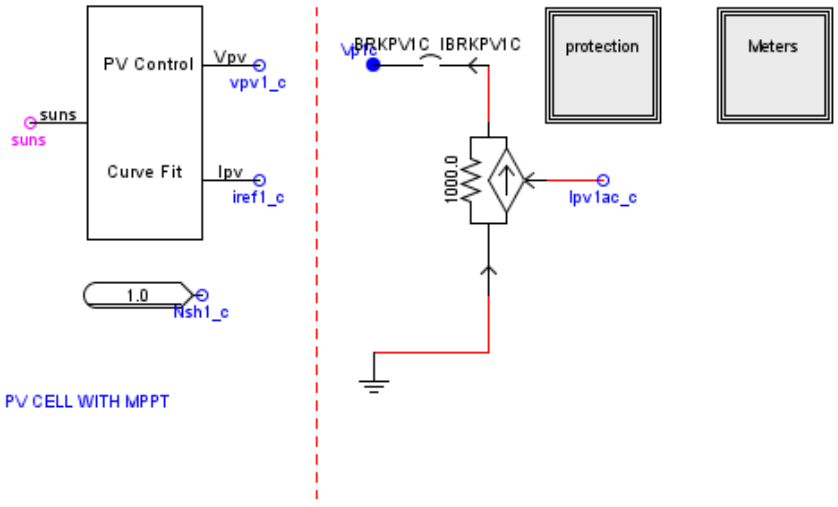

Fig 3.6 Modified RSCAD Average PV System Model

3.5 Inverter Model Comparison in RTDS Environment

IEC 61000-3-3 is concerned with the limitation of voltage fluctuations and flicker impressed on the public low-voltage system. It specifies limits of voltage changes that may be produced by equipment tested under specified conditions and gives guidance on methods of assessment. In this section we choose to study the impact of variations of solar radiation on the load voltage profile to compare the two inverter models (See Fig 3.7) introduced in previous chapters.

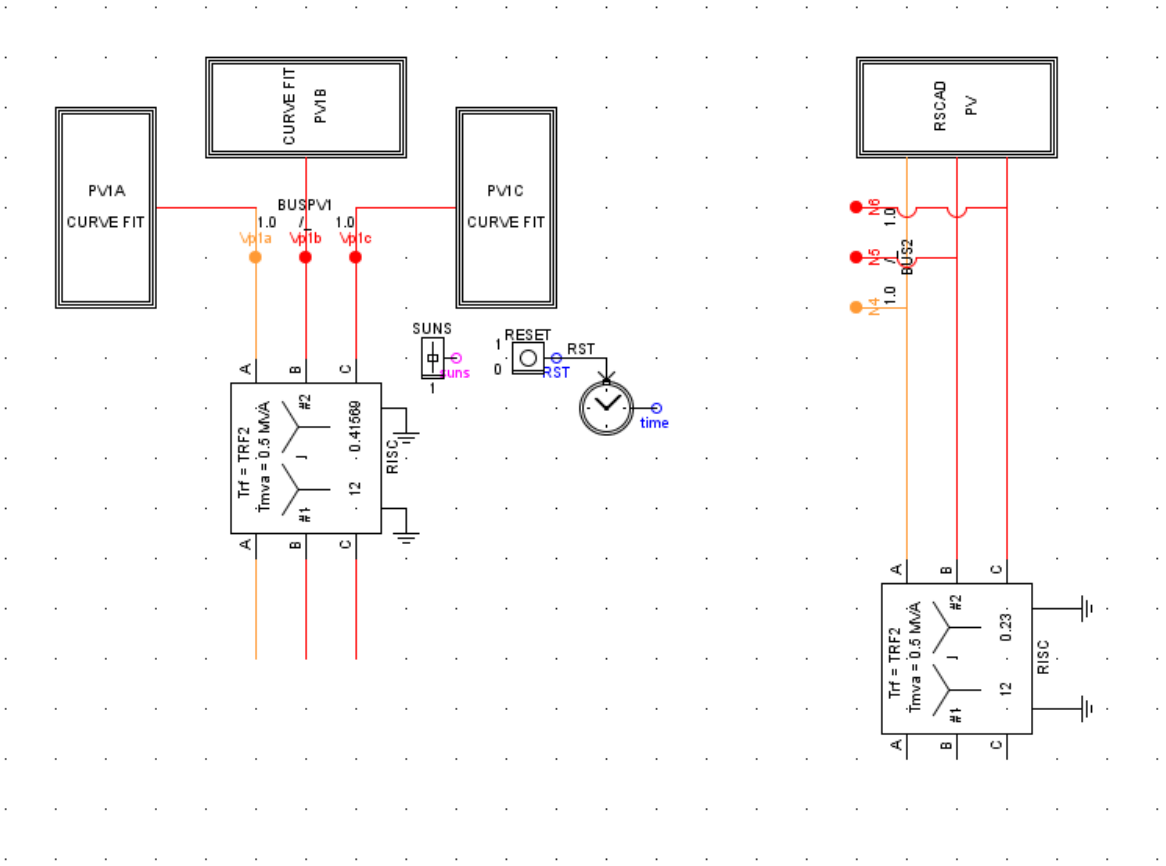

Fig 3.7 Comparison Between Built in RSCAD Model and Average Model of PV Inverter

The models will be tested in a typical distribution system shown in Fig 2.6. For the purpose of monitoring change of PV output more clearly, the test is designed to simulate the extreme case

in which the irradiation suddenly drops to zero. The output current plots of the two different solar inverter model are given in Fig 3.8 and Fig 3.9 respectively. For this case of study, the reason that we only monitor current output instead of node voltage variation is that, the voltage variation on certain nodes will be mainly decided by the equivalent input impedance seen from the input side. Therefore, it is not reasonable to use monitored node voltage variation to evaluate the two models unless a set of realistic parameters of the distribution system can be determined.

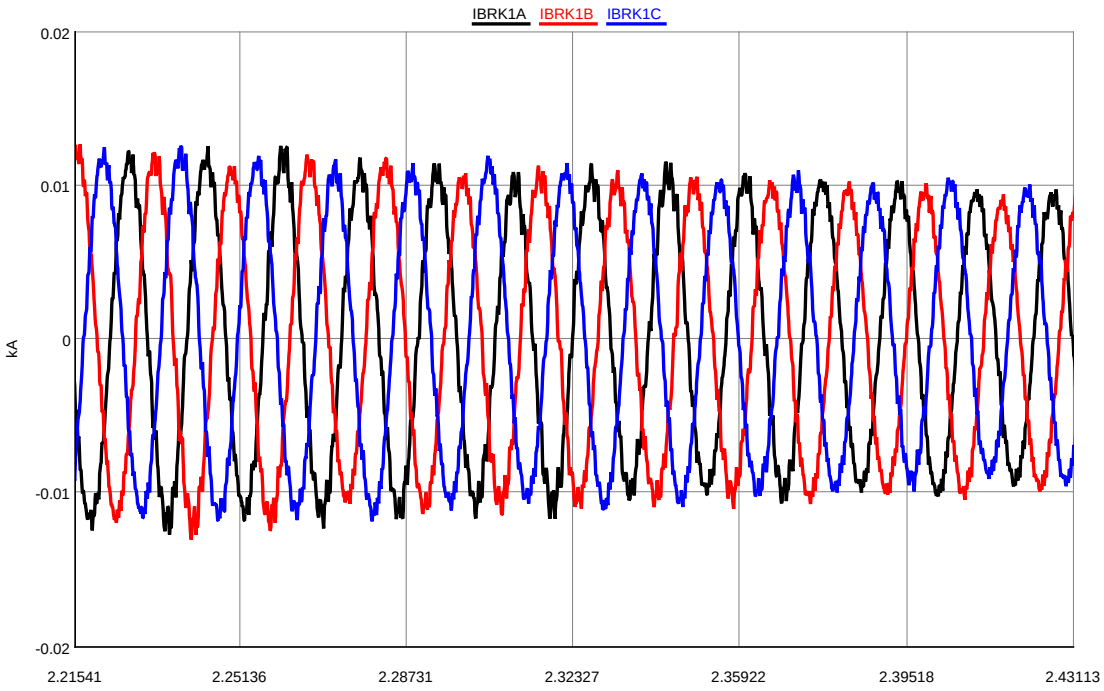

Fig 3.8 Output Current Variation for Built-in RSCAD Inverter Model after Intentional Power Curtailment

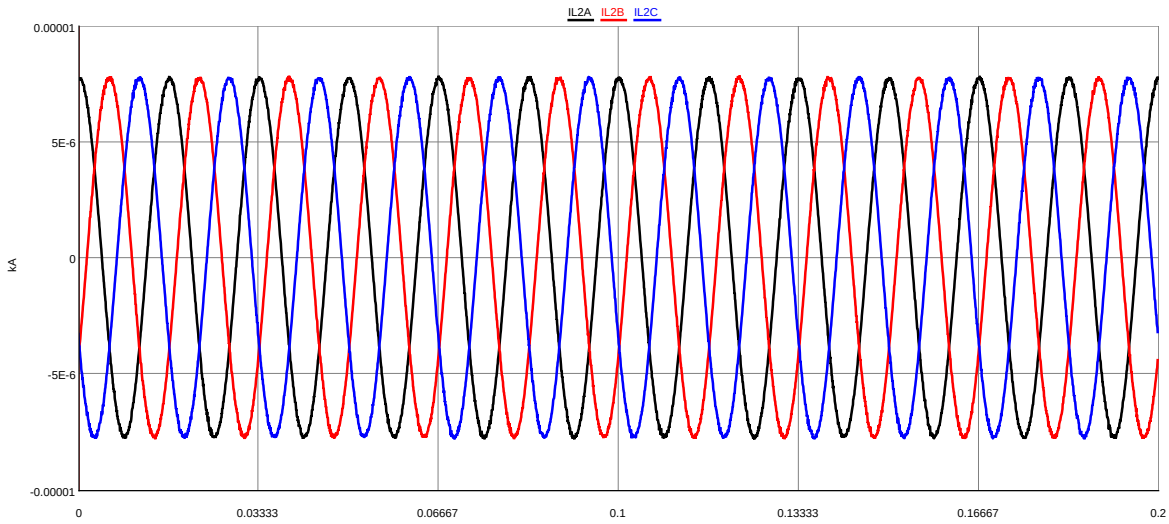

Fig 3.9 Output Current Variation for Average Inverter Model after Intentional Power Curtailment

It can be observed from the plots that, the built-in RSCAD model can provide details of current drop with certain amount of harmonics components. In comparison, the average inverter model shows very little variation details and acts as a 'step response'. However, the average model puts a lot less computation burden on RTDS racks and yields steady-state waveform in a shorter period.

Chapter IV: Fault Diagnosis in Residential PV System

A detailed study of fault diagnosis function is conducted in our proposed residential PV system. First, conventional protection devices in PV system are reviewed. Different types of faults and miswiring issues are addressed, simulated and then analyzed on both sides of the PV inverter. These include both AC side and DC side faults, both bolted and arcing faults. Taking these limits of fault diagnosis into account, improvements of detection functionality which can be applied to our PnP PV system are suggested at last.

4.1 Overview of Residential PV System Protection

As mentioned in the first chapter, a typical grid-connected PV system consists of PV arrays, a grid-connected inverter, connection wirings and protection devices. From a protection design perspective, a residential PV system model in compliance with NEC codes yet with minimum cost should at least include, a AC disconnect for over/under voltage protection and over/under frequency protection, a DC disconnect which provides overcurrent and over-voltage protection for PV modules as well as ground fault protection. The baseline schematic is shown in Fig 4.1.

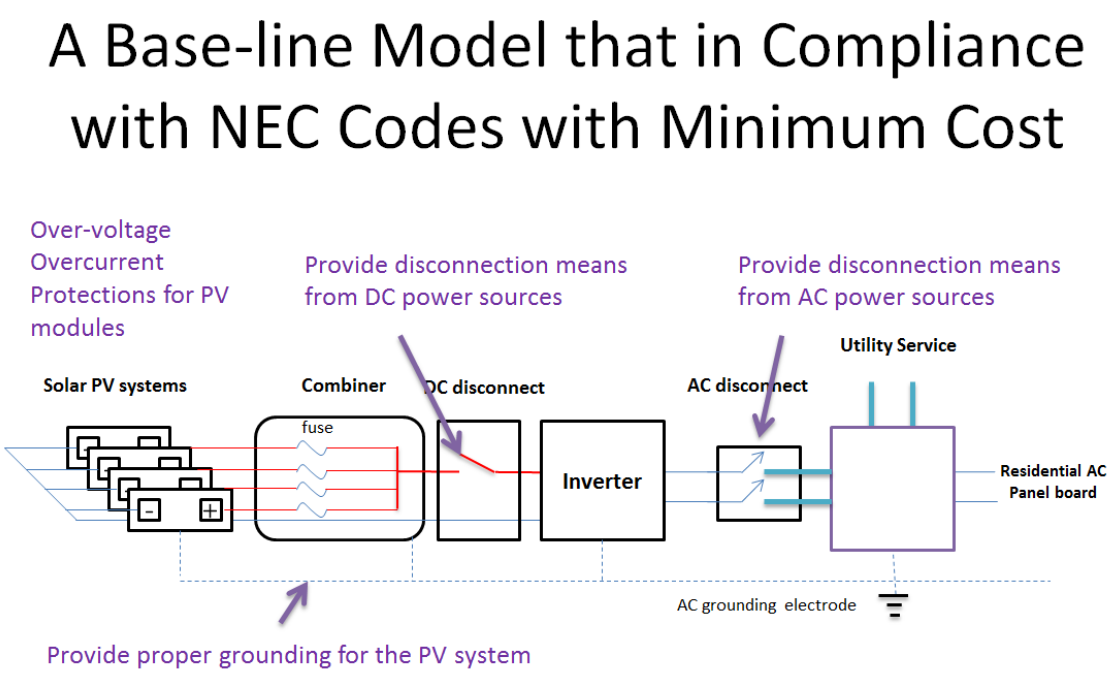

Fig 4.1 Baseline Model that in Compliance with NEC Codes with Minimum Cost

What makes fault analysis in PV System Unique from traditional power system problem is the protection devices on DC side. Conventional protection devices in residential PV system should include overcurrent protection devices (OCPD) and ground fault protection devices (GFPD):

Overcurrent Protection Devices (OCPD):

For overcurrent protection, fuses are the most common overcurrent protection devices for PV modules and combiner conductors because of its simplicity. The NEC requires that a single overcurrent protection device shall be used in series-connected strings of two or more modules. The rating of overcurrent devices shall be no less than 156 percent of module rated short-circuit current [21].

Ground Fault Protection Devices (GFPD):

For ground fault protection, according to NEC, the GFPD should be capable of ground fault detection, fault current interruption, and fault indication. In practice, the GFPDs can be mounted either inside or outside the inverter and are actually installed between the negative

current-carrying conductor and system grounding point. Under pre-fault conditions, current will flow in the negative conductor but not in any of the system grounding due to the fact that there is only one point connecting the negative conductor to ground. In the case of a ground fault when the positive conductor is accidentally connected to ground, the ground-fault current will flow through GFPD in a loop caused by multi-point ground. The conventional GFPD is either a circuit breaker or a fuse with rated current range from 0.1A to 1A. If the ground-fault current exceeds its pickup value, the GFPD may operate and clear the fault [21].

4.2 AC Side Fault Analysis in Residential PV System

AC side or grid-side fault in residential PV system somewhat departs from traditional distribution system protection problem because of the addition of inverter and the independent operating logic itself. Also inverter trips not only on faults but other grid disturbances like islanding or other abnormal grid conditions. The purpose of this chapter is to simulate the possible disconnection scenarios caused by abnormal voltage or frequency conditions in our RSCAD testbed. The protection scheme implemented in our inverter is shown in Table 4.2 [16].

Table 4.1 Protection Scheme for Typical Residential PV System

	Range	Trip
Terminal Voltage	V<0.5 pu	6 cycles
	0.5 pu ≤ V < 0.88 pu	120 cycles
	0.88 pu ≤ V < 1.1 pu	normal operation
	1.1 pu ≤ V < 1.37 pu	120 cycles
	1.37 pu ≤ V	6 cycles
Grid Frequency	f < 59.3 Hz	6 cycles
	59.3 Hz ≤ f < 60.5 Hz	Normal operation
	60.5 Hz < f	6 cycles

There are two types of coordination failure case to be simulated and analyzed in this section:

1) Coordination failure between inverter protection and upstream breaker.

2) Coordination failure between islanding mode and anti-islanding mode.

The first case is a balanced downstream ground fault which is the most common fault type. The RSCAD testbed for this fault simulation is shown in Fig 4.2. The upstream transformer represents the customer level distribution transformer.

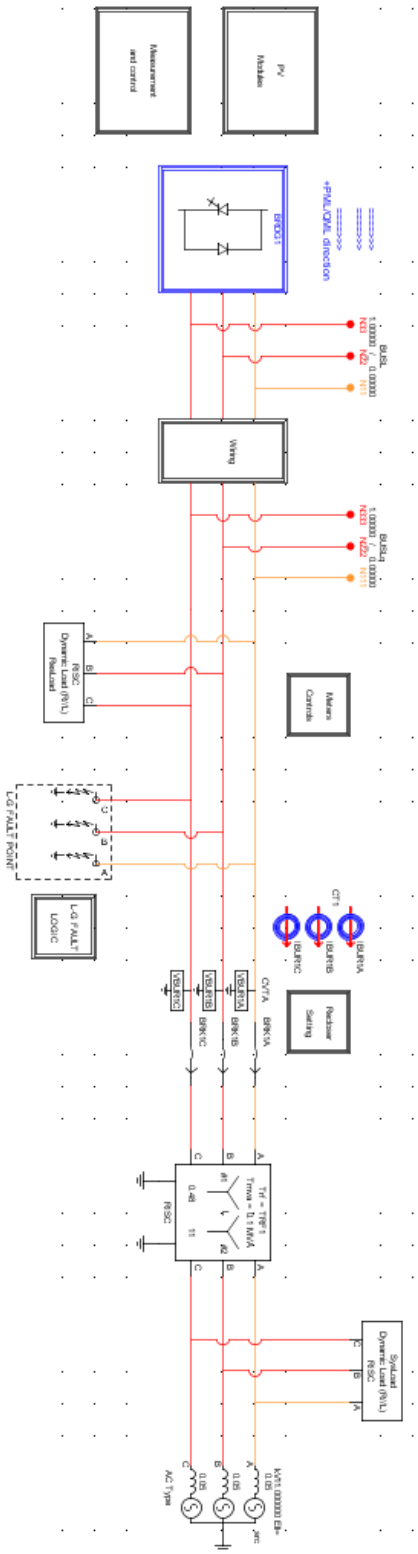

Fig 4.2 RSCAD Testbed for Downstream Ground Fault

For this type of fault, since the fault location is above the load location, both the inverter and the upstream breaker should detect the fault current and trip in order to isolate the fault. However, different anti-islanding or low voltage/frequency ride through may bring some coordination issues with the upstream breaker. One typical mis-coordination under this type of situation is that the upstream relay trips the breaker while the PV inverter 'rides through' the fault. However, normally utility will want to make sure that inverter trips off before breaker operate.

The breaker current evolution and inverter output current evolution are shown in Fig 4.3 and Fig 4.4 respectively. The default inverter protection logic needs to consider avoiding nuisance tripping during the start-up as well unexpected load variation during the whole day, same as the islanding mode setting in the next case.

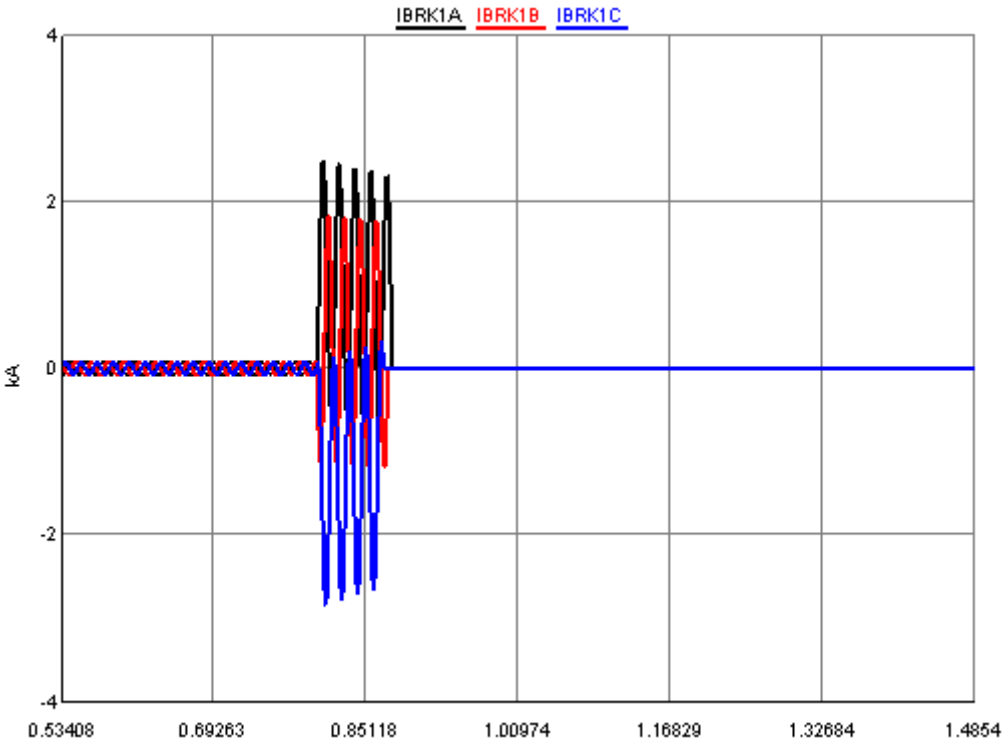

Fig 4.3 Upstream Breaker Current Evolution in Case 1

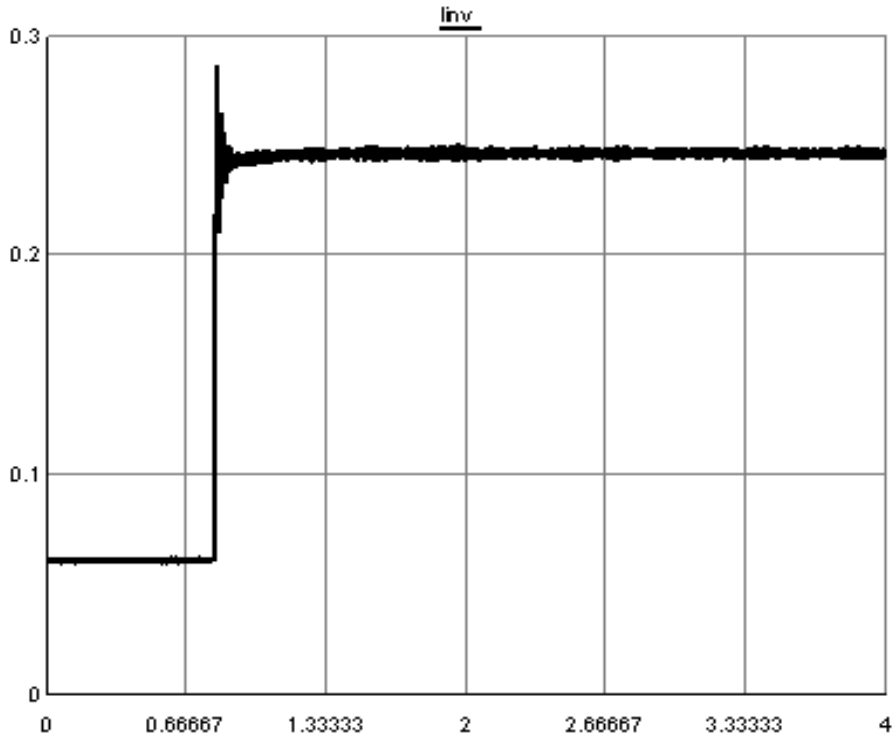

Fig 4.4 Inverter Output Current Evolution in Case 1

From the figures above (with default horizontal axis to be time/second), it is clear that the inverter 'rides though' the fault current after the upstream breaker trips. The operation results from the insufficient voltage drop and overcurrent seen from the inverter, determined by its protection scheme. This coordination only applies to a temporary fault because the tripping of upstream breaker does not clear the fault. However, if the house's load exactly matches the output of the panels at the instant of the grid interruption, there is still a possibility that the inverter does not trip during the fault. If the fault is constant and evolves with time, the consumer will expect to suffer from large amount of power loss as well as possible fire hazards. The second case is a balanced upstream ground fault. The RSCAD testbed for fault simulation is shown in Fig 4.5.

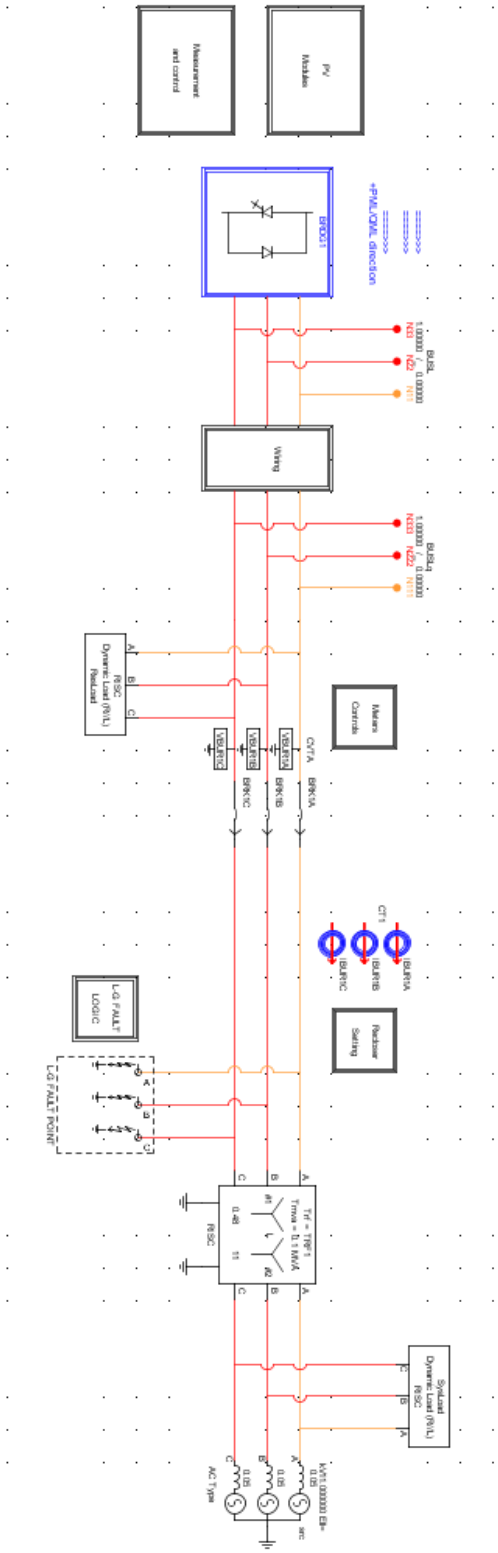

Fig 4.5 RSCAD Testbed for Upstream Ground Fault

Different from the first case, the upstream ground fault is expected to be cleared by upstream breaker only. The inverter can either 'ride through' the fault current or choose anti-islanding scheme to operate, depending on the prospective utility's requirement. The islanding mode of the inverter results in the fault current evolution shown in Fig 4.6 and Fig 4.7. The relay of the upstream breaker and the inverter fault detection mechanism both sense the fault current and trip the whole system (in this situation the inverter protection operates very shortly after the upstream breaker trips). Fig 4.8 and Fig 4.9 shows the fault current evolution under anti-islanding mode of the inverter. The inverter rides through the fault at 0.8s and resynchronizes to operate at islanding mode to support local loads after a time period defined by MPPT control.

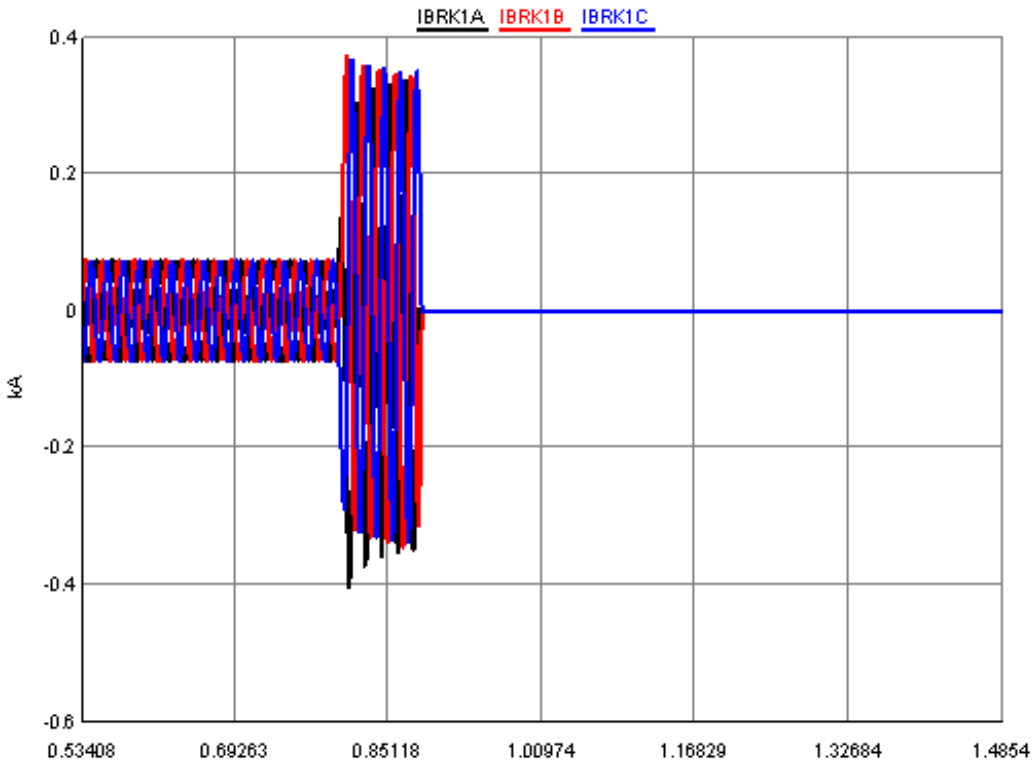

Fig 4.6 Breaker Current Evolution for Upstream Ground Fault on Islanding Mode

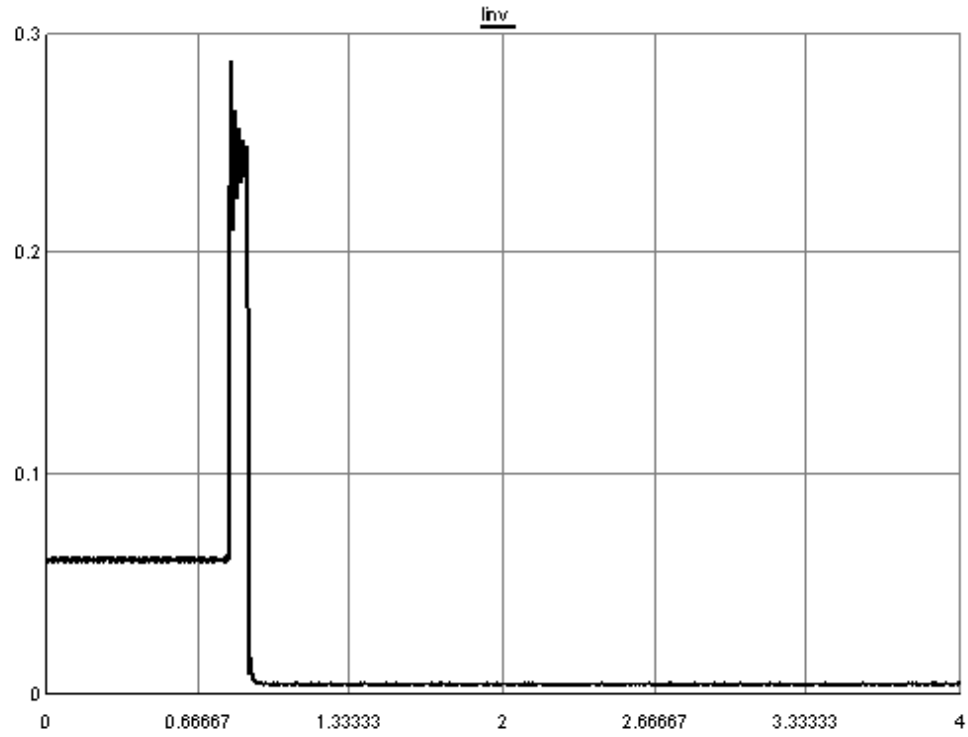

Fig 4.7 Inverter Output Current Evolution for Upstream Ground Fault on Islanding Mode

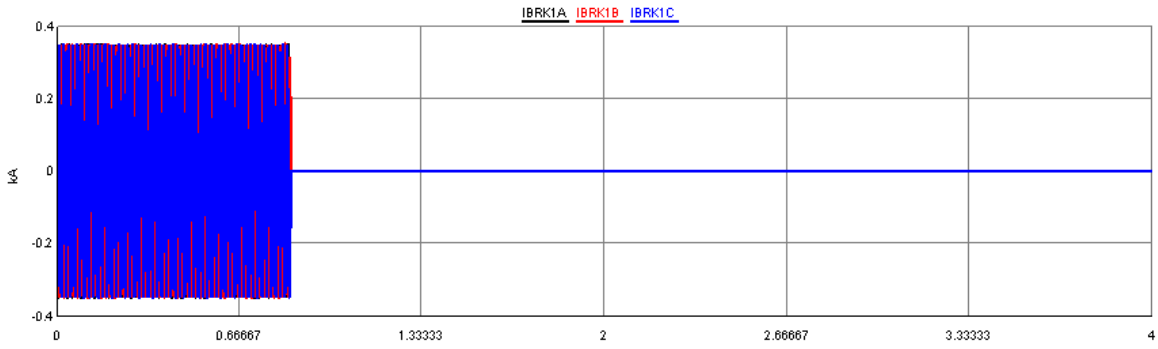

Fig 4.8 Breaker Current Evolution for Upstream Ground Fault on Anti-Islanding Mode

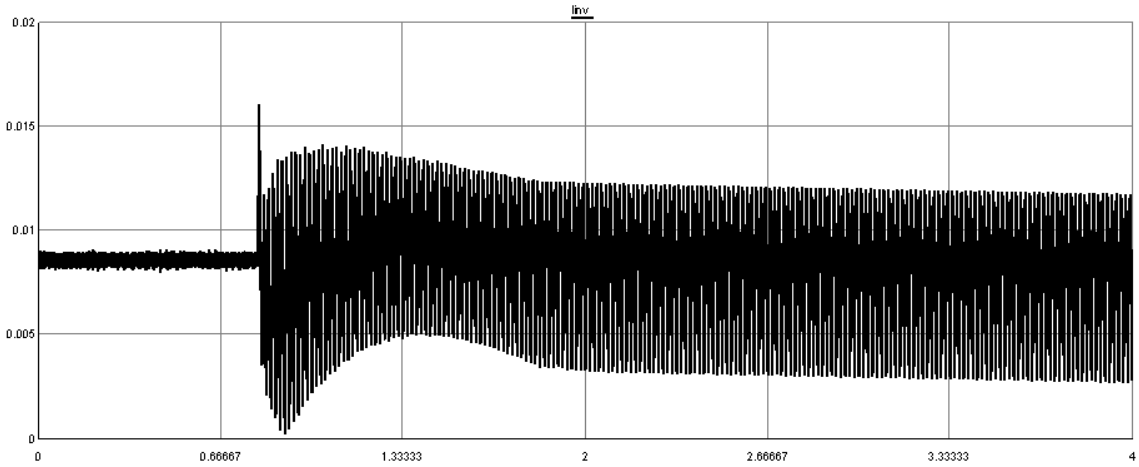

Fig 4.9 Inverter Output Current Evolution for Upstream Ground Fault on Anti-Islanding Mode

From the simulation results of case 1 and case 2, it is noticeable that if we want to implement the protection function in our baseline model. There is a trade-off in designing the inverter protection logic to cover as many as fault scenarios versus to reach a more reasonable coordination with upstream protection devices. Therefore, introducing more complicated functions like directional overcurrent protection and waveform-based fault detection to the system will be an addition to improve the PV system performance in case of AC fault.

4.3 Fault Analysis in Solar PV Arrays

Fault analysis in PV arrays is another unique problem that departs from traditional AC fault analysis. Faults in PV arrays can damage PV modules and cables, as well as result in fire risk or electrical shock hazards. A significant amount of power loss can also be seen during faults occurring in PV arrays. Therefore, fault analysis for this type of failure should be given top priority with respect to system reliability and efficiency.

The magnitude of the ground–fault current depends on fault location, fault impedance as well as ambient weather conditions. If a ground fault is not clear by proper fault protection, the fault connection is very likely to grow and generate a DC arc, which may lead to a fire hazard. Typical ground faults are caused by the following reasons:

1) Incidental short circuit between normal conductor and ground. For example, a cable in the combiner box might contact a ground conductor incidentally;
2) Insulation failures. For example, an animal may chew through cable insulation and cause a ground fault;
3) Ground faults within PV modules. For example, a solar cell may short circuit to grounded module frames due to deteriorating encapsulation of a PV module.

This section describes the RSCAD-based simulation of various types of faults in PV arrays under nominal irradiance level without considering the effect of the MPPT algorithm. Fundamental approaches of fault analysis are utilized in this section, including I-V characteristic analysis and circuit analysis.

One important assumption in this chapter's simulation is that the PV array is the only source of fault current, meaning no backfed current is contributed from utility grid. This assumption is valid with respect to most micro inverters or string inverters under 10 kW. Also, for simplicity, this section only takes into account steady state analysis due to the fact that the fault current settling time is negligible under the tested array capacity (usually less than 0.1ms) and hardly has any effects on conventional protection devices like fuses.

For our RSCAD model, the system negative conductor and module frames are all solidly grounded to meet the US NEC requirement. Under normal working conditions, two switches in the GFPD are all closed. In simulation, it is assumed that the MPPT of the inverter ranges from 80V to 240V. The schematic of RSCAD array fault simulation model is shown in Fig 4.10.

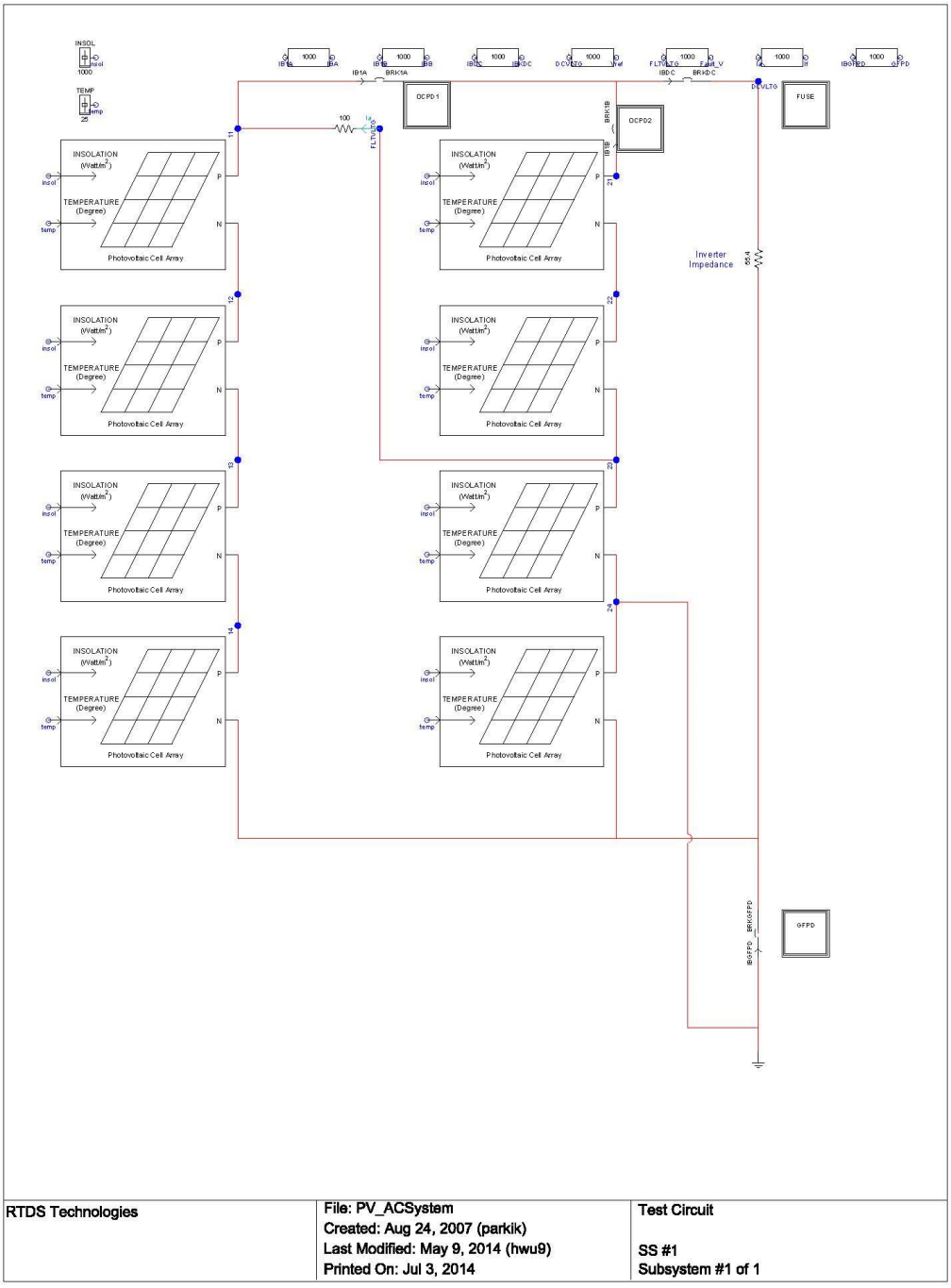

Fig 4.10 Schematic of RSCAD Array Fault Simulation Model with Inverter Simplification

As stated earlier, a DC–grounded, AC–isolated central inverter is modeled in each of the simulations because this topology is susceptible to faults that are undetected by GFPDs.

According to the comparison study conducted by Sandia National Laboratory [12], if the voltage ripple and maximum power tracking are ignored, the PV system can be approximated by a steady state DC system with a constant resistance. Only the real component of the inverter impedance needs to be modeled, despite the fact that physical inverters are a complex system containing transistors, capacitors, and switching controls. This means that the reactive components of the inverter impedance have no effect on the steady state solution before and after the fault occurs; there is a discrete change in system state, in which the storage the storage elements in the inverter backfed current through the PV system if there are no blocking diodes. As will be shown later, the inverter bus capacitor is charged to nominal value before the fault, but the ground fault drops the operating voltage of the array so the capacitor discharges into the array. This spike in current into the array is large, but the time period of the backfed is unlikely to trip a GFPD fuse.

If inductive and capacitive parasitics, such as those present in real systems, are added to the circuit simulations, there will be greater variation between modelling the fault as a simple resistor in comparison to the non-linear arc fault model discussed in Section 5.4. However, there is no analytical different in the post-fault analysis excluding transient response.

4.3.1 Classification of Faults in PV Arrays

Generally faults in PV Arrays can be classified into three different types [21]:

- Ground fault: ground fault happens when any string node is arbitrarily attached to a grounding point, either solidly grounded or with ground impedance. The instantaneous fault often creates voltage changes and unbalanced currents between the faulted string and other normal strings.
- Line-to-line fault: this type of fault is usually defined as a short-circuit fault among PV modules or array cables with different potential. In this thesis, it is assumed that line to line fault does not involve any ground points. The magnitude of line-line fault current

depends on environmental factors as well as the fault type: cross-string parallel fault or cross-string parallel fault.

- Open-circuit fault: An open-circuit fault is an accidental disconnection at a normal current-carrying conductor. This might occur on cracking PV cells/modules, or between module interconnections, typically in bus wiring or junction box.

The classification drawing of faults in PV arrays are shown in Fig 4.11.

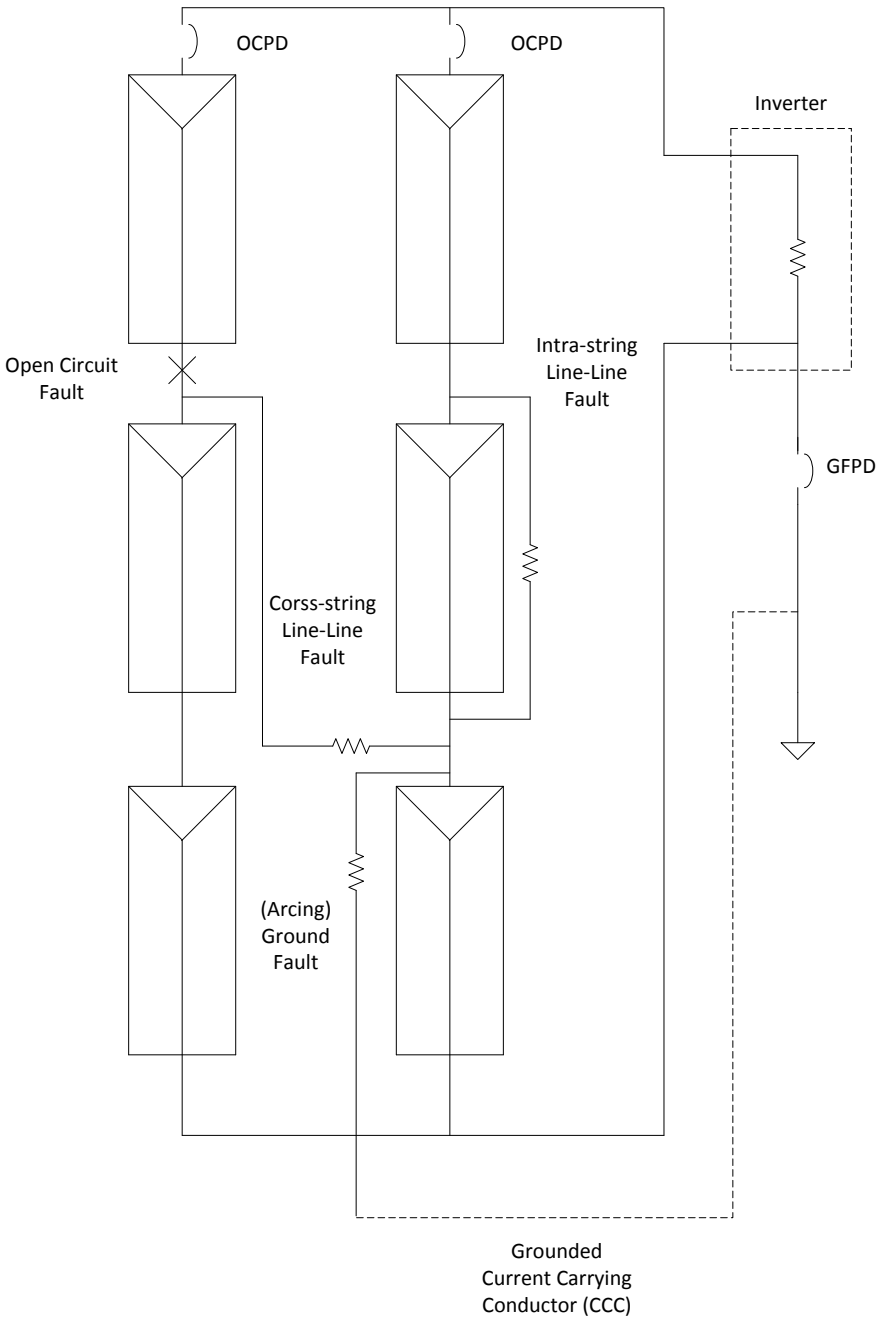

Fig 4.11 Different Types of Faults on the DC Side of a PV Array Composed of Two Strings

4.3.2 Analytical Approach of PV Fault Study: Circuit Analysis and I-V Curve Analysis

For DC fault analysis in PV array, it is very important to obtain a basic idea about the evolution of fault current before the simulation process or the field test is carried on. This section summarizes the two fundamental yet widely-used fault analysis approaches based on circuit analysis and I-V characteristics analysis.

The first approach is circuit analysis, which manipulates Kirchhoff's Current Law (KCL) and Kirchhoff's Voltage Law (KVL) to solve the steady-state fault current level directly.

We choose the solid ground fault as a baseline to illustrate this type of method. The schematic drawing is shown in Fig 4.12.

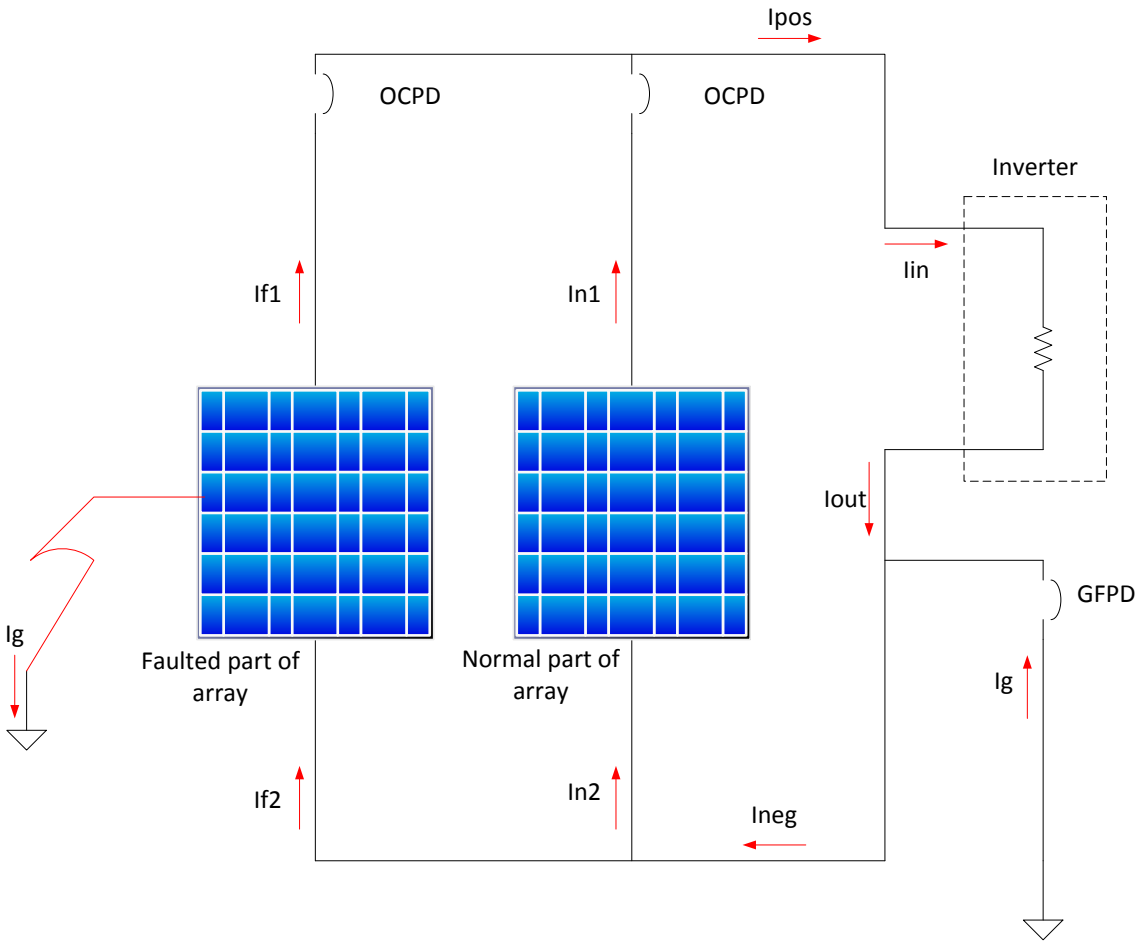

Fig 4.12 Schematic of Different Types of Faults on PV Array

Under normal conditions, the ground current Ig in the GFPD is close to zero. As a result, the current coming out of the inverter Ineg should be equal to Ipos. If there is a fault occurring in the PV array, the current flow of the PV array will be changed accordingly. There are currents If1 flowing out and If2 flowing into the faulted part of the array. Meanwhile, there are currents In1 flowing out and In2 flowing into the normal part of array, where In1 = In2.

Ground fault will create a ground fault path from the fault location to the system grounding point at the negative conductors. If the fault current flowing through the GFPD Ig = If1-If2 is above the pickup value, Ig might trip the GFPD and the fault can be isolated. The tripping of the GFPD will usually lead to subsequent tripping of the OCPD and the shutdown of the whole system. On the other hand, If the fault is a non-ground fault, the ground-fault current will be zero, where Ig = If1 - If2 = 0.

From a circuit analysis point of view, a grounding connection point, the positive or negative bus bar and the inverter can be treated as a node. In addition, if the working points of the arrays do not change too much during the fault, it is convenient to view each array as a constant current source from pre-fault to post-fault to carry out necessary circuit analysis.

The circuit analysis summary of our baseline schematic in Fig 4.12 is listed in Table 4.2. One example of using this approach is on ground fault blind spot detection, which is presented in next chapter.

Table 4.2 Summary of Circuit Analysis in Baseline Model

Node to Apply KCL at	Current Relationship
Ground-Fault Point	If2 – (If1 + Ig) = 0
Positive Bus Bar	(If1 – In1) – Ipos = 0
Negative Bus Bar	Ineg – (If2 + In2) = 0
At Inverter	Iin = Iout & Iin = Ipos
At GPFD	Iout + Ig – Ineg = 0

The second approach to DC fault analysis is I-V characteristic analysis. The I-V characteristic describes the behaviors of PV arrays, and it is a basic tool for normal and fault analysis. For the purpose of the fault study, the I-V curve in this thesis can either be simulated by MATLAB codes (shown in Appendix C) or obtained from fault data points directly.

In a faulted PV array with series-parallel configuration, the normal part and faulted part share the same operation voltage. According to the given I-V characteristics for PV arrays and array operation voltage, it is possible to derive the working points of normal and faulted parts of the array. Fig 4.13 shows the general procedure of this approach to analyze the occurrence of backfed currents in faulted PV string.

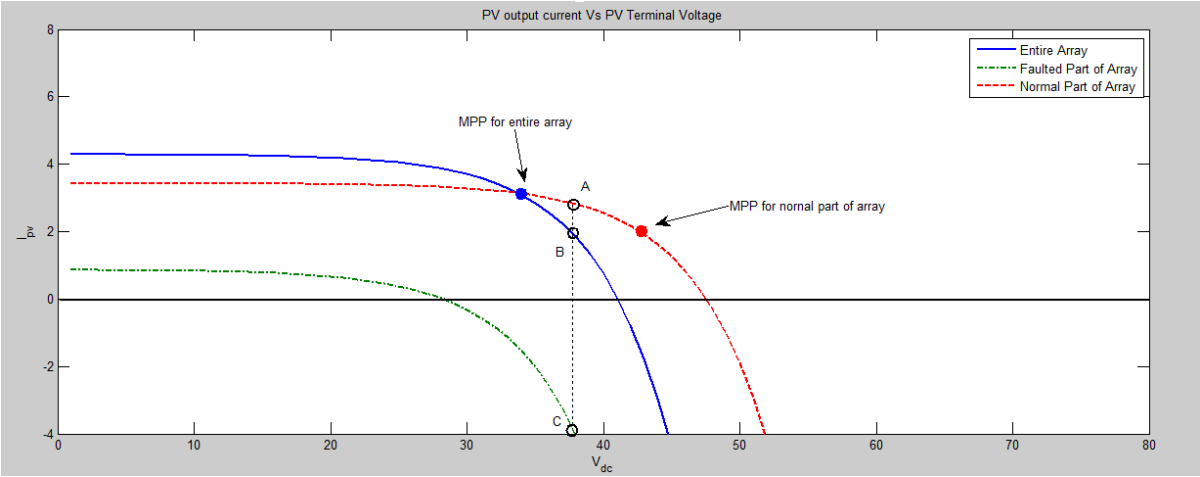

Fig 4.13 I-V Characteristics Analysis of Ground Fault with Backfeed Current

In Figure 4.13 we plot I-V curves for the entire array, the normal part of the array, and the faulted part of array. The faulted part and the normal part of the array must work at the same voltage, since they are in parallel with each other. But they do not have the same MPP anymore. The post-fault operation points of the normal part, the entire array, and the faulted part can be found at points A, B and C, respectively. It should also be noticed that the normal part will still have positive current even under fault conditions, but the faulted part of the array will have backfeeding current which may damage PV modules and cables.

The main reason for having fault current is that the I-V curve of the faulted string changes to a lower open-circuit voltage. However, the operating voltage of the array does not change immediately after the fault, since the MPPT in the inverter responds relatively slow compared to the fault. Therefore, the MPPT is keeping the system voltage relatively constant immediately after the fault. As a result, the faulted string must work in the 4th quadrant of its I-V curve as a load, instead of in the 1st quadrant as a source. If the fault happens on a clear day, or the fault location is on upper string, it is very likely that the backfeeding current becomes sufficient to trip the OCPD in series with the faulted PV string. The example of using this approach is the study of MPPT impact on the evolution of PV array fault current, which is also presented in next chapter [21].

4.3.3 RSCAD Simulation Verification

Fig 4.14 shows the schematic of the RTDS testbed used to simulate different fault types in PV arrays. As been discussed in the previous sections, the fault current depends on the fault type, fault location as well as the fault impedance. Therefore, the combination of possible fault locations and impedance needs to be included. The node on each module has been named in Fig 4.14 and fault impedance is chosen to be either 1Ω or 100Ω to represent bolted fault or high impedance fault. Low impedance fault can represent an accidental contact to equipment grounding point while high impedance may serve as a steady-state approximation of arcing fault. Here for convenience of analysis, we assume string #1 is the faulted string for ground fault and string #2 is the faulted string for line-to-line fault. The normal operating point of the entire array is set to be (277V, 5A) as reference.

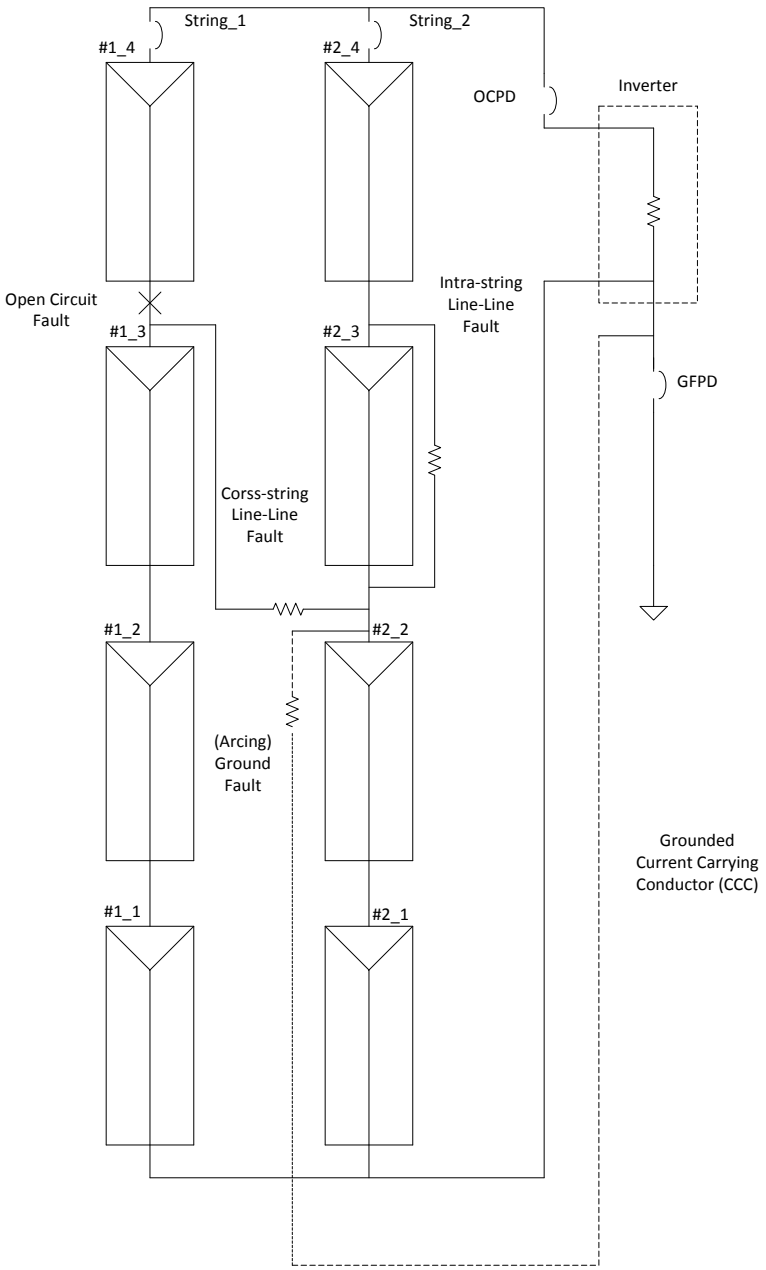

Fig 4.14 Schematic of the RTDS Testbed to Simulate Different Fault Types in PV Arrays

The ground fault current plot from simulation data are shown in Figure 4.15 and Figure 4.16. It is clear that the upper string fault will cause larger fault current than lower string fault, and that backfed current is likely to be seen when a solid ground fault occurs on the upper string. From a protection prospective, this type of fault should be cleared by the OCPD on the faulted

string if there is a large amount of reverse current. If not, the GFPD should operate and shunt down the entire system.

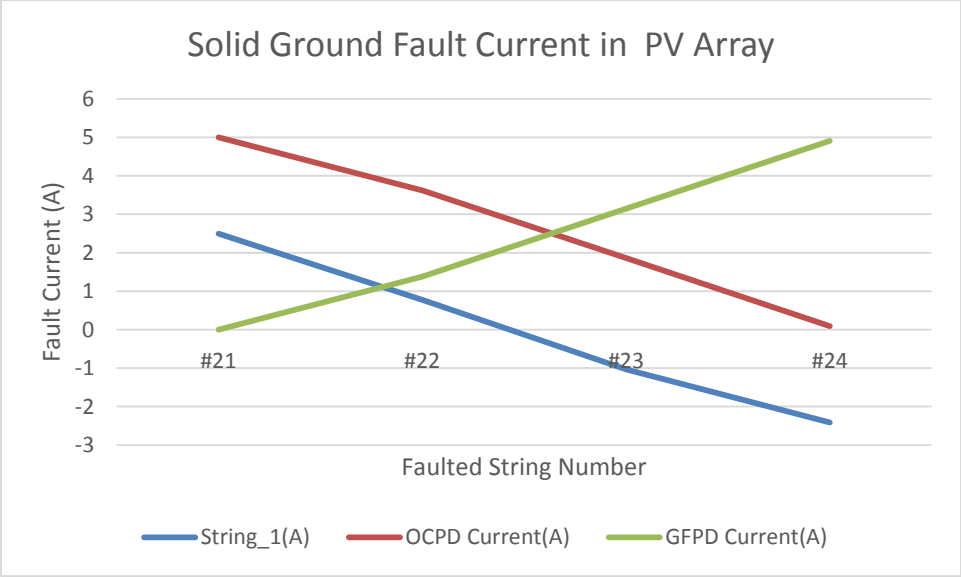

Fig 4.15 Summary of Solid Ground Fault in PV Array

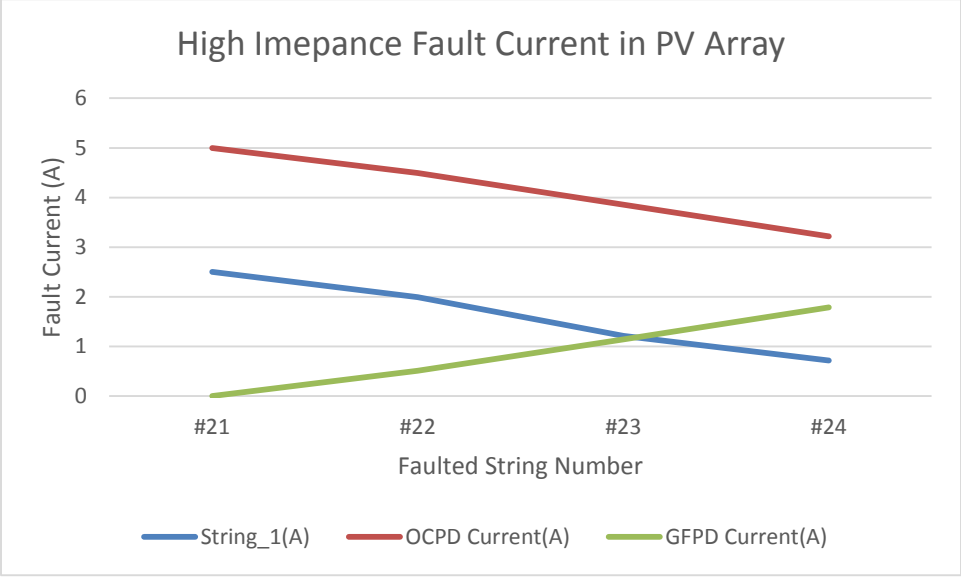

Fig 4.16 Summary of High Impedance Ground Fault in PV Array

For a line-to-line fault, a summary of simulation results are listed in Table 4.3, from which we can draw the conclusion that line-to-line fault in PV arrays does not lead to any fault current through the GFPD. On the other hand, intra-string faults can bring down the current level in the string but probably not be enough to trip any protection. However, cross-string faults may cause backfed currents if the fault sees very large voltage difference and with low fault impedance (See the fault data highlighted in yellow). From the protection prospective, this backfed current may trip the OCPD connected to the faulted string and make the cross-string fault evolve to an open-string fault, which has less impact on the PV system much like an intra-string fault. Usually the system can withstand these two types of fault and operate with a slightly lower efficiency.

Table 4.3 Summary of Line-to-Line Fault Current in PV Arrays

Fault Location	Fault Type	Fault Impedance (Ω)	Fault Current in String #1(A)	Fault Current in String #2(A)	Backfeed?	Current through OCPD(A)	Current through GFPD(A)	Fault Current(A)
2-21	Intra-String Fault	100	2.499	2.5	N	4.999	5.12E-06	7.95E-04
		1	2.499	2.499	N	4.999	5.46E-04	7.94E-04
2-22		100	2.293	2.511	N	4.805	0.00192	0.1959
		1	1.884	2.598	N	4.481	5.54E-04	0.5186
2-24		100	2.5	2.5	N	4.999	7.79E-04	0.001726
		1	2.562	1.931	N	4.493	2.99E-04	0.5073
2-12	Cross-String Fault	100	2.499	2.499	N	4.997	2.38E-04	0.001425
		1	2.499	2.499	N	4.997	8.57E-05	0.001319
2-13		100	1.993	2.5	N	4.492	0.001432	0.507
		1	1.118	2.503	N	3.621	9.44E-04	1.385
2-14		100	1.223	2.635	N	3.858	7.56E-04	1.142
		1	-1.006	2.868	Y	1.862	1.57E-04	3.132
2-23		100	2.307	2.5	N	4.808	0.001594	0.1934
		1	1.93	2.562	N	4.493	7.04E+04	0.5081
2-24		100	1.681	2.5	N	4.182	6.56E-07	0.819
		1	0.2622	2.5	N	2.762	2.11E-04	2.238
2-34		100	2.306	2.502	N	4.808	3.20e--4	0.1938
		1	1.931	2.561	N	4.493	0.001	0.5064

Chapter V: Fault Diagnosis of Arcing in Residential PV System

In recent years public awareness of arc faults has been growing tremendously. An arc fault is usually produced in residential electrical system. In many cases arcing can result in significant power loss as well as fire hazards.

An arc fault occurs when two exposed conductors at different electrical potentials approach or briefly contact each other. Rather than making firm contact, current flows via electrical breakdown of gas between the two conductors without a solid physical connection between the two conductors [13]. Arcing fault is different from fixed-impedance fault in that it usually requires a long-period degrading process for arcing fault to evolve to be detected by conventional devices. However, the initial 'high impedance' arcing can increase severe fire risks if not detected and cleared in time.

As far as the arcing type goes, the AC low-voltage arc fault and DC arc fault are discussed for the purpose of PnP auto-diagnosis function study. Both types of faults pose an extreme safety risk in existing residential PV system, due to the aging of the PV system components by environmental factors. A DC arcing fault must be detected before the fire happens and according to UL1699B, the system shall detect and interrupt arcing faults resulting from a failure in the intended continuity of a conductor, connection, module, or other system component in the DC PV source and output circuits. Another existing code which can be applied to AC arc fault in PV system is NEC Article 210.12, defines the AC Arc Fault detection device, which is tended to provide protection from the effects of arc faults by recognizing characteristics unique to arcing and by functioning to de-energize the circuit when an arc fault is detected [13].

Since details of arc faults can vary from system to system, there is no 'one-stop' computational analysis approach to study all types of arcing. For residential PV systems, a rigorous inspection is needed to make sure that wires are placed and secured so that no future arcing faults are likely to occur. However, the prevalence of residential PV system will require a faster process

to ensure meeting the UL 1699B standards. So if we don't rigorously inspect wiring, we need to make sure that we have good algorithms for arcing faults detection.

On the other hand, for arc detection algorithm development of research institutes, there is an obvious budget limit for field testing as well as safety concern. Therefore, a safer simpler method of conducting arc fault detection test is extremely important and the Power-Hardware-in-the-Loop approach is the way to go. This section will mainly discuss the details of implementing RTDS tedbed for arc fault detection in PV residential system.

5.1 Arc Fault Modelling in RTDS

There are many successful arc models that can be found in different simulation platforms. In general arc models include both microscopic models (particles physics) and macroscopic models (thermal, dynamic, electric). And electric models which are to be used in electrical system simulation can be divided into two types:

- Electrical behavioral models that mathematically describe the mechanism of the arc from an analysis of current and voltage.
- Models of impedance, where current and voltage are used as references to calculate the equivalent impedance of the arc.

A 'meta model' proposed in [14] has been developed in MATALB/Simulink environment (shown in Fig 5.1). The advantage of this model is the capability of including zero current crossing as well as corona effect during arcing process. In addition, 'meta model' can be treated as one 'plug and play' model, meaning that it can be applied directly to both DC arcing and AC arcing, both serial and parallel configuration without further modifications.

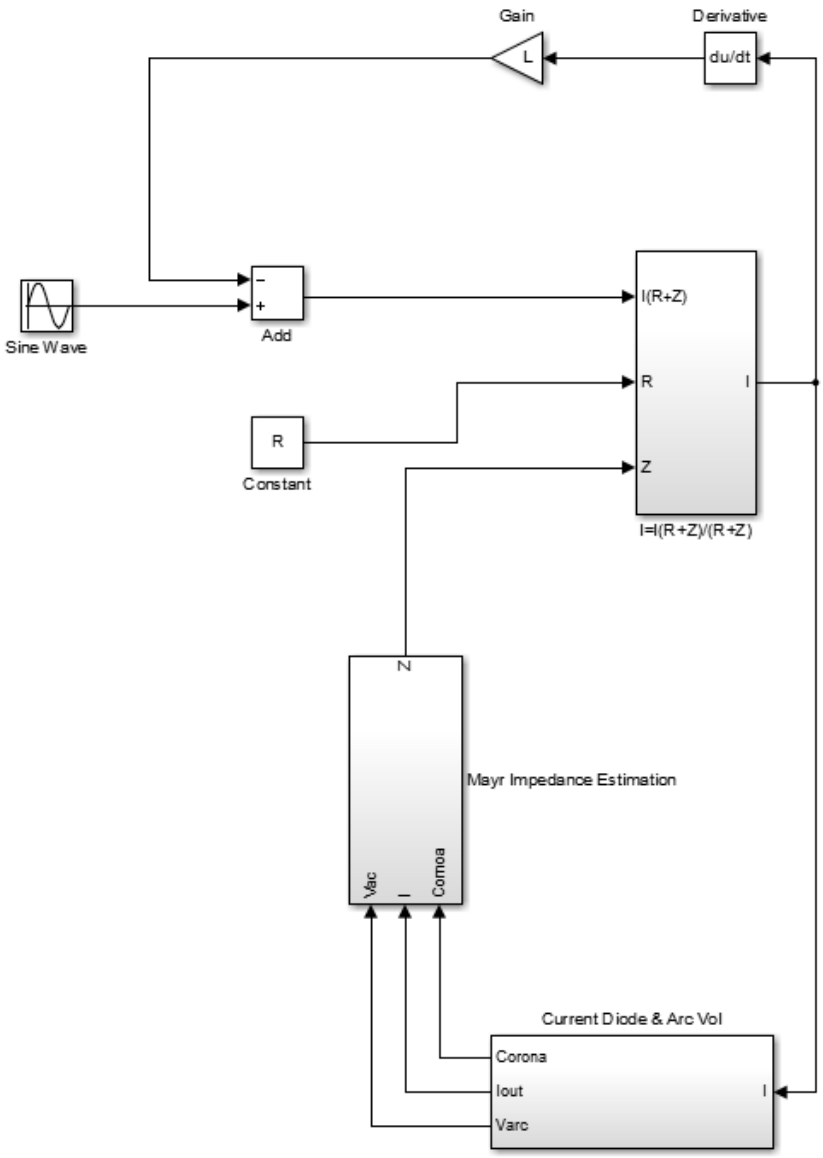

Fig 5.1 RSCAD Arc Fault Model Tested in Single-Phase AC System

The ‘meta model’ is ideal for pure simulation level verification as well as Opal-RT based HIL testing environment. However, for RTDS environment designed for PHIL test, it is not a desired model because of its heavy computation burden and pertinent unstable loop problem.

Therefore, in this thesis a compromise of simulation accuracy and computation burden has been made when we are developing a RSCAD-based arc fault model.

Previous work on DC arcs has shown that an arc is a highly nonlinear system, with a non-constant resistance. The current-voltage properties of DC arcs for systems with copper electrodes and air gap between 1 and 10 mm were investigated by [12] and can be described by the following equation:

$$V = 27.5 + \frac{44}{I^{0.67}} \tag{9}$$

A large amount of effort has been put into modelling low voltage AC arc faults. Due to the fact that energy consumed by low voltage arcing is relatively small compared to medium-to-high voltage arcing, the impact of arcing on voltage profile as well as steady state fault currents is usually very small at residential voltage level. The typical AC fault arc resistance R_{arc} can be obtained based on the Warrington expression:

$$R_{arc} = \frac{2.9\times10^{4}\cdot L}{I^{1.4}} \tag{10}$$

Where L is the conductor spacing, I is fault current.

Two nonlinear resistors are accomplished in RSCAD using a current-controlled voltage source with a voltage value equal to (9) and (10), named ‘DC Arc’ and ‘AC Arc Model’ respectively. The RSCAD detailed implementation of the arc fault model is shown in Fig 5.2.

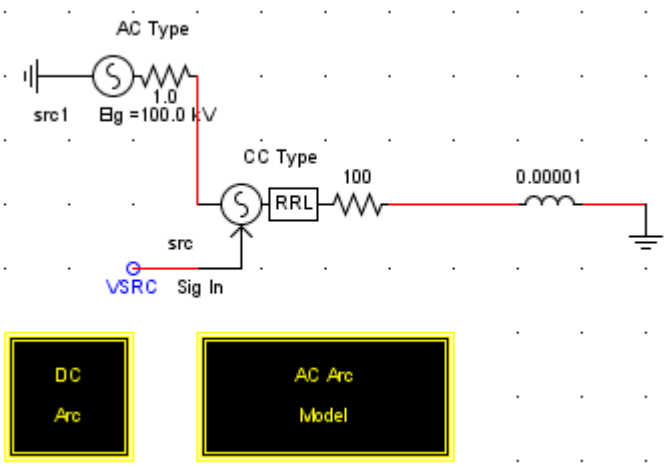

Fig 5.2 RSCAD Arc Fault Model Tested in Single-Phase AC System

Before being applied to a more complicated PV system, the model is tested in a single phase AC system to verify that there is no feedback problem, sampling problem or data overflow in RTDS system. The resulting waveform shows a large amount of flickers and distortion of the sinusoidal current (See Fig 5.3 and Fig 5.4).

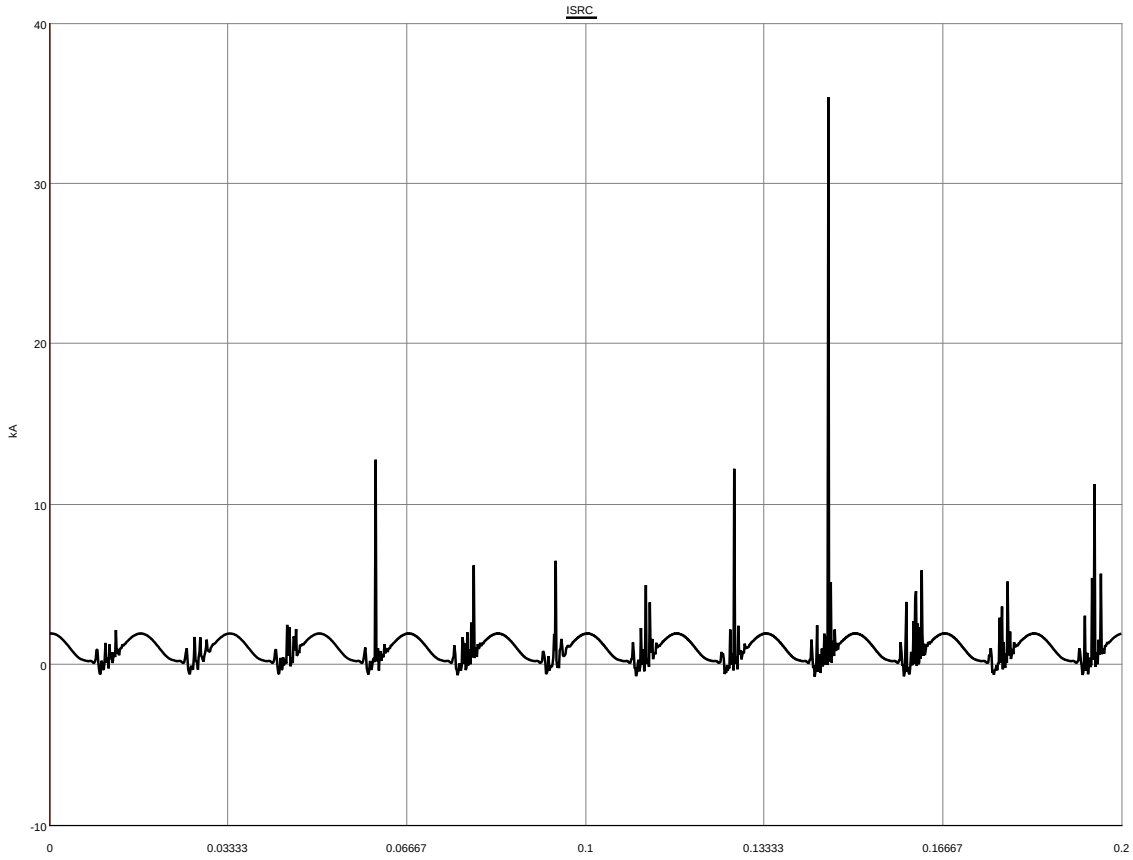

Fig 5.3 RTDS Arc Fault Current Waveform for Single-Phase AC System

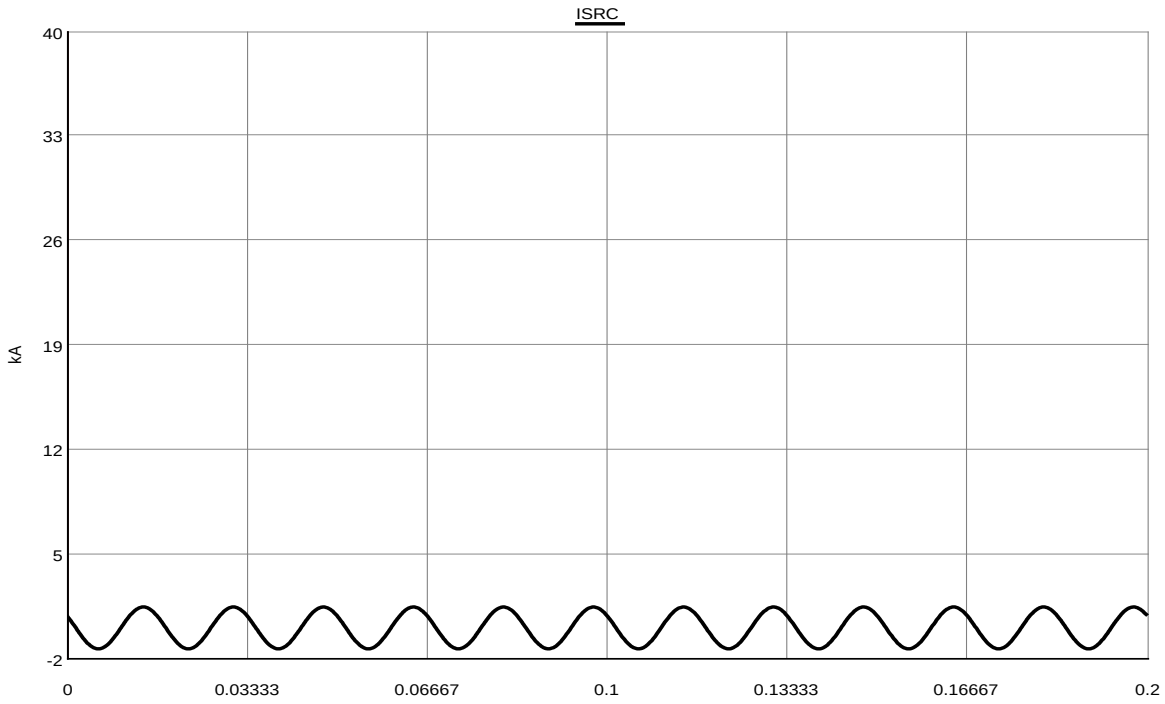

Fig 5.4 RTDS Pre-Fault Current Waveform for Single-Phase AC System

The arcing model was tested in different fault configurations and it is believed the model can serve as a hardware-in-the-loop version of arc-fault generator (AFG) [20] similar to the one used in UL 1699B to simulate arcing ground faults, series arc-faults in the string, intra-string parallel arc faults and cross-string parallel arc-faults.

5.2 Arc Fault Detection in Residential PV System

Today detecting arcing faults remains one of the biggest challenges for fault-diagnosis function implementation of PV systems. This is due to the fact that arc faults may nuisance trip on different inverter noise signatures. Inverter noise varies greatly between different manufacturer and model. In reality, the magnitude and excited frequencies of arc faults drastically vary between inverters due to differences in transistor switching noise, galvanic coupling from the AC side of the array to the DC, and maximum power point tracking behavior.

What makes arc faults simulation in a PV system different from other arc fault simulation is the presence of the PV inverter. In circuit analysis as well as software analysis, the PV inverter normally behaves like a current source instead of a voltage source. Therefore, the impedance model for arc faults discussed in the previous section must be used for the purpose of accuracy while the behavior model might not be able to perform correctly in this type of simulation.

The purpose of this simulation is to develop a feasible arc fault detection tedbed for constant arc fault in PV Residential System. A monitoring point has been a chosen to keep record of real-time current waveform (See Fig 5.5).

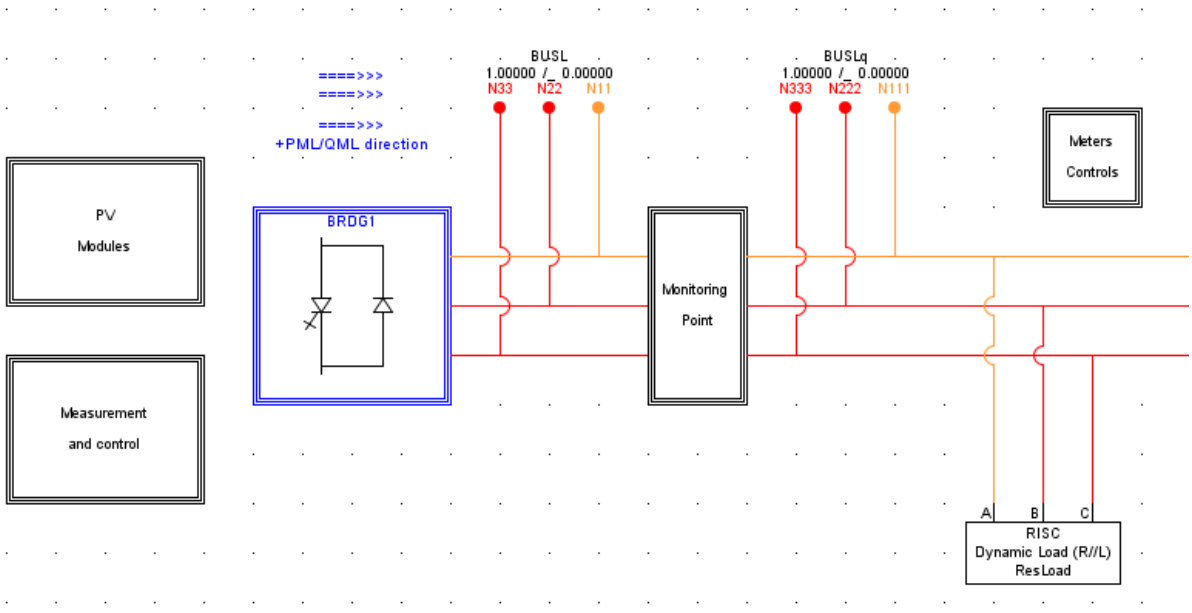

Fig 5.5 RTDS Testbed for Arcing Fault Detection

The following behavior should be recorded during the auto-inspection process. It is the baseline measurements to be established for system noise level.

An arc fault in the string generates 1/f pink noise on top of the DC current. The signal travels down the line through the system. As the signal passes through the PV modules and connectors, a variable attenuation occurs in the PV modules and changes the frequency profile of the

electrical noise as it propagates downstream. In addition, antenna effects, crosstalk and other RF phenomena further modify the signal profile and characteristics. Inverter noise is injected onto the PV string and inverter switching generates frequency and harmonics from 1 kHz to >100 kHz [13].

In our simplified testbed, due to the simulation capability only the switching frequency noise will be considered. This means that the noise component the Arc Fault Circuit Interrupter (AFCI) on the PV side will see is no different than the monitoring point on the AC side will see, except for the inverter switching noise. Therefore, the feasibility of arc fault detection is only evaluated at the proposed monitoring point in RSCAD.

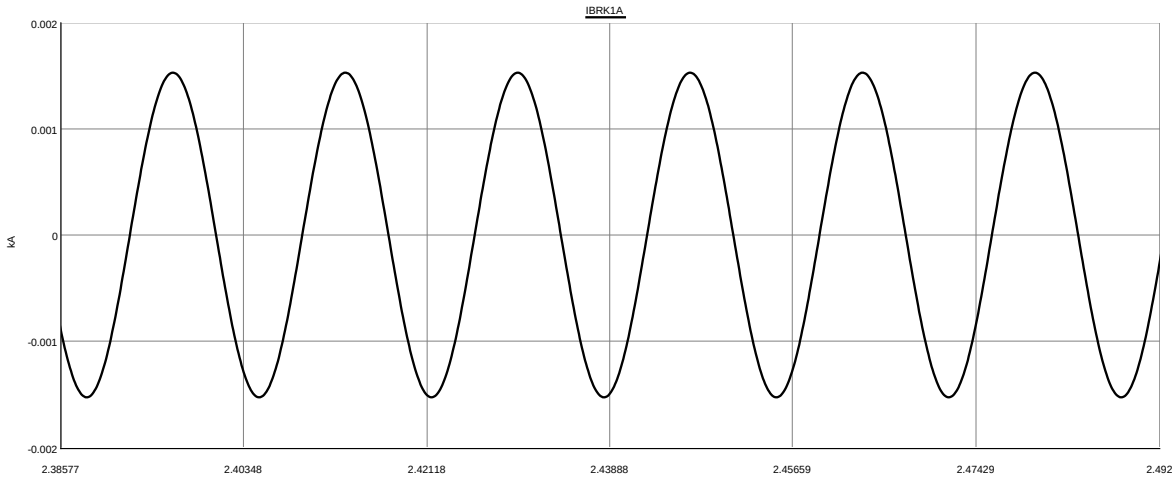

Fig 5.6 Pre-Fault RTDS Waveform of PV Residential System Current

Fig 5.6 represents the waveform of steady-state current from a residential breaker monitoring point. We choose the current capture after 3s as the baseline so that the start-up noise and MPPT control noise from the inverter are eliminated.

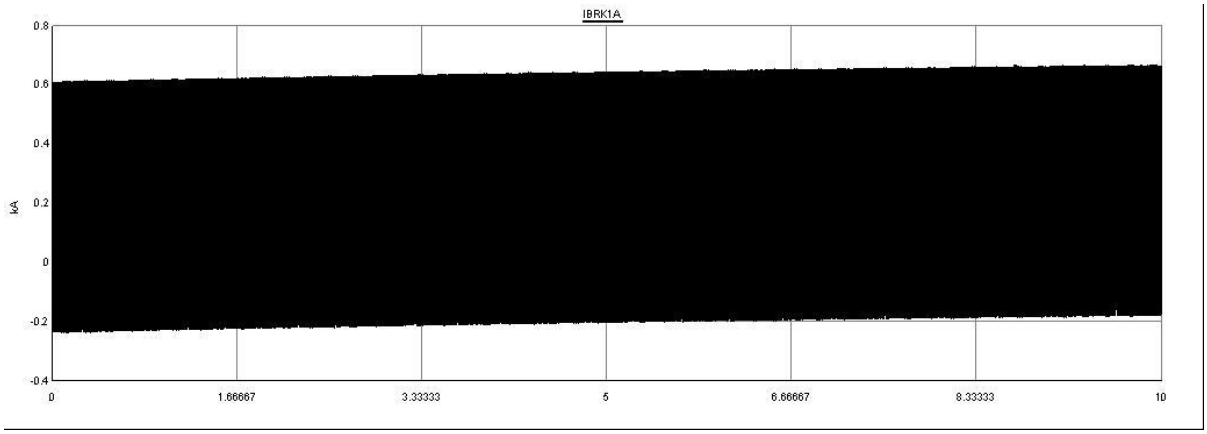

Fig 5.7 RTDS Waveform of PV Residential System Current after a Constant AC Arcing

Fig 5.7 represents the waveform after a constant AC arcing on the inverter side. It is clear that a noticable DC componnent can be moniored and analyzed to detect this type of fault.

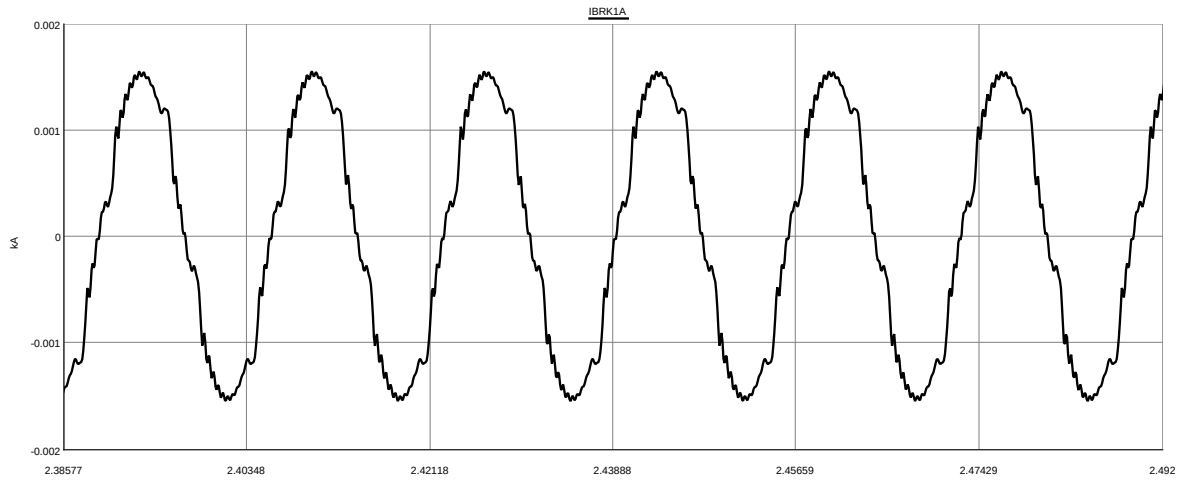

Fig 5.8 RTDS Waveform of PV Residential System Current after a Constant DC Arcing

Fig 5.8 represents the waveform after a constant DC arcing on PV side. A noticable high-order harmonic can be moniored and analyzed to detect this type of fault.

From the simulation results, it can be concluded that it is possible to detect arc faults in PV system using waveform analysis like FFT or DFT, but very complicated when it comes to a threshold setting for arc fault determination [13]. The detailed discussion of arcing detection algorithm is not present in this thesis and will be focused on an associated project.

In this section a safe method for creating arcing faults in small residential PV system on the RSCAD tesdbed was developed. To evaluate the feasibility of arc fault detection algorithm, plots from real-time digital simulation were obtained and used for basic FFT analysis. With proper assumption regarding system noise being made, it can be concluded that a harmonic-based arcing fault detection method can reliably work in our proposed PnP system.

Chapter VI: Advanced Topics of Fault Diagnosis in Residential PV System

In order to represent the actual response of PV system to different types of faults, there are a few unique problems that we need to take into consideration. An all-around functioning Plug and Play PV system should be capable of detecting these underlying 'pre-fault' situations, including ground fault bind spot and nuisance tripping caused by MPPT control. This chapter introduces a general consideration for potential wiring protection as well as smart monitoring in residential system.

6.1 Ground Fault Blind Spot Detection

The blind spot occurs when the ground current carrying conductor (CCC) is faulted to the equipment grounding conductor (EGC) [12]. Sometimes the blind spot fault may produce very small fault current that can go undetected by GFPDs. The resulting energized EGC can be a shock hazard and even worse, if there is a second ground fault, the array can be shorted through the EGC, bypassing the GFPD and allowing fault current to flow undetected through the system with no means of interruption. One important fact to be note is that field experiments by Sandia National Laboratory have confirmed the unique existence of the ground fault blind spot only in grounded systems, meaning this type of fault does not exist in ungrounded, non-isolated or hybrid systems.

The goal of the study in this section is to develop an analytical approach to solve this type of problem and modify the RTDS tedbed to simulate blind spot events.

6.1.1 Detailed Modelling of PV System in RSCAD and Blind Spot Event Simulation

It is necessary to introduce a more detailed model of the PV system before we can carry on the circuit analysis of ground fault blind spot.

To model current flow during a ground fault, the internal resistances of the conductors and the GFPD must be included because the current division between the fault path and the intended

conduction path is heavily dependent on small internal resistances. In the ideal case, fuse ratings could be decreased freely without affecting the GFPD current.

Leakage current is another crucial factor that determines the GFPD current. While there is current leakage from a number of places in the array, the primary source of leakage is in the modules. Module leakage current is defined as current between the module, biased at some high voltage, and the grounded frame. Leakage current measurements are described by IEC 61215 (section 10.15.3) and UL 1703 (section 21.5).

For the purpose of the RSCAD simulations, a variety of module leakage resistance values were chosen because these values change due to ambient weather conditions (rain, due, humidity, etc.), module technology and age. Values of leakage currents for different fielded arrays are presented in the Solar ABCs paper, "Final Report: Examination of Inverter Ground-Fault Detection 'Blind Spot' with Recommendations for Mitigation" [12].

The current leakage from any single module in an array may be described by:

$$I_{leak}^{module} = \frac{V}{R_{leak}} \tag{11}$$

Since the resistance of R_{leak} is modeled as the same value for each module, the leakage current will be greatest for modules at the top of the string with the highest voltage to ground. The module voltage above ground increases with the number of modules in a string. In an unfaulted array, each module is at an electrical potential V_{mp} higher above ground than the module below it. Therefore, the module leakage per string is dependent on the number of modules in the string, M, by:

$$I_{leak}^{string} = \sum_{i=1}^{M} \frac{i \cdot V_{mp}}{R_{leak}} \tag{12}$$

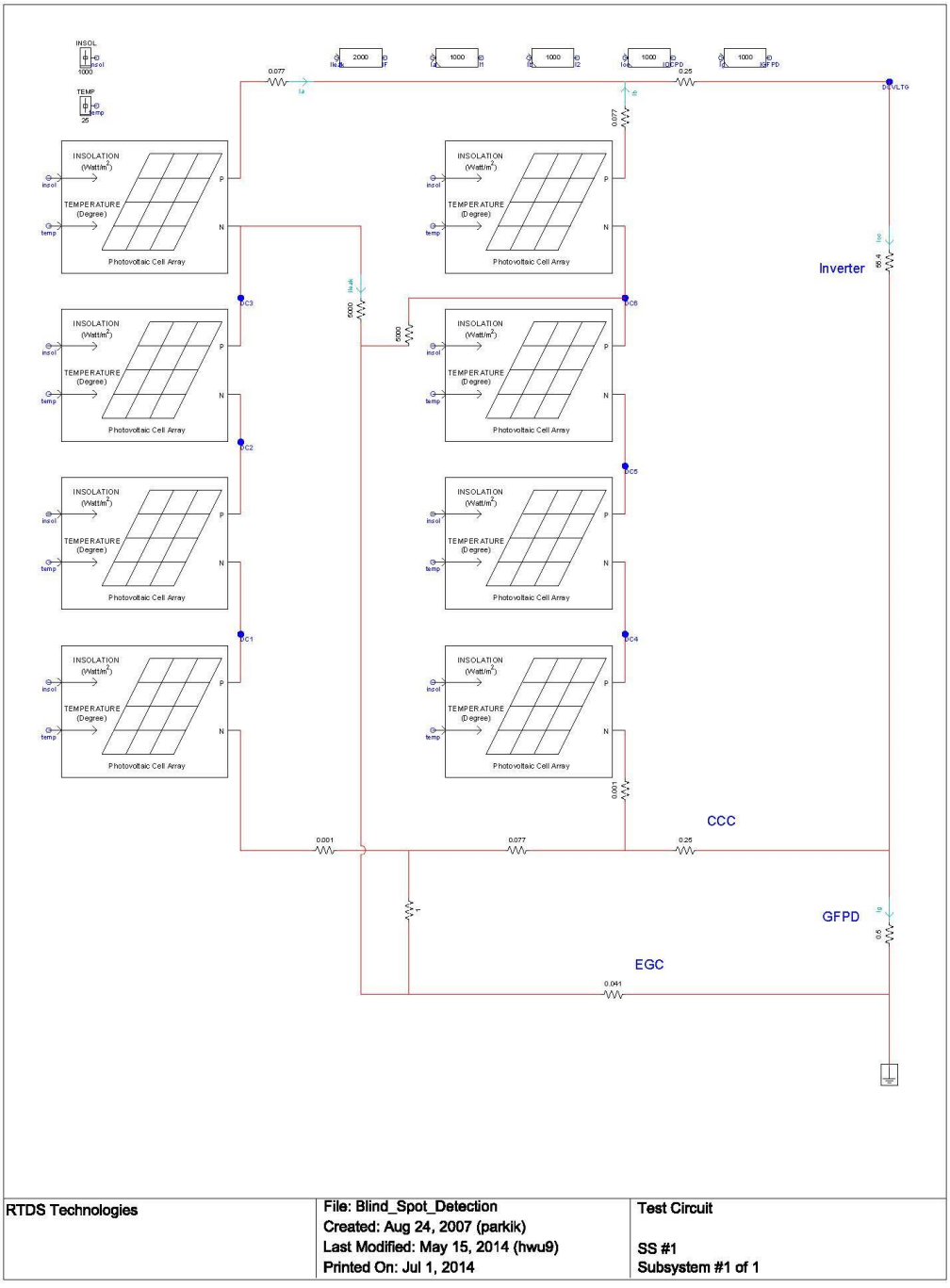

Fig 6.1 Modified RSCAD Testbed for Ground Fault Blind Spot Simulation

A modiefied RSCAD testbed was created with the internal resistance of the conductors and GFPS fusing, as shown in Fig 6.1, in order to investigate ground faults involving the grounded CCC. Each string was composed of four modules having a leakage current to ground determined by R_{leak}. The DC cable resistance connecting the PV array to the combiner box sums up to 0.25Ω (80 ft of coated copper 12 AWG cabling). Prior to each string being combined, the positive DC cable was connected to the inverter through cabling with an impedance of 0.00165Ω (50 ft of coated copper 400 kcmil cabling). The ground fault was modeled by a resistor connected from the negative CCC to ground through the 0.045Ω EGC. For the faulted string in Fig 6.1, the PV cabling resistance was split by the fault. This was done so that, by altering the resistance before and after the fault, the fault location in the faulted PV cabling could be varied. The value of inverter resistor was set to the max power point of the unfaulted array. The negative inverter connection was connected to ground through the GFPD. The fault impedance is chosen to be either 1Ω or 50Ω. A summary of RSCAD simulation results is shown in Fig 6.2.

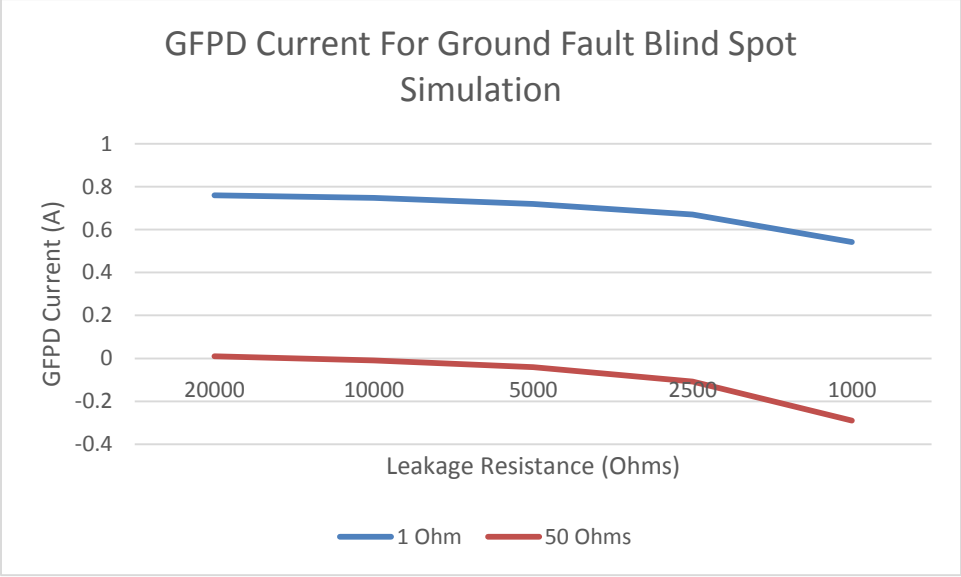

Fig 6.2 Summary of GFPD Current In relation to Fault Impedance and Leakage Impedance

It can be seen that the fault current level is below 1A under all fault situations so that the operating points of the modules do not move from MPP too much due to the blind spot fault. It should also be noted that the fault current is in the opposite direction of the leakage current, which indicates that in arrays with large leakage currents, it is more difficult for the GFPD to detect a blind spot ground fault because the fault current must first reverse the leakage current. The results also show that, for most fault resistances the leakage current has little effect on the GFPD current. At very low values of R_{fault}, there is a slight dependence of leakage current on GFPD current.

Due to the difficulty of detecting ground fault blind spot, the use of harmonics signature analysis for fault current has also been conducted. For the purpose of consistency and economy, we try to evaluate the feasibility of using the same testbed and monitoring spot as for the arcing fault study. The post-fault current waveform obtained from the inverter AC side is sent to the RSCAD Fourier analysis tool (See Fig 6.3 and Fig 6.4). Results show that that there is no more than 10% harmonic distortion difference between pre-fault condition and blind spot ground fault condition. Therefore, with the given metering error rate and inverter switching noise which might count up to 10% uncertainty of data, it is probably not feasible to detect the PV blind spot ground fault simply by use of inverter-side harmonic analysis tool.

On the other hand, recently some micro inverter manufacturers like Enphase have developed a new micro inverter family under 250W with integrated (DC isolated) ground. Because the DC circuit is isolated and insulated from ground, this type of PV system without Grounding Electrode Conductor (GEC) will eliminate ground fault blind spot problem. [3]

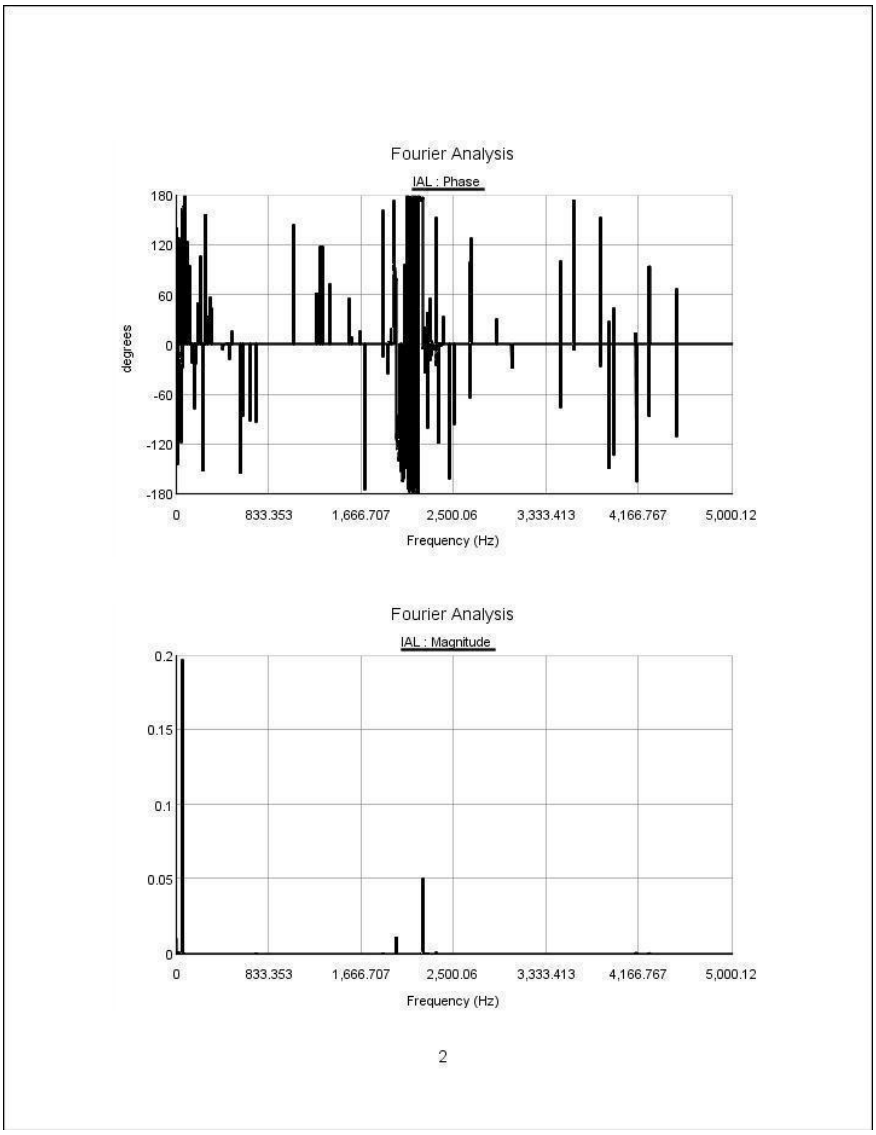

Fig 6.3 Harmonic Analysis of Pre-Fault Current on Inverter AC side

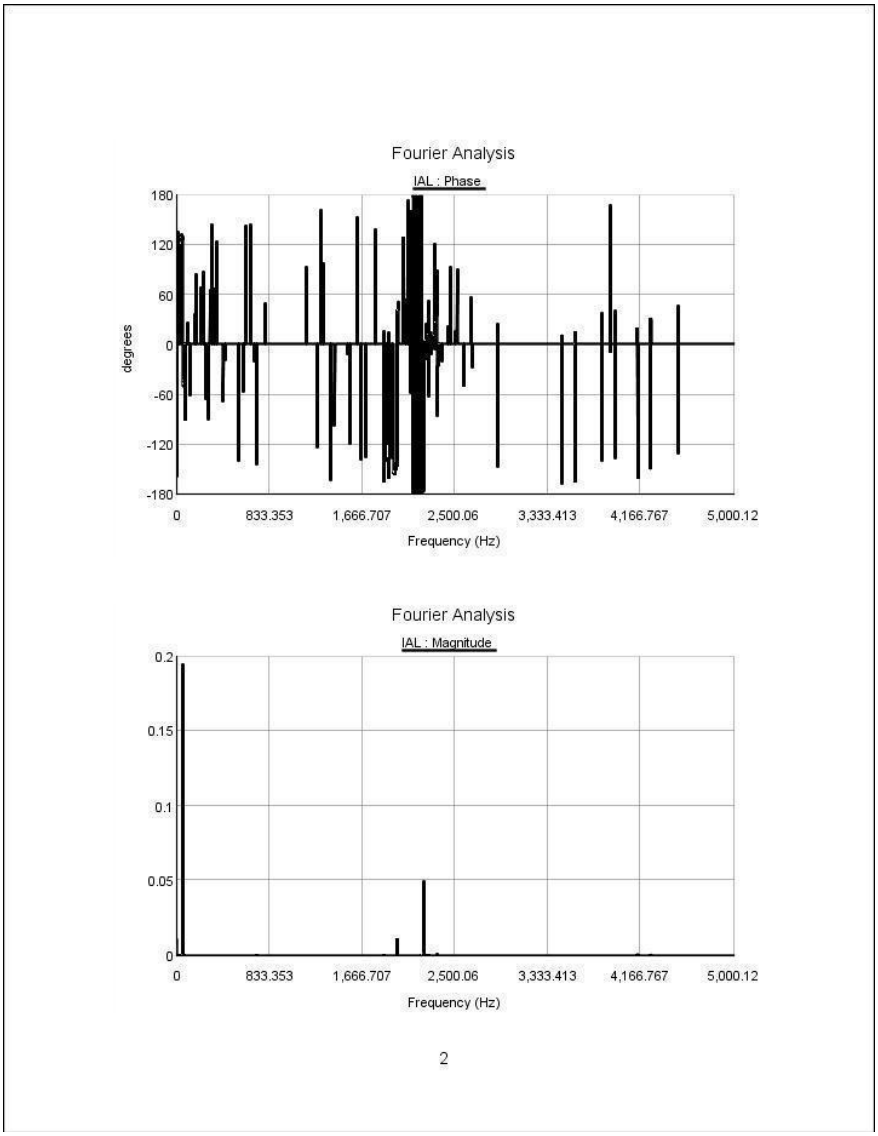

Fig 6.4 Harmonic Analysis of Blind Spot Ground Fault Current on Inverter AC Side

6.1.2 Analytical Solution to Ground Fault Blind Spot and RSCAD Simulation Validation

Through circuit analysis, the GFPD current can be shown to be a function of module maximum power current (I_{mp}), number of strings (C), wring resistance (R_{comb}, R_{EGC}), resistance of the faulted potion of the PV cabling (R_x), and the array leakage current (I_{leak}).

The circuit diagram in Fig 6.5 shows the current paths for negative CCC fault of an array with a number of parallel strings.

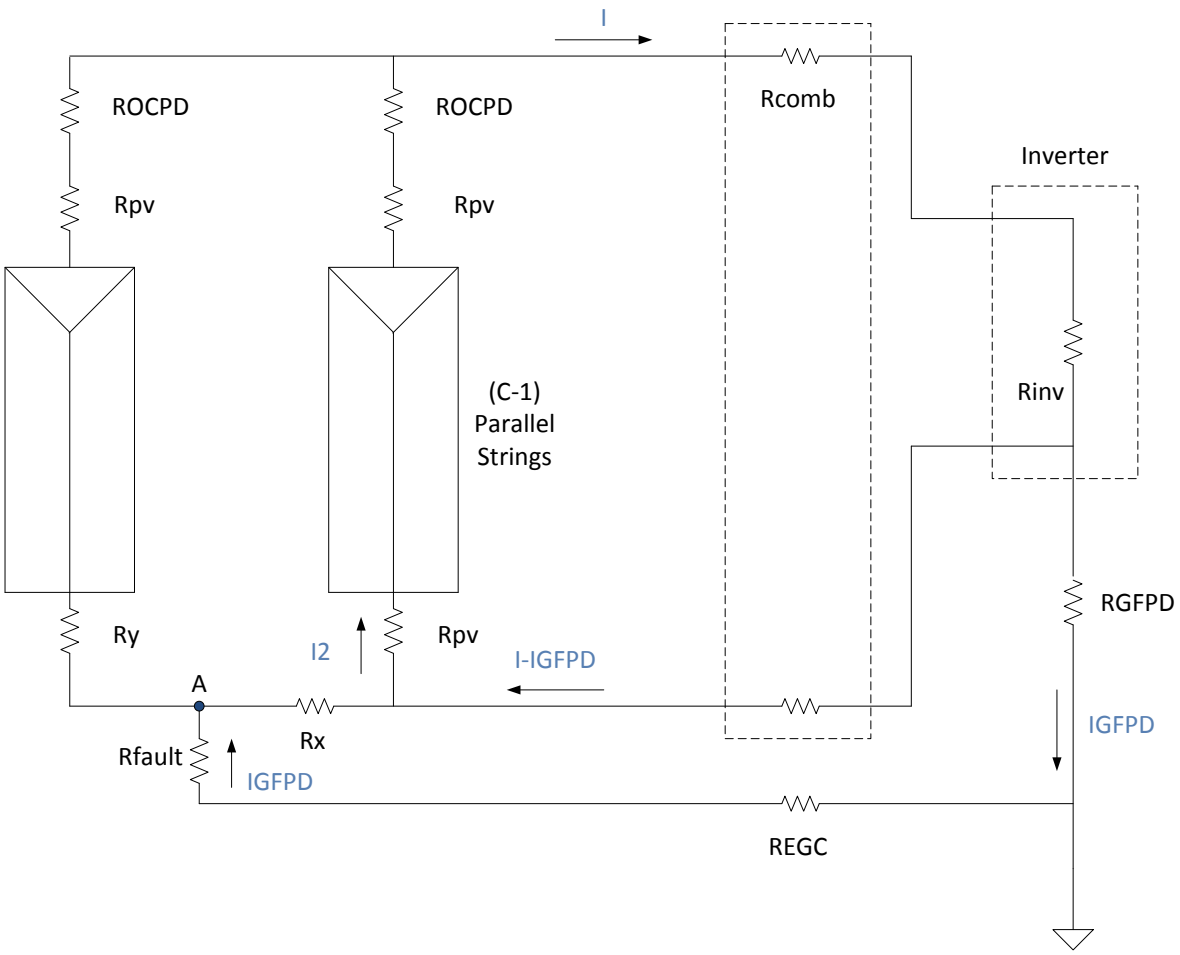

Fig 6.5 Circuit Diagram for Blind Spot Fault Current Path

The location of the PV modules on their IV curve is nearly unchanged due to the blind spot fault, so the string current is treated as constant in the following analytical analysis. By KCL and KVL,

$$(I - I_{GFPD}) \cdot R_{comb} + I_1 \cdot R_x = I_{GFPD} \cdot \left(R_{GFPD} + R_{EGC} + R_{fault}\right) \quad (13)$$

Combined with,

$$I = C \cdot I_{mp} \tag{14}$$

$$I_1 + I_{GFPD} = I_{mp} \tag{15}$$

Gives,

$$I_{GFPD} = \frac{I_{mp} \cdot (C \cdot R_{comb} + R_x)}{(R_{GFPD} + R_{EGC} + R_{fault} + R_{comb} + R_x)} \tag{16}$$

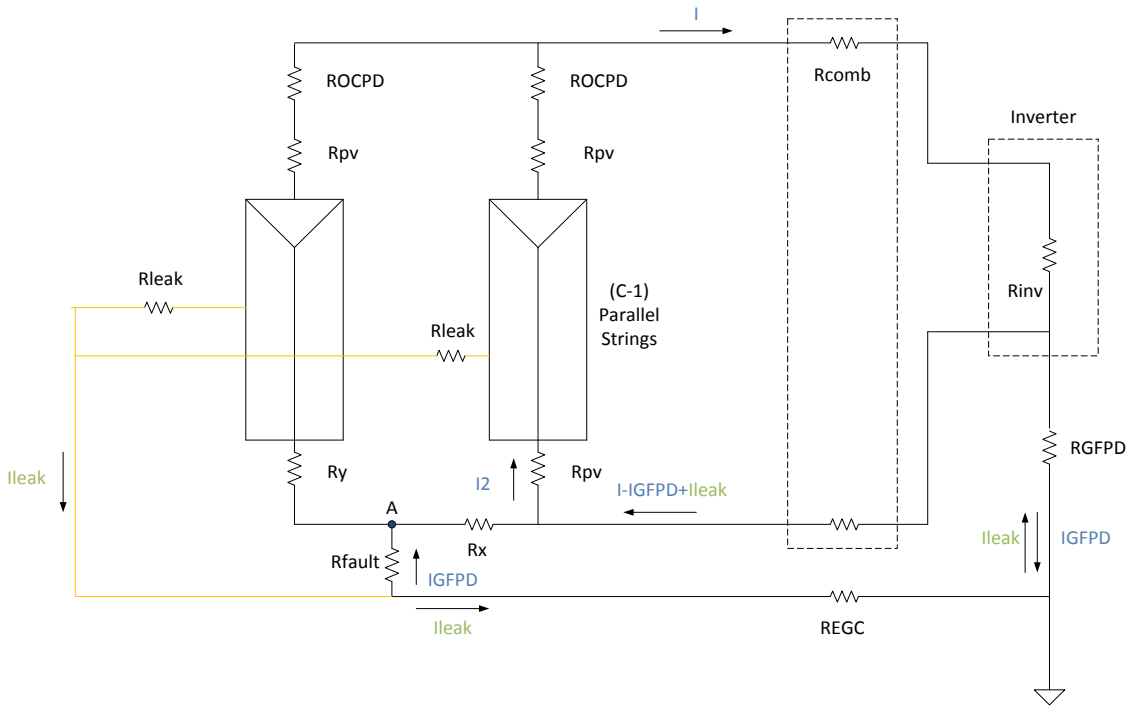

Fig 6.6 Circuit Diagram for Blind Spot Fault Current Path with Module Leakage Current

If we also include the string leakage current I_{leak} path shown in Fig 6.6, the KCL and KVL equation should be modified as:

$$\left(I + I_{leak} - I_{fault}\right) \cdot R_{comb} + I_1 \cdot R_x =$$

$$\left(I_{fault} - I_{leak}\right) \cdot R_{GFPD} + \left(I_{fault} - I_{leak}\right) \cdot R_{EGC} + I_{fault} \cdot R_{fault} \tag{17}$$

And the current flowing through the GFPD becomes,

$$I_{GFPD} = \frac{I_{mp} \cdot (C \cdot R_{comb} + R_x)}{(R_{GFPD} + R_{EGC} + R_{fault} + R_{comb} + R_x)} - I_{leak} \tag{18}$$

Therefore, because of the existence of leakage current, the fault current through GFPD may go completely undetected ($I_{GFPD} = 0$) under certain circumstances.

6.2 Challenges for Protection Design in Plug and Play System

In this section the RTDS simulation results obtained from previous chapters has been summarized to provide a discussion on current challenges for protection design in future Plug and Play system.

NEC 690.9 requires overcurrent protection for PV circuits in order to prevent conductors from exceeding their rated ampacity and starting fires. In the case of systems with three or more strings, overcurrent fuses are required for each of the strings and typically selected to be the next highest fuse rating above 1.56Isc (125% of the string current, defined as 125% of the module short circuit current). This section seeks to summarize the protection issues for faults in PV array and highlights three main concerns for PV system protection design.

The coordination between OCPD and GFPD stands out to be the main challenge for improving reliability of the system. Generally speaking, the GFPD is responsible for protecting against ground-type of fault while the OCPD is used to protect against a line-to-line fault with large backfed current.

For a ground fault, if the OCPD possesses a smaller rating than the GFPD, it is possible for the OCPD to open before the GFPD, even though more current flows through the GFPD ($I_{GFPD} = I_{OCPD} + I_{SC}$). Which fuse will clear is dependent on the characteristic time-current curve of the device.

For GFPD design, it was demonstrated that an IEC-compliant module leakage would not cause nuisance tripping. This means that the rating of GFPD should not be too stringent for the sum of module leakage current. On the other hand, protecting the system from line-to-line fault requires a relatively narrow rating of the OCPD between the normal current and the faulted backfed current. Therefore, the design considerations of the GFPD and the OCPD altogether may bring two coordination scenarios for the PV system:

- The GFPD clears the fault before the OCPD.

It indicates that a small (less than string Isc) GFPD rating should be used and the characteristic clearing time of the GFPD should be less than the OCPD. This is the conventional and probably most common coordination in existing PV system. The drawback of the coordination is the loss of dependability since any type of ground fault will trip the GFPD and lead to a complete shutdown of the system, which may cause a power shortage on the residential-side for a time period as well severe power quality issue before the fault is fixed. In addition, to accommodate the GFPD setting, the OCPD rating is raised to some extend so that the sensitivity of detecting line-to-line fault is decreased.

- The OCPD clears before the GFPD when large backfed current flows through the faulted string.

  When ground fault with large backfed current happens, the fault path is no longer being fed with the other strings, but there is still a fault path through the GFPD. The modules above the fault are effectively at Voc while the modules below the fault (C) are effectively short-circuited. These short-circuited modules continue to source current through the fault and the GFPD, though the magnitude of the current is equal to Isc. Since this new fault current is much less than the GFPD trip point, the fault will persist. This type of coordination is well suited for PV arrays with multiple parallel strings because the reliability of the whole system is greatly improved. However, for PV arrays with very few strings, this type of coordination will heavily depend on the capability of the inverter control as well as local energy storage devices because the post-fault operating point of the entire array is changed. Nevertheless, this type of coordination should be considered as the ideal choice for a future Plug and Play system. After adding a counter or fault current indicator at the OCPD, any fault type resulting in large backfed current will be detected, cleared and well indicated without causing too much impact on residential load.

The second concern in designing GFPD is that reducing GFPD fuse ratings actually reduces fault protection sensitivity. In the ideal case, fuse ratings could be decreased freely without affecting the GFPD current. However, in reality, fuse impedance is correlated to fuse rating.

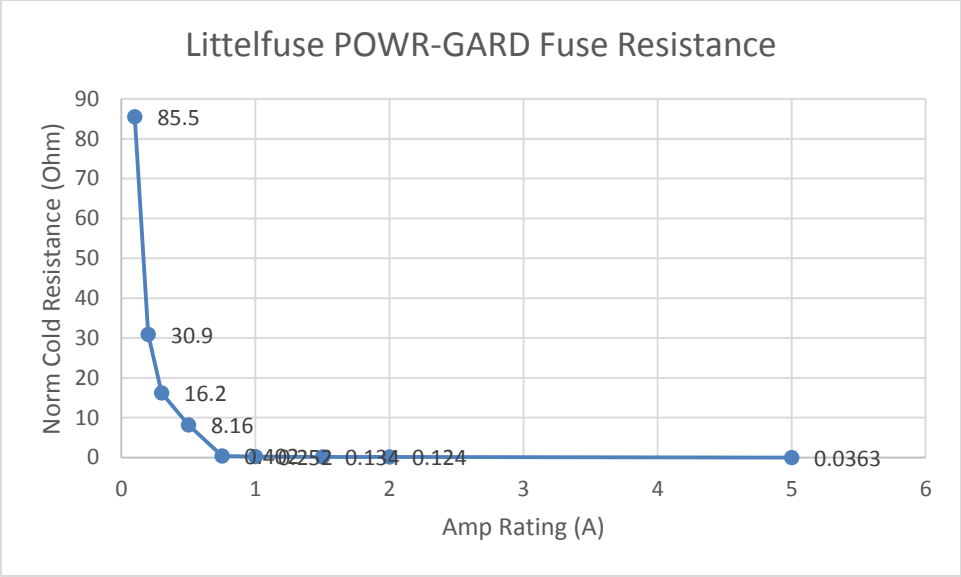

Fig 6.7 Littelfuse POWR-GARD Fuse Resistance with Amp Rating Difference

From Fig 6.7, it is shown that the resistance of the fuse is inversely proportional to the fuse rating so fuses with low ratings can have significant resistance. For example, the Littelfuse fuse has a resistance of 85.5Ω for a 0.1A fuse. Such large resistance can have significant effects on the GFPD current and fuse resistance must be balanced with fuse trip point in order to maximize GFPD fault detection capabilities.

Last but not least, the fault impedance proves to play an important role in determining the resulting fault current. Unfortunately, there is little known about the probability or progression of different impedances. With better understanding of the distribution of ground faults resistances, the fuse ratings could be selected for specific percentiles of protection. Without this knowledge, PV system designers are left to try to protect for as many fault cases as possible. This said, it stands to reason that undetectable, high-impedance faults will degrade over time, reducing their impedance to the point of detection. For this reason, it may not be critical to detect the high-impedance faults, as the currents produced by the fault in the EGC are not sufficient to cause injury and may eventually become detectable.

6.3 Impact of MPPT Control on Fault Diagnosis Function

MPPT is an algorithm which is generally integrated with the inverter to harvest maximum power output for given irradiance and temperature. The most common MPPT algorithm is the Perturb and Observe (P&O) method, which is implemented in the RTDS testbed. Fig. 6.8 shows the P-V curve of a PV array which has a maximum power point (MPP). The P&O perturbs the operating voltage of an array in a certain direction and observes changes in its output power. From Figure 6.8, it can be seen that if the change of power is in the same direction of voltage perturbation (dP/dV>0), then the operation point is on the left of the MPP, and the operating voltage will be increased to reach the MPP. If the change of power is in the opposite direction of the voltage perturbation (dP/dV<0), then the operation point is on the right of the MPP and the operating voltage will be decreased to reach MPP. The P&O algorithm is processed iteratively until the MPP is reached. The PV array will oscillate around its present MPP in steady-state operation [22].

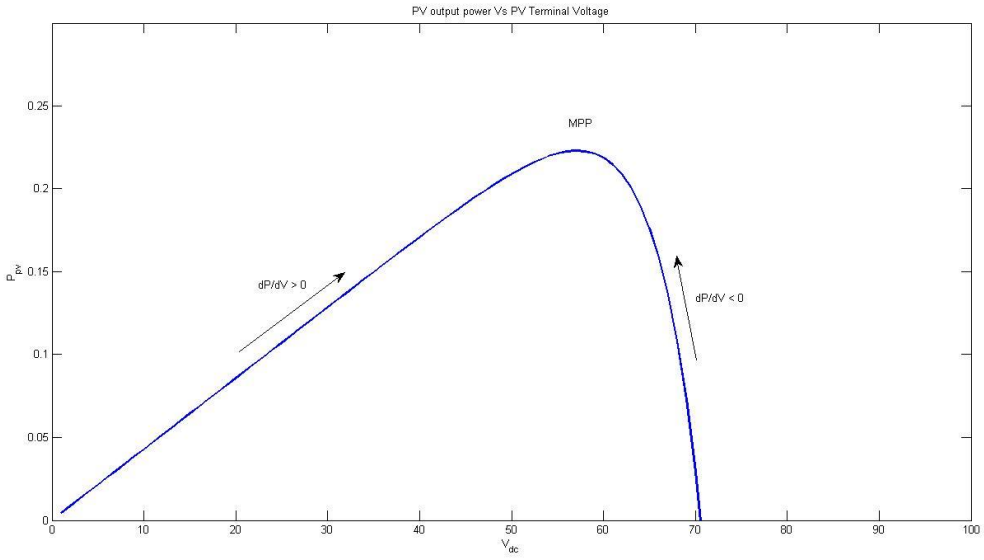

Fig 6.8 Pre-Fault RTDS Waveform of PV Residential System Current

The MPPT plays an important role in determining the normal current as well as the fault current. This leads to new protection issues in PV arrays that have not previously been documented.

Generally during the fault, as long as the MPPT is still working, the MPPT helps the PV array work as maximum power point and therefore, clips the fault current in the PV array to a small value. This feature of the MPPT may result in hidden fault currents within a PV array and bring new challenges to existing conventional protection devices.

Simulation of typical faults has been carried out in the proposed residential PV system RSCAD model (shown in Fig 6.9). The supported cases include solid ground fault, high impedance ground, line-to-line fault and intra-string fault.

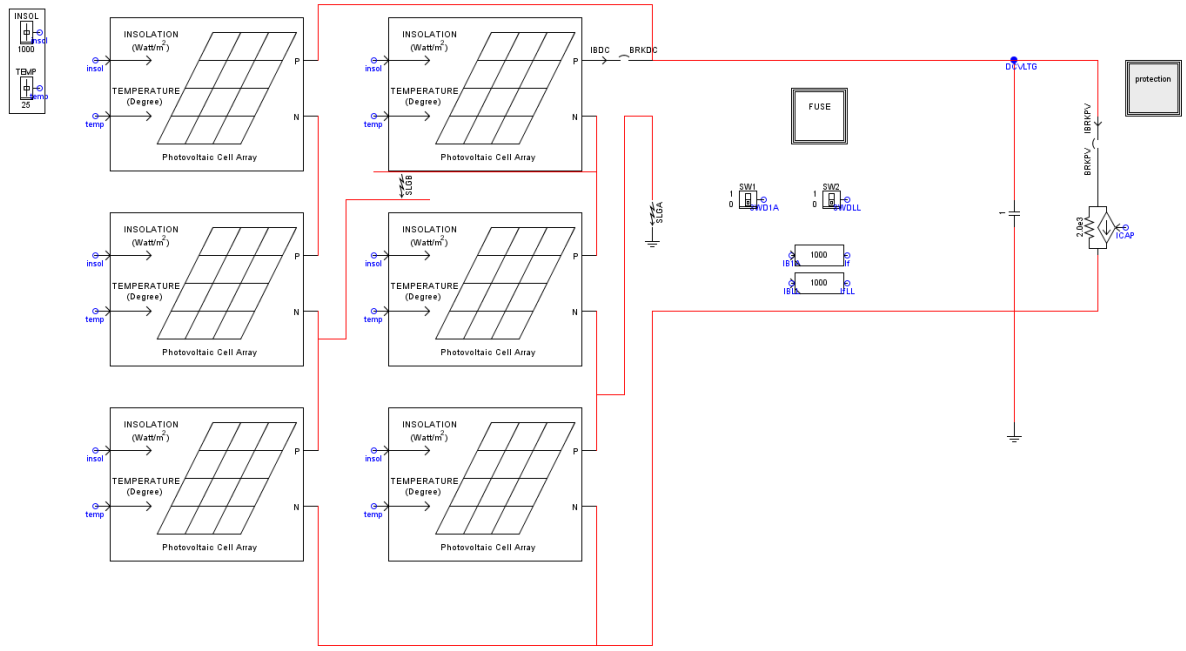

Fig 6.9 Schematic of Different Fault Types in PV Array under RSCAD

Instead of listing all simulation results, here we focus the case of a low impedance ground fault to study the impact of MPPT control, since the backfed current flowing through the OCPD is

most likely to be seen in this case. Therefore, development of a new protection algorithm should probably use this type of fault as a baseline.

In the study case, an upper string ground fault is simulated in the RSCAD-based benchmark system. In simulation, the ground fault impedance is set to 5Ω and the fault is triggered after 10s of inverter normal state operation. To fully understand the evolution of fault current, the operation of OCPD and GFPD is disabled so that the fault can evolve without interruption.

First I-V characteristics analysis is presented to derive the PV working points for the PV array during the fault, which is shown in Fig 6.10.

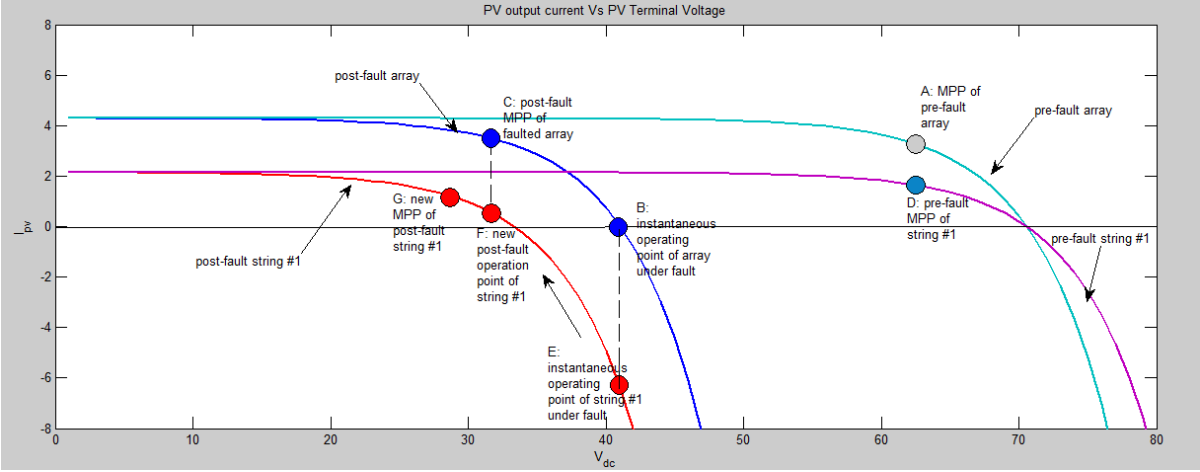

Fig 6.10 Schematic of Different Fault Types in PV Array under RSCAD

Before fault occurs, the PV array operates at its optimum point ‘A’. When the fault occurs at t = 2s, the operating point of the array drops to ‘B’ instantaneously. At the same time, the output current and power are both zero, since all the normal strings are backfeeding current into the fault string (String #1). Meanwhile, the faulted String #1 operates instantaneously at point ‘E’ under fault from pre-fault MPP ‘D’. It is noticed that the faulted String #1 has a large backfed current from other strings that may damage modules and cables and will usually cause OCPD tripping within a preset time slot. The MPPT will detect the sudden drop of output power and begin to optimize the output power of the array. The MPPT will decrease array voltage in order

to reduce the reverse current and power losses in the faulted string. As a result, the PV array's operation point is from 'B' to 'C' gradually. With the help of the MPPT, the operation point of the faulted string is changed from 'E' to 'F' with positive current. However, the faulted string cannot work its real MPP 'G' anymore, since it is mismatched with other strings due to the fault.

At the beginning of the upper ground fault, the faulted PV String #1 has the large reverse string current and works as a load in the 4th quadrant of the I-V characteristics. If the faulted evolves without interruption, the MPPT can help the faulted PV array operate at new MPP, then the faulted string can generate power again.

The simulation results have been summarized in Table 6.1.

Table 6.1 Simulation Results of 5Ω Upper String Ground Fault in RSCAD with MPPT Impact

Upper ground fault	**Fault current (A)**	**Current though OCPD (A)**	**System efficiency**
When fault occurs	54.74	-17.76 (Backfeeding Current)	0
Post-fault steady state	43.53	1.47	19%

The simulated fault current and OCPD current in RTDS testbed are given in Fig 6.11 and Fig 6.12 respectively.

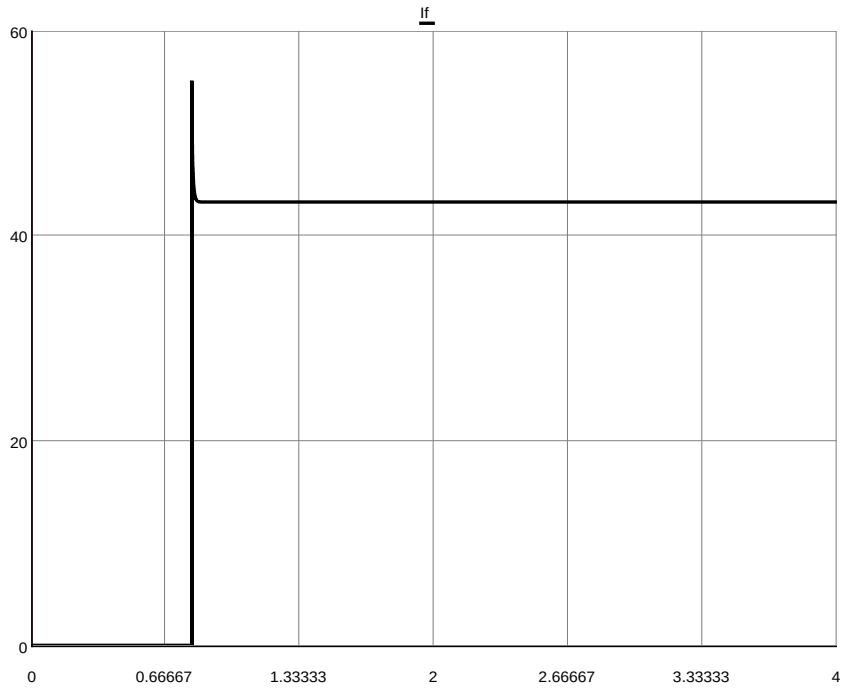

Fig 6.11 Fault Current Evolution with MPPT Impact

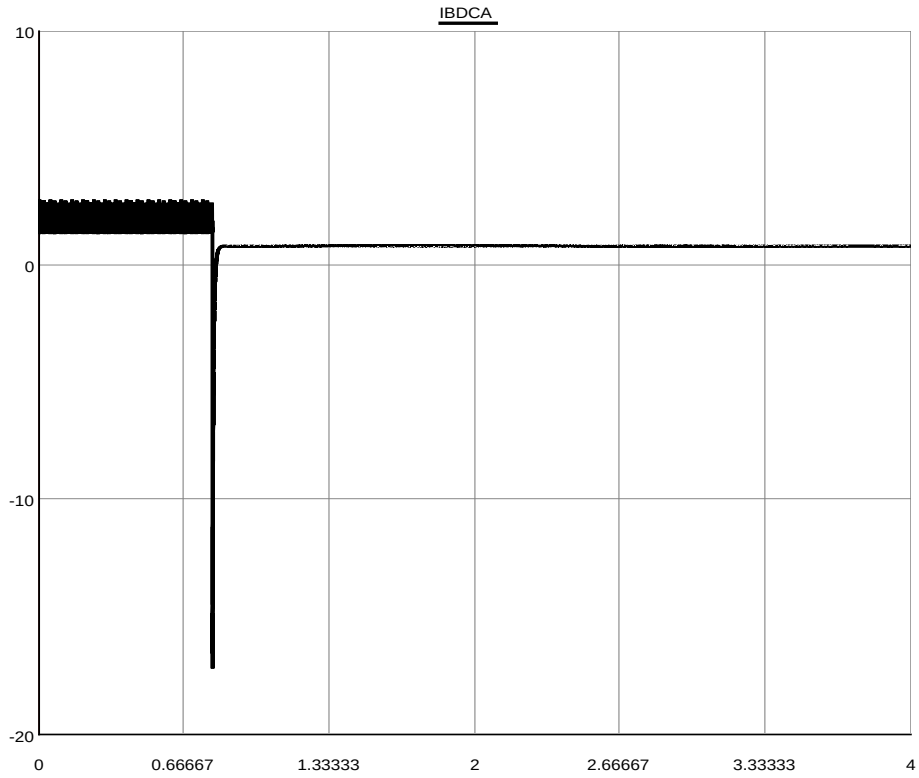

Fig 6.12 OCPD Current Evolution with MPPT Impact

It is shown that if the fault can evolve without interruption, the MPPT of the inverter can reduce the fault effects on a PV array by reducing the array's operating point to the new maximum power point. The impact of MPPT on this type of fault is significant. Given the default setting of protection devices (OCPD 5A, GFPD 1A), the OCPD in this case fails to detect the fault currents and let GFPD trip the whole system, which is defined as a loss of dependability according to protection principle. Without the impact of MPPT, both the OCPD and GFPD should detect the fault current and ideally the OCPD should operates first with proper coordination.

For line-to-line faults, simulation results of the RTDS show that the MPPT control of the inverter helps recover the sudden drop of OCPD current but does not play a big role in

determining the fault current. In comparison to our baseline case, RTDS plot of line-to-line high impedance fault current evolution is shown in Fig 6.13 and Fig 6.14.

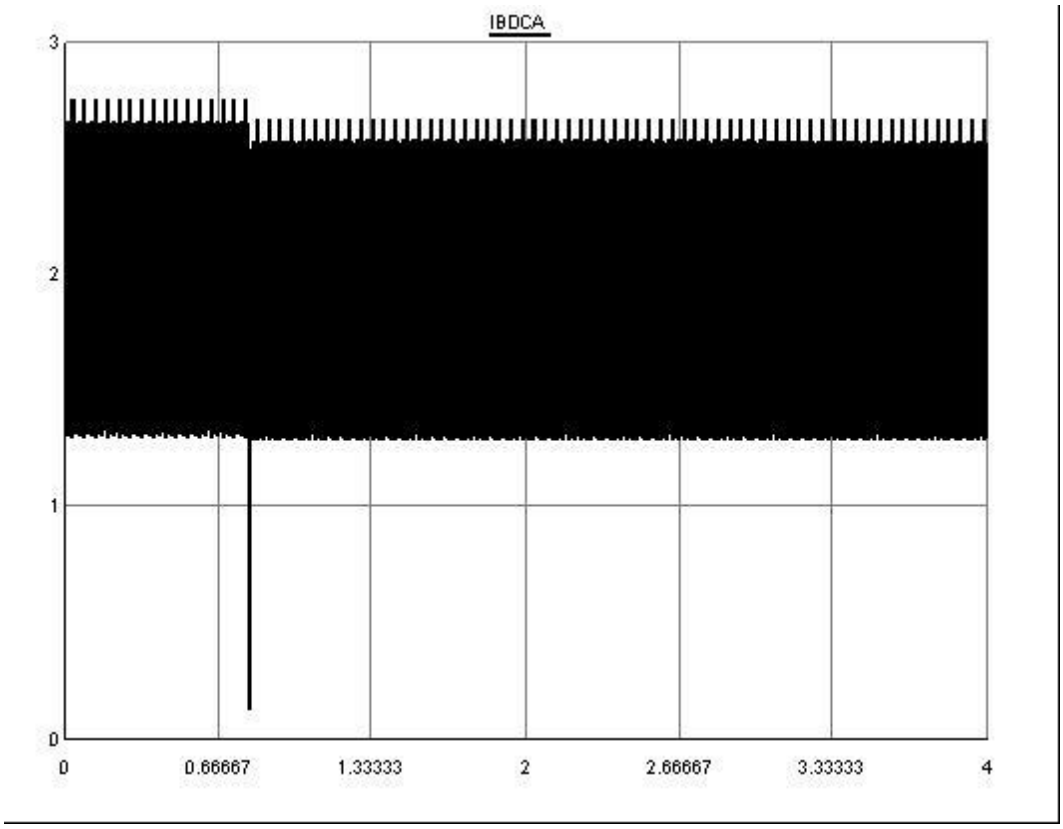

Fig 6.13 High Impedance Line-to-Line Fault OCPD Current Evolution with MPPT Impact

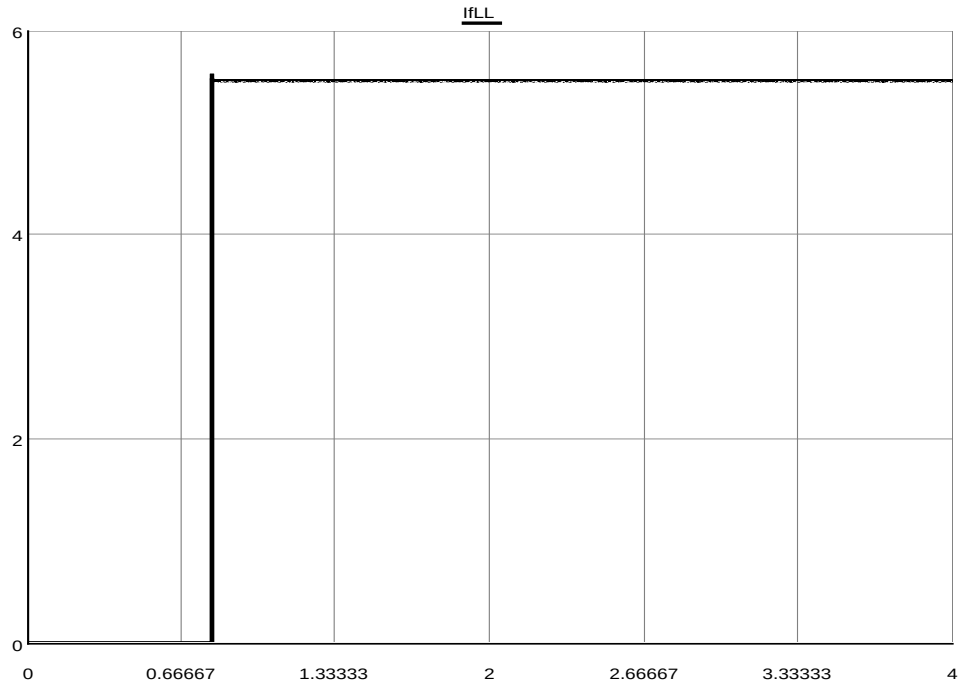

Fig 6.14 High Impedance Line-to-Line Fault Current Evolution with MPPT Impact

From a protection design prospective, the impact of MPPT on fault current detection should be taken into consideration when the fault type is associated with backfed current level that is originally detected by OCPD. For example, a line-to-line cross string fault with large voltage difference can also lead to very large backfed current while the fault current flowing through GFPD is still too small to be detected. This is a case where the fault goes totally undetected because of MPPT control of the inverter. Unlike other undetected faults with small fault current discussed in Chapter 4, the high level of fault current flowing through of this type of fault will pose a severe safety issue on the residential level power system.

Our last study case is the impact of settling time of MPPT on fault current detection.

Fig 6.15 shows the default setting of MPPT controller in our RTDS testbed. The setting of the MPPT controller has a significant impact on determining the inverter transient response of the fault current. The modified case is simulated in RSCAD with a different MPPT controller

setting (sampling period 10ms, input smoothing filter disabled) in comparison to our baseline case.

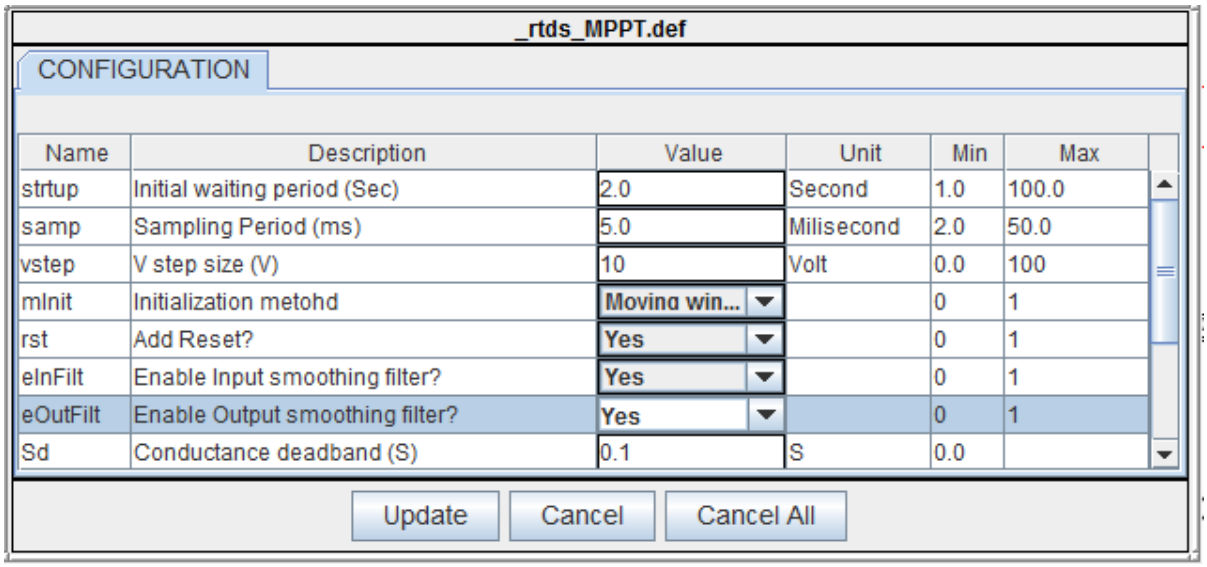

Fig 6.15 High Impedance Line-to-Line Fault Current Evolution with MPPT Impact

From Fig 6.16, it is clear that the simulated case has approximate 3 more seconds of the settling time. According to the RTDS user manual, the initial waiting period, sampling period, voltage step size and smoothing filter design altogether determines the settling time of the post-fault current.

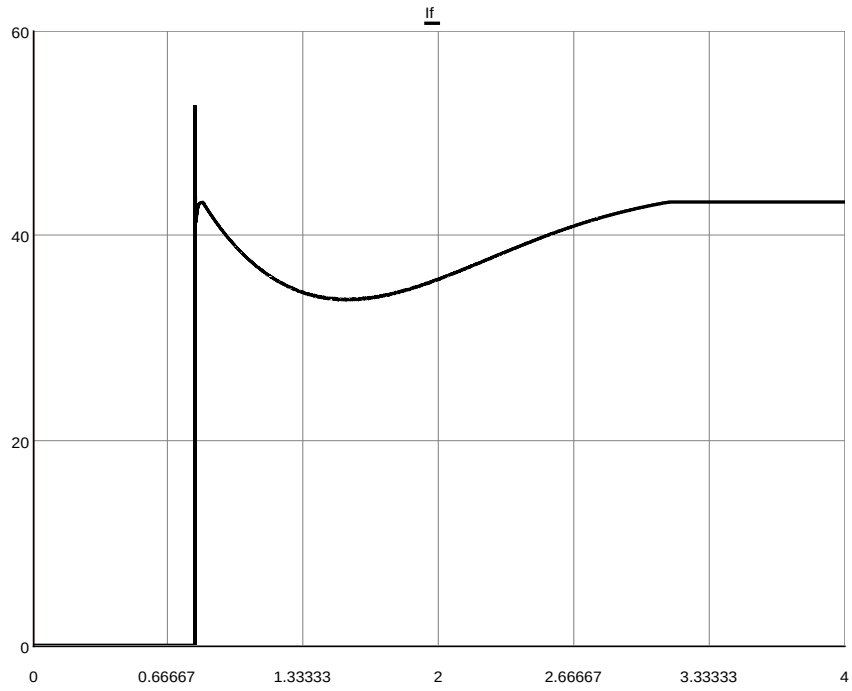

Fig 6.16 Fault Current Evolution with Different MPPT Setting

As for future fault diagnosis function application, it is suggested that the MPPT setting data should be obtained to help determine potential fault scenarios more accurately. The main reason is that, if the settling time is out of the OCPD and the GFPD's detection range, the fault may either goes undetected or cause nuisance tripping because the MPPT will eventually bring down the fault current level. The MPPT setting will finally reach an acceptable compromise value between the maximizing system efficiency and a more reliable protection scheme.

Chapter VII: Conclusion and Future Work

The first part of the thesis presented an implementation of an RTDS tedbed for PHIL testing on solar inverters. The second part described and analyzed required fault diagnostics functions of the Plug and Play PV system, the developed RSCAD platform to generate simulation plots can be modified and used for PHIL testing as well. The developed RTDS testbed can be utilized for testing either micro inverters or central inverters in the previous four types of testing scenarios, from commissioning tests to grid-friendly functionality tests. The testbed also provides a preliminary, trustworthy and safe environment for fault diagnosis function development.

Based on simulation and experiment results, some key findings with respect to fault diagnosis function of the residential PV system are listed as follows:

- Special considerations need to be taken to reach a proper coordination between inverter protection scheme and upstream overcurrent protection relay. Faults near the breaker spot may lead to a completely different system response based on the islanding scheme defined by the utilities.
- The research results show that an upper string ground fault or a line-line fault with large-voltage difference could result in backfed fault current, which may bring new coordination issues between the OCPD and the GFPD; On the other hand, a line-line fault with mall-voltage difference might be difficult to clear by conventional protection devices.
- It is discovered that the MPPT in the inverter can significantly affect the fault current in a PV system. This leads to new protection issues in PV arrays that have not previously been documented.
- An arcing fault or high impedance fault with degradation can hardly be detected by conventional protection devices. Simulation results show that fault detection algorithms based on harmonics signature analysis can be used for future PnP system to handle these safety concerns

A summary of the thesis work and future work is shown in Fig 7.1.

In the future we want to see if we can utilize the developed testbed to test different fault diagnosis algorithms in PnP system. Future work should also focus on the implementation of hardware on PHIL testing. As has been discussed in Chapter 3, the stability of the PHIL testing loop should be paid enough attention to because of the possible latency brought by RSCAD models as well as amplifiers. In addition, the assignment of the RTDS processors need to be well designed, especially when to it comes to system-level testing scenarios. A hybrid model of PV inverter model which combines the built-in RSCAD model and the average model can be used in this case so that the computation burden is alleviated. Last but not least, future tests should also extend to using the developed testbed on PV penetration study, which represents the last two test scenarios in Section 2.4.

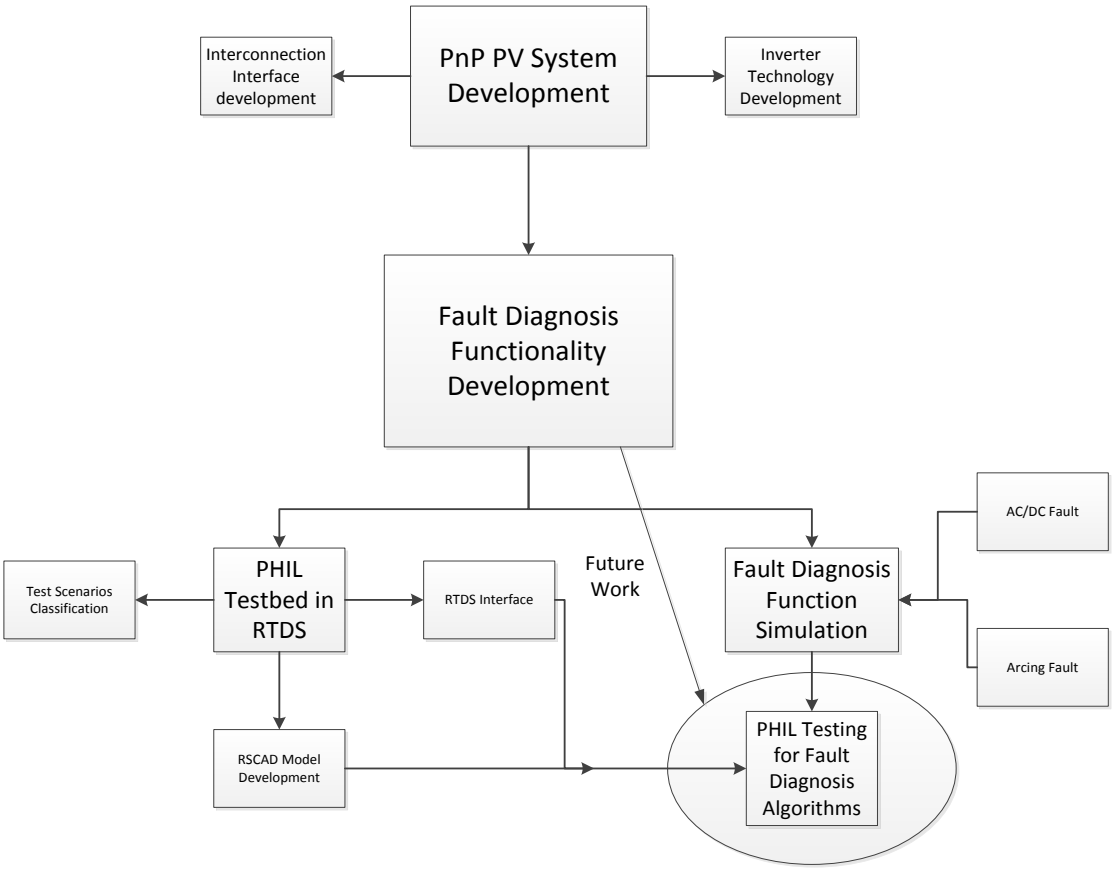

Fig 7.1 Summary of Thesis Work and Future Work

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APPENDICES

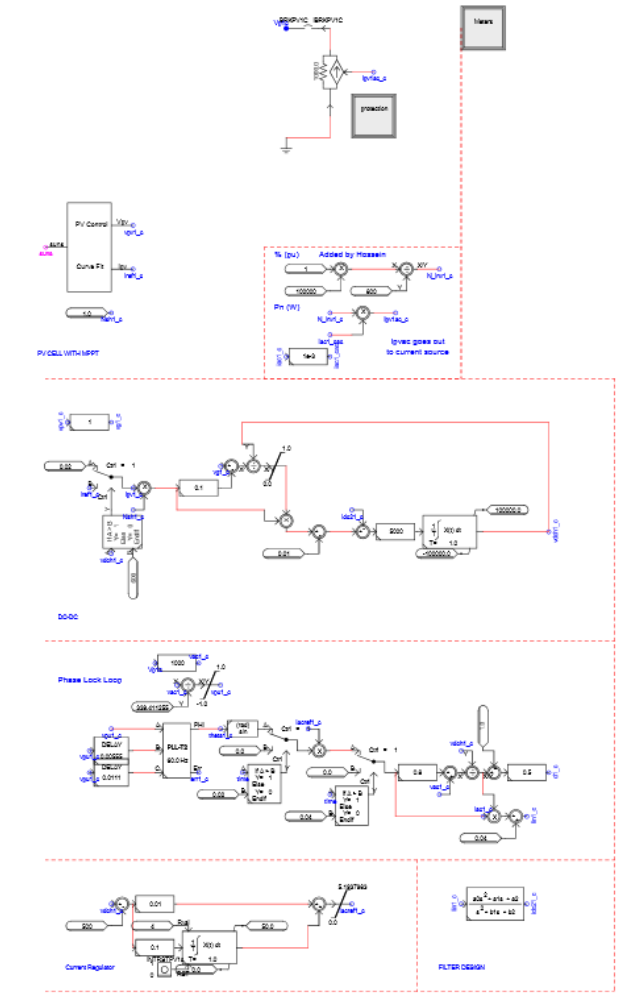
Appendix A

Overview of DER Advanced Functions

		Autonomous DER Functions
1	***Mandatory Autonomous DER Functions***	Support anti-islanding to trip off under extended anomalous conditions
2		Provide ride-through of low/high voltage excursions beyond normal limits
3		Provide ride-through of low/high frequency excursions beyond normal limits
4		Provide volt/var control through dynamic reactive power injection through autonomous responses to local voltage measurements
5		Counteract frequency excursions beyond normal limits by decreasing or increasing real power
6		Counteract voltage excursions beyond normal limits by providing dynamic current support
7		Reconnect randomly within a preset time window after grid power is restored
8		Limit maximum real power output at the PCC to a preset value
9		Modify real power output autonomously in response to local voltage variations
10		Provide reactive power by a fixed power factor
11		Set actual real power output at the PCC
12		Schedule actual or maximum real power output at specific times
13	***Recommended Autonomous DER Functions***	Smooth minor frequency deviations by rapidly modifying real power output to these deviations
14		Follow schedules for energy and ancillary service outputs
15		Set or schedule the storage of energy for later delivery, indicating time to start charging, charging rate and/or "charge-by" time
16	***Recommended DER Functions Requiring Communications***	Support direct command to disconnect or reconnect
17		Provide operational characteristics at initial interconnection and upon changes
18		Test DER software patching and updates

Appendix B

Details of Average Inverter Model in RSCAD



RTDS Technologies

File: Test
Created: Sep 14, 2013 (hwu9)
Last Modified: Apr 22, 2014 (hwu9)
Printed On: Jul 14, 2014

Test Circuit
PV1C CURVE FIT
SS #1
Subsystem #1 of 1

Appendix C

MATLAB Codes to Generate the I-V curve and P-V curve of PV Module

```
Iscr=3.83; %cell short circuit current at reference T and S
Irs=1.2e-7; %reverse saturation current
q=1.602e-19; %unit charge constant
k=1.38e-23; %boltzman constant
A=1.92; %ideality factor
K=0.0017; %temperature coefficient
Tr=300; %Reference Temperature
T=273+25; % cell temperature
ns=113; %number of cells in series {round(Voc/0.61)}
np=112; %number of cells in parallel
S=0:0.01:1; %solar radiation
a=(Iscr+K*(T-Tr))*(S/(100*Irs))+1;
b=q/(k*T*A*ns);
Vopt=(lambertw(a*exp(1))-1)/b;
%figure(1)
%pt1=plot(S,Vopt);
%set(pt1,'LineWidth',2)
%xlabel('Solar insulation (S)')
%ylabel('V_{optimal}(V)')
%title('Optimal Voltage for MPPT')
S1=[1 1 1];
Iph=0.01.*(Iscr+K.*(T-Tr)).*S1;
vdc=1:1:100;
ipv1=np.*Iph(1)-np.*Irs.*(exp((q.*vdc)./(k.*T.*A.*ns))-1)*200;
ipv3=(np*0.2).*Iph(3)-(np*0.5).*Irs.*(exp((q.*vdc)./(k.*T.*A.*ns))-1)*800;
ipv5=(np*0.8).*Iph(4)-(np*0.5).*Irs.*(exp((q.*vdc)./(k.*T.*A.*(ns*1)))-
1)*100;
figure(2)
pt2=plot(vdc,ipv1,vdc,ipv3,vdc,ipv5);
set(pt2,'LineWidth',2)
axis([0 80 -4 8])
xlabel('V_{dc}')
ylabel('I_{pv}')
title('PV output current Vs PV Terminal Voltage')
ppv1=np.*Iph(1).*vdc-np.*vdc.*Irs.*(exp((q.*vdc)./(k.*T.*A.*ns))-1);
ppv2=np.*Iph(2).*vdc-np.*vdc.*Irs.*(exp((q.*vdc)./(k.*T.*A.*ns))-1);
ppv3=np.*Iph(3).*vdc-np.*vdc.*Irs.*(exp((q.*vdc)./(k.*T.*A.*ns))-1);
figure(3)
pt3=plot(ppv3./1000);
set(pt3,'LineWidth',2)
axis([0 100 0 0.3])
legend('S=1')
xlabel('V_{dc}')
ylabel('P_{pv}')
title('PV output power Vs PV Terminal Voltage')
```

Appendix D

Nomenclature

AWG	American Wire Gauge
CCC	Current Carrying Conductor
EGC	Equipment Grounding Conductor
GEC	Grounding Electrode Conductor
GFPD	Ground Fault Protection Device
IEC	International Electrotechnical Commission
HIL	Hardware-in-the-Loop
HuT	Hardware-under-Test
kcmil	Circular mil
MPP	Maximum Power Point
MPPT	Maximum Power Point Tracking
NEC	National Electrical Code
OCPD	Overcurrent Protection Device
PHIL	Power-Hardware-in-the-Loop
PnP	Plug and Play
RTDS	Real Time Digital Simulator
UL	Underwriters' Laboratory
VDE	Verband der Elektrotechnik