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Chambers

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(54) **STRUCTURE AND METHOD TO FABRICATE SELF-ALIGNED TRANSISTORS WITH DUAL WORK FUNCTION METAL GATE ELECTRODES**

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See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

6,130,123 A * 10/2000 Liang et al. 438/217
6,383,879 B1 5/2002 Kizilyalli et al.
6,397,861 B1 6/2002 Wing et al.
6,534,423 B1 3/2003 Turner
6,583,012 B1 * 6/2003 Buynoski et al. 438/275
2004/0080001 A1 * 4/2004 Takeuchi 257/407

FOREIGN PATENT DOCUMENTS

GB 2 347 789 A 9/2000

OTHER PUBLICATIONS

"Pursuing the Perfect Low-K Dielectric"; www.e-insite.net/semiconductor/index.asp?layout=articlePrint&articleID=CA164243.
B. Maiti and P.J. Tobin; "Metal Gates for Advanced CMOS Technology"; SPIE vol. 3881; Sep. 1999; pp. 46-57.

* cited by examiner

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(57) **ABSTRACT**

The present invention provides, in one embodiment, a method (**100**) of forming dual work function metal gate electrodes in a semiconductor device. The method includes forming a gate dielectric (**105**) over a substrate (**110**) and depositing a mold layer (**115**) having a first opening (**120**) therein over the gate dielectric (**105**). The method further includes creating a first metal gate electrode (**125**) by depositing a first metal in the first opening (**120**). Other embodiments include an active device (**200**) produced by the above-described method and method of manufacturing an integrated circuit (**300**) using the above-described method.

6 Claims, 5 Drawing Sheets