US006275068B1

(12) **United States Patent**
Kermani et al.

(10) **Patent No.: US 6,275,068 B1**
(45) **Date of Patent: Aug. 14, 2001**

(54) **PROGRAMMABLE CLOCK DELAY**

(75) Inventors: **Bahram Ghaffarzadeh Kermani**, Whitehall; **Clinton Hays Holder, Jr.**, Slatington, both of PA (US)

(73) Assignee: **Lucent Technologies Inc.**, Murray Hill, NJ (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/469,905**

(22) Filed: **Dec. 22, 1999**

(51) **Int. Cl.**[7] **H03K 5/13**
(52) **U.S. Cl.** **326/93**; 327/276; 327/270
(58) **Field of Search** 327/276, 277, 327/278, 281, 288, 261, 263, 264, 269, 270, 271; 326/93

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,126,691	6/1992	Mijuskovic et al. .	
5,268,656	12/1993	Muscavage	331/45
5,438,300 *	8/1995	Saban et al.	331/16
5,828,870	10/1998	Gunadisastra	395/558
5,838,179	11/1998	Schmidt	327/156
5,841,296	11/1998	Churcher et al.	326/49
5,881,271	3/1999	Williams	395/552
5,923,611	7/1999	Ryan	365/233
5,926,837	7/1999	Watanabe et al.	711/167
6,046,620 *	4/2000	Relph	327/277
6,130,567 *	10/2000	Kobayashi	327/278
6,150,863 *	11/2000	Conn et al.	327/270

FOREIGN PATENT DOCUMENTS

64-1322-a *	1/1989	(JP)	327/278

* cited by examiner

Primary Examiner—Tuan T. Lam
(74) *Attorney, Agent, or Firm*—Ratner & Prestia

(57) **ABSTRACT**

In an integrated circuit, a system and method of programmably controlling the delay between a second clock signal with respect to a first clock signal after fabricating the integrated circuit. Prior to fabrication, a programmable delay group is formed and will be included in the integrated circuit. The programmable delay group includes a plurality of parallel coupled sets of delay stages. Each set having at least one delay stage. For the sets having more than one delay stage, the delay stages are serially coupled. After fabrication of the integrated circuit and in operation, the first clock signal is applied to one end of each of the sets of delay stages. The enable signals are generated and applied to the programmable delay group in order to enable one of the sets of delay stages. The enabled set delays the first clock signal, thereby producing the second clock signal at the other end of the enabled set and hereby controlling the delay of the second clock signal.

8 Claims, 2 Drawing Sheets