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(54) **METHOD OF MANUFACTURING A VERTICAL JUNCTION FIELD EFFECT TRANSISTOR HAVING AN EPITAXIAL GATE**

(75) Inventors: **Christopher Harris**, Taby (SE); **Andrei Konstantinov**, Sollentuna (SE); **Cem Basceri**, Reston, VA (US)

(73) Assignee: **Cree, Inc.**, Durham, NC (US)

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See application file for complete search history.

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Primary Examiner—Brook Kebede
(74) *Attorney, Agent, or Firm*—Volentine & Whitt, P.L.L.C.

(57) **ABSTRACT**

A vertical junction field effect transistor includes a trench formed in an epitaxial layer. The trench surrounds a channel region of the epitaxial layer. The channel region may have a graded or uniform dopant concentration profile. An epitaxial gate structure is formed within the trench by epitaxial regrowth. The epitaxial gate structure may include separate first and second epitaxial gate layers, and may have either a graded or uniform dopant concentration profile.

25 Claims, 8 Drawing Sheets