Interface formation and thermal stability of advanced metal gate and ultrathin gate dielectric layers

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The compatibility of metallic titanium nitride (TiN) films for advanced gate electrodes and remote plasma enhanced chemical vapor deposited silicon oxide (SiO$_2$) or silicon oxide/silicon nitride (Si$_3$N$_4$) advanced gate dielectric layers is investigated by interrupted growth and on-line rapid thermal annealing using on-line Auger electron spectroscopy. Growth of TiN$_x$ on SiO$_2$ and Si$_3$N$_4$ occurs uniformly without a titanium seed layer. TiN$_x$/SiO$_2$ and TiN$_x$/Si$_3$N$_4$ interfaces are chemically stable against reaction for rapid thermal annealing treatments below 850 °C. Metal–oxide–semiconductor capacitors using TiN$_x$ gate contacts and SiO$_2$ or SiO$_2$/Si$_3$N$_4$ gate dielectrics exhibit excellent C–V characteristics. The measured TiN$_x$/SiO$_2$ barrier height in these devices is $\Phi_b = 3.7 \pm 0.1$ eV. The observed difference in fixed charge for SiO$_2$ and SiO$_2$/Si$_3$N$_4$ dielectrics is briefly discussed in terms of a new interface dipole model. © 1998 American Vacuum Society.

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I. INTRODUCTION

The continuing effort to reduce metal–oxide–semiconductor (MOS) device dimensions has led to considerable interest in silicon oxide$^1$ (SiO$_2$) and silicon oxide/silicon nitride$^{2,3}$ (Si$_3$N$_4$) layered films with an equivalent oxide thickness $t_{eq}$ below 3 nm for advanced gate dielectrics. Similarly, to maintain proper device scaling and to avoid the effects of gate electrode depletion, attention is being focused on advanced gate materials such as metallic titanium nitride$^{4-8}$ (TiN) as a possible replacement for heavily doped polycrystalline silicon. However, before such materials can be incorporated into device production they must be shown to be compatible with the other materials and with subsequent process conditions required for fabrication. Of particular concern is the possibility of chemical reaction at the interface between these advanced dielectric and gate materials at elevated temperatures.$^9,10$ For example, the gate metal/dielectric interface must be able to withstand rapid thermal annealing (RTA) temperatures of at least 800–1000 °C which are required to activate dopants in source and drain structures.

In this article, the interface formation between reactively sputtered TiN$_x$ metallic films and SiO$_2$ or SiO$_2$/Si$_3$N$_4$ dielectric layers prepared by low-temperature remote plasma enhanced chemical vapor deposition (RPECVD) is investigated as well as the chemical stability of these interfaces following on-line RTA treatments up to 850 °C. The evolution of the TiN$_x$/SiO$_2$ and TiN$_x$/Si$_3$N$_4$ interfaces is investigated from their initial formation at the monolayer level to the buried interface by interrupted film growth using on-line Auger electron spectroscopy (AES). The stability of TiN$_x$/SiO$_2$ and TiN$_x$/Si$_3$N$_4$ interfaces against reaction during RTA treatments at temperatures below 850 °C is also established by on-line AES. Finally, capacitance–voltage (C–V) characteristics of MOS capacitors employing TiN$_x$ gate electrodes with ultrathin single layer SiO$_2$ and dual layer SiO$_2$/Si$_3$N$_4$ gate dielectrics are presented. These C–V results are compared with similar MOS devices made using Al gate contacts.

II. EXPERIMENT

Interrupted growth and chemical stability experiments were conducted on 3 in. p-type Si(100) wafers on which either a single layer SiO$_2$ dielectric or a dual layer SiO$_2$/Si$_3$N$_4$ dielectric stack was deposited. In both cases, the SiO$_2$ layer was 5 nm thick and was prepared by a two-step plasma assisted oxidation/RPECVD process$^1$ which is described in detail elsewhere. The Si$_3$N$_4$ layer was 3 nm thick and was deposited by RPECVD with NH$_3$ and SiH$_4$ source gases injected downstream$^2,11,12$ at a ratio of 10:1. Prior to TiN$_x$ deposition, the SiO$_2$ and SiO$_2$/Si$_3$N$_4$ dielectric layers were subjected to a 30 s RTA treatment at 900 °C to improve their electrical properties by reducing bond defects.$^{13,14}$ This bonding rearrangement was verified by Fourier transform infrared (FTIR) spectroscopy.

Metallic TiN$_x$ films were deposited at room temperature by reactive dc magnetron sputtering of a 99.9% Ti target at 50 W with a 5:1 mixture of 99.999% Ar and 99.999% N$_2$ at a chamber pressure of 6 mTorr. Several ultrathin TiN$_x$ layers were deposited sequentially and AES spectra collected until the Si$_{LVV}$ Auger peak could no longer be observed, indicating that the interface had been buried. Thicker TiN$_x$ layers (each about 0.5–1.0 nm) were then added until bulk characteristics were observed. To study the chemical stability of the metal/dielectric interfaces, a 0.6–1.0 nm thick TiN$_x$ layer was deposited on SiO$_2$ or SiO$_2$/Si$_3$N$_4$ and annealed in vacuum for 180 s in 100 °C steps from 350 to 850 °C. Following each on-line RTA treatment, AES spectra were collected.

MOS capacitors were prepared on n-type Si(100) wafers with ultrathin SiO$_2$ or SiO$_2$/Si$_3$N$_4$ dielectrics and TiN$_x$ or Al gate electrodes. The wafers were cleaned, a thermal field
oxide was grown and patterned, and the active area was chemically etched. The wafers were cleaned again prior to RPECVD deposition of a 3.5 nm SiO$_2$ gate dielectric or a 2.0 nm SiO$_2$/2.0 nm Si$_3$N$_4$ dielectric bilayer. The wafers were patterned for liftoff and a 50 nm TiN$_x$ or 100 nm Al gate electrode deposited by sputtering. A 100 nm thick Al layer was sputtered on top of the TiN$_x$ gate to facilitate external contact. Liftoff was performed, Al back contacts evaporated, and the samples were annealed at 300 °C in H$_2$ for 1800 s. Standard high frequency C–V measurements were conducted to determine the device characteristics.

II. RESULTS AND DISCUSSION

To evaluate the integration of TiN$_x$ and RPECVD dielectrics with existing Si technology and process flows it is critical to use optimal preparation conditions for these new materials. It has been shown previously that a 15 s, 900 °C RTA treatment improves the dielectric quality of RPECVD SiO$_2$ films by reducing the amount of suboxide (SiO$_x$ with $x<2$) at the Si/SiO$_2$ interface and hence the number of electrically active dangling bond defects. A similar improvement in the dielectric reliability of RPECVD Si$_3$N$_4$ films occurs by annealing at 900 °C for 30 s and can be monitored with FTIR as seen in Fig. 1. The top curve shows the FTIR spectrum of RPECVD SiO$_2$ as deposited and following a 90 s 900 °C RTA treatment. The decrease of Si–H stretch and bending modes while the Si–N asymmetric stretch increases after annealing indicates conversion of Si–H dangling bonds to Si–N network bonds.

FTIR as seen in Fig. 1. The spectrum displays three main features: a Si–N asymmetric stretching mode at approximately 850 cm$^{-1}$, a SiN–H bending mode at 1200 cm$^{-1}$, and a SiN–H stretching mode near 330 cm$^{-1}$. Figure 1 shows a decrease in the intensity of SiN–H bending and stretching modes while the Si–N asymmetric stretch increases from as-deposited levels following a 900 °C RTA treatment. These changes in the IR spectra have recently been explained as resulting from a conversion of correlated Si–H and SiN–H dangling bonds into Si–N network bonds.

The wafers were used to study the interface formation, growth, and chemical stability of TiN$_x$. Derivative AES spectra demonstrating the growth of TiN$_x$ on RPECVD SiO$_2$ are provided in Fig. 2 with the relevant Auger transitions indicated. The bottom curve shows the spectrum for the bare SiO$_2$ dielectric layer. The vertical offset of subsequent curves corresponds to the integrated TiN$_x$ sputtering time elapsed, indicated by the right-hand axis. Film thickness was estimated from the bulk deposition rate of 1.0 nm/min which was determined by cross-sectional scanning electron microscopy on thick samples.

A quantitative difficulty which arises in the TiN$_x$ system is that the Ti$_{LVV}$ and O$_{KVV}$ AES peaks overlap at 385 eV; however the Ti$_{LMV}$ feature at 420 eV does not suffer from this deficiency. For TiN$_x$, the Ti$_{LVV}$+N$_{KVV}$ features exhibit a peak to peak intensity ratio that is about 2:1. In contrast, for pure Ti the intensity of these two peaks decreases as successive TiN$_x$ layers are added and the intensity of this peak is always about twice that of Ti$_{LMV}$. This asymmetry in these peak intensities, which occurs even for submonolayer coverage, indicates that TiN$_x$ grows directly on SiO$_2$ without the need for an intermediate Ti seed layer. The Si$_{LVV}$ peak intensity at 76 eV decreases as successive TiN$_x$ layers are deposited and disappears entirely for a metal thickness greater than about 0.8 nm. The O$_{KVV}$ peak near 510 eV also initially decreases; however a small amount of parasitic oxygen is always observed even after the TiN$_x$/SiO$_2$ interface is completely buried and bulk TiN$_x$ features are observed.

Figure 3 shows similar derivative AES spectra for interrupted TiN$_x$ growth on Si$_3$N$_4$. Because the dielectric contains nitrogen, the initial development of the Ti$_{LVV}$+N$_{KVV}$ feature is impossible to observe. However, the Ti$_{LMV}$ peak evolution...
on Si$_3$N$_4$ is similar to the behavior observed in Fig. 2 on SiO$_2$ and suggests that TiN$_x$ grows directly on Si$_3$N$_4$ without a buffer layer. The Si$_{LVV}$ peak intensity in Fig. 3 is diminished by successive TiN$_x$ layers and disappears above about 0.8 nm as expected.

The decrease of the Si$_{LVV}$ peak intensity normalized to its value in the bare dielectric is plotted on a log scale as a function of TiN$_x$ deposition time in Fig. 4 for both the SiO$_2$ and the SiO$_2$/Si$_3$N$_4$ substrates. In both cases the intensity decreases exponentially with TiN$_x$ thickness although the slopes differ by about a factor of 2. This exponential decrease of the Si$_{LVV}$ peak intensity with TiN$_x$ thickness indicates uniform layer growth on both SiO$_2$ and Si$_3$N$_4$. The difference in the slopes of these curves corresponds to different deposition rates due to target aging. Detailed kinetics of the interface formation and morphology of the TiN$_x$ layer in each case require further investigation.

Derivative AES spectra for TiN$_x$/SiO$_2$ and TiN$_x$/Si$_3$N$_4$ interfaces subjected to on-line RTA treatments up to 850 °C are shown in Figs. 5 and 6, respectively. In both cases, a dramatic increase of the Si$_{LVV}$ AES peak at 850 °C indicates that a reaction has occurred.

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**Fig. 3.** Interrupted growth of TiN$_x$ on RPECVD Si$_3$N$_4$ measured by AES. The Si$_{LVV}$ peak decreases while the Ti$_{LVV}$ and Ti$_{MV}$ peaks increase with additional TiN$_x$ deposition. The similarity in growth of the Ti$_{MV}$ peak to Fig. 2 suggests that no seed layer is required.

**Fig. 4.** Decrease of normalized Si$_{LVV}$ AES peak intensity with increasing TiN$_x$ deposition on SiO$_2$ and Si$_3$N$_4$ dielectric layers. The exponential decay indicates uniform TiN$_x$ layer growth on both dielectrics.

**Fig. 5.** Chemical stability of TiN$_x$/SiO$_2$ interface following the RTA treatments indicated. The dramatic increase of the Si$_{LVV}$ AES peak at 850 °C indicates that a reaction has occurred.

**Fig. 6.** Chemical stability of TiN$_x$/Si$_3$N$_4$ interface following the RTA treatments indicated. A slight increase of the Si$_{LVV}$ AES peak at 850 °C indicates that the interface is chemically stable.
minimal thickness of TiN was deposited to bury the interface, reducing the SiLVV peak intensity to nearly zero. Only minor changes in the AES spectra for both TiNx/SiO2 and TiNx/Si3N4 interfaces are observed below 850 °C and are most likely the result of slight variations in thickness of the TiNx overlayer. Following the 850 °C anneal, however, the SiLVV peak intensity increases substantially for the TiNx/SiO2 interface and modestly for TiNx/Si3N4. The fact that these changes in the AES spectra occur at the same temperature for both dielectrics suggests that decomposition of TiNx begins at 850 °C. The dramatic change in the AES spectra for the TiNx/SiO2 interface compared to that of TiNx/Si3N4 indicates that the metal chemically reacts with the underlying SiO2 layer but does not interact with Si3N4. The details of this reaction and the chemical structure that results, including the possible formation of a titanium silicide layer, still need to be elucidated.

High frequency C–V characteristics for MOS capacitors using TiNx and Al gates on ultrathin RPECVD SiO2 dielectrics are shown in Fig. 7. The flatband voltage for the TiNx gate is shifted by ΔΦ=0.5±0.1 eV above Al. A similar shift ΔΦ=0.4±0.1 eV is observed in Fig. 8 for capacitors with TiNx and Al gates on a SiO2/Si3N4 bilayer. In each case, the flatband voltage shift results from the work function difference of the two metals. Using the known18 barrier height of 3.2 eV for Al on SiO2, the observed flatband voltage shift gives a barrier height of Φb=3.7±0.1 eV for TiNx/SiO2, in agreement with previous studies.8 Comparing the two devices with TiNx gates, there is an additional flatband voltage shift ΔΦ=0.3 eV between the capacitors using SiO2 and SiO2/Si3N4 dielectrics as seen in Fig. 9. This flatband voltage shift is not due to a work function difference between the contacts since the same gate metal and substrate were used in each device. Instead, this difference in flatband voltage must result from fixed positive charge in the dielectric. However, since the wafers were processed in parallel and subjected to the same treatments at each step except for deposition of the dielectric layer, it is assumed that this fixed positive charge is intrinsic to the dielectric and does not result from device processing. The most likely source of this fixed charge is an interface dipole layer in the dielectric. Recent calculations19 suggest that dipole layers between Si/SiOx and Si/Si3N4 interfaces may account for the observed flatband voltage shift.

IV. CONCLUSIONS

As MOS device dimensions are reduced, the impact of interface physics on their operation and performance increases dramatically. Understanding, controlling, and optimizing interface properties will be critical to continued de-
issue scaling. In particular, issues relating to the integration of novel gate dielectrics and gate metals with existing Si technology and process flows must be investigated and verified.

Metallic TiN gates are compatible with advanced RPECVD SiO$_2$ dielectric layers and SiO$_2$/Si$_3$N$_4$ dielectric stacks. TiN$_x$ grows uniformly on these dielectrics without an intermediate seed layer. TiN$_x$/SiO$_2$ and TiN$_x$/Si$_3$N$_4$ interfaces are stable against chemical reaction for RTA treatments below 850 °C. At 850 °C, the metal reacts with SiO$_2$ possibly due to decomposition of TiN$_x$, but is more stable on Si$_3$N$_4$.

MOS capacitors have been fabricated which integrate TiN$_x$ gate electrodes with RPECVD SiO$_2$ or SiO$_2$/Si$_3$N$_4$ gate dielectrics and exhibit good C–V characteristics. From the flatband voltage shift of the C–V curves for TiN$_x$ gates relative to Al, a barrier height of $\Phi_b = 3.7 \pm 0.1$ eV for TiN$_x$ on SiO$_2$ is determined. In addition, a flatband voltage shift $\Delta \Phi = 0.3$ eV is observed between TiN$_x$ gates on SiO$_2$ and SiO$_2$/Si$_3$N$_4$ gate dielectrics. This difference may result from a change in the charge dipole layer in the dielectric.

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