Plasma-assisted formation of low defect density $SiC-SiO_2$ interfaces

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The initial stages of $SiC-SiO_2$ interface formation by low temperature (300 °C) remote plasma assisted oxidation (RPAO) on flat and vicinal 6H SiC(0001) wafers with Si faces have been studied by on-line Auger electron spectroscopy (AES). Changes in AES spectral features associated with Si–C and Si–O bonds are readily evident as oxidation progresses; however, there are no detectable AES features that can be attributed to C–O bonds. Initial oxidation rates as determined from AES data are greater for vicinal wafers than for flat wafers paralleling results for RPAO oxidation of Si. Devices fabricated on vicinal SiC wafers require an 1150 °C anneal in an H_2 containing ambient to reduce defect densities from the 10^{13} to 10^{11} cm^{-2} range, consistent with termination of C atom step edge dangling bonds by H atoms. Devices prepared by thermal oxidation also require a 1150 °C anneal in H_2 even though silicon oxycarbide regions with C–O bonds are formed in a transition region at the $SiC-SiO_2$ interfaces. [S0734-211X(97)07304-6]

I. INTRODUCTION

There is considerable interest in SiC for high temperature device applications, including power transistors. To fabricate these devices, it will be necessary to gain an increased understanding of the chemical bonding at the $SiC-SiO_2$ interface, and in particular to develop processing that minimize interfacial defects and transition regions, and maximize device reliability as manifested in reductions in the rate of interfacial and bulk defect generation during operation. It has been established that the oxide that forms on SiC during high temperature oxidation in O_2 ambients is SiO_2, and that this oxidation process can yield $SiC-SiO_2$ interfaces and gate dielectrics with sufficiently low defect densities for field effect transistor (FET) operation.[1] However, channel mobilities at room temperature (in depletion mode FETs) are significantly lower than expected from bulk SiC properties and much research has been focused on explaining these differences and improving channel mobilities.[2] Since SiO_2 is the dominant solid state oxidation product, oxidation products involving carbon atoms must include gaseous molecules such as CO; as oxide growth progresses these must be transported from the buried growth interface through the oxide and out of the film. However, this does not preclude the formation of additional interfacial carbon atom bonding arrangements such as Si–C and C–O as have been reported in silicon oxycarbide transition regions.[3] The molar volume mismatch between SiC and SiO_2 is greater than the corresponding mismatch between Si and SiO_2, so that intrinsic levels of strain at $SiC-SiO_2$ interfaces are anticipated to be at least as high as the values of approximately 5×10^9 dynes/cm^2 reported in $Si-SiO_2$.[4] This article deals with an alternative low temperature method for semiconductor-dielectric interface formation that has been successfully applied to crystalline Si device technology.[5,6] As applied to Si, this approach provides independent control of $Si-SiO_2$ interface formation and dielectric film grown. The $Si-SiO_2$ interface and a superficially thin oxide layer (~0.5 nm) are formed by a low temperature (300 °C) remote plasma-assisted oxidation (RPAO) process, and the remainder of the oxide layer is deposited by a low temperature (300 °C) remote plasma enhanced chemical vapor deposition (RPECVD) process. Device quality interfaces are obtained by subjecting the plasma processed $Si-SiO_2$ heterostructure to a post-deposition rapid thermal anneal (RTA), e.g., for 30 s at 900 °C. The 900 °C anneal promotes both chemical and structural interface relaxations, including a minimization of interfacial sub-oxide bonding arrangements in transition regions between the Si crystal and the stoichiometric bulk oxide.[7] A similar plasma-assisted process has recently been applied to SiC, and has yielded $SiC-SiO_2$ interfaces with defect state densities comparable to what has been achieved on SiC by conventional high temperature thermal oxidation.[8] The potential advantages of this two step approach to $SiC-SiO_2$ interface formation are: (i) it reduces the requirement for transporting gaseous reaction products such as CO molecules away from the interface as the oxide grows; and (ii) it can also reduce strain induced interface defect generation, since only a small fraction of the total oxide layer thickness is generated by consumption of the SiC substrate. The focal point of this article is a study of $SiC-SiO_2$ interface formation by RPAO using on-line Auger electron spectroscopy (AES) to monitor interface bonding chemistry and the initial oxide growth rate.

Before discussing the SiC AES measurements, it is useful

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to summarize the results of device studies on vicinal Si and SiC wafers using the plasma-assisted processing steps identified above. Studies by Bjorkman *et al.*[9] demonstrated that densities of mid-gap defect states (D_{it}) as low as 1×10^{10} cm^{-2} eV^{-1} could be obtained on Si(111) surfaces by using conventional thermal oxidation, metal electrodes and 400 °C post metal anneals in an H_2 containing ambient. Previous studies had always shown higher values for Si(111) as compared to the Si(100) surfaces used in the integrated circuit wafers (see Reference 9). Studies performed by Yasuda *et al.* on *p*-type Si(111) vicinal up to 5° in the 112 direction showed that the density of mid-gap states (D_{it}) increased by relatively small amounts from $\sim1\times10^{10}$ cm^{-2} eV^{-1} to about 6×10^{10} cm^{-2} eV^{-1} as the vicinal angle increased to about 5°.[10] The studies of Yasuda *et al.* were on Si–SiO_2 structures prepared by the same two-step RPAO-RPECVD 300 °C process that has been described above, and is discussed in detail in Ref. 5. Al electrodes were employed and a 400 °C postmetallization anneal (PMA) in a H_2 containing ambient was used. The magnitudes of the incremental increases in D_{it} with increasing vicinal angle indicated that only a relatively small fraction of the dangling bond states at the step edges contributed to increases in D_{it} with increasing step edge density due to increasing vicinal angle.

At the present state of the art, the highest quality SiC crystals for devices are epitaxial layers formed on Si atom terminated 6H SiC vicinal approximately 3.5° in the 1120 direction. Using RPAO-RPECVD, the results of device studies using vicinal 6H *p*-type SiC as reported by Gölz *et al.*[7] are markedly different than the results reported for vicinal Si. Metal-oxide-semiconductor (MOS) capacitors were prepared the essentially the same two-step RPAO-RPECVD process as used by Yasuda *et al.*[5] for Si. However, following a conventional PMA in an H_2 containing ambient, D_{it} values were in excess of 10^{13} cm^{-2} eV^{-1}, even when an 1150 °C furnace anneal in Ar was interposed between the oxide film deposition and the metallization steps. However if the high temperature anneal was performed in an H_2 containing ambient then D_{it} values after the conventional 400 °C PMA were reduced significantly into the 10^{11} cm^{-2} eV^{-1} range.[8] This large difference in defect densities is approximately equal to the number of carbon atom dangling bonds at the step edges suggesting that these dangling bonds were not H-terminated after a conventional 400 °C PMA, but instead required the higher temperature exposure to H for termination. It is important to note that interfaces prepared on the same type of vicinal SiC surfaces by conventional high temperature thermal oxidation processes also required a high temperature anneal in an H_2 containing ambient to yield values of D_{it} in the 10^{11} cm^{-2} eV^{-1} range.[10] Step edge carbon atom dangling bonds on vicinal Si wafers can either terminated by oxygen atoms that connect into the SiO_2 dielectric, or by hydrogen atoms. The annealing results in Refs. 8 and 10 are consistent with hydrogen atom termination of step edge carbon atom dangling bonds (see Section II for atomic structure at the step edges); i.e., dangling bond elimination would be accomplished by atomic hydrogen generated during the 1150 °C anneal.

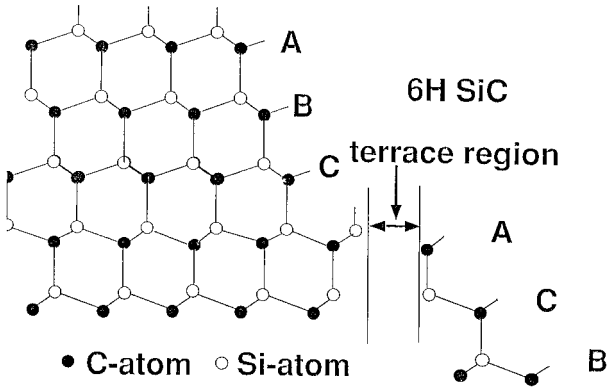

FIG. 1. Schematic representation of surface and step bonding for 6H SiC vicinal wafers. The C atom dangling bonds for the first 6-atom, 3-layer sequence are one per step edge C atom; for the second 6-atom, 3-layer sequence, there are two dangling bonds per step edge C atom. The 6-atom steps are separated by flat terrace regions with Si-atom dangling bonds.

To study interfacial bonding arrangements between SiC and SiO_2, on-line AES has been used to monitor the initial stages of SiC–SiO_2 interface formation. This same approach has been used to study the initial stages of interface formation on Si by both RPAO and rapid thermal oxidation (RTO), and using both O_2 and N_2O oxygen atoms sources gases.[7] This article extends this approach to SiC and focuses on the initial stages of the RPAO process as applied to both flat or vicinal SiC surfaces using O_2 source gases. Preliminary results are also presented for RPAO using N_2O as the oxygen atom source gas. Section II discusses briefly the local bonding arrangements at the step edges of the vicinal 6H SiC wafers. Section III presents results of AES studies of SiC RPAO, and includes comparisons between the RPAO of SiC and Si. Detailed results are presented for RPAO using O_2, and preliminary results for RPAO using N_2O. Section IV summarizes the major results of this study as they apply to (i) the results of the on-line AES studies, and (ii) the passivation of step edge dangling bonds as revealed by changes reductions in D_{it} levels as determined from electrical measurements.

II. LOCAL BONDING AT STEP EDGES

The dangling bond geometry for Si(111) wafers off cut in the 112 direction has been discussed in Ref. 4 and references therein. The steps are effectively two atom layers high, and the step edge atoms have a single dangling bond. The steps on 6H SiC with Si terminated surfaces are more complex due to the larger unit cell. The repeat pattern of 6H SiC extends over 12 atomic planes of alternating Si and C atoms as shown in Fig. 1. For off cut angles in the 1120 direction, the vicinal Si face surfaces can either include two different 6 atom steps that are separated by Si atom terminated terrace regions, or alternatively consist of six 2 atom layer steps/6H repeat pattern. Figure 1 indicates the bonding arrangements for the two different 6 atoms steps. The first set of steps are in an ABC sequence with one carbon atom dangling bond

per double layer Si–C component, and the second set of steps are an ACB sequence with two carbon atom dangling bonds per double layer Si–C component. The average number of dangling bonds per step in 6H SiC(0001) is 1.5 dangling bonds per step edge atom, whereas in Si(111) off cut in the 112 direction it is only 1 dangling bond per step atom. The spacing between single steps on Si(111) off cut in the 112 direction is ~5 nm for a 3.5° off cut angle, so that the ratio of step edge to terrace dangling bonds is approximately 0.06. For a 3.5 off cut angle on SiC, the dangling bond ratio is higher by a factor of 1.5 due to the different step edge terminations of the ABC and ACB sequences. If the 6H SiC surface has two atom steps, as is likely for the wafers used in this study, the dangling bond considerations are the same. Starting with the same ABC sequence as in Fig. 1, the first three 2 atom steps are terminated by C atoms with one dangling, and the second three 2 atom steps by C atoms with two dangling bonds. This means that the number of dangling bonds per step on the average is still 1.5 times greater than for off cut Si wafers.

III. EXPERIMENTAL RESULTS

The samples used in this study were *p*-type 6H SiC purchased from Cree Corporation with Si faces. Similar to polar faces on III–V compounds, the polar faces on SiC are either Si or C faces. Note further that this particular designation is used independent of any surface contamination. One of the wafers was oriented on a principal axis, the (0001) direction, and the other was a vicinal wafer off cut at approximately 3.5° in the 1120 direction. The surface of the on-axis sample was prepared from and bulk ingot, and the surface of the off-axis sample used in these studies was from an epitaxially grown film. The surfaces of the wafers were cleaned following a procedure suggested by Cree Research, Inc.[11] The *ex situ* cleaning consisted of (i) sequential rinses in tri-chloroethane (TCE), acetone and methanol, followed by (ii) a conventional two bath RCA clean. The sacrificial oxide formed in the second step of the RCA clean was removed by rinse in dilute HF. Samples were then loaded into a multichamber system, which provides a separate ultrahigh vacuum (UHV) compatible chambers for RPAO and AES. The experimental procedure was to alternate AES measurements with RPAO processing. A similar approach has been applied to RPAO of Si, and through analysis of the AES data, two kinds of information were obtained: (i) the chemical bonding at the Si–SiO_2 interface, and (ii) the oxide thickness as a function of oxidation time.[12]

Figures 2(a) and 2(b), respectively give differential AES spectra for flat and vicinal SiC obtained by RPAO using an O_2 source gas. The experimental processing conditions are:

(i) a substrate temperature of 300 °C,
(ii) a process pressure of 300 mTorr,
(iii) a plasma power to the He/O_2 mixture of 30 W, and
(iv) flow rates 200 standard cubic centimeters per minute (sccm) of He, and 20 sccm and O_2.

The as-loaded samples show surface contamination by oxygen and nitrogen that was not removed by the *ex situ* cleaning process. Since the levels of surface contamination were sub-monolayer, no *in situ* cleaning was attempted. This was in part due to the limited temperature capabilities of the plasma-processing chamber; the substrate heater in this chamber cannot heat a wafer to a temperature greater than about 500 °C. Never-the-less, the nitrogen contamination problem must be overcome before detailed studies of interface bonding using an N_2O source gas can be definitive with respect to any preferential nitrogen atom incorporation at the SiC–SiO_2 interface. It should be further noted that the SiC samples used in this study were *n*-type with a N atom doping level of $\sim 1.4\times10^{18}$ cm^{-3}, so that the N contamination

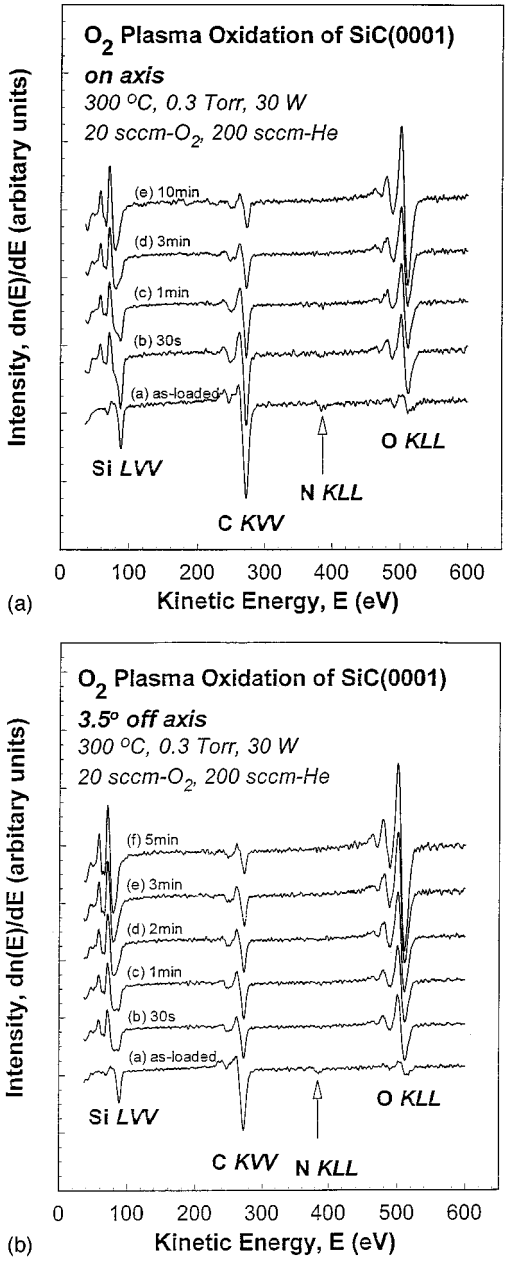

FIG. 2. Derivative mode AES spectra for (a) flat and (b) vicinal SiC obtained by RPAO at 300 °C using O_2 as the oxygen atom source gas.

may have its origin in the doping of the SiC wafers; however, it cannot be attributed simply to the doping because the area density of dopant atoms in a 2 nm thickness (~2 electron escape depths) is $\sim 3\times 10^{11}$ cm^{-2}, which is considerably less than the minimum AES detection limit of $\sim 10^{13}$ cm^{-2}. In spite of the sub-monolayer surface N concentration, information relative to oxidation rates could be obtained using the N_2O source gas. In the case of Si, as-loaded samples generally showed small levels of oxygen contamination, but never showed any nitrogen signal, so that more detailed interface bonding studies could be performed with both O_2 and N_2O source gases.[12] Prior to oxidation, the flat and vicinal SiC wafers displayed essentially the same ($\pm 3\%$) Si/C surface ratios so that changes in these ratios could be correlated with the effects of the oxidation processes. As the oxidation time for the SiC wafers is increased, there are four changes evident in the SiC spectra in Figs. 2(a) and 2(b):

(i) the line shapes and multiplicity of features within the Si_{LVV} group changed,
(ii) the C_{KVV} signal strength decreased,
(iii) the N_{KLL} signal strength decreased, and
(iv) the O_{KLL} signal strength increased.

These spectral changes are consistent with the growth of an SiO_2 film on the SiC substrate.

Figures 3(a) and 3(b), and 4(a) and 4(b) display, respectively, changes in (a) the Si_{LVV} and (b) the C_{KVV} (AES) features as a function of the oxidation time for flat (Fig. 3) and vicinal (Fig. 4) surfaces. Consider first the Si_{LVV} features in Figs. 3(a) and 4(a). The feature at ~88 eV is associated with Si–C bonds, in particular with a Si atom that is bonded to four C atoms. As the oxidation proceeds this feature decreases in strength as the Si–O feature at ~76 eV increases. These changes in relative intensity are due to increase of the oxide thickness with time and are consistent with the relative values of the electron escape depth, ~0.6 nm, and the oxide thickness. There is also a shift of the Si–C feature to lower energy as the oxidation proceeds; this is more easily seen in the spectra for the off-axis sample. Figures 5(a) and 5(b) display the integrated Si_{LVV} spectra. It is evident from Figs. 3(a) and 5(a) that as the intensity of the Si–C feature decreases, the position of this spectral feature moves to lower energy. In particular in Fig. 3(a), the Si–C feature is evident as a distinct spectral peak at ~88 eV prior to oxidation, after the oxidation has progressed for 3 min it has shifted to lower energy and appears as shoulder at ~84 eV on the 76 eV peak. In contrast, the C–Si feature in the C_{KVV} spectrum in Fig. 4(a) simply decreases in strength as the oxidation process proceeds. The absence of any significant spectral change in this region of the AES spectrum is indicative of the fact that C–O bonds are not formed during the RPAO process. The development of interfacial C–O bonds would produce a satellite peak at lower energy, which would increase in relative strength to the C–Si feature as the oxide growth proceeds and the AES signal becomes more sensitive to the SiC interface than the bulk.

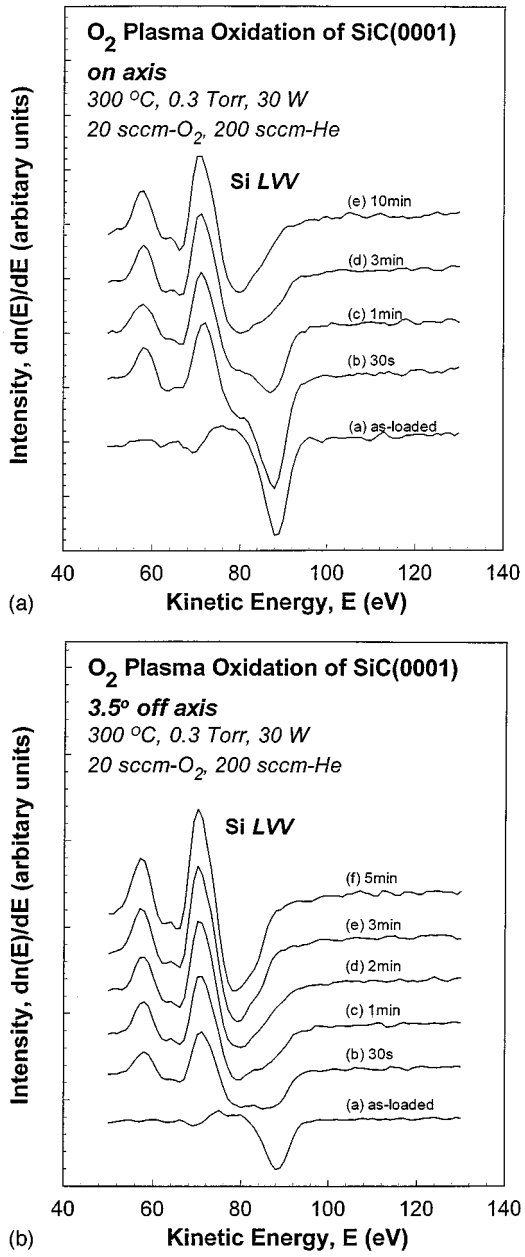

FIG. 3. Changes in the Si_{LVV} AES features as a function of the oxidation time for (a) flat and (b) vicinal SiC surfaces for O_2 RPAO.

The oxide thickness can be obtained to $\pm 5\%$ from the relative intensity changes in the C_{KVV} feature using the characteristic escape depth of 0.96 nm for 275 eV electrons. A similar approach has been applied for the determination of the oxide thickness for the RPAO process on Si, and has been validated by a direct measurement of oxide thickness by cross-sectional high resolution transmission electron microscopy.

Figures 6(a) and 6(b) shows log-log plots, respectively of the oxide thickness versus the oxidation time for the RPAO of (a) Si and (b) SiC for the O_2 source gas. In each instance the data can be fit by a power law dependence of the form, $t_{ox}=At^b$, where t_{ox} is the oxide thickness in nm, t is the oxidation time in minutes, and A and b are fit

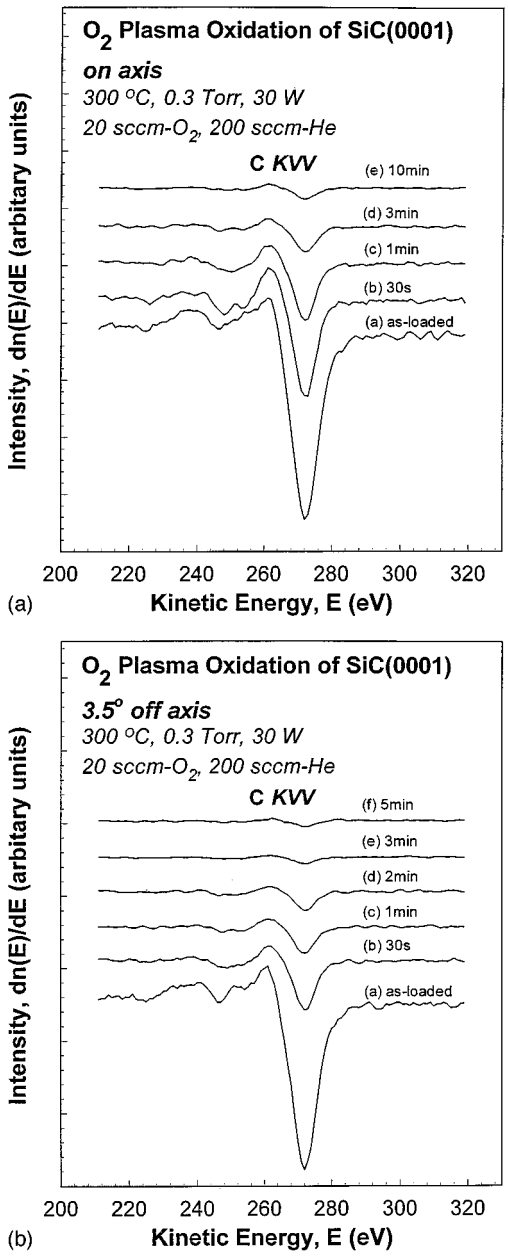

FIG. 4. Changes in the C_{KVV} AES features as a function of the oxidation time for (a) flat and (b) vicinal SiC surfaces for O_2 RPAO.

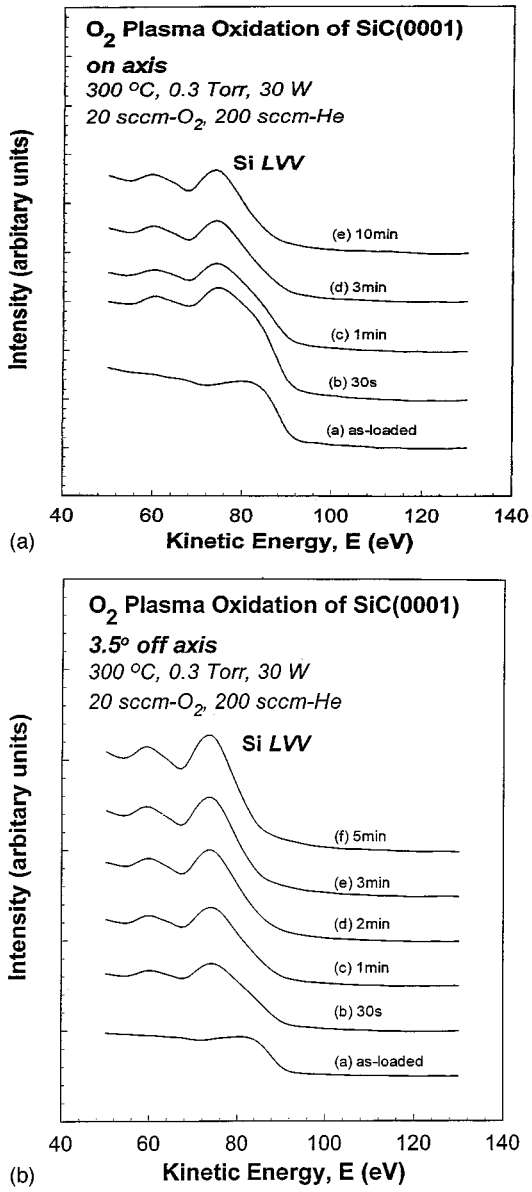

FIG. 5. Integral, n(E), Si_{LVV} AES spectra as a function of the O_2 RPAO oxidation time for (a) flat and (b) vicinal SiC surfaces.

parameters.[12,13] The initial oxidation rates are about one and one-half times faster for the vicinal than for the flat wafers, and the initial oxidation rates are faster for Si than for SiC. However, the power law exponents for the SiC oxidations for both flat and vicinal surfaces are greater than the corresponding exponential factor for Si; however, all of the these power law exponents are less than 1. The relative differences in the power law factors means that at long times of about 10 min or more the thicknesses of the oxides formed on both Si and SiC are comparable for both the flat and vicinal wafers. Figure 7 illustrates this by showing a comparison of oxide thickness versus oxidation time for flat Si and SiC; a similar situation also prevails for the oxidation of the off-axis wafers.

Finally for the RPAO of Si using the same relative flow rates of N_2O and O_2, the oxide growth rate was slower by a factor of 2 using the N_2O source gas.[12] Comparisons of RPAO rates have also been made for SiC for plasma excited O_2 and N_2O source gases. For the same relative flow rates of these two source gases, the situation is reversed with respect to Si, i.e., the oxidation rate of SiC is greater using the N_2O source gas. This increased growth rate using plasma excited species from the N_2O discharge is illustrated in Fig. 8 for the RPAO of flat SiC wafers.

IV. DISCUSSION AND SUMMARY

A. AES results

The analysis of the AES spectra for the flat and vicinal SiC surface RPAO processes using the O_2 source gas indicates:

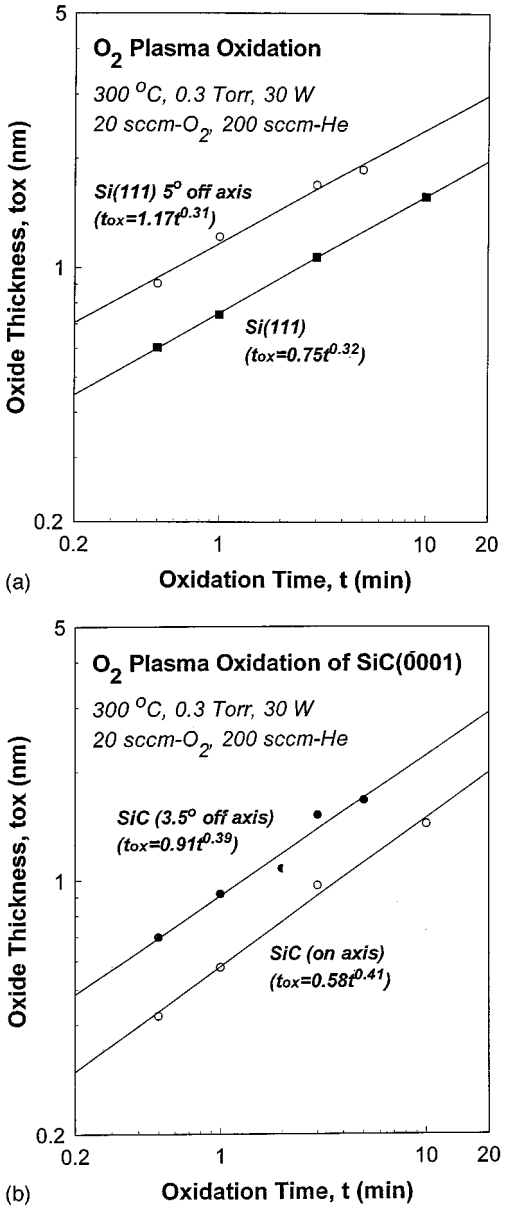

FIG. 6. Log-log plots of the oxide thickness versus the oxidation time for the O_2 RPAO of flat and vicinal (a) Si and (b) SiC. The data are fit to a power law dependence, $t_{ox}=at^b$.

(i) the solid state oxidation product is SiO_2;
(ii) there are no interfacial C-O bonds; and
(iii) oxidation proceeds initially more rapidly on vicinal surfaces than on flat surfaces, paralleling what has been found for Si.

The primary solid state oxidation product for thermal oxidation of SiC is also SiO_2; however, there have been reports of the observation of C–O at or near the SiC–SiO_2 interface.[3] This means that there are significant differences in the oxide formation chemistries by low temperature plasma assisted and high temperature thermal oxidation processes. For example, in the plasma assisted processes the oxidation species are typically long-lived molecular metastables such as O_2^* or positive molecular ions such as O_2^+, whereas in the thermal

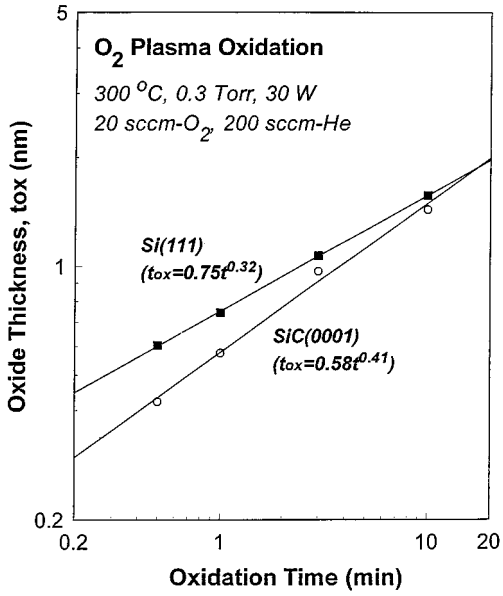

FIG. 7. Log-log plots comparing oxide thickness versus the oxidation time for the O_2 RPAO of flat Si and SiC. The data are fit to a power law dependence, $t_{ox}=at^b$.

oxidation process the oxidation species are typically O atoms. Since the thermal and plasma oxidation processes are qualitatively different with respect to the formation of C–O bonds, then the differences between the two types oxidation processes could be expected to require different post-oxidation and post-deposition procedures for forming low defect density SiC–SiO_2 interfaces. However, this is not the case, as is discussed in Sec. IV B of the article. Before dis-

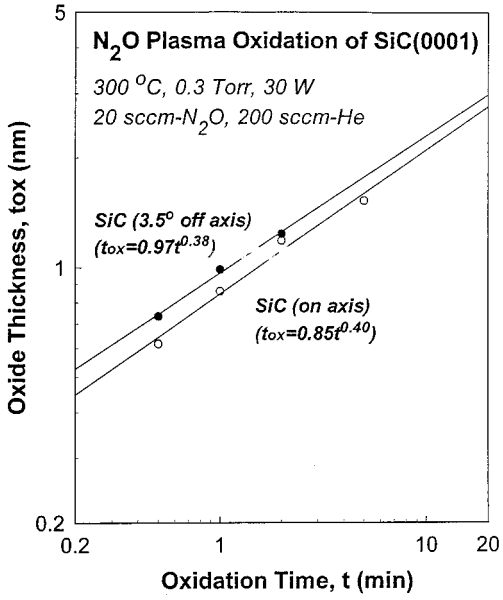

FIG. 8. Log-log plots comparing the oxide thickness versus the oxidation time for the RPAO of flat SiC using O_2 and N_2O as the oxygen atom source cases. The data are fit to a power law dependence, $t_{ox}=at^b$.

cussing this aspect of the experimental results, additional aspects of the power laws fits are discussed below.

The power laws fits to RPAO data show that the oxidation process proceeds very rapidly initially and then slows down considerably with increasing oxidation time. This means chemical reaction rates between excited oxygen species and Si- and Si- and C atom dangling bonds on Si and SiC, respectively, are decreased after Si–O bonds and a superficial layer of SiO_2 are formed at the onset of RPAO.[14]

For the case of RPAO of Si the oxidation rate for flat surfaces is faster using O_2 than N_2O for the same relative flow rates of He and O_2 or N_2O. For the RPAO of SiC the situation is reversed for flat surfaces and the oxidation rate is faster using N_2O. Studies are currently underway to address this difference. A model has been proposed for RPAO of Si that explains the differences in the oxidation rates using O_2 or N_2O source gases.[15] This model was developed primarily to explain the retention of nitrogen atoms at the Si–SiO_2 interface during oxide growth using the N_2O source gas. The surface contamination of SiC by nitrogen makes it impossible to determine whether there is nitrogen retention at the SiC–SiO_2 interface during oxide growth in N_2O. This issue is presently under study, and will require the development of procedures for *ex situ* surface preparation that remove residual nitrogen atom contamination from the SiC surface.

B. Electrical properties of SiC–SiO_2 interfaces

This section summarizes results of recent electrical measurements made on MOS capacitors, in particular it compares values of D_{it} as extracted from capacitance-voltage measurements on SiC interfaces prepared on *p*-type substrates. The experimental studies of Stein von Kaminski *et al.*[11] have demonstrated mid-gap D_{it} values in the low 10^{11} cm^{-2} eV^{1} range for interfaces prepared by high temperature thermal oxidation. These device structures used metal electrodes. The attainment of low defect densities required two annealing steps:

(i) a post-oxidation an Ar/H_2 mixture at 1150 °C, and
(ii) a conventional PMA in an H_2 containing ambient at 400 °C after metallization.

When annealing procedures that did not include H_2 in the 1150 °C anneal were applied to the RPAO formed interfaces, the D_{it} values were significantly higher, in the 10^{13} cm^{-2} eV^{-1} range.[7] However as shown in Ref. 8, these D_{it} values were significantly reduced for the RPAO interfaces following a high temperature (1150 °C) anneal in an Ar/H_2 mixture. It is interesting to note that the difference in D_{it} values between RPAO devices subjected to the Ar and Ar/H_2 anneals is very nearly equal to the density of carbon atom dangling bonds at the step edges. This suggests the possibility that carbon atom dangling bonds are not terminated by during the oxidation or oxide deposition steps, or during the conventional PMA.

Consider first the RPAO interfaces. Since our studies show no C–O bonding in interfacial regions for either the flat or vicinal wafers, it is suggested that the step edge carbon atom dangling bonds may remain unterminated after the oxidation process. The high defect density after the conventional 400 °C PMA in a hydrogen containing ambient further suggests that the step edge carbon atom dangling bonds are not hydrogen terminated by this process. If this is the case then hydrogen atom production during the 1150 °C anneal in Ar/H_2 is sufficiently high to produce C–H bonding at the step edges. Since thermal oxidation processes show evidence for C–O bonding in interfacial transition regions[3] and the RPAO process does not, this suggests that there might be differences related to the way step carbon atom dangling bonds are terminated, either during thermal and plasma oxidations, or in post-oxidation annealing. However, this appears not to be the case, since interfaces produced by high temperature thermal oxidation also require a high temperature anneal in an H_2 containing ambient. This means that even though C–O bonds can be found in silicon oxycarbide transition regions after high temperature thermal oxidation[3] they may not be formed in sufficient numbers at carbon atom step edges to neutralize dangling bond defects. Alternatively, the local bonding environment of carbon atoms in interfacial regions and at the Si–C step edges is different and may be a contributing factor to oxygen atom termination.

Finally, it is also interesting to note that fabrication of low D_{it} interfaces on n-type SiC by RPAO and thermal oxidation does not require a high temperature anneal in an H_2 containing ambient.[7] There are two possible explanations for not requiring such an anneal for the RPAO formed interfaces:

(i) the active interfacial defects are in the bottom half of the SiC band gap and hence are more active in *p*-type material, or
(ii) the formation of C–O bonds at an SiC interface is Fermi level dependent favoring C–O bond formation in *n*-type material.

The wafers that we studied were nitrogen doped *n*-type wafers, and there was no evidence of interfacial C–O bond formation. However, the concentration of step edge C atom danglings bonds that are available for termination by C–O bonding is below the AES detection limit. 6H SiC flat and vicinal SiC wafers with C faces have been ordered from Cree Research, Inc., upon their receipt, an AES study of the initial stages of PRAO will be initiated. It is clear that these questions identified with respect to electrical results on SiC devices need additional experimental and theoretical studies before they can be satisfactorily resolved. In particular, electron spin resonance experiments that can readily distinguish between Si and C atom dangling bonds may be helpful in resolving the issues discussed in the last two paragraphs.

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