# New approach for the fabrication of device-quality $Ge/GeO_2/SiO_2$ interfaces using low temperature remote plasma processing

R. S. Johnson
*Department of Physics, North Carolina State University, Raleigh, North Carolina 27695-8202*

H. Niimi
*Department of Materials Science and Engineering, North Carolina State University, Raleigh, North Carolina 27695-8202*

G. Lucovsky[a)]
*Departments of Physics, Materials Science and Engineering, and Electrical and Computer Engineering, North Carolina State University, Raleigh, North Carolina 27695-8202*

(Received 10 January 2000; accepted 3 April 2000)

It has been shown that low temperature (300 °C) remote plasma enhanced processing can separately and independently control interface formation and bulk oxide deposition on silicon substrates. Plasma processing is followed by a low thermal budget thermal anneal, e.g., 30 s at 900 °C. In this article, this process has been modified and applied to germanium substrates to determine if it can provide a successful pathway to device-quality Ge–dielectric interfaces. The new process also employs a three-step process: (i) an $O_2$/He plasma-assisted, predeposition oxidation of the germanium surface to form a superficial germanium–oxide passivating film, (ii) deposition of a $SiO_2$ bulk film by remote plasma-enhanced chemical vapor deposition from $SiH_4$ and $O_2$, and (iii) a postdeposition anneal for chemical and structural relaxation. The resulting interfaces are improved by the predeposition, plasma-assisted oxidation step, but are still far too defective for device applications. © *2000 American Vacuum Society.* [S0734-2101(00)13304-4]

## I. INTRODUCTION

Previously there have been several different approaches attempted to produce device quality metal–oxide–semiconductor (MOS) devices using germanium as the semiconductor substrate. Germanium nitrides and oxynitrides have been integrated in MOS and devices, including MOS field effect transistors, MOSFETs.[1–3] While deposited silicon dioxide, $SiO_2$, has been extensively studied as a dielectric both on silicon and germanium, its use on germanium has proven considerably less effective than on Si.[4–8] For example, Vitkavage *et al.*[9] used remote plasma techniques to deposit a thin layer of Si onto hydrogen plasma cleaned germanium surfaces to act as a buffer layer for the silicon dioxide deposition. The silicon buffer layer prevented subcutaneous oxidation of the germanium substrate during the low temperature remote plasma enhanced chemical vapor deposition, RPECVD, of the silicon dioxide film. Compared with the direct deposition of $SiO_2$ onto germanium, the density of interface traps, $D_{it}$, was improved by an order of magnitude.

Following this article, it has been shown that *in situ* hydrogen plasma cleaning of silicon damages the semiconductor surface, resulting in electrically active defect sites.[10] Instead a remote plasma oxidation step has been used to clean and passivate the silicon surface prior to the $SiO_2$ deposition. High resolution transmission electron microscopy (HRTEM) studies of hydrogen cleaned Si(100) surfaces indicated a root mean squared (rms) roughness of 0.6 nm and a spatial frequency of about 3.5 nm, while preoxidized surfaces had a rms roughness of about 0.3 nm and spatial frequency of about 10 nm. The predeposition plasma-assisted oxidation step also typically decreased $D_{it}$ from $1–3\times10^{-11}$ $cm^{-2}$ $eV^{-1}$ to $1\times10^{-10}$ $cm^{-2}$ $eV^{-1}$. The predeposition oxidation also stabilized the Si-dielectric interface, as has been demonstrated by studies where the deposition process conditions were varied while the preoxidation step process conditions were held constant. These studies indicated there was essentially no dependence of the $D_{it}$ values on deposition conditions, while the same study, with hydrogen cleaning instead of a preoxidation step, showed large variances in the $D_{it}$ values.[10]

In this article, we have used RPECVD to deposit silicon dioxide on germanium wafers with, and without, a remote plasma predeposition oxidation step similar to what had been previously used in Ref. 10 for Si. MOS capacitors were then fabricated by conventional techniques, and capacitance–voltage and current–voltage measurements were preformed to evaluate the effectiveness of the predeposition plasma-assisted oxidation step.

## II. EXPERIMENT

### A. Sample preparation

The substrate samples were *n*-type Ge(111) with a resistivity of $\sim$0.4 Ω cm. The samples were cleaned in four separate baths. Bath one was bromine (1%) in methanol for 2 min. This combination has been shown by ellipsometry to produce the smoothest and most oxide free surface, between the substrate and ambient, when used as the etch in a chemical-mechanical polishing step.[11] Bath two was a

[a)]Electronic mail: gerry_lucovsky@ncsu.edu

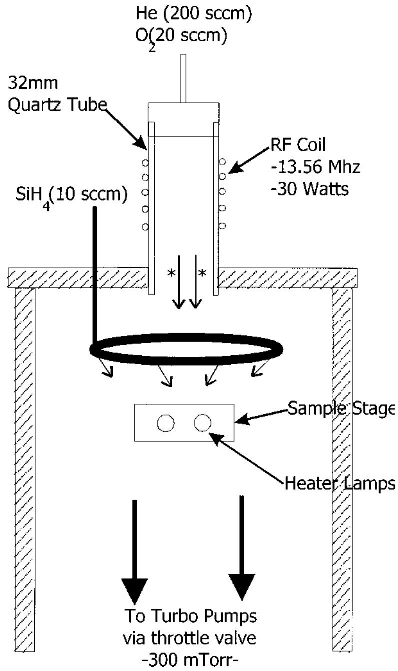


FIG. 1. Diagram of the RPECVD chamber used for the oxidation and deposition steps.

methanol bath for 20 s; this was used to rinse away any residual bromine from bath one. Baths three and four were used to remove residual Ge oxides: (i) bath three was a 60 °C de-ionized water bath for 5 min, and (ii) bath four was an ammonium hydroxide ($NH_4OH$) soak for 2 min. The germanium wafers were then rinsed for 20 s in de-ionized water to remove any $NH_4OH$ residues from bath four. Samples were blown dry with dry nitrogen and loaded into the processing/analysis system load lock within 5 min of the last deionized water rinse. Based on an on-line Auger electron spectroscopy (AES) measurement, discussed in the next subsection, these samples typically displayed small amounts of carbon and oxygen contamination, in the monolayer to submonolayer regime.

## B. Deposition process

For comparisons with preoxidized substrates, silicon dioxide was deposited directly onto to the germanium substrates using a remote plasma enhanced chemical vapor deposition (CVD) process.[12] The remainder of the germanium substrates were treated with a preoxidation step. For this predeposition, plasma-assisted oxidation step, helium and oxygen were introduced through the quartz plasma tube and excited with 30 W of 13.56 MHz rf power (see Fig. 1). The excited gases were transported from the plasma generation region to the substrate where plasma-assisted oxidation of the surface was accomplished at process pressure of 300 mTorr, and at a substrate temperature of 300 °C. The oxidation time was 15 s, and based on the AES spectra in Fig. 2, as well as previous experience with plasma-assisted oxidation of Si, the oxide layer thickness was estimated to be at most 0.5–0.6 nm.

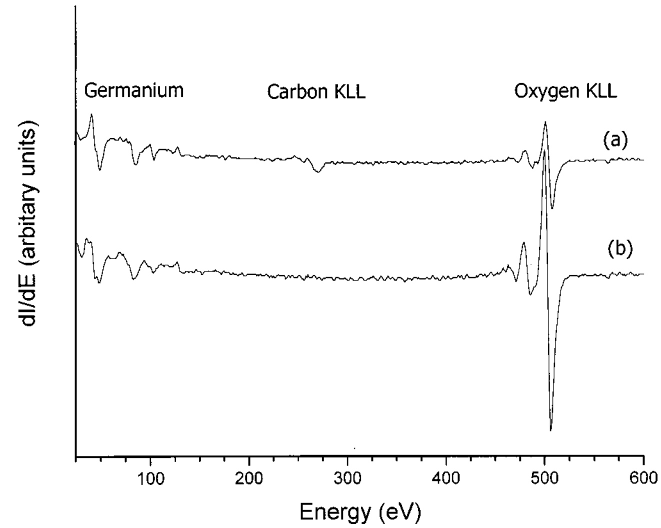


FIG. 2. Differential AES spectra of the Ge(111) surface: (a) after chemical cleaning; and (b) after 15 s of oxidation.

The AES results in Fig 2 show spectra before and after the predeposition plasma oxidation step, and indicate reduction of the carbon *KLL* peak below the level of AES detection. In addition the oxygen signal increases and the line shape of the germanium changed confirming that oxidation of the germanium surface had occurred. As the oxidation time increased, the intensity of the $Ge_{MVV}$ peak at 48 eV decreased while the Ge–$O_{MVV}$ peak at 44 eV increased (see Fig. 3).

The evolution of these two peaks demonstrates that the bonding environment of the evolved from one where Ge atoms have only Ge nearest neighbors (at ~48 eV) to one where the Ge atoms are bonded to oxygen (at ~44 eV). A plot of the ratio of these two peak heights versus log(time) in Fig. 4 indicates an almost linear dependence. This is very similar to what has been reported by our group for a similar

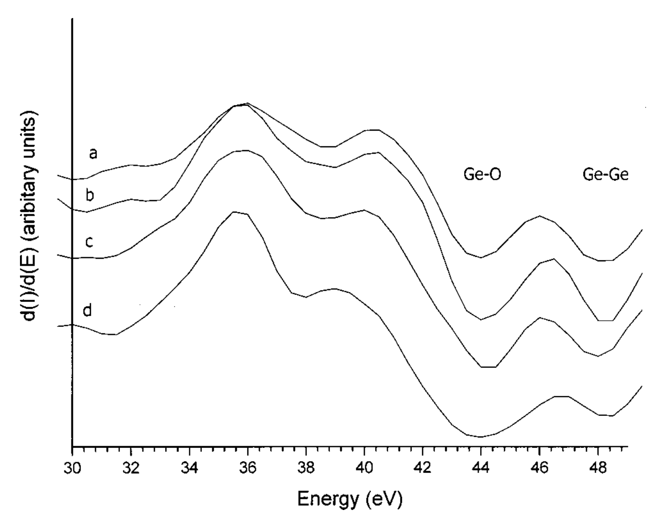


FIG. 3. AES of germanium–oxygen (44 eV) and germanium–germanium (48 eV) signals for (a) 15 s, (b) 30 s, (c) 3 min, and (d) 10 min of plasma-assisted oxidation.

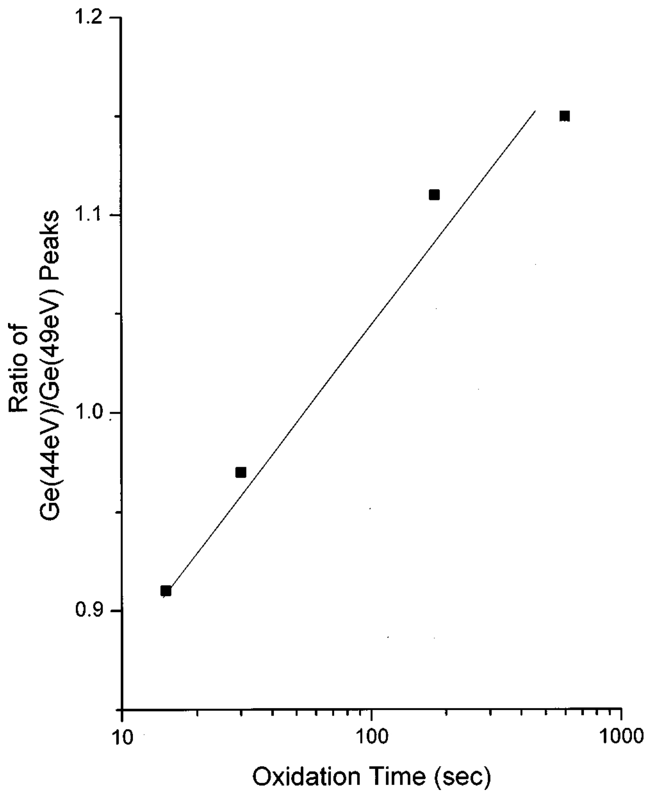


FIG. 4. Ratio of the Ge–O/Ge–Ge peaks vs oxidation time.

plasma-assisted oxidation of silicon.[12] In particular, the linear dependence versus log(time) is indicative of an oxidation process that is effectively self-limiting.

After a remote plasma-assisted oxidation for 15 s, a silicon dioxide layer about 4–5 nm thick was deposited by RPECVD. For this process, in addition to helium and oxygen being introduced through the plasma tube, 2% silane in helium was injected through the dispersal ring located directly above the substrate (see Fig. 1). This downstream injection of silane prevented it from being directly excited by the plasma. This was due to (i) the point of injection, (ii) gas flow rate of oxygen and helium through the plasma tube, and (iii) the process pressure. The CVD reaction responsible for deposition occurred at the oxidized Ge substrate surface and was between plasma-excited oxygen species and nonexcited or fragmented silane.[13] The substrate temperature was held at 300 °C; the process pressure was 300 mTorr, and the rf power at 13.56 MHz applied to the plasma was 30 W. The deposition time was 4 min giving an estimated film thickness of $4.6\pm0.5$ nm of silicon dioxide as determined from analysis of capacitance–voltage, $C$–$V$ data.

In applications where the substrate is silicon, not germanium, the resulting structure is annealed at 900 °C for 30 s. This anneal promotes structural and chemical relaxation of the silicon dielectric interface and the silicon dioxide layer.[14] In the case of germanium, the substrate melts at 937 °C and the interfacial germanium oxide layer decomposes to form gaseous GeO at about 450 °C. We found that any sample annealed at 600 °C was visibly damaged by being subjected

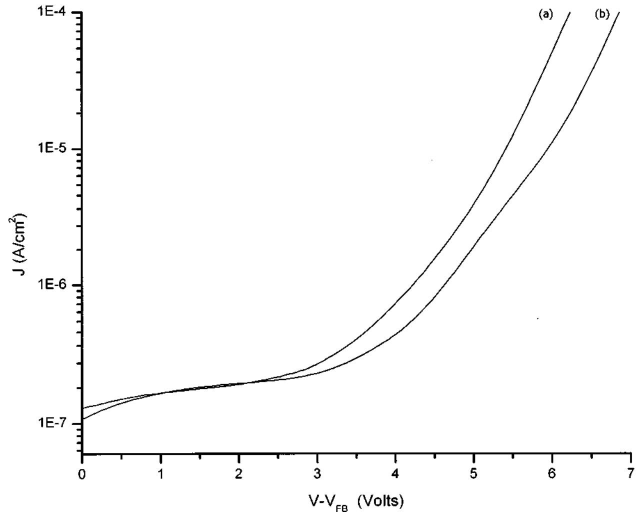


FIG. 5. Leakage current density vs gate voltage. (a) No preoxidation, (b) 15 s of preoxidation.

to this anneal. For example, the sample either showed physical signs of melting, bubbling and deformation, or the resulting MOS capacitors were shorted.

### C. Electrical measurement of MOS structures

MOS capacitors were fabricated by evaporating aluminum dots onto the silicon dioxide layer through a shadow mask. The masks were constructed by Towne Technologies and had apertures of 50–500 $\mu$m. The dot sizes were measured using an optical microscope with a digital camera attached. The backside contact to the Ge wafer was aluminum. After metallization the samples were subjected to a postmetallization anneal (PMA) at 400 °C in forming gas for 30 min.

The $I$–$V$ data of Fig. 5 are representative of the MOS devices prepared in this way. The onset of current in both types of devices at about 3 V and the preoxidized samples increases slightly slower than the nonpreoxidized sample. An analysis of the leakage current based on the functional dependence expected for Fowler–Nordheim tunneling[15] in the region from 3 to about 6 V indicates that there is more current than is expected and that the current increases more slowly with increasing bias voltage. Therefore, we interpret the onset of current flow as being associated with a soft, but otherwise unspecified, breakdown/leakage process. $C$–$V$ curves of both a preoxidized sample and a nonpreoxidized sample show about the same capacitance in the substrate accumulation bias regime (see Fig. 6). However, the nonplasma-oxidized sample has a flatband voltage of about +0.8 V while the plasma-oxidized sample flatband voltage has about +0.3 V. Based on the Fermi level position for substrate doping and the use of an Al gate electrode, the anticipated flatband voltage is approximately −0.4 V. The positive shifts of flat band voltage for both types of samples are indicative of fixed negative charge, or equivalently filling of electron traps at the Ge–dielectric interface. The larger shift for the nonplasma-oxidized sample is indicative of a more defective interface, either from a higher density of

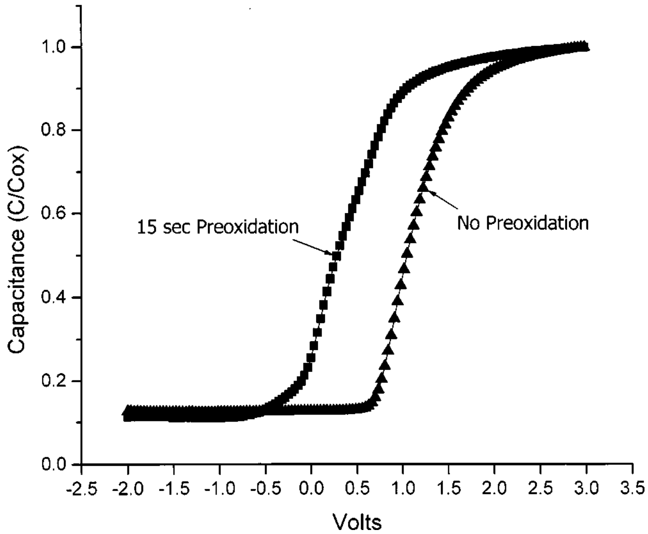


FIG. 6. Capacitance versus voltage for devices with a preoxidation plasma-oxidized interface and without a preoxidation plasma-oxidized interface. (a) 15 s of preoxidation ($V_{FB}$=0.294 V), (b) no preoxidation ($V_{FB}$=0.812 V). Oxide thickness as calculated from oxide capacitance, 46±5 Å.

fixed negative charge, or from a higher density of interface traps. In either case the electrical quality of either of these interfaces is significantly poorer than Si–$SiO_2$ interfaces, and well below a threshold for applications in MOS devices.

The transition region between substrate depletion at negative gate voltages and accumulation at positive gate voltages shows less distortion from an ideal *C–V* curve for the sample without the predeposition oxidation treatment. For the sample with a predeposition oxidation treatment there are two different slopes in this transition region, which can be indicative of integration through two different defect states. A comparison of the two *C–V* curves with what is expected for a device quality interface with respect to flatband voltage and distortion indicates that neither can be characterized as device quality.

## III. CONCLUSIONS

Contrary to experience with deposited $SiO_2$ on Si substrates, where the predeposition plasma-assisted oxidation passivates the interface and prevents further oxidation of the Si substrate during silicon dioxide deposition, yielding device-quality interfaces for MOS structures, the same processing sequences applied to Ge yield significantly poorer interface electrical properties as determined from *C–V* data. While the predeposition step did ''clean'' the surface it produced an oxidized Ge interface that when combined with deposited $SiO_2$ resulted in poor quality *C–V* traces. The poor electrical quality of the interface means that neither intentionally grown Ge oxide, as formed by the predeposition plasma-assisted oxidation, nor subcutaneous formation of Ge oxide that occurs during $SiO_2$ deposition generates a device-quality interface. The difference between the two *C–V* traces indicates that different defect states result from these two processes.

## ACKNOWLEDGMENTS

This research has been supported in part by the Office of Naval Research, and the Air Force Office of Scientific Research.

[1]Q. Hua, J. Rosenberg, J. Ye, and E. S. Yang, J. Appl. Phys. **53**, 8969 (1982).
[2]D. J. Hymes and J. Rosenberg, J. Electrochem. Soc. **135**, 961 (1988).
[3]D. B. Alford and L. G. Meiners, J. Electrochem. Soc. **134**, 979 (1987).
[4]J. J. Rosenberg and S. C. Martin, IEEE Electron Device Lett. **9**, 639 (1988).
[5]T. O. Sedgwick, J. Appl. Phys. **39**, 5066 (1968).
[6]K. L. Wang and P. V. Gray, J. Electrochem. Soc. **123**, 1392 (1976).
[7]T. Yashiro, Jpn. J. Appl. Phys. **9**, 740 (1970).
[8]M. D. Jack and J. Y. M. Lee, J. Electron. Mater. **10**, 571 (1981).
[9]D. J. Vitkavage, G. G. Fountain, R. A. Rudder, S. V. Hattangady, and R. J. Markunas, Appl. Phys. Lett. **53**, 692 (1988).
[10]G. Lucovsky, J. J. Wortman, T. Yasuda, X.-L. Lu, V. Misra, S. V. Hattangady, Y. Ma, and B. Hornung, J. Vac. Sci. Technol. B **12**, 2839 (1994).
[11]D. E. Aspnes and A. A. Studna, Appl. Phys. Lett. **39**, 316 (1981).
[12]T. Yasuda, Y. Ma, S. Habermehl, and G. Lucovsky, J. Vac. Sci. Technol. B **10**, 1844 (1992).
[13]D. V. Tsu, G. N. Parsons, G. Lucovsky, and M. W. Watkins, J. Vac. Sci. Technol. A **7**, 1115 (1989).
[14] B. J. Hinds, F. Wang, D. M. Wolfe, C. L. Hinkle, and G. Lucovsky, J. Vac. Sci. Technol. B **16**, 2171 (1998).
[15]D. K. Schroder, *Semiconductor Material and Device Characterization*, 2nd ed. (Wiley, New York, 1998).