Separate and independent reductions in direct tunneling in oxide/nitride stacks with monolayer interface nitridation associated with the (i) interface nitridation and (ii) increased physical thickness

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Direct tunneling limits aggressive scaling of thermally grown oxides to about 1.6 nm, a thickness at which the tunneling current density J_g at 1 V is ~1 A/cm^2. This article demonstrates that stacked gate dielectrics prepared by remote plasma processing and including (i) ultrathin nitrided SiO_2 interfacial layers and (ii) either silicon nitride or oxynitride bulk dielectrics can extend the equivalent oxide thickness to 1.1–1.0 nm before J_g exceeds 1 A/cm^2. Significant reductions in direct tunneling are derived from (i) interface nitridation at the monolayer level and (ii) the increased physical thickness of the nitride or oxynitride alloy layers. The ''portability'' of the interface contribution is demonstrated by combining the nitrided SiO_2 interface layers with transition-metal oxides, e.g., Ta_2O_5, in stacked gate dielectric structures and obtaining essentially the same reductions in tunneling current on *n*- and *p*-type substrates with respect to non-nitrided plasma-grown interface layers. [S0734-2101(00)18304-6]

I. INTRODUCTION

Scaling of Si complementary metal-oxide semiconductor (CMOS) devices to smaller feature sizes to achieve increases in device speed and integration requires increases in gate dielectric capacitance, which must be accomplished by reducing the equivalent oxide thickness (EOT) of the gate dielectric to less than 1 nm. Direct tunneling limits scaling of thermally grown oxides and nitrided oxides to approximately 1.5–1.6 nm, a thickness regime in which direct tunneling current at ~1 V in inversion bias generally exceeds 1 A/cm^2, as for example, in microprocessor applications for desk-top computers.[1] Significantly lower direct tunneling currents, ~10^{-3} A/cm^2, are required for battery-operated devices. The requirement of reduced tunneling has stimulated considerable research in alternative insulators with dielectric constants *k* greater than SiO_2. This is based on an assumption that increased physical thickness will significantly reduce the direct tunneling current while at the same time meet targeted goals for increased capacitance or decreased EOT through the increases in *k*. The transition to alternative gate dielectrics can proceeded in two steps: (i) the implementation of stacked gate dielectrics comprised of SiO_2 interface layers and either Si-nitride or oxynitride bulk dielectrics,[2–5] followed by (ii) the substitution of alternative high-*k* oxides or silicates, such as $Zr(Hf)O_2–SiO_2$ (Refs. 6 and 7) or Ta_2O_5 (Refs. 8 and 9) for the nitrides or oxynitride alloys. Direct substitution of plasma-deposited nitrides for oxides without an interfacial oxide layer has been shown to degrade field-effect transistor (FET) drive currents in *n*-channel devices by about a factor of 2, and in *p*-channel devices by more than a factor of 10,[10,11] thereby nullifying any gains from the increased capacitance. The insertion of ~0.5–0.6 nm of a plasma-grown interfacial oxide with or without monolayer scale interface nitridation, between the Si substrate and the bulk nitride dielectric layer, restores *n*-type MOS (NMOS) and *p*-type MOS (PMOS) FET drive currents to essentially the same values as in devices with oxide gate dielectrics of the same EOT.[10,11] Similar improvements in interface-controlled electrical properties have been obtained with

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transition-metal-oxide bulk dielectrics as demonstrated in this article for Ta_2O_5 on both *n*- and *p*-type Si(100) substrates.

II. EXPERIMENTAL RESULTS

Stacked dielectric layers have been prepared by 300 °C remote plasma processing, including; (i) interface formation and monolayer interface nitridation,[12,13] followed by (ii) remote plasma-assisted deposition of nitride and oxynitride alloy films.[14,15] Analysis of nitrided interface layers by secondary ion mass spectrometry (SIMS) and nuclear reaction analysis (NRA) were used to identify the process conditions that resulted in monolayer nitridation, i.e., a concentration of nitrogen atoms, $7\pm1\times10^{14}\,\mathrm{cm}^{-2}$, that equals the concentration of Si atoms on a (100) surface. After plasma processing, dielectric stacks were subjected to an *in situ* rapid thermal anneal for 30 s at 900 °C in an inert gas atmosphere (e.g., He or Ar at ~1–2 mTorr). This was followed by (i) deposition of polycrystalline Si gate electrodes, ion implantation of As or B at a dose of $\sim5\times10^{-15}\,\mathrm{cm}^{-2}$, and dopant activation annealing at 1000 °C for about 60 s. Device structures were then completed by conventional processing steps, including photolithography, wet/dry etching, and postmetallization annealing (PMA). Devices were also fabricated with SiO_2 and Ta_2O_5 films deposited at 300 °C by remote plasma processing. The down-stream injected source gases for the respective SiO_2 and Ta_2O_5 depositions were silane and Ta ethoxide. These devices had Al gate electrodes, but the PMAs were done prior to deposition of Al gates to prevent chemical reactions between the Ta_2O_5 dielectrics and the Al electrode.

Capacitance–voltage ($C-V$) and current–voltage ($I-V$) were made using Hewlett Packard HP 4248A and HP 4155B/41546B, respectively. The values of EOT were obtained from analysis of 100 kH $C-V$ data including corrections for polysilicon depletion and potential drops in the channel region.[16] This article (i) demonstrates separate and independent contributions for reduction of direct tunneling from interface nitridation and physically thicker bulk dielectric layers, (ii) compares direct tunneling for nitrides and oxynitride alloys relative to oxides, and (iii) demonstrates improvements in $C-V$ and $I-V$ properties obtained by incorporating plasma-grown oxide and monolayer-nitrided oxide interface layers in devices with Ta_2O_5 bulk dielectrics.

Figures 1(a), 1(b), and 1(c), respectively, illustrate reductions of direct tunneling derived from (i) monolayer interface nitridation[12,13] and (ii) incorporation of physically thicker nitride layers into stacked dielectrics, and then from (iii) a combination of monolayer interface nitride and incorporation of physically thick nitride layers in stacked structures. Reductions in direct tunneling at about a 1 V bias across the dielectric are (i) a factor of ~10 for interface nitridation for substrate accumulation at EOTs of ~2 and 3 nm, (ii) a factor of ~10 for EOT of ~1.9 nm, for different ratios of nitride-to-oxide thickness from ~4:1 and 0.67:1, and (iii) a factor of more than 200 for EOT ~1.6 nm, for the *combination* of interface nitridation, and increased physical thickness. The effects of interface nitridation in the direct tunneling regime

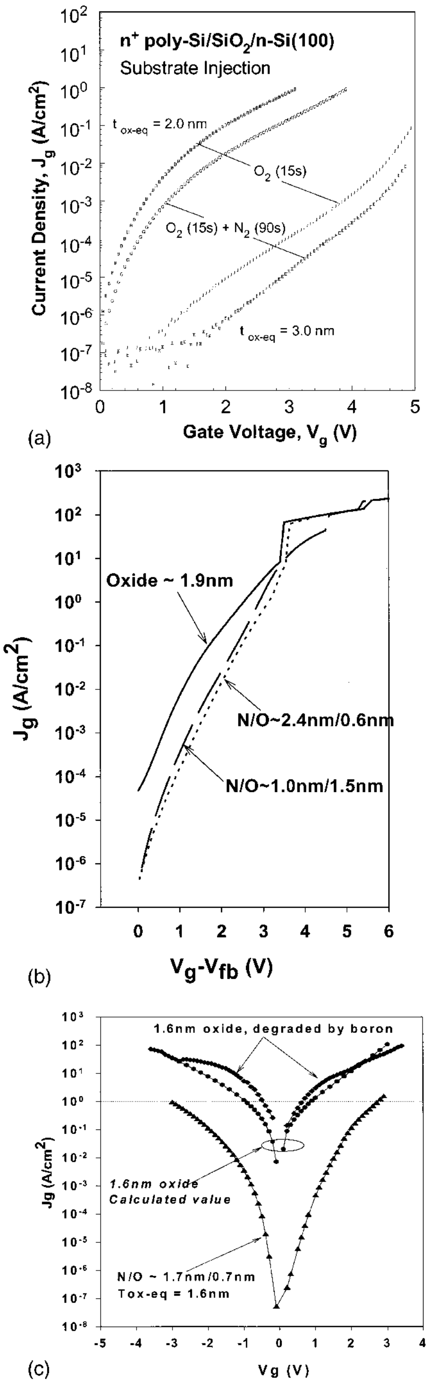

FIG. 1. (a) Current density–gate voltage ($J-V$) plots for MOS capacitors with EOT ~2 and 3 nm. (b) $J-V$ characteristics of MOS capacitors with plasma-deposited nitride/oxide (N/O) stacks compared to device with a homogeneous oxide layer (EOT~1.9 nm). (c) $J-V$ characteristics for a PMOS FET compared to a device with a homogeneous oxide for EOT~1.9 nm.

have been found to be the same for both substrate accumulation and inversion using FET devices with grounded and connected source and drain contacts and with an appropriate sign of bias voltage applied to the gate electrode.[15] These reductions in direct tunneling are effectively independent of oxide thickness in range that extends from at least 2 to 3 nm for devices with bulk oxide dielectrics, and down to ~1 nm for devices with Ta_2O_5, as shown in Fig. 2(b). Interface ni-

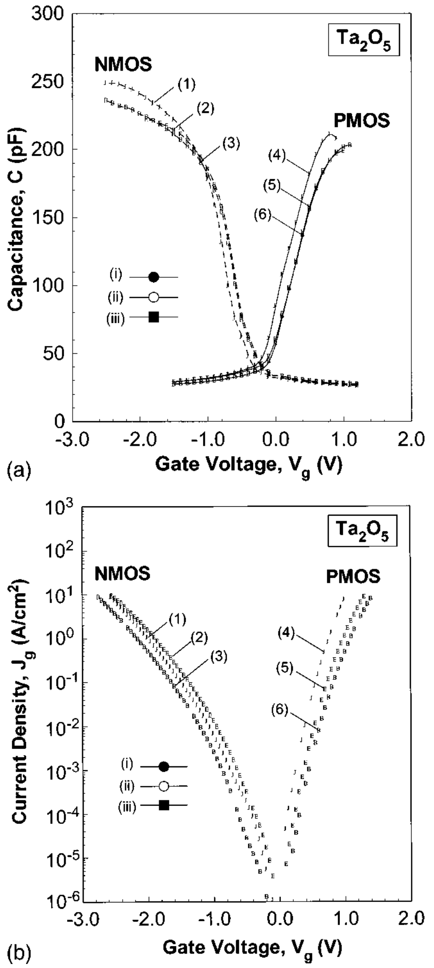

FIG. 2. (a) $C-V$ and (b) $J-V$ characteristics for devices with plasma-deposited Ta_2O_5. The solid squares are for direct deposition onto HF-last Si, and the other solid and open characters are for devices with nitride and non-nitride plasma-grown $Si-SiO_2$ interfaces. The $C-V$ curves for the PMOS capacitors have not been plot for an accumulation bias of more than about 1 V due to significant leakage current [see (b)]. The solid circles are for deposition onto HF-last Si, the open circles for a RPAO SiO_2 layer, and the solid squares are for monolayer nitrided RPAO SiO_2. The EOT values for the traces labeled (1)–(6) are: (1) 1.09 nm, (2) 1.20 nm, (3) 1.17 nm, (4) 1.19 nm, (5) 1.30 nm, and (6) 1.29 nm.

tridation also reduces tunneling in the Fowler–Nordheim regime but by different amounts depending on the bias, ~6–10 for gate injection, and more than 50 for substrate injection.[15] In Fig. 1(b), the approximately equal reductions of tunneling in (ii) different nitride-to-oxide ratios is consistent with the tunneling mass of electrons in the nitride films being reduced by a factor of about one half with respect to the tunneling mass of electrons in SiO_2, from $\sim 0.55\, m_0$ for SiO_2 to $\sim 0.25\, m_0$ for Si_3N_4, where m_0 is the free-electron mass.[15] These tunneling mass values are in effect fitting parameters obtained by assuming conduction-band offset energies of 3.15 and 2.15 eV, respectively, for $Si-SiO_2$ and $Si-Si_3N_4$. The effective mass fit parameter for Si_3N_4 is smaller than values quoted elsewhere for films produced by other chemical-vapor deposition (CVD) techniques,[17,18] and is assumed to reflect the relatively high concentration of bonded hydrogen in the nitrides prepared by remote plasma-enhanced chemical-vapor deposition (RPECVD) ~10–15 at. % after annealing/thermal exposure at 1000 °C.[19] Figure 1(c) demonstrates a tunneling current reduction of more than 200 with respect to SiO_2 for a device with a nitride gate dielectric and a nitrided SiO_2 interface layer and EOT, as determined from analysis of $C-V$ data of 1.6 nm. The SiO_2 device data are degraded due to boron transport to the $Si-SiO_2$ interface during the activation anneal for the p^+ poly-Si gate electrode, and a calculated $J-V$ curve is also shown for comparison in Fig. 1(c).

MOS capacitors were fabricated for devices with a Ta_2O_5 RPECVD layer with three different interfaces on (i) HF-last Si and (ii) with ~0.5–0.6 nm of plasma-grown SiO_2, with and without interfacial nitridation. Figures 2(a) and 2(b) display, respectively, $C-V$ and $J-V$ data for these stacked devices with the RPECVD Ta_2O_5 bulk dielectrics. The electrical thickness of stacked dielectrics, extracted from $C-V$ data, ranged from 1.1 to 1.6 nm. Direct deposition onto HF-last Si gave negative flatband voltage shifts of ~0.05–0.15 V relative to flatband voltages for MOS capacitors with interfaces formed by plasma oxidation with and without interfacial nitridation. In addition, the flatband voltages of MOS capacitors with the plasma-processed interfaces were the same to ±0.005 V as those prepared on Si wafers from the same ingot with similarly processed interfaces and plasma-deposited SiO_2 dielectrics. Similar to the devices with SiO_2 dielectrics, monolayer interface nitridation reduced direct tunneling by factors ~5–10 for a substrate accumulation bias of approximately 1 V, which was independent of substrate type.

Figures 3(a) and 3(b) include, respectively (a) $J-V$ characteristics for PMOS FETs with stacked oxide/nitride dielectrics in an EOT range from about 2.4 to 1.3 nm, and (b) a plot of J_g versus EOT for an inversion bias voltage of -1 V, which demonstrates that the 1 A/cm^2 line is *not crossed* until the EOT is reduced below ~1.1 nm. The devices of Fig. 3 included monolayer-nitrided interfaces. Figure 4 compares the direct tunneling current for both substrate accumulation and inversion in NMOS devices without the interfacial nitridation step with EOT ~2 nm. Three *different* stacked gate dielectrics are in the devices of Fig. 4: (i) a plasma-processed oxide with the interface layer prepared by RPAO and the bulk dielectric by RPECVD, (ii) an oxide/nitride stack, with ~0.6 nm of oxide prepared by remote plasma-assisted oxidation (RPAO), and the nitride layer deposited by RPECVD,[14] and (iii) an oxide/oxynitride stack with ~0.6 nm of oxide prepared by RPAO, and the oxynitride layer also deposited by RPECVD.[14] The oxynitride alloy has an approximate composition of $(SiO_2)_{0.5}(Si_3N_4)_{0.5}$, or equivalently, a N:O ratio of about 2:1. Studies of alloys with SiO_2 fractions ranging from 0.3 to 0.7 have demonstrated that the maximum direct tunneling current reductions relative to homogeneous oxides were obtained for nearly equal SiO_2 and Si_3N_4 alloy fractions, or an alloy composition given by $(SiO_2)_{0.5}(Si_3N_4)_{0.5}$, the same as shown in Fig. 4.

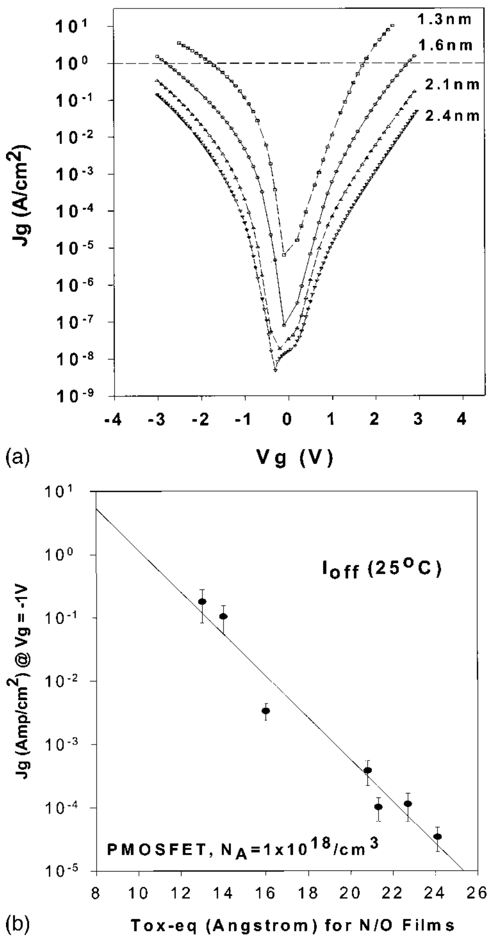

FIG. 3. (a) J_g vs V_g for PMOS FETs with EOT from 1.3 to 2.4 nm. (b) Scaling of J_g vs EOT for PMOS FETs of (a). Limiting EOT for J_g <1 A/cm^{-2} is less than 1.1 nm.

III. DISCUSSION

Two issues relevant to data presented above are now addressed: (i) application of a microscopic model that accounts for the reduction of tunneling current associated with interface nitridation, and (ii) a model calculation which demonstrates why stacks with Si-oxynitride alloy bulk layers, rather than stacks with Si-nitride bulk layers, show the largest reductions in direct tunneling.

The interfacial bonding structure of devices with nitrided interfaces has been determined from analysis of x-ray photoelectron spectroscopy (XPS) spectra,[20] and has been discussed in detail in Ref. 17. In summary, XPS studies were performed with plasma-grown ultrathin oxides in the thickness regime from 1 to 1.5 nm on Si(111) and Si(100) substrates: (i) both interfaces displayed an integrated spectral content in the *suboxide bonding regime* between the $2p$ Si substrate feature at ~99 eV and the SiO_2 bulk oxide feature at ~103.5 eV in excess of the one monolayer that defines and the ideal abrupt and flat interface, (ii) integrated intensities in this region decreased by 15%–20% between as-deposited (300 °C) and annealed conditions (900 °C), and (iii) the decreases in suboxide bonding occurred mostly in bonding arrangements that were not *intrinsic* with respect to a particular surface; e.g., the so-called Si^{2+} feature decreased markedly on Si(111) after the 900 °C anneal and significantly smaller reductions took were found for the Si^{1+} and Si^{3+} features which are intrinsic to flat Si(111) surfaces and interfaces.

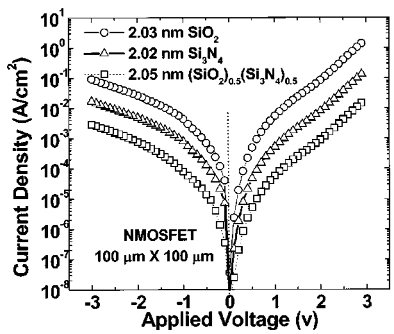

FIG. 4. J_g vs V_g for NMOS FETs with plasma-grown non-nitrided Si–SiO_2 interfaces and RPECVD oxide, nitride, and oxynitride gate dielectric layers.

Figure 5 indicates a modified interface band structure presented in Ref. 21 for 900 °C annealed (a) non-nitrided and (b) nitrided Si–SiO_2 interfaces. The suboxide bonding defines a transition region with an average SiO composition between the Si substrate and the SiO_2 dielectric which is different for non-nitrided interfaces. The thickness of the transition region between the Si substrate has been obtained from normalizing the excess Si interfacial bonding to an average density for a SiO alloy composition; i.e., the average of the densities of Si and SiO_2. The calculation for direct tunneling would give the same results if the triangular barriers were replaced by steps with an appropriately averaged band offset energy, ~1.58 eV for the interface with suboxide bonding, and 2.65 eV for the nitrided interface with suboxide bonding. The difference band offset energies between the non-nitrided and nitrided interfaces is consistent with characterizations that indicate that the *N* atoms are bonded at the interface and in a configuration with in which they have three Si neighbors.[12,13,22]

Figure 6 compares calculations of direct tunneling based on the WKB approximation[23,24] for three different dielectrics with EOT=2.0 nm: (i) an *ideal* oxide with no interfacial transition region (1), (ii) an oxide with interfacial suboxide bonding (2), and (iii) an oxide with interfacial suboxide bonding and a nitrided interface (3). The tunneling mass for

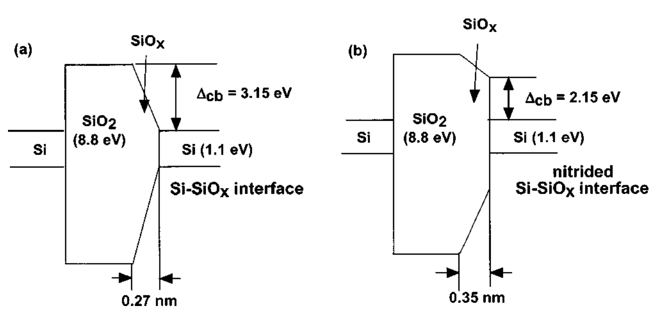

FIG. 5. Modified interface band structures determined from XPS data in Refs. 17 and discussed in detail in Refs. 18.

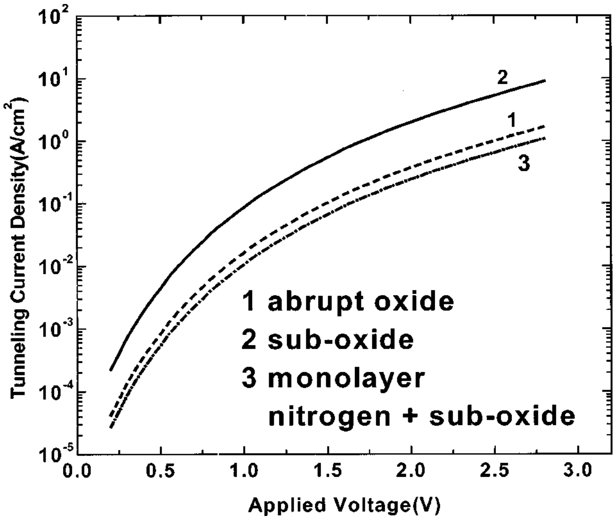

FIG. 6. Calculated tunneling based on the band structures in Fig. 5 (see Ref. 18).

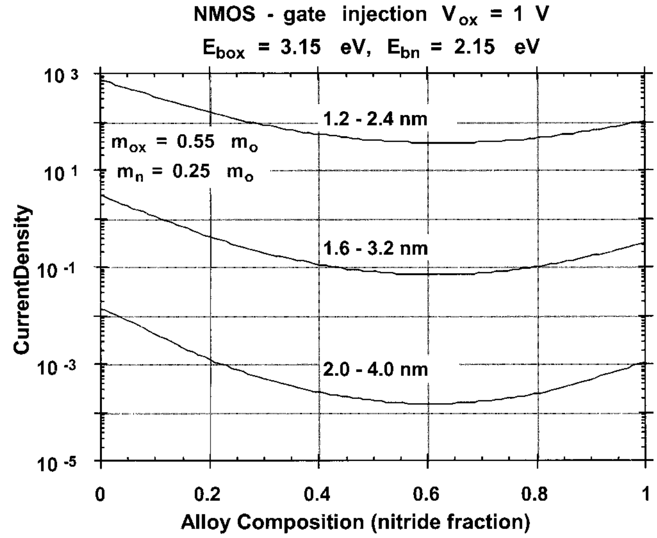

FIG. 7. Calculated tunneling current vs alloy composition for fixed EOT of 1.2, 1.6, and 2.0 nm. The calculations assume linear E_b, k, and m_e^* with alloy composition.

these calculations was taken to be 0.5 m_0, and the rest of the details of the calculations are discussed in Ref. 21. The calculations demonstrate that direct tunneling is reduced by interfacial nitridation by a factor of ~10 with respect to devices with suboxide bonding. Additionally, the calculated tunneling in the device with the nitrided interface is nearly equal to that of the device with the *ideal* abrupt interface.

Studies of direct tunneling in composite oxide/nitride gate stacks prepared by combining low-temperature plasma-assisted oxidation, oxide deposition, and nitride deposition, followed by postdeposition rapid thermal annealing,[4,19,23] have demonstrated that increases in physical thickness for these O/N stacks are significantly compensated by *decreases* in the tunneling mass and effective barrier height for tunneling. This has been determined by fitting the tunneling data with a model calculation in which the conduction-band energies for Si–SiO_2 and Si–Si_3N_4 have been taken to be 3.15 and 2.15 eV, respectively. The tunneling mass then becomes the fit parameter. For example, as shown above, in the physical thickness range between 1.5 and 2.5 nm, reductions of tunneling associated with ~20% increases physical thickness are ~10, consistent with a reduced band offset (~2.15 eV) and tunneling mass (~0.25 m_0–0.3 m_0) for the nitride.[19]

Figure 7 compares calculated tunneling currents for single-layer gate dielectrics along the pseudobinary alloy join line from SiO_2 to Si_3N_4 (Refs. 23 and 24) for three different EOT=2.0, 1.6, and 1.2 nm. The calculation has been performed for a potential drop of 1 V across the dielectric layer. The dielectric constant has been assumed to scale linearly from a value of 3.8 in SiO_2 to 7.6 in Si_3N_4, so that the physical thickness for a constant EOT increases linearly with nitride fraction from values of 2.0, 1.6, and 1.2 nm in SiO_2 to corresponding respective values of 4.0, 3.2, and 2.4 nm in Si_3N_4. Linear scaling of the dielectric constant is consistent with the pseudobinary character of the Si oxynitride alloy system. The tunneling mass has been assumed to decrease from ~0.55 to 0.25 m_0, and the band-offset energy from 3.15 to 2.15 eV as the alloy composition is changed from SiO_2 to Si_3N_4. These assumed linear variations do not follow directly from the pseudobinary character of the Si oxynitride alloys, and therefore, represent the simplest possible assumption. The calculation of the tunneling current has been performed using the approach of Refs. 23 and 24. The WKB approximation for direct tunneling for single-layer dielectrics indicates that tunneling transmission probability through a square barrier is approximately proportional to

$$\exp[-2ta(m_e^*\{E_b-V_{\mathrm{eff}}\})^{0.5}], \tag{1}$$

where a is a constant, t is the physical thickness of the dielectric, m_e^* is an electron tunneling mass and E_b-V_{eff} is an *effective uniform barrier height* for tunneling: E_b is the interfacial barrier height (e.g., the conduction-band offset energy between the Si substrate and the dielectric). For a voltage drop V_{die} across the dielectrics, E_b-V_{eff} is approximately equal to $E_b-0.5\ V_{\mathrm{die}}$. There are two things to note: (i) consistent with what has been discussed above with respect to tunneling reductions in oxide–nitride stacks, the tunnel current reduction for thicker nitride film with respect to a thinner oxide film of the same EOT is about a factor of 10. This is due to compensating or off-setting factors; i.e., the factor of 2 increase in physical thickness is compensated by decreases in the product of the tunneling mass and effective average tunneling barrier height. The bowing of the curves in Fig. 7 results from the incorporation of linear scaling into an exponential tunneling current relationship that is qualitatively similar to the approximate WKB expression introduced above. The increases in physical thickness along with the decreases in mass and *effective* barrier height combine to predict a minimum in the direct tunneling near the middle of the alloy composition range, rather than at the nitride end of the system. As noted above, this has been born out of the experiments described above.

It is important to note that bowing of the curves in Fig. 7 is a direct result of the end-member value of the tunneling mass assumed for Si_3N_4 on the basis of the data in Fig. 1(b). As note earlier in the article this value of the tunneling mass used in this calculation may reflect the properties of RPECVD nitrides. Other authors have determined tunneling masses for Si_3N_4 that are higher, $\sim$0.4–0.5 m_0, for nitrides prepared in other ways.[17,18] If higher values of m_0 for Si_3N_4 are used in the scaling of the tunneling mass, the bowing in Fig. 7 is significantly reduced, in particular, the calculated tunneling current is essentially constant for $x>0.6$, rather than increased between the middle of the alloy regime and the end-member Si_3N_4 composition.

IV. CONCLUSIONS

Based on the experimental results presented above, and the discussions in Sec. III, there will likely be two steps in the transition from (i) thermally grown oxides, including modest levels of bulk and interface nitridation achieved by processing with NO and N_2O,[25] (ii) stacked dielectrics that include alternative higher-*k* materials. For the EOT range from about 1.6 to 1.8 nm to about 1.1 to 1.0 nm, the *ideal* gate dielectric stack will be comprised of a superficially thin ($\sim$0.5 nm) SiO_2 layer with monolayer interface nitridation, and an oxynitridation alloy with a composition near the middle of the alloy range, $(SiO_2)_{1-x}(Si_3N_4)_x$, where $x \sim 0.5$–0.6 (see Fig. 7). For the EOT range below about 1.1–1.0 nm, the oxynitride alloys will be replaced by high-*k* alternative materials such as transition-metal silicates (and/or silicate alloys), and/or Ta_2O_5.[6–9] Figures 2(a) and 2(b) demonstrate that the same interface that reduces nitride and alloy degradation of device performance and reliability also can provide the same function when used with high-*k* gate dielectric materials such as Ta_2O_5. The flatband voltages for the plasma-processed interfaces in Fig. 2(a) are the same to within 5 mV as those obtained using the same wafer lot with devices in which the bulk oxide layer is SiO_2. The reductions in direct tunneling for these two sets of devices are essentially the same.

ACKNOWLEDGMENTS

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