Interface studies of tungsten nitride and titanium nitride composite metal gate electrodes with thin dielectric layers

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Interface formation between reactively sputtered tungsten nitride (WN_x) or titanium nitride (TiN_x) metallic films and thermally grown silicon dioxide (SiO_2) layers is studied by interrupted growth with on-line Auger electron spectroscopy. For both composite metals, growth proceeds directly without a metal precursor layer. The chemical stability of these WN_x/SiO_2 and TiN_x/SiO_2 interfaces is investigated by rapid thermal annealing up to 850 °C. The WN_x/SiO_2 interface is stable up to 650 °C while TiN_x/SiO_2 is stable below 850 °C. Metal–oxide–semiconductor capacitors have been fabricated with WN_x and TiN_x gates and 7.5 nm thick thermal oxide gate dielectrics with interface trap densities, $D_{it}<2\times10^{11}$ $cm^{-2}\,eV^{-1}$. Capacitance–voltage and current–voltage measurements indicate the Fermi level for TiN_x lies near midgap in Si, while for WN_x it lies closer to the valence band. © *1998 American Vacuum Society.* [S0734-2101(98)59303-7]

I. INTRODUCTION

The choice of design parameters for each new generation of complimentary metal–oxide–semiconductor (CMOS) devices relies heavily on the application of scaling laws to the values used in the previous generation of integrated circuits. Several scaling laws[1–4] have been proposed to address particular design issues while providing flexibility in the selection of other device parameters. In general, these scaling laws produce shorter channels, thinner dielectric layers, shallower source and drain junctions, reduced operating voltages, and heavier channel doping. These requirements impose demanding specifications on the choice of gate electrode material, thus creating significant technological challenges to the continued use of heavily doped polycrystalline silicon (poly-Si) for this application. Depletion effects in the poly-Si gate electrode and the corresponding voltage drop become more significant for smaller devices and may destroy the targeted scaling performance.

Metals and metal alloys are attractive as alternative gate electrode materials because they do not suffer from depletion effects. However, these materials may suffer from problems due to diffusion or reactivity with the gate dielectric during later processing steps. In particular, many transition metals either exhibit poor adhesion or chemically react with SiO_2 at elevated temperatures resulting in the formation of a silicide layer covered by a metal oxide.[5,6]

Recently, several groups[7–15] have investigated TiN_x as a potential gate electrode material because it has low resistivity, its work function lies near midgap in Si, and it is frequently used as a diffusion barrier. In this article, on-line Auger electron spectroscopy (AES) is used to examine the initial growth and subsequent evolution of WN_x and TiN_x metallic films deposited by reactive magnetron sputtering on thermal SiO_2 dielectric layers. Sequential rapid thermal annealing (RTA) treatments followed by AES measurements are used to monitor the chemical stability of the WN_x/SiO_2 and TiN_x/SiO_2 interfaces up to 850 °C. Finally, capacitance–voltage ($C-V$) and current–voltage ($I-V$) characteristics of metal–oxide–semiconductor (MOS) capacitors employing WN_x and TiN_x gates are presented.

II. EXPERIMENT

Thin films of WN_x and TiN_x were deposited at 300 K by reactive magnetron sputtering of a 99.98% W or 99.9% Ti target, respectively, using 99.999% Ar and 99.999% N_2 mixed in a 5:1 ratio and a plasma power of 50 W. Substrates were 3 in. Si (100) wafers on which a 5.5 nm thick thermal oxide was grown. The chamber pressure during deposition was 6 mTorr while the base pressure was $P_b\leqslant2\times10^{-9}$ Torr. Under these conditions, average deposition rates of 6 nm/min for WN_x and 1 nm/min for TiN_x were determined from cross-sectional scanning electron microscope measurements of bulk films.

The formation and evolution of WN_x/SiO_2 and TiN_x/SiO_2 interfaces were observed by interrupted growth and AES. Several ultrathin layers of WN_x or TiN_x were sequentially deposited and AES spectra collected until the disappearance of the Si_{LVV} Auger peak at a metal thickness, $d\sim0.8$ nm, indicated that the interface was buried. Thicker layers (0.5–1.0 nm each) were then deposited and measured with AES to monitor the development of the WN_x or TiN_x layer, and finally, thick films were prepared to verify bulk characteristics. AES spectra were measured using a model 10-155 PHI cylindrical mirror analyzer at a primary electron energy of 3 keV. For reference, bulk W and Ti AES spectra were also collected.

The chemical stability of WN_x/SiO_2 and TiN_x/SiO_2 interfaces was investigated by on-line rapid thermal annealing. A 0.6–0.7 nm thick WN_x or TiN_x layer was deposited on SiO_2 and annealed for 3 min in vacuum from 350 to 850 °C in 100 °C steps. AES spectra were measured between each annealing treatment.

MOS capacitors were fabricated with WN_x and TiN_x gate electrodes. A field oxide was thermally grown on RCA

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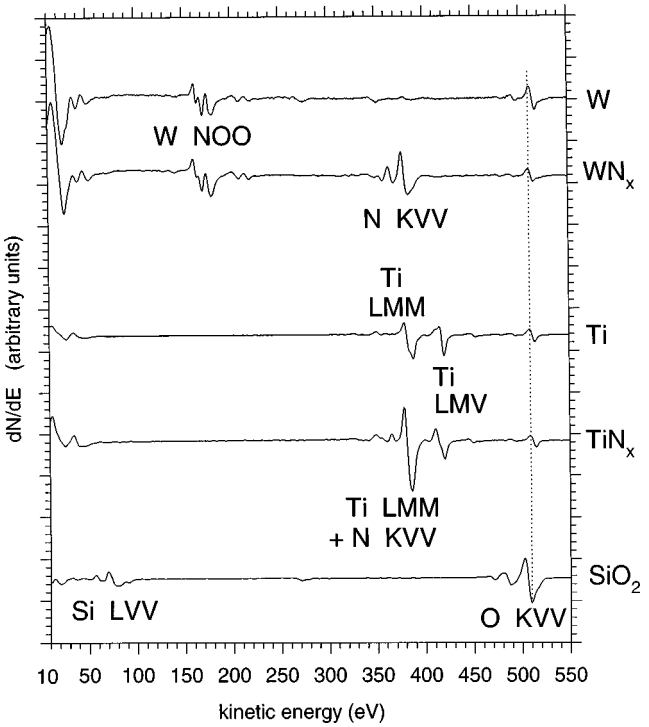

FIG. 1. Derivative AES spectra of bulk SiO_2, TiN_x, Ti, WN_x, and W films with Auger transitions identified. The O_{KVV} peak is chemically blueshifted for the metals relative to SiO_2.

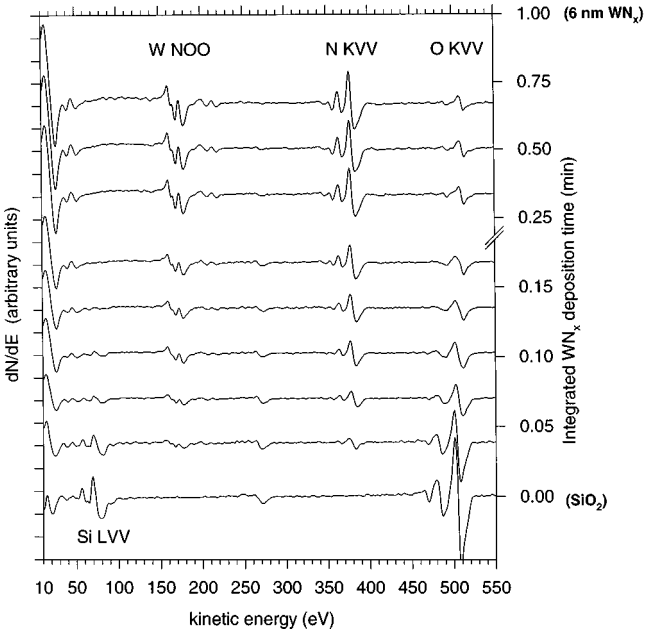

FIG. 2. Interrupted growth of WN_x on SiO_2. Si_{LVV} and O_{KVV} intensities decrease while W_{NOO} and N_{KVV} peaks increase as additional layers are deposited. The O_{KVV} peak gradually blueshifts to metal–oxide position as the interface gets buried.

cleaned p-type Si (100) wafers. Active areas were patterned, wet chemically etched, and another RCA clean performed before a 7.5 nm thermal gate oxide was grown. The wafers were patterned for lift-off and 50 nm of WN_x or TiN_x sputtered. A 100 nm Al layer was subsequently sputtered to facilitate external contact. After lift-off, Al back-contacts were evaporated and a postmetallization anneal was carried out in H_2 at 350 °C for 30 min. High-frequency and quasistatic $C-V$ measurements were performed in addition to $I-V$ measurements in the Fowler–Nordheim tunneling regime.

III. RESULTS

Figure 1 shows derivative AES reference spectra for bulk SiO_2, W, WN_x, Ti, and TiN_x films with the relevant spectral features labeled according to the Auger transitions involved. For TiN_x, the Ti_{LMM} and N_{KVV} features overlap[16–19] resulting in a peak intensity at 385 eV nearly twice that of the Ti_{LMV} transition at 420 eV. In contrast, for pure Ti these intensities are nearly equal. A small concentration of parasitic oxygen is seen for each of the metallic films, but the O_{KVV} peak is chemically blueshifted by about 5 eV from its position in SiO_2.

Derivative AES spectra of the WN_x/SiO_2 interface formation and growth is shown in Fig. 2 as metallic layers are deposited sequentially. The bottom curve shows the bare SiO_2 spectrum and subsequent spectra are offset from it corresponding to their integrated WN_x deposition time. The Si_{LVV} and O_{KVV} peak intensities decrease rapidly as the first few metallic layers are added while the W_{NOO} and N_{KVV} intensities increase. The O_{KVV} peak also gradually blueshifts to the position characteristic of the metal by the time the Si_{LVV} signal has completely disappeared, indicating the presence of parasitic oxygen. Additional layers increase the intensity of the W and N features until bulk spectra are observed.

Similar AES spectra for the growth of TiN_x on SiO_2 are presented in Fig. 3. As was seen for WN_x, the Si_{LVV} and O_{KVV} intensities decrease while the $Ti_{LMM}+N_{KVV}$ and Ti_{LMV} peaks increase as successive layers of TiN_x are deposited. The O_{KVV} blueshift is again observed and the intensity of the $Ti_{LMM}+N_{KVV}$ peak at 385 eV is seen to be about twice that of the Ti_{LMV} peak at 420 eV for all spectra.

The chemically stability of the WN_x/SiO_2 interface is displayed in Fig. 4 for RTA treatments up to 750 °C. The bottom curve shows the bare SiO_2 AES spectrum followed by the as-deposited WN_x layer. To provide the most sensitivity to chemical reactivity at the interface, the minimum metallic layer thickness, $d=0.7$ nm, was used such that the Si_{LVV} peak intensity was reduced to zero as seen. Successive curves were measured after 3 min RTA treatments in vacuum at the temperatures shown. A dramatic change in the spectrum is observed after annealing at 650 °C; the Si_{LVV} peak reappears, the O_{KVV} signal increases and redshifts back to the position corresponding to SiO_2. At lower temperatures, other subtle changes in intensity are observed particularly for the O_{KVV} peak. These effects are being studied further but are believed to be due to oxidation from residual gases in the RTA chamber rather than intrinsic to the sample.

Figure 5 shows similar data for the chemical stability of the TiN_x/SiO_2 interface subjected to RTA treatments up to 850 °C. No dramatic changes are observed in the AES spec-

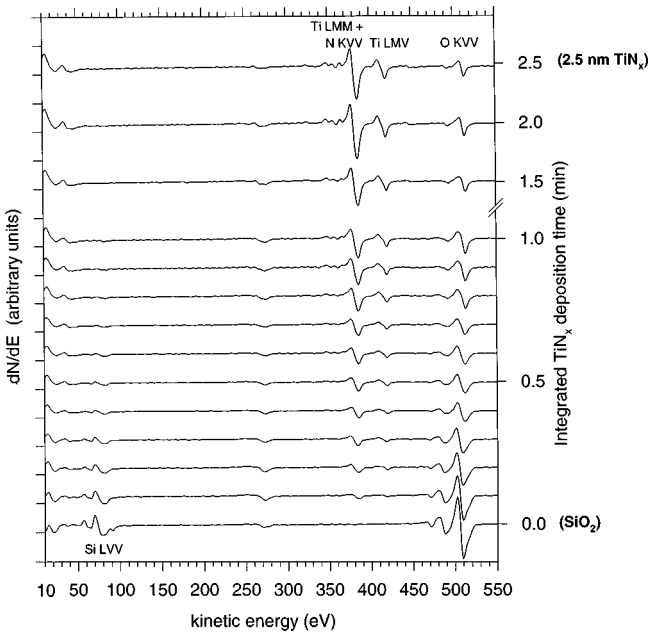

FIG. 3. Interrupted growth of TiN_x on SiO_2. Si_{LVV} and O_{KVV} intensities decrease while $Ti_{LMM}+N_{KVV}$ and Ti_{LMV} peaks increase. $Ti_{LMM}+N_{KVV}$ peak at 385 eV and Ti_{LMV} peak at 420 eV have asymmetric intensities indicating growth of TiN_x without a seed layer.

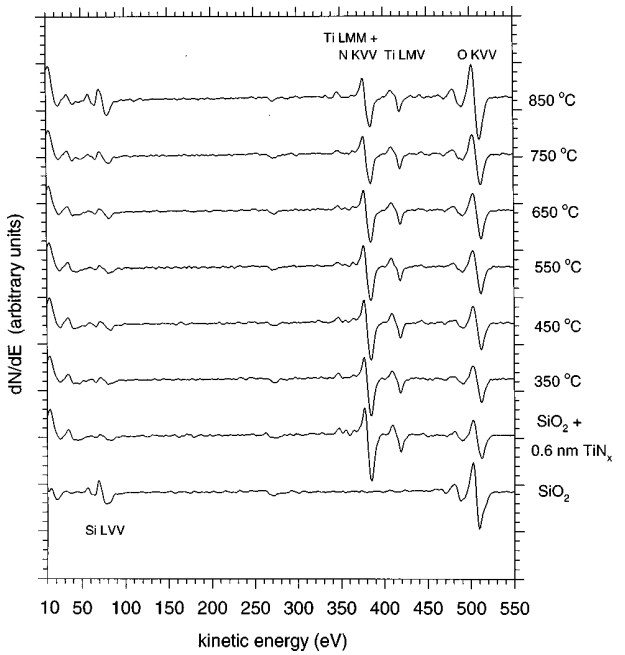

FIG. 5. Chemical stability of the TiN_x/SiO_2 interface for sequential RTA treatments. Si_{LVV} increases and O_{KVV} redshifts above 850 °C, indicating the oxide has been re-exposed.

tra until 850 °C, at which point the Si_{LVV} intensity increases significantly. In addition, the O_{KVV} peak is redshifted and increases in intensity, similar to the behavior observed for WN_x.

The electrical characteristics of MOS capacitors fabricated with WN_x and TiN_x gate electrodes are presented in Figs. 6 and 7. In Fig. 6, quasistatic and high-frequency $C-V$ data for both composite metal gate electrodes show good electrical characteristics with densities of interface traps, $D_{it}<2\times10^{11}$ cm^{-2} eV^{-1}. The capacitors fabricated with a TiN_x gate display a flatband voltage that is 0.47 eV lower

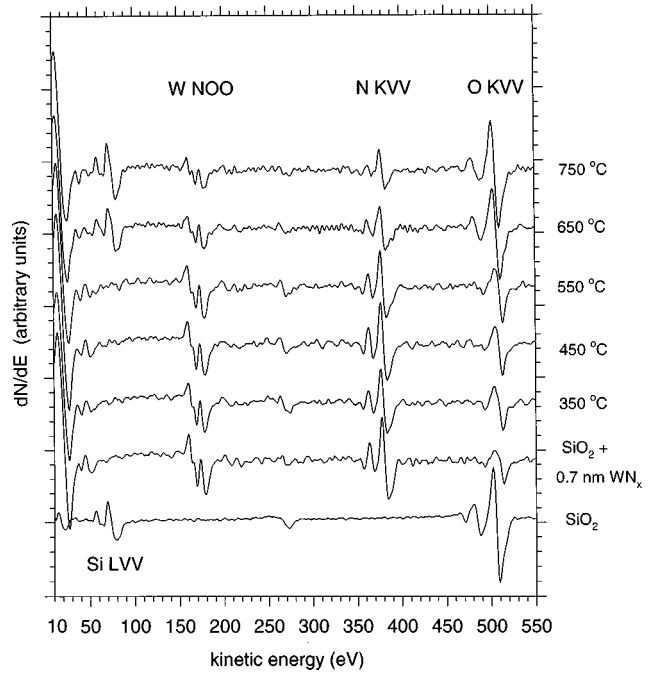

FIG. 4. Chemical stability of the WN_x/SiO_2 interface for sequential RTA treatments. Si_{LVV} reappears and O_{KVV} redshifts above 650 °C, indicating the oxide has been re-exposed.

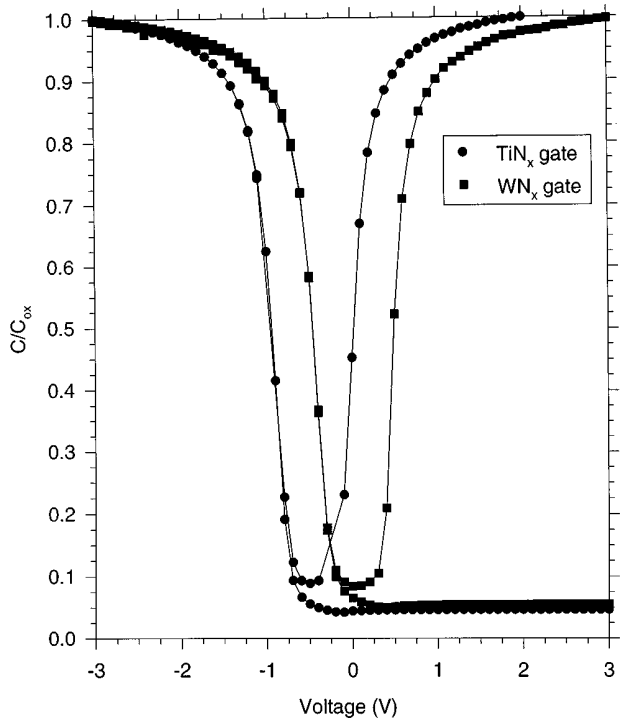

FIG. 6. High-frequency and quasistatic $C-V$ curves for MOS capacitors using WN_x and TiN_x gates. The flatband voltage for the TiN_x devices is 0.47 eV lower than the WN_x capacitors.

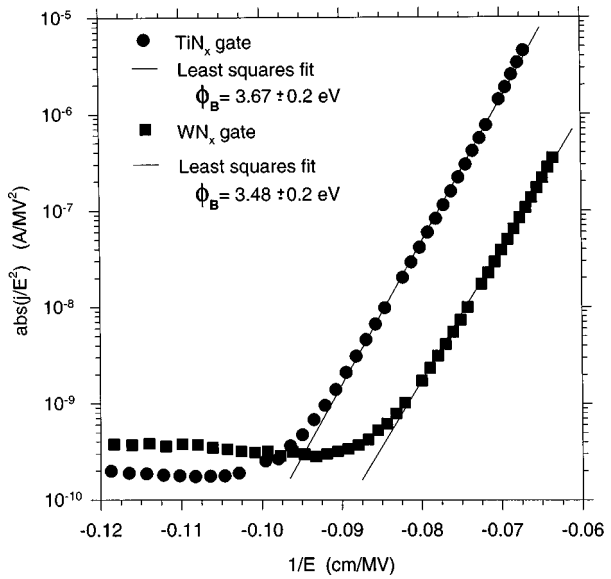

FIG. 7. Fowler–Nordheim plot of tunneling current for MOS capacitors using WN_x and TiN_x gates. Least-squares fits give barrier heights of $\Phi_B = 3.48 \pm 0.2$ eV and $\Phi_B = 3.67 \pm 0.2$ eV, respectively.

than those using a WN_x gate. A Fowler–Nordheim plot of the tunneling current is exhibited in Fig. 7 for both gate metals along with least-squares fits to the data. From the slopes of these fits, barrier heights with respect to SiO_2 of $\Phi_B = 3.48 \pm 0.2$ eV for WN_x and $\Phi_B = 3.67 \pm 0.2$ eV for TiN_x are calculated assuming an effective-mass $m^* = 0.5 m_e$.[20]

IV. DISCUSSION

The initial formation of the WN_x/SiO_2 interface seen in Fig. 2 shows the presence of both W_{NOO} and N_{KVV} features indicating that the compound metal grows directly on SiO_2 without the need for an intervening metallic seed or template layer. Similarly, comparing the asymmetric intensities of the peaks at 385 and 420 eV for the initial TiN_x layers in Fig. 3 with the bulk Ti and TiN_x spectra shown in Fig. 1, it is clear that TiN_x growth on SiO_2 also proceeds without a seed layer. Both figures show the Si_{LVV} peak intensity decreasing as the metal layer grows and the interface is effectively buried by about 0.8 nm of metal. This thickness is consistent with the escape depth of ~0.6 nm for Auger electrons at the Si_{LVV} energy of ~90 eV.[21] The gradual blueshift of the O_{KVV} peak from the position characteristic of SiO_2 to that of the metal oxide is also consistent with the interface being buried. For both compound metals, bulklike spectra are observed once the thickness is greater than 1.5–2.0 nm.

Turning to the RTA data, the reappearance of the Si_{LVV} peak in Fig. 4 after annealing at 650 °C indicates that a change has occurred in the metal film which re-exposes the WN_x/SiO_2 interface. This conclusion is supported by the redshift of the O_{KVV} peak from the metal–oxide energy back to the position characteristic of SiO_2. This change may be the result of a chemical reaction between the metal film and the dielectric or it may result from a change in the physical properties of the film such as crystallization and grain growth.[22] Similar behavior is observed in Fig. 5 for the TiN_x/SiO_2 interface, except in this case changes in the AES spectrum do not occur until the sample is annealed at 850 °C. The Si_{LVV} and O_{KVV} peak intensities grow and the latter is redshifted, indicating that Auger electrons from the interface region are being detected. For both composite metals, further study is needed to elucidate the details of these changes and to determine the final composition and structures that result. It is also unclear if these metal/SiO_2 interfaces are stable above their respective threshold temperature for shorter duration anneals, which would be expected if the changes are controlled by kinetics.

Finally, the MOS capacitors made with WN_x and TiN_x gate electrodes shown in Figs. 6 and 7 exhibit excellent device characteristics. The density of interface traps, $D_{it} < 2 \times 10^{11}$ cm^{-2} eV^{-1} for both TiN_x and WN_x indicate deposition of the gate metal has not affected the underlying Si/SiO_2 interface. The flatband voltage shift observed between the $C-V$ curves of Fig. 6 suggests the WN_x/SiO_2 barrier height is larger than TiN_x/SiO_2. Since these wafers were processed in parallel and received the same treatment at each step except for the gate metal deposition, it is assumed that the flatband voltage shift due to fixed positive charge, etc., is the same for both samples. The observed flatband voltage shift should be a direct measure of the difference in barrier height for the two metals. The WN_x/SiO_2 and TiN_x/SiO_2 barrier heights determined from Fowler–Nordheim tunneling, $\Phi_B = 3.48 \pm 0.2$ eV and $\Phi_B = 3.67 \pm 0.2$ eV, respectively, include substantial corrections to properly account for the flatband voltage and potential drop in the substrate. Although the barrier height for WN_x is not internally consistent with the $C-V$ results, these values generally agree with similar measurements made by other authors.[12,15]

The TiN_x/SiO_2 barrier height places the Fermi-level E_F for TiN_x near midgap in Si, making it unsuitable for CMOS applications because its large threshold voltage V_t is unacceptable. However, the $C-V$ data indicate E_F for WN_x lies closer to the valence band, resulting in an attractive V_t for n MOS devices. In addition, if it is possible to modify the work function of these compound metals by depositing an appropriate metal overlayer such as W,[12–15] then they may be incorporated as a reaction barrier in advanced gate stack designs.

V. CONCLUSIONS

The compound metals WN_x and TiN_x are promising candidates for use in future CMOS engineered gate stack designs. Both materials grow on SiO_2 without a seed layer and films as thin as 0.8 nm are chemically stable below 650 °C for WN_x or 850 °C for TiN_x. MOS capacitors made using WN_x and TiN_x gates display good quasistatic and high-frequency $C-V$ characteristics with low interface trap densities, $D_{it} < 2 \times 10^{11}$ cm^{-2} eV^{-1}. The observed shift in flatband voltage indicates the Fermi level lies near the Si midgap for TiN_x and closer to the valence band for WN_x.

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