Characteristics of metalorganic remote plasma chemical vapor deposited Al_2O_3 gate stacks on SiC metal–oxide–semiconductor devices

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Metalorganic remote plasma chemical vapor deposited SiO_2/Al_2O_3 stacks were deposited on 6H *p*-type silicon SiC to fabricate a high-*k* gate stack SiC metal–oxide–semiconductor capacitors. Capacitance–voltage (C–V) and current–voltage ($I-V$) measurements were performed. C–V characteristics showed excellent properties at room and higher temperatures. Samples exhibited a slight negative flatband shift from which the net oxide charge (Q_{ox}) was calculated. Low leakage currents were observed even at high temperatures. $I-V$ characteristics of Al_2O_3 were superior to those observed on AlN and SiO_2 dielectrics on SiC. [DOI: 10.1063/1.1392973]

SiC has long been studied for high power, high frequency, and high temperature applications.[1–3] Its high breakdown field, high saturation velocity, and relative high electron mobility make it a candidate for fabricating high power devices with reduced power loss. High power, however, leads to high fields placed on the semiconductor. Since the field across the dielectric is proportional to the SiC electric field, a large field is dropped across the dielectric resulting in a low breakdown field. Using high-*k* gate dielectric materials can reduce these fields and increase the lifetime of the device.[4]

Issues surrounding the wide band gap of SiC and interface defect density will define the materials that can be deposited or grown on SiC. Most dielectrics follow the trend of decreasing band gap with increasing dielectric constant.[5] Al_2O_3 and Si_3N_4 are exceptions to this rule exhibiting large dielectric constants and large band gaps. There have been few successful reports of high-*k* dielectrics on SiC including Si_3N_4, oxynitrides, and AlN. However, their dielectric constants are lower than Al_2O_3 ($\varepsilon \sim 10$).[5–8] Lipkin *et al.* deposited AlN on SiC and then oxidized the film to create AlN:O.[4] It should be noted that after the oxygen anneal, there would be a significant amount of nitrogen left in this film and, therefore, can not be directly compared to Al_2O_3. In this work, Al_2O_3 gate stacks are deposited on SiC and electrical and interface characteristics are reported.

The 6H *p*-type SiC wafers used were aluminum-doped p^- epitaxial layers with a nominal doping of 5.5×10^{17} grown on p^+ 6H SiC substrates.[9] These wafers were diced and a standard Radio Corporation of America clean was performed at 75 °C. A low-temperature oxide (LTO) was deposited at 200 °C, 25 W, and at a pressure of 1 Torr with a target thickness of 50 Å. This SiO_2 interface layer was chosen since to date, the SiO_2–SiC interface has been reported to have the best properties.[4] Furthermore, Al_2O_3 deposition directly on Si surfaces has shown degraded interface properties requiring the use of a thin SiO_2 interface layer.[10] After the interface layer formation, Al_2O_3 was deposited using metalorganic remote plasma chemical vapor deposition (RPCVD) at 300 °C, 30 W, and at a pressure of 300 mTorr with a target thickness of 200 Å to create a SiO_2/Al_2O_3 gate stack. Triethyldialuminum tri-sec-butoxide in helium was used as the precursor for deposition. The Al_2O_3 films were then annealed at 800 °C in argon for 30 s in order to relax the chemical and structural nature of the film.[10] Aluminum metal, 100 nm in thickness, was evaporated and patterned as a gate electrode to fabricate metal–oxide–semiconductor (MOS) capacitors. Measurements were taken before and after a forming gas anneal (FGA) at 400 °C for 30 min. Interface and electrical properties were determined by high frequency capacitance–voltage (C–V) using a HP 4284A Precision LCR Meter and current–voltage ($I-V$) measurements using a HP 4155B Semiconductor Parameter Analyzer. Room and high temperature measurements were taken using a Temptronics temperature controller. All measurements were obtained under dark conditions.

Auger electron spectroscopy (AES) was performed at intermittent steps of a previous Al_2O_3 deposition on Si and on 0.6 nm of RPCVD SiO_2 on Si. Evolving chemical composition and bonds of the Si interface and the deposited Al_2O_3 thin film can be determined from this measurement. As seen in Fig. 1, the Al–O feature at ~ 55 eV does not change with increasing deposition time and its energy is consistent with aluminum bonded to oxygen.[11] From this, it was concluded that Al atoms are not bonded to Si atoms at the interface and the Al is fully oxidized throughout the deposited film.

The capacitors fabricated with SiO_2/Al_2O_3 gate stacks show excellent electrical characteristics. The room temperature C–V curves of *p*-type 6H SiC before and after FGA are shown in Fig. 2. The effective oxide thickness of the Al_2O_3 samples obtained from the HF accumulation capacitance was 135 Å. Ideal flatband voltage, assuming no oxide charge, for

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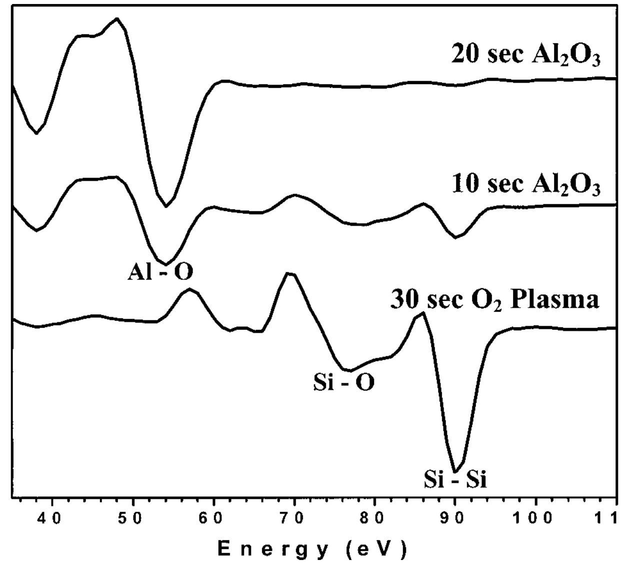

FIG. 1. AES of Al_2O_3 deposition on 0.6 nm of SiO_2 on HF last Si is shown.

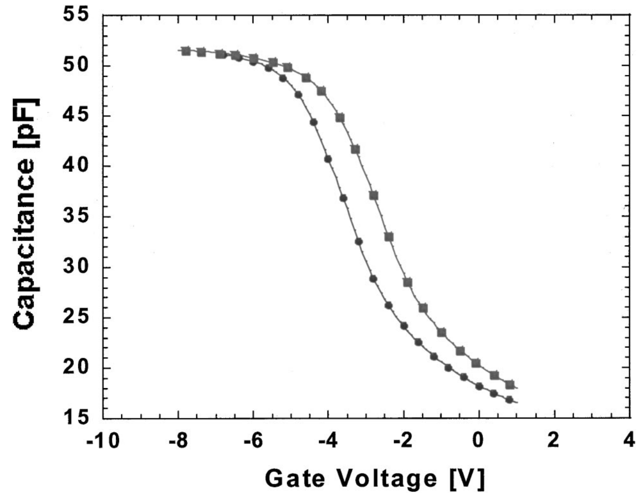

FIG. 2. C–V plot of 6H *p*-type SiC MOS capacitor before (circles) and after (squares) FGA (400 °C) is shown. The stack consists of 50 Å SiO_2/200 Å Al_2O_3 and the areas are 100 μm×200 μm. A parallel shift in flatband voltage shows a reduction in fixed charge.

aluminum on 6H SiC can be calculated using the doping density stated and the following values: $E_g = 3.0\,\mathrm{eV}$, $q\chi = 3.85\,\mathrm{eV}$,[12] and $n_i = 1.6\times10^{-6}\,\mathrm{cm}^{-3}$.[3] For *p*-type 6H SiC, ideal flatband is about -2.65 V. The extracted flatband voltage was -4.1 V before FGA and -3.3 V after FGA, corresponding to a net positive charge in the range of $10^{12}\,\mathrm{cm}^{-2}$. This agrees with values reported for both SiO_2 (Refs. 13 and 14) and alternate dielectrics on SiC.[4,7,8,15] A parallel shift of the experimental capacitance curve towards the ideal flatband after FGA was attributed to a reduction in fixed charge. The stretch out of the $C-V$ curves is attributed to the interface trap charge (D_{it}) contribution to the voltage in the *p*-type samples, which agrees with values reported in literature. However, minimal frequency dependence is observed due to the nonresponsive nature of the interface traps. Recent data of RPCVD SiO_2/Al_2O_3 gate stacks on Si has indicated the presence of negative charge at the SiO_2–Al_2O_3 internal interface.[10] In this work, the high D_{it} values present at the SiO_2–SiC interface dominate the negative charge contribution coming from the SiO_2–Al_2O_3 internal interface and thereby result in a net negative flatband shift.

Cooper reported that states which lie 0.7 eV above the band edge (for *p*-type material) can not respond to the changes in dc bias and are not detected for measurements at room temperature.[16] Therefore, in order to sample more of the interface states, higher temperatures must be utilized. $C-V$ measurements taken at several temperatures for two different frequencies are shown in Fig. 3. The negative flatband shift observed as temperature increases is larger in value and opposite in direction than compared with the temperature dependence of the work function difference between Al and 6H SiC. Since the curves are shifting towards negative values, the flatband can be attributed to the generation of positive charge arising from either fixed charge or slow interface traps.[17]

Gate leakage current was measured as a function of voltage for several temperatures. Current densities derived from these $I-V$ characteristics for dielectric fields of 0.8 and 1.7 MV/cm are plotted as a function of inverse temperature (1/K) and are shown in Fig. 4. The current density at the maximum temperature for a 1.7 MV/cm dielectric field is only $10^{-6}\,\mathrm{A/cm}^2$, which is lower than reported for AlN on SiC.[6] The observed superior leakage currents of Al_2O_3 are a product of two advantages of Al_2O_3 over AlN. The first advantage is the dielectric constant of Al_2O_3 is higher than AlN, resulting in a physically thicker film. Accounting for the 50 Å of LTO, the dielectric constant of Al_2O_3 was found to be ~9 whereas published reports of AlN range from 7.8–8.5.[6–8] The second advantage is that the barrier height at the metal–Al_2O_3 interface is larger than that of AlN thereby decreasing the tunneling probability of gate injected electrons in accumulation. Published metal work functions of

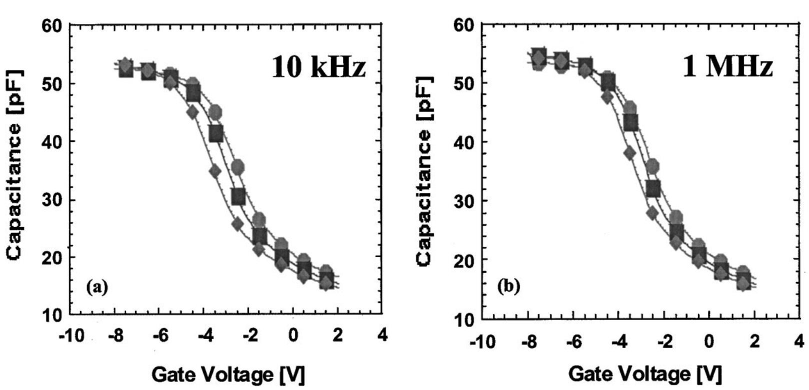

FIG. 3. C–V plot of 6H *p*-type SiC MOS capacitor at 25 °C (circles), 100 °C (squares), and 150 °C (diamonds) for (a) 10 kHz and (b) 1 MHz is shown. Area is 100 μm×200 μm and the parallel shift in flatband is attributed to the increase in the number of states involved at higher temperatures.

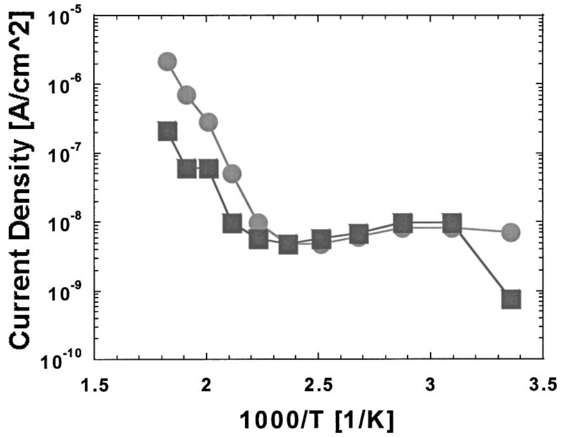

FIG. 4. Current density as a function of inverse temperature [1/K] for 6H *p*-type SiC at fields of 0.8 and 1.7 MV/cm is shown. Values are less than reported values at equivalent fields.

gate electrodes on AlN were close to 4.1 eV, which are similar to the aluminum work function of this work. A higher dielectric constant and larger barrier height result in lower leakage currents and indicate that Al_2O_3 films are a strong candidate for SiC MOS field effect transistor devices.

In summary, metalorganic RPCVD SiO_2/Al_2O_3 gate stack MOS capacitors were successfully fabricated on 6H *p*-type SiC. Well-behaved $C-V$ and $I-V$ characteristics were demonstrated at 25 °C and above. A reduction in fixed charge was found after FGA and large D_{it} screened the negative charge present at the SiO_2–Al_2O_3 interface, resulting in a net negative flatband shift. High temperature C–V showed increasing negative flatband shift with increasing temperature. High temperature $I-V$ showed an increase in current with temperature but current densities are lower than reported values at equal fields. These results are encouraging for metalorganic RPCVD Al_2O_3 gate stacks on other wide band gap semiconductors such as GaN and GaAs.

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