Optimization of nitrided gate dielectrics by plasma-assisted and rapid thermal processing

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(Received 3 February 1998; accepted 9 March 1998)

This article addresses several aspects of nitrogen atom (N atom) incorporation into ultrathin gate oxides including: (i) monolayer incorporation of N atoms at the $Si–SiO_2$ interfaces to reduce tunneling currents and improve device reliability; and (ii) the incorporation of silicon nitride films into stacked oxide–nitride (ON) gate dielectrics to (a) increase the capacitance in ultrathin dielectrics without decreasing film thickness, and (b) suppress boron atom (B atom) diffusion from p^+ polycrystalline Si gate electrodes through the dielectric layer to the Si substrate channel region. The results of this article demonstrate that these N-atom spatial distributions can be accomplished by low thermal budget, single wafer processing which includes (i) low-temperature (300 °C) plasma assisted oxidation, nitridation, and/or deposition to achieve the desired N-atom incorporation, followed by (ii) low thermal budget (30 s at 900 °C) rapid thermal annealing to promote chemical and structural bulk and interface relaxation. © *1998 American Vacuum Society.*
[S0734-2101(98)58403-5]

I. INTRODUCTION

As the lateral dimensions of advanced Si field effect transistors (FETs) shrink into the deep submicron range ($d < 0.25$nm), the oxide equivalent thickness ($t_{ox\,eq}$) of gate dielectrics must decrease proportionally into an ultrathin regime ($t_{ox\,eq} < 3$ nm) in which direct tunneling becomes an important factor in the off-state leakage current. It has been demonstrated that N atoms can be incorporated into ultrathin gate dielectrics by (i) thermal, (ii) rapid thermal, and (iii) plasma-assisted processing.[1–3] Interfacial N-atom incorporation has been shown to improve device reliability.[4] Incorporation of nitrogen in the bulk of the dielectric film in nitride layers has been shown to promote values of $t_{ox\,eq}$ that are less than the physical thickness of the stacked dielectric as in ONO structures.[5] Finally, N-atom incorporation at the top surface of oxide dielectrics has been demonstrated to suppress B-atom penetration from p^+ polysilicon gate electrodes.[6,7]

This article describes a novel plasma-assisted process for N-atom incorporation at $Si–SiO_2$ interfaces, and demonstrates that dielectrics with nitrided interfaces prepared in this way display reduced tunneling currents. The article also describes new results relative to the preparation and characterization of silicon nitride films prepared by remote plasma-assisted deposition. These films have been incorporated into *n*-channel FET devices with stacked ON dielectrics.[8] The performance of these FETs with stacked ON gate dielectrics is compared with FETs with oxide dielectrics with the same $t_{ox\,eq}$. The suppression of B-atom diffusion from $p+$ polycrystalline silicon gate electrodes and accompanying improvements in device reliability are demonstrated for ultrathin nitride films, $t_n \sim 0.8$ nm incorporated into stacked ON dielectrics.[7]

II. DEVICE FABRICATION

A. Nitrided interfaces

It was previously shown that interface nitridation by plasma-assisted processing could be accomplished by a 300 °C plasma-assisted oxidation process in which N_2O was used as the source gas for both initial oxide growth and interface nitridation.[3,4] This process is the first of a two-step plasma process that has been used to fabricate device quality gate dielectrics.[9] The second plasma processing step is a 300 °C remote plasma-assisted deposition of an oxide,[3,4,9] or a stacked ONO,[5] or ON structure.[7,8] To obtain device quality performance and reliability, a post deposition rapid thermal anneal (RTA) at 900 °C for 30 s was required to promote bulk dielectric and interfacial chemical and structural relaxations, e.g., to evolve hydrogen from both oxide and nitride dielectrics and to reduce interfacial suboxide bonding.[10] This article describes an alternative plasma-assisted oxidation/nitridation process.

Figure 1 illustrates how this process is accomplished for Si(100) substrates by tracking the process sequence by online Auger electron spectroscopy.[10] After an *ex situ* rinse in

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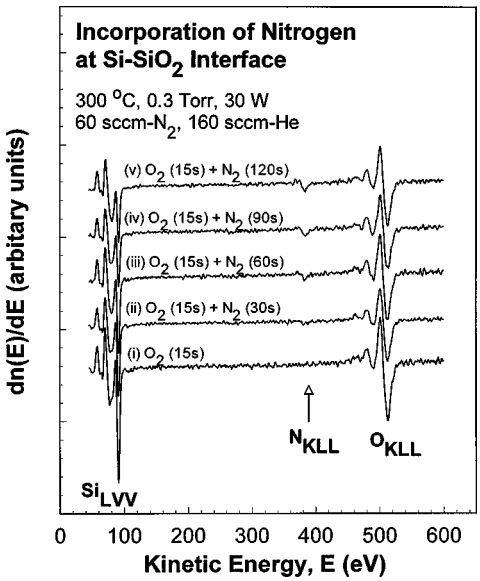

FIG. 1. Derivative AES spectra for interface nitridation times of 30, 60, 90, and 120 s following a 15 s plasma-assisted oxidation (Ref. 10).

dilute HF that (i) removes a thin sacrificial oxide layer and (ii) produces a hydrogen atom (H atom) terminated surface, the first step in the process is a remote plasma-assisted oxidation (RPAO) using excited species (e.g., O_2^*) extracted from a remote He/O_2 plasma.[3,9,10] This step (i) accomplishes an *in situ* clean that reduces carbon and fluorine atom contamination,[3] (ii) forms a $Si–SiO_2$ interface, and (iii) grows $\sim$0.5 nm of SiO_2 which serves as a substrate layer for the deposition of a dielectric film. The 0.5 nm oxide film also prevents further oxidation of the Si substrate during plasma-assisted deposition of oxide layers.[9] Interface nitridation is accomplished before deposition of the dielectric by exposure to the products from a remote He/N_2 plasma, primarily neutral N atoms.[11] Systematic changes in the N_{KLL} feature of the AES spectra in Fig. 1 demonstrate that the N-atom concentration in the dielectric increases with increasing plasma exposure time. Quantification of the rate at which N atoms are introduced in the dielectric will be discussed in the next section, where additional results from secondary ion mass spectrometry (SIMS) studies are presented.

Device structures were fabricated on these nitrided oxide interfacial oxide layers by completing the following additional steps: (i) 300 °C plasma-assisted deposition of SiO_2 from remote plasma excitation of a He/O_2 and downstream injection of SiH_4,[3,9,10] (ii) a 30 s 900 °C rapid thermal anneal,[10] (iii) formation of MOS capacitors using conventional photolithographic techniques following either (a) physical vapor deposition (PVD) of aluminum (Al) contacts, or (b) chemical vapor deposition, doping, and dopant activation of n^+ polycrystalline silicon contacts. Following electrode deposition, there was a conventional 30 min postmetallization anneal (PMA) at 400 °C in a forming gas (H_2/N_2) mixture. Interface characterization and device results are presented in Sec. III A.

B. ON stacked gate dielectrics

These were formed in two different ways. The gate stacks for the FETs were formed by the following *in situ* sequence:[8] (i) 300°C plasma-assisted oxidation using a remote He/O_2 plasma to form $\sim$1.3 nm of oxide; (ii) deposition of $\sim$1.3 nm of hydrogenated silicon nitride by a 300 °C remote plasma-assisted deposition process using SiH_4 and NH_3 as the source gases; (iii) a vacuum anneal at 900 °C for 30 s; and (iv) an on-line deposition of polycrystalline Si for the gate electrode. The remainder of the FET structure was formed by conventional processing techniques. A source gas ratio of $NH_3:SiH_4$ of $\sim$10:1 that previously gave optimum electrical performance in devices with ONO structures was used in the nitride deposition step.[11] Device results are presented in Sec. III C following a discussion of the unique properties of the plasma deposited nitride films in Sec. III B.

The MOS capacitors for the B-diffusion studies were fabricated on 5 Ω cm (100) *n*-type Si substrates with previously grown oxide gate dielectrics.[7] Gate oxides in the range from $\sim$3 to $\sim$6 nm were grown by furnace oxidation in dry O_2 at 800 °C. This was followed by deposition of nitride films 0.4–0.8 nm thick by 300 °C remote plasma-assisted process. The nitride layer thickness estimated by on-line AES, and confirmed by spectroscopic ellipsometry. The nitride deposition was followed by a 30 s 900 °C RTA. Undoped polycrystalline silicon, prepared by a conventional low pressure chemical vapor deposition (LPCVD) process with a thickness of $\sim$200 nm, was deposited following the gate dielectric RTA. Boron implantation into the polysilicon was performed at 12 keV to a dose of 5×10^{15} cm^{-2}; this was followed by an aggressive drive-in anneal in argon for 4 min at 1000 °C which activated and redistributed the implanted B atoms. MOS capacitors for electrical testing were completed by conventional metallization, patterning and postmetallization annealing processes. Electrical results for these PMOS device structures are presented in Sec. III D.

III. EXPERIMENTAL RESULTS

A. Interface characterization and tunneling studies

Figures 2(a) and 2(b) present the results of SIMS measurements made at Evans East on a stacked dielectric comprised of the nitrided interface and template film, $\sim$0.5–0.6 nm thick, and a $\sim$5 nm plasma-deposited SiO_2 film. The nitrided interface then is $\sim$5.5–6 nm below the film surface. The SIMS determination of N was made by counting both SiN^- and CsN^+ ions during the sputtering process. The profiles of these ions indicate that the N atoms are incorporated in the *immediate vicinity* of the $Si–SiO_2$ interface, and differences in the profiles are associated with the *drive-in* of the N atoms into the Si substrate during the SIMS measurements. Figures 3(a) and 3(b) indicate that the normalized SIMS signals of Figs. 2(a) and 2(b), respectively, display a linear dependence as function of nitridation time. In addition, based on normalization procedures discussed in Ref. 3, the

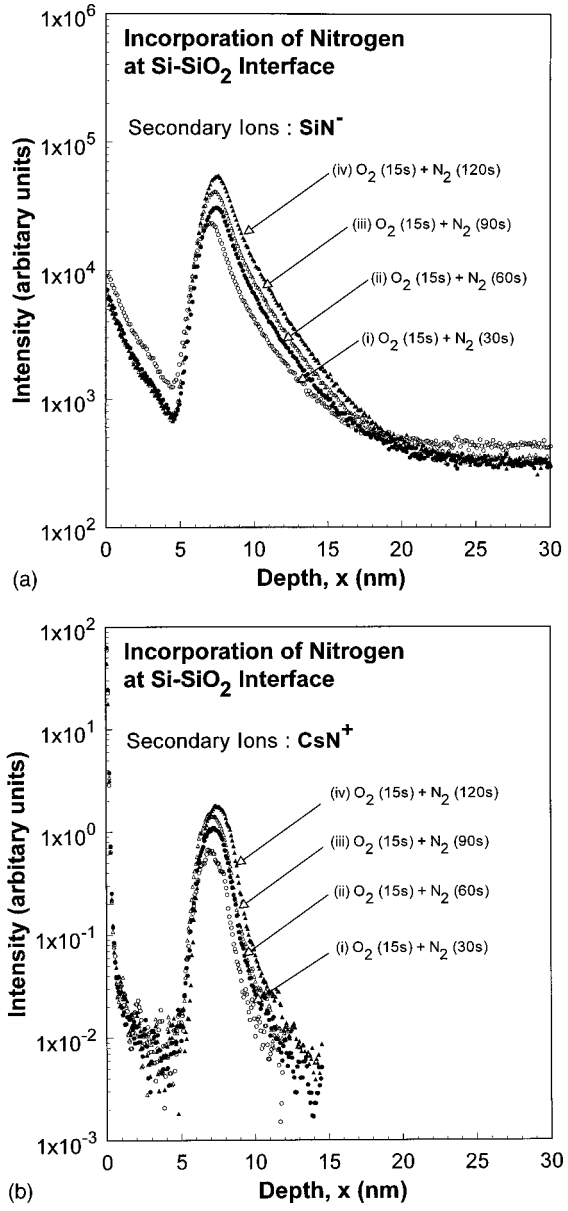

FIG. 2. SIMS data on nitride interfaces as a function of nitridation time (see Fig. 1), by detection of (a) SiN^- ions and (b) CsN^+ ions. The strong rise of the N-signal marks the interface between the dielectric and a crystalline Si substrate.

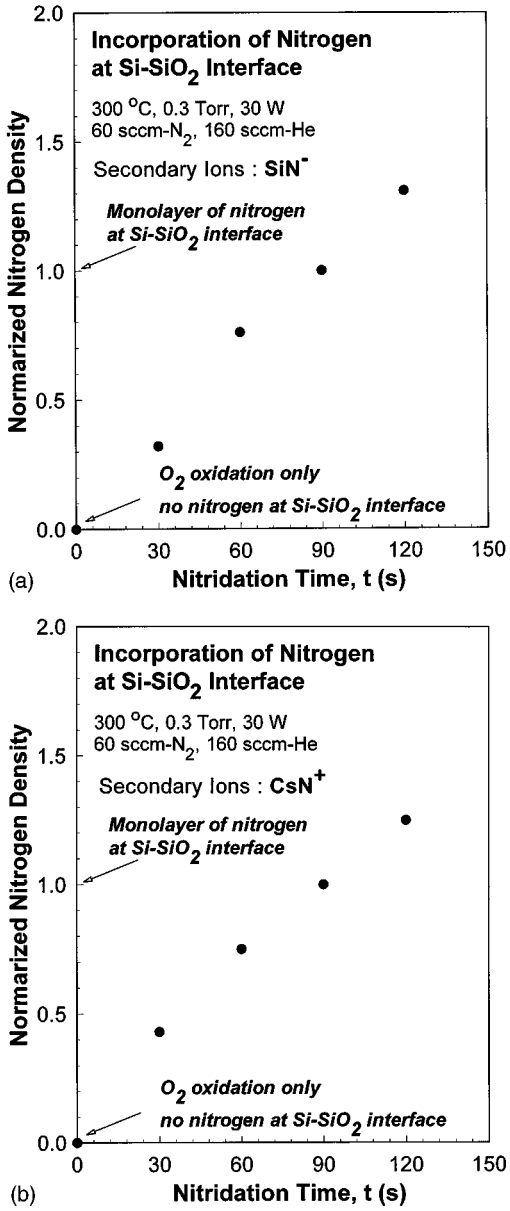

FIG. 3. Normalized plots of integrated ion counts vs time: (a) SiN^- ions and (b) CsN^+ ions. A normalized count of 1 corresponds to an ~1 monolayer of interfacial N atoms.

interface concentration of N atoms attains a monolayer coverage (±10%) after a 90 s exposure to the He/N_2 plasma process described above.

Figure 4 contains a plot of the ratio of the amplitudes of N_{KLL} and substrate Si_{LVV} (91 eV) features versus nitridation time. A plot of the N_{KLL} strength versus time shows a sublinear dependence. However, plotting the data as a ratio also yields a linear dependence of the nitrogen concentration versus nitridation time. The use of the N/Si ratio demonstrates that the N atoms are at the $Si–SiO_2$ interface, which is then more accurately characterized as a $Si–N–SiO_2$ interface. Since the 91 eV Si_{LVV} features comes from the substrate, normalization of the N_{KLL} signal takes into account passage of the N_{KLL} electrons through the oxide film, and the increase in overall film thickness as N atoms are incorporated at the $Si–SiO_2$ interface. Note that the escape depth for AES electrons with energies of 90 eV is approximately 0.6 nm. Since the SIMS data indicate a linear dependence of N-atom incorporation with time, the normalized plotting of the AES data establishes the N atoms are at the interface, rather than in the bulk of the plasma grown oxide layer.

Figures 5(a) and (b) are current density–voltage ($J–V$) plots for the MOS capacitors with nitrided interfaces and n-type substrates described in Sec. II A. The plot in Fig. 5(a) is for an oxide thickness of ~5 nm. This sample has an Al gate electrode, and the $J–V$ plot is for substrate injection. The current below about 3 V is displacement current associated with the ramped voltage that was used in the $J–V$ data acquistion. The tunneling currents for voltages approxi-

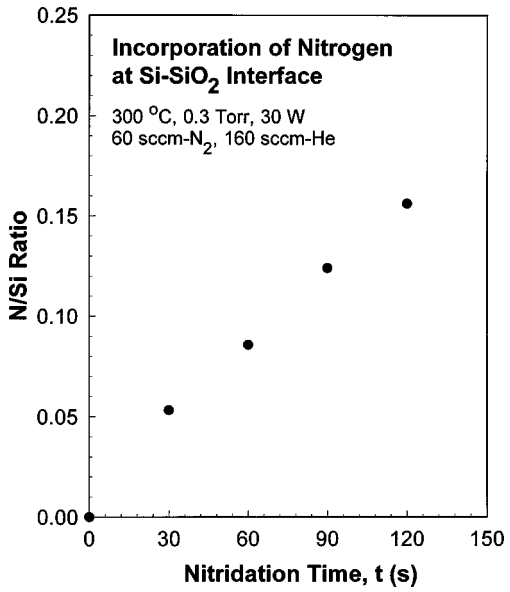

FIG. 4. Plot of the ratio of the amplitudes of N_{KLL} and substrate Si_{LVV} (91 eV) features vs nitridation time.

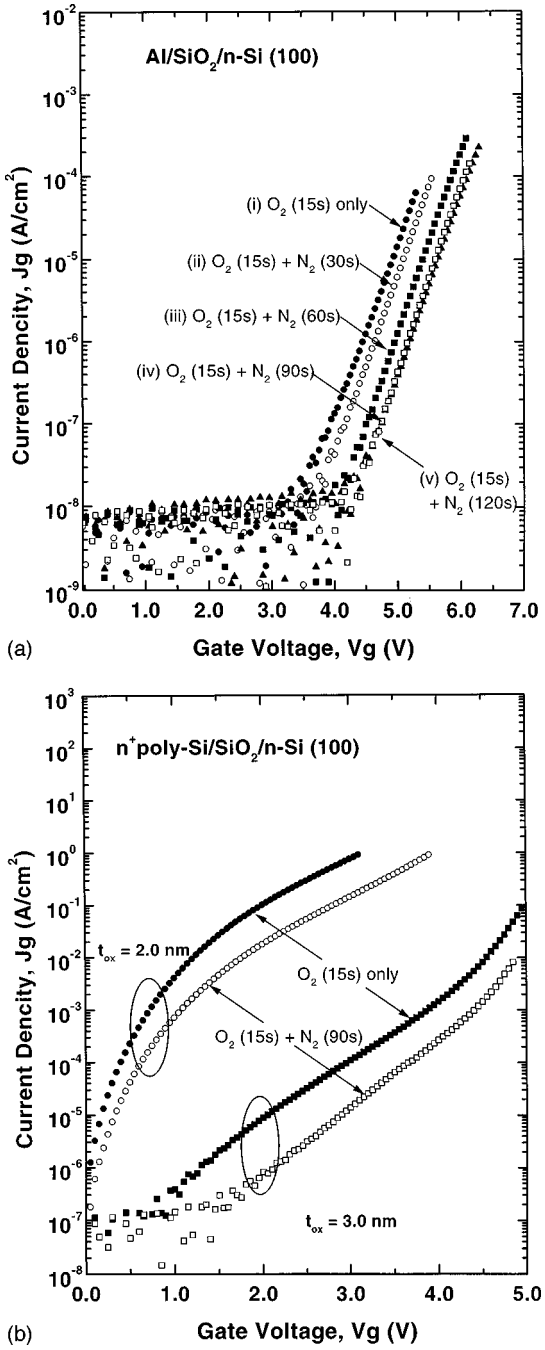

FIG. 5. (Current–density)-voltage ($J-V$) characteristics for substrate for NMOS capacitors: (a) with ~5 nm thick oxide layers, Al gate electrodes, and with (i) non-nitrided, (ii) and (iii) partially nitrided, and (iv) and (v) fully nitrided interfaces as discussed with respect with Figs. 1–4; and (b) for capacitors with ~2 and 3.0 nm oxide layers, with n^+ polysilicon gate electrodes for non-nitrided and fully nitrided interfaces.

mately 3 V and above are associated with a Fowler–Nordheim tunneling process. These tunneling currents decrease as the time of nitridation increases, and hence as the interfacial nitrogen concentration increases. For a fully-nitrided interface, the tunneling current is reduced by approximately an order of magnitude by the interface nitridation with respect to a non-nitrided interface. Similar reductions in tunneling current density are also observed for direct tunneling as in Fig. 5(b) which displays $J-V$ plots for oxide thickness of approximately 2 and 3.0 nm. These samples have n^+ polycrystalline Si gate electrodes and the $J-V$ plots are also for substrate injection. It is important to note that the flat-band voltages for the MOS structures of Figs. 5(a) and 5(b), do not vary by more than 0.05 eV, so that the changes in the $J-V$ plots represent decreased current flow, and are not a result of differences in zero-bias built-in electric fields. Finally, similar results have been obtained for samples with p-type substrates and oxide thicknesses of ~5 nm. For these samples, tunneling currents for gate injection were also reduced by approximately a factor of 10 as interface nitridation increased to the ones monolayer level. As in the case of the MOS devices prepared on n-type substrates, the flat-band voltages for the MOS capacitors prepared on p-type substrates also displayed a change of no more than ~0.05 eV between the non-nitrided and fully-nitrided interfaces.

B. Characterization of plasma deposited nitrides

The hydrogenated plasma deposited nitrides have been characterized by infrared (IR) absorption measurements.[12] IR spectra indicated features due to: (i) the Si–N asymmetric bond-stretching vibration at ~850 cm^{-1}; (ii) the bond-stretching vibration of the N–H group at ~3350 cm^{-1}; (iii) the bond-bending vibration of the N–H group at ~1150 cm^{-1}, and (iv) the bond-stretching vibration of the Si–H group at ~2170 cm^{-1}. Films deposited at 300 °C from different source gas mixtures of NH_3/SiH_4 established that beginning at about 400 °C hydrogen was evolved from the film. The loss of H atoms could be described by a temperature-activated process with an activation of ~0.4 eV. This was consistent with H-atom loss being associated with processes in which molecular H_2 was formed. For example, it was

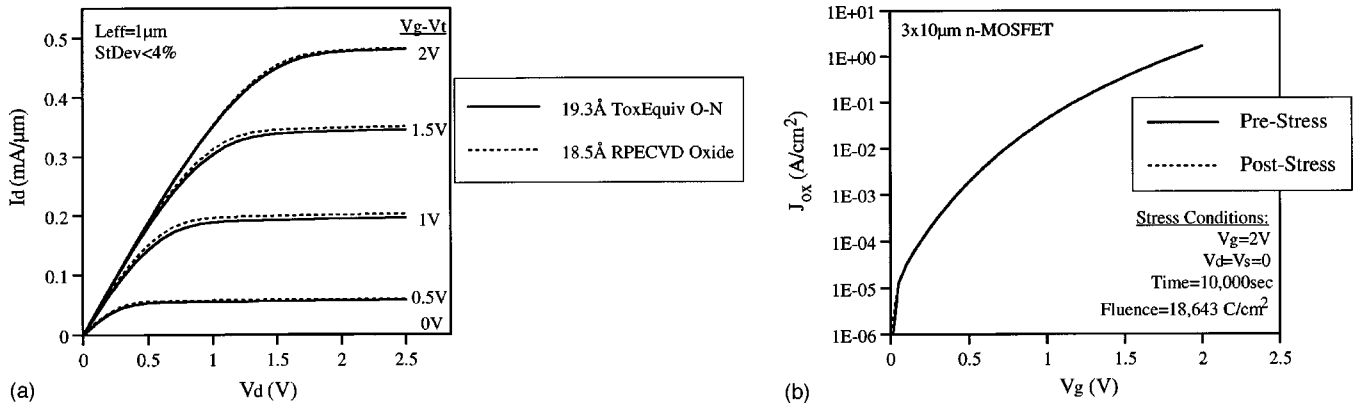

FIG. 6. (a) Current–voltage characteristics of FETs with ultrathin oxide and stacked ON gate dielectrics. (b) Reliability for ultrathin FETs with stacked ON gate dielectrics.

demonstrated that the hydrogenated silicon nitride films contained nearest-neighbor Si–H—H–N–Si bonding arrangements, and that there were significant decreases in the both the Si–H and N–H vibrational signatures with annealing.[12,13] A reaction pathway for H-atom evolution that is suggested by these results is

$$\text{Si–H—H–N–Si} \rightarrow \text{Si}^0 + {}^0\text{N–Si} + \text{H}_2, \tag{1}$$

where the superscript notation (^{0}) indicates a neutral dangling bond, and the H—H notation indicates nearest network neighbors. In the temperature range to about 500–600 °C, the only significant changes in the IR were decreases in the amplitudes of the Si–H and N–H vibrations, whereas at temperatures greater than about 600 °C, there was a systematic increase in the amplitude of the Si–N feature. The combination of these results for annealing temperature >600 °C suggests that as H atoms were evolved from the films, new Si–N bonds were formed. This is represented symbolically in Eqs. (2a) and (2b):

$$\text{Si–H—H–N–Si} \rightarrow \text{Si}^0 + {}^0\text{N–Si} + \text{H}_2, \tag{2a}$$

$$\text{Si}^0 + {}^0\text{N–Si} \rightarrow \text{Si–N–Si}. \tag{2b}$$

The as-deposited films also contain SiNH groups in two other bonding arrangements: (i) in nearest-neighbor pairs, where they interact via H-bonding interactions, and (ii) as isolated bonding groups where the H atoms of the N group interact with near-neighbor N atoms of the network. The interactions in (ii) are also H-bonding-type interactions, and the distribution of near-neighbor N atoms is determined by the local network bonding at the particular N–H site. Loss of hydrogen with the subsequent evolution of different N–H bonding groups such as N–H_2 can occur from the nearest neighbor pairs, with reaction pathways being similar to those described in Eqs. (1) and (2). Loss of H atoms from the isolated N–H groups is considerably less likely due to the relatively high N–H bond energy, of the order of 5 eV.

As noted in Sec. II, a source gas ratio of $\text{NH}_3:\text{SiH}_4$ of ~10:1 gave optimum electrical performance. Combining IR and AES data with a statistical model of bonding in amorphous Si:N:H alloys indicates that this source gas ratio corresponds to a film in which the respective silicon, nitrogen, and hydrogen concentrations are [Si] ~28 at. %, [N] ~42 at. %, and [H] ~30 at. %[14] It was shown in Ref. 14, that the average number of bonds/atom for this composition is ~2.7, the same as in device-quality plasma-deposited SiO_2 films. In addition, hydrogenated silicon nitride films with this composition have been used in amorphous silicon thin film transistors as the gate dielectrics and yielded optimized electrical performance. For example, transconductance electron mobilities of ~1.5 $\text{cm}^2\ \text{V}^{-1}\ \text{s}^{-1}$ 15 were obtained indicating a low concentration of charged defect centers. For both lower and higher source gas ratios, the film composition changed and the effective channel mobility decreased. This behavior has been interpreted as being a manifestation of the similarity in bonding statistics to SiO_2 as noted earlier in this paragraph.

C. Electrical performance of FETs with ON dielectrics

Figures 6(a) and 6(b) present data on the performance and reliability of FETs incorporating stacked ON gate dielectrics.[8] These data have been discussed in more detail in Ref. 8. In summary, the approximate electrical thickness of the gate dielectrics was obtained to ±1 Å from analysis of capacitance–voltage ($C-V$) data. TEM micrographs of the composite ON structures indicated approximately equal oxide and nitride layer thickness. Based on an approximately 1:2 ratio of silicon nitride to silicon oxide static dielectric constants, this means that a 1.8±0.1 nm ON film is comprised of oxide and nitride layers which are each approximately 1.2±0.1 nm thick. The transistor characteristics, drain current, I_d, versus drain bias voltage, V_d, plotted for different normalized gate voltages ($V_g - V_{th}$, where V_g is the gate voltage and V_{th} is the threshold voltage). Since the I_d is proportional to the inversion capacitance, the equality of the drain currents for the two devices is consistent with their having the same oxide equivalent dielectric thickness. Figure 6(a) demonstrates that the FET with the ON dielectric performs as well as a FET with an oxide dielectric. The oxide dielectric in this case was formed by a combination of (i) 300 °V remote plasma-assisted oxidation and deposition, and

(ii) an *in situ* vacuum anneal at 900 °C for 30 s. The current voltage plots in Fig. 6(b) indicate the robust nature of the ON gate dielectric, i.e., there is no detectable degradation after an integrated current exposure equivalent to about 1.6×10^4 C cm^{-2} (V_g=2.0 V). Finally, the direct tunneling current for the FET with the ON dielectric was reduced by a factor of ~5–7 with respect to that of the FET with oxide dielectric.

D. Boron penetration studies for ON films

Quasi-static $C-V$ curves were compared in Fig. 7(a) for MOS capacitors (i) with a control thermal oxide, and (ii) with composite oxide–nitride dielectrics with 0.4 nm, and 0.8 nm thick nitride layers. The $C-V$ curve for the control oxide shifted significantly to a relatively high flatband voltage, $V_{FB,}$ as compared to nitride-deposited devices indicating a large amount of B atom penetration has occurred. This was confirmed by preparing capacitors with Al gate electrodes on the different gate dielectrics used above, i.e., the control thermal oxide, and the composite oxide–nitride dielectrics. The flatband voltages for these NMOS structures were obtained from $C-V$ measurements and were also essentially the same, -0.82 ± 0.1 V. Using these results enabled us to determine an anticipated value for using a B-atom doped polycrystalline Si gate electrode in a PMOS structure. One of the most important aspects of this comparative study on NMOS structures was the consistency of the flatband voltages for the different gate dielectric structures. This consistency means that introducing the nitride films on the oxide substrate did not introduce fixed charge at either the Si–SiO_2 interface, or the internal interface between the nitride and oxide constituents of the dual layer dielectrics similar to what had been found in our earlier studies tri-layer oxide–nitride–oxide dielectrics which were made using essentially the same sequence of plasma and rapid thermal annealing process steps.[15] The anticipated V_{FB} is approximately +0.7 V, and V_{FB} for the control oxide is shifted to approximately +1.1 V. The V_{FB} value for the capacitor with the 0.8 nm nitride is at approximately +0.7 eV indicating essentially no boron penetration to the underlying n-type Si substrate. V_{FB} for the device with the 0.4 nm top nitride is intermediate, approximately +0.8 V, which shows the degree of boron penetration is controllable for a fixed thermal budget by changing the deposited nitride layer thickness. Oxide reliability was examined by measuring charge to breakdown (Q_{BD}) under constant Fowler–Nordheim current stressing as shown in Fig. 7(b). Each experimental point is the average of 15 device runs. Q_{BD} was highest for film with the thickest top nitride layer. The relative decreases in Q_{BD} in capacitors with the control oxide, and the composite dielectric with the 0.4 nm nitride layer are attributed to boron penetration. The Q_{BD} value of the capacitor with the 0.8 nm top nitride is twice as high as that of the capacitor with the control oxide. As a point for reference, the Q_{BD} values for MOS capacitors with Al-gate electrodes were found to be essentially the same as that of the capacitor with the dual layer oxide–nitride dielectric with the 0.8 nm nitride. Figure 7(c) shows applied gate voltages shifts as a function of injected charge. The reliability of the devices with the top surface nitride layers is clearly improved.

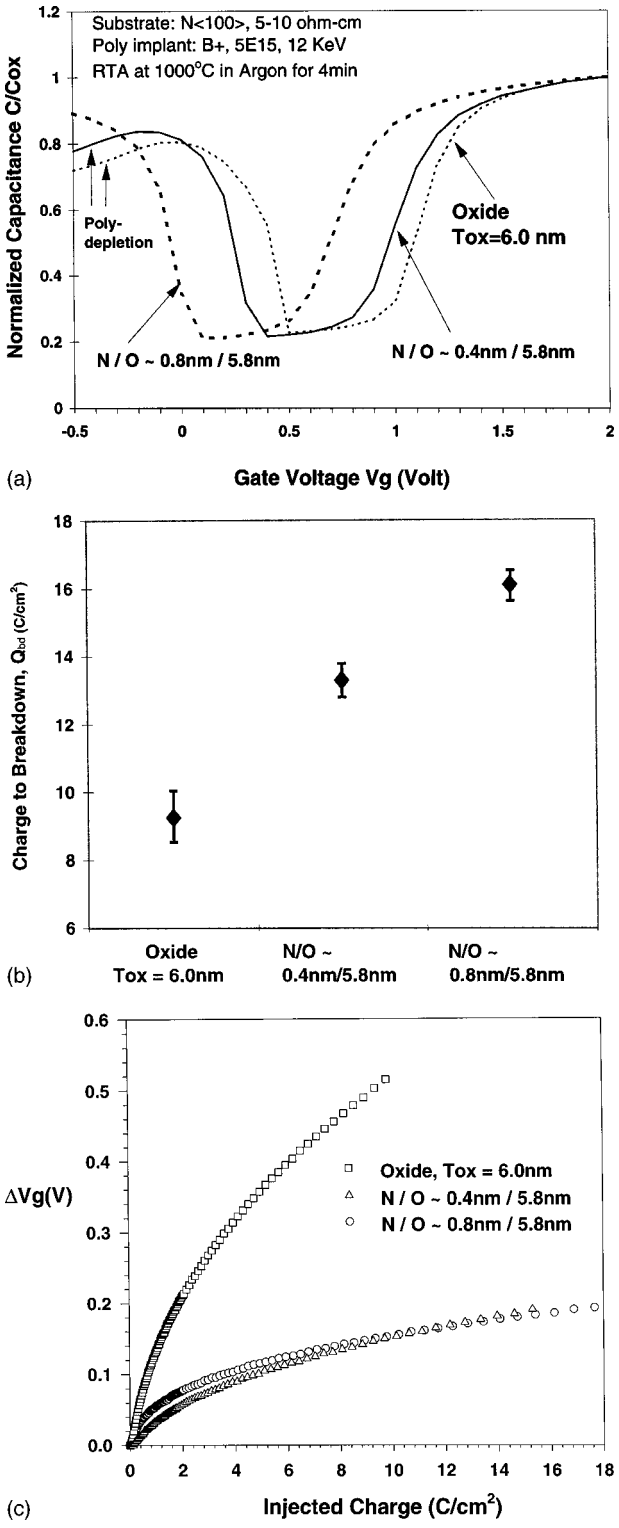

FIG. 7. Date for PMOS devices with ~5–6 nm dielectrics: (a) Normalized quasistatic $C-V$ curves for MOS capacitors with different thickness of top nitride layers: t_n=0.0, 0.4, and 0.8 nm; (b) charge to breakdown (QBD) for 50% failure under constant current substrate injection at 100 mA cm^{-2}; and (c) applied gate voltage shifts, dV_g during the same constant current substrate injection as in (b).

IV. DISCUSSION

This section is divided into three parts which address, respectively: (i) the reduction of tunneling currents in MOS capacitors with nitrided interfaces; (ii) the unique character of the nitride films formed by the two step process sequence of 300 °C deposition by remote plasma-assisted deposition followed by a vacuum or inert ambient RTA for 30 s at 900 °C; and (iii) the suppression of nitrogen diffusion through ultrathin nitride layers.

A. Nitrided interfaces

The $J-V$ data in Figs. 5(a) and 5(b) in Sec. III A indicate significant decreases in tunneling current density with increasing interface nitridation. At first sight this result is surprising since the $Si-SiO_2$ conduction band off-set energy is significantly higher than the $Si-Si_3N_4$ conduction band off-set energy, ~3.1 eV as compared to 2.1 eV,[16] suggesting that interfacial nitridation would be expected to increase tunneling currents. The nearly constant reduction of tunneling current for thicknesses in the Fowler–Nordheim regime as in Fig. 5(a), and in the direct tunneling regime as in Fig. 5(b), as well as the fact that similar reductions occur for both substrate and gate injection, indicates that the reduction is not simply due to changes in effective oxide thickness, or the direction of current injection. Flat-band voltages, obtained from analysis of $C-V$ curves have indicated a small variation of flat-band voltage with interface nitridation (<0.05 V), demonstrating that built-in oxide fields were not the cause of the current reductions. In addition, a newly developed model for band off-set energies that includes the effects of charge transfer interface dipoles places an upper limit on the possible flat band voltage shifts[17] of ~0.1 eV that supports to the results of the $C-V$ and $J-V$ studies.

Studies of $Si-SiO_2$ interfaces have shown that the oxidation of Si invariably results in transition regions with excess suboxide bonding between the crystalline Si substrate and the SiO_2.[18] If Φ_{ms} is the metal-semiconductor work function in the absence of interfacial dipoles, then the effective metal-semiconductor work function for a non-nitrided interface with interfacial Si–O bonds, $\Phi'_{ms}(Si-O)$, is given by:

$$\Phi'_{ms}(Si-O) = \Phi_{ms} - V_{dipole}(Si-O), \quad (3)$$

where $V_{dipole}(Si-O)$ is the potential energy step associated with interfacial dipoles. This potential energy step adds to the conduction band offset as determined from vacuum levels. In Ref. 17, it is demonstrated that $V_{dipole}(Si-O)$ depends on the nature of the bonding at the $Si-SiO_2$ interface. The dipole step is greater for an abrupt $Si-SiO_2$ interface, $V_{dipole}(Si-O_{abrupt})$, than for an interface with suboxide bonding, $V_{dipole}(Si-O_{suboxide})$. In addition, it was shown that the dipole step is greater for a nitrided $Si-N-SiO_2$ interface than for an interface with significant suboxide bonding as has been reported for $Si-SiO_2$ interfaces even after a 30 s 900 °C RTA. The difference in the height of the potential barrier between a nitrided interface and an interface with suboxide bonding is given by

$$\delta V = V_{dipole}(Si-N) - V_{dipole}(Si-O_{suboxide}). \quad (4)$$

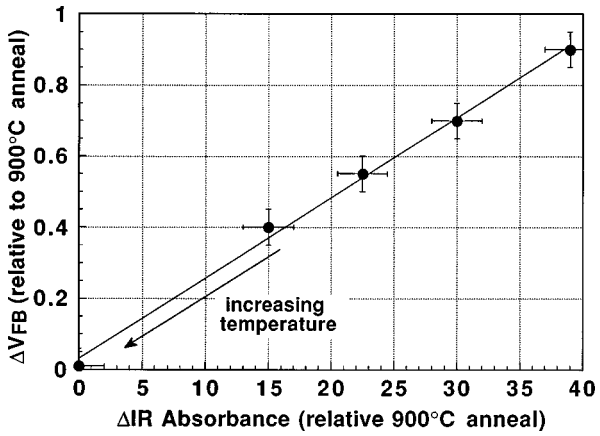

FIG. 8. Decreases in V_{th} as a function of increases in peak IR absorption strength in Si–N bond-stretching mode. The arrow in the figure indicates the direction of increased annealing temperatures. Data are normalized with respect to values at 900 °C.

The calculations of Ref. 18 show that δV at most equal to 0.1 eV so that the barrier height is not significantly different for an abrupt nitrided interface and for a $Si-SiO_2$ interface that has a minimized degree of suboxide bonding after a 900 °C RTA. The driving force for dipole formation is an equalization of a chemical potential that can be obtained from considerations of the relative electronegativities of the interfacial bonding arrangements. Under this driving force, electrons are transferred from the Si substrate to the dielectric. The magnitude of the charge transfer is $\sim 0.1-0.2e$, where e is the charge on the electron.[17] This analysis supports the results of the $C-V$ and $J-V$ measurements of Sec. III A; i.e., that the changes in tunneling currents are not due to systematic changes in built in fields, associated with changes in flat band voltages.

Therefore, an alternative mechanism must be invoked to explain the tunneling results. One way to interpret the data in Figs. 5(a) and 5(b), as well as the additional results for the *p*-type substrate, is to invoke an interfacial *reflection coefficient* that is significantly different for non-nitrided and fully-nitrided $Si-SiO_2$ interfaces. One rationale for this type of effect has its origin in effects well-known in physical optics, where thin surface layers of transparent materials with different optical indices of refraction will either enhance or reduce surface reflectivity, and thereby reduce or enhance, respectively, the optical transmission independent of the surface on which the light is incident. The optical path length for these surface layers must be in the range of about one-quarter of the optical wavelength in the surface layer material. For this type of mechanism to apply to the nitrided oxide dielectrics, the monolayer nitridation would have to have an *effective index of refraction higher than* that of the oxide surface. Stated differently, the reduced tunneling mechanism would have to rely on a significant phase shift for the electron transport in the nitrided layer relative to that of the non-nitrided interface. This type of contribution to the tunneling transport needs additional theorectical and experimental study.

B. Unique chemical bonding in plasma-deposited nitride layers

As has already been shown in Sec. III B, the nitride films prepared by 300 °C, and subsequently subjected to a 900 °C RTA display interesting behavior in regard to H loss as well as Si–N formation. The explanation for the unexpected electrical properties of these films, that has evolved from a combination of the IR studies and electrical data is best illustrated in Fig. 8. The *x* axis of this figure is obtained from IR data, and the *y* axis from electrical data on MOS capacitors. The decrease of V_{FB} to its expected value in films annealed at 900 °C is indicative of decreases in fixed dielectric positive charge, i.e., reductions in defects in the nitride film. Therefore this figure demonstrates that the formation of additional Si–N bonds from bonding groups that have loose H atoms is responsible for the improved behavior.

To best understand the unique attributes of the two-step process for forming device-quality nitride films with low bulk defect densities, it is necessary to contrast the bonding changes that take place in these films as a function of processing, with the bonding in nitride films prepared by conventional higher temperature (T>500 °C) LPCVD processes. Summarizing the IR data presented above: (i) as-deposited silicon nitride films are Si:N:H alloys with an average number of bonds/atom (~2.7) which is essentially the same as deposited SiO_2; (ii) these films are therefore low defect continuous random network structures with low bulk defect densities, primarily because of their high H-atom content (~30 at. %); (iii) these films contain several kinds of bonded H: (a) in nearest-neighbor SiH/SiNH and SiNH/SiNH pairs, and (b) in isolated SiNH groups; (iv) upon annealing to 500 °C, H is released from these nearest-neighbor groups leading to defect formation as both Si- and N-atom dangling bonds; (v) upon further annealing at temperature >500 °C, H evolution continues, but additional Si–N bonds are formed; (vi) the formation of additional Si–N bonds from bonding sites that have lost H atoms reduces bulk defect densities accounting for the unique electrical properties of the films. In effect the special bonding arrangements in which H atoms are nearest-network neighbors in the as deposited films is the key to the unique behavior. For example, these bonding sites are the reason for poor performance in films annealed to 500 °C, but are the reason for improvements in performance in films that have been annealed to 900 °C. The IR spectra of Ref. 12 clearly indicate that additional Si-N bonds are formed after the 900°C anneal; however, at this time we offer no microscopic model for the atomic motions that are involved in these relaxation processes.

It is found in Ref. 12 that the nitride films contain bonded hydrogen after 900 °C. This is mostly in isolated bonding arrangements in SiNH bonding arrangements. The bonding energy of the HN bond in a SiNH group is in excess of 5 eV. As an isolated bonding arrangement, this site will not be an electronically active defect, although under certain conditions it may act as a defect precursor. One pathway for defect generation is through hole trapping and the formation of an ammonium center. However, at the low bias voltages that are contemplated for the stacked ON gate dielectrics, hole injection into the nitride layer is unlikely.

In contrast, films prepared by LPCVD at temperatures in excess of 500 °C contain only small concentrations of bonded H, and in order to form a network comprised of threefold coordinated N atoms and fourfold coordinated Si atoms, these films must contain significant numbers of both Si- and N-atom dangling bond defects. Entropy considerations require that these defects be distributed throughout the network rather than occurring as nearest-neighbors. Since silicon–nitride films do not display a viscoelastic relaxation, these bonding defects cannot recombine, as in the films produced at lower temperature by remote plasma processing, and therefore the films have high defect densities even after higher temperature processing. The only way that defects in these films can be reduced in density is by postdeposition annealing in an oxygen containing ambient as shown by the recent results reported by the University of Texas at Austin Group.[19] Films prepared in this way are oxynitride alloys with dielectric constants below those of silicon nitride. Oxynitride alloy films have been incorporated into FETs, but in general this leads to significant reductions in peak channel mobilities in NMOS devices.[20]

C. Stopping power of nitride layers for B-atom diffusion

The stopping power of nitride films prepared by remote plasma processing and subsequent RTAs is simply associated with the high areal density of N atoms obtained in this way. The areal density of N atoms in a film that is 0.8 nm thick is estimated to be $4-5\times10^{15}$ cm^{-2}.[7] Since the bonding radius of N atoms is ~0.8 nm, this means that the fractional area coverage of these N atoms is ~0.8–1.0. Since it has been shown that the diffusion of B atoms through oxide films involves B–O bond formation, the 0.8 nm nitride film effectively screens the B atoms from the O atoms in the underlying oxide film of the stacked ON dielectric.[21] Reducing the nitride thickness to ~0.4 nm reduces the fractional coverage to 0.4–0.5, enabling the B atoms to interact with the underlying oxide layer, and be transported to the Si substrate where they can degrade electrical performance. As anticipated, increasing the nitride layer to 1.2 nm, as in the FETs described above will then not only reduce direct tunneling, but also improve resistance to B-atom penetration in PMOS devices.

V. SUMMARY

This article has indicated a processing pathway to the formation of ultrathin nitrided gate oxides that can play a significant role in advanced FET devices. By using 300 °C plasma assisted processing including: (i) oxidation and nitridation to form nitride interfaces and an ultrathin oxide film (~0.5–0.6 nm thick) that serves as a platform for further film deposition, and (ii) film deposition forms ultrathin oxide, nitride, or stacked ON dielectrics, in combination with low thermal budget RTAs (typically 30 s at 900 °C), it has been shown that device-quality ultrathin gate dielectrics can

be formed. The interface nitridation and ON stacked dielectrics have been demonstrated to yield improved behavior with respect to ultrathin oxides in NMOS devices with oxide equivalent thickness down to 1.8 nm. Extensions of this approach, based on the calculation of tunneling currents in stacked ON devices suggests that the stacked ON dielectrics can be used for several device generations, in particular for $t_{\mathrm{ox\,eq}}$ extending down to at least 1.5 nm, and perhaps to 1.2 nm. The stacked ON gate dielectrics with at least 0.8 nm of nitride have shown excellent resistance to B-atom transport out of p^+ polycrystalline silicon gate electrodes. Since the top surface nitridation process also nitrides the $Si-SiO_2$ interface,[22] the channel mobilities of holes in PMOS devices may be degraded by the use of these structures.

ACKNOWLEDGMENTS

This work was supported in part by the NSF Engineering Research Center for Advanced Electronic Materials Processing at North Carolina State University, the Office of Naval Research, and the Semiconductor Research Corporation.

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