The Effects of Interfacial Sub-Oxide Transition Regions and Monolayer Level Nitridation on Tunneling Currents in Silicon Devices

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***Abstract*—Direct tunneling (D-T) in Si metal-oxide-semiconductor (MOS) devices having 1.8 to 3 nm thick gate oxides is reduced approximately tenfold by monolayer Si-dielectric interface nitridation with respect to devices with nonnitrided interfaces. The reduction is independent of gate oxide-equivalent thickness, and gate or substrate injection, and extends into the Fowler–Nordheim tunneling (F–N–T) regime for thicker oxides as well. A barrier layer model, including sub-oxide transition regions, has been developed for the interface electronic structure for tunneling calculations using X-ray photoelectron spectroscopy data. These calculations provide a quantitative explanation for the observed tunneling current reductions.**

I. Introduction

EXPONENTIAL increases in tunneling current with decreasing gate oxide thickness, tox, present a significant limitation in aggressive scaling of Si MOS devices for $t_{ox} < 2.5$ nm. The SIA National Technology Roadmap for Semiconductors [1] calls for oxide-equivalent thicknesses, $t_{ox\text{-}eq}$, < 1 nm by 2112, stimulating research on alternative insulators with dielectric constants, ε, higher than SiO_2. Implementation of alternative dielectrics increases capacitance without accompanying decreases in physical thickness, and has generated near-term interest in nitrided oxides, including oxide/nitride stacks [2]–[5] and oxynitride alloys [6].

Studies have demonstrated that tunneling is reduced in devices with monolayer Si-SiO_2 interface nitridation compared to devices with nonnitrided interfaces and the same $t_{ox\text{-}eq}$ [3], [7]. Tunneling is reduced by about 8 ± 2 for both substrate and gate injection for $t_{ox\text{-}eq} \sim 1.8$ to 3 nm. Reductions are not due to 1) flatband voltage shifts [7], 2) *simple* increases in physical thickness [7], and/or 3) decreases in interface roughness [8]. Mesarjian *et al.*were first to recognize interfacial transition regions with sub-oxide bonding modified F-N tunneling [9]. This letter extends their approach into the D-T regime, using X-ray photoelectron spectroscopy (XPS) to estimate the widths of the interfacial transition regions [10].

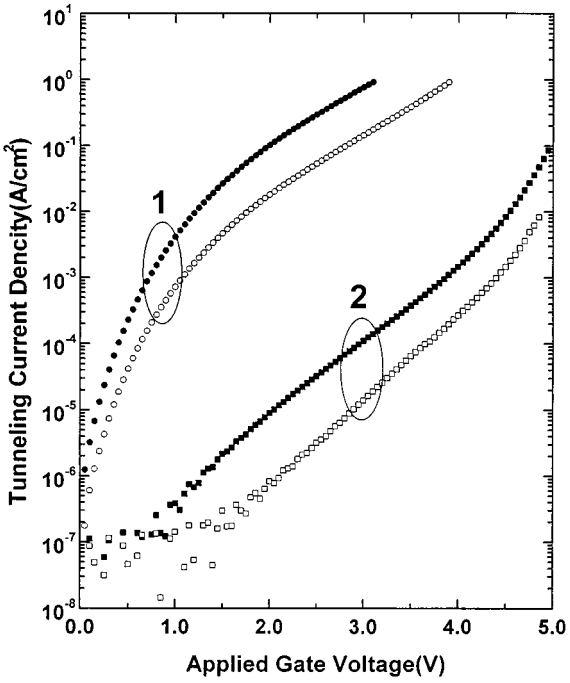

Fig. 1. Current density-voltage (J-V) plots for devices with oxide dielectrics for substrate injection for n^+-poly-Si-SiO_2-n-Si devices with nonnitrided (solid squares) and nitrided (open squares) interfaces with $t_{ox\text{-}eq} = 2.0$ nm (group 1) and 3.0 nm (group 2). The doping in the n layer is ~2–5 × 10^{17} cm^{-3}.

II. Experimental Results

Fig. 1 displays J–V plots in the D-T regime for devices prepared by combined remote plasma-assisted/rapid thermal processing [7], [11]. Similarly, J–V data in the F-N regime show a saturation in current reduction of ~10–15 for interface nitridation at the monolayer level [7], [11]. The characterizations used to establish interfacial nitridation, and quantify N concentrations are detailed in [7], [11] and [12]. Etch-back combined with Auger electron spectroscopy, angle-resolved XPS (ARXPS) and nonlinear optical second harmonic generation (SHG) demonstrated interfacial N-localization; while secondary ion mass spectrometry and nuclear reaction analysis established the N content and identified process conditions for achieving monolayer N-concentrations of 7 ± 1 × 10^{14} cm^{-2} at Si(100)-SiO_2 interfaces [7], [11].

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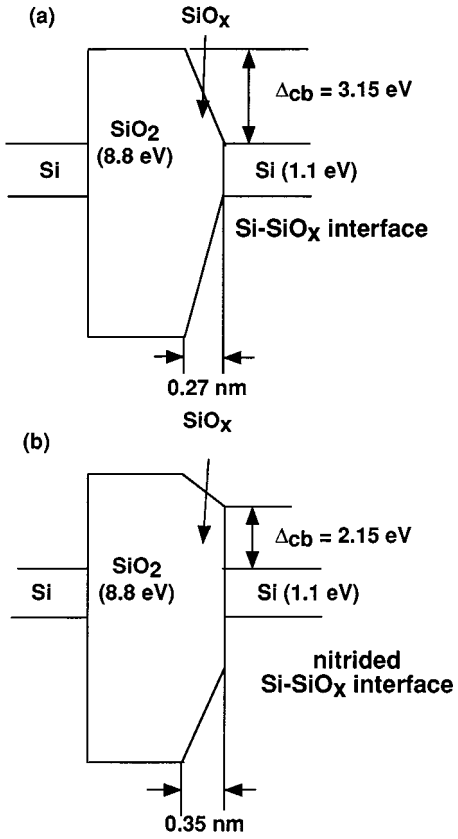

Fig. 2. Schematic representations symmetric n-Si-SiO_2-n-Si gate stacks with (a) a sub-oxide (SiO_x) interfacial transition region, and (b) a sub-oxide interfacial transition region (SiO_x) with a nitrided Si-dielectric interface. The widths of the interfacial regions have been estimated from XPS studies [10].

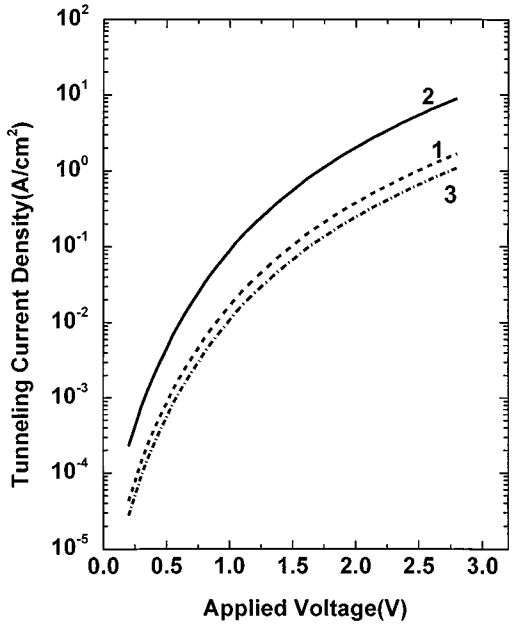

Fig. 3. Calculated D-T currents for devices with $n^+(5 \times 10^{19} cm^{-3}$ Si-SiO_2-n (5×10^{17} cm^{-3} Si gate stacks with an oxide equivalent thickness, $t_{ox\text{-}eq} = 2.0$ nm. The gate stacks are 1) and *ideal* oxide with abrupt interfaces: $t_{ox} = 2.0$ nm, (curve 1); 2) an oxide with a sub-oxide transition region: $t_{ox} = 1.85$ nm and $t_{trans\ region} = 0.27$ nm as in Fig. 2(a) (curve 2); and 3) an oxide with a sub-oxide transition region with a nitrided interface: $t_{ox} = 1.77$ nm and $t_{trans\ region} = 0.35$ nm as in Fig. 2(b) (curve 3).

XPS studies were performed on Si(111) and Si(100) substrates with similar results: 1) interfaces showed integrated spectral content in the sub-oxide/nitride bonding regime between the $2p$ Si substrate feature at ~99 eV and the SiO_2 bulk oxide feature at ~103.5 eV in excess of the monolayer defining the interface; 2) integrated intensities in this region decreased by 15–20% between as-deposited (300°C) and annealed conditions (900°C) consistent with other measurements [13]; and 3) decreases in sub-oxide bonding occurred predominantly in arrangements not intrinsic to a particular surface (e.g., the Si^{2+} feature decreased markedly on Si(111) after a 900°C inert ambient anneal [10]). Other studies have shown that interfaces formed by thermal oxidation at 900°C display additional changes in interface morphology after 900°C nonoxidizing anneals [14], emphasizing *fundamental differences* in interface morphology and bonding for growth and annealing at the same temperatures.

III. Modified Barrier Layer Model for Direct Tunneling

Fig. 2 indicates modified interface structures proposed for 900°C annealed [Fig. 2(a)] nonnitrided and [Fig. 2(b)] nitrided Si-SiO_2 interfaces. The sub-oxide bonding in (a) defines a transition region between the Si substrate and SiO_2 dielectric with an average SiO_1 composition. Following [9], a linear variation in the conduction band offset energy has been assumed. The width of this region was estimated from XPS results. First, the areal density of Si atoms in a mono-molecular layer with an SiO_1 composition ($5.2 \pm 0.1 \times 10^{14}$ cm^{-2}) was determined by averaging Si-atom areal densities in c-Si ($\sim 7.8 \times 10^{14}$ cm^{-2}) and SiO_2 ($\sim 2.6 \times 10^{14}$ cm^{-2}) The thickness of a molecular layer of SiO_1 0.32 ± 0.05 nm, was obtained by similar averaging. For nonnitrided interfaces, XPS data indicated an excess Si areal density of $4.4 \pm 0.4 \times 10^{14}$ cm^{-2} or approximately 0.85 ± 0.1 of a molecular layer. This corresponds to a transition region width of ~0.27 ± 0.03 nm. For the nitrided interfaces the corresponding excess areal density increases to ~1.1 ML with a thickness ~0.35 ± 0.03 nm. The observance of different resonance energies for nitrided and nonnitrided Si-SiO_2 interfaces in optical SHG measurements [12] establishes that conduction band offset profiles at these interfaces are different. A potential step of 2.15 eV, equal to the conduction band offset energy between Si and Si_3N_4 has been applied at the nitrided Si-dielectric interface, and following [9], the remainder of transition region is represented in Fig. 2(b) by a linear variation between the top of the interface step and the SiO_2 conduction band edge.

Fig. 3 compares calculations of D-T based on the WKB approximation [15], [16] for three different dielectrics, each with $t_{ox\text{-}eq} = 2.0$ nm:

1) an ideal oxide with no interfacial sub-oxide bonding (curve 1) ($t_{ox} = 2.0$ nm);
2) an oxide with interfacial sub-oxide bonding (curve 2), ($t_{ox} = 1.85$ nm);
3) an oxide with interfacial sub-oxide bonding and a nitrided interface (curve 3), ($t_{ox} = 1.77$ nm).

The tunneling barrier is 3.15 eV, and the tunneling mass is $0.5m_o$ [15], where m_o is the free electron mass. The deter-

minations for t_{ox} for 2) and 3) fixed $t_{ox\text{-}eq} = 2.0$ nm, and assumed in the sub-oxide regions in 2) has increased from 3.8 for SiO_2 to 6.7, and in 3) from 3.8 to 5.7. These calculations demonstrate that D-T currents are reduced by interfacial nitridation ~8–10 with respect to devices with sub-oxide bonding alone. Additionally, the calculated tunneling in the device with the nitrided interface is nearly equal to that of the device with *ideal* abrupt interface; in the spirit of the WKB approximately the same thickness-(tunneling mass-average barrier height)$^{0.5}$ products [15], [16].

The *approximate* reduction in direct tunneling current, $R_{D\text{-}T}$, can be estimated using the WKB approximation [15], [16].

$$R_{D\text{-}T} \sim \exp\{t_n(m^*_{ox} \cdot E_n)^{0.5} - t_o(m^*_{ox} \cdot E_o)^{0.5}\} \quad (1)$$

where t_n and t_o are the respective widths of sub-oxide regions (in Å) with and without interface nitridation, and E_n and E_o are average conduction band offset energies (in eV). From Fig. 2, $t_n = 3.5$ Å, $t_o = 2.7$ Å, $E_n = 2.7$ eV and $E_o = 1.6$ eV, so that $R_{D\text{-}t} \sim 6$, consistent with the decreases in the calculated J-V curves of Fig. 3. Since the integrand in the WKB integral for D-T includes the interface terms in the same way independent of oxide thickness [15], [16], the same reductions in D-T are expected for $t_{ox\text{-}eq} \sim 1.5$ to 3 nm in agreement with experiment [7], [12]. Additionally, since the WKB tunneling probability is independent of current direction for applied voltages below the onset of F-N-T, $R_{D\text{-}T}$ is the same for substrate and gate injection in this voltage regime consistent with other results not reported in this letter.

An estimate of tunneling current reductions in the F-N-T regime is not as straightforward, since the integrand in the WKB integral for gate injection does not explicitly include the interface region, but does for substrate injection. However, based on estimates of the elecric field in the bulk and interface regions of the dielectric, $R_{F\text{-}N}$, can be estimated using the WKB approximation for tunneling through a trapezoidal barrier [9], [15], [16]. Proceeding in this way, the reduction in devices with nitrided interfaces for a thickness ~5 nm and an applied bias of ~4–6 V is estimated to be 13 ± 3, in agreement with experimental data in [7], [12].

IV. Conclusions

Experimental data have demonstrated that monolayer interface nitridation reduces tunneling currents in the D-T regime by a factor of 8 ± 2 compared to devices with nonnitrided interfaces [7], [11], consistent with calculated J–V curves and (1). These comparisons are based on devices with the same $t_{ox\text{-}eq}$ and flatband voltage. Therefore, decreases in D-T due to interface nitridation must be considered in evaluating the performance of aggressively-scaled devices with O/N stacks and oxynitride alloys [2]–[6], since *interfacial* nitridation can result from nitrogen transport during processing, including post-deposition anneals [3].

The comparisons in Fig. 3 between calculated D-T currents for *ideal abrupt* Si-SiO_2 interfaces, and those with sub-oxide transition regions demonstrate that transition regions must be considered in fitting experimental data to model calculations even for nonnitrided dielectrics. For example, determinations of fit parameters based on ideal interface models can lead to values of tunneling masses and/or band offset energies which are *effective values* due to neglect of the interfacial sub-oxide transition regions.

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