# Ultrathin Oxide–Nitride Gate Dielectric MOSFET's

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***Abstract*— The first ultrathin oxide–nitride (O–N) gate dielectrics with oxide equivalent thickness of less than 2 nm have been deposited and characterized in n-MOSFET's. The O–N gates, deposited by remote plasma-enhanced CVD, demonstrate reduced gate leakage when compared with oxides of equivalent thickness while retaining comparable drive currents.**

## I. Introduction

As the desire for increased ULSI circuit density continues, MOSFET device dimensions will accordingly be scaled down well into the sub-100-nm regime. Coincident with these shrinking channel dimensions is the continued reduction in gate insulator thickness with current projections indicating reductions as low as 1.0 nm in the next 15 years [1]. While ultrathin gate MOSFET's have been realized at 1.5 nm oxide thickness, a major obstacle to overcome is the high level of direct tunneling current through the gate [2]. One possible solution is to incorporate the use of a high permittivity, or high-$k$, film in the gate dielectric. High-$k$ films allow the use of a physically thicker film while acting electrically as a thin dielectric. However, a trade-off exists since the bandgap, or more importantly the barrier height, tends to decrease with increasing dielectric constant [3].

Silicon nitride is an excellent choice for substitution in the gate stack since it provides almost double the dielectric constant of oxide while demonstrating a barrier height of 2.1 eV [4], a level just above the proposed operating voltages of these ultrathin gate devices. However since the silicon-nitride interface has demonstrated poor electrical qualities [5], it is advantageous to incorporate the interfacial qualities of oxide with the advantages of a bulk nitride film. This paper compares the performance of MOSFET's with an ultrathin oxide–nitride (O–N) dielectric and an oxide of approximately equivalent thickness.

## II. Experimental

The ultrathin gates were deposited in a cluster tool system where all gate depositions are completed prior to exposure to atmosphere [6]. All insulator depositions were performed by remote plasma-enhanced chemical vapor deposition (RPECVD) at 400 W, 300 mTorr, and 300 °C substrate temperature. The O–N gate was created by an initial 60-s remote plasma oxidation step using a $He/O_2$ plasma to create the $Si\text{-}SiO_2$ interface followed by remote plasma nitride deposition using a $SiH_4$ and $NH_3$ reaction with energy provided by a He plasma. A 15-s 900 °C vacuum anneal of the nitride layer was performed to further reduce hydrogen concentration in the nitride film [7]. This combination of low-temperature deposition followed by high-temperature annealing provides a high-quality nitride film containing a very low density of electronically active defects [8]. The pure oxide gate was formed by a 30-s remote plasma oxidation step followed by a 10-s remote plasma deposition using $O_2$ and $SiH_4$. Each of the insulators was then capped with 140-nm gate polysilicon deposited rapid thermally at 650 °C.

These experiments were performed on 100-mm CZ wafers with a boron doping density of $2\times 10^{17}/cm^3$. Basic MOSFET fabrication was used to reduce possible post-processing effects and attempt to focus on the gate dielectric itself. Device isolation was created by formation of a 250-nm field oxide followed by patterning of the device active area and etch-back to 10 nm leaving a sacrificial oxide on the active area. Prior to entry into the cluster tool system, the sacrificial oxide was removed in a 3% HF solution. Following gate stack completion, RIE etching using a $Cl_2/O_2$ process was performed to etch the gate of the MOSFET's, and phosphorous disk diffusion was used for simultaneous doping of the gate, source, and drain. The diffusion step included a drive-in step of 875 °C for 60 min. Low-temperature oxide deposition was used for contact isolation, and a Ti/Al metal liftoff procedure was used for final contact to gate, source, and drain. A final forming gas anneal was perfomed at 400 °C.

## III. Results and Discussion

Electrical equivalent oxide thickness was measured by modeling 100 kHz high-frequency CV curves from $1\times 10^{-4}$ $cm^2$ capacitors using a least-squares method to fit the modeled curve to experimental data. The model incorporates both poly-depletion and quantum confinement effects to calculate substrate doping density, oxide thickness, and flatband voltage.

Fig. 1 compares gate injection currents for the O–N stack with a pure oxide. A transition occurs where leakage through the O–N gate becomes greater than the oxide gate at approximately 2 V past the flatband condition. Therefore assuming a standard operating voltage of less than 2 V for these devices, the O–N gate will have reduced tunneling current. It is important to note also that the tunneling current through

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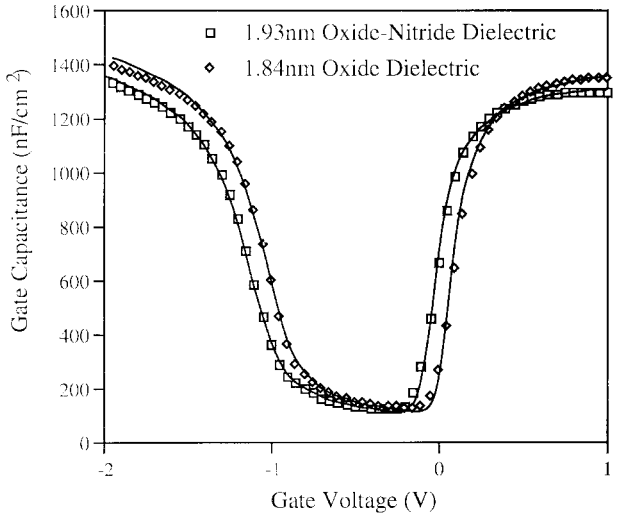


Fig. 1. Current density $J_{ox}$ as a function of oxide electric field, $(V_g - V_{fb})/t_{ox}$, for both ultrathin dielectrics obtained on $2.5 \times 10^{-5}$ cm$^2$ capacitors with p-type Si substrates. Note $t_{ox}$ is electrical equivalent oxide thickness.

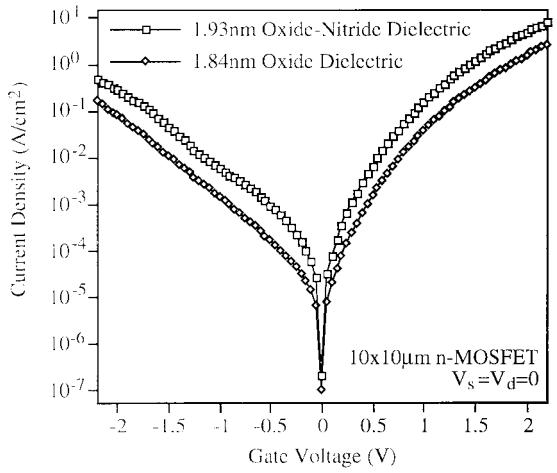


Fig. 2. Current density $J_{ox}$ as a function of oxide electric field, $(V_g - V_{th})/t_{ox}$, for both ultrathin dielectrics obtained on $1 \times 10$ $\mu$m n-MOSFET's with source and drain grounded. Designated $L$ is effective channel length.

the RPECVD oxide compares very well with published data from 1.7-nm thermally grown oxides [9].

Substrate injection on MOSFET's as shown in Fig. 2 also demonstrates reduced tunneling currents through the O–N gate. Here there is no crossover point in the current density plots. The ratio of drain to gate current demonstrates the effectiveness of the O–N gate in a device under test as shown in Fig. 3. Independent of drain voltage, the ratio of $I_d$ to $I_g$ is increased when the O–N gate is used. Note also that only substrate injection is depicted in this figure. At high $V_d$ and low $V_g$, gate injection occurs due to the reversed field across the insulator, but from Fig. 1, lower gate currents are still realized with the O–N gate.

Current drive of the O–N and oxide gate MOSFET's with effective channel lengths of 1 $\mu$m are compared in Fig. 4. Each plot is an average of eight devices distributed throughout a 4 cm$^2$ area on the wafer. Both ultrathin gate devices demonstrate

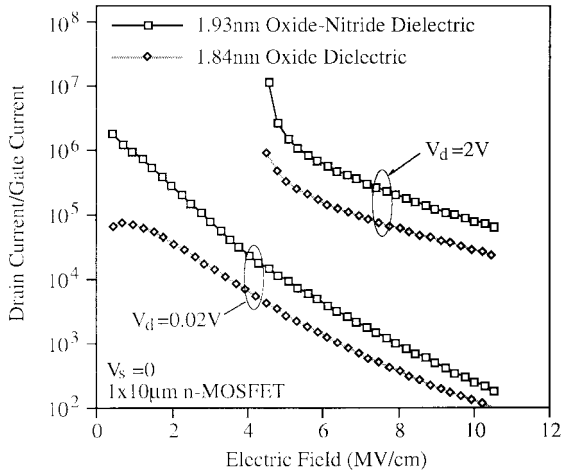


Fig. 3. Ratio of drain to gate current as a function of oxide electric field, $(V_g - V_{th})/t_{ox}$, for both ultrathin dielectrics obtained on $1 \times 10$ $\mu$m n-MOSFET's at drain voltages of 2 V and 20 mV.

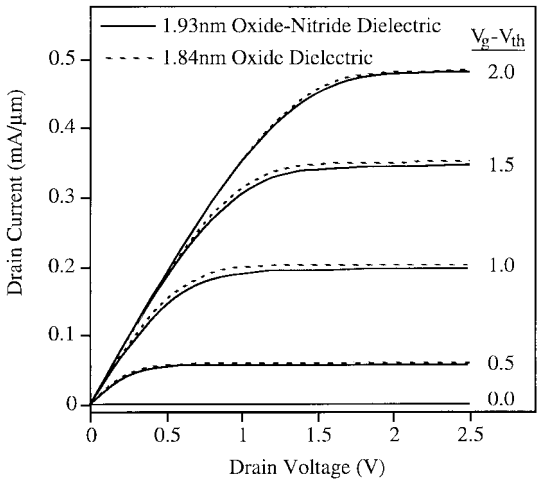


Fig. 4. Drain current versus drain voltage for $1 \times 10$ $\mu$m ultrathin gate n-MOSFET's. Curves are an average of eight devices over a 4-cm$^2$ area.

excellent and essentially equivalent $I_d$–$V_d$ characteristics with the capability to drive currents of approximately 0.18 mA/$\mu$m at a normalized gate voltage of 1 V.

## IV. Conclusion

Ultrathin oxide–nitride gate dielectric MOSFET's with equivalent oxide thickness of 1.8 nm have been fabricated for the first time. All gate depositions were performed by a high-quality RPECVD process in a cluster tool system. MOSFET's with these gates demonstrate equivalent drive currents but with decreased gate leakage when compared to devices with oxides of equivalent thickness.

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