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Baliga

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[54] **METHODS OF FORMING SILICON CARBIDE SEMICONDUCTOR DEVICES HAVING BURIED SILICON CARBIDE CONDUCTION BARRIER LAYERS THEREIN**

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[52] **U.S. Cl.** ..... **437/22**; 437/24; 437/26; 437/41 SH

[58] **Field of Search** ..... 437/22, 24, 26, 437/40 SH, 40 DM, 41 SH, 41 DM, 100; 148/DIG. 148, DIG. 139, DIG. 140

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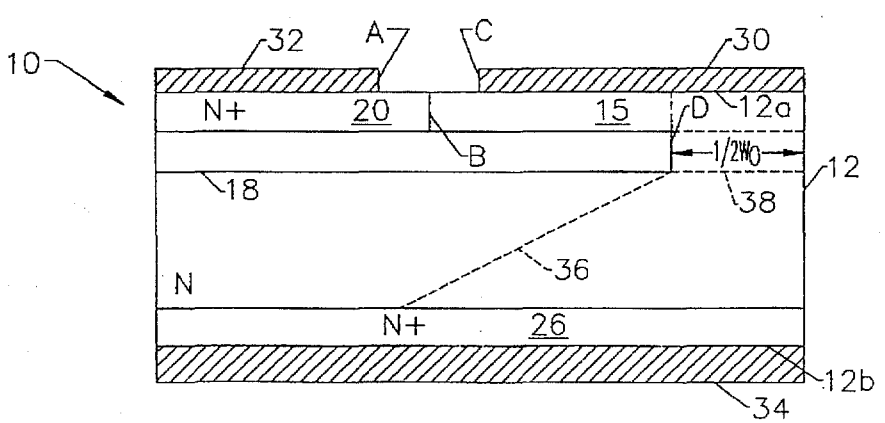
[57] **ABSTRACT**

A silicon carbide semiconductor device includes a silicon carbide substrate, an active layer in the substrate and a silicon carbide buried layer which provides a conduction barrier between the substrate and at least a portion of the active layer. The buried layer is preferably formed by implanting second conductivity type dopants into the substrate so that a P-N junction barrier is provided between the active layer and the substrate. The buried layer may also be formed by implanting electrically inactive ions into the substrate so that a relatively high resistance barrier is provided between the active layer and the substrate. The electrically inactive ions are preferably selected from the group consisting of argon, neon, carbon and silicon, although other ions which are electrically inactive in silicon carbide may be used. The implantation of the electrically inactive ions is designed to cause the formation of a large number of electrically active deep level defects in the buried layer, particularly near the peak of the implant profile which is Gaussian in shape. These steps can be utilized in the formation of a variety of silicon carbide semiconductor devices such as lateral field effect devices and devices having both vertical and lateral active regions which are designed for high power applications. In particular, lateral silicon carbide-on-insulator enhancement and depletion mode field effect transistors (FETs) can be formed in accordance with the present invention. Vertical silicon carbide power MESFET devices can also be formed by incorporating a silicon carbide source region in the active layer at the first face of a silicon carbide substrate and a drain region at the second face and by providing a Schottky barrier gate electrode on the first face.

4 Claims, 3 Drawing Sheets