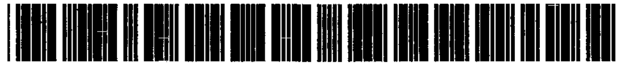

US005637898A

United States Patent [19]

Baliga

[11] **Patent Number: 5,637,898**

[45] **Date of Patent: Jun. 10, 1997**

[54] **VERTICAL FIELD EFFECT TRANSISTORS HAVING IMPROVED BREAKDOWN VOLTAGE CAPABILITY AND LOW ON-STATE RESISTANCE**

[75] Inventor: **Bantval J. Baliga**, Raleigh, N.C.

[73] Assignee: **North Carolina State University**, Raleigh, N.C.

[21] Appl. No.: **577,859**

[22] Filed: **Dec. 22, 1995**

[51] **Int. Cl.**[6] **H01L 29/94**

[52] **U.S. Cl.** **257/330**; 257/331; 257/333; 257/342

[58] **Field of Search** 257/330, 331, 257/333, 342

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,412,297	11/1968	Amlinger	257/330
4,288,801	9/1981	Ronen	257/337
4,893,160	1/1990	Blanchard	257/334
4,903,189	2/1990	Ngo et al.	363/127
4,914,058	4/1990	Blanchard	257/333
5,072,266	12/1991	Bulucea et al.	357/23.4
5,202,750	4/1993	Gough	257/133
5,233,215	8/1993	Baliga	257/490
5,283,201	2/1994	Tsang et al.	437/31
5,298,781	3/1994	Cogan et al.	257/333
5,323,040	6/1994	Baliga	257/332
5,473,176	12/1995	Kakumoto	257/333
5,558,313	9/1996	Hshieh et al.	257/342

FOREIGN PATENT DOCUMENTS

0494597A1 7/1992 European Pat. Off. .

OTHER PUBLICATIONS

Y. Babe, et al., *A Study on a High Blocking Voltage UMOS–FET with a Double Gate Structure*, Proceedings of 1992 International Symposium on Power Semiconductor Devices & ICs, Tokyo, pp. 300–302. No Month.

M. Bhatnagar and B. J. Baliga, *Analysis of Silicon Carbide Power Device Performance*, IEEE, 1991, pp. 176–180. No Month.

T. Syau, et al., *Extended Trench–Gate Power UMOSFET Structure with Ultralow Specific On–Resistance,* Electronics Letters, vol. 28, No. 9, Apr., 1992, pp. 865–867.

(List continued on next page.)

Primary Examiner—Jerome Jackson
Assistant Examiner—John Guay
Attorney, Agent, or Firm—Bell, Seltzer, Park & Gibson

[57] **ABSTRACT**

A power transistor having high breakdown voltage and low on-state resistance includes a vertical field effect transistor in a semiconductor substrate having a plurality of source, channel, drift and drain regions therein. A trench having a bottom in the drift region and opposing sidewalls which extend adjacent the drift, channel and source regions is also provided in the substrate, at a face thereof. The trench preferably includes an insulated gate electrode therein for modulating the conductivity of the channel and drift regions in response to the application of a turn-on gate bias. The insulated gate electrode includes an electrically conductive gate in the trench and an insulating region which lines a sidewall of the trench adjacent the channel and drift regions. The insulating region has a nonuniform cross-sectional area between the trench sidewall and the gate which enhances the forward voltage blocking capability of the transistor by inhibiting the occurrence of high electric field crowding at the bottom of the trench. The thickness of the insulating region is preferably greater than 1500 Å along the portion of the sidewall which extends adjacent the drift region and less than 750 Å along the portion of the sidewall which extends adjacent the channel region. To provide low on-state resistance, the drift region is also nonuniformly doped to have a linearly graded doping profile which decreases from greater than about 1×10^{17} cm^{-3} to less than about 5×10^{-16} cm^{-3} in a direction from the drain region to the channel region.

7 Claims, 6 Drawing Sheets