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[54] **STATIC-INDUCTION TRANSISTORS HAVING HETEROJUNCTION GATES AND METHODS OF FORMING SAME**

[75] Inventors: **Naresh I. Thapar; Praveen Muraleedharan Shenoy; Bantval Jyant Baliga**, all of Raleigh, N.C.

[73] Assignee: **North Carolina State University**, Raleigh, N.C.

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[58] **Field of Search** 257/77, 136, 192, 257/264, 266, 267

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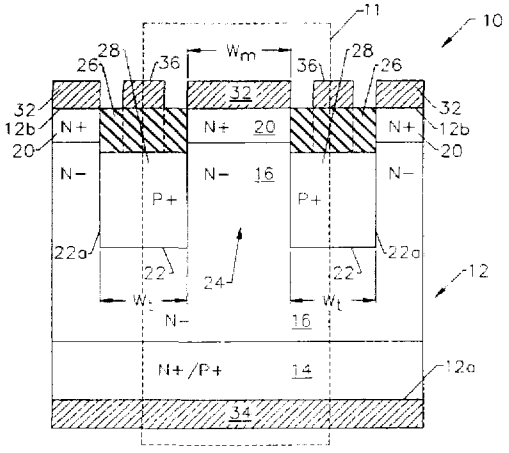
Primary Examiner—Gene M. Munson
Attorney, Agent, or Firm—Myers, Bigel, Sibley & Sajovec

[57] **ABSTRACT**

A semiconductor switching device includes a plurality of adjacent heterojunction-gate static-induction transistor (SIT) unit cells connected in parallel in a monocrystalline silicon carbide substrate having first and second opposing faces, a relatively highly doped silicon carbide drain region adjacent the first face and a relatively highly doped silicon carbide source region adjacent the second face. A relatively lightly doped drift region is also provided in the substrate and extends between the drain region and source region. A plurality of trenches are also provided in the substrate so that sidewalls of the trenches extend adjacent the drift region. Each trench preferably contains a relatively highly doped second conductivity type nonmonocrystalline silicon gate region comprised of a material selected from the group consisting of polycrystalline silicon or amorphous silicon. These gate regions form P-N heterojunctions with the drift region at the sidewalls and bottoms of the trenches. An electrically insulating layer, such as a thermally grown silicon dioxide layer, is also provided on the nonmonocrystalline silicon gate regions in order to electrically insulate the gate regions from metallization on the second face. The use of nonmonocrystalline materials for the gate regions is preferred because the nonmonocrystalline lattice structure of the gate regions provides numerous grain boundaries and other lattice defects which act as scattering sites for electrons. By providing scattering sites, the probability that accelerated electrons will reach the threshold energy to induce avalanche breakdown in the gate regions is reduced and an increase in forward blocking voltage capability is achieved. Hole injection from the P+ polycrystalline silicon gate region into the N-type drift can also be suppressed to significantly improve the switching speed by reducing the amount of stored charge in the drift region.

5 Claims, 4 Drawing Sheets