



US006261929B1

(12) **United States Patent**  
**Gehrke et al.**

(10) **Patent No.:** **US 6,261,929 B1**  
(45) **Date of Patent:** **Jul. 17, 2001**

(54) **METHODS OF FORMING A PLURALITY OF SEMICONDUCTOR LAYERS USING SPACED TRENCH ARRAYS**

(75) Inventors: **Thomas Gehrke**, Carrboro; **Kevin J. Linthicum**, Angier; **Robert F. Davis**, Raleigh, all of NC (US)

(73) Assignee: **North Carolina State University**, Raleigh, NC (US)

(\*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/512,242**

(22) Filed: **Feb. 24, 2000**

(51) **Int. Cl.**<sup>7</sup> ..... **H01L 21/20**; H01L 21/301

(52) **U.S. Cl.** ..... **438/478**; 438/483; 438/462

(58) **Field of Search** ..... 438/478, 479, 438/480, 481, 483, 412, 460, 462, 931; 257/76

(56) **References Cited**

**U.S. PATENT DOCUMENTS**

Re. 34,861	2/1995	Davis et al. ....	437/100
4,127,792	11/1978	Nakata .....	313/500
4,522,661	6/1985	Morrison et al. ....	148/33.2
4,651,407	3/1987	Bencuya .....	29/571
4,865,685	9/1989	Palmour .....	156/643
4,876,210	10/1989	Barnett et al. ....	437/5
4,912,064	3/1990	Kong et al. ....	437/100
4,946,547	8/1990	Palmour et al. ....	156/643
5,122,845	6/1992	Manabe et al. ....	357/17
5,156,995 *	10/1992	Fitzgerald, Jr. et al. ....	438/483
5,389,571	2/1995	Takeuchi et al. ....	437/133
5,397,736	3/1995	Bausier et al. ....	437/92
5,549,747	8/1996	Bozler et al. ....	117/43
5,710,057	1/1998	Kenney .....	437/62
5,760,426	6/1998	Marx et al. ....	257/190
5,786,606	7/1998	Nishio et al. ....	257/103

(List continued on next page.)

**FOREIGN PATENT DOCUMENTS**

2258080 10/1998 (CA) .  
0 551 721 A2 7/1993 (EP) .  
0 852 416 A1 7/1998 (EP) .

(List continued on next page.)

**OTHER PUBLICATIONS**

U.S. application No. 60/109,674, Linthicum et al., filed Nov. 24, 1998.

U.S. application No. 60/109,860, Gehrke et al., filed Nov. 24, 1998.

U.S. application No. 09/441,753, Gehrke et al., filed Nov. 17, 1999.

(List continued on next page.)

*Primary Examiner*—Savitri Mulpuri

(74) *Attorney, Agent, or Firm*—Myers Bigel Sibley & Sajovec

(57) **ABSTRACT**

Methods of forming compound semiconductor layers include the steps of forming a plurality of selective growth regions at spaced locations on a first substrate and then forming a plurality of semiconductor layers at spaced locations on the first substrate by growing a respective semiconductor layer on each of the selective growth regions. The first substrate is then divided into a plurality of second smaller substrates that contain only a respective one of the plurality of semiconductor layers. This dividing step is preferably performed by partitioning (e.g., dicing) the first substrate at the spaces between the selective growth regions. The step of forming a plurality of semiconductor layers preferably comprises growing a respective compound semiconductor layer (e.g., gallium nitride layer) on each of the selective growth regions. The growing step may comprise pendeoepitaxially growing a respective gallium nitride layer on each of the selective growth regions. Each of the selective growth regions is also preferably formed as a respective plurality of trenches that have sidewalls which expose compound semiconductor seeds from which epitaxial growth can take place.

**36 Claims, 5 Drawing Sheets**

