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(54) **PENDEOEPITAXIAL METHODS OF FABRICATING GALLIUM NITRIDE SEMICONDUCTOR LAYERS ON SAPPHIRE SUBSTRATES**

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(58) **Field of Search** 438/479, 481, 438/483, 484, 604

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,127,792 A 11/1978 Nakata 313/500

(List continued on next page.)

FOREIGN PATENT DOCUMENTS

CA 2258080 10/1998

(List continued on next page.)

OTHER PUBLICATIONS

Honda et al., *Selective Area Growth of GaN Microstructures on Patterned (111) and (001) Si Substrates*, 4th European Workshop on GaN, Nottingham, UK, Jul. 2–5, 2000.

(List continued on next page.)

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(57) **ABSTRACT**

More specifically, gallium nitride semiconductor layers may be fabricated by etching an underlying gallium nitride layer on a sapphire substrate, to define at least one post in the underlying gallium nitride layer and at least one trench in the underlying gallium nitride layer. The at least one post includes a gallium nitride top and a gallium nitride sidewall. The at least one trench includes a trench floor. The gallium nitride sidewalls are laterally grown into the at least one trench, to thereby form a gallium nitride semiconductor layer. However, prior to performing the laterally growing step, the sapphire substrate and/or the underlying gallium nitride layer is treated to prevent growth of gallium nitride from the trench floor from interfering with the lateral growth of the gallium nitride sidewalls of the at least one post into the at least one trench. Embodiments of gallium nitride semiconductor structures according to the present invention can include a sapphire substrate and an underlying gallium nitride layer on the sapphire substrate. The underlying gallium nitride layer includes therein at least one post and at least one trench. The at least one post each includes a gallium nitride top and a gallium nitride sidewall. The at least one trench includes a sapphire floor. A lateral gallium nitride layer extends laterally from the gallium nitride sidewall of the at least one post into the at least one trench. In a preferred embodiment, the at least one trench extends into the sapphire substrate such that the at least one post each includes a gallium nitride top, a gallium nitride sidewall and a sapphire sidewall and the at least one trench includes a sapphire floor. The sapphire floor preferably is free of a vertical gallium nitride layer thereon and the sapphire sidewall height to sapphire floor width ratio preferably exceeds about 1/4. A mask may be included on the sapphire floor and an aluminum nitride buffer layer also may be included between the sapphire substrate and the underlying gallium nitride layer. A mask also may be included on the gallium nitride top. The mask on the floor and the mask on the top preferably comprise same material.

35 Claims, 11 Drawing Sheets