ABSTRACT

SARKAR, ANIRBAN. Efficient Power Amplifiers for Millimeter-Wave Beamformers. (Under the direction of Dr. Brian Floyd.)

Wireless communication systems in the millimeter-wave frequency bands have shown the capability to meet higher capacity desired in the future generation of communication systems. One of the challenges in realizing commercial millimeter-wave communication systems is the availability of compact and power-efficient phased-array transceiver integrated circuits in low-cost silicon-based technologies. To enable low-power and compact phased arrays, this work investigates circuit design techniques for high efficiency and high output power millimeter-wave Power Amplifiers (PAs) in low-cost SiGe BiCMOS processes. Further, the efficiency and output power enhancement techniques presented in this work are suitable for high peak-to-average ratio modulation schemes.

Harmonic-tuned continuous class-AB mode PAs are investigated for high peak and back-off power added efficiency (PAE) while eliminating the necessity of short and open resonators. A novel harmonic output matching network architecture consisting of a bandpass filter cascaded with or surrounded by a low pass matching network is proposed for integrated continuous class-AB mode millimeter-wave PAs. A parasitic-aware design technique is introduced to realize compact and low-loss harmonic matching networks with lumped components. This technique demonstrates a method of manipulating the second-harmonic phase of a Chebyshev band-pass filter while maintaining a suitable impedance match at the fundamental. The harmonic-tuned PA shows 4–5% point improvement in peak PAE compared to a traditional LC-tuned PA at 28 GHz. The technique is applied to a 28-GHz PA in SiGe BiCMOS which achieves 15.3-dB gain, 18.6-dBm saturated output power, 15.5-dBm output 1-dB compression point (oP1dB), 35.3% peak PAE, and 11.5% PAE at 6-dB output power back-off (PAE-6dB0).

Efficacy of second-harmonic tuning versus frequency is studied to establish a break-even frequency above which harmonic tuning no longer offers any performance benefit. Harmonic generation capability of the device is studied through constrained load-pull simulations. A second type of
A harmonic matching network is presented which can be realized with microstrip transmission lines and is suitable for higher millimeter-wave frequencies. Simulation results with finite-Q elements show that harmonic tuning improves PAE by 3–5% points from 28 to 43 GHz and about 2–3% points from 43 to 66 GHz and the break-even frequency is established as 68 GHz. Two-stage PAs operating at 28 and 60 GHz were fabricated to demonstrate the effect of harmonic tuning and validate our predictions. A broadband inter-stage match network design technique is also presented for the 60 GHz PA. The 28(60)-GHz PA achieves 30(19)-dB gain, 16.2(13.3)-dBm O\text{P}_{1\text{dB}}, 35.5(25)% peak PAE and 14(9)% PAE\text{,}_6\text{dB}_0\text{.}

After investigating techniques for high peak efficiency single-path millimeter-wave PAs, we explore multi-path PA architectures that can improve the output power or back-off PAE of the PA. Design methodologies for a Doherty PA suitable for a millimeter-wave Doherty beamformer are presented. In particular, choice of multi-stage Doherty architectures, necessity of harmonic matching networks, output combiner choice are investigated for optimum Doherty operation. Bandwidth versus PAE trade-off of harmonic tuning in Doherty PA is demonstrated. Trade-offs in design of the peaking PA and impact on overall Doherty performance are presented. With these design considerations, a 60-GHz Doherty PA is fabricated and characterized. Measurement results demonstrate at least 3–4% point improvement in PAE\text{,}_6\text{dB}_0\text{ over state-of-the-art 60-GHz PAs.}

Transformer-based compact and low-loss combiners are investigated for realizing efficient and high output power millimeter-wave PAs. A simplified and generalized co-design technique for the transformer and the adjoining matching network is presented to minimize the power loss of a series-parallel combiner using an accurate lumped transformer model. Efficacy of this technique is demonstrated with a two-way series two-way parallel power-combined PA which shows greater than 5-dB improvement in output power with only 3–4% point reduction in efficiency compared to the unit PA.
DEDICATION

To my parents.
BIOGRAPHY

Anirban Sarkar was born in Kolkata, India. He received his B. E. degree (Honors) in Electrical Engineering from the National Institute of Technology, Durgapur in 2006. After spending some time in industry, he joined NC State University as a Masters student in Electrical Engineering in 2009. He received the MS degree in Electrical Engineering in 2011 and joined Prof. Floyd's research group at NC State University as a doctoral student. He was a student paper finalist at the SiRF 2014 conference. During the spring of 2015, he was an intern at Samsung Research America. He has served as a reviewer for the IEEE Journal of Solid-State Circuits. His research interests include RF power amplifiers, millimeter-wave and RF integrated circuits, especially, linear and power-efficient transmitters.
ACKNOWLEDGEMENTS

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Most present-day cellular communication systems use carrier frequencies in the 300 MHz to 3.5 GHz range [1, 2]. Also, most of the popular short-range communication systems, such as WiFi, WiMax, Bluetooth and NFC use a carrier frequency below 6 GHz [3]. The spectrum below 6 GHz is crowded and restricts the use of higher bandwidths to increase capacity [4]. Demand for higher data rates can only be fulfilled by increasing capacity. Wireless communication at millimeter-wave carrier frequencies (30-300 GHz) can potentially overcome this limitation. The objective of this work is to investigate circuit techniques that would enable the realization of low-power, high-performance silicon transmitter integrated circuits (ICs) for commercial millimeter-wave communication systems. One of the key challenges in millimeter-wave transmitters is the generation of high-transmit output power with high linearity and high efficiency in low-cost silicon IC technologies. Efficiency and linearity of the millimeter-wave transmitter is mainly dominated by the power amplifier (PA). In this work, three key efficiency enhancement techniques are investigated for millimeter-wave PAs
and successfully demonstrated in hardware as follows: harmonic terminations, Doherty PA, and low-loss power combining.

Two different wireless communication systems operating at center frequencies of 28 GHz and 60 GHz have been considered for demonstration of the proposed PA enhancement techniques. First of these is a fifth-generation cellular network (5G) operating in the frequency band of 27-28.35 GHz, targeting a data rate of about 1 Gbps and a range of around 1 km. The second is a short-range communication system operating in the 57-66 GHz oxygen absorption band targeting a data rate of about 4 Gbps and a range less than 10 m. Brief system aspects and link budgets of these systems are presented in the following sections.

The key enabling technologies for millimeter-wave communication systems are multi-antenna phased arrays. Compared to single-antenna systems, phased arrays can synthesize more directional beams giving higher antenna gain. The higher antenna gain is particularly necessary at millimeter-wave frequencies due to increased path loss. A short discussion of phased-array transmitters is presented in section 1.3 including the trade-off between performance, cost and power consumption. The impact of PA output power and efficiency on the overall system is presented.

In section 1.4 the goals of this work are established based on the system requirements presented in sections 1.1 and 1.2 of this chapter, and the phased array trade-offs presented in section 1.3. A literature survey in section 1.4 discusses state-of-the-art achievements in millimeter-wave PAs and the gaps in current work that are addressed in this dissertation. Section 1.5 summarizes the original contributions of this dissertation.

1.1 5G cellular communication system

Initial proposals for a fifth-generation cellular system (5G) considered several frequency bands at 28 GHz, 38 GHz and 70 GHz [5–7]. Recently, the Federal Communications Commission (FCC) has allocated about 3.85 GHz of licensed spectrum and 7 GHz of unlicensed spectrum for development of 5G systems [8] as shown in Fig. 1.1. Among the allocated bands, the 27.5-28.35 GHz and 38.6-40 GHz bands have been proposed for development of high-capacity, high-throughput small cells for
mobile broadband. A mobile millimeter-wave broadband (MMB) system for 5G communications was presented in [5] and summarized here. One key difference with a traditional cellular architecture is that MMB base stations can be located more closely to each other because they can avoid interference due to the use of narrower beams (Fig. 1.2); thus, a mobile device can be surrounded by a grid of MMB base stations in contrast to a cellular architecture where it has only one or two nearby base stations. This can eliminate the poor link quality at cell edge. The MMB network can also be built to co-exist with the existing 4G system as shown in Fig. 1.2. Although millimeter-wave signals in this frequency band experience little atmospheric absorption, they are attenuated by building materials, foliage, and rain much more than Electromagnetic (EM) waves below 3 GHz frequencies. Thus, the 4G system can serve as a backup and carry important control channels and signals while the MMB network transmits at a high data rate.

The uplink budget of a MMB system is shown below [6]. For a 0.65-Gbps uplink at a distance of 200 km with 1-GHz bandwidth around 28-GHz center frequency, we need 30-dBm Effective Isotropic

![Figure 1.1 Millimeter-wave frequency bands allocated by the FCC for 5G and WiGig.](image-url)
Figure 1.2 Hybrid MMB + 4G architecture [5].
Radiated Power (EIRP) from the transmitter. This is supported by the following table:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Rate</td>
<td>0.65 Gbps</td>
</tr>
<tr>
<td>Center Frequency</td>
<td>28 GHz</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>1 GHz</td>
</tr>
<tr>
<td>SNR at receiver baseband, SNR&lt;sub&gt;RXBB&lt;/sub&gt;</td>
<td>4.7 dB</td>
</tr>
<tr>
<td>Receiver Noise figure, NF&lt;sub&gt;RX&lt;/sub&gt;</td>
<td>5 dB</td>
</tr>
<tr>
<td>Thermal Noise PSD</td>
<td>$-174$ dBm/Hz</td>
</tr>
<tr>
<td>Receiver sensitivity, $P_{RX}$</td>
<td>$SNR_{RXBB} + (\text{Thermal Noise PSD}) + 10 \log_{10}(B) + NF_{RX} = -74$ dBm</td>
</tr>
<tr>
<td>Receiver antenna gain</td>
<td>23 dB</td>
</tr>
<tr>
<td>Link Distance, $R$</td>
<td>250 m</td>
</tr>
<tr>
<td>Free space propagation loss, $L_{\text{free−space}}$</td>
<td>$20 \log_{10}\left(\frac{\lambda}{4\pi R}\right) = 107.4$ dB</td>
</tr>
<tr>
<td>Link margin, $L_{\text{link−margin}}$</td>
<td>20 dB</td>
</tr>
<tr>
<td>Transmitter EIRP, $EIRP_{TX}$</td>
<td>$P_{RX} - G_{RX} + L_{\text{free−space}} + L_{\text{link−margin}} = 30.4$ dBm</td>
</tr>
</tbody>
</table>

1.2 60-GHz Multi-Gigabit-per-second Wireless (IEEE 802.11ad/ WiGiG)

The unlicensed Industrial-Scientific-Medical (ISM) bands in the USA and other countries at 60 GHz are shown in Fig. 1.1 and Fig. 1.3. About 5 to 7 GHz of bandwidth is available in the range of 57–66 GHz with significant overlap between different countries. This band is attractive for short-range multi-Gbps communications due to high oxygen absorption. The IEEE 802.11ad standard has been developed to augment the existing 2.5-GHz and 5-GHz WiFi channels with a high speed 60-GHz multi-Gbps channel for applications involving large data transfers between nearby devices, e.g., high-definition video streaming and large file transfer. Data rates of up to 7 Gbps are possible using OFDM with different modulation schemes [9]. Recently, the FCC has allocated an additional 7 GHz
A sample uplink/downlink budget for the 60-GHz WiGig system is shown below:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Rate</td>
<td>10 Gbps</td>
</tr>
<tr>
<td>Center Frequency</td>
<td>62 GHz</td>
</tr>
<tr>
<td>Bandwidth, $B$</td>
<td>5 GHz</td>
</tr>
<tr>
<td>SNR at receiver baseband, $\text{SNR}_{RXBB}$</td>
<td>17 dB</td>
</tr>
<tr>
<td>Receiver Noise figure, $\text{NF}_{RX}$</td>
<td>7 dB</td>
</tr>
<tr>
<td>Thermal Noise PSD</td>
<td>$-174 \text{ dBm/Hz}$</td>
</tr>
<tr>
<td>Receiver sensitivity, $P_{RX} = \text{SNR}<em>{RXBB} + (\text{Thermal Noise PSD}) + 10\log</em>{10}(B) + \text{NF}_{RX} = -53 \text{ dBm}$</td>
<td></td>
</tr>
<tr>
<td>Receiver antenna gain, $G_{RX}$</td>
<td>20 dB</td>
</tr>
<tr>
<td>Link Distance, $R$</td>
<td>10 m</td>
</tr>
<tr>
<td>Free space propagation loss, $L_{\text{free-space}} = 20\log_{10}\left(\frac{\lambda}{4\pi R}\right)= 81.4 \text{ dB}$</td>
<td></td>
</tr>
<tr>
<td>Link margin, $L_{\text{link-margin}}$</td>
<td>20 dB</td>
</tr>
<tr>
<td>Transmitter EIRP, $EIRP_{TX} = P_{RX} - G_{RX} + L_{\text{free-space}} + L_{\text{link-margin}} = 28.4 \text{ dBm}$</td>
<td></td>
</tr>
</tbody>
</table>
1.3 Beamforming at millimeter-wave

Friis transmission equation for received power states that

\[
P_r = P_t \left( \frac{\lambda}{4\pi R} \right)^2 G_t G_r, \tag{1.1}
\]

where \( P_t \) is the transmitted power, \( \lambda \) is the wavelength, \( R \) is link distance, \( G_t \) is the transmit antenna gain and \( G_r \) is the receiver antenna gain. It could be observed that millimeter-wave radiation incurs more attenuation compared to low frequency radio signals for the same transmit and receive antenna gains due to smaller wavelength and hence smaller aperture. In addition, they are attenuated much more than low-frequency signals due to obstacles like walls, foliage and rain. However, the smaller wavelength also implies smaller passive elements, allowing smaller chip size or integration of larger systems, such as a phased array. Two major benefits can be obtained by using multiple transmitter elements: a) higher output power by using over the air power combining and b) higher antenna gain by synthesizing more directional (narrower beamwidth) radiation patterns using phased arrays termed as beamforming. As shown in Fig. 1.4, in a phased-array transmitter the RF signal fed to each antenna is phase shifted by a desired angle. This phase shift can be generated at baseband, an intermediate frequency (IF) or at RF. By changing the phase shift between the elements, the direction of the main lobe of the radiation pattern can be changed or the beam can be steered. This is beneficial for communication with mobile terminals. An expression for the full array response is derived below for a linear array and some radiation patterns demonstrating beam-steering are shown in Fig. 1.5 [10].
Figure 1.4 Four-element phased-array block diagram.

Antenna position vector for the n-th element of the array, \( \mathbf{r}_n = n d_x \hat{x} \)

Element vector, \( A_n(\theta) = S_{el}(\theta)a_n e^{-j\alpha_n} \)

Wave vector in the \( xz \) plane, \( \mathbf{k} = \frac{2\pi}{\lambda}(\sin \theta \hat{x} + \cos \theta \hat{z}) \)

Element response, \( S_n(\theta) = A_n(\theta)e^{j(\mathbf{k} \cdot \mathbf{r}_n)} \)

Array response, \( S(\theta) = S_{el}(\theta) \sum_{n=0}^{N-1} a_n e^{j(nkd \sin \theta \alpha_n)} \)

Array Factor, \( AF(\theta) = \sum_{n=0}^{N-1} a_n e^{j(nkd \sin \theta \alpha_n)} \)

where \( \hat{x} \) is the unit vector along the x coordinate (Fig. 1.4),

\( a_n \) is the amplitude weight for the n-th element of the array,

\( \alpha_n \) is the phase of the the n-th element of the array, and

\( S_{el}(\theta) \) is the element radiation pattern.
The half-power beamwidth of a phased array with $N$ elements can be shown to be $1/N$ times the half-power beamwidth of a single element; hence, the gain of the array would be $NG_{el}$ where $G_{el}$ is the gain of a single element [11]. The total output power of the array would be $NP_{el}$ where $P_{el}$ is the output power of a single element. The EIRP of the array is given by [12]

$$\text{EIRP} = (NG_{el})(NP_{el}). \quad (1.2)$$

The efficiency of the array can be defined as $\eta = \frac{(NP_{el})}{P_{DC}}$, so the dc power consumption of the array can be related to EIRP as

$$P_{DC} = \frac{\text{EIRP}}{\eta NG_{el}}. \quad (1.3)$$

Based on 1.3, a plot demonstrating key trade-offs in a phased array can be generated as shown in Fig. 1.6. If the number of array elements is fixed by the die size and cost constraints, then for a given EIRP, an improvement in front-end efficiency would reduce the dc power consumption of the array. On the other hand, if the dc power consumption is constrained by battery life and cooling requirements, an improvement in front-end efficiency would reduce the number of elements in the array.
1.4 Literature Survey and Research Goals

The discussion in sections 1.1 and 1.2 reveal that 5G and WiGig systems need an EIRP of about 30 dBm owing to high path loss and smaller receive apertures. This is quite a challenging task for silicon ICs given that 4G-LTE transmitters operating at frequencies less than 3.5 GHz have an EIRP specification of 23 dBm\cite{13}. Of course, the use of phased arrays as discussed in section 1.3 relaxes the output power requirement per element. However, as we will show in this section, the desired output power per element and the EIRP requirement for millimeter-wave systems has not been met with existing PA and transmitter techniques with both high efficiency and linearity.

For higher spectral efficiency, 4G-LTE and WiFi systems use high peak-to-mean-envelope-power-ratio (PMEPR) modulation schemes like orthogonal frequency division Multiplex (OFDM). To transmit the signal without distortion, the PA needs to operate with high linearity. Fig. 1.7 shows a typical gain and output power plot of a PA versus input power, with a superimposed normal distribution curve. The normal distribution curve represents the amplitude distribution of symbols.
Figure 1.7 Typical compression characteristic of a PA with a superimposed Normal distribution.

in a high PMEPR modulation scheme. We can observe that for low distortion we need to back-off from the high output power region where the gain is highly compressed. Typically, OFDM waveforms with 1024 sub-carriers have 10 to 12-dB PMEPR [14]. With the help of mitigation schemes presented in [15], the PMEPR could be reduced to 6–7 dB; hence, in this work, we consider 6–7 dB output power back-off from 1-dB gain compression as the point where we should meet the EIRP requirements.

Based on the 5G system link budget presented in section 1.1, the requirements for a 28-GHz beamformer element in an 8-element phased array can be derived as follows:
Transmitter EIRP, $EIRP_{TX} = 30 \text{ dBm}$

Single element antenna gain, $G_{el} = 3 \text{ dB}$

Number of antenna elements, $N = 8$

Output power per element, $P_{el} = EIRP_{TX} - 10 \log_{10}(N^2) - G_{el} = 9 \text{ dBm}$

For linearity we assume, output power per element at 6-dB-back-off = $P_{el} = 9 \text{ dBm} = 8 \text{ mW}$

Beamformer element output power at 1-dB compression = $oP_{1dB} = 15 \text{ dBm} = 31.6 \text{ mW}$

To limit the power consumption of the array to 600 mW at 6-dB-back-off, dc power consumption per element, $P_{DC-el} = 75 \text{ mW}$

Efficiency of the beamformer element at 6-dB-back-off = 10.7%

Similarly, the requirements for a 60-GHz beamformer element in an 8-element phased array based on the WiGig link budget presented in section 1.1 can be derived as:

Transmitter EIRP, $EIRP_{TX} = 28.4 \text{ dBm}$

Single element antenna gain, $G_{el} = 3 \text{ dB}$

Number of antenna elements, $N = 8$

Output power per element, $P_{el} = EIRP_{TX} - 10 \log_{10}(N^2) - G_{el} = 7.3 \text{ dBm}$

For linearity we assume, output power per element at 6-dB-back-off = $P_{el} = 7.3 \text{ dBm} = 5.3 \text{ mW}$

Beamformer element output power at 1-dB compression = $oP_{1dB} = 13.3 \text{ dBm} = 21.4 \text{ mW}$

To limit the power consumption of the array to 500 mW at 6-dB-back-off, dc power consumption per element, $P_{DC-el} = 62.5 \text{ mW}$

Efficiency of the beamformer element at 6-dB-back-off = 8.5%
Table 1.1 Si based IC technologies with their peak $f_T$ and $f_{\text{max}}$

<table>
<thead>
<tr>
<th>Technology</th>
<th>$f_T$ (GHz)</th>
<th>$f_{\text{max}}$ (GHz)</th>
<th>REF</th>
</tr>
</thead>
<tbody>
<tr>
<td>IBM 8HP 130-nm SiGe</td>
<td>200</td>
<td>250</td>
<td>[16]</td>
</tr>
<tr>
<td>IBM 8XP 130-nm SiGe</td>
<td>260</td>
<td>320</td>
<td>[17]</td>
</tr>
<tr>
<td>IBM 9HP 90-nm SiGe</td>
<td>300</td>
<td>450</td>
<td>[18]</td>
</tr>
<tr>
<td>90nm bulk CMOS</td>
<td>105</td>
<td>150</td>
<td>[19]</td>
</tr>
<tr>
<td>65nm bulk CMOS</td>
<td>170</td>
<td>240</td>
<td>[20]</td>
</tr>
<tr>
<td>45nm CMOS SOI</td>
<td>250</td>
<td>250</td>
<td>[21]</td>
</tr>
<tr>
<td>40nm bulk CMOS</td>
<td>-</td>
<td>300</td>
<td>[22]</td>
</tr>
</tbody>
</table>

The $\text{oP}_{1\text{dB}}$ requirements of the PA is same as that of the full beamformer element whereas the PAE at 6-dB-back-off needs to be approximately 3-4% points higher than the beamformer element to account for the power consumption of active phase shifters or variable gain amplifiers in the beamformer element. As we shall see in the subsequent literature survey, these goals have not been met by existing millimeter-wave PAs. As a result, compact power-efficient phased array transmitters have not been realized for 5G and WiGig systems.

1.4.1 Survey of Silicon millimeter-wave PAs

Integrated phased arrays in silicon enable low cost and the potential for a mass market for millimeter-wave communication systems. Table 1.1 shows the existing silicon technologies, both CMOS and SiGe HBT with their peak transit frequencies ($f_T$) and peak oscillation frequencies ($f_{\text{max}}$). The $f_T$ and $f_{\text{max}}$ values suggest reasonable gain at 28-GHz and 60-GHz frequencies; however, for PAs power, linearity and efficiency are more important metrics. Diminishing supply voltages, substrate losses, higher passive losses, device non-linearities and device reliability issues make millimeter-wave PA design a challenging task. In this section, we survey the published millimeter-wave PA results in bulk CMOS, SOI CMOS and SiGe technologies.

The majority of millimeter-wave PAs published at Ka, Q and V-band [23–55] operate in class-AB mode to achieve high linearity and efficiency. One key point that has not been studied in these
works is the impact of harmonic terminations on the performance of class-AB PAs. Ideal class-AB operation requires short impedance terminations at second and higher harmonics. It appears that in existing work, it has been implicitly assumed that the harmonic component would be small enough to not impact performance. Further, continuous class-AB modes [56, 57] which can operate with capacitive second-harmonic terminations have not been utilized in millimeter-wave PAs. Recently, published literature in board-level RF PAs also show that continuous class-AB mode PAs can not only match class-AB PAs at back-off but also exceed their performance at high output power levels [58].

Mortazavi has demonstrated high performance class-F and inverse class-F PAs at 28 and 38 GHz frequencies [59–61]. However, class-F/ inverse class-F PA theory tells us that high efficiency could be achieved only near saturated output power levels when third-harmonic components in the device voltage or current waveforms are significant. While linearity data is not available in [59–61], it is expected that one would need some pre-distortion to operate the PA near saturated power levels.

Class-E like PAs have also been demonstrated at Q and V bands by several authors [21, 62–68]. Although class-E operation is difficult to achieve at millimeter-wave frequencies due to the switching speed of the transistor, some benefits could be observed as mentioned by the authors in [21, 62] with class-E like waveforms. However, the usage of class-E PA with high PMEPR modulation schemes needs complicated pre-distortion techniques or more involved transmitter system design such as outphasing or RF Digital-to-Analog converters (RF-DAC). It is not clear at present if these techniques can be incorporated into a millimeter-wave beamformer. Further, class-E PAs have low gain per stage which ultimately requires higher gain in preceding stages, degrading the system’s power efficiency.

We also find a few works on improving the back-off efficiency using Doherty technique at millimeter-wave frequencies. In [23] an active phase shifter is used to compensate for phase shifts in carrier and peaking PA paths in a Doherty PA, whereas in [69] an ultra-compact Doherty structure is realized using a series combiner. However, in both of these works, significant improvement in back-off PAE has not been demonstrated as compared to Class-AB PAs.

Finally, there has been significant effort in improving the output power of millimeter-wave
PAs using a variety of power combining techniques. These include hybrid combiners [65], parallel combiners [41, 42, 45, 47, 50], transformer-based series [32, 36, 38, 39, 46, 51, 70] and series-parallel combiners [43, 44, 54]. Hybrid combiners and parallel combiners are area-inefficient and ill-suited for beamformers. Transformer-based series-parallel combiners are compact and could reduce the impedance transformation ratio if the number of series and parallel stages are chosen properly. Several series-parallel power combined PAs have been demonstrated at millimeter-wave; however, a generalized design technique which does not rely on full 3-D EM simulations has not been presented for the series-parallel combiner. The work in [70] demonstrated a method to develop lumped or coupled-line model for a differential transformer combiner but this method has not been adapted for multi-way series and parallel combiners that use transformers. Furthermore, power combined PAs mostly show degraded efficiency compared to single-path PAs. In particular, a 6-dB-backoff-PAE greater than 10% for $\text{oP}_{1\text{dB}}$ greater than 20 dBm has not been demonstrated for millimeter-wave PAs. Thus, existing power combined PA solutions are not capable of reducing phased array size for a given EIRP without a big penalty in power consumption.

A scatter plot of $P_{\text{sat}}$ and peak PAE of CMOS and SiGe PAs at 60 GHz is shown in Fig. 1.8. We observe that most of these have lower than 20% peak PAE. Recently, a few designs have shown a good improvement with up to 30% PAE; however, the back-off PAEs of 60 GHz PAs still remain significantly lower than 10% as shown in Fig. 1.9. Similarly, scatter plots of $P_{\text{sat}}$ and peak PAE of Ka and Q band PAs at 28 GHz shown in Fig. 1.10 reveal that only a few designs have achieved greater than 35% peak PAE or greater than 20-dBm output power. Also, $\text{oP}_{1\text{dB}}$ and back-off PAE plots in Fig. 1.11 reveal that most of the PAs have lower than 10% efficiency at 6-dB-back-off. Furthermore, only a few designs have shown greater than 20-dBm $\text{oP}_{1\text{dB}}$ but not with good efficiency. Thus, new architectures and design techniques are needed to allow improved PAE and output power for linear millimeter-wave PAs.
Figure 1.8 $P_{\text{sat}}$ and PAE of state-of-the-art CMOS (red) and SiGe (blue) 60-GHz PAs.

Figure 1.9 $oP_{1\text{dB}}$ and PAE at 6-dB back-off of state-of-the-art CMOS (red) and SiGe (blue) 60-GHz PAs.
Figure 1.10 $P_{\text{sat}}$ and PAE of state-of-the-art CMOS (red) and SiGe (blue) 28-GHz PAs.

Figure 1.11 $oP_{1\text{dB}}$ and PAE at 6-dB back-off of state-of-the-art CMOS (red) and SiGe (blue) 28-GHz PAs.
1.5 Contributions of this work

The objective of this work is to investigate peak and back-off efficiency enhancement techniques for millimeter-wave PAs to be used in linear phased-array transmitters. We evaluate the effectiveness of second-harmonic control on PAE in continuous class-AB mode PAs through constrained load-pull simulations at 28 GHz. For the first time, the continuous class-AB mode is adopted for a high peak PAE and good linearity at millimeter-wave frequencies. A novel harmonic matching network architecture suitable for realizing fundamental and second harmonic impedances for a millimeter-wave continuous-mode PA consisting of a bandpass filter cascaded with or surrounded by a low pass matching network is proposed. This technique uses a Chebyshev bandpass filter with tunable second harmonic phase and well-matched fundamental. The design technique is further adapted to include the effect of parasitic components of passive elements using Norton transformations. A thorough comparison is performed between a classical class-AB PA, an LC-tuned PA, and a harmonic-tuned continuous class-AB mode PA. The design techniques are demonstrated with an integrated circuit implementation of a 28-GHz PA in 130-nm SiGe BiCMOS technology. The PA achieves 15-dB gain, 18-dBm $P_{\text{sat}}$, 15.5-dBm $O_{1\text{dB}}$, 35% peak PAE and 11.5% 6-dB back-off PAE. The peak and back-off PAEs are among the highest reported PAEs for silicon-based technologies. Excellent linearity is demonstrated with less than 2 degree AM-PM distortion up to 1-dB compression and less than $-33$ dBc third-order intermodulation product at 6-dB back-off.

Having demonstrated the utility of harmonic terminations at 28 GHz, we next study the efficacy of this technique versus frequency to establish the frequency limits up to which harmonic tuning contributes to PAE improvement. Generation of harmonic components versus frequency by active devices is studied with the help of constrained load-pull simulations. A design methodology for a second kind of harmonic matching network using microstrip transmission lines is introduced. To evaluate the efficacy of harmonic tuning, and its dependency on frequency of operation and passive loss, we evaluate harmonic-tuned continuous from 28 GHz to 78GHz and compare them to LC-tuned PAs which achieve only fundamental match using real passive components. This allows us
to estimate a break-even frequency at which the harmonic tuned PA provides no additional benefit over the LC-tuned PA. This frequency is approximately 70 GHz for SiGe 8HP technology. To reinforce the result of these simulation studies, two stage integrated PAs are designed and fabricated at 28 GHz and 60 GHz. A broadband inter-stage match design technique is also presented for the 60 GHz PA. Measurement results of the 28 GHz PA show 30-dB gain, 17.5-dBm $P_{sat}$, 16-dBm $O_{1dB}$, 35.3% peak PAE and 14% 6-dB back-off PAE. Measurement results of the 60 GHz PA show 20-dB gain, greater than 12GHz 3-dB bandwidth, 15.5-dBm $P_{sat}$, 13.8-dBm $O_{1dB}$, 25% peak PAE and 9% 6-dB back-off PAE. The back-off PAEs are one of the highest demonstrated to date.

Having identified architectures and design techniques to realize unit PAs of high efficiency and good linearity, we next study efficient combining techniques which can increase output power and/or increase back-off efficiency. The key design choices and trade-offs in a millimeter-wave Doherty PA are first investigated. In particular, few if any millimeter-wave Doherty PAs have demonstrated compelling performance. We have studied whether these are due to technology limits, poor execution, and/or poor unit amplifiers. Design techniques studied include multi-stage architecture choices, benefits and limitations of harmonic tuning in the carrier PA, trade-offs in peaking PA design, and output combiner choice. The effectiveness of these design choices are demonstrated with the integrated circuit implementation of a 60-GHz Doherty PA. Measurement results of the Doherty PA demonstrates a 18-dB gain, 17.5-dBm $O_{1dB}$, 23% peak PAE and 13.8% 6-dB-back-off PAE. The 6-dB-back-off PAE exceeds that of recently published PAs by 3-4% points.

Finally, a simplified and generalized design techniques for series-parallel power combiners based on a lumped transformer model is presented. Given an arbitrary impedance, we demonstrate a technique for co-designing the transformer with adjoining matching elements for minimum insertion loss. This technique enables the selection of the number of series and parallel combining stages, combiner dimensions and parasitic element values for minimum insertion loss. These techniques are applied for optimum design of a four-way power combined PA. Integrated circuit implementation of a two-stage 28 GHz two-way series two-way parallel power combined PA is presented to demonstrate the efficacy of these techniques. Measurement results demonstrate 27-dB
gain, 23.2-dBm $\text{OP}_{1\text{dB}}$, 32.7% peak PAE and 15% 6-dB-back-off PAE at 28 GHz. For the first time, greater than 20-dBm $\text{OP}_{1\text{dB}}$ has been achieved with greater than 10% 6-dB back-off PAE which would enable smaller and power-efficient phased arrays suitable for 5G mobile transmitters.
2.1 Introduction

In this chapter a 28-GHz harmonic-tuned PA operating in continuous class-AB mode is presented. After a brief review of continuous class-AB mode theory, the efficacy of second harmonic tuning is studied with constrained load pull simulations. A parasitic-aware design technique for the output network realized as a band-pass filter cascaded with or surrounded by a lowpass matching network is presented. This technique demonstrates a method of manipulating the second-harmonic phase
of a Chebyshev band-pass filter while maintaining a suitable impedance match at the fundamental. Thorough comparison of the continuous class-AB mode PA with a classical class-AB PA and a LC-tuned PA is presented to evaluate the efficiency enhancement capability of second-harmonic tuning. To verify the efficiency enhancement capability of second harmonic in continuous class-AB mode operation, a 28-GHz PA is fabricated in SiGe BiCMOS which achieves 15.3-dB gain, 18.6-dBm saturated output power, 15.5-dBm output 1-dB compression point, and 35.3% peak PAE in measurements. When backed off 6 dB from 1-dB compression, the PA achieves 11.5% PAE with a third-order intermodulation product of -33.7 dBC.

Mobile millimeter-wave (mm-wave) broadband systems at 28 GHz have the potential to support high-throughput fifth-generation (5G) cellular networks [5–7]. Based on link budgets presented in [5] and [6], the handset’s up-link transmitter needs moderate beamforming capabilities with a four- to eight-element phased array. Specifically, as shown in [6], the receiver sensitivity ($P_R$) for a data rate of 0.65 Gb/s is estimated to be $-74$ dBm. To achieve a 20-dB link margin (LM) at a 200-m distance ($D$), the effective isotropic radiated power (EIRP) needed at the mobile transmitter’s output is about 30 dBm, given by

$$EIRP = P_R - G_{RX} + 20 \log_{10} \left( \frac{4\pi D}{\lambda} \right) + LM$$

(2.1)

where $G_{RX}$ is the antenna gain of the basestation receiver, assumed here to be 23 dB (~100 elements, each with 3-dBi unit antennas). This EIRP can be achieved at the handset using an eight-element phased array ($N = 8$) with 9-dBm output power per element ($P_{el} = EIRP - 20 \log_{10} (N) - G_{TX}$) and unit antennas having 3-dBi gain ($G_{TX}$). Orthogonal frequency-division-multiplexing (OFDM) schemes used in fourth-generation cellular systems can have 10-dB peak-to-mean-envelope power ratio (PMEPR) for 1024 sub-carriers[14], and we assume 5G systems will be similar. Techniques proposed in [15] can reduce the OFDM waveform PMEPR to 6–7 dB at the cost of implementation complexity, bandwidth, and/or bit-error-rate degradation. Assuming a 6-dB back-off for our design, the 1-dB compressed output power ($oP_{1dB}$) per element should therefore be greater than 15 dBm for an

1Assumes signal-to-noise ratio of 4.7 dB, receiver noise figure of 5 dB, and 1-GHz receiver bandwidth.
eight-element array\(^2\).

The handset’s phased-array transmitter needs to be power efficient to maximize battery life. For example, to limit the eight-element phased-array front-end power consumption to 0.6 W, each transmitter element needs to have greater than 10.7% power-added efficiency (PAE) at 6-dB back off. Improving the power amplifier (PA) efficiency at power levels ranging from back off to 1-dB compression point (\(P_{1dB}\)) is thus of extreme importance.

Harmonic impedance terminations can be used to improve the PA efficiency through the shaping of the voltage and/or current waveforms at the output of the device. These harmonic terminations are used in high-efficiency PA modes, including Class-B, Class-J, Class-E, and Class-F [71]. A literature survey of mm-wave PAs at Ka, Q, and V bands [23–29, 59–64, 66] reveals that most of these PAs operate in Class-AB mode, with a few Class-E and Class-F designs. With the exception of the Class-F PAs in [59–61], little information is found on the design methods for harmonic output-matching networks.

Recently, the continuous Class-B mode has been formalized, wherein a continuum of harmonic terminations can be used to provide for high efficiency, high linearity, and broadband operation [56, 57, 71–74]. Class-J and Class-B represent points along this continuum, and other points along this continuum can also be used to achieve high performance. The Class-F and inverse Class-F modes have also been extended to continuous modes that allows reactive terminations for second and/or third harmonic [56, 75]. However, as in traditional Class-F, we need to operate the PA in saturation and allow the voltage to swing into the knee region to generate a significant third-harmonic component of current or voltage. For our 5G application, operation at back-off and high linearity are essential; hence, we prefer continuous Class-B (or Class-AB).

To the authors’ knowledge, a design method for a harmonic output matching network suitable for integrated mm-wave PAs operating along the Class-B/J continuum has not been described. In this work, we present such a method and adapt it to accommodate parasitics of on-chip passive components. We first review the continuous mode in section II, modified for Class-AB. A har-

\(^2\)The per-element \(P_{1dB}\) would increase to 21 dBm for a 4-element array.
monic matching network consisting of a Chebyshev bandpass filter cascaded or subsumed within a fundamental-frequency matching network is then presented in section III. We benchmark our approach in section IV through a simulation study between classical Class-AB, two element LC-tuned, and continuous Class-AB PAs. Finally, we validate our approach in section V through the realization of a fully-integrated 28-GHz harmonic-tuned PA in 130-nm GlobalFoundries SiGe BiCMOS 8HP technology which achieves 35.3% peak PAE and 18.6-dBm saturated output power, with 11.5% PAE at 6-dB back off from a 15.5-dBm OP1dB. This PA was first reported in [76] and classified as Class-J; but, as will be shown, the PA is better classified as operating along a Class-AB continuum.

2.2 Continuous Class-AB Power Amplifier

The continuous Class-B mode PA was introduced in [56], and refers to the continuum of harmonic terminations which can be leveraged to achieve wideband operation. In this work, we focus on the continuous Class-AB mode design, rather than continuous Class-B described in [56], as Class-AB provides higher gain which is useful for silicon mm-wave PAs. The current and voltage waveforms
for continuous Class-AB mode can be written in terms of their harmonic components as

$$I(t) = I_{DC} + I_1 \cos(\omega t) + I_2 \cos(2\omega t) + \sum_{r=3}^{\infty} I_r \cos(r\omega t),$$  \hspace{1cm} (2.2)$$

$$V(t) = V_{DC} - V_1(\cos(\omega t) - \beta \sin(\omega t) + \frac{\beta}{2} \sin(2\omega t)), \hspace{1cm} (2.3)$$

where $I_r$ is the amplitude of the $r^{th}$ harmonic component of current. Fundamental voltage amplitude, $V_1$, equals $V_{DC} - V_K$, where $V_K$ is the knee voltage of the transistor. By varying the parameter $\beta$ from $-1$ to $1$, a series of waveforms can be generated which theoretically have the same output power, efficiency, and linearity as the classical Class-AB PA ($\beta=0$).

The second harmonic current, $I_2$, is a function of the conduction angle ($\theta$), and can be shown to be [71, Ch. 3, p. 41]

$$I_2 = \frac{4}{3} \frac{\sin^3\left(\frac{\theta}{2}\right)}{(\theta - \sin(\theta))} I_1. \hspace{1cm} (2.4)$$

Using this relationship, the fundamental-frequency and second-harmonic load impedances, $Z_1$ and $Z_2$ respectively, are given as

$$Z_1 = R_{opt}(1 + j\beta), \hspace{1cm} (2.5)$$

$$Z_2 = -j\frac{3}{8}R_{opt}\frac{(\theta - \sin(\theta))}{\sin^3\left(\frac{\theta}{2}\right)} - \beta, \hspace{1cm} (2.6)$$

where $R_{opt} = V_1/I_1$ is the optimum fundamental resistance for the classical Class-AB PA.

As evident in (2.3), the continuous Class-AB mode does result in higher voltage swing at the device; hence, devices with higher breakdown voltage are preferred. The higher voltage swing is handled in SiGe technology through the use of cascode amplifier structures, since these are limited by the NPN $BV_{CEO}$ (equal to 6 V in SiGe 8HP), rather than $BV_{CEO}$ (equal to 1.8 V in SiGe 8HP).

The cascode PA used in this work is designed to meet the output power requirements for our 28-GHz 5G application. The initial schematic is shown in Fig. 2.1. To achieve a minimum of 15-dB gain with high efficiency, the cascode amplifier is biased with a current density of 0.5 mA/$\mu$m with base voltages of $V_{bias1} = 0.85$ V and $V_{bias2} = 1.7$ V for the bottom (Q_1) and top (Q_2) devices, respectively.
The knee voltage $V_K$ for the cascode amplifier is approximately 0.9 V and the supply voltage is set to 3.6 V. For $\beta = 0$, these set the RF voltage amplitude ($V_{RF}$) to 2.7 V. With this supply voltage and $Q_2$ base voltage, the range of $\beta$ which can be supported without entering breakdown is $|\beta| < 0.67$, corresponding to a peak collector voltage less than 7.7 V and a peak collector-base voltage less than 6 V.

The current amplitude ($I_I$) is set to be $\sim 37$ mA, dictated by a 17-dBm output power target to provide margin over our system requirement. The calculated quiescent current is 19 mA for a $1.25\pi$ radian conduction angle. Based on this, we choose an emitter length of four 10-$\mu$m stripes in parallel to achieve quiescent current density of 0.5-mA/\mu m. With our values of voltage and current amplitudes, the calculated optimum fundamental impedance is $R_{opt} = V_{i}/I_{1} = 72$ $\Omega$. A load-pull simulation of the ideal Class-AB mode ($\beta = 0$) shows that the optimum fundamental impedance for maximum PAE is 65 $\Omega$ which is close to the calculated load-line value. With the device size and operating current set, we then impedance match the input using a $\Pi$-network topology, shown in Fig. 2.1.

Although we could use a larger device size to set $R_{opt}$ close to 50 $\Omega$, we choose not to do so for a few reasons. First, the increased capacitance at the PA input and output would result in reduced bandwidth. Second, for devices with a large number of fingers, unequal current and temperature profiles across the device can degrade performance [77].

Before beginning to design an output matching network which can provide the necessary harmonic impedances described in (2.5) and (2.6), we check our network assumption by performing a harmonic load pull within the simulator. This simulation will account for the non-linearities of the device. These non-idealities make it difficult to obtain a full analytic solution for optimum harmonic impedances, as described in [71]. Our simulation uses the HiCUM model for SiGe 8HP. Previous results from the authors have validated the accuracy of the model for fundamental-frequency terminations; however, measurement validation of the second and third harmonics cannot be performed at this time due to equipment limitations.

The harmonic load-pull simulation set up is shown in Fig. 2.1. A bias-tee connects $Q_2$'s collector
to the output through $C_1$ and to the supply through $L_1$. An ideal triplexer is implemented as an S-parameter block to subdivide the output power from the cascode into the fundamental, second- and third-harmonic frequency components. Each of these are parametrically load pulled as follows. The first- and second-harmonic impedance are set according to (2.5) and (2.6). The second-harmonic impedance is then locally swept across resistive components for particular points of interest. The third harmonic is simply shorted because simulations show it has less than a two percentage point effect on PAE.

This impedance sweep focuses on the continuous Class-AB mode, whereas our earlier work in [76] explored a wider sweep for the first three harmonics. In this earlier work, the optimum
second-harmonic termination in simulation occurred at $-j75 \Omega$, which we originally classified as a Class-J condition. Class-J in this use generically referred to PAs having complex fundamental and a reactive second-harmonic termination, according to a definition provided in [71]. However, now with continuous Class-AB mode, we refine our definition such that Class-J refers to fundamental and second-harmonic impedances given by (2.5) and (2.6) for $|\beta| = 1$ whereas continuous Class-AB more broadly refers to the full range of possible values of $\beta$.

In addition to this terminology update, the HiCUM bipolar transistor model has also been recently updated in the SiGe 8HP design kit, and this new model is used for the simulations herein. The model update indicates optimum performance occurs near a second-harmonic termination of $-j62.5 \Omega$.

The results of the harmonic load pull are shown in Fig. 2.2. These results indicate that the $\text{oP}_{1\text{dB}}$ and PAE can vary by 2.4 dB and over 12% points with $\beta$. According to [58], this is due to three key transistor non-linearities: (a) the non-linear input capacitor of $Q_1$, (b) operation into the knee region, and (c) the non-linear output capacitor of $Q_2$. Our results show that the optimum $\beta$ for maximum PAE is 0.4 which sets a target fundamental impedance of $65 + j25 \Omega$ and second-harmonic impedance of $-j62.5 \Omega$.

To evaluate the impact of a more realistic second-harmonic impedance with a resistive component, we perform a second load pull with the fundamental impedance fixed at $65 + j25 \Omega$ and vary the resistive and reactive parts of the second harmonic. The results are shown in Fig. 2.3. While a resistive component in the second harmonic impedance degrades the PAE and $\text{oP}_{1\text{dB}}$ as expected, these results indicate that some loss in the second harmonic can be accommodated without significant efficiency degradation. Although the variation of the second-harmonic reactance along these load-pull contours deviates the PA from ideal continuous-mode operation, the effect on linearity is small, according to simulation. We thus target a second-harmonic reactance between $-j60 \Omega$ to $-j30 \Omega$ when including the resistance in the second harmonic.

Circuit topologies have been proposed which can provide a reactive fundamental and a reflective, capacitive second harmonic. One such network consists of a series transmission line to set the
second-harmonic phase, an open-circuit stub which is a quarter-wavelength at the second harmonic to provide an harmonic short, and then a fundamental-frequency matching network [78]. Although this network is easy to design, the quarter-wave stub can be large and the series transmission line can introduce unwanted insertion loss. We therefore seek to find a harmonic matching network which is both compact and low loss, leading us to consider the topologies presented in the following section.

2.3 Harmonic Matching Network Design

The primary objective of the harmonic output matching network design is to convert the 50-Ω load to the optimum fundamental and second-harmonic impedances determined by the load-pull analysis. In addition, the network should be able to source the dc bias to the collector of the cascode amplifier and provide dc isolation between the output load and the cascode amplifier. This isolation allows the PA to be later incorporated with transmit/receive switches which may short the output.
to ground. Our objectives should be met with the lowest possible insertion loss and a compact size. Furthermore, the output network topology should be capable of realizing a wide range of fundamental and second-harmonic impedance so that it is useful for designs having different power specifications or implemented in different technologies.

A general network which is capable of achieving these objectives consists of a band-pass filter which passes the fundamental and reflects the second harmonic and a low-pass matching network which optimally matches the fundamental. The design procedure of the low-pass matching network is straightforward [3]; however, placement of this matching network in relation to the band-pass filter has implications on the overall output network’s size and performance. Since the band-pass filter is designed to be transparent at the operating frequency, the fundamental-frequency matching network can either follow (Fig. 2.4(a), 2.4(b)) or be wrapped around (Fig. 2.4(c)) the band-pass filter. The location of the low-pass function can be used to reduce the size of the overall network.

The choice of the harmonic network topology in Fig. 2.4 can be made based on three considerations. First, the configuration of the matching element section can be determined based on whether we need to transform the load to a higher or lower impedance. Second, the ability to combine
different elements including transistor parasitic capacitance and the pad capacitance can result in
a compact and low-loss network. Third, the reference impedance of the band-pass filter is affected
by its position with respect to the matching network. The reference impedance of the band-pass
filter determines the element values and hence the size and insertion loss of the network.

2.3.1 Design of Band-pass Filter for Second-Harmonic

We begin with the design of the band-pass filter to achieve a pass band at the fundamental and a full
(reactive) reflection with a desired phase at the second harmonic. To achieve a steep out-of-band
response, a Chebyshev type-1 filter is proposed. This band-pass filter can be designed such that
in-band reflections are minimized and second-harmonic reactance (or phase-shift) is specified.
The m-th pole and zero of the reflection coefficient ρ of an n-th-order Chebyshev type-1 filter can be
expressed as [79]

\[
Z_{p,m} = \begin{cases} 
\sinh\left[-a + j\frac{\pi}{n}\left(\frac{1}{2} + m\right)\right], & \text{for } n \text{ even} \\
\sinh\left[-a + j\frac{\pi}{n}m\right], & \text{for } n \text{ odd}
\end{cases}
\]

\[
Z_{o,m} = \begin{cases} 
\sinh\left[-b + j\frac{\pi}{n}\left(\frac{1}{2} + m\right)\right], & \text{for } n \text{ even} \\
\sinh\left[-b + j\frac{\pi}{n}m\right], & \text{for } n \text{ odd}
\end{cases}
\]

where \( m \) is an integer-valued index varying over the range

\[
m = \begin{cases} 
-\frac{n}{2} \text{ to } \left(\frac{n}{2} - 1\right), & \text{for } n \text{ even} \\
-\left(\frac{n-1}{2}\right) \text{ to } \left(\frac{n-1}{2}\right), & \text{for } n \text{ odd}
\end{cases}
\]

Parameters \( a \) and \( b \) (real numbers \( \geq 0, \ a \geq b \)) determine the magnitude of maximum and
minimum reflection coefficient, $|\rho|_{\text{max}}$ and $|\rho|_{\text{min}}$, from zero up to the cut-off frequency

\begin{align*}
|\rho|_{\text{max}} &= \frac{\cosh(nb)}{\cosh(na)} \\
|\rho|_{\text{min}} &= \frac{\sinh(nb)}{\sinh(na)}
\end{align*}

(2.10)

(2.11)

All poles and zeros of $\rho$ are determined by the two independent variables $a$ and $b$; thus, two conditions are necessary to determine the filter reflection coefficient. In this work the two conditions we impose are the minimum $|\rho|_{\text{max}}$ and a specific phase of a large reflection (ideally perfect reflection) at the second harmonic. The required second-harmonic phase can be obtained by setting

\begin{align*}
\arg(\rho_{2,\text{opt}}) &= \sum_m \arg(j\omega_{2\text{nd}} - Z_{o,m}) - \sum_m \arg(j\omega_{2\text{nd}} - Z_{p,m}) \\
&= \sum_m \arctan \left( \frac{\omega_{2\text{nd}} - \cosh(b) \sin \left( \frac{\pi}{n} \left( \frac{1}{2} + m \right) \right)}{\sinh(b) \cos \left( \frac{\pi}{n} \left( \frac{1}{2} + m \right) \right)} \right) - \sum_m \arctan \left( \frac{\omega_{2\text{nd}} - \cosh(a) \sin \left( \frac{\pi}{n} \left( \frac{1}{2} + m \right) \right)}{\sinh(a) \cos \left( \frac{\pi}{n} \left( \frac{1}{2} + m \right) \right)} \right)
\end{align*}

(2.12)

where $\rho_{2,\text{opt}}$ is the desired optimum reflection coefficient at the second harmonic frequency and $m$ is taken over the range specified in (2.9). Parameter $\omega_{2\text{nd}}$ is the low-pass equivalent of the second harmonic frequency which can be found from (2.13) by setting $\omega_{BP} = 2\omega_0$

\begin{equation}
\omega_{LP} = \frac{\omega_0}{\omega_2 - \omega_1} \left( \frac{\omega_{BP}}{\omega_0} - \frac{\omega_0}{\omega_{BP}} \right)
\end{equation}

(2.13)

where $\omega_1$ and $\omega_2$ are band-edge frequencies and $\omega_0 = \sqrt{\omega_1 \omega_2}$ is the center frequency of the band.

Maximum in-band reflection coefficient ($|\rho|_{\text{max}}$) can be minimized subject to the constraint in (2.12) using the method of undetermined multipliers. This is the same procedure used by Fano in [79] but for a different set of constraints. Due to the arctangent function involved in (2.12), it is difficult to derive a minimum $|\rho|_{\text{max}}$ condition for a generalized $n$-order filter. Here, we derive the condition for minimum $|\rho|_{\text{max}}$ for a second-order filter.
For a second-order filter \((n = 2, \ m = \{-1, 0\})\),

\[
\arg(\rho_2,\text{opt}) = \arctan \left( \frac{\sqrt{2} \omega_{2nd} - \cosh(b)}{\sinh(b)} \right) + \arctan \left( \frac{\sqrt{2} \omega_{2nd} + \cosh(b)}{\sinh(b)} \right) \\
- \arctan \left( \frac{\sqrt{2} \omega_{2nd} - \cosh(a)}{\sinh(a)} \right) - \arctan \left( \frac{\sqrt{2} \omega_{2nd} + \cosh(a)}{\sinh(a)} \right) = \phi(a, b) \quad (2.14)
\]

Applying the method of undetermined multipliers to minimize \(|\rho|_{\text{max}}\) with the constraint in (2.14) results in the following:

\[
\frac{\partial \phi(a, b)}{\partial a} - \lambda \frac{\partial \phi(a, b)}{\partial b} = 0 \quad (2.15)
\]

\[
\frac{\partial |\rho|_{\text{max}}}{\partial a} - \lambda \frac{\partial |\rho|_{\text{max}}}{\partial b} = 0 \quad (2.16)
\]

After evaluating the derivatives (2.15) can be written as

\[-f(a) - \lambda f(b) = 0 \quad (2.17)\]

where

\[
f(x) = \frac{1 - \sqrt{2} \omega_{2nd} \cosh(x)}{\sinh^2(x) + (\sqrt{2} \omega_{2nd} - \cosh(x))^2} - \frac{1 + \sqrt{2} \omega_{2nd} \cosh(x)}{\sinh^2(x) + (\sqrt{2} \omega_{2nd} + \cosh(x))^2} \quad (2.18)
\]

and (2.16) can be written as

\[-\frac{\cosh(2b) \cdot 2 \sinh(2a)}{\cosh^2(2a)} - \lambda \frac{2 \sinh(2b)}{\cosh(2a)} = 0 \quad (2.19)\]

Eliminating \(\lambda\) from (2.17) and (2.19) we obtain

\[
\frac{\tanh(2a)}{f(a)} = \frac{\tanh(2b)}{f(b)} \quad (2.20)
\]

Solutions to (2.20) can be obtained graphically as shown in Fig. 2.5, and these values of \(a\) and \(b\) can be substituted into (2.14) to obtain the phase condition. Fig. 2.6, shows the reflection coefficient.
looking into the band-pass filter at both the fundamental and second-harmonic, for a range of valid $a$ and $b$. These results indicate that the phase can be tuned by 55 degrees while maintaining an in-band reflection coefficient less than $-25$ dB and a second-harmonic reflection coefficient higher than $-1.7$ dB across 26.5 to 29.5 GHz.

The second-harmonic reflection coefficient magnitude can be improved further by using a third-order filter. If we define

$$
g(x) = \frac{\sqrt{3} - 2\omega_{2nd} \cosh(b)}{\sinh^2(x) + \left(2\omega_{2nd} - \sqrt{3}\cosh(b)\right)^2} - \frac{\sqrt{3} + 2\omega_{2nd} \cosh(b)}{\sinh^2(x) + \left(2\omega_{2nd} + \sqrt{3}\cosh(b)\right)^2} - \frac{\omega_{2nd} \cosh(x)}{\omega_{2nd}^2 + \sinh^2(x)} \tag{2.21}
$$

then, minimum $|\rho|_{\text{max}}$ condition for the third-order filter is similar to (2.20) and can be written as

$$
\frac{\tanh(3a)}{g(a)} = \frac{\tanh(3b)}{g(b)} \tag{2.22}
$$
**Figure 2.6** Reflection coefficient of a second-order band-pass filter demonstrating second-harmonic phase tuning and well-matched fundamental. Frequency range corresponds to 26 GHz to 30 GHz for fundamental and 52 GHz to 60 GHz for second harmonic.
The reflection coefficient for the third-order filter is shown in Fig. 2.7. The third-order filter also shows an improved second-harmonic phase tuning capability of 100 degrees.

![Reflection Coefficient Diagram](image)

**Figure 2.7** Reflection coefficient of a third-order band-pass filter demonstrating second-harmonic phase tuning and well-matched fundamental. Frequency range corresponds to 26 GHz to 30 GHz for fundamental and 52 GHz to 60 GHz for second harmonic.

After the values of $a$ and $b$ have been determined for the required second-harmonic phase, the
poles and zeros of $\rho$ are known. The remaining steps in the design of the band-pass filter are (a) express $\rho$ as a rational function in the $s$-domain, (b) extract the LC low-pass ladder network, and (c) perform low-pass to band-pass and then impedance transformations. These steps are standard for band-pass filter design [3, 80] and are demonstrated in the following section. Note that a negative sign was used for the reflection coefficients for plots in Fig. 2.6 and Fig. 2.7, meaning the first element is a parallel LC resonator.

Finally, when the fundamental-frequency matching network is wrapped around the band-pass filter (Fig. 2.4(c)), the target second-harmonic phase of the band-pass filter should be revised by taking into account the phase shift of the fundamental-frequency matching component. This can be done by de-embedding that impedance.

### 2.3.2 Design Examples

Examples of two harmonic matching network designs are shown in Fig. 2.8, for fundamental matching networks either following or wrapped around the band-pass filter. The target fundamental and second-harmonic impedances are taken from our original design, namely $Z_1 = 65 + j25 \, \Omega$ (equivalent to $74.6||j194 \, \Omega$) and $Z_2 = -j40 \, \Omega$ (taking into account the impact of loss at the second harmonic, as in Fig. 2.3). The network topologies of Fig. 2.4(b) or Fig. 2.4(c) are selected for this example because $R_L$ needs to be transformed to a higher impedance. In these examples, passive losses and parasitics are not yet taken into account, but will be included subsequently.

We begin with the topology from Fig. 2.4(b) and shown again in Fig. 2.8(a), where the load impedance is first transformed to the target fundamental impedance and then the band-pass filter is designed. A series inductor, $L_{se} = 200 \, \text{pH}$, and shunt capacitor, $C_{sh} = 25 \, \text{fF}$, transform the 50-Ω load to $65 + j25 \, \Omega$ at the fundamental. The band-pass filter is then designed with a reference impedance of $74.6 \, \Omega$, which is the real part of the parallel equivalent of $Z_1$. For this reference impedance, the required second-harmonic impedance corresponds to a phase of $\arg(\rho_{2,\text{opt}}) = 123^\circ$. A second-order low-pass Chebyshev prototype with $123^\circ$ second-harmonic phase shift is achieved with $a = 2.94$ and $b = 0.044$. The low-pass prototype elements are $C_{\text{shuntLP}} = 0.151 \, \text{F}$ and $L_{\text{seriesLP}} = 0.148 \, \text{H}$ and the
band-pass filter elements are $C_{1bp} = 107 \text{ fF}$, $L_{1bp} = 300 \text{ pH}$, $C_{2bp} = 55 \text{ fF}$ and $L_{2bp} = 584 \text{ pH}$. The final network and its simulated reflection coefficient are shown in Fig. 2.8(a).

**Figure 2.8** Design examples for harmonic matching network topologies for PA targeting $Z_1 = 65 + j25 \Omega$ and $Z_2 = -j40 \Omega$. Example (a) is from Fig. 2.4(b) where the matching network follows the band-pass filter. Example (b) is from Fig. 2.4(c) where the matching network is wrapped around the band-pass filter.

We now design a harmonic matching network where the fundamental impedance matching network is wrapped around the band-pass filter—the topology from Fig. 2.4(c) and shown again in Fig. 2.8(b). Since the final series leg now includes two inductors and a single capacitor, these can be simplified into a single series LC network. As a result, this topology is preferred over the previous for smaller chip size. The values necessary for the fundamental match remain the same; however,
we must now absorb the shunt capacitance into the design of the band-pass filter. The rotation of the second-harmonic impedance due to $C_{sh}$ is de-embedded by modifying the second-harmonic impedance target of the band-pass filter to $-j62 \, \Omega$. The reference impedance for the filter is still 74.6 $\Omega$. The required second-harmonic impedance corresponds to a phase of $\arg(\rho_{2,\text{opt}}) = 100^\circ$. A second-order low-pass Chebyshev prototype with $100^\circ$ second-harmonic phase shift is achieved with $a = 3.2$ and $b = 0.037$. The low-pass prototype elements are $C_{\text{shuntLP}} = 0.116 \, \text{F}$ and $L_{\text{seriesLP}} = 0.114 \, \text{H}$ and the band-pass filter elements are $C_{1\text{bp}} = 82 \, \text{fF}$, $L_{1\text{bp}} = 393 \, \text{pH}$, $C_{2\text{bp}} = 72 \, \text{fF}$ and $L_{2\text{bp}} = 453 \, \text{pH}$. The final network and its simulated reflection coefficient are shown in Fig. 2.8(b).

### 2.3.3 Compensation of Network for Finite-Q Elements

Passive component losses deviate $\rho$ from the optimum value and must be compensated for within the design. The procedure for compensation of passive losses within the band-pass filter can be explained better if we consider one of the networks, namely Fig. 2.8(b).

First, the loss of the series tank ($L_{2\text{bp}}$ and $C_{2\text{bp}}$) can be compensated by simply modifying the matching network on the right side by adjusting the target load impedance. Second, the resistance $r_p$ of the parallel tank ($L_{1\text{bp}}$ and $C_{1\text{bp}}$) shunts the reference impedance of the filter $R_0$. Thus, the effect of $r_p$ can be compensated by increasing the filter reference impedance to $R'_0$ such that $r_p || R'_0 = R_0$, where $R_0$ is the original reference impedance. This can be incorporated in the design procedure described above when we transform the low-pass filter with 1-$\Omega$ reference impedance to a band-pass filter of a desired reference impedance. For example, if the shunt capacitor of the low-pass network is $C$, the band-pass filter elements can be determined as $L_{1\text{bp}} = \frac{R'_0}{\alpha C \omega_0}$ and $C_{1\text{bp}} = \frac{\alpha C}{\omega_0 R_0}$, where $\alpha = \frac{\omega_0}{\omega_2 - \omega_1}$[3, 80]. The modified reference impedance $R'_0$ can be related to the original reference impedance by

$$R'_0 = R_0 \frac{Q_{L1} Q_{C1} + \alpha C (Q_{L1} + Q_{C1})}{Q_{L1} Q_{C1}}, \quad (2.23)$$

where $Q_{L1}$ and $Q_{C1}$ are unloaded quality-factors of $L_{1\text{bp}}$ and $C_{1\text{bp}}$. Equation (2.23) indicates that the modified reference impedance would always be greater for finite quality passives than that for ideal passives. It is difficult to estimate the exact $R'_0$ because $Q_{L1}$ and $Q_{C1}$ are functions of $L_{1\text{bp}}$ and
\( C_{1\text{bp}} \); however, an approximate estimation of \( R'_0 \) can be made using average values of \( Q_{L_{1}} \) and \( Q_{C_{1}} \) suitable for the technology. Furthermore, an iterative approach can be taken, where the network is first designed for loss-less components, then these L and C values are used to estimate Q factors, which then are used to update the reference impedance. Iteration can continue until we converge on accurate Q values.

### 2.3.4 Final Network Accommodating Parasitics

We conclude this section by discussing how the final design is updated to accommodate parasitic shunt capacitance and interconnect inductance. We also discuss how the design values can be adjusted to reduce insertion loss. This example is done for the network in Fig. 2.8(b) and describes the final design values used for the PA we have implemented and which is discussed in section V.

First, the network is updated to accommodate parasitics and the pad capacitor. We update the low-pass prototype and the fundamental match with a new load impedance \( (R_L||C_P) \), where \( C_P (46 \text{ fF}) \) is the pad capacitance which shunts the output load. The filter’s reference impedance was originally \( R_{\text{optFP}} (74.6 \text{ } \Omega) \) for a loss-less network; however, assuming Q-factors of 25 and 14 for the inductor and capacitors and band-edge frequencies of 26.5 GHz and 29.5 GHz, the impedance is increased to 84 \( \text{ } \Omega \) according to (2.23). The value of the fundamental network and band-pass filter elements are now \( C_{\text{sh}} = 30 \text{ fF}; L_{\text{se}} = 330 \text{ } \mu\text{H}; C_{1\text{bp}} = 77 \text{ fF}; L_{1\text{bp}} = 421 \text{ } \mu\text{H}; C_{2\text{bp}} = 61 \text{ fF}; \) and \( L_{2\text{bp}} = 536 \text{ } \mu\text{H}. \) Also, instead of using an extra inductance to implement \( L_{\text{se}} \), \( C_{2\text{bp}} \) is increased to 157 fF.

The series capacitor \( C_{2\text{bp}} \) and inductor \( L_{2\text{bp}} \) can have undesirable insertion loss at 28 GHz. Also, the resonant frequency of the inductor \( L_{2\text{bp}} \), realized here as a 1.25-turn spiral, is 40 GHz, which is close to our frequency of operation. The fundamental match can be maintained if the inductor \( L_{2\text{bp}} \) is reduced and the capacitor \( C_{2\text{bp}} \) is increased such that the impedance of the series tank at fundamental \( Z_{\text{series}} = j(\omega L_{2\text{bp}} - (1/\omega C_{2\text{bp}})) \) remains constant. The impact on the second-harmonic impedance is small as long as the impedance of the series arm is high at the second harmonic.

Reducing \( L_{2\text{bp}} \) to 400 \( \mu\text{H} \) and increasing \( C_{2\text{bp}} \) to 600 fF maintains the fundamental impedance, reduces the insertion loss at fundamental frequency by 0.6 dB and changes the magnitude and
phase of the second-harmonic reflection coefficient by 0.5 dB and 4 degrees only.

The last design step is to compensate for the parasitic elements needed to realize an actual design. These parasitics are shown in Fig. 2.9(a) in red, described as follows: $C_{1bp}$ is realized by the device and wiring capacitance; $L_{\text{par}}$ (25 pH) represents the parasitic transmission line between the device and inductor $L_{1bp}$; $C_{\text{par1}}$ (18 fF) is the parasitic capacitance of inductor $L_{1bp}$; and $C_{\text{par2}}$ and $C_{\text{par3}}$ (20 fF each) are the parasitic capacitances of inductor $L_{2bp}$.

Compensation for $C_{\text{par3}}$ is straightforward through combining it with the output pad capacitance. To compensate for the other parasitic elements we perform two Norton transformations as shown in Fig. 2.9(b) and (c). In Fig. 2.9(b), a Norton transform was applied to rearrange $C_{\text{par1}}$ and $C_{2bp}$ which results in multiplication of all resistance and reactances to the right of $C_{2bp}$ by $n_1^2$, where $n_1 = \frac{C_{2bp}}{C_{2bp} + C_{\text{par1}}}$. Inductors $L_{\text{par}}$ and $L_{1bp}$ can be rearranged as shown in Fig. 2.9(c) by using another Norton transform which results in multiplication of all resistance and reactances to the right of $L_{1bp}$ by $n_2^2$, where $n_2 = \frac{L_{1bp} + L_{\text{par}}}{L_{1bp}}$. The network in Fig. 2.9(c) differs from the original architecture in Fig. 2.4(c) due to the parasitic capacitor $\frac{C_{\text{par4}}}{n_2^2}$ only. The effect of the parasitic capacitor $\frac{C_{\text{par4}}}{n_2^2}$ in Fig. 2.9(a) is to reduce the value of $C_{1bp}$.

Note that the parasitic elements $C_{\text{par1}}$, $C_{\text{par2}}$ and $C_{\text{par3}}$ are dependent on the values of the passive elements $L_{1bp}$ and $L_{2bp}$. The final values of the network components were $C_{1bp} = 85$ fF; $L_{1bp} = 350$ pH, $C_{2bp} = 646$ fF and $L_{2bp} = 368$ pH. As illustrated in Fig. 2.10, the fundamental impedance is the same as the targeted value whereas the second harmonic impedance was $4 - j32$ Ω compared to a target of $-j40$ Ω.

### 2.4 Class-AB PA Comparisons

To evaluate the efficacy of harmonic tuning, we compare the continuous Class-AB PA ($\beta = 0.4$) with a classical Class-AB PA ($\beta = 0$) and a simple LC-tuned PA for realistic component loss. The output networks of the three PAs being compared along with the fundamental and second-harmonic impedance are shown in Fig. 2.11. All PAs have the same operating point and bias conditions as originally presented in Fig. 2.1.
Figure 2.9 Effect of parasitic components on the output network (a) major parasitic components (b) re-arrangement of $C_{2\text{bp}}$ and $C_{\text{par1}}$ (c) re-arrangement of $L_{1\text{bp}}$ and $L_{\text{par}}$. 

$\frac{C_{2\text{bp}}}{n_1^2}$

$\frac{C_{\text{par4}}}{n_1^2}$

$\frac{C_{\text{par1}}}{n_1^2} + \frac{C_{\text{par2}}}{n_1^2}$
**Figure 2.10** Fundamental and second harmonic impedance of the final network including all parasitics.

**Figure 2.11** Output network schematic of PA modes compared in Section 2.4 (top), fundamental and second harmonic impedances realized by the three networks: Class-AB (green), LC tuned (blue), continuous mode class-AB (red).
Figure 2.12 Effect of finite quality factor of passive elements on 1-dB compression PAE and output power for the three types of Class-AB PA, for (a) varying inductor Q with capacitor Q fixed at 14 and (b) varying capacitor Q with inductor Q fixed at 25.
The classical Class-AB PA shown in Fig. 2.11(a) is designed using an open-circuited stub which is \( \lambda/4 \) at the second harmonic, where \( \lambda \) is the wavelength. This achieves a second-harmonic short condition. A third-harmonic short could be achieved using another resonant open stub but it is avoided here to reduce the insertion loss of the network. The classical Class-AB network then has a two-element LC network to achieve a fundamental impedance of 65 \( \Omega \). The LC-tuned network shown in Fig. 2.11(b) is initially designed to achieve a fundamental impedance which is the same as the classical Class-AB PA. Then the component values are swept over a limited range to maximize the PAE. Finally, the continuous Class-AB PA shown in Fig. 2.11(c) uses the network architecture in Fig. 2.4(c) and the design technique outlined in Section 2.3.2.

Using large-signal PA simulations, the output power and PAE at 1-dB compression is compared for the three PA modes with varying quality factor of inductors and capacitors, as shown in Fig. 2.12. This shows how much the performance improvement depends upon quality factor. Fig. 2.12(a) shows the comparison between the PA modes for a fixed capacitor quality of 14 with inductor \( Q \) varied from 10 to 20. The continuous Class-AB PA shows significant benefit in PAE over the other two modes for inductor \( Q \) factors above 15. Similarly, Fig. 2.12(b) shows the comparison between the PA modes for a fixed inductor \( Q \) of 25 with capacitor \( Q \) varied from 6 to 22. The capacitor \( Q \) degrades the performances of all the PA modes by a similar amount, meaning the benefit of the continuous mode is retained even for low capacitor \( Q \).

A comparison of the PA modes is presented in Table 2.1 for ideal passives and for finite-quality passives. For the finite-\( Q \) factor case we assume an inductor \( Q \) of 25, a capacitor \( Q \) of 14 and a transmission line loss of 0.1 dB/mm. The continuous Class-AB mode shows 4-5% (10-11%) point benefit in peak PAE and 1-dB compression PAE over the LC-tuned PA (Class-AB PA). The benefit reduces to 1% (3%) point at both 3-dB and 6-dB back-offs with respect to the LC-tuned PA (Class-AB PA). The continuous Class-AB mode also has a higher gain, a wider 3-dB bandwidth and a higher \( oP_{1dB} \). A small part of the peak efficiency benefit shown by the continuous Class-AB mode is due to the 0.06-dB (0.16-dB) lower insertion loss of the output network compared to the LC-tuned PA (Class-AB PA). However, by increasing the \( Q \) of the passives and equalizing the network losses
Table 2.1 Performance comparison of classical Class-AB PA, LC-tuned PA and Continuous Class-AB mode PA

<table>
<thead>
<tr>
<th>Ideal Passives</th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Class</td>
<td>Class-AB</td>
<td>LC-tuned</td>
<td>Cont. mode</td>
</tr>
<tr>
<td>Gain (dB)</td>
<td>15.7</td>
<td>16.7</td>
<td>17.2</td>
</tr>
<tr>
<td>3-dB bandwidth (GHz)</td>
<td>25-31.7</td>
<td>24.3-36.4</td>
<td>25.2-39</td>
</tr>
<tr>
<td>$P_{sat}$ (dBm)</td>
<td>18.4</td>
<td>19.8</td>
<td>19.4</td>
</tr>
<tr>
<td>$oP_{1dB}$ (dBm)</td>
<td>17.6</td>
<td>17.7</td>
<td>18</td>
</tr>
<tr>
<td>Peak PAE (%)</td>
<td>41.1</td>
<td>48.6</td>
<td>53.7</td>
</tr>
<tr>
<td>PAE 1-dB comp. (%)</td>
<td>40.6</td>
<td>47.3</td>
<td>52.9</td>
</tr>
<tr>
<td>PAE 6-dB-back-off (%)</td>
<td>19.5</td>
<td>20.5</td>
<td>20.7</td>
</tr>
</tbody>
</table>

| Finite-Q passives |   |   |   |
| Class            | Class-AB | LC-tuned | Cont. mode |
| Output network loss (dB) | 0.5     | 0.4     | 0.34     |
| Gain (dB)        | 14.6      | 15.4      | 15.8      |
| 3-dB bandwidth (GHz) | 24.7-33.4 | 24-38    | 25.4-41  |
| $P_{sat}$ (dBm)  | 18.1      | 19.4      | 19        |
| $oP_{1dB}$ (dBm) | 17.4      | 17.5      | 17.8      |
| Peak PAE (%)     | 34.7      | 41        | 45        |
| PAE 1-dB comp. (%) | 34.7      | 39.6      | 44        |
| PAE 3-dB-back-off (%) | 25.8      | 28       | 29.2      |
| PAE 6-dB-back-off (%) | 16.6      | 17.9      | 18.9      |
| AM-PM 3-dB-back-off (°) | 0.1     | 0.6      | 3        |
| IM3 3-dB-back-off (dBc) | -54.6    | -49      | -42.5    |

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we have verified that the continuous Class-AB PA retains 3.6% (9%) point benefit at peak and 1-
dB compression point and 0.5-1% (1.5-2%) point benefit up to 6-dB back-off over the LC-tuned (Class-AB) PA.

Linearity of the PA modes can be assessed in simulation from the $oP_{1dB}$, amplitude-modulation to phase-modulation (AM-PM) distortion, and third-order intermodulation distortion product (IM3). The classical Class-AB PA has superior AM-PM, and IM3 metrics compared to the other two modes. The continuous Class-AB mode PA has better $oP_{1dB}$ response compared to the LC-tuned PA but worse AM-PM and IM3 performance. This can be attributed to the higher output voltage swing of the continuous Class-AB mode which causes a larger variation of the nonlinear device capacitance. However, the IM3 performance of the continuous Class-AB mode is still adequate to meet our IM3 target of -33 dBc at 6-dB back-off.

Variation of peak PAE and $oP_{1dB}$ of the three PAs with frequency are shown in Fig. 2.13. Across 26 to 30 GHz, the continuous Class-AB mode PA has better PAE and $oP_{1dB}$ than the other two PAs; however, it does show slightly higher variation in $oP_{1dB}$ across the band.

### 2.5 IC Implementation and Measurements

To illustrate the performance possible for a continuous Class-AB design in SiGe, we have implemented a 28-GHz PA with a harmonic output harmonic matching network using the topology in Fig. 2.4(c). The PA was designed and fabricated in 130-nm GlobalFoundries SiGe BiCMOS 8HP technology. The high-performance NPN transistor with peak $f_T$ ($f_{max}$) of 200 GHz (265 GHz) is used because of its superior RF performance. We use a five-layer back-end-of-line (BEOL), where the top three thick layers (MQ, LY, and AM) are used to realize low-loss passive structures.

The final PA schematic is shown in Fig. 2.14. The output matching network includes the final component values and transformations we applied from Fig. 2.9(c). We use a dual-base Collector-Base-Emitter-Base-Collector (CBEBC) layout for each device of the cascode. Compared to the Collector-Base-Emitter (CBE) style layout, the CBEBC configuration has higher $f_T$, $f_{max}$ and lower external base resistance and collector resistance[16] and hence it gives a higher gain and $oP_{1dB}$. The
Figure 2.13 Variation of performance across frequency for classical Class-AB, LC-tuned, and continuous Class-AB PAs for (a) PAE and (b) $oP_{1dB}$. 
Figure 2.14 Schematic of final 28-GHz single-stage PA.

Figure 2.15 Die photograph of 28-GHz single-stage PA.
CBE configuration reduces the emitter inductance as mentioned in [49], however in our design this is not a problem because we use explicit inductive degeneration at the emitter (TL3) to improve the stability and the linearity of the PA. The four fingers of the device share adjacent deep trench regions for a compact layout, minimizing device interconnects. The base terminals are wired using M1, M2 metal layers whereas the emitter and collector terminals are wired using M1, M2 and MQ to meet electromigration current density at 100°C and to minimize interconnect resistance. Inductors \( L_{1bp} \) (octagon, 116-\( \mu \)m diameter, 12-\( \mu \)m width, 1.25 turns) and \( L_{2bp} \) (octagon, 110-\( \mu \)m diameter, 8-\( \mu \)m width, 1.25 turns) were implemented in top-level metal with a patterned ground shield in the bottom metal layer. Transmission lines for the input match were implemented as grounded coplanar waveguide. The chip micrograph is shown in Fig. 2.15, and the die area is 0.61 mm by 0.73 mm, including pads.

![Figure 2.16](image)

**Figure 2.16** S-parameter measurement results of the PA (simulation results are shown with dashed curves).

The PA measurements were performed with a collector supply voltage of 3.6 V and a collector bias current of 17 mA. S-parameter simulation and measurement results of the PA are shown in Fig. 2.16. The input match, \( S_{11} \), shows close agreement with the simulations whereas \( S_{22} \) is slightly
Figure 2.17 Swept power measurement results of the PA at 28 GHz (simulation results are shown with dashed curves).

offset due to an imperfect pad model. The gain at 28-GHz is 15.3 dB, agreeing with the simulated value. The gain has less than 0.8-dB variation across 26 to 30 GHz.

Fig. 2.17 presents measured and simulated gain and PAE versus output power at 28 GHz. The saturated output power ($P_{sat}$) is 18.6 dBm, $oP_{1dB}$ is 15.5 dBm, peak PAE is 35.3%, PAE at 1-dB compression is 31.5%, and PAE at 6-dB back-off is 11.5%. Compared to simulations, measurement results show the same $P_{sat}$, three percentage point lower PAE at 1-dB compression and 1.5-dB lower $oP_{1dB}$.

To further assess linearity of the PA, we first measure AM-PM distortion and IM3. The AM-PM distortion measurement shown in Fig. 2.18 reveals less than 2° phase shift up to the 1-dB compression point. The swept-power IM3 measurement is presented in Fig. 2.19. The measured IM3 product at 6-dB back-off with a second tone at 17-MHz, 107-MHz and 211-MHz offsets from 28 GHz were -34.6 dBc, $-33.7$ dBc and $-44$ dBc, respectively. Measurements with modulated waveforms are not possible due to equipment limitations; however, our commercial partner did measure our PA and reported error-vector magnitude (EVM) results for a slightly different, and more linear (larger conduction angle) bias condition in [81]. The measured EVM in this condition was $-22$ dB at 6-dB
Figure 2.18 AM-PM distortion measurement of the PA at 28 GHz.

Figure 2.19 IM3 distortion measurement of the PA at 28 GHz.
Table 2.2 Performance of the PA across band

<table>
<thead>
<tr>
<th>Frequency (GHz)</th>
<th>27</th>
<th>28</th>
<th>29</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain (dB)</td>
<td>15</td>
<td>15.3</td>
<td>15.5</td>
</tr>
<tr>
<td>$P_{sat}$ (dBm)</td>
<td>18.8</td>
<td>18.6</td>
<td>18</td>
</tr>
<tr>
<td>$oP_{1dB}$ (dBm)</td>
<td>15.1</td>
<td>15.5</td>
<td>15.9</td>
</tr>
<tr>
<td>Peak PAE (%)</td>
<td>33.8</td>
<td>35.3</td>
<td>34.7</td>
</tr>
<tr>
<td>PAE 1-dB comp. (%)</td>
<td>27.6</td>
<td>31.5</td>
<td>33.2</td>
</tr>
<tr>
<td>PAE 6-dB-back-off (%)</td>
<td>10.7</td>
<td>11.5</td>
<td>13.5</td>
</tr>
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</table>

Table 2.3 Measured PA performance vs. temperature at 28 GHz

<table>
<thead>
<tr>
<th>Temperature (°C)</th>
<th>25</th>
<th>56</th>
<th>86</th>
</tr>
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<tr>
<td>Gain (dB)</td>
<td>15.3</td>
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<td>13.5</td>
</tr>
<tr>
<td>$P_{sat}$ (dBm)</td>
<td>18.6</td>
<td>18.3</td>
<td>17</td>
</tr>
<tr>
<td>$oP_{1dB}$ (dBm)</td>
<td>15.5</td>
<td>14.4</td>
<td>11.3</td>
</tr>
<tr>
<td>Peak PAE (%)</td>
<td>35.3</td>
<td>34</td>
<td>30.6</td>
</tr>
<tr>
<td>PAE 1-dB comp. (%)</td>
<td>31.5</td>
<td>27</td>
<td>17.3</td>
</tr>
<tr>
<td>PAE 6-dB-back-off (%)</td>
<td>11.5</td>
<td>11.2</td>
<td>8</td>
</tr>
</tbody>
</table>

back-off for an 800-MHz OFDM signal with 16-level quadrature amplitude modulation. Measured peak PAE was 35% and gain was approximately 17.3 dB.

Tables 2.2 and 2.3 summarize the performance of the PA across 27 to 29 GHz and across temperature. The gain, $P_{sat}$ and $oP_{1dB}$ show small variation across the frequency band.

### 2.6 Conclusions

In this chapter the efficacy of second harmonic tuning for millimeter-wave PAs is demonstrated with a 28-GHz harmonic-tuned continuous Class-AB mode PA. A design methodology for realizing a
### Table 2.4 Performance comparison with Ka and Q-band Power Amplifiers

<table>
<thead>
<tr>
<th>Reference</th>
<th>Frequency (GHz)</th>
<th>Architecture</th>
<th>Gain (dB)</th>
<th>Psat (dBm)</th>
<th>oP1dB (dBm)</th>
<th>33.8-35.3 (%)</th>
<th>10.7-13.5 (%)</th>
<th>Technology</th>
</tr>
</thead>
<tbody>
<tr>
<td>This work</td>
<td>27-29</td>
<td>Continuous Class-AB</td>
<td>15-15.5</td>
<td>18.8-18</td>
<td></td>
<td>15.1-15.9</td>
<td>33.8-35.3</td>
<td>10.7-13.5</td>
</tr>
<tr>
<td>[60] Mortazavi</td>
<td>27-31</td>
<td>Class-F, two-stage</td>
<td>21.2</td>
<td>17.1</td>
<td>15</td>
<td>42</td>
<td>18.5</td>
<td>130-nm SiGe</td>
</tr>
<tr>
<td>[59] Mortazavi</td>
<td>26-30</td>
<td>Class-F¹/F</td>
<td>10.3</td>
<td>17.1</td>
<td>15</td>
<td>40</td>
<td>12</td>
<td>130-nm SiGe</td>
</tr>
<tr>
<td>[61] Mortazavi</td>
<td>38</td>
<td>Class-F¹</td>
<td>16</td>
<td>16.5</td>
<td>15</td>
<td>38.5</td>
<td>16.5</td>
<td>130-nm SiGe</td>
</tr>
<tr>
<td>[62] Datta</td>
<td>39-47</td>
<td>Stacked Class-E</td>
<td>4</td>
<td>23.4</td>
<td>N.A¹</td>
<td>34.9</td>
<td>N.A¹</td>
<td>130-nm SiGe</td>
</tr>
<tr>
<td>[24] Agah</td>
<td>45</td>
<td>Stacked Class-AB</td>
<td>9.5</td>
<td>18.6</td>
<td>17.5</td>
<td>34.4</td>
<td>15</td>
<td>45-nm SOI CMOS</td>
</tr>
<tr>
<td>[27] Dabag</td>
<td>38-47</td>
<td>Stacked</td>
<td>9.4</td>
<td>15.9</td>
<td>N.A¹</td>
<td>32.7</td>
<td>N.A</td>
<td>45-nm SOI CMOS</td>
</tr>
<tr>
<td>[64] Datta</td>
<td>42-46</td>
<td>Class-E, two-stage</td>
<td>10</td>
<td>20.2</td>
<td>N.A¹</td>
<td>31.5</td>
<td>N.A¹</td>
<td>130-nm SiGe</td>
</tr>
<tr>
<td>[28] Kim</td>
<td>45</td>
<td>Class-AB, two-stage</td>
<td>19.5</td>
<td>15</td>
<td>14.5⁹</td>
<td>27.5</td>
<td>9⁹</td>
<td>45-nm SOI CMOS</td>
</tr>
<tr>
<td>[26] Tai</td>
<td>45</td>
<td>Class-B, two-stage</td>
<td>16.6</td>
<td>17.5</td>
<td>N.A¹</td>
<td>26</td>
<td>N.A¹</td>
<td>130-nm SiGe</td>
</tr>
<tr>
<td>[66] Chakrabarti</td>
<td>47.5</td>
<td>Stacked Class-EE</td>
<td>9.8</td>
<td>17.9</td>
<td>14¹</td>
<td>25.5</td>
<td>7.5⁹</td>
<td>45-nm SOI CMOS</td>
</tr>
<tr>
<td>[23] Agah</td>
<td>42</td>
<td>Doherty</td>
<td>7</td>
<td>18</td>
<td>11³</td>
<td>23</td>
<td>8³</td>
<td>45-nm SOI CMOS</td>
</tr>
<tr>
<td>[25] Chen</td>
<td>37</td>
<td>double stacked cascode</td>
<td>8</td>
<td>14.8</td>
<td>11.5</td>
<td>16.2</td>
<td>4.5¹</td>
<td>45-nm SOI CMOS</td>
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<tr>
<td>[29] Essing</td>
<td>27</td>
<td>8-way combined, Class-AB</td>
<td>20.7</td>
<td>31</td>
<td>NA</td>
<td>13</td>
<td>NA</td>
<td>250-nm SiGe</td>
</tr>
</tbody>
</table>

¹ Estimated from swept power plots.

⁹ Could not be estimated due to excessive gain expansion
the parasitics require some modification to the topology which has been achieved primarily through Norton transformation. Through simulations, we have demonstrated that the harmonic termination in continuous Class-AB mode improves PAE at $P_{1\text{dB}}$ by four to seven percentage points compared to a traditional Class-AB PA as well as a PA realized using a simple LC matching network targeting a fundamental-frequency match only. At 6-dB back off, the PAE improvement is reduced to around one percentage point. The net result is that the PAE can be improved over the range from 6-dB back off up through $P_{1\text{dB}}$, reducing power consumption in the transmitter.

We demonstrated the application of this design methodology with a 28-GHz integrated PA designed in a 130-nm SiGe BiCMOS technology. A performance comparison with state-of-the-art PAs in Ka-band and Q-band is shown in Table 2.4. As observed in Table 2.4, Class-F and inverse Class-F PAs presented in [59, 60] achieve 4 to 5% points higher peak and back-off PAE compared to our design. However, for a high PMEPR modulation scheme we also need to compare the linearity of the Class-F and inverse Class-F PAs with the continuous class-AB mode PA presented in this work. While the continuous class-AB mode PA achieves excellent linearity demonstrated by low AM-PM distortion and IM3 product, linearity data of the Class-F/inverse Class-F PAs is not available at the moment for comparison. One other benefit of this work is the usage of the cascode amplifier compared to the common-emitter amplifier in the Class-F/inverse Class-F PAs. While the cascode amplifier has a higher knee voltage which causes a small reduction in PAE, it also provides about 5-dB higher gain per stage, better reverse isolation and is better suited to handle the higher breakdown limit of $BV_{CBO}$. Note that, the Class-F/inverse Class-F PAs as well as the continuous mode PA in this work use the $BV_{CBO}$ limit. The Class-E design presented in [62] achieves 5-dB higher output power and similar efficiency as our design, however, it has excessive non-linearity as shown by the 10-dB gain expansion in swept power plots. To summarize, the PA presented in this work achieves high peak and back-off PAEs with high gain, consistent performance across 27-29 GHz and excellent back-off linearity.
In the previous chapter it was demonstrated that harmonic-tuned continuous-mode Class-AB PAs can achieve significant improvement in peak and 1-dB compression PAE at 28-GHz over classical Class-AB and LC-tuned PAs. Performance comparison with state-of-the-art Class-F and Class-E PAs is section 2.6 showed higher gain per stage, better reliability and potentially better linearity. We also demonstrated that this performance benefit is dependent on the quality of passive components. As
we go higher up in the millimeter-wave frequency bands we expect a decrease in the performance benefit of harmonic tuned PAs over fundamental-match-only PAs due to both passive and active components of the PA. Review of existing work in harmonic-tuned millimeter-wave PAs in silicon-based technologies, specifically Class-F PAs in [59–61] and Class-E PAs in [64, 67, 68] shows that there has not been a thorough study on the efficacy of harmonic tuning versus frequency. Investigating the relative benefit given by harmonic tuning over fundamental-match-only PAs in a particular silicon technology is of prime interest for both integrated circuit designers and device manufacturers. For IC designers, this study could be beneficial for deciding whether to choose harmonic-tuned PA or a fundamental-match-only PA for a given frequency and for choosing the quality factor of passive components. For device manufacturers, this research would reveal the ultimate limits on the performance of their technology at different frequencies and potential improvements possible with device enhancements. In this chapter, the effect of harmonic tuning in continuous-mode Class-AB PAs was investigated to establish the break-even frequency at which harmonic tuning provides no additional benefit.

In the first part of this chapter the harmonic generation capability of the active device versus frequency is studied for a SiGe BiCMOS technology. The contribution of different kinds of device non-linearities to harmonic generation is studied with the help of modified load-line simulations. The variation of these non-linearities with frequency is presented. Next, constrained harmonic load-pull simulations similar to those in chapter 2 are performed for a range of millimeter-wave frequencies. Rough conclusions are drawn about the break-even frequency based on the simulation of the active device with ideal passive components.

Next, a second type of harmonic matching network which can be realized with microstrip stubs is presented. Compared to the harmonic matching network presented in Chapter 2, the network presented here is easier to realize for higher frequencies and is more suitable for our study. The target second harmonic reactance is realized with a series microstrip line and a quarter-wave long open stub whereas the fundamental impedance is realized with a $\pi$-network. A virtual impedance based design technique is introduced for a $\pi$-network and trade-offs between power loss and bandwidth
of the network is presented. The performance of the full harmonic-tuned PA is then studied and compared with a fundamental-match-only LC-tuned PA for a wide range of frequencies through simulations. The impact of passive quality on the performance is demonstrated versus frequency and the break-even frequency is established.

Finally, to validate these simulation studies, two PAs are fabricated and measured, one at 28 GHz and another at 60 GHz. The 28-GHz PA achieves 30.9-dB gain, 16.2-dBm oP1dB, 35.5% peak-PAE, and 14% PAE at 6-dB back-off. Use of harmonic tuning at 28 GHz improves the efficiency by an estimated four percentage points. The 60-GHz PA achieves 18.7-dB gain, 13.3-dBm oP1dB, 25% peak-PAE, and 9% PAE at 6-dB back-off. Use of harmonic tuning at 60 GHz improves the efficiency by an estimated two percentage points.

### 3.1 Harmonic generation of active devices with frequency

Harmonic components at the PA output are generated due to non-linearities in the device including i) non-linear transconductance of the device, ii) variation of input capacitor \(C_{be}\) with voltage, iii) operation in reduced conduction angle mode (e.g Class-AB), iv) variation of output capacitor \(C_{cb}, C_{cs}\) with voltage, and v) effect of the I-V knee (saturation region for bipolar devices/ triode region for MOSFET devices) [71]. To study the impact of these non-linearities over frequency, large-signal simulations are performed on a cascode amplifier with open and short impedances. These simulations use the HiCUM model which is accurate up to the second harmonic frequencies considered in our work [82]. Due to equipment limitations direct measurement of second and third harmonic components of current and voltage is not possible at this time. For a short output impedance, the collector current of the cascode amplifier would swing between its maximum and minimum limits, provided the input power is high enough, whereas the voltage swing would be very small. Thus, out of the above-mentioned non-linearities only i), ii) and iii) would contribute to harmonic generation. For an open output impedance, the collector voltage of the cascode amplifier would swing between the limits whereas the current swing would be very small. In this case, effects of iv) and v) would dominate. This method enables the study of harmonic component generation prior to
the design of a full harmonic matching network at different frequencies. For the short and open

![Diagram of harmonic matching network](image)

**Figure 3.1** (a) Set up for cascode amplifier simulation with short impedance (b) Second and third harmonic current amplitude normalized to fundamental versus frequency for short load.

output impedance simulations a good input match is provided and maintained for all frequencies. For the short load simulation, a bias tee is used at the cascode output as shown in Fig. 3.1(a). For the open load simulation, the dc feed inductor tunes out the intrinsic device capacitance as shown in Fig. 3.2(a). Fig. 3.1(b) shows the normalized second- and third-harmonic components of current for a short load from 28 to 78 GHz for a fixed fundamental component (39 mA). A couple of important observations can be made from this figure. The second-harmonic component is the dominant component compared to the third harmonic. Also, the magnitude of the second-harmonic current does not change significantly with increasing frequency. Fig. 3.2(b) shows the normalized harmonic components of voltage from 28 to 78 GHz for a fixed fundamental component (2.9 V). For the open load simulation, the second harmonic voltage is the dominant component as well. The second
and third harmonic component show significant reduction as we move to higher harmonics. Thus, apart from fundamental, the second harmonic impedance would have a significant impact on the performance of the PA. This impact would reduce with increasing frequency.

![Diagram](image)

**Figure 3.2** (a) Set up for cascode amplifier simulation with open impedance (b) Second and third harmonic voltage amplitude normalized to fundamental versus frequency for open load.

To further illustrate the impact of second harmonic tuning on the performance of the PA, a constrained load pull simulation is performed at 28, 38, 56 and 78 GHz according to the optimum fundamental and harmonic impedances of the continuous class AB-mode PA given by the equations (equations (2.5) and (2.6) from chapter 2):

\begin{align}
Z_1 &= R_{\text{opt}}(1 + j\beta), \\
Z_2 &= -j\frac{3}{8}R_{\text{opt}}\frac{(\theta - \sin(\theta))}{\sin^3\left(\frac{\theta}{2}\right)}\beta,
\end{align}

(3.1)  (3.2)
As already mentioned in chapter 2, the continuous class-AB mode of operation is preferred in

![Figure 3.3 Variation of \( P_{\text{sat}} \) with continuous-mode parameter \( \beta \) for different frequencies. This demonstrates the effect of harmonic tuning on \( P_{\text{sat}} \) at various frequencies.](image)

our work because it has similar linearity performance as a classical class-AB PA. Impact of second
harmonic tuning on the performance of the PA can be demonstrated by varying \( \beta \). Fig. 3.3 and
Fig. 3.4 show the variation of \( P_{\text{sat}} \) and peak PAE with \( \beta \) for different frequencies. As expected, at
higher frequencies variation of \( \beta \) has less impact on \( P_{\text{sat}} \) and peak PAE. Around 28 GHz \( P_{\text{sat}} \) varies by
about 2 dB with \( \beta \), whereas around 70 GHz this variation reduces to 1 dB. The 12% points variation
in PAE with \( \beta \) is also more pronounced at 28 GHz compared to only 4% points at 70 GHz.

### 3.2 Harmonic matching network design

The matching network topology used in this work is shown in Fig. 3.5. This harmonic-tuning
technique has been proposed in [83] and has the benefit of decoupling the design of the harmonic
termination from the fundamental matching network. Specifically, the open-circuit stub \( T_q \) is
designed to be a quarter-wave long at the \( 2f_o \) frequency and ensures that the second-harmonic
Figure 3.4 Variation of PAE with continuous-mode parameter $\beta$ for different frequencies. This demonstrates the effect of harmonic tuning on PAE at various frequencies.

The impedance is not affected by the portion of the matching network to the right of $T_q$. The series transmission line $T_{se}$ can be used to tune the second-harmonic reactance to the optimum value, creating a second-harmonic termination which is near the edge of the Smith chart. This technique has been used in load-pull tuning instruments as well as some board-level PA designs, and then more recently in an integrated 28-GHz PA presented by the authors in [84].

Figure 3.5 Harmonic matching network

The fundamental matching network used in this work is a $\pi$-network as shown in Fig. 3.5.
This network is capable of transforming the load to an arbitrary complex fundamental impedance, sourcing the collector dc voltage with the shunt inductor and providing a dc block. The reason behind choosing a \( \pi \)-network instead of a traditional two-element matching network can be explained with the help of Fig. 3.7. In Fig. 3.7 the Smith chart is shown as partitioned into two regions by the conductance circle \( G = 1/R_L \) where \( R_L \) is the 50-\( \Omega \) load. Let \( Z'_{\text{opt}} = R_{\text{opt}} || jX_{\text{opt}} \) be the fundamental impedance needed at the SS' plane (Fig. 3.5) at the center frequency after de-embedding the passive elements to the left of SS'. When \( Z'_{\text{opt}} \) is inside the \( G = 1/R_L \) circle (Fig. 3.7(a)), which is the case in our design, a two element network consisting of shunt inductor \( L_3 \) and series capacitor \( C_2 \) would be incapable of sourcing the dc bias. Alternatively, we could consider another two element network by interchanging the positions of \( L_3 \) and \( C_2 \) i.e. shunt capacitor \( C_2 \) and series inductor \( L_1 \) but it would neither be capable of sourcing the dc bias nor providing a DC block. Thus we need the extra inductor \( L_1 \) as shown in Fig. 3.5 which results in a \( \pi \)-network. The additional element in a \( \pi \)-network also gives the flexibility of improving the bandwidth while maintaining the optimum match as described later in this section. When \( Z'_{\text{opt}} \) is outside the \( G = 1/R_L \) conductance circle (Fig. 3.7(b)), both two element (dashed and dotted line) and \( \pi \)-network (dotted black lines and solid colored lines) could be used for fundamental match.

The classical \( \pi \)-network design technique for matching between two resistive loads is well described in [3]; however, this technique is not suitable for our design due to several reasons. First, in some cases the traditional technique involves unnecessary transitions which increases the insertion loss. Second, this technique is intended for narrowband networks. To overcome these limitations, we present a modified design technique based on a simple virtual impedance. The design methodology incorporates commonly occurring layout parasitics line transmission line interconnects, passive loss and pad capacitance.

The fundamental matching network is redrawn in Fig. 3.6 showing a virtual impedance \( (Z_V = R_V + jX_V) \) and parasitic resistors representing losses of the passive components. In the traditional \( \pi \)-network design methodology, the load resistance is transformed to an intermediate virtual resistance which is then transformed to the source resistance. Also, the virtual resistance is restricted to
values lower than load and source resistances to achieve a narrowband network [3]. In our design technique we use a generalized virtual impedance for the intermediate match. By changing the virtual impedance we can easily modify the size, insertion loss and frequency response of the matching network.

In Fig. 3.7 we have compared networks designed by the traditional virtual resistance method (dashed lines) with the proposed virtual impedance method (colored solid lines) for two different $Z'_{\text{opt}}$. It is clearly observed that the virtual impedance method avoids unnecessary transitions across the $X=0$ line and also results in a larger, lower insertion-loss capacitor. Note that in Fig. 3.7(b), the parasitic series transmission lines $T_{p1}$ and $T_{p2}$ are necessary to achieve the match. Restrictions on the choice of virtual impedance and design equations for the $\pi$-network with finite Q-factor passives are presented in Appendix A.

To demonstrate the effect of virtual impedance on the performance of the network we present a 28 GHz design example. We assume $Z'_{\text{opt}} = 10 + j 12 \, \Omega$, $R_L = 50 \, \Omega$, $C_P = 46 \, \text{fF}$, $Q_{L1} = Q_{L3} = 20$, $Q_C = 15$, $L_{p1} = L_{p2} = 20 \, \text{pH}$, $Q_{L_{p1}} = Q_{L_{p2}} = 20$ for this example. Equations in Appendix A are used to determine the passive elements $L_1$, $C_2$ and $L_3$. Table 3.1 shows the value of network elements $L_1$, $C_2$ and $L_3$, the maximum gain ($G_{\text{max}}$) and the bandwidth of optimum match for a few virtual impedance values. The virtual impedances in the table are ordered by decreasing quality factor, $Q_V = X_V / R_V$. A few important conclusions can be drawn from this table which are helpful in optimizing the network for minimum power loss and/or wider bandwidth. Firstly, for certain virtual impedances, multiple
Figure 3.7 π-networks designed using virtual resistance (dotted lines) and virtual impedance (solid lines) method for $Z'_{\text{opt}}$ (a) inside the conductance circle $G = 1/R_L$ (b) outside the conductance circle $G = 1/R_L$. The dashed-cum-dotted line in (b) shows that a two-element network which is not possible in case (a) due to absence of DC feed or DC block. $Z'_{\text{opt}}$ is shown at center frequency only.
Table 3.1 Effect of virtual impedance on π-network performance

<table>
<thead>
<tr>
<th>Virtual Impedance ($Z_V$ in Ω)</th>
<th>$L_1$ (pH)</th>
<th>$C_2$ (fF)</th>
<th>$L_3$ (pH)</th>
<th>$G_{\text{max}}$ (dB)</th>
<th>Bandwidth (GHz)*</th>
</tr>
</thead>
<tbody>
<tr>
<td>12 + j20</td>
<td>540.1</td>
<td>396.3</td>
<td>124.1</td>
<td>-0.53</td>
<td>1.0</td>
</tr>
<tr>
<td></td>
<td>68.3</td>
<td>141.3</td>
<td>124.1</td>
<td>-1.5</td>
<td>1.0</td>
</tr>
<tr>
<td>20 + j20</td>
<td>312.9</td>
<td>355.3</td>
<td>139.4</td>
<td>-0.57</td>
<td>1.2</td>
</tr>
<tr>
<td></td>
<td>86.9</td>
<td>144</td>
<td>169.5</td>
<td>-1.6</td>
<td>3.4</td>
</tr>
<tr>
<td>20 + j10</td>
<td>190.7</td>
<td>289</td>
<td>165.7</td>
<td>-0.66</td>
<td>1.4</td>
</tr>
<tr>
<td></td>
<td>85</td>
<td>142.5</td>
<td>165.7</td>
<td>-1.27</td>
<td>3.0</td>
</tr>
<tr>
<td>25 + j2</td>
<td>129.4</td>
<td>211.5</td>
<td>191.6</td>
<td>-0.83</td>
<td>2.0</td>
</tr>
<tr>
<td></td>
<td>105.8</td>
<td>170.3</td>
<td>191.6</td>
<td>-1.0</td>
<td>2.9</td>
</tr>
<tr>
<td>25</td>
<td>104.35</td>
<td>167.9</td>
<td>190.8</td>
<td>-1.0</td>
<td>3.1</td>
</tr>
<tr>
<td>25 − j5</td>
<td>101.5</td>
<td>163.3</td>
<td>188.8</td>
<td>-1.05</td>
<td>3.4</td>
</tr>
</tbody>
</table>

* Bandwidth is defined as the frequency range for which the match to $Z'_\text{opt}$ is better than -30 dB

solutions exist for the network elements as can be seen in rows one to four of Table 3.1. In these cases, one of the solutions (highlighted) crosses the X=0 line during the impedance transformation (like the dashed trajectory in Fig. 3.7(a)) and has higher loss. Usually, the solution with higher loss also has improved bandwidth. If we assume that the network with highest $G_{\text{max}}$ is chosen whenever there are multiple solutions, then the bandwidth of the network is improved for lower quality factors of $Z_V$. This is also shown by the reflection coefficient plots on the Smith Chart in Fig. 3.8 from 23 GHz to 33 GHz with a reference impedance of $Z'_\text{opt}(\omega_0)$, where $\omega_0$ is the center frequency. For our 28 GHz PA, $Z_V = 20 + j10$ Ω is chosen to minimize insertion loss while maintaining an optimum match over 1.4 GHz.

3.3 Performance benefit of harmonic matching versus frequency

We now assess the impact of harmonic matching from 28 to 78 GHz for our SiGe BiCMOS 8HP technology with real back-end metalization (i.e., a seven-layer back-end-of-the-line with thick copper (MQ) and aluminum (LY, AM) top-level metals). A traditional two-element shunt L, series C network can provide an optimum fundamental impedance match; however, the second harmonic impedance would be far from optimum as observed from Fig. 2.2 and Fig. 2.11. Although the mi-
Figure 3.8 Impact of virtual impedance on bandwidth of optimum power match shown with plots of reflection coefficient $\frac{Z_{\text{opt}}(\omega)-Z_{\text{opt}}(\omega_0)}{Z_{\text{opt}}(\omega)-Z_{\text{opt}}(\omega_0)}$ from 23 to 33 GHz where $\omega_0$ is the center frequency.

crostrip stub-based harmonic matching network just presented can achieve both fundamental and second-harmonic match, it has extra passive components compared to a simple two-element LC matching network. With increasing frequency we expect that the higher insertion loss of the additional passive components would partially offset the performance benefit of the harmonic termination. As a result, we expect a "break-even" frequency where the additional efficiency enhancement provided by harmonic matching is offset by the additional insertion loss at the fundamental.

To estimate the relative benefit of harmonic matching with respect to simple LC fundamental matching we design a family of PAs with both types of networks optimized for frequencies ranging from 28 GHz to 78 GHz. A single-stage cascode PA with emitter length of 8.5 $\mu$m having three fingers was used for this comparison. The design equations provided in Appendix A are then used to obtain component values for the matching networks. For 28-38 GHz, inductors $L_1$ and $L_3$ are implemented as octagonal spirals in the top metal layer with patterned ground shield in the metal-1 plane. Above
38 GHz, inductors $L_1$ and $L_3$ are implemented as shorted microstrip transmission-line stubs with side shields. This choice was made to take advantage of the passive component models which exist in the SiGe-8HP design kit and thereby avoid the need to create a large family of custom-modeled inductors using an electromagnetic simulator. In SiGe 8HP, the diameter of the modeled spiral inductor is limited to 100 $\mu$m, thereby establishing a minimum modeled inductance of a single-turn spiral of about 130 pH (160 pH) at 28 GHz (60 GHz). Moving from spiral inductor to transmission lines causes a significant drop in Q-factor, for example, a 200-pH spiral inductor has a quality factor of 25 at 38 GHz whereas an equivalent short stub has a quality factor of 15.

Fig. 3.9(a) shows the simulated peak PAE of the harmonic matching network and the LC network for the family of PAs designed across 28 to 78 GHz. The harmonic matching network achieves about four percentage points higher peak PAE from 28 to 43 GHz and two to three percentage points higher peak PAE from 48-63 GHz. Fig. 3.9(b) compares the simulated $P_{sat}$ of the harmonic matching network and the LC network. The harmonic matching network achieves about a dB higher $P_{sat}$ compared to the LC network up to 68 GHz.

To probe further into the break-even frequency, we evaluate the impact of the loss in the transmission-lines used to realize the second-harmonic load. Fig. 3.10 shows the performance of the harmonic matching network when the series transmission line $T_{se}$ in the harmonic matching network (Fig. 3.5) has an improved attenuation constant of 0.1 dB/mm. Note that the attenuation constant of $T_{se}$ is 0.2-0.4 dB/mm in the frequency range of 28-78 GHz when a microstrip line form the design kit is used. With reduced loss of the series line $T_{se}$, PAE is further improved compared to the LC network up to 78 GHz. The plots show that harmonic matching can achieve significant improvement in PAE from 28 to 43 GHz and a modest improvement from 48 GHz to 68 GHz. Based on these results, we estimate the "break-even" frequency for harmonic-matched continuous-mode PAs in SiGe 8HP to be 68 GHz. Above this frequency, a traditional fundamental-frequency impedance match yields better results, whereas below this frequency, a harmonic matching network can result in improved $P_{sat}$ and improved PAE.
Figure 3.9 Simulated peak PAE and $P_{sat}$ of the harmonic matching network and the two element LC matching network versus frequency. Each point on the curve is a design optimized at the specific frequency.
Figure 3.10 Peak PAE of the harmonic matching network and the two element LC matching network with improved attenuation constant for $T_{se}$ (see Fig. 3.5)

Figure 3.11 Two-stage 28-GHz PA schematic, including component details.
3.4 IC design and measurements

To validate both our harmonic-matching methodology as well as our conclusions made with regards to the efficacy of harmonic matching networks over frequency, we have implemented two power amplifier prototypes, one at 28-GHz and the other at 60-GHz. Both employ microstrip harmonic matching networks and both have been implemented in GlobalFoundries SiGe BiCMOS 8HP technology.

3.4.1 28-GHz two-stage PA

A schematic of the 28-GHz two-stage PA is shown in Fig. 3.11. The PA is designed for 17-dBm $P_{1\mathrm{dB}}$ at 28-GHz to achieve about 29-dBm Effective Isotropic Radiated Power (EIRP) using an eight-element beamformer. We bias our driver PA in class-AB mode with a current density of 0.5 mA/µm to achieve greater than 15-dB gain and high PAE. The supply voltage is set to 3.6 V to allow high output voltage swing. Finally, device sizes are determined from the fundamental-frequency current amplitude using the procedure described in section 2.2. The driver stage transistors have 10-µm emitter length with four fingers. The output matching network is designed to achieve a target fundamental impedance of $65 + j25 \, \Omega$ and a second harmonic impedance of $-j62.5 \, \Omega$ using the methodology described in Section III. Inductors $L_1$ and $L_3$ were realized as spiral inductors with shielded ground planes.

A pre-driver stage is added for additional gain and to improve the $P_{1\mathrm{dB}}$ with a small (0.5 dB) gain expansion. The pre-driver transistors have 8.5-µm emitter length with two fingers to deliver sufficient RF power to the driver stage and dissipate less dc power. The supply voltage (2 V) is also scaled down compared to the driver stage (3.6 V). The inter-stage matching network has the same architecture as the output matching network. The fundamental impedance is optimized to achieve maximum pre-driver PAE with less than 1-dB gain variation in the 27 to 29-GHz frequency band. A die photo of the PA is shown in Fig. 3.12. Die size is 0.945 mm by 0.825 mm.

S-parameter measurement results of the 28-GHz PA are shown in Fig. 3.13. The PA achieves a peak 32-dB gain at 29 GHz and shows good correlation between simulation and measurement...
results. The swept-power measurement at 28 GHz is presented in Fig. 3.14. The PA has 17.6-dBm $P_{\text{sat}}$, 35.5% peak PAE, $+16.2$-dBm $O_{\text{1dB}}$, 34.7% PAE at 1-dB compression and 14% 6-dB back-off PAE with less than 0.5-dB gain expansion. Performance across the 27–29 GHz frequency band is summarized in Table 3.2. When comparing this result to our simulated results in Fig. 3.9a, we find that the harmonic matching was projected to provide 45% peak PAE, whereas our implemented PA achieves 35% peak PAE. About 5–6% point reduction is due to additional layout parasitics as visible
in the dotted red PAE plot in Fig. 3.14. The remaining 3–4% point reduction is due to small increase in passive loss and a pad model mismatch. The increased passive loss is due to unavailability of accurate data for conductivity of metal layers, substrate resistivity and dielectric loss tangent of insulators. With simulations it has been verified that if we incorporate layout parasitics and extra passive losses in both harmonic matching and LC networks, the harmonic tuned PA would still retain 3–4% point benefit in PAE at 28 GHz.

Linearity of the PA is assessed with both amplitude-modulation to phase-modulation (AM-PM) distortion and third-order intermodulation (IM3). As shown in Fig. 3.15, the PA has higher AM-PM distortion at 1-dB compression but at 3-dB back-off and lower power levels the AM-PM distortion is lower than 4°. A two-tone measurement presented in Fig. 3.16 shows that the PA has less than $-33$ dBc IM3 distortion product at 6-dB back-off.

### 3.4.2 60-GHz two-stage PA

A schematic of the 60-GHz two-stage PA is shown in Fig. 3.17. The PA is designed for 14-dBm $oP_{1dB}$ at 60-GHz to achieve about 29-dBm EIRP using a 16-element beamformer. The driver stage transistors
Figure 3.15 Measured AM-PM distortion measurement of the 28-GHz PA.

Figure 3.16 IM3 distortion measurement results of the 28-GHz PA with fundamental tones at 28 GHz (magnitude shown by the blue curve) and 28.017 GHz.
Table 3.2 Performance summary of the 28-GHz PA

<table>
<thead>
<tr>
<th>Frequency (GHz)</th>
<th>27</th>
<th>28</th>
<th>29</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain (dB)</td>
<td>29.2</td>
<td>30.9</td>
<td>31.7</td>
</tr>
<tr>
<td>( P_{\text{sat}} ) (dBm)</td>
<td>17</td>
<td>17.6</td>
<td>17.5</td>
</tr>
<tr>
<td>( P_{\text{1dB}} ) (dBm)</td>
<td>15.6</td>
<td>16.2</td>
<td>15.3</td>
</tr>
<tr>
<td>Peak PAE (%)</td>
<td>32.4</td>
<td>35.5</td>
<td>35.7</td>
</tr>
<tr>
<td>PAE 1-dB comp. (%)</td>
<td>32.4</td>
<td>34.7</td>
<td>32.1</td>
</tr>
<tr>
<td>PAE 6-dB-back-off (%)</td>
<td>13.6</td>
<td>14</td>
<td>12.9</td>
</tr>
</tbody>
</table>

have 8.5\( \mu \text{m} \)-long emitter with three fingers. The output matching network is designed to achieve a target fundamental impedance of \( 80 + j15\Omega \) and a second-harmonic impedance of \(-j50\Omega \) using the methodology described in Section 3.2. Inductors \( L_1 \) and \( L_3 \) were realized as microstrip transmission lines with side shields.

**Figure 3.17** Two stage 60-GHz PA schematic
The pre-driver stage transistors have 8.5 µm-long emitter with single finger. The inter-stage matching network needs to transform a low impedance at the driver input \( (Z_{\text{dri-in}} = 12 - j6 \Omega) \) to a high impedance \( (Z_{\text{pre-opt}} = 200 + j100 \Omega) \) at the pre-driver output. The harmonic network described in Section III is not adequate to maintain low gain variation across our target band of 57–66 GHz. To achieve this impedance transformation with a broadband performance, we start with the basic three-element \( \pi \)-network shown in Fig. 3.18(a) and modify it in two steps. The \( \pi \)-network can source the bias for the pre-driver collector and driver base and provide dc isolation between the stages; however, the series capacitor \( C_2 \) (50 fF) is small to achieve the big impedance transformation. This makes the network lossy and narrow band. In the second network topology Fig. 3.18(b) the \( \pi \)-network transforms \( Z_{\text{dri-in}} \) to an intermediate resistance of approximately 35 Ω. Transformation from this intermediate resistance to \( Z_{\text{pre-opt}} \) is achieved using a 500 µm-long, 6 µm-wide series transmission line TL3. The bandwidth improves but due to the thin transmission line, insertion loss is still high. Using a T-network of transmission lines (Fig. 3.18(c)) instead of a single transmission line allows the series transmission lines to be thicker. The final interstage network thus achieves a low gain variation of 0.7 dB in 57–66 GHz band as well as low insertion loss of 2 dB. A die photo of the PA is shown in Fig. 3.19. Die size is 0.837 mm by 0.482 mm.

S-Parameter measurement results of the 60-GHz PA are shown in Fig. 3.20. The PA achieves 20-dB peak gain at 64-GHz. Gain variation is less than 2-dB from 55–66 GHz. Small deviation in measured \( S_{11} \) and \( S_{21} \) from simulation is due to in situ measurement of the PA, where the amplifier was measured while embedded within a transmitter; hence, the previous stage's off-state capacitance loads the input of the PA. A swept-power measurement result at 58 GHz is presented in Fig. 3.14. The PA has 18.7-dB gain, +15.4-dBm \( P_{\text{sat}} \), 25.3% peak PAE, +13.3-dBm \( O_{1\text{dB}} \), 25% PAE at 1-dB compression and 9% 6-dB back-off PAE with less than 0.5-dB gain expansion. Performance across the 58-64 GHz frequency band is presented in Table 3.3. The PAE shows an increased variation across the frequency band compared to simulations. This is due to an estimated 0.2–0.4 dB of de-embedding error during measurements at the output of the PA.
Figure 3.18 Interstage matching network design for the 60-GHz PA.

Figure 3.19 Two stage 60-GHz PA die photo (837 µm by 482 µm, including RF pads).
Figure 3.20 S-Parameter simulation (dashed) and measurement (solid) results of the 60-GHz PA.

Figure 3.21 Swept power simulation (dashed) and measurement (solid) results of the 60-GHz PA.
Table 3.3 Performance of the 60-GHz PA across band

<table>
<thead>
<tr>
<th>Frequency (GHz)</th>
<th>58</th>
<th>60</th>
<th>62</th>
<th>64</th>
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<tbody>
<tr>
<td>Gain (dB)</td>
<td>18.7</td>
<td>18.5</td>
<td>19.7</td>
<td>20</td>
</tr>
<tr>
<td>$P_{sat}$ (dBm)</td>
<td>15.4</td>
<td>14.2</td>
<td>14.4</td>
<td>14.2</td>
</tr>
<tr>
<td>$oP_{1dB}$ (dBm)</td>
<td>13.3</td>
<td>12.8</td>
<td>12.8</td>
<td>11.3</td>
</tr>
<tr>
<td>Peak PAE (%)</td>
<td>25.3</td>
<td>18.3</td>
<td>20.3</td>
<td>20.4</td>
</tr>
<tr>
<td>PAE 1-dB comp. (%)</td>
<td>25</td>
<td>17</td>
<td>19.5</td>
<td>17</td>
</tr>
<tr>
<td>PAE 6-dB-back-off (%)</td>
<td>9</td>
<td>7.2</td>
<td>7.8</td>
<td>7</td>
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</table>

3.5 Conclusion

In this chapter, the efficacy of harmonic tuning was investigated over a wide range of millimeter-wave frequencies. Harmonic generation by the active device and optimum continuous-mode operation were studied versus frequency. We presented a network topology that is capable of achieving an arbitrary fundamental and second-harmonic impedance termination and showed techniques to optimize this network including a virtual-impedance based design technique for a $\pi$-network. PA designs from 28 to 78 GHz were evaluated to show that optimum second-harmonic termination improves PAE by 3-5% points from 28-43 GHz and about 2% points from 48-68 GHz. The break even frequency above which second-harmonic termination provides no additional performance benefit was established as 68 GHz. We verified these assertions by two-stage PA designs at 28-GHz and 60-GHz which achieve high peak and back-off PAE. The 60-GHz PA also achieves broadband gain. Performance comparison of the 28-GHz and 60-GHz PA with state of the art designs is shown in Tables 3.4 and 3.5. The 28-GHz PA achieves comparable peak and back-off PAE as the result in [60] with about a dB higher $oP_{1dB}$. The 60-GHz PA achieves one of the highest back-off PAE among all published PAs in V-band.

Impact of harmonic tuning versus frequency could also be investigated for Class-E, Class-F and inverse Class-F PAs in future. These PA modes would also show reduced impact of harmonic tuning.
with higher frequency due to reduction of the second and third harmonic voltage or current and increased passive losses. Further, Class-F and inverse Class-F PAs would need an additional passive components to tune the third harmonic impedance. These additional passive components would result in a bigger impact of passive loss on the Class-F or inverse Class-F PA performance versus frequency compared to continuous Class-AB mode PAs. Class-E mode PAs are usually realized with a fixed network architecture independent of the number of harmonics being tuned [62, 71]. However, the relative benefit of harmonic tuning over simple fundamental match and the break-even frequency for Class-E and Class-F PAs would be different from continuous Class-AB mode PAs because of different harmonic impedances and network topologies.

### Table 3.4 Performance comparison of the 28-GHz PA with Ka and Q-band Power Amplifiers.

<table>
<thead>
<tr>
<th>Reference</th>
<th>Frequency (GHz)</th>
<th>Architecture</th>
<th>Gain (dB)</th>
<th>Psat (dBm)</th>
<th>oP1dB (dBm)</th>
<th>Peak PAE (%)</th>
<th>PAE at 6-dB-back-off (%)</th>
<th>Technology</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>This work</strong></td>
<td>27-29</td>
<td>Continuous Class-AB</td>
<td>30.9</td>
<td>17.6</td>
<td>16.2</td>
<td>35.5</td>
<td>14</td>
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* Estimated from swept power plots
† Could not be estimated due to excessive gain expansion
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* Estimated from swept power plots. ** DAT=Distributed Active Transf. † Could not be estimated due to excessive gain expansion.
4.1 Introduction

Harmonic tuning techniques presented in Chapters 2 and 3 achieve maximum PAE improvement near 1-dB compression point and retain some of the benefit up to 6-dB back-off. Unfortunately, high PMEPR modulation schemes like OFDM which are preferred due to their spectral efficiency need to operate at 6-7 dB back-off even after the application of some PMEPR mitigation techniques. Several techniques have been proposed to improve the efficiency of PAs operating with high PMEPR signals [71]. Among these techniques, the Doherty PA is particularly suited for multi-Gbps modulating signals used in millimeter-wave communication systems. Smaller passive components at millimeter-wave are also beneficial for the Doherty architecture. However, the few millimeter-wave Doherty PAs that have been published so far do not display significant improvement in back-off efficiency compared to simple Class-AB PAs. We begin this chapter with a brief overview of the basic Doherty
operation and the non-idealities in a practical implementation. We then investigate some of the key design choices and trade-offs in millimeter-wave Doherty operation to understand the subpar performance of millimeter-wave Doherty PAs. These include multistage architecture choice, benefits and limitations of harmonic tuning, trade-offs in design of the peaking PA and output combiner choice. To demonstrate the benefit of Doherty operation, we fabricate and characterize a 60-GHz Doherty PA with 2-stage carrier and peaking PAs. Measurement results would show significant improvement in back-off efficiency compared to the harmonic-tuned two-stage 60-GHz PA presented in Chapter 3 as well as state-of-the art PAs in literature.

### 4.2 Basic Doherty PA operation

![Doherty PA block diagram](image.png)

Figure 4.1 Doherty PA block diagram.

Block diagram of the Doherty PA is shown in Fig. 4.1. The operation can be explained in brief as follows. An optimally designed class-AB PA has maximum voltage and current amplitudes near 1-dB compression point. At backed-off power levels both the current and voltage swings are smaller. The collector dc voltage is chosen such that the maximum negative voltage swing at 1-dB compression point does not clip the sinusoidal voltage waveform (or in other words doesn't drive the bipolar
transistors into saturation region). At back-off power levels, the collector dc voltage required to
maintain a sinusoidal unclipped voltage waveform is smaller compared to that at 1-dB compression
due to smaller voltage amplitude. Hence there is a wastage of dc power. To improve the efficiency
one has to either dynamically change the supply voltage or the load impedance at the backed-off
power levels. The Doherty PA takes the later approach. The carrier PA in the Doherty block diagram
is a class-AB PA. A class-C peaking PA is introduced which ideally has zero current (and voltage)
amplitude near 6-dB backed-off power levels. As input power is increased beyond the 6-dB back-
off, the peaking PA turns on delivering additional current to the load. Due to increased voltage
swing at the load terminal and the impedance inversion characteristic of the quarter wave line,
the impedance seen by the carrier PA is reduced. At 1-dB compression, the peaking PA has same
current amplitude as the carrier PA; thus, the impedance seen by the carrier PA is half of that at 6-dB
back-off. Due to this load modulation characteristic, the voltage swing of the carrier PA remains
constant in the 6-dB back-off regime as shown in Fig. 4.2(b). The current amplitudes for varying
levels of input power are shown in Fig. 4.2(a).

The real characteristics of the class-C peaking PA cause a big discrepancy between the perfor-
mance of the ideal Doherty PA and the actual implementation. The class-C PA does not have the
ideal turn on characteristic shown in Fig. 4.2(a). One of the problems is the non-zero current at 6-dB
back-off power level which impacts dc power consumption as well as the load modulation charac-
teristic. The class-C PA current amplitude response from back-off to 1-dB compression cannot be
precisely controlled as shown in Fig. 4.2(a) by tuning the bias current density. Further, the class-C
PA shows increased AM-PM distortion as its current density is reduced which further restricts the
ability to control the turn-on characteristic of the peaking PA.

Another deviation from the ideal Doherty operation arises from the fact that at 6-dB back-off
and lower power levels the impedance looking into the peaking PA is not infinite as assumed in
the ideal Doherty operation. Thus, the carrier PA leaks some power into the peaking PA at back-off
power levels reducing the improvement in back-off PAE as proposed in the ideal Doherty PA theory.
At millimeter-wave frequency this effect is more pronounced due to lower quality factor of passive
Figure 4.2 Ideal Doherty PA a) Current Amplitudes b) Voltage Amplitudes of Carrier and Peaking PAs.

4.3 Millimeter-wave Doherty PA design considerations

Overall architecture and circuit-level techniques for optimum Doherty operation at millimeter-wave frequencies are presented in this section. First, multi-stage Doherty architectures are presented and trade-offs between size, power consumption, bandwidth, design complexity, and flexibility are discussed. Impact of harmonic tuning in carrier PA on Doherty efficiency and bandwidth is presented next. Peaking PA design considerations including choice of bias current density and output matching network design are presented and their impact on overall Doherty PA performance is discussed. Finally, output combiner choices are presented and trade-off between area and insertion-loss is discussed. Apart from the techniques presented in this section, the broadband inter-stage network design method presented in section 3.4.2 is used in both carrier and peaking PAs.
4.3.1 Multistage architecture selection

The 60-GHz Doherty PA in this work targets a 3-dB higher \( P_{1dB} \) (17 dBm) compared to the two-stage PA presented in Chapter 3 in addition to back-off efficiency improvement. Due to low \( P_{1dB} \) of active phase shifters [87] and high loss in passive phase shifters [12], the Doherty PA targets a high gain of 20 dB to be linearly driven by the preceding stages. Single-stage PAs at 60-GHz can achieve about 13-dB gain as discussed in Chapter 3, so we need a multi-stage design to achieve our gain target. Possible multi-stage Doherty architectures are shown in Fig. 4.3. The first architecture shown in Fig. 4.3(a) has a two-stage carrier PA and a single-stage peaking PA. Compared to the other two topologies, this one has lower power consumption in the pre-driver stage. However, the asymmetrical carrier and peaking PA paths have very different phase shifts hence additional offset lines are needed for phase compensation. Offset lines increase the overall size of the PA and cause additional power loss. Further, the compensation is narrow-band and is difficult to achieve because the phase shift between the two paths can vary with the input power. One other drawback of this architecture can be observed if we consider driving the carrier and peaking PAs with two independent RF inputs coming from two separate phase shifters. In that case, the peaking PA path would not have sufficient gain. The second Doherty PA shown in Fig. 4.3(b) uses a single pre-driver to drive both the carrier and peaking PAs. This PA also suffers from the drawback that it does not allow the flexibility of being driven with two independent RF inputs. The interstage matching network design is also more complicated since it needs to include a power splitter.

In this work the Doherty PA shown in Fig. 4.3(c) is adopted because the carrier and peaking could be driven by two phase shifters. Such a flexible arrangement allows for independent amplitude and phase adjustment of the carrier and peaking PA paths. Further, the 90 degree hybrid coupler can also be eliminated if the phase shifters are adjusted to have quadrature outputs. Having a separate pre-driver for the peaking path allows operation with further reduced conduction angle compared to the Doherty PA in Fig. 4.3(b) because the small signal gain is unaffected by the peaking PA path.
4.3.2 Harmonic tuning in Carrier PA

The two-stage PA presented in Chapter 3 has a 19-dB small signal gain and 14-dBm oP_{1dB}, and is adopted as the carrier PA of the Doherty. One key consideration for the carrier PA is whether the driver output match should be just a fundamental match or a harmonic match. As noted in Chapter 3, the harmonic tuned PA would improve the peak PAE of the carrier PA by an additional 2% points. However, the harmonic tuned network has a few limitations. Firstly, use of a quarter-wave resonator based harmonic tuning network in the carrier PA creates additional phase offset between the carrier PA and the peaking PA paths. This is based on the fact that the peaking PA uses a simple LC network as explained in the next section. While an offset line could be used to compensate for this phase difference, the compensation would not be broadband. In a Doherty PA the quarter-wave transformer already introduces some performance variation across the frequency band. Use of the harmonic matching network worsens this performance variation across the band. To make this point clearer, in Fig. 4.4 we have shown the phase shifts of the quarter-wave transformer, quarter wave transformer with LC matching network and quarter wave transformer with harmonic matching network. It could be observed that the harmonic matching network causes a larger phase variation
Figure 4.4 Comparison of phase shifts of quarter-wave line, LC output matching network with quarter-wave line, harmonic output matching network with quarter-wave line.

across the frequency band. One other limitation of the harmonic matching network is the increased area. In view of these disadvantages we opted for a simple LC network for the carrier PA.

4.3.3 Peaking PA trade-offs

The peaking PA has a similar design as the carrier PA. Specifically, the pre-driver and driver stages are cascode amplifiers with same device sizes of 8.5umx1 (emitter length * number of fingers) and 8.5umx3 as the carrier PA. The inter-stage matching network is also same as the carrier PA. Class-C operation of the peaking PA is achieved by operating the pre-driver and driver stages of the peaking PA at current densities of 0.09 mA/um and 0.17 mA/um. AM-AM response of the peaking PA under reduced bias current densities of the pre-driver and driver stages is shown in Fig. 4.5. It can be observed that for lower current densities the AM-AM response has excessive gain expansion which would severely degrade the linearity of the PA. This puts a lower limit on the standby current of the peaking PA. We choose pre-driver and driver stage current densities such that the power gain expansion of the peaking PA is about 3-4 dB based on the theory presented in [71, Ch. 10, p. 292]. It has been shown in [71] that the carrier PA would undergo 3-dB gain compression in the load
modulation region (6-dB back-off to 1-dB gain compression of the Doherty PA) which dictates that
the peaking PA should have a similar gain expansion in that region.

![Graph showing swept power gain of the peaking PA for different current densities.]

**Figure 4.5** Swept power gain of the peaking PA for different current densities.

One other important trade-off in the peaking PA is the design of the output matching network. To maximize the peaking PA peak efficiency we need to present an impedance of $75 + j16\ \Omega$ which was determined from a load pull analysis. On the other hand at 6-dB back-off and lower power levels the impedance looking into the peaking PA ($Z_{\text{peak-o}}$ in Fig. 4.1) should be high and ideally infinite so that the carrier PA does not leak power into the peaking PA path. Using a LC network at the output the maximum $|Z_{\text{peak-o}}|$ we can achieve is about 300 $\Omega$. This value is limited by the Q-factor of the shunt inductor TL10 (Fig. 4.9) in the LC network. To demonstrate this, we have shown the variation of $Z_{\text{peak-o}}$ in Fig. 4.6 with the Q-factor of the shunt inductor TL10. In SiGe 8HP technology the inductor Q is limited to about 12 at 60-GHz causing a 3-4% points degradation in PAE compared to an ideal inductor. When the LC network is tuned to maximize $Z_{\text{peak-o}}$, the load impedance seen by the device is $51 + j29\ \Omega$ instead of the optimum value of $75 + j16\ \Omega$ which decreases the peak PAE of the peaking PA by 2.6% points. However, the impact on the overall Doherty efficiency is low because
the peak PAE of the Doherty PA is a weighted function of the peak PAEs of carrier and peaking PAs.

Figure 4.6 Variation of output impedance looking into the peaking PA with inductor quality factor.

4.3.4 Output combiner choice

Output combiner design of the Doherty PA involves a trade-off between area, insertion loss, bandwidth and robustness. Some possible combiner choices are shown in Fig. 4.7. In this work, we mainly emphasized on reducing both the insertion loss of the combiner and the sensitivity to parasitic impedances. A quarter-wave line with characteristic impedance of $50 \, \Omega$ using the top level AM metal has a low insertion loss of $0.25 \, \text{dB}$ at 60 GHz in SiGe 8HP technology. The quarter-wave line combiner, however, is $600 \, \mu\text{m}$ long and is area-inefficient. A left handed $\pi$-network shown in Fig. 4.7(b) is more compact, however the insertion loss of the network is increased to $0.8 \, \text{dB}$ which reduces the efficiency of the Doherty PA. Finally, a highly compact transformer based series combiner for Doherty PA was also proposed in [69] (Fig. 4.7(c). However, transformer-based series combiners suffer from impedance imbalance problems as mentioned in [47]. Further, series combining transforms the output 50-Ohm load into a lower resistance. This could be beneficial for CMOS PA designs which
need low optimum impedances at the device plane. For the SiGe PAs in our work the optimum impedance required at the devices is higher than 50 Ω, so the series combiner is not suitable for our work. Further series combiners have an insertion loss of about 1 dB which degrades the peak PAE. Hence, in our work we use the quarter-wave impedance transformer for power combining owing to its low insertion loss. The quarter-wave line is meandered to save area. We use a 55-Ω characteristic

![Quarter-wave line schematic](image)

**Figure 4.7 Doherty Combiner choices**

impedance for the transmission line so that the impedance seen by the carrier PA at the quarter wave line input is 60 Ω.
Figure 4.8 Doherty Carrier PA.

Figure 4.9 Doherty Peaking PA.
4.4 Measurement Results

Details of the carrier and peaking PA are shown in Fig. 4.8 and Fig. 4.9. The die photo of the Doherty PA is shown in Fig. 4.10 and the chip size is 1.37 mm by 0.96 mm including pads. S-parameter measurement results are presented in Fig. 4.11. The PA has 17 to 19 dB gain in 57–66 GHz band and 3-dB bandwidth greater than 12 GHz. Impact of the broadband inter-stage network design presented in chapter 3 for the carrier PA can be observed in these measurements. $S_{11}$ is somewhat reflective because the input match was tuned for a preceding phase shifter stage in a full beamformer design. The breakout chip is measured with 50-Ω input and output impedances. Overall S-parameters show good model-to-hardware correlation. Swept-power measurement results at 62-GHz are shown in Fig. 4.12. The PA has 17.5-dBm $O_{1dB}$, 23.9% peak PAE, and 13.8% 6-dB back-off PAE at 62 GHz. The 6-dB back-off PAE exceeds that of all PAs published at 60-GHz by 3–4 percentage points. Performance across the frequency band is presented in Table 4.1. A low $O_{1dB}$ and PAE variation across the frequency band is achieved owing to the design choices made in Section 4.3.

Due to equipment limitations linearity measurements could not be performed at this time. EVM
Figure 4.11 Measured S-Parameters of the Doherty PA

Figure 4.12 Swept power measurements of the Doherty PA
Table 4.1 Performance of the 60-GHz Doherty PA across band

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simulation results of the Doherty with a 2-Gbps, 16-QAM 13-dB PAPR OFDM signal is shown in Fig. 4.13. With average input power set at 7-dB back-off, the EVM is -23.4 dB (6.7%).

4.5 Conclusion

In this chapter we identified and investigated some of the critical steps in realization of a millimeter-wave Doherty PA. We evaluated multi-stage architectures based on their power consumption, bandwidth, reconfigurability and ease of implementation. A Doherty PA with two-stage carrier amplifier path and two-stage peaking amplifier path was adopted due to its symmetrical structure and the possibility of amplitude and phase reconfigurability along the carrier and peaking paths. Simple fundamental match for carrier PA was preferred over harmonic-tuned network due to its relatively broadband performance. Peaking PA trade-offs and their impact on Doherty operation was investigated. Impact of the peaking PA bias current density on standby DC power consumption and gain expansion of the overall Doherty PA was demonstrated and the bias current density was chosen to complement the gain compression characteristic of the carrier PA. The peaking PA output network was designed for high impedance instead of optimum power match to prevent power leakage from the carrier PA into the peaking PA network under backed-off conditions. Output combiner choices including a quarter-wave combiner, a $\pi$-network equivalent of quarter-wave combiner,
Figure 4.13 Simulated EVM of the Doherty PA
Table 4.2 Performance comparison of the Doherty PA with other V-band Power Amplifiers and millimeter-wave Power Amplifiers

<table>
<thead>
<tr>
<th>Reference</th>
<th>Frequency (GHz)</th>
<th>Architecture</th>
<th>Gain (dB)</th>
<th>Psat (dBm)</th>
<th>oP1dB (dBm)</th>
<th>Peak PAE (%)</th>
<th>PAE at 6-dB-backoff (%)</th>
<th>Technology</th>
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* Estimated from swept power plots. ** DAT = Distributed Active Transf. † Could not be estimated due to excessive gain expansion.
and a transformer-based series combiner were evaluated in the context of millimeter-wave and SiGe Doherty PAs in terms of area and insertion loss and the quarter-wave combiner was adopted because of its low insertion loss. Also, the broadband inter-stage network design method presented in section 3.4.2 was used for carrier and peaking PA chains. Importance of these techniques are demonstrated with the successful implementation of a 60-GHz Doherty PA which has 18-dB gain, 17.5-dB $oP_{1dB}$, 23% peak PAE and a record 13.5% 6-dB-back-off PAE and consistent performance across 57-64 GHz band.

Comparison with prior art is shown in Table 4.2. The Doherty-PA exceeds reported back-off PAEs in literature by at least 3% points. In addition, our design techniques result in lower gain, $oP_{1dB}$ and PAE variation across 58-64 GHz compared to other designs. Thus, our Doherty PA has the potential to reduce the power consumption of linear phased array transmitters significantly.
5.1 Introduction

In chapter 2 and 3 we presented techniques for high-efficiency PAs with $\text{oP}_{1\text{dB}}$ of around 16 dBm (14 dBm) at 28 GHz (60 GHz) also demonstrating good linearity. In chapter 4, we investigated a Doherty PA which showed a 3-dB increase in $\text{oP}_{1\text{dB}}$ with a significant improvement in back-off.
PAE as well. It was also mentioned that assessment of linearity of the Doherty PA is not possible at this time due to equipment limitations, however, it is clear from existing PA literature [71] that the Doherty PA has worse linearity compared to a class-AB PA. For stringent linearity requirements, a preferred way to improve \( \text{O}_{1\text{dB}} \) is to combine the output power of unit class-AB PAs. This chapter investigates efficient power combining techniques for millimeter-wave class-AB PAs. One of the main motivations for increasing the output power per beamformer element that was discussed in chapter-1 is the reduction in the number of elements in the beamformer which can lead to a lower cost for a fixed EIRP. Also, for a fixed number of elements in the beamformer, the EIRP could be improved, leading to an increased link distance or data rate. Finally, higher packaging losses at millimeter-wave frequencies also demand increased \( \text{O}_{1\text{dB}} \) per beamformer element.

Single-transistor and cascode PAs in SiGe and CMOS technologies have demonstrated 15-18 dBm \( \text{O}_{1\text{dB}} \) with 30-40% peak PAE [61, 76, 84] at 28 GHz. To improve the output power we could use larger devices, but the higher impedance transformation ratio and increased parasitics reduce the gain and the bandwidth of the PA. For multi-finger bipolar devices unequal current and temperature profiles across the fingers is also a limitation, leading to ballasting. Another technique that has been commonly used in silicon-on-insulator (SOI) CMOS technologies [52, 53] and sometimes in SiGe [62] technologies is stacking two or more devices to allow increased voltage swing. The limitations of this technique are reduced gain and linearity [54]. Alternatively, transformer-based series-parallel combined PAs can achieve higher output power while maintaining the same linearity as the unit PA [54]. For two to eight-way power combining, the increase in die area of the PA is also minimal because some of the matching elements present in the unit PA can be absorbed into the power combiner structure.

Prior work on series and series-parallel power combined PAs have presented optimization of the transformer structure [70], comparison between series and parallel combining architectures [47, 50, 54, 88] and choice of combiner architecture based on the transformed load [50, 54]. In this work, we present a methodology to co-optimize the transformer structure with adjoining matching elements to minimize the insertion loss of a two-way series two-way parallel power combiner. Our
methodology uses a lumped-element model for this optimization procedure and does not require full 3-D Electromagnetic (EM) simulations. This is in contrast to existing design methodologies for series-parallel power combiners [47, 50, 54, 88] where optimization of just the transformer structure has been considered requiring extensive EM simulations. Inclusion of a matching network in this methodology also enables the possibility of realizing a broader range of impedances at the device plane compared to existing work. The efficacy of this methodology is demonstrated by the simulated and measured $\text{OP}_{1\text{dB}}$ and PAE. The measured $\text{OP}_{1\text{dB}}$ and PAE are within 0.8 dB and 3% points of an ideal combiner. Measured results also show high gain and excellent linearity.

5.2 Combiner optimization

Among multi-way power combining architectures, hybrid power combiners provide excellent isolation but occupy a large die area and have a large insertion loss at 28 GHz. In this work we focus on transformer-based series and series-parallel combiners which have dimensions much smaller than $\lambda/4$ and less than 1-dB insertion loss at millimeter-wave frequencies [39, 54, 70]. In prior work on series-parallel power combined PAs [47, 50, 54, 88], selection of optimum number of series and parallel stages and selection of optimum transformer dimensions [54] has been emphasized. It has been demonstrated that the loss of the transformer could be minimized versus diameter [70] for a fixed trace width. However, if we optimize the transformer with the sole objective of minimizing its power loss, the impedance presented by the combiner to the device may be far from the optimum impedance for PAE. In that case, the loss incurred due to additional matching elements could become significant. Hence the transformer structure needs to be co-optimized with adjoining matching elements to minimize the overall loss of the combiner network. Further, optimization of the full combiner structure including matching elements in a 3-D EM simulator is time consuming and not intuitive. In this work, we present a methodology to co-optimize the transformer with adjoining matching elements with the aid of a lumped-element transformer model for a two-way series two-way parallel combiner (Fig. 5.1(a)). This co-optimization is performed to minimize the loss of the network while providing the optimum impedance ($Z_{\text{opt}}$) to the devices for maximum PAE.
Our main goal is to express the loss of the full network i.e. the transformer and matching elements as a function of the transformer diameter.

To design and co-optimize the combiner and the matching network, we use the simplified schematic shown in Fig. 5.1b. It includes the transformed load resistance $R_{LT} = R_L \times (M/K)$ and the transformed pad capacitance $C_{PT} = C_p \times (K/M)$, where $M (>1)$ is the number of parallel combining stages and $K (>1)$ is the number of series combining stages. Other components of the schematic include an output series inductor $L_o$, a vertically coupled 1:1 turn ratio transformer, an input series inductor $L_i$, and a shunt capacitor $C_T$. The series inductor $L_o$ represents the inductance of output feed line plus the inductance of the transmission line used in the parallel combiner. $L_i$ represents the inductance of the input feed line between the device and the transformer. $C_T$ represents any shunt capacitance at the device terminal excluding the transistor's internal capacitance. The transformer is represented by a shunt magnetizing inductance $L_m$, a shunt parasitic capacitor $C_s$ and two series leakage inductances $L_{s1}$ and $L_{s2}$. In the actual optimization procedure the transformer elements $L_m, C_s, L_{s1}$, and $L_{s2}$ are replaced by a lumped model.
The impedance transformation trajectory from $R_{LT}$ to $Z_{opt}$ could be determined using Fig. 5.2. If $Z_{opt}$ is outside the conductance circle $G = 1/R_{LT}$, which is the case in this design, then $L_m$, $L_i$ and $C_T$ are used for impedance transformation (Fig. 5.2(a)), while rest of the components are fixed. On the other hand, if $Z_{opt}$ is inside this circle, $L_o$, $C_{PT}$ and and $L_m$ could be used for impedance transformation, and other components are fixed (Fig. 5.2(b)). To meet our $\text{OP}_{1\text{dB}}$ target of 23-dBm, we prefer a two-way series two-way parallel ($K=2,M=2$) power combiner over a four-way series combiner ($K=4,M=1$). This choice could be understood with the help of Fig. 5.2(a) which indicates that due to a smaller $R_{LT}$ in case of a four-way series combiner, $Z_{opt}$ is further out from the $G = 1/R_{LT}$ conductance circle compared to a two-way series two-way parallel combiner. Thus, a bigger series inductor $L_i$ is necessary for impedance transformation increasing the insertion loss of the network when using a four-way series combiner.

The impedance looking into the transformer ($Z_T$) can be expressed as a function of transformer’s external diameter ($d_{\text{ext}}$) for a fixed trace width of the transformer and for fixed parasitic components $L_o$ and $C_{PT}$. For a desired $Z_{opt}$, the matching components can be calculated as:

\[
R_L\frac{M}{K}\frac{Z_{opt}}{3}451 C_{PT} \text{ (parasitic)} \quad 2 \quad L_o \text{ (parasitic)} \quad 3 \quad L_m || C_s \text{ (matching/parasitic)} \quad 4 \quad L_i \text{ (parasitic)} \quad 5 \quad C_T \text{ (parasitic)}
\]

\[
R_L\frac{M}{K}\frac{Z_{opt}}{13}451 C_{PT} \text{ (matching)} \quad 2 \quad L_o \text{ (matching)} \quad 3 \quad L_m || C_s \text{ (matching/parasitic)} \quad 4 \quad L_i \text{ (parasitic)} \quad 5 \quad C_T \text{ (parasitic)}
\]

**Figure 5.2** Determination of the impedance transformation network, matching and parasitic elements based on the location of optimum impedance $Z_{opt}$ (a) $Z_{opt}$ outside the conductance circle $G=1/(RL^*M/K)$ (b) $Z_{opt}$ inside the conductance circle $G=1/(RL^*M/K)$. 
\[ L_i = \frac{1}{\omega} \left( \sqrt{R_{\text{optP}} \Re[Z_T(d_{\text{ext}})] - \left(\Re[Z_T(d_{\text{ext}})]\right)^2} - \Im[Z_T(d_{\text{ext}})] \right) \]  

\[ C_T = \frac{1}{\omega} \left( \frac{\sqrt{R_{\text{optP}} \Re[Z_T(d_{\text{ext}})] - \left(\Re[Z_T(d_{\text{ext}})]\right)^2}}{\Re[Z_T(d_{\text{ext}})] R_{\text{optP}} X_{\text{optP}}} \right) \]  

for lossless passives, where \(R_{\text{optP}}||X_{\text{optP}}\) is the parallel equivalent of \(Z_{\text{opt}}\). Since the elements \(Z_T\), \(C_T\) and \(L_i\) are functions of \(d_{\text{ext}}\), the maximum gain \(G_{\text{max}}\) of the network in Fig. 5.1(b) can also be expressed as a function of \(d_{\text{ext}}\). In this work, \(G_{\text{max}}\) of a two-way series two-way parallel combiner has been numerically calculated as a function of \(d_{\text{ext}}\) using a lumped element model of the transformer and equations for lossy matching components \(C_{P\text{T}}\) and \(L_{\text{s1}}\) presented in Appendix B.

The lumped model used for the transformer is shown in Fig. 5.3 and was proposed in [70]. Most of the parameters of the model have been calculated using analytical equations presented in [70] and [89], whereas others have been fit to EM simulations. Agreement of the lumped model with 3-D EM simulations is shown in Fig. 5.4 for diameters ranging from 100 \(\mu\text{m}\) to 220 \(\mu\text{m}\). Using this model,
the required matching element values $C_{PT}$ and $L_i$ are calculated with the help of equations B.1 and B.2 for our target $Z_{opt}$ of $28 + j32$. Fig. 5.5(a) shows the $G_{max}$ of the transformer and the full combiner network obtained using the lumped model. For comparison, we also include the $G_{max}$ plot obtained using 3-D EM simulation of the transformer. To calculate the loss of the combiner in Fig. 5.5(b) we have assumed inductor and capacitor Q-factors of 18 and 12 which are typical values in this technology. Fig. 5.6 compares the combiner loss and efficiency for three sets of Q-factors. It can be observed that the full network has about 0.2-0.5 dB extra insertion loss compared to the transformer. Further, loss of the transformer is almost constant for $d_{ext}$ ranging from 160 $\mu$m to 260 $\mu$m, whereas the loss of the combiner quickly increases as we deviate from the optimum $d_{ext}$ of 180 $\mu$m. The impact of combiner loss on the drain efficiency of the PA can be estimated using the expression

$$\eta_{\text{drain}} = \eta_{LP} \times \eta_{\text{combiner}},$$

where $\eta_{LP}$ is the drain efficiency obtained from load pull simulations with ideal passives. With $\eta_{LP}$ of 40% and 18% at peak and 6-dB back-off power levels, $\eta_{\text{drain}}$ varies by 3-4% points at the peak power level and 1-2 % points at the back-off power level for $d_{ext}$ ranging from 100 $\mu$m to 220 $\mu$m.

Implementation of the output combiner structure is shown in Fig. 5.7. Top level metals M6 and M5 with thicknesses of 2.81 $\mu$m and 1.59 $\mu$m are used for the transformer windings. To reduce power loss, the transformer is implemented over the substrate with no ground plane underneath. However, the transformer is surrounded by M2 ground planes on the sides at a distance of about 30 $\mu$m from the circumference to avoid unexpected coupling with adjacent structures. The ground plane also isolates the two transformer windings. For parallel combining, we prefer microstrip line rather than coplanar stripline due to well-controlled mode and consequently characteristic impedance of the microstrip line and ease of connecting to a single-ended GSG output. To provide a good AC bypass at the center taps an array of MIM capacitors is used as shown in Fig. 5.7. EM simulation of the full structure shows that $G_{max}$ is $-1$ dB at 28 GHz.
Figure 5.4 Comparison of two-port S-Parameters of transformers obtained using lumped model and HFSS simulations a) $S_{11}$, $d_{ext}$=100 $\mu$m b) $S_{21}$, $d_{ext}$=100 $\mu$m c) $S_{11}$, $d_{ext}$=160 $\mu$m d) $S_{21}$, $d_{ext}$=160 $\mu$m e) $S_{11}$, $d_{ext}$=220 $\mu$m f) $S_{21}$, $d_{ext}$=220 $\mu$m.
Figure 5.5 Estimated $G_{\text{max}}$ of the transformer and the combiner network using lumped model and HFSS simulations.

Figure 5.6 Variation of $G_{\text{max}}$ and efficiency of the combiner network with inductor and capacitor Q-factor.
5.3 Unit Driver-PA design

The two-stage PA schematic is shown in Fig. 5.7. Four driver stage PAs are combined using a two-way series two-way parallel combiner consisting of two spiral-transformer baluns and a microstrip T-combiner. Each transformer-combined driver PA pair is driven by one pre-driver with a balun. The two pre-driver PAs are driven by a microstrip T-splitter. The PA is designed in TowerJazz 180-nm SiGe BiCMOS technology which includes high performance npn transistors with $f_T/f_{max}$ of 200/260 GHz, a $BV_{CEO}$ of 1.6 V and a $BV_{CBO}$ of 5.5 V. The unit-driver stage PAs are cascode amplifiers as shown in Fig. 5.7. The cascode topology is chosen because of the higher allowed voltage swing across the common base (CB) device, higher gain and better reverse isolation. Both devices of the cascode amplifier use dual emitter, triple base and dual collector (CBEBEBEC) style layout for reduced base

Figure 5.7 Two stage 28-GHz PA schematic.
resistance and a compact layout. The devices have 10-µm long emitter with two fingers to deliver greater than 18-dBm oP$_{1\text{dB}}$. The adjacent deep trench regions of multiple fingers are merged to further reduce parasitic interconnects. The technology supports MIM capacitors at lower metal levels (M3 and M4) which enables us to realize a high quality bypass capacitor at the base terminal of the CB device. The common emitter (CE) and CB devices are biased using two separate but identical current mirrors. Load-pull simulations indicate the cascode amplifier can achieve 18-dBm oP$_{1\text{dB}}$ with a 37% maximum peak PAE for $Z_{\text{opt}} = 28 + j32 \, \Omega$ (excluding the device capacitance). Transient simulation of the unit PA with input and output matching networks revealed generation of small subharmonic parametric oscillations at 3-dB back-off and higher power levels. To suppress this tone a shunt-connected series LC notch at the subharmonic frequency is added at the base of the CE transistor. Details of the implementation of the notch is presented with the inter-stage matching network.

### 5.4 Pre-driver, Inter-stage matching and Input matching

A pre-driver stage is added to improve the gain of the PA so that the oP$_{1\text{dB}}$ requirements of the previous stage is relaxed. We use one pre-driver amplifier to drive each pair of balanced PAs. Our pre-driver stage is also a cascode amplifier designed to deliver greater than 10-dBm oP$_{1\text{dB}}$ and about 11-dB gain. The device sizes, supply voltage and bias current density are scaled compared to the driver stage to conserve dc power. We use a single-finger device with 10-µm long emitter biased at a current density of 0.4 mA/µm and a collector supply voltage of 2.8 V. A load pull simulation indicates that the optimum impedance at the pre-driver output excluding the device capacitance ($Z_{\text{opt-pre}}$) to maximize PAE is $90 + j45\Omega$.

We design the interstage-matching network to provide out-of-phase inputs to the balanced driver PA pair as well as to transform $Z_{\text{in-driver}}$ to $Z_{\text{opt-pre}}$, where $Z_{\text{in-driver}}$ is the impedance looking into the driver stage. The interstage matching network consists of a transformer balun, a series line $L_{\text{se-inter}}$ and a shunt MIM capacitor $C_{\text{sh-inter}}$ as shown in Fig. 5.7. Since $Z_{\text{opt-pre}}$ is outside the conductance circle $G=\text{Re}[1/Z_{\text{in-driver}}]$, the impedance transformation trajectory is similar to the
one shown in Fig. 5.2(a) and the same optimization procedure presented in the previous section is applied. Also, as mentioned in section 5.2 the unit driver PAs need a subharmonic notch around 14 GHz at the input to suppress parametric oscillations. The notch is implemented with a series tank consisting of a 2.5-um thick 480-µm long line and a 196-fF MIM capacitor. To make the layout compact, the line is meandered around the transformer on both sides and over the ground planes as shown in Fig. 5.7

The input network consists of a shunt microstrip line ($L_{in2}$) at the input of the pre-driver amplifiers, a parallel combiner, a series MIM capacitor ($C_{in2}$) and a sub-harmonic notch filter ($L_{in1}$ and $C_{in1}$) (Fig. 5.7). The input match is achieved using the $\pi$-network of $L_{in2}$, $C_{in2}$ and the notch filter. $L_{in2}$ also sources the base bias voltage for the CE device of the pre-driver amplifier and $C_{in2}$ performs the additional function of dc blocking.

### 5.5 Measurement Results

A die photo of the fabricated chip is shown in Fig. 5.8 and the chip measures 1.2 mm by 0.8 mm including RF and dc pads. All measurements were performed with a of 2.8-V pre-driver collector voltage, 7.5-mA pre-driver quiescent dc current, 3.8-V driver collector voltage and 50-mA driver quiescent dc current. S-parameter measurement and simulation results are shown in Fig. 5.9. The PA achieves 30-dB peak gain at 31-GHz and less than 12-dB input return loss and less than 3-dB gain variation across the 27-31 GHz frequency range. Output return loss is somewhat worse than simulation possibly due to over-estimation of losses in our EM simulation set up. Small signal stability of the PA in the frequency range 100 MHz - 67 GHz is verified by the $\mu$-factor and large signal stability from 100 MHz- 40 GHz is ascertained using a spectrum analyzer.

Swept power results at 28 GHz are shown in Fig. 5.10. The PA has 23.8-dBm $P_{sat}$, 23.2-dBm $O_{1dB}$, 32.7% PAE at 1-dB compression and 15% PAE at 6-dB back-off. Swept power performance in the 27 to 31 GHz frequency range is presented in Table I and shows that the PA has only 1.2-dB variation in $O_{1dB}$ across 27–31 GHz. To assess the linearity of the PA we also performed AM-PM distortion and two-tone measurements. AM-PM measurements of the PA shown in Fig. 5.11(a) indicate that the PA
has less than 4 degree distortion at 3-dB back-off and lower power levels. Two tone measurements are presented in Fig. 5.11(b). The PA shows less than $-32.6 \text{dbc}$ third-order intermodulation product (IM3) compared to the fundamental tone at 6-dB back-off.

Figure 5.8 Die photo of the PA. Size is 1.2 mm by 0.8 mm including pads.

Figure 5.9 Measured S-Parameters of the PA (simulations showed with dashed lines).
Figure 5.10 Measured swept power performance the PA (simulations showed with dashed lines).

Figure 5.11 Linearity measurements of the PA (a) AM-PM distortion at 28 GHz (b) Third order intermodulation (IM3) with tones at 28.2 GHz and 28.5 GHz.
5.6 Conclusion

In this chapter, we demonstrated a co-optimization technique for transformer-based two-way series two-way parallel combiners. The transformer structure is simultaneously optimized with matching elements to minimize the power loss of the full network. An accurate lumped-element model is used in this technique, thus, avoiding the need for full 3-D EM simulations for optimization. $G_{\text{max}}$ of the network is calculated as a function of the transformer diameter using this lumped model and equations for matching components which enables us to choose the optimum diameter. Efficacy of this technique is demonstrated by our measurement results which shows 5.2-dB boost in $\text{oP}_{1\text{dB}}$ with only 2-3% point degradation in PAE compared to a unit PA. Due to the high gain the PA could be easily driven by a low power (~0 dBm) source. Performance comparison with state-of-the art PAs is shown in Table II, where only the highest efficiency and high $\text{oP}_{1\text{dB}}$ results have been included for conciseness. Compared to high-efficiency one-way PAs like the ones presented in [60] and [76], this work improves $\text{oP}_{1\text{dB}}$ by 8 dB with only 2-3% point efficiency reduction. Compared to other high-$\text{oP}_{1\text{dB}}$ PA results [51–53], our PA achieves at least 8% point higher PAE at 6-dB back-off. Comparison to those PAs in Table II which have linearity data (IM3) [51, 53] available shows that our PA achieves a better linearity as well.

Table 5.1 Performance of the 28-GHz power-combined PA across band

<table>
<thead>
<tr>
<th>Frequency (GHz)</th>
<th>27</th>
<th>28</th>
<th>29</th>
<th>30</th>
<th>31</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain (dB)</td>
<td>27.2</td>
<td>28.6</td>
<td>28.6</td>
<td>28.7</td>
<td>29.9</td>
</tr>
<tr>
<td>$P_{\text{sat}}$ (dBm)</td>
<td>23.6</td>
<td>23.7</td>
<td>23.3</td>
<td>23.8</td>
<td>22.9</td>
</tr>
<tr>
<td>$\text{oP}_{1\text{dB}}$ (dBm)</td>
<td>23.3</td>
<td>23.2</td>
<td>22.7</td>
<td>22.6</td>
<td>22.2</td>
</tr>
<tr>
<td>Peak PAE (%)</td>
<td>30.3</td>
<td>32.7</td>
<td>30.6</td>
<td>30.8</td>
<td>33</td>
</tr>
<tr>
<td>PAE 1-dB comp. (%)</td>
<td>29.9</td>
<td>32.7</td>
<td>29.8</td>
<td>29.5</td>
<td>32.4</td>
</tr>
<tr>
<td>PAE 6-dB-back-off (%)</td>
<td>13.7</td>
<td>15</td>
<td>13.8</td>
<td>13.4</td>
<td>13.8</td>
</tr>
</tbody>
</table>
Table 5.2 Performance comparison with Ka and Q-band Power Amplifiers

<table>
<thead>
<tr>
<th>Reference</th>
<th>Frequency (GHz)</th>
<th>Architecture</th>
<th>Supply Voltage (V)</th>
<th>Gain (dB)</th>
<th>P1dB (dBm)</th>
<th>PAE at P1dB (%)</th>
<th>PAE at 6-dB-backoff (%)</th>
<th>ITRS FOM†</th>
<th>Technology</th>
</tr>
</thead>
<tbody>
<tr>
<td>This work</td>
<td>28</td>
<td>Two stage, 4-way power combined</td>
<td>3.8</td>
<td>28</td>
<td>23.2</td>
<td>32.7</td>
<td>15</td>
<td>96.4</td>
<td>180-nm SiGe</td>
</tr>
<tr>
<td>[53] Helmi et. al.</td>
<td>28</td>
<td>Three Triple-Stacked</td>
<td>10.8</td>
<td>17.3</td>
<td>23</td>
<td>12.5</td>
<td>5'</td>
<td>62.6</td>
<td>45-nm SOI CMOS</td>
</tr>
<tr>
<td>[60] Mortazavi et. el.</td>
<td>28</td>
<td>Two stage, Class-F</td>
<td>2.4</td>
<td>21.2</td>
<td>15</td>
<td>38</td>
<td>18.5'</td>
<td>83.5</td>
<td>130-nm SiGe</td>
</tr>
<tr>
<td>[52] Jayamon et. el.</td>
<td>28</td>
<td>Multigate-cell</td>
<td>5.2</td>
<td>13</td>
<td>21</td>
<td>20</td>
<td>6'</td>
<td>80.6</td>
<td>45-nm SOI CMOS</td>
</tr>
<tr>
<td>[51] Welp et. el.</td>
<td>24</td>
<td>1-stage differential</td>
<td>5</td>
<td>18.5</td>
<td>23.7</td>
<td>27</td>
<td>7'</td>
<td>85</td>
<td>350-nm SiGe</td>
</tr>
</tbody>
</table>

* Estimated from swept power plots
† FOM = P_{sat} (dBm) + Gain (dB) + 20\log_{10} (Frequency (GHz)) + 10\log_{10} (PAE) [53]
This work advances state-of-the-art research in millimeter-wave PAs with several key contributions. Firstly, second-harmonic tuned PA operating in continuous class-AB mode was investigated to improve peak efficiency. To achieve the resistive-inductive fundamental and capacitive second-harmonic impedances, a lumped-element network topology was introduced. This lumped-element network consists of a bandpass filter cascaded with or surrounded by a lowpass matching network. A novel technique was demonstrated to tune the second harmonic phase of a Chebyshev bandpass filter while maintaining a good fundamental match. Further, the technique was adapted to be parasitic aware with the use of Norton transforms. Benefit of continuous-mode operation and the proposed harmonic network design technique are demonstrated with a 28-GHz PA designed in 130-nm SiGe process which achieves high peak and back-off efficiency with good linearity.

Having demonstrated a significant improvement in PAE at 28-GHz, the efficacy of second-harmonic tuning is investigated for a wide range of millimeter-wave frequencies. Harmonic genera-
tion capability of the device is evaluated with load-line and load-pull simulations versus frequency. A second type of harmonic-matching network realizable with microstrip lines is adopted and a design methodology for this network is presented. Harmonic-tuned PAs are realized using this matching network from 28 to 78 GHz and compared to LC-tuned PAs to evaluate the improvement in power and/or efficiency due to second harmonic tuning. Using real passive components, we demonstrate 3-4% points improvement in peak PAE from 28 to 43 GHz and 2% points improvement in peak PAE up to 63 GHz with the use of second-harmonic tuning. The break-even frequency where the harmonic-tuned network does not provide any additional benefit is established as 68 GHz. These simulations are also validated by two integrated circuit designs at 28 GHz and 60 GHz which demonstrate state-of-the-art efficiency.

After demonstrating high peak PAE single-path PAs, we investigate architectures that can improve output power and back-off PAE of millimeter-wave PAs. We investigate techniques for Doherty PAs that are key to improve the output power and back-off efficiency at millimeter-wave. These include multi-stage architecture choice, benefits and limitations of harmonic tuning, peaking PA trade-offs and output combiner choice. Two-stage carrier and peaking amplifiers were used for sufficient gain along each path which enabled the possibility of independent amplitude and phase adjustment of the two amplifiers using preceding phase shifter stage. Simple fundamental output match was preferred over harmonic tuning due to broadband performance. Design methodology of the peaking PA presented the impact of bias current density on power consumption and linearity of the Doherty PA. A high-impedance output match was preferred over optimum power match for the peaking PA to minimize leakage from the carrier PA. Efficacy of these techniques/design considerations are demonstrated with the implementation of a 60-GHz Doherty PA which demonstrates 3-dB higher oP_{1dB} and 5% points higher 6-dB-back-off PAE than the harmonic-tuned continuous class-AB mode PA.

Finally, we investigate compact low-loss transformer-based combiners which preserve the linearity of unit PAs. A co-optimization technique was developed to minimize the loss of a two-way series two-way parallel combiner including the transformer and the adjoining matching elements. A
simple but accurate lumped-model is used for this co-optimization procedure eliminating 3-D EM simulations. The technique presented is generalized for an arbitrary impedance and a K-way series M-way parallel combiner. We demonstrate this technique with the implementation of a 28-GHz two-way series two-way parallel power combined PA which improves the $O_{1\text{dB}}$ by $\sim 5$ dB compared to that of a single-path class-AB PA with only 3% point degradation in peak PAE.

Comparison of the 28-GHz harmonic-tuned PAs and the two-way series two-way parallel power-combined PA with Ka-band and Q-band PAs published in literature is shown in Fig. 6.1 and Fig. 6.2. The single-stage and two-stage 28-GHz PAs presented in chapter two and chapter three achieve one of the highest peak and back-off PAEs. These are only exceeded by the Class-F / inverse Class-F PAs presented in [59–61]; however, our designs achieve about a dB higher output power. We also achieve good linearity demonstrated by AM-PM and IM3 measurements whereas linearity data of the class-F/ inverse Class-F PAs are not available for comparison. The result in [24] has lower peak PAE than our designs but achieves about one percentage point higher back-off PAE due to higher gain expansion; however, it has only 9-dB gain and needs additional pre-driver stages to boost the gain. The power-combined PA presented in this work achieves highest peak and back-off PAE among linear PAs which have greater than 20-dBm output power. The Class-E PA in [62] achieves about 1-2% points higher peak PAE with similar output power as our design, but it is highly non-linear and has only 14-dB power gain.

Comparison of the 60-GHz two-stage PA and the Doherty PA with published V-band PAs is shown in Fig. 6.3 and Fig. 6.4. The 60-GHz PAs designed in this work have 4-5% lower peak PAE compared to those presented in [32, 40, 67] but have highest back-off PAEs. In particular, the Doherty PA exceeds the 6-dB-back-off PAE of other published PAs by 3-4% points.

We demonstrate the impact of these performance improvements on a beamformer in Table 6.1 and Table 6.2. The 28-GHz power-combined PA can achieve 30-dBm EIRP with half the number of beamformer elements compared to the PA presented in [60] but the beamformer would consume about 3.4 times higher dc power. On the other hand compared to another high output power PA presented in [51], our PA has 2.4 times lower dc power consumption while delivering the same EIRP.
A four-element 28-GHz beamformer which achieves highest peak and back-off PAE is presented in Appendix C. The 60-GHz Doherty PA can reduce power consumption of the beamformer significantly compared to the PAs in [55] and [32] as shown in Table 6.2.

Thus, the methodologies developed in this work have the capability to reduce power consumption and/or die area (cost) of silicon millimeter-wave phased arrays significantly. This will further enable integration of phased arrays into mobile systems for high data rate communications in millimeter-wave frequency bands.

Figure 6.1 $P_{\text{sat}}$ and PAE of state-of-the-art CMOS (red) and SiGe (blue) 28-GHz PAs compared to the single-stage continuous mode PA, the two-stage continuous mode PA, and the two-stage power-combined PA presented in this work.

6.1 Future Work

In chapter 2 we presented a methodology to realize a network that can achieve fundamental and harmonic impedances necessary to realize continuous class-AB mode PAs. These networks are
Figure 6.2 $P_{1\text{dB}}$ and PAE at 6-dB back-off of state-of-the-art CMOS (red) and SiGe (blue) 28-GHz PAs compared to the single-stage continuous mode PA, the two-stage continuous mode PA, and the two-stage power-combined PA presented in this work.

Figure 6.3 $P_{\text{sat}}$ and PAE of state-of-the-art CMOS (red) and SiGe (blue) 60-GHz PAs compared to the two-stage continuous mode PA and the Doherty PA presented in this work.
Figure 6.4  $oP_{1dB}$ and PAE at 6-dB back-off of state-of-the-art CMOS (red) and SiGe (blue) 60-GHz PAs compared to the two-stage continuous mode PA and the Doherty PA presented in this work.

Table 6.1 Impact of 28-GHz PA performance on beamformer

<table>
<thead>
<tr>
<th>Reference</th>
<th>$oP_{1dB}$</th>
<th>Number of elements</th>
<th>EIRP (dBm)</th>
<th>PAE 6-dB back-off (%)</th>
<th>$P_{dc}$ (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power combined PA</td>
<td>23.2</td>
<td>5</td>
<td>31.2</td>
<td>15</td>
<td>1750</td>
</tr>
<tr>
<td>[60]</td>
<td>15</td>
<td>12</td>
<td>30.6</td>
<td>18.5</td>
<td>515</td>
</tr>
<tr>
<td>[51]</td>
<td>23.7</td>
<td>5</td>
<td>31.7</td>
<td>7</td>
<td>4206</td>
</tr>
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</table>

Table 6.2 Impact of 60-GHz PA performance on beamformer

<table>
<thead>
<tr>
<th>Reference</th>
<th>$oP_{1dB}$</th>
<th>Number of elements</th>
<th>EIRP (dBm)</th>
<th>PAE 6-dB back-off (%)</th>
<th>$P_{dc}$ (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Doherty PA</td>
<td>17.5</td>
<td>8</td>
<td>29.6</td>
<td>13.8</td>
<td>819</td>
</tr>
<tr>
<td>[55]</td>
<td>18.2</td>
<td>8</td>
<td>30.2</td>
<td>10</td>
<td>1327</td>
</tr>
<tr>
<td>[32]</td>
<td>19.9</td>
<td>6</td>
<td>29.5</td>
<td>6.5</td>
<td>2265</td>
</tr>
</tbody>
</table>
capable of tracking the continuous mode contour for about 10% bandwidth around the center frequency. Network design techniques could be investigated in future such that the continuous mode contour is followed for a wider bandwidth; thus, enabling wideband large-signal performance. The harmonic matching network design technique could be applied in many other scenarios including Class-F, inverse Class-F, Class-E PAs, and inter-stage matching networks. Finally, the second-harmonic phase tuning technique developed for lumped-element Chebyshev filters could be extended to distributed filters; this could be particularly useful at higher millimeter-wave frequencies where parasitic components of lumped-elements become a major problem for filter design.

In chapter 3 the effectiveness of harmonic tuning in continuous class-AB mode PAs over a wide range of millimeter-wave frequencies is investigated. The study was done with the help of a physics-based HiCUM model. Due to equipment limitations, measurement of harmonic components and external harmonic load pull is not feasible at the moment but could be a scope of research in the future. Also, we used a stub-based network to study the efficacy of harmonic tuning over frequency. Alternately the lumped network presented in chapter 2 could be used for this study in future.

Chapter 4 investigated techniques that are key to achieve a high performance Doherty PA at millimeter-wave. It is well known that the Doherty technique has bandwidth limitations. One key research direction in future would be to investigate broadband back-off efficiency enhancement techniques. The Doherty-Outphasing continuum proposed in [90] could be a possible solution. However, compact and low-loss passive combiners need to be developed to realize the Doherty-Outphasing continuum in integrated circuits.

Chapter 5 presented a methodology to co-optimize the transformer structure with adjoining matching elements to minimize power loss in a two-way series two-way parallel combiner using a lumped model. The methodology could be used for other transformer based combiners including series combined PAs and transformer-combined Doherty PAs. The feasibility of implementing harmonic-matching in transformer combined PAs could be investigated in future. Finally, compact power-combiner architectures that could also provide isolation between the unit PAs could be investigated.
BIBLIOGRAPHY


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The equations for virtual impedance based $\pi$-network design introduced in section 3.2 are given below. These could be derived following a similar method as the standard $\pi$-network design with virtual resistance. We have considered the effect of finite quality factor and parasitic components. The $\pi$-network including parasitic elements is redrawn in Fig. A.1.

$$a|X_{C21}|^2 + b|X_{C21}| + c = 0$$  \hspace{1cm} (A.1)
Figure A.1 π-network for fundamental match with parasitics and virtual impedance.

\[
X_{L1} = \frac{\left(\left( R_{V1} + \frac{|X_{C21}|}{Q_C}\right)^2 + (X_{V1} - |X_{C21}|)^2\right) X_{opt}}{\left(\left( R_{V1} + \frac{|X_{C21}|}{Q_C}\right)^2 + (X_{V1} - |X_{C21}|)^2 - X_{opt}(X_{V1} - |X_{C21}|)\right)} \tag{A.2}
\]

\[p|X_{C22}|^2 + q|X_{C22}| + r = 0 \tag{A.3}\]

\[
X_{L3} = \frac{\left(\left( R_{V2} - \frac{|X_{C22}|}{Q_C}\right)^2 + (X_{V2} + |X_{C22}|)^2\right)}{\left(\omega C_P\left( R_{V2} - \frac{|X_{C22}|}{Q_C}\right)^2 + \omega C_P (X_{V2} + |X_{C22}|)^2 - X_{opt}\left( X_{V2} - |X_{C22}|\right)\right)} \tag{A.4}
\]

\[|X_{C2}| = |X_{C21}| + |X_{C22}| \tag{A.5}\]

where \(X_{L1}, X_{C21}, X_{C22},\) and \(X_{L3}\) are the reactances of \(L_1, C_{21}, C_{22}\) and \(L_3\),

\[a = \frac{1}{Q_C^2} + 1 \tag{A.6}\]

\[b = \frac{2R_{V1}}{Q_C} - 2X_{V1} - \frac{X_{opt}R_{opt}}{X_{opt}Q_{L1} - R_{opt}} \left(1 + \frac{Q_{L1}}{Q_C}\right) \tag{A.7}\]

\[c = R_{V1}^2 + X_{V1}^2 + \frac{X_{opt}R_{opt}(X_{V1} - Q_{L1}R_{V1})}{X_{opt}Q_{L1} - R_{opt}} \tag{A.8}\]

\[p = \left(\frac{1}{Q_C^2} + 1\right)\left(\omega C_P R_L + Q_{L3}\right) \tag{A.9}\]

\[q = \left(\frac{R_L - 2R_{V2}}{Q_C}\right)Q_{L3} - 2\omega C_P R_L R_{V2} - 2X_{V2}\left(\omega C_P R_L + Q_{L3}\right) + R_L \tag{A.10}\]

\[r = R_{V2}^2 + X_{V2}^2\left(\omega C_P R_L + Q_{L3}\right) + R_L X_{V2} - R_L R_{V2} Q_{L3} \tag{A.11}\]
\[ R_{V1} = R_V + \frac{\omega L_{p1}}{Q_{Lp1}} \]  
(A.12)

\[ X_{V1} = X_V + \omega L_{p1} \]  
(A.13)

\[ R_{V2} = R_V - \frac{\omega L_{p2}}{Q_{Lp2}} \]  
(A.14)

\[ X_{V2} = X_V - \omega L_{p2} \]  
(A.15)

and \( Q_{L1}, Q_{Lp1}, Q_C, Q_{Lp2}, Q_{L3} \) are quality factors of \( L_1, L_{p1}, C_{21} \) (and \( C_{22} \)), \( L_{p2}, L_3 \). The allowed values of \( R_V \) and \( X_V \) are those which satisfy the following conditions:

\[ b^2 - 4ac > 0 \]  
(A.16)

\[ q^2 - 4pr > 0 \]  
(A.17)

\[ b < 0 \parallel c < 0 \]  
(A.18)

\[ q < 0 \parallel r < 0 \]  
(A.19)
The following equations for the matching elements $X_{Li}(=\omega L_i)$ and $X_T(=1/(\omega C_T))$ in the combiner network shown in Fig. B.1(b) and redrawn in Fig. B.1 have been derived using the same procedure that is used for a standard two element matching network design \cite{3} but finite Q-factors $Q_{Li}$ and $Q_T$ have been assumed

$$aX_{Li}^2 + bX_{Li} + c = 0 \quad (B.1)$$
\[ R_{LT} = (M/K) \times RL \]

\[ L_0 = L_{o1} + L_{o2} \times (M/K) \]

\[ C_{PT} = (K/M) \times CP \]

\[ L_s1, L_s2, L_m, C_s, CT \]

**Figure B.1** Simplified schematic for impedance seen by an unit PA.

\[ X_T = \frac{\left(\text{Re}[Z_T] + \frac{X_{Li}}{Q_{Li}}\right)^2 + \text{Im}[Z_T] + X_{Li}}{X_{optP} (\text{Im}[Z_T] + X_{Li}) - \left(\left(\text{Re}[Z_T] + \frac{X_{Li}}{Q_{Li}}\right)^2 + (\text{Im}[Z_T] + X_{Li})^2\right)} \] (B.2)

where

\[ a = \left(\frac{1}{Q_{Li}^2} + 1\right) \left(Q_T X_{optP} + R_{optP}\right) \] (B.3)

\[ b = \left(\frac{2 \text{Re}[Z_T]}{Q_{Li}} + 2 \text{Im}[Z_T]\right) \left(Q_T X_{optP} + R_{optP}\right) - X_{optP} R_{optP} \left(Q_T + 1\right) \] (B.4)

\[ c = |Z_T|^2 \left(Q_T X_{optP} + R_{optP}\right) - X_{optP} R_{optP} \left(Q_T \text{Re}[Z_T] + \text{Im}[Z_T]\right) \] (B.5)

\[ R_{optP} \parallel X_{optP} \] is the parallel equivalent of \( Z_{opt} \), the optimum impedance at the unit PA excluding the device capacitance.
The two stage 28-GHz PA presented in Chapter 3 was integrated into a 4-element beamformer whose block diagram is shown in Fig. C.1 [84]. The beamformer includes a 1:4 cascaded Wilkinson power splitter, a 4-bit phase shifter comprised of a differential quadrature generator and a vector interpolator, a serial interface for digital control of phase settings and the two stage 28-GHz PA. Die photo of the beam former is shown in Fig. C.2, it has a die area of 1.9 mm by 2.8 mm including all the pads. Measured S-Parameter and vectors of the beamformer for 16 different phase settings are shown in Fig. C.3. The end to end $S_{21}$ was around 27 dB, with 2-3 dB gain variation across the band and across the 16 phase settings. Swept power measurement results for a single element of the beamformer are shown in Fig. C.4. The beamformer element has a 16.3-dBm $P_{\text{sat}}$, 16-dBm $P_{1\text{dB}}$, 28.2% peak PAE, 9% 7-dB-backoff PAE. The beamformer has the ability to produce 15-dBm on chip output power and 21-dBm EIRP at 7-dB back off consuming less than 380 mW dc power. The measured $P_{1\text{dB}}$, peak PAE and 7-dB-backoff PAE exceed that of all existing beamformers/ phased
arrays at millimeter-wave frequencies.

**Figure C.1** 4 element Beamformer block diagram
Figure C.2 Beamformer die photo

Figure C.3 Measured a) S-Parameters and b) vectors of the 28-GHz 4-element beamformer
Figure C.4 4 element Beamformer swept power measurement
One of the challenges in realizing high output power PAs in deeply scaled CMOS technologies is the lower drain voltage. A technique that has been commonly used in SOI CMOS technologies is the stacking of more than one devices to increase the voltage swing the drain of the transistor [52, 53]. However, this technique has the limitation of lower gain and degraded linearity [54]. In this work, we use cascode amplifiers with thick-oxide common-gate transistor and regular thin-oxide common-source transistor to realize high-output power driver stage with good gain in 45-nm SOI CMOS technology. The driver stage amplifier uses the high-performance floating body devices to reduce parasitic interconnects and improve gain. The pre-driver stage amplifier which is biased at a lower current density compared to the driver stage amplifier uses body-connected devices to avoid the floating-body effect associated with SOI devices. A PMOS varactor is included at the input of the pre-driver stage to compensate for AM-PM distortion of the PA. Matching networks are implemented with high-quality spiral inductors, microstrip transmission lines and metal-oxide-metal (MOM)
capacitors. The inductors are realized with 1.25 turn octagonal spirals in top metal with floating shield. Schematic of the 28-GHz PA is shown in Fig. D.1 and swept power measurement results at 28 GHz are shown in Fig. D.2. The PA has 15.2-dB gain, 17-dBm $P_{\text{sat}}$, 14.9-dBm $P_{1\text{dB}}$ and 31.5% peak PAE at 28 GHz. Performance across the band is presented in Table D.1.
Figure D.2 Swept power measurement results at 28 GHz

Table D.1 Performance of the 28-GHz PA across band

<table>
<thead>
<tr>
<th>Frequency (GHz)</th>
<th>27</th>
<th>28</th>
<th>29</th>
</tr>
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<tbody>
<tr>
<td>Gain (dB)</td>
<td>13.5</td>
<td>15.2</td>
<td>15.7</td>
</tr>
<tr>
<td>$P_{\text{sat}}$ (dBm)</td>
<td>16.7</td>
<td>17</td>
<td>17.2</td>
</tr>
<tr>
<td>$oP_{1\text{dB}}$ (dBm)</td>
<td>15.3</td>
<td>14.9</td>
<td>15.2</td>
</tr>
<tr>
<td>Peak PAE (%)</td>
<td>29.7</td>
<td>31.5</td>
<td>30.5</td>
</tr>
<tr>
<td>PAE 1-dB comp. (%)</td>
<td>25</td>
<td>22.5</td>
<td>23.3</td>
</tr>
<tr>
<td>PAE 6-dB-back-off (%)</td>
<td>6.5</td>
<td>6</td>
<td>6.5</td>
</tr>
</tbody>
</table>
In this Appendix, a 28-GHz Doherty PA is presented. The top level schematic is shown in Fig. E.1. The harmonic-tuned PA presented in chapter-2 is adopted for the carrier and peaking amplifiers of the Doherty PA. Lumped element equivalents of transmission lines are used in the Wilkinson power divider, the quarter-wave impedance transformer and the 120° line as shown in Fig. E.3.

Die photo of the Doherty PA is shown in Fig. E.2 and the chip measures 1.25 mm by 1.33 mm including pads. S-parameter and swept-power measurement results of the Doherty PA are shown in Fig. E.4 and Fig. E.5. Measurement results of the Doherty PA demonstrate 8.2-dB gain, 18.8-dBm $P_{\text{sat}}$, 15.5-$P_{1\text{dB}}$, 20% peak PAE and 12.7% 6-dB-back-off PAE at 28 GHz. The Doherty PA showed 3-4 dB lower measured gain compared to simulations due to extra inductive degeneration in the carrier and peaking PA. We also observed a 4-5% reduction in back-off PAE in measurements compared to initial simulations. Revised simulations with an updated model (HiCUM) of the SiGe npn transistor explained most of these discrepancies. Performance of the PA across 27-29 GHz band is presented.
Table E.1 Performance of the Doherty PA across band

<table>
<thead>
<tr>
<th>Frequency (GHz)</th>
<th>27</th>
<th>28</th>
<th>29</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain (dB)</td>
<td>8.9</td>
<td>8.2</td>
<td>8</td>
</tr>
<tr>
<td>$P_{sat}$ (dBm)</td>
<td>19.1</td>
<td>18.8</td>
<td>18.4</td>
</tr>
<tr>
<td>$O_{P1dB}$ (dBm)</td>
<td>15.1</td>
<td>15.5</td>
<td>16.5</td>
</tr>
<tr>
<td>Peak PAE (%)</td>
<td>23.5</td>
<td>20.6</td>
<td>20.1</td>
</tr>
<tr>
<td>PAE 1-dB comp. (%)</td>
<td>22.7</td>
<td>20</td>
<td>20.1</td>
</tr>
<tr>
<td>PAE 6-dB-back-off (%)</td>
<td>10.9</td>
<td>9.9</td>
<td>11.5</td>
</tr>
</tbody>
</table>

Figure E.1 28-GHz Doherty PA top level schematic
Figure E.2 28-GHz Doherty PA top level schematic
Figure E.3 Passive components in the Doherty PA (a) Wilkinson combiner (b) 70-Ω line for Wilkinson combiner (c) 50-Ω quarter-wave line (d) 50-Ω 120° line
**Figure E.4** Measured S-parameters of the Doherty PA

**Figure E.5** Swept power measurements of the Doherty PA at 28 GHz