ABSTRACT

Chen, Tianxiang. Single-Stage Dual-Phase-Shift DAB AC-DC Converter based on GaN Transistor. (Under the direction of Dr. Alex Q. Huang).

During the past few decades, renewable energy has been demonstrated as a promising energy resource because of its sustainability and minimal negative impact on environment. Nevertheless, the feature of renewable energy source, discontinues, unstable, unreliable, indeed have challenge to the current power system. Therefore, the energy storage system was proposed to meet the need of a stable and reliable power source.

This thesis focus on the control and hardware design of a AC-DC distributed energy storage device. This system could achieve single stage AC-DC power conversion, bidirectional power flow, ZVS at whole period and unity power factor.

In this thesis, dual-phase-shift modulation, single-phase-shift modulation, variable frequency control, partial-load improved modulation are proposed. These control methods could improve the ZVS condition during zero-crossing situation, and further achieve a unity power factor through variable frequency.

Experimental verification is made to demonstrated the function of this converter with a 1.6kW hardware prototype. Hardware design is described in this thesis to prevent EMI interface and achieve basic function of proposed converter. Experimental test is finished with the proposed function of this converter.
Single-Stage Dual-Phase-Shift DAB
AC-DC Converter based on GaN Transistor

by
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A thesis submitted to the Graduate Faculty of
North Carolina State University
in partial fulfillment of the
requirements for the degree of
Master of Science

Electrical Engineering

Raleigh, North Carolina

2017

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DEDICATION

To my father, Guoqi Chen.
BIOGRAPHY

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ACKNOWLEDGMENTS

I would like to give my deepest appreciation to Dr. Alex Q. Huang for his instruction and inspiration to all my work. With this precious opportunity to join Dr. Huang’s research team at FREEDM system center at NC State University, I have great improvement in academics.

Thanks Dr. Srdjan Lukic and Dr. Wensong Yu for being my committee member to further instruct my thesis work.

Specially, I would like to deliver my appreciation to Dr. Ruiyang Yu and Mr. Fei Xue in DESD team. I could never finish my work without their great support and help.
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CHAPTER 1 INTRODUCTION

1.1. Background of Energy Storage Device

Energy, demonstrated long time in history, plays a core role in the development, discovery and support of human life. To make use of nature resource, fossil energy has been proved as a huge part of our resource during the past century, while we human gradually realize that fossil energy would one day be exhausted and could have huge negative impact, such as greenhouse gas, climate change and pollution, on next generation. Therefore, a long term, sustainable development is not only a requirement for people current living, but also a precious gift for our descendant. [1] indicates by 2040, the majority of renewable-based generation is competitive without any subsidies.

Nowadays, variety of sustainable energy lighten the tomorrow of human being. Photovoltaics, wind power, geothermal energy, all kinds of energy resource has been used in a “green home”. [2] and [3] indicates a green home revolution that has been changing the way of people’s living.

Though it could provide tremendous energy, those energy type have some drawbacks. Discontinues, unstable, unreliable power source indeed have challenge to the current power system. As a system require stable and continues source, sustainable energy is not at its preference due to those drawbacks. While energy storage provides a chance, [4] shows ESS could enhance the stability and reliability of renewable energy micro-grid. [5] indicates a typical structure of a DC microgrid with distributed energy storage system, and have the image of future AC microgrid.
Fig. 1 System Level DC Micro-Gird

Fig. 2 Proposed System Level AC Micro-Gird
More importantly, energy storage could not only participate on the sustainable energy, but could also involve deeply in the current energy system. Energy would no longer be wasted if usage could not match the generation. In many extreme weather situation where power outage might occur, energy storage system could meet the need of electricity\cite{6}.

![Fig. 3 Green Home](image)

A home use AC micro-gird is proposed in figure 3, this mircogrid system could connect a solar panel with solar inverter, modular distributed energy storage device, AC grid and home usage. This microgrid system could meet the need of renewable energy generation and power backup during power outage.

**1.2. Energy Storage Device Topology Comparison**

A conventional approach to distributed energy storage system is two-stage power converter, which attract huge attention recently. This subchapter reviews two-stage AC-DC topology and single-stage AC-DC topology to provide a comparison.
1.2.1. Two-Stage Isolated AC-DC Topology

Figure 4 shows the conventional two-stage isolated AC-DC structure. This structure combined with a AC-DC power factor correction (PFC) and a DC-DC converter to meet the battery voltage level.

![Conventional Two-Stage Isolated AC-DC Structure](image)

**Fig.4 Conventional Two-Stage Isolated AC-DC Structure**

PFC AC-DC converter rectifies AC voltage to a regulated DC link bus. Bidirectional AC-DC converter also have the capability of inverts DC link voltage to AC grid. In this battery storage system application, several typical bidirectional PFC topologies are shown in figure 5\[7\][8].

![Typical Bidirectional PFC Topology](image)

**Fig.5 Typical Bidirectional PFC Topology**

DC-DC converter transfer power from DC bus to the ideal voltage level to charge the battery. Several typical non-isolated bidirectional DC-DC converter topologies are shown in figure 6. Non-isolated DC-DC topology normally have simply structure, high efficiency, low
cost and high reliability. Typical non-isolated bidirectional DC-DC converter could include half-bridge converter, cascaded half bridge converter, Ćuk converter and SEPIC converter.

As for isolated DC-DC topology, dual-active-bridge and LLC which potentially have high efficiency and high power density\textsuperscript{[9]}. A dual active bridge consists of two active bridge linked by a high frequency transformer. The conventional control method of DAB is to set a switching frequency and adjust by single-phase-shift control or dual-phase-control.

An LLC resonant converter is widely used because its advantage of ZVS from zero to full load and high efficiency. Through the variation of LLC could lead to a complex control design, its high efficiency and high power density feature still wins great attention.
The topology of DC DAB and LLC are shown in figure 7 as typical isolated bidirectional DC-DC converter.

![DC DAB DC-DC Converter](image1)

(a) Isolated DAB DC-DC Converter

![LLC DC-DC Converter](image2)

(b) Isolated LLC DC-DC Converter

Fig.7 Typical Isolated Bidirectional DC-DC Converter Topology

1.2.2. Single-Stage Isolated AC-DC Topology

The conventional DC-DC DAB topology could provide inherent bidirectional power flow capability, electrical isolation as well as an easy way to achieve ZVS. While design a two-stage AC-DC converter, a huge DC link capacitor is unavoidable to maintain the stability of DC voltage and instantaneous power flow. Moreover, the set-frequency single-phase-shift control method also suffer from light load efficiency and limited soft-switching range.\textsuperscript{10,11,12,13}. 
To overcome those drawbacks and further increase system efficiency and power density, an isolated AC-DC topology is proposed in [14] to meet the structure of figure 8. This topology could emit the huge DC link capacitor.

![AC Grid ↔ AC/DC ↔ Battery](image)

**Fig. 8 Proposed Single-Stage Isolated AC-DC Structure**

![Diagram of AC Grid ↔ AC/DC ↔ Battery](image)

**Fig. 9 Proposed Rail-to-Rail Cascade Dual Active Bridge Topology**

As shown in figure 9, this topology could transfer 60Hz AC waveform to high frequency voltage go through the high frequency transformer, and transfer to DC voltage. As a topology which capable of bidirectional power flow, the power could also flow in the opposite direction. As a part of DAB topology, it could also handle ZVS during whole range
and achieve unity power factor. Capacitor C₃ could provide a current loop when all switches are closed[15].

1.3. Thesis Outline

The scope of this thesis is organized as follows.

Chapter 2 presents half-bridge full-bridge dual-active-bridge topologies of dual-active-bridge, the ZVS conditions of these two modulations are full analyzed.

Chapter 3 presents partial-load variable frequency dual-phase-shift control and rated-load variable frequency dual-phase-shift control in this single-stage AC-DC converter. Theoretical analysis and simulation verification are presented in this chapter.

Chapter 4 shows the AC power stage design and test; DC power stage assemble and test. A system PCB design is included in this chapter. This chapter also shows the experimental operation waveform and thermal performance.

Chapter 5 summarizes and concludes the work of this thesis. Future work is also states in this chapter.
CHAPTER 2 CONTROL OF DUAL ACTIVE BRIDGE

The structure of basic Dual Active Bridge (DAB) shown in figure 10. DAB topology is widely use in DC-DC converter because of its wide range zero-voltage-switching (ZVS) and bidirectional capability.

![Fig.10 Structure of Basic Dual Active Bridge Topology](image)

In this chapter, the single-phase-shift (SPS) mode, dual-phase-shift (DPS) mode are compared to achieving ZVS. Frequency variable is discussed to achieve power factor correction (PFC). A full bridge AC-DC DAB topology is stated in figure 11.

![Fig.11 Structure of a Full Bridge AC-DC Dual Active Bridge Topology](image)

To emit the passive full bridge rectifier, a rail-to-rail cascade topology is proposed as shown in figure 12. This topology requires slight different strategy when AC voltage turns to be negative.
2.1. Single-Phase-Shift Modulation Principle\cite{16}

2.1.1. Single-phase-shift Modulation Operation Analysis

The voltage and current applied to the transformer and gate signal are presented in figure 13 when $V_{ac} > 0$ and figure 14 when $V_{ac} < 0$. In the modulation, $\theta$ is the phase shift percentage (from 0 to 1) between the primary bridge and secondary bridge. $T_s$ is the time period of a single switching period, where $T_s = t_4 - t_1$. $V_{ac}$ is the primary side voltage reflect on transformer, and $V_{dc}$ is the secondary side voltage reflect on transformer.
Fig. 13 Single-Phase-Shift Modulation Operation Principle where $V_{ac} > 0$
The leakage inductance current of transformer in SPS modulation is calculated in equation (2.1).
The transferred instantaneous power in SPS modulation is given in equation (2.2).

\[
P(t) = \frac{n\theta |v_{ac}| v_{dc}(1 - 2\theta)}{2 f_s L_{\delta}}
\]  

2.1.2. Zero Voltage Analysis in SPS Modulation
To achieve ZVS in SPS Modulation, both the absolute value of $i_{t_o}(t_0)$ and $i_{t_o}(t_1)$ should be large enough to charge and discharge the switch junction capacitor. The current value to achieve ZVS is included in equation (2.3).

\[
\begin{align*}
    i_{t_o}(t_0) & \leq -I_{s,ac} \\
    i_{t_o}(t_1) & \geq I_{s,dc}
\end{align*}
\]  

(2.3)

Where

\[
I_{s,ac} = \frac{v_{ac}}{\sqrt{L_O / C_{eq,ac}}}
\]

\[
I_{s,dc} = \frac{v_{dc}}{\sqrt{L_O / C_{eq,dc}}}
\]

Combine equation 2.1 and 2.3, the range of phase shift could be derived in equation 2.4.

\[
\begin{align*}
    \theta \geq & \frac{4f_sL_O I_{s,ac} - \frac{1}{2}v_{ac} + nv_{dc}}{4nv_{dc}} \\
    \theta \geq & \frac{4f_sL_O I_{s,dc} + \frac{1}{2}v_{ac} - nv_{dc}}{2v_{ac}}
\end{align*}
\]  

(2.4)

Meanwhile, $\theta$ should be $0 \leq \theta \leq \frac{1}{2}$ to guarantee the obtained principle of operation.

Figure 15 indicates the ZVS range of different AC DC voltage ratio that are independent from frequency. When $\theta \geq 0.25$, ZVS could always be guaranteed while would generate a larger circulating current. ZVS range is limited when $\theta \leq 0.25$. 

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2.2. Dual-Phase-Shift Rated-Load Modulation Principle\[16] [17] [18]

2.2.1. Dual-Phase-Shift Rated-Load Modulation Operation Analysis

The voltage and current applied to the transformer and gate signal are presented in figure 16 when \( V_{ac} > 0 \) and figure 17 when \( V_{ac} < 0 \). In the modulation, \( \theta_{3,4} \) is the phase shift percentage (from 0 to 1) between the primary bridge and bridge leg of \( S_3 \) and \( S_4 \), and \( \theta_{5,6} \) is the phase shift percentage (from 0 to 1) between the primary bridge and bridge leg of \( S_5 \) and \( S_6 \). \( T_s \) is the time period of a single switching period.
Fig. 16 Dual-Phase-Shift Rated-Load Modulation Operation Principle where $V_{ac} > 0$
Fig. 17 Dual-Phase-Shift Rated-Load Modulation Operation Principle where \( V_{ac} < 0 \)

The leakage inductance current of transformer in SPS modulation is calculated in equation (2.5).
Where

\[ i_{t_\delta}(t) = \begin{cases} 
\frac{|v_{ac}| + nv_{dc}}{L_\delta} (t - t_0) + i_{t_\delta}(t_0) & t_0 \leq t \leq t_1 \\
\frac{|v_{ac}|}{L_\delta} (t - t_1) + i_{t_\delta}(t_1) & t_1 \leq t \leq t_2 \\
\frac{|v_{ac}|}{L_\delta} (t - t_2) + i_{t_\delta}(t_2) & t_2 \leq t \leq t_3 \\
\frac{|v_{dc}|}{L_\delta} (t - t_3) + i_{t_\delta}(t_3) & t_3 \leq t \leq t_4 \\
\frac{|v_{ac}|}{L_\delta} (t - t_4) + i_{t_\delta}(t_4) & t_4 \leq t \leq t_5 \\
\frac{|v_{ac}| + nv_{dc}}{L_\delta} (t - t_5) + i_{t_\delta}(t_5) & t_5 \leq t \leq t_6 
\end{cases} \]  

(2.5)
The transferred instantaneous power in SPS modulation is given in equation (2.6).

\[
P(t) = \frac{n|v_{ac}|v_{dc}(-2\theta_{3,4}^2 - 2\theta_{5,6}^2 + \theta_{3,4} + \theta_{5,6})}{4f_sL_s}
\]  

(2.6)

2.2.2. Zero Voltage Analysis in DPSR Modulation

To achieve ZVS in DPSR Modulation, both the absolute value of \(i_{L_s}(t_i)\) and \(i_{L_s}(t_3)\) should be large enough to charge and discharge the switch junction capacitor. The current value to achieve ZVS is included in equation 2.7 and 2.8. Equation 2.7 concludes the ZVS requirement for AC side.
\[ i_{t_0}(t_0) \leq -I_{s,ac} \]
\[ i_{t_0}(t_3) \geq I_{s,ac} \]  

(2.7)

Where

\[ I_{s,ac} = \frac{v_{ac}}{\sqrt{L_5/C_{eq,ac}}} \]

The ZVS condition requirement for DC side is conclude in equation 2.8.

\[ i_{t_0}(t_1) \geq I_{s,dc} \]
\[ i_{t_0}(t_2) \geq I_{s,dc} \]  

(2.8)

Where

\[ I_{s,dc} = \frac{v_{dc}}{\sqrt{L_5/C_{eq,dc}}} \]

Combine equation 2.5, 2.7 and 2.8, the range of phase shift could be derived. To simplify calculation and maintain trapezoidal current shape, set \( i_{t_0}(t_1) = i_{t_0}(t_3) \), therefore the relationship of \( \theta_{3,4} \) and \( \theta_{5,6} \) could be derived in equation 2.9.

\[ \theta_{3,4} = \frac{v_{ac}(1-2\theta_{5,6})}{4nv_{dc}} \]  

(2.9)

Combine equation 2.7, 2.8 and 2.9, the range of \( \theta_{5,6} \) phase shift could be derived in equation 2.10.
Meanwhile, \( \theta_{3,4} \geq 0 \), \( \theta_{5,6} \geq 0 \) and \( \theta_{3,4} + \theta_{5,6} \leq \frac{1}{2} \) are necessary to maintain proposed principle of operation. 

Figure 18 indicates the ZVS range of different AC DC voltage ratio that are independent from frequency. When \( \theta \geq 0.25 \), ZVS could always be guaranteed while would generate a larger circulating current. ZVS range is larger than single-phase-shift mode when \( \theta \leq 0.25 \).

\[
\begin{cases}
\theta_{5,6} \geq \frac{4f_s L_o I_{s,ac}}{|v_{ac}| + 2n v_{dc}} \\
\theta_{5,6} \geq \frac{4f_s L_o I_{s,dc}}{|v_{ac}| + 2n v_{dc}}
\end{cases}
\]  (2.10)

Fig. 18 ZVS Range of Dual-Phase-Shift Control

2.3. Dual-Phase-Shift Partial-Load Modulation Principle
2.3.1. Dual-Phase-Shift Partial-Load Modulation Operation Analysis

The voltage and current applied to the transformer and gate signal are presented in figure 19 when $V_{ac} > 0$ and figure 20 when $V_{ac} < 0$. In the modulation, $\theta_{3,4}$ is the phase shift percentage (from 0 to 1) between the primary bridge and bridge leg of $S_3$ and $S_4$, and $\theta_{5,6}$ is the phase shift percentage (from 0 to 1) between the primary bridge and bridge leg of $S_5$ and $S_6$. $T_s$ is the time period of a single switching period.
Fig. 19 Dual-Phase-Shift Partial-Load Modulation Operation Principle where $V_{ac} > 0$
Fig. 20 Dual-Phase-Shift Partial-Load Modulation Operation Principle where $V_{ac} < 0$

The leakage inductance current of transformer in DPSP modulation is calculated in equation (2.11).
\[ i_{t_a}(t) = \begin{cases} 
\frac{1}{2} |v_{ac}| \frac{(t - t_0) + i_{t_a}(t_0)}{L_s} & t_0 \leq t \leq t_1 \\
\frac{1}{2} |v_{ac}| - \frac{n v_{dc}}{L_s} (t - t_1) + i_{t_a}(t_1) & t_1 \leq t \leq t_2 \\
\frac{1}{2} |v_{ac}| \frac{(t - t_2) + i_{t_a}(t_2)}{L_s} & t_2 \leq t \leq t_3 \\
\frac{1}{2} |v_{ac}| \frac{(t - t_3) + i_{t_a}(t_3)}{L_s} & t_3 \leq t \leq t_4 \\
\frac{1}{2} |v_{ac}| + \frac{n v_{dc}}{L_s} (t - t_4) + i_{t_a}(t_4) & t_4 \leq t \leq t_5 \\
\frac{1}{2} |v_{ac}| \frac{(t - t_5) + i_{t_a}(t_5)}{L_s} & t_5 \leq t \leq t_6 
\end{cases} \] (2.11)

Where
\[
\begin{align*}
    i_{L_0}(t_0) &= \frac{-\frac{1}{4}|v_{ac}| + n\theta_{3,4}v_{dc}}{2f_sL_0} \\
    i_{L_0}(t_1) &= \frac{\left(\frac{1}{4} - \theta_{5,6} - \theta_{3,4}\right)|v_{ac}| + n\theta_{3,4}v_{dc}}{2f_sL_0} \\
    i_{L_0}(t_2) &= \frac{\left(\frac{1}{4} - \theta_{5,6}\right)|v_{ac}| - n\theta_{3,4}v_{dc}}{2f_sL_0} \\
    i_{L_0}(t_3) &= \frac{\frac{1}{4}|v_{ac}| - n\theta_{3,4}v_{dc}}{2f_sL_0} \\
    i_{L_0}(t_4) &= -\frac{\left(\frac{1}{4} - \theta_{5,6} - \theta_{3,4}\right)|v_{ac}| + n\theta_{3,4}v_{dc}}{2f_sL_0} \\
    i_{L_0}(t_5) &= \frac{-\left(\frac{1}{4} - \theta_{5,6}\right)|v_{ac}| + n\theta_{3,4}v_{dc}}{2f_sL_0}
\end{align*}
\]

The transferred instantaneous power in DPSP modulation is given in equation 2.12.

\[P(t) = \frac{n|v_{ac}|v_{dc}\theta_{3,4}(\frac{1}{2} - 2\theta_{5,6} - \theta_{3,4})}{2f_sL_0} \tag{2.12}\]

2.3.2. Zero Voltage Analysis in DPSP Modulation

To achieve ZVS in DPSP Modulation, both the absolute value of \(i_{L_0}(t_0)\) and \(i_{L_0}(t_1)\) should be large enough to charge and discharge the switch junction capacitor. The current value to achieve ZVS is included in equation 2.13 and 2.14. Equation 2.13 concludes the ZVS requirement for AC side.
\[ i_{t_a}(t_0) \leq -I_{s,ac} \]  

(2.13)

Where

\[ I_{s,ac} = \frac{v_{ac}}{\sqrt{L_0/C_{eq}}} \]

Equation 2.14 concludes the ZVS requirement for DC side.

\[ i_{t_a}(t_1) \geq I_{s,dc} \]
\[ i_{t_a}(t_2) \leq -I_{s,dc} \]

(2.14)

Where

\[ I_{s,dc} = \frac{v_{dc}}{\sqrt{L_0/C_{eq}}} \]

Combine equation 2.13 and equation 2.14, the range of phase shift could be derived.

To simplify calculation and maintain trapezoidal current shape, set \( i_{t_a}(t_0) = i_{t_a}(t_2) \), therefore the relationship of \( \theta_{3,4} \) and \( \theta_{5,6} \) could be derived in equation 2.15.

\[ \theta_{3,4} = \frac{v_{ac}(1 - 2\theta_{5,6})}{4nv_{dc}} \]

(2.15)

Combine equation 2.13, 2.14 and 2.15, the range of \( \theta_{5,6} \) phase shift could be derived in equation 2.16.
\[
\begin{align*}
\theta_{5,6} & \geq \frac{4f_s L_0 I_{\text{ac}}}{|v_{\text{ac}}|} \\
\theta_{5,6} & \geq \frac{4f_s L_0 I_{\text{dc}}}{|v_{\text{ac}}|} \\
\theta_{5,6} & \geq \frac{4f_s L_0 I_{\text{ac}} n v_{\text{dc}} / v_{\text{ac}} + \frac{1}{2} v_{\text{ac}} - n v_{\text{dc}}}{|v_{\text{ac}}| - 3 n v_{\text{dc}}} 
\end{align*}
\] (2.16)

Meanwhile, \( \theta_{3,4} \geq 0 \), \( \theta_{5,6} \geq 0 \) and \( \theta_{3,4} + \theta_{5,6} \leq \frac{1}{2} \) are necessary to maintain proposed principle of operation.

2.4. Conclusion

In this chapter, two modulations of half-bridge full-bridge dual-active-bridge topology are proposed. Single phase shift and dual phase shift modulation have been analyzed to discover its zero-voltage switching range.
CHAPTER 3 VARIABLE-SWITCHING-FREQUENCY DUAL-PHASE-SHIFT CONTROL ALGORITHM

As ZVS being fully analyzed during the chapter 2, PFC is also required to magnify the power transfer and to protect the equipment in the system. In this thesis, PFC is mainly achieved by frequency adjustment. [16] and [19] indicates a variable frequency control.

3.1. Variable Frequency Power Factor Correction Control Algorithm

3.1.1 Theoretical Analysis of Variable Frequency Power Factor Correction Control

To realize zero voltage switching for GaN transistor, certain negative communication current that used to charge and discharge junction capacitance is necessary. For transistors in both AC side and DC side, the minimum communication current is listed in equation 3.1 and 3.2.

\[
I_{s,\text{ac}} = \frac{v_{ac}}{\sqrt{L_0/C_{\text{eq,ac}}}} \quad (3.1)
\]

\[
I_{s,\text{dc}} = \frac{v_{dc}}{\sqrt{L_0/C_{\text{eq,dc}}}} \quad (3.2)
\]

Since this control method of bidirectional dual-active-bridge topology should operate on both AC-DC and DC-AC situation, in figure 15, both absolute value \(i_{L_{t_1}}(t_1)\) and \(i_{L_{t_3}}(t_3)\) should be larger than \(I_{s,\text{ac}}\) and \(I_{s,\text{dc}}\). Set \(I_s = \max\{I_{s,\text{ac}}, I_{s,\text{dc}}\}\), therefore,

\[
\begin{align*}
\left[ i_{L_{t_1}}(t_1) \right] & \leq -I_s \\
\left[ i_{L_{t_3}}(t_3) \right] & \geq I_s
\end{align*}
\quad (3.3)
\]

To simplify calculation and maintain trapezoidal current shape, set \(i_{L_{t_1}}(t_1) = i_{L_{t_3}}(t_3)\),
therefore the relationship of $\theta_{3,4}$ and $\theta_{5,6}$ could be derived in equation 3.4.

$$\theta_{3,4} = \frac{v_{ac}(1 - 2\theta_{5,6})}{4nv_{dc}}$$  \hspace{1cm} (3.4)

Combine equation 3.3 and 3.4, the range of $\theta_{5,6}$ phase shift could be derived in equation 3.5.

$$\theta_{5,6} \geq \frac{4f_sL_{s}I_s}{|v_{ac}| + 2nv_{dc}}$$ \hspace{1cm} (3.5)

Meanwhile, $\theta_{3,4} \geq 0$, $\theta_{5,6} \geq 0$ and $\theta_{3,4} + \theta_{5,6} \leq \frac{1}{2}$ are necessary to maintain proposed principle of operation.

To achieve unity power factor in the AC side, the half bridge capacitor should be considered while matching the transformer power flow and AC side power flow. A power equation for transformer is stated in equation 3.6.

$$P_{pfc}(t) = V_{ac}I_{ac} \sin^2(\omega t) - \frac{\omega(C_1 + C_2)}{4} \sin(\omega t) \cos(\omega t)$$ \hspace{1cm} (3.6)

In DPSR, power flow is stated in equation 3.7.

$$P_{DPSR}(t) = \frac{n|V_{ac}|v_{dc}(-2\theta_{3,4}^2 - 2\theta_{5,6}^2 + \theta_{3,4} + \theta_{5,6})}{4f_sL_s}$$ \hspace{1cm} (3.7)

Therefore, $P_{DPSR}(t) = P_{pfc}(t)$ is made in order to achieve power factor correction.

For given phase shift $\theta_{3,4}$ and $\theta_{5,6}$, a switching frequency could be derived in equation 3.8.

$$f_s = \frac{n|V_{ac}|v_{dc}(-2\theta_{3,4}^2 - 2\theta_{5,6}^2 + \theta_{3,4} + \theta_{5,6})}{4L_sP_{pfc}(t)}$$ \hspace{1cm} (3.8)
Since the relationship of \( \theta_{3,4} \) and \( \theta_{5,6} \) is derived in equation 3.4, From a certain phase, the maximum value of \( P_{DPSR} \) could be derived in equation 3.9.

\[
P_{DPSR,\text{max}}(t) = \frac{nv_{dc}|v_{ac}|(v_{ac}^2 + 4nv_{dc}|v_{ac}| + 4n^2v_{dc}^2)}{32f_sL_d(v_{ac}^2 + 4nv_{dc}^2)}
\]  

(3.9)

In this situation, the value of \( \theta_{5,6} \) could be realized in equation 3.10.

\[
\theta_{5,6,\text{max}} = \frac{v_{ac}^2 - nv_{dc}|v_{ac}| + 2n^2v_{dc}^2}{2(v_{ac}^2 + 4nv_{dc}^2)}
\]  

(3.10)

Since the range of \( \theta_{5,6} \) already be derived in equation 3.5, the minimum value of \( \theta_{5,6} \) could be derived in equation 3.11.

\[
\theta_{5,6,\text{min}} = \frac{4f_sL_iI_s}{|v_{ac}| + 2nv_{dc}}
\]  

(3.11)

To ensure zero voltage switching, the switching phase \( \theta_{5,6} \) should be larger than \( \theta_{5,6,\text{min}} \) and leave a margin that is large enough. Therefore, a switching phase \( \theta_{5,6,\text{av}} \) is introduced to provide average amount of power between the maximum and minimum power, and it is shown in equation 3.12.

\[
\theta_{5,6,\text{av}} = \frac{\alpha|v_{ac}|^3 + (\alpha n v_{dc} + \beta)v_{ac}^2 + 4\alpha n^3v_{dc}^3 + 4\beta n^2v_{dc}^2}{4(v_{ac}^2 + 4n^2v_{dc}^2)(|v_{ac}| + 2nv_{dc})}
\]  

(3.12)

Where

\[
\alpha = 2 - \sqrt{2}
\]

\[
\beta = 8\sqrt{2}f_sL_iI_s
\]
Combine equation 3.4, 3.8 and 3.12, the power for $\theta_{5,6,max}$, $\theta_{5,6,av}$ and $\theta_{5,6,min}$ in half cycle is shown in figure 21.

![Figure 21](image_url)

3.1.2. Zero Crossing Improvement of Variable Frequency Power Factor Correction Control Algorithm

According to equation 3.8, it is obvious that for a relatively low $P_{pfc}$, $f_s$ could be rather high. In practical, an upper limitation of $f_s$ is reasonable since hardware could not stand an ultra-high switching frequency. Since the requirement of power factor is fulfilled by
switching frequency, it could not be achieved while $f_s$ is beyond frequency limitation in equation 3.8. The instantaneous power needed for a 1.6 kW power factor correction control is shown in figure 22.

![Instantaneous Power needed for a 1.6 kW Power Factor Correction Control](image)

Fig. 22 Instantaneous Power needed for a 1.6 kW Power Factor Correction Control

While in most time, $P_{pfc}$ is equal to $P_{av}$, it becomes separate while frequency reaches its limitation. The image around frequency reaches its limitation of power transfer of $\theta_{5,6,\text{max}}$, $\theta_{5,6,\text{av}}$ and $\theta_{5,6,\text{min}}$ is shown in figure 23.
Fig. 23 Power Transfer of $\theta_{5,6,\text{max}}$, $\theta_{5,6,\text{av}}$ and $\theta_{5,6,\text{min}}$ around Zero Crossing

Moreover, the power transfer should at least above the requirement ZVS in order to limit the switching loss, which means it should above the $P_{\text{min}}$. The control strategy of zero-crossing situation has two modulations.

Modulation 1 is shown in figure 24. Modulation 1 starts from zero-crossing point and follows $P_{\text{min}}$ until the crossing point of $P_{\text{min}}$ and $P_{\text{pfc}}$. Then it follows $P_{\text{pfc}}$ in the main range until next crossing point of $P_{\text{min}}$ and $P_{\text{pfc}}$. 

![Graph showing power transfer and frequency limitation border](image-url)
Fig. 24 Modulation 1 for Zero-Crossing Improvement

Modulation 2 is shown in figure 25, Modulation 2 starts from zero-crossing point and follows $P_{\min}$ until switching frequency behind its limitation. Then it follows $P_{pfc}$ in the main range until next time the switching frequency reaches its limitation.
Fig. 25 Modulation 2 for Zero-Crossing Improvement

3.1.3 Simulation Result of Variable Frequency Power Factor Correction Control

To demonstrate the rated-load variable frequency power factor correction control, a simulation is made. The simulation software is Matlab/Simulink, with input voltage of 240Vrms, output voltage of 48V and operation power for 1.6kW. The system parameter is shown in table 1.
Table 1 System Parameter of Variable Frequency Power Factor Correction Control

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_m$</td>
<td>Grid Frequency</td>
<td>60Hz</td>
</tr>
<tr>
<td>$f_s$</td>
<td>Switching Frequency</td>
<td>80-500kHz</td>
</tr>
<tr>
<td>$V_{ac}$</td>
<td>Grid Voltage</td>
<td>240Vrms</td>
</tr>
<tr>
<td>$V_{dc}$</td>
<td>Battery Voltage</td>
<td>48V</td>
</tr>
<tr>
<td>$L_{ac}$</td>
<td>AC Side Inductor</td>
<td>4mH</td>
</tr>
<tr>
<td>$C_1$, $C_2$</td>
<td>Capacitor</td>
<td>1.5µF</td>
</tr>
<tr>
<td>$C_{eq}$</td>
<td>Switch Junction Capacitor</td>
<td>130pF</td>
</tr>
<tr>
<td>$L_\delta$</td>
<td>Transformer Leakage</td>
<td>20µH</td>
</tr>
<tr>
<td>$n$</td>
<td>Transformer Turn Ratio</td>
<td>5:1</td>
</tr>
<tr>
<td>$P$</td>
<td>Power Transfer</td>
<td>1.6kW</td>
</tr>
</tbody>
</table>

Figure 26 shows the waveform of control variable $\theta_{3,4}$, $\theta_{5,6}$ and switching frequency $f_s$ during half grid period. The frequency limitation is applied during zero-crossing period. In this period, $\theta_{5,6}$ is kept to minimum value to ensure zero voltage switching.
Fig. 26 Waveform of Control Variable $\theta_{3,4}$, $\theta_{5,6}$ and Switching Frequency $f_s$

Figure 27 indicates the waveform of AC and DC side transformer voltage and transformer leakage current. The transformer AC side voltage would change during half grid frequency period. Figure 28 further shows the zoom-in waveform of AC and DC side transformer voltage and transformer leakage current. The zoom-in waveform could match the theoretical analyze of dual-active bridge transformer leakage inductor current.
Fig. 27 Waveform of AC, DC Side Transformer Voltage and Leakage Inductance Current for Half Grid Period
Fig. 28 Zoom-In Waveform of AC, DC Side Transformer Voltage and Leakage Inductance Current for 5 Switching Period

Figure 29 shows the ZVS result of variable-frequency dual-phase-shift modulation. All switches of AC and DC side could achieve ZVS during whole grid frequency period. In Simulink simulation, the ZVS could be seen as achieved if the current is negative when the transistor is on. In this situation, the transistor turn-on loss is negligible.
From system level, given the parameter in table 3.1, for an AC input voltage of 240V\textit{rms} and a DC output of 48V, for a power flow of 1.6kW, the AC voltage (grid voltage), AC current, AC power input and DC voltage is shown in figure 30. In this situation, this topology deliver 1600W active power, 1.2W reactive power with 3.5% total harmonic distortion.
3.2 Partial-Load Variable Frequency Power Factor Correction Control

3.2.1 Theoretical Analysis of Partial-Load Variable Frequency Power Factor Correction Control

To realize zero voltage switching for GaN transistor, certain negative communication current that used to charge and discharge junction capacitance is necessary. For transistors in both AC side and DC side, the minimum communication current is listed in equation 3.13 and 3.14.
\[ i_{L_o}(t_0) \leq -I_{s,ac} \quad (3.13) \]

Where

\[ I_{s,ac} = \frac{v_{ac}}{\sqrt{L_o / C_{eq}}} \]

Equation 3.14 concludes the ZVS requirement for DC side.

\[ i_{L_o}(t_1) \geq I_{s,dc} \]
\[ i_{L_o}(t_2) \leq -I_{s,dc} \quad (3.14) \]

Where

\[ I_{s,dc} = \frac{v_{dc}}{\sqrt{L_o / C_{eq}}} \]

Combine equation 3.13 and equation 3.14, the range of phase shift could be derived.

To simplify calculation and maintain trapezoidal current shape, set \( i_{L_o}(t_0) = i_{L_o}(t_2) \), therefore the relationship of \( \theta_{3,4} \) and \( \theta_{5,6} \) could be derived in equation 3.15.

\[ \theta_{3,4} = \frac{v_{ac}(1-2\theta_{5,6})}{4nv_{dc}} \quad (3.15) \]

Combine equation 3.13, 3.14 and 3.15, the range of \( \theta_{5,6} \) phase shift could be derived in equation 3.16.
\[
\begin{align*}
\theta_{5,6} & \geq \frac{4 f_s L_\delta I_{r,ac}}{|v_{ac}|} \\
\theta_{5,6} & \geq \frac{4 f_s L_\delta I_{r,dc}}{|v_{ac}|} \\
\theta_{5,6} & \geq \frac{4 f_s L_\delta I_{r,dc} n v_{dc} / v_{ac} + \frac{1}{2} v_{ac} - n v_{dc}}{|v_{ac}| - 3 n v_{dc}}
\end{align*}
\]

(3.16)

Meanwhile, \( \theta_{3,4} \geq 0 \), \( \theta_{5,6} \geq 0 \) and \( \theta_{3,4} + \theta_{5,6} \leq \frac{1}{2} \) are necessary to maintain proposed principle of operation.

To achieve unity power factor in the AC side, the half bridge capacitor should be considered while matching the transformer power flow and AC side power flow. A power equation for transformer is stated in equation 3.17.

\[
P_{pfc}(t) = V_{ac} I_{ac} \sin^2(\omega t) - \frac{\omega(C_1 + C_2)}{4} \sin(\omega t) \cos(\omega t)
\]

(3.17)

In DPSP, power flow is stated in equation 3.18.

\[
P_{DPSP}(t) = \frac{n |v_{ac}| v_{dc} \theta_{3,4} (1 - 4 \theta_{5,6} - 2 \theta_{3,4})}{4 f_s L_\delta}
\]

(3.18)

Therefore, \( P_{DPSP}(t) = P_{pfc}(t) \) is made in order to achieve power factor correction. For given phase shift \( \theta_{3,4} \) and \( \theta_{5,6} \), a switching frequency could be derived in equation 3.19.

\[
f_s = \frac{n |v_{ac}| v_{dc} \theta_{3,4} (1 - 4 \theta_{5,6} - 2 \theta_{3,4})}{4 L_\delta P_{pfc}(t)}
\]

(3.19)
3.2.2 Simulation Result of Partial-Load Variable Frequency Power Factor Correction Control

To demonstrate the partial-load variable frequency power factor correction control, a simulation is made. The simulation software is Matlab/Simulink, with input voltage of 240\textit{Vrms}, output voltage of 48\textit{V} and operation power for 360\textit{W}. The system parameter is shown in table 2.

Table 2 System Parameter of Variable Frequency Power Factor Correction Control

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>( f_m )</td>
<td>Grid Frequency</td>
<td>60\textit{Hz}</td>
</tr>
<tr>
<td>( f_s )</td>
<td>Switching Frequency</td>
<td>80-500\textit{kHz}</td>
</tr>
<tr>
<td>( V_{ac} )</td>
<td>Grid Voltage</td>
<td>240\textit{Vrms}</td>
</tr>
<tr>
<td>( V_{dc} )</td>
<td>Battery Voltage</td>
<td>48\textit{V}</td>
</tr>
<tr>
<td>( L_{ac} )</td>
<td>AC Side Inductor</td>
<td>4\textit{mH}</td>
</tr>
<tr>
<td>( C_1, C_2 )</td>
<td>Capacitor</td>
<td>1.5\textit{\mu F}</td>
</tr>
<tr>
<td>( C_{eq} )</td>
<td>Switch Junction Capacitor</td>
<td>130\textit{pF}</td>
</tr>
<tr>
<td>( L_\delta )</td>
<td>Transformer Leakage Inductance</td>
<td>20\textit{\mu H}</td>
</tr>
<tr>
<td>( n )</td>
<td>Transformer Turn Ratio</td>
<td>5:1</td>
</tr>
<tr>
<td>( P )</td>
<td>Power Transfer</td>
<td>360\textit{W}</td>
</tr>
</tbody>
</table>

Figure 31 shows the waveform of control variable \( \theta_{3,4}, \theta_{5,6} \) and switching frequency \( f_s \) during half grid period. The frequency limitation is applied during zero-crossing period. In this period, \( \theta_{5,6} \) is kept to minimum value to ensure zero voltage switching.
Fig.31 Waveform of Control Variable $\theta_{3,4}$, $\theta_{5,6}$ and Switching Frequency $f_s$

Figure 32 indicates the waveform of AC and DC side transformer voltage and transformer leakage current. The transformer AC side voltage would change during half grid frequency period. Figure 33 further shows the zoom-in waveform of AC and DC side transformer voltage and transformer leakage current. The zoom-in waveform could match the theoretical analyze of dual-active bridge transformer leakage inductor current.
Fig. 32 Waveform of AC, DC Side Transformer Voltage and Leakage Inductance Current for Half Grid Period
Figure 34 shows the ZVS result of variable-frequency dual-phase-shift modulation. All switches of AC and DC side could achieve ZVS during whole grid frequency period. In Simulink simulation, the ZVS could be seen as achieved if the current is negative when the transistor is on. In this situation, the transistor turn-on loss is negligible.
Fig. 34 ZVS Turn-on of AC and DC Side Transistor during 4 Switching Period

From system level, given the parameter in Table 3.2, for an AC input voltage of 240Vrms and a DC output of 48V, for a power flow of 360W, the AC voltage (grid voltage), AC current, AC power input and DC voltage is shown in Figure 35. In this situation, this topology delivers 360W active power, 12W reactive power with 8% total harmonic distortion.
Fig. 35 Waveform of AC voltage, AC current, AC power input and DC voltage

As Compared, if the DPSR is applied in this situation, the THD could be rather high. A simulation is running where 330W power transferred. In this situation, this topology deliver 330W active power, 152W reactive power with 12% total harmonic distortion. The waveform of AC voltage, AC current, AC power input and DC voltage is shown in figure 36.
3.3 Conclusion

In this chapter, partial-load variable frequency dual-phase-shift control and rated-load variable frequency dual-phase-shift control are proposed in this single-stage AC-DC converter. This two control method could achieve unity power factor and maintain ZVS. The proposed partial-load control method could significantly reduce the THD and reactive power in partial load situation.
CHAPTER 4 EXPERIMENTAL VERIFICATION OF VARIABLE FREQUENCY DUAL PHASE SHIFT DUAL ACTIVE BRIDGE

4.1. System Hardware Design and Assemble

4.1.1. High Voltage Power Stage Design

High voltage power stage based on GaN transistor requires a low loop inductance. Therefore, a design for power stage is applied. This vertical power path structure design is shown in figure 37. In this design, power stage output and input is connected by a capacitor where the power path is overlap, and the area included could be reduced to minimum. For a minimum area included, the loop inductance could be reduced to minimum. This vertical power path structure diagram from top view is shown in figure 38 from top view.
Figure 39 shows the applied design in power stage in the proposed version of PCB. The double pulse test of high voltage power stage would be included in subchapter 4.2.

4.1.2. Low Voltage Power Stage Assemble

Low voltage power stage has higher current stress compare to the high voltage power stage. This thesis use a previous designed low power stage GaN card with state of art enhancement mode GaN transistor and GaN gate driver. Without laser cutting of PCB, the
copper pad is not ideal, and therefore have challenge to solder. Figure 40 shows the copper pad of GaN half bridge gate driver LM5113.

With length of $1.2mm$, LM5113 is not considered easy to solder, and since the low voltage GaN card have 12 layer and thickness of $3mm$, the standard EPC solder procedure could not fulfill due to the thickness of PCB. Figure 41 shows the situation following EPC solder procedure.

![Fig.41 Failure Pad Attachment of LM5113](image)

In this situation, a stencil is necessary to put the exact amount of solder paste without making it shorted, and it could provide enough solder paste to make sure it could attach to the pad in a certain temperature.

![Fig.42 Proper Pad Attachment of LM5113](image)

[20] indicates a reference procedure of die attach. Figure 42 shows the proper pad attachment of LM5113. With stencil, the pad is connected to BGA.
4.1.3. System PCB Design

The system includes AC power stage, transformer, DC power stage (previous design), analog to digital converter (ADC), digital to analog (DAC), PWM and protection. Figure 43 indicates the system structure diagram. Figure 44 shows the area distribution of PCB.
4.2. System Operation Experimental Result

4.2.1. High Voltage Power Stage Double Pulse Test

Double pulse test is a useful way to test the power stage design. Figure 45 shows the double pulse test circuit while $S_{1a}$ and $S_{2a}$ switch, or $S_{1b}$ and $S_{2b}$ switch.

![Double Pulse Test Circuit](image)

(a) $S_{1a}$ and $S_{2a}$ Switch  
(b) $S_{1b}$ and $S_{2b}$ Switch

Fig.45 Double Pulse Test Circuit

Table 3 shows the system parameter of double pulse test. This system runs with DC voltage of 400V and inductance of $11\mu H$.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{dc}$</td>
<td>DC Voltage</td>
<td>400V</td>
</tr>
<tr>
<td>$t_{pulse}$</td>
<td>Pulse Width</td>
<td>500ns</td>
</tr>
<tr>
<td>$L$</td>
<td>Inductance</td>
<td>$11\mu H$</td>
</tr>
<tr>
<td>$I_{max}$</td>
<td>Maximum Current</td>
<td>25A</td>
</tr>
</tbody>
</table>
Figure 46 indicates the \( V_{ds} \) of low side transistor and inductor current when double pulse test, and figure 47 indicates the detailed figure of figure 46.

(a) First Low Side Transistor Turn On
(b) First Low Side Transistor Turn Off
(c) Second Low Side Transistor Turn On
(d) Second Low Side Transistor Turn Off

Fig. 47 Detailed figure of Low Side Transistor \( V_{ds} \) and Inductor Current
Since the control method of this thesis have zero-voltage-switch, the value of turn off energy should be considered as priority. The turn off time is the key of turn off energy. The turn off time while current is 12.5 A is 20 ns, with $dv/dt$ of 20V/ns. 10 ns while current is 25 A, with $dv/dt$ of 40V/ns.

4.2.2. Low Voltage GaN Card Buck Mode Test

Buck mode test is a useful way to test the power stage design long time performance.

Figure 48 shows the buck mode test circuit. Table 4 shows the system parameter of buck mode test.

![Buck Mode Test Circuit](image)

**Table 4 System Parameter of Buck Mode Test**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{dc}$</td>
<td>Input Voltage</td>
<td>30V</td>
</tr>
<tr>
<td>$I_{dc}$</td>
<td>Input Current</td>
<td>10A</td>
</tr>
<tr>
<td>$f_{sw}$</td>
<td>Switch Frequency</td>
<td>100kHz</td>
</tr>
<tr>
<td>$L_1, L_2$</td>
<td>Inductance</td>
<td>11µH</td>
</tr>
<tr>
<td>$C_{load}$</td>
<td>Load Capacitor</td>
<td>3600µF</td>
</tr>
</tbody>
</table>
Figure 49 indicates the waveform of buck mode test. Channel 1 and 2 shows the $V_{ds}$ of $S_4$ and $S_6$, Channel 3 and 4 shows the current of $L_1$ and $L_2$. Figure 50 shows the thermal performance of buck mode test. During this test, no fan or heat sink is used. The maximum transistor temperature is 62.5 °C, and the average transistor temperature is 60 °C.
4.2.3. System Test under DC-AC Mode

After AC high voltage power stage and DC low power stage is design and tested, a system assemble and test is realized. Figure 51 shows the experimental prototype of this single-stage bidirectional AC-DC converter.

![Experimental Prototype of Single-Stage Bidirectional AC-DC Converter](image)

Table 5 shows the system parameter of DC-AC Mode.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_m$</td>
<td>Grid Frequency</td>
<td>60Hz</td>
</tr>
<tr>
<td>$f_s$</td>
<td>Switching Frequency</td>
<td>80-250kHz</td>
</tr>
<tr>
<td>$V_{ac}$</td>
<td>AC Voltage</td>
<td>100V$_{rms}$</td>
</tr>
<tr>
<td>$V_{dc}$</td>
<td>DC Voltage</td>
<td>24V</td>
</tr>
<tr>
<td>$L_{ac}$</td>
<td>AC Side Inductor</td>
<td>4mH</td>
</tr>
<tr>
<td>$C_1, C_2$</td>
<td>Capacitor</td>
<td>1.5µF</td>
</tr>
<tr>
<td>$C_{eq}$</td>
<td>Switch Junction Capacitor</td>
<td>130pF</td>
</tr>
<tr>
<td>---------</td>
<td>--------------------------</td>
<td>-------</td>
</tr>
<tr>
<td>$L_δ$</td>
<td>Transformer Leakage Inductance</td>
<td>10µH</td>
</tr>
<tr>
<td>$n$</td>
<td>Transformer Turn Ratio</td>
<td>5:1</td>
</tr>
<tr>
<td>$P$</td>
<td>Rated Power Transfer</td>
<td>1.6kW</td>
</tr>
</tbody>
</table>

Figure 5.2 shows the waveform of experimental test result. Channel 1 shows the AC voltage, channel 2 shows the transformer AC side voltage, channel 3 shows the transformer DC side voltage, and channel 4 shows the leakage inductance current. Figure 5.3 shows the detailed waveform of figure 5.2, where the operation is similar with the control mode mentioned on chapter 3.

![Fig.52 Waveform of Experimental DC-AC Operation Result](image_url)
Fig. 53 Detailed Waveform of Experimental DC-AC Operation Result

Fig. 54 Thermal Performance of Experimental DC-AC Operation Result

Figure 54 shows the thermal performance under operation of 270W, with no fan or heat sink used. The Maximum temperature is 59.5°C under this situation.
4.3. Conclusion

In this chapter, an experimental prototype is designed and tested.

A high voltage AC power stage is design and tested with double pulse test. A low voltage DC power stage is assembled and tested with buck mode tested.

A system PCB is designed includes AC power stage, transformer, DC power stage (previous design), analog to digital converter (ADC), digital to analog (DAC), PWM and protection.

The System is tested under DC-AC mode with unity power factor.
CHAPTER 5 CONCLUSION AND FUTURE WORK

5.1. Conclusion

This thesis mainly focus on the design and control of a single-stage single-phase bidirectional dual-active-bridge isolated AC-DC converter based on GaN transistor.

Chapter 1 introduces the background of energy storage device and the advantage of dual-active-bridge as a single stage AC-DC converter. This chapter compare several types of two-stage AC-DC converter.

Chapter 2 presents the theoretical analysis of single-phase-shift, dual-phase-shift rated-load, and dual-phase-shift partial-load control method and its zero-voltage-switch (ZVS) realization. This chapter discusses the range of ZVS of each control method.

Chapter 3 states the theoretical analysis of variable-frequency control to achieve power-factor-correction (PFC) and zero-crossing improvement, and includes the partial-load analyze of its ability of achieving PFC. This chapter also includes simulation in Matlab Simulink to achieve expected function.

Chapter 4 shows the AC power stage design and DC power stage assemble. Both power stage test is included in this chapter. A system experimental verification is states in this chapter to achieve the expected function in DC-AC operation.

5.2. Future Work

The future research work on this topic can be focused on the following aspects:

(1) AC-DC mode test and DC-AC mode test with battery;

(2) Close loop control;

(3) Further optimization in power density, magnetic component and efficiency.
REFERENCES


