ABSTRACT

XU, YANG. Development of Advanced SiC Power Modules (Under the direction of Dr. Douglas C. Hopkins)

Fast adoption of wide-bandgap (WBG) semiconductor technology in today’s power electronics is currently being heavily pursued by industry, academia and government. Although the WBG power device is superior to silicon counterpart in both transient and steady-state performance, the WBG power packaging technology remains basically the same as has been used in silicon power packaging. A traditional power module uses metal clad ceramic (e.g. DBC or DBA) bonded to a baseplate that creates a highly thermally resistive path, and wire bond interconnect that introduces substantial inductance and limits thermal management to single-sided cooling. Advanced power modules are needed to make full use of the high-performance SiC power devices. In this work, finite element analysis (FEA) based multi-physics approach for power module design has been proposed and applied to SiC power module design cases. Two innovative double-sided power module structures have been proposed and studied. The performance advantages of these new modules have been proven by simulation and partially by experiments. Fabrication processes have also been proposed.

The research is organized as the following:

Chapter 1 introduces the properties of silicon carbide (SiC) power semiconductor devices and reviews various power module technologies and electric vehicle inverter/converter topologies. Power module parasitic elements, particularly inductance, that influence switching transients and methods for extracting values for such elements are also discussed.

Chapter 2 investigates the power module substrate thermal spreading behavior and the resulting thermal design considerations. Thermal-mechanical optimization for power
substrates is demonstrated, and applied through a case study using multi-physics finite element analysis (FEA) of a 6.5 kV/10kV SiC power module.

Chapter 3 proposes Power Chip on Bus (PCoB) power module design that reduces parasitic inductances through an integrated power interconnect structure. The PCoB maximizes thermal performance by directly attaching power chips to the busbar, integrating the heatsink and busbar as one, and using a dielectric fluid, such as air, for electrical isolation. This new power module topology features all planar interconnects and double-sided air cooling. Performance evaluations are carried out through comprehensive electrical and multi-physics simulation and thermal test. Fabrication and assembly processes are included. Ultra-low parasitic inductance and thermal resistance have been validated. A single switch version of PCoB module is fabricated. A double-pulse tester has been designed and assembled, and used for module switching tests. Chapter 5 concludes the dissertation with a discussion of future work.
Development of Advanced SiC Power Modules

by
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DEDICATION

To my parents
BIOGRAPHY

The author was born in the city of Wuhan, Hubei, China. He received B.S. degree in Automation from Shanghai University of Electric Power, Shanghai, China in 2009. The author then received the M.S degree in Electrical Engineering from State University of New York at Buffalo in 2011. From 2011, he started to pursue Ph.D. degree in North Caroline State University Department of Electrical and Computer Engineering. During the time in NC State, his research projects are associated with National Science Foundation (NSF) Future Renewable Electric Energy Delivery and Management (FREEDM) system center, and the US Department of Energy (DoE) Power America Institute. He is a co-founding developer of the NCSU Laboratory for Packaging Research in Electronic Energy Systems (PREES). He was an intern power packaging engineer at RF Micro devices (now Qorvo) headquarter in Greensboro, North Carolina from May to August 2014. His research interests include advanced power package design, fabrication, multi-physics simulation and power electronic systems integration. Upon graduation, he will join Tesla Motors headquarter at Palo Alto, California as a senior electronic design engineer.
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Chapter 1. Introduction

1.1 SiC Power Device

The critical breakdown electric field strength of SiC is about 10 times that of Si. Therefore, SiC devices can be made with much thinner drift layer or higher doping concentration. So the SiC power semiconductor device features high blocking voltage and low on-state resistance. In addition, the SiC power device can also switch faster with lower switching loss. The larger bandgap of SiC material leads to much lower intrinsic carrier density, which makes SiC devices capable for operation at 200 °C and even higher. Key material properties of Si and SiC are listed in Table 1.1. The causal relationship between SiC material properties and performance advantages is shown in Figure 1.1

<table>
<thead>
<tr>
<th>Properties</th>
<th>Silicon</th>
<th>4H-SiC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Energy Band Gap (eV)</td>
<td>1.11</td>
<td>3.26</td>
</tr>
<tr>
<td>Relative Dielectric Constant</td>
<td>11.7</td>
<td>9.7</td>
</tr>
<tr>
<td>Thermal Conductivity (W/cm-K)</td>
<td>1.5</td>
<td>3.7</td>
</tr>
<tr>
<td>Electron Affinity (eV)</td>
<td>4.05</td>
<td>3.7</td>
</tr>
<tr>
<td>Density of States Conduction Band (cm^{-3})</td>
<td>(2.80 \times 10^{19})</td>
<td>(1.23 \times 10^{19})</td>
</tr>
<tr>
<td>Density of States Valence Band (cm^{-3})</td>
<td>(1.04 \times 10^{19})</td>
<td>(4.58 \times 10^{18})</td>
</tr>
</tbody>
</table>
1.2 Conventional Power Module

Discrete power package provides a low-cost, reliable and flexible solution for wide range of power electronic application. By using discrete power packages, the power devices are mounted on PCB boards which are flexible to layout. The PCB board may introduce significant amount of parasitic inductance which is not desirable for fast switching and current sharing between paralleled power switches. Also the power device thermal interface material introduces significant amount of thermal resistance. However, by very careful design and the adoption of special PCB features, those thermal and electrical issues can be largely solved.

In most power electronic applications multi-die (multichip) power modules provide better thermal and electrical performance and higher power density compared to using multiple discrete-packaged power devices for the same power circuit topology. As shown in Figure 1.2 and Figure 1.3, the conventional multichip power modules are comprised of power semiconductor die,
interconnect, insulation substrate, metal base plate, encapsulation material and housing [2]. The power semiconductor dies include power diode, power MOSFET, IGBT and so on. These brittle power semiconductor devices function as an electrical switch in power electronic circuits and dissipate significant amount of heat during current conduction and switching. Thus, thermal dissipation and mechanical stress management are the two most important considerations for any power module design. The interconnections on “top-side” of the die is usually done through flexible welded interconnects (FWIs), such as bond wires and ribbons. Bond wires in most cases are made of aluminum or gold. Very thin bondwires of less than a mil (25µm) in diameter are usually made of gold. Thicker wires and ribbon are usually of aluminum, but research and development of copper wire is popular today for an “all copper interconnect system” [3]. The “bottom-side” of the die interconnects to an electrically insulating substrate by soldering, and the substrate is then attached typically with solder to baseplate. The insulating substrate is typically a Cu/dielectric/Cu or Al/dielectric/Al structure where the top metal is for electrical conduction and the bottom copper is for mechanical stress balance, thermal spreading and substrate soldering. The substrate dielectric is usually ceramic materials such as alumina, aluminum nitride, silicon nitride and beryllium oxide. Critical properties are given in Table 1.2. The base plate is usually made of Ni-plated copper for regular applications or copper/molybdenum or aluminum/silicon carbide metal matrix composite (AlSiC) for thermal-stress sensitive applications.

<table>
<thead>
<tr>
<th>Material</th>
<th>Resistivity (Ω-cm)</th>
<th>Dielectric Strength (kV/mm)</th>
<th>Dielectric Constant at 1MHz</th>
<th>Thermal Conductivity (W/mK)</th>
<th>CTE (ppm/C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Al₂O₃ (96%)</td>
<td>&gt; 10¹⁴</td>
<td>12</td>
<td>9.2</td>
<td>24</td>
<td>6.0</td>
</tr>
<tr>
<td>Al₂O₃ (99%)</td>
<td>&gt; 10¹⁴</td>
<td>12</td>
<td>9.9</td>
<td>33</td>
<td>7.2</td>
</tr>
<tr>
<td>AlN</td>
<td>&gt; 10¹⁴</td>
<td>15</td>
<td>8.9</td>
<td>150-180</td>
<td>4.6</td>
</tr>
<tr>
<td>BeO</td>
<td>&gt; 10¹⁴</td>
<td>12</td>
<td>6.7</td>
<td>270</td>
<td>7.0</td>
</tr>
</tbody>
</table>
Although the above mentioned conventional power module has advantages of good reliability, easy fabrication and relatively low cost, the electrical and thermal performances are limited by its structural topology. The wire bond has significant amounts of parasitic inductances which is a primary obstacle for high switching speed of the wide bandgap power semiconductors, and limits the density and performance of power electronics that utilize WBG devices. Also, the top-side of the die cannot dissipate much heat when interconnected with wire bonds. Wirebond and die-attach reliability is the bottle neck to increasing conventional power module power-cycling reliability.

1.3 Power Module Parasitic Inductance

Parasitics parameters are critical for power module electrical performance. Minimizing the parasitic parameters has become one of the major driving forces for new power module technology. Power interconnect parasitic resistance introduces extra thermal loss. Parasitic capacitance between source and drain or collector and emitter of each device slows down the switching transient. Parasitic inductance is of the most concern for it causes large voltage spikes.
when rapid current change exists. Parasitic inductance is associated with power device overvoltage transient and high switching loss, all of which are detrimental for fast switching. Thus, it is very important to understand the influence of parasitic inductance and how to extract it from a physical design.

1.3.1 Introduction to Gate Loop Inductance

The gate loop parasitic impedance has significant influence on the switching transient. An R, L, C circuit can be used to describe the gate loop dynamic response during the process of charging the gate voltage from negative bias to MOSFET threshold voltage. The R is the sum of device internal gate resistance and external gate driver resistance. The L is the parasitic inductance associated with the gate loop, which includes package and gate driver PCB parasitic inductances. The C is the MOSFET input capacitor.

\[ R_{\text{critical}} = 2 \cdot \sqrt{L/C} \]  

Equation 1.1 determines the loop resistance needed for avoiding oscillation. The higher the gate loop inductance, the larger the loop resistance is needed to suppress gate voltage oscillation. Take 1200V, 50A rated CREE’s C2M0025120D SiC MOSFET for example, the internal gate resistance is 1.1 Ohms and the input capacitance is 2788 pF. A set of R,L,C circuit simulations indicate the gate voltage transient at different loop resistance values, as can be seen in Figures 1.4 and 1.5. The reduction of the gate loop inductance will result in a much lower resistance needed to suppress oscillations, and, thus, provide a much faster gate voltage transition.
Figure 1. 4 Gate voltage for gate loop inductance of 26 nH

Figure 1. 5 Gate voltage for gate loop inductance of 10 nH
1.3.2 Gate Driver Parasitic Extraction

Parasitic inductance introduced by a gate drive board is critical for mitigating switching transients. Conducted in this research was an investigation of gate driver loop inductance in circuits implemented through PCBs. This formed a benchmark for comparison to the effects impacting the Power Chip On Bus (PCoB) modules described in later chapters.

The gate driver current loop in one of the paralleled power MOSFET gate drivers is shown as in Figure 1.6. The dashed line represents parasitic inductances inside the power module. The solid lines represent parasitic inductances of the PCB. The corresponding physical layout of the traces are shown in Figure 1.7.

Submission of the board design to ANSYS Q3D provided evaluation of the parasitic inductance. In this case, trace 1 and 2 in Figure 1.15 has $L_1 = 2.2nH$ and $L_2 = 5.0nH$ respectively (at DC). The mutual inductance is $0.3nH$ ($<<$ self inductance). The total gate drive loop parasitics contributed by PCB traces is about $7nH$. A 3D model representing the critical traces is generated as shown in Figure 1.8, and the current density distribution is plotted in Figure 1.9. These figures provide insight into the adequacy and source of inductances in the PCB design.
This information adds to the understanding for creation of ultra-low inductance power modules and test circuits for evaluating those modules.

![Model for simulation](image1)

Figure 1. 8 Model for simulation

![Current density distribution](image2)

Figure 1. 9 Current density distribution

### 1.3.3 Power Loop Inductance

A SPICE model of a double-pulse test circuit is given in Figure 1.6. The Wolfspeed C2M0025120D SiC MOSFET is the device under test (DUT). The Wolfspeed CPW51200Z050B SiC Schottky diode is used as a freewheeling diode. Both these devices are 1200V 50A rated. The SPICE models of these devices are provided by Wolfspeed. The temperature terminals of the MOSFET model is fixed at 25 degree C.
The parasitics of the DUT is modeled by the gate inductance, source inductance and drain inductance as L4, L2 and L3 respectively in Figure 1.10. In this study the gate inductance is fixed at 5 \( nH \) and the gate resistance is fixed at 10 Ohms. The gate pulse voltage has a rise time and fall time of 20 ns and 18 ns respectively. To study the influence of source inductance, the source inductance is swept from 2 \( nH \) to 10 \( nH \) with the drain inductance fixed at 10 \( nH \).
The source inductance acts as negative feedback for the gate loop. As indicated in simulation results in Figure 1.11, larger source inductance slows down the switching transient significantly which increases the switching loss.

Figure 1.11 Source inductance’s influence on switching transient by SPICE simulation
To study the influence of drain inductance, the drain inductance is swept from 8\,nH to 24\,nH with the source inductance fixed at 10\,nH.

The drain inductance is critical for the power loop, as shown in simulation result in Figure 1.12. The larger drain inductance enhances the ringing magnitude and lengthens the settling time, which increases the switching loss. Hence, this shows the criticality of reduced power loop inductance to device and subsequent application performance. Packaging is developed to minimize this inductance.

Figure 1.12 Drain inductance’s influence on switching transient by SPICE simulation
1.3.4 Power Module Parasitics Extraction

During this research an approach was developed to characterize power modules and extract key parameters for multi-physics modeling. An important parameter extraction was inductances. The process is documented as follows. To conveniently measure the power module internal dimensions and create a 3D model for finite element analysis (FEA) simulation, a non-destructive approach is proposed. The module under investigation was opened to expose the internal topology. A Hesse Mechatronics BJ939 Heavy Wire/Ribbon Bonder digital camera system, accurate to within 10μm, was used to measure die, interconnect, and substrate length and width dimensions as shown in Figure 1.13.

![Image](image.jpg)

Figure 1.13 Wolfspeed Six pack SiC module from BJ939 Bonder digital camera

Initial heights and thicknesses were measured through a 45° perspective holder, as shown in Figure. 1.14. Trigonometric relationships in conjunction with Snell’s Law were used for determining the internal layer thicknesses of the substrate and die. The silicone gel’s index of refraction was ~1.33 at room temperature [4, 5].
The nondestructive measurement procedure using the BJ939 digital camera system is enumerated as:

1) Remove the module housing lid and place the opened module onto the known-angle perspective holder.

2) Place the module and perspective holder onto the center of the BJ939 work holder.

3) Center the BJ939 bond head and camera system over the opened power module, lowering the bond head until the internal power stage of the power module is in focus.

4) Use the BJ939 camera system target reticle cross-hairs to measure the horizontal distance, parallel to the work holder, between the top and bottom edges of each material layer within the power module.

5) Assuming the index of refraction of silicone gel is ~1.33, calculate individual layer thicknesses using the trigonometric relationships and Snell’s Law.
Through this method, the layout of the DBC substrate, DBC copper thickness, and bond wire diameter were measured. The measured layer thickness and DBC dimensions are summarized in Figures 1.15, 1.16 and Table 1.3. To validate the measurement procedure, another Wolfspeed module was disassembled and directly measured with calipers to within ±25.4μm (1mil) accuracy. It should be noted that accurate measurement of the solder layers using a technique, such as SEM, was not used. However, solder layers were assumed to be 50μm for this study. As listed in Table 1.4, the tear down measurement validates the nondestructive measurement.

![Figure 1.15 Measured vertical dimensions](image)

![Figure 1.16 DBC pattern layout](image)

<table>
<thead>
<tr>
<th>Dimension</th>
<th>Size (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>a</td>
<td>1.2</td>
</tr>
<tr>
<td>b</td>
<td>10.3</td>
</tr>
<tr>
<td>c</td>
<td>21.6</td>
</tr>
<tr>
<td>d</td>
<td>19.24</td>
</tr>
<tr>
<td>e</td>
<td>23.24</td>
</tr>
<tr>
<td>f</td>
<td>2.5</td>
</tr>
<tr>
<td>g</td>
<td>2.5</td>
</tr>
<tr>
<td>h</td>
<td>4.0</td>
</tr>
<tr>
<td>i</td>
<td>31.24</td>
</tr>
<tr>
<td>j</td>
<td>23.6</td>
</tr>
</tbody>
</table>
Table 1. 4 DBC dimension measurement accuracy

<table>
<thead>
<tr>
<th>DBC AlN</th>
<th>Nondestructive</th>
<th>Destructive</th>
<th>% Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thickness</td>
<td>24.2 mils</td>
<td>25 mils</td>
<td>3.2 %</td>
</tr>
<tr>
<td>Length</td>
<td>1210 mils</td>
<td>1236 mils</td>
<td>2.1 %</td>
</tr>
<tr>
<td>Width</td>
<td>885 mils</td>
<td>902 mils</td>
<td>1.9 %</td>
</tr>
</tbody>
</table>

According to the measurement, 3D model of the module is generated as in Figure 1.17.

Figure 1. 17 Wolfspeed 3D module constructed

Figure 1. 18 Wolfspeed 3D module ANSYS Q3D simulation current density
The simulated module parasitics are summarized in Table 1.5. The manufacturer indicated a phase loop inductance of 30 nH at a few hundred kHz. The simulation matches with reasonable differences.

Table 1.5 Simulated module parasitics

<table>
<thead>
<tr>
<th>Phase</th>
<th>Freq. (Hz)</th>
<th>DC</th>
<th>10k</th>
<th>100k</th>
<th>1M</th>
<th>10M</th>
<th>100M</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>L(nH)</td>
<td>43.37</td>
<td>42.20</td>
<td>36.21</td>
<td>32.76</td>
<td>31.61</td>
<td>31.24</td>
</tr>
<tr>
<td>B</td>
<td>L(nH)</td>
<td>51.52</td>
<td>48.72</td>
<td>40.46</td>
<td>36.54</td>
<td>35.25</td>
<td>34.85</td>
</tr>
<tr>
<td>C</td>
<td>L(nH)</td>
<td>41.56</td>
<td>40.44</td>
<td>34.80</td>
<td>31.56</td>
<td>30.48</td>
<td>30.13</td>
</tr>
<tr>
<td>A</td>
<td>R(mΩ)</td>
<td>4.83</td>
<td>4.98</td>
<td>6.90</td>
<td>14.12</td>
<td>37.28</td>
<td>110.6</td>
</tr>
<tr>
<td>B</td>
<td>R(mΩ)</td>
<td>5.04</td>
<td>5.31</td>
<td>7.59</td>
<td>15.64</td>
<td>41.34</td>
<td>122.7</td>
</tr>
<tr>
<td>C</td>
<td>R(mΩ)</td>
<td>4.76</td>
<td>4.90</td>
<td>6.79</td>
<td>14.13</td>
<td>37.72</td>
<td>112.5</td>
</tr>
</tbody>
</table>

1.4 Review of Double-sided Power Package

To improve power density, and electrical and thermal performances, replacing the top-side bond wire connection by a flat planar interconnection can be considered a solution. The all-planar interconnected power module or double-sided power module has significant advantages over conventional modules. However, due to the sandwiched structure and non-standard fabrication processes, it also has some issues.

**Advantages of all-planar package:**
1) Extremely low parasitic inductance and resistance
2) Enhanced heat transfer
3) Higher power density

**Disadvantages of all-planar package:**
1) Thermal stress management
2) Top-side power die attachment
3) Top and bottom substrate alignment
4) Voltage isolation
5) Assembly complexity

The Power Chip on Bus (PCoB) research reported here addresses this specific topic. A review of similar approaches is needed to place into perspective the PCoB work.

Two types of double-sided power package/modules exist. The first type features a double-sided wirebond-less planar electrical interconnect and single-sided heat transfer. For this type of module, the double sided planar electrical interconnect helps to form localized power and gate
drive loops to reduce parasitics and power density. In the late 1990’s, GE proposed the POL (Power Overlay) package [6]. Semikron, Fuji, Mitsubishi also have double-sided power module technology in this category [7–19].

Figure 1. 19 GE POL cross section [6]

Figure 1. 20 Fuji SiC module cross section

Figure 1. 21 Fuji SiC module

Figure 1. 22 Semikron SKiN cross section

Figure 1. 23 Semikron SKiN
The second type of double-sided power module features double-sided wirebond-less planar electrical interconnect and double-sided heat transfer. For this type of module, both electrical and thermal performance are improved. Considering the thermal-mechanical stress, either a thin copper lead frame is used or low coefficient of thermal expansion (CTE) spacer is used. The lead frame significantly limits the current carrying capability, thus, is only suitable for low power applications. International Rectifier DirectFET uses the lead frame. Toyota-Denso and Oak Ridge National Lab’s double-sided modules are good for higher power electrical vehicle application.
University of Grenoble in France also had extensive research on double-sided power module.

1.5 Electric Vehicle Inverter/Converter Module

Hybrid Synergy Drive (HSD) is the brand name for Toyota hybrid car drive train technology [20]. It is used in many Toyota/Lexus hybrid vehicles including Toyota Prius, Toyota Camry Hybrid, Lexus CT200h, and Lexus ES hybrid. HSD is a very typical EV/HEV inverter/converter topology. Figure 1.36 shows the HSD topology.
Figure 1. 36 Toyota HSD converter- inverter

Figure 1. 37 Toyota Prius 2010 inverter assembly

Figure 1. 38 Toyota Prius 2010 power module
Chapter 2. Power Module Thermal Design and Multi-physics Simulation

Heat is an inevitable byproduct of semiconductor device operation due to conducted joule heating, as well as switching loss, and the induced increase of device temperature affects the device performance and reliability. Of particular concern is the non-linear increase in failure rate:

\[ F = A e^{-E_A / K T} \]  

Eq. 2.1

where \( A \) is a constant, \( E_A \) is activation energy (eV), \( K \) is Boltzmann constant; \( T \) is junction temperature) which is highly sensitive to junction temperature [21,22]. Detriments to the reliability include mechanical stresses induced at interconnects between metal, electrically insulating material (e.g ceramic), and semiconductor at an elevated temperature.

Conduction, blocking and switching performance of power semiconductor devices are all influenced by junction temperature. Thus, thermal dissipation is one of the most important design considerations for power module engineers. The multi-physics simulation is a very useful tool for studying thermal-mechanical behavior of power modules.

2.1 Power Module Thermal Resistance

A typical power module has a structure shown in Figure 2.1.

![Figure 2.1 Power module structure](image-url)
A 3D model is created to study the thermal resistance breakdown of this structure. Material and layer thickness in this module are summarized in Table 2.1. The power semiconductor chip has a size of 5mm by 5mm by 180 µm. The DBC copper has a 2mm margin on each side of the chip, and the baseplate has a 1mm margin on each side beyond the DBC substrate.

<table>
<thead>
<tr>
<th>Layer</th>
<th>Chip</th>
<th>Die attach</th>
<th>DBC top trace</th>
<th>DBC dielectric</th>
<th>DBC bottom trace</th>
<th>DBC attach</th>
<th>Base plate</th>
</tr>
</thead>
<tbody>
<tr>
<td>Material</td>
<td>SiC</td>
<td>Sn60Pb40</td>
<td>Cu</td>
<td>AlN</td>
<td>Cu</td>
<td>Sn60Pb40</td>
<td>Cu</td>
</tr>
<tr>
<td>Thermal conductivity w/(m·K)</td>
<td>450</td>
<td>50</td>
<td>400</td>
<td>180</td>
<td>400</td>
<td>50</td>
<td>400</td>
</tr>
<tr>
<td>Thickness (mm)</td>
<td>0.15</td>
<td>0.1</td>
<td>0.3 (12mils)</td>
<td>0.625 (25mils)</td>
<td>0.3 (12mils)</td>
<td>0.1</td>
<td>3</td>
</tr>
</tbody>
</table>

In the FEA simulation model, a 100w power dissipation is applied on the top-side of the chip. The bottom-side of the baseplate is fixed to reference temperature. The maximum temperatures of each interface are extracted and the thermal resistance of each layer is calculated in Table 2.2.

<table>
<thead>
<tr>
<th>Layer</th>
<th>Chip</th>
<th>Die attach</th>
<th>DBC top Cu</th>
<th>DBC AlN dielectric</th>
<th>DBC bottom Cu</th>
<th>DBC attach</th>
<th>Baseplate</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal resistance (C/w)</td>
<td>0.013</td>
<td>0.075</td>
<td>0.026</td>
<td>0.064</td>
<td>0.019</td>
<td>0.046</td>
<td>0.121</td>
<td>0.364</td>
</tr>
</tbody>
</table>
Figure 2. 2 Typical SiC power module thermal resistance breakdown percentage

The baseplate, die attach solder and DBC dielectric layer account for the dominant portion of the power module junction-to-case thermal resistance due to the facts that: 1) the baseplate is much thicker than any other layer in the structure; 2) the die attach solder has the lowest thermal conductivity and smallest cross-sectional area in the heat path; and 3) the DBC dielectric is relatively thick and relatively thermally insulating compared to copper layers.

2.2 Influence of Thermal Spreading on Power Module Thermal Resistance
2.2.1 Introduction to Fixed-angle Thermal Spreading Model

Quick thermal-impedance-based temperature evaluation of an IGBT module is of great interest to power electronic designers to provide quick evaluation of the junction to ambient temperature rise. Three methods are commonly used to estimate temperature distribution in a power module: 1) a one-dimensional thermal impedance approach based on a fixed-angle spreading angle model, 2) finite element analysis (FEA) and 3) analytical method. Each method is
presented as it applies to the power module design and fundamental errors in the results are discussed.

In an IGBT package, heat is conducted from a relatively small area on a semiconductor chip through a layered package structure underneath the chip and heat spreads laterally from chip-center to side walls. For simplicity, power module designers try to simplify a three-dimensional heat flow model to one-dimension and create an equivalent thermal resistance model based on the fundamental thermal resistance equation:

\[ R_{th} = \frac{L}{kA} \]  

Eq. 2.2

where \( k \) is thermal conductivity of material, \( L \) and \( A \) are length and cross-sectional area of the heat path. The fixed-angle heat spreading assumes the heat path has a similar shape as the pyramid structure in Figure 2.3. The pyramid structure can be completely defined by \( \phi \) (angle between each side wall of the pyramid and vertical axis) and thickness \( t \). Papers [23, 24] studied the accuracy of this approach.

Figure 2.3 Fixed-angle thermal spreading angle model
Based on this fixed-angle model, the thermal resistance of the pyramid structure can be determined by Equation 2.3:

$$R_{th} = \int_0^{t_s} \frac{1}{k(a+2z\tan\theta)^2} \, dz = \frac{1}{2k\tan\theta} \left( \frac{1}{a} - \frac{1}{a+2t_s\tan\theta} \right)$$  \hspace{1cm} \text{Eq. 2.3}

Assuming a 5mm by 5mm heat source is on top of a copper layer, the error (referring to FEA simulation) introduced by the fixed-angle model is calculated and plotted in Figure 2.4.

![Figure 2.4 Fixed-angle thermal spreading angle model error for single layer copper](image)

The 45 degree thermal spreading model cannot give an accurate estimation for thermal resistance for a very thin layer structure. Nguyen [25] proposed that, for multiple-layered IGBT package structures, the spreading angle can be determined by:

$$\alpha = \arctan(\frac{k_1}{k_2}) \quad (0 < \alpha < 90^\circ)$$  \hspace{1cm} \text{Eq. 2.4}

where $\alpha$ is the thermal spreading angle, $k_1$ is thermal conductivity for the present layer, and $k_2$ is the thermal conductivity for the layer underneath. However, from the 3D FEA simulation, for a multiple-layer power substrate with materials has various thermal conductivity, no fixed-degree thermal spreading model can capture the complexity for thermal spreading [26].
2.2.2 Power Substrate Thermal Spreading Design

To study the influence of thermal spreading on junction to case thermal resistance, a 3D model as described in Figure 2.5 is created. In order to capture the thermal spreading in thin layers, structured mesh is applied. In this study the SiC chip size is fixed at 5mm by 5mm by 0.15mm. The copper margin distance for the die attach pad is swept under various substrate dielectric material and DBC copper thickness conditions. The thermal resistance vs. copper margin distance for alumina and AlN substrates are plotted in Figure 2.7 and Figure 2.8 respectively. (The use of imperial units, i.e. mils, versus metric µm, is common in the older literature that this discussion was specifically addressing during its development, hence is maintained here. A mil or 1/1000 inch equals 25.4µm)

![Figure 2.5 3D CAD model for FEA simulation](image1)

![Figure 2.6 3D CAD model with mesh](image2)
At 8 mm copper pad margin distance, the junction to case thermal resistance reduction percentage is summarized in Table 2.3.
Table 2.3 Thermal resistance reduction percentage at full thermal spreading

<table>
<thead>
<tr>
<th></th>
<th>4mil Cu</th>
<th>8mil Cu</th>
<th>12mil Cu</th>
<th>16mil Cu</th>
</tr>
</thead>
<tbody>
<tr>
<td>25 mils AlN substrate</td>
<td>26.3%</td>
<td>30.1%</td>
<td>33.5%</td>
<td>36.5%</td>
</tr>
<tr>
<td>25 mils Alumina substrate</td>
<td>31.1%</td>
<td>40.4%</td>
<td>46.8%</td>
<td>51.6%</td>
</tr>
</tbody>
</table>

As indicated in Figure 2.7, defining the recommended margin distance as where 90% of thermal resistance reduction by full thermal spreading is achieved, the recommended copper margin distances are summarized in Table 2.4.

Table 2.4 Recommended minimal copper margin distance

<table>
<thead>
<tr>
<th></th>
<th>4mil Cu</th>
<th>8mil Cu</th>
<th>12mil Cu</th>
<th>16mil Cu</th>
</tr>
</thead>
<tbody>
<tr>
<td>25 mils AlN substrate</td>
<td>2.0mm</td>
<td>2.1mm</td>
<td>2.2mm</td>
<td>2.3mm</td>
</tr>
<tr>
<td>25 mils Alumina substrate</td>
<td>1.4mm</td>
<td>1.8mm</td>
<td>2.0mm</td>
<td>2.2mm</td>
</tr>
</tbody>
</table>

The AlN has a thermal conductivity of 180 W/(m·K) and the Alumina has a thermal conductivity of only 27 W/(m·K). The junction to case thermal resistance reduction percentage at full thermal spreading for AlN substrate is less than that with alumina substrate.

In the case of the DBC based power module, the selection of top layer copper is critical to minimize the total junction-to-case thermal resistance. Suppose there is a simplified two layer substrate structure with a side view as in Figure 2.9. A power semiconductor chip of 5mm by 5mm seats on top of the copper layer and dissipates 50W heat flux (200W/cm²). The bottom-side of the ceramics is fixed to room temperature at 20°C degrees. To determine the optimal thickness for the top copper layer in terms of least thermal resistance, a few sets of FEA simulations are conducted. The simulation results are extracted as the maximum temperature vs. upper copper thickness curves in Figure 2.10. The temperature is referred to room temperature.
The copper thickness, which corresponds to lowest thermal resistance is defined as the optimal thickness. For the same substrate size, the optimal top copper thickness is almost the same. Both green and red curves have a minimal point at around 3.1mm. Both the cadet blue curve and the dark blue curve have a minimum at around 5.1mm. Thus the alumina thickness has relatively small influence to the optimal thickness of top copper. However, the size of the substrate copper influences the optimal copper thickness significantly. In another word, it’s actually the area difference between heat source and substrate that determines the copper thickness needed for sufficient thermal spreading for reducing the total thermal resistance.

Based on the typical alumina thickness of 25 mils (0.625mm), the simulation results for maximum temperature vs substrate size and upper layer copper thickness is shown in the 3-D plot Figure 2.11. For the reference temperature 20°C, the maximum allowable temperature of 125 °C, and the maximum temperature rise of 105°C is allowed. The 105°C increase contour line in the 3-D plot is extracted to a 2-D plot shown in Figure 2.12. The region on the upper right side of each curve is the valid design space (temperature increase less than 105°C).
2.3 Power Module Thermal-mechanical Optimization

The failure mechanisms that limit the number of power cycles are caused by coefficient of thermal expansion (CTE) mismatch between the interfacing materials. The thermal stress is also influenced by Young’s modulus of package materials and pre-stress introduced in fabrication process. As the paper [27] states the common failure mechanism for an IGBT module includes: emitter bonding wire lifting failure, solder degradation, cracks in silicon die and substrate, and electro-migration in bonding wires. In this study, a multi-physics EFA based optimization approach is proposed based on bulk material mechanical failure mechanisms. Although some simplifications are made, this assumption has practical meaning. More detailed consideration including pre-stress and electro-migration can be added to the proposed model in the future. The approach proposed in this section gives me a general method for thermal-mechanical design in research.

2.3.1 Thermal Stress and Mechanical Fracture Criterion

In a typical IGBT-based motor drive, 4% of the controlled power is dissipated as heat within the device [27]. Thus thermal and thermal – mechanical management is critical for power
modules. The Hooke’s law states the relation between stress and strain: \( \sigma = E \times \varepsilon \) for elastic deformation where \( E \) is Young’s modulus. Before the stress reaches the yielding stress \( \sigma_y \) the deformation is purely elastic, as the stress is removed the deformation goes back to 0. Beyond the yielding stress point, the deformation is no longer elastic and the object cannot change back completely even when the stress is removed.

1) Copper fracture

The von Mises stress is an equivalent or effective stress at which yielding is predicted to occur in ductile materials. The von Mises stress is a scalar and it’s defined as:

\[
\sigma' = \frac{1}{\sqrt{2}} \sqrt{(\sigma_{11} - \sigma_{22})^2 + (\sigma_{22} - \sigma_{33})^2 + (\sigma_{33} - \sigma_{11})^2 + 6(\sigma_{12}^2 + \sigma_{23}^2 + \sigma_{31}^2)}
\]

Eq. 2.5

For the case of principal stress only, the von Mises stress is simplified to

\[
\sigma' = \frac{1}{\sqrt{2}} \sqrt{(\sigma_{11} - \sigma_{22})^2 + (\sigma_{22} - \sigma_{33})^2 + (\sigma_{33} - \sigma_{11})^2}
\]

Eq. 2.6

Figure 2. 13 Three-dimensional Stress

Figure 2. 14 Critical stress of alumina

To determine the criterion for fracture within copper, we can apply von Mises yield criterion directly. Von Mises criterion suggests that the yielding of ductile material begins when the von Mises stress reaches the yielding stress and the yielding stress for copper is 200MPa.

2) Ceramic fracture
The measured fracture strengths of most ceramic materials are substantially lower than predicted by theory from interatomic bonding forces. This can be explained by very small and omnipresent flaws in the material that serve as stress raiser-points where the magnitude of an applied tensile stress is amplified and no mechanism such as plastic deformation exists to slow down or divert such cracks. Brittle fracture takes place without any appreciable deformation and by rapid crack propagation. The direction of crack motion is very nearly perpendicular to the direction of the applied tensile stress and yields a relatively flat fracture surface [28]. Ceramic’s ability to resist fracture when a crack is present is defined as fracture toughness. The plane strain fracture toughness is

$$m_{IJ}=Y\sigma \sqrt{\pi a}$$

Eq. 2.7

where $Y$ is a dimensionless parameter dependent on the relative geometric relation between crack and the specimen. $\sigma$ is the applied stress and $a$ is half of internal crack size. In this equation, $K_{IC}$ is a material property, for 96% pure aluminum oxide (alumina), $K_{IC} = 3.9MPa\sqrt{m}$. Crack size is highly determined by the ceramics fabrication process, assuming half internal crack size $a$ is $50\mu m$. Parameter $Y$ can be calculated by equation:

$$Y\left(\frac{a}{w}\right) = \sqrt{\sec\left(\frac{\pi a}{w}\right)}$$

Eq. 2.8

where $w$ is the ceramics thickness. Thus $\sigma$ can be calculated as a comparison stress for maximum principal stress in the ceramic to determine when the ceramic layer fractures. The critical stress for alumina vs. alumina thickness relation is calculated and plotted in Figure 2.14.

3) Silicon fracture

Silicon lattice is very brittle. It has a mechanical property similar to ceramic. By nature being a brittle material, moderate stress levels could result in detrimental failure such as cracking and fracture in the die. In addition, wafer processing steps such as thinning and sawing could further induce defects in the silicon die [29]. Both die size and thickness have influence on the
silicon die failure stress (called silicon die critical stress in later sections). According to paper [29], the silicon die failure stress is about 400MPa for the thickness of 0.12 mm.

4) Solder fracture

Solder is used in the power module to connect power semiconductor chips and DBC substrate. Solder is a bypath for both electric current and heat. One of the commonly used solders in power modules is Sn60Pb40 solder. In tin-lead system, the solid phases are designated by $\alpha$ and $\beta$. A solid-solution of tin and lead is represented by $\alpha$. For $\beta$, tin is the solvent and lead is the solute. Compared to copper and ceramics, Sn60Pb40 solder has a very small Young’s modulus which is 10GPa. This means that Sn60Pb40 solder is relatively soft. Moreover, the melting point of Sn60Pb40 is 185°C which makes this material attractive as a low-temperature solder. The mechanical strength of solder is highly dependent on temperature. Book [30] shows the mechanical loading capability for solder vs. temperature. Solder’s mechanical strength decreases significantly after 120°C. For temperature within our concern, the mechanical strength of the solder changes less than 10% from room temperature. Thus, in this study we assume the solder critical stress for fracture determination is a constant. Based on the data in paper [31], the critical stress of solder is assumed to be 170 MPa.

2.3.2 Power Module Thermal-mechanical Optimization Formulation

Based on the failure mechanism mentioned previously, an optimization model can be formulated to achieve the optimal geometric dimensions with least chance of mechanical failure.

1) Design variables

Due to geometric symmetry, only one quarter of the geometry is studied. The one quarter geometry is shown in Figure 2.15. All dimension variables are summarized in Table 2.5. Chip size, chip thickness and solder thickness are fixed at values that are in the typical range. Substrate size,
The top copper thickness, bottom copper thickness and ceramic thickness are the 5 design variables in the optimization algorithm.

Table 2. 5 Geometry dimension variables

<table>
<thead>
<tr>
<th>Variable (mm)</th>
<th>Substrate size</th>
<th>Chip size</th>
<th>Chip thickness</th>
<th>Solder thickness</th>
<th>Bottom Cu thickness</th>
<th>Top Cu thickness</th>
<th>Ceramic thickness</th>
</tr>
</thead>
<tbody>
<tr>
<td>Value/Type</td>
<td>Design</td>
<td>5</td>
<td>0.12</td>
<td>0.1</td>
<td>Design</td>
<td>Design</td>
<td>Design</td>
</tr>
</tbody>
</table>

2) Constraints

The constraint and initial value of each of the design variables are listed in Table 2.6.

Table 2. 6 Design variable constraints

<table>
<thead>
<tr>
<th>Design Variable</th>
<th>Lower Bound (mm)</th>
<th>Upper Bound (mm)</th>
<th>Initial Value (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Substrate Size</td>
<td>6</td>
<td>20</td>
<td>12</td>
</tr>
<tr>
<td>Top Cu Thickness</td>
<td>0.1</td>
<td>1</td>
<td>0.4</td>
</tr>
<tr>
<td>Alumina Thickness</td>
<td>0.1</td>
<td>1.2</td>
<td>0.625</td>
</tr>
<tr>
<td>Bottom Cu Thickness</td>
<td>0.1</td>
<td>1</td>
<td>0.4</td>
</tr>
</tbody>
</table>

3) Objective function

Based on the previous section, the criteria for material fracture to occur are (where $\sigma'$ is the Von Mises stress):

For copper:

$$\sigma'_{Cu\ max} > \sigma_{Cu\ yield}, \text{ or } \frac{\sigma'_{Cu\ max}}{\sigma_{Cu\ yield}} > 1$$

Eq. 2.9
For ceramic:

\[
\sigma'_{\text{alumina\_max\_principal}} > \sigma_{\text{alumina\_critical}}, \text{ or } \frac{\sigma'_{\text{alumina\_max}}}{\sigma_{\text{alumina\_critical}}} > 1 \quad \text{Eq. 2.10}
\]

For semiconductor:

\[
\sigma'_{\text{silicon\_max}} > \sigma_{\text{silicon\_critical}}, \text{ or } \frac{\sigma'_{\text{silicon\_max}}}{\sigma_{\text{silicon\_critical}}} > 1 \quad \text{Eq. 2.11}
\]

For solder:

\[
\sigma'_{\text{Sn60Pb40\_max}} > \sigma_{\text{Sn60Pb40\_critical}}, \text{ or } \frac{\sigma'_{\text{Sn60Pb40\_max}}}{\sigma_{\text{Sn60Pb40\_critical}}} > 1 \quad \text{Eq. 2.12}
\]

In order to define an objective function that takes care of all different material fracture criteria, the objective function must include multiple terms.

Define the objective function as:

\[
Obj = \max\left(\sigma'_{\text{Cu\_max\_top}} \frac{\sigma'_{\text{alumina\_max\_principal}}}{\sigma_{\text{alumina\_critical}}}, \sigma'_{\text{silicon\_max}} \frac{\sigma'_{\text{Si\_max}}}{\sigma_{\text{Si\_critical}}}, \sigma'_{\text{Sn60Pb40\_max}} \frac{\sigma'_{\text{Sn60Pb40\_max}}}{\sigma_{\text{Sn60Pb40\_critical}}}\right) \quad \text{Eq. 2.13}
\]

Since the bottom copper layer is of less issue for fracture, no term for bottom copper layer is included in the above expression. In order to avoid fracture, the above objective function should be less than unity, and the smaller the objective function value, the better for preventing a mechanical fracture failure. The optimization is to minimize this objective function.

4) Optimization algorithm

Nelder Mead is a commonly used heuristic direct search method used for nonlinear optimization problems. It belongs to the simplex method family and sometimes is referred to as downhill simplex method. It is based on evaluating a function at the vertices of a simplex, then iteratively shrinking the simplex as better points are found until some desired bound is obtained [32]. The method does not require any derivative information which makes it possible for problems with non-smooth functions.

In many practical problems, like parameter estimation and process control, the function values are uncertain or subject to noise. Therefore, a highly accurate solution is not necessary, and
may be impossible to compute. The Nelder-Mead method frequently gives significant improvements in the first few iterations and quickly produces acceptable results. This is important in applications where each run of the simulation is very expensive or time-consuming. In many numerical tests, the Nelder-Mead method succeeds in obtaining a good reduction in the function value using a relatively small number of evaluations.

5) Multi-physics FEA simulation
   Based on the quarter symmetry geometry defined in Figure 2.15, the FEA simulation is set up in COMSOL multi-physics. The heat transfer and solid mechanics physics are applied at the same time. A 25w heat flux is applied on top of the quarter chip which represents 100w applied to the whole chip. The bottom of the lower copper is fixed at a room temperature of 20℃. All the other surfaces are thermally insulated. Convective cooling is not included in this model. The center point of the bottom copper is mechanically fixed which does not have x, y and z direction displacements. Due to the quarter symmetry, two vertical symmetry planes are also fixed mechanically.

6) Algorithm interface
   The execution of this multi-physics FEA optimization is shown in Figure 2.16 [33]. The purple boxes are inputs and outputs.
2.3.3 Optimization Results and Discussion

The convergence processes of each design variable and objective function are plotted in Figures 2.17 to 2.21.
The optimized top copper thickness is greater than the bottom copper thickness, because better heat spreading in the top copper layer is critical for reducing temperature. The ceramic thickness is very thin due to low thermal conductivity of alumina. This study does not consider electrical insulation. For a high voltage module, the minimal ceramic thickness to withstand a safe voltage needs to be added as another boundary condition.
2.4 Case Study: Multi-Physics Simulation Based HV SiC Module Design

At the time of this work, no commercially available SiC power devices above 1700V existed in the market. Although there are $\geq$6kV SiC device prototypes in industry [34,35], the price is expected to be very high, hence, the 3.3kV to 6.5kV IGBT modules still dominate the industry. However, by taking advantages of the super-cascode topology to create a SuperCascode Power Module (SCPM) as shown in Fig. 2.24 with specifications given in Table 2.8, It is feasible to develop very high performance 6.5kV and 10kV SiC power modules by using 1.2kV and 1.7kV rated SiC JFET dies. Papers [36–42] stated the principle of power JFET cascode operation. The target of the work described below (and performed at the PREES Laboratory in the FREEDM Systems Center under contract from the PowerAmerica Institute) is to develop such powerful modules compatible with the industry standard 57 Pak footprint module with much higher power density and faster switching speed than ever reported, and be a replacement of HV IGBT modules.
The work here establishes a very high power density due to the use of highly efficient JFETs, and distributed heating. The PCoB research can be compared in density to this module, which will compare a water cooled SCPM to an air cooled PCoB.

![Image: 24 Power module schematic]

Table 2. 8 Module specifications

<table>
<thead>
<tr>
<th>Version</th>
<th>Voltage</th>
<th>Current</th>
<th>Package</th>
<th>Device configuration</th>
</tr>
</thead>
<tbody>
<tr>
<td>Version 1</td>
<td>6.5kV</td>
<td>100A</td>
<td>57 Pak</td>
<td>6 of 1.2 kV JFETs series, 2 parallel</td>
</tr>
<tr>
<td>Version 2</td>
<td>10kV</td>
<td>200A</td>
<td>57 Pak</td>
<td>6 of 1.7 kV JFETs series, 2 parallel</td>
</tr>
</tbody>
</table>

2.4.1 Physical Layout and Design

The power semiconductors used in the modules are shown in Figs. 2.25-2.28. The original module layout accommodates the larger UJ3N1701Z (1700V/100A) die. However, early fabrication and testing was with the UJN1202Z (1200V/50A) die.
Figure 2. 25 USCi 1200V 12 mOhms SiC JFET UJN1202Z

Figure 2. 26 USCi 1700V 6 mOhms SiC JFET UJ3N1701Z

Figure 2. 27 3.6 mOhms MOSFET USM141

Figure 2. 28 0.9 mOhms MOSFET AW1046

Figure 2. 29 Power module physical implementation
The physical layout of the power module is illustrated in Figures 2.29 to 2.30. Design features include: 1) simplicity: no electrical layer on top of DBC except for internal busbar; 2) low-cost: minimize the area needed for DBC, 1 single-sided PCB are used for balancing network; 3) Good thermal performance for power devices and gate resistors; 4) high yield: 4 small DBC are used (the DBC on lower voltage side can have thinner AlN layer); 5) reduced inductance: internal busbar included, two power loop in parallel, low profile module; 6) PCB as fixture for DBC soldering; 7) compact 57 Pak compatible; 8) low JFETs gate to ground capacitance; and 9) short bond wires

2.4.2 Thermal Analysis Results

A 3D model is created for FEA thermal simulation. The model features: 3mm baseplate, 0.1mm solder (Tin-lead, with thermal conductivity of 50 w/mK), 10 mils DBC copper, 1mm margin distance from DBC substrate to baseplate. The thermal resistance is extracted and plotted as a function of distance between DBC copper pad edge and the power chip side.
Based on the above study, the DBC layout is designed to be compatible with both UJN1202Z and UJ3N1701Z dies. A 3mm copper margin distance is guaranteed for the smaller chip and 1.5mm copper margin distance is guaranteed for the larger chips for allowing sufficient thermal spreading in both cases.

Figure 2. 32 DBC layout (half module) a) bare DBC, b) UJN1202Z on DBC, c) UJ3N1701Z on DBC
To evaluate the junction-to-case thermal resistance based on the above design, only one DBC substrates is simulated as shown in the Figure 2.33. COMSOL Multi-physics is used for the simulation. In the study, 20w heat dissipation is applied to the low voltage (LV) MOSFET (AW1046), 50w was applied to each high voltage SiC JFET (UJN 1202Z).

Table 2. 9 Thermal simulation model definition

<table>
<thead>
<tr>
<th>Material</th>
<th>Thickness (mm)</th>
<th>Thermal conductivity (w/mK)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiC Die</td>
<td>0.15</td>
<td>450</td>
</tr>
<tr>
<td>Die attach solder</td>
<td>0.10</td>
<td>50</td>
</tr>
<tr>
<td>DBC top copper</td>
<td>0.25</td>
<td>400</td>
</tr>
<tr>
<td>AlN</td>
<td>1.00 or 0.63</td>
<td>180</td>
</tr>
<tr>
<td>DBC bottom copper</td>
<td>0.25</td>
<td>400</td>
</tr>
<tr>
<td>DBC attach solder</td>
<td>0.10</td>
<td>50</td>
</tr>
<tr>
<td>AlSiC base plate</td>
<td>3.00</td>
<td>180</td>
</tr>
</tbody>
</table>

For 40 mil AlN substrate, the simulated junction to case thermal resistance of JFET (UJN 1202Z) is:

\[
R_{th_{jc,JFET}} = \frac{28.55 \degree C}{50w} = 0.57 \degree C/w
\]

Eq.2.14

And the junction to case thermal resistance of LV MOSFET (AW1046) is:

\[
R_{th_{jc,MOSFET}} = \frac{15.26 \degree C}{20w} = 0.76 \degree C/w
\]

Eq.2.15

For 25 mil AlN substrate, the JFET (UJN 1202Z) junction to case thermal resistance is 0.45°C/w and the LV MOSFET (AW1046) junction to case thermal resistance is 0.61°C/w
2.4.3 Pin Fin Base-plate Thermal Performance Evaluation

Two versions of the base plate cooling solutions are designed. The first design has a regular baseplate and cold plate system as in Figures 2.36, 2.37 and 2.40. The pin fins on the base plate are optimized by manufacturing for a low temperature gradient across the power module. I proposed a second design with special cold plate profiles as in Figures 2.38, 2.39 and 2.41. The special design has a wider inlet and narrower outlet to provide more cooling for outlet end heat source to further minimize the temperature gradient across the module. Moreover the second design has a pin fin only under power devices and two cooling channels in parallel. The vertical profile of the water channel in the second design needs to be optimized to have very little temperature gradient for rated flow rate range. However, by doing this the average temperature may increase slightly. In order to study the thermal performance of both design, FEA models are created with fluid cooling physics.
Table 2. 10 Thermal simulation model definition

<table>
<thead>
<tr>
<th>Properties</th>
<th>Dimensions/feature</th>
</tr>
</thead>
<tbody>
<tr>
<td>57 Pak baseplate</td>
<td>137(L)/70(W)/5(H) (mm)</td>
</tr>
<tr>
<td>baseplate Material</td>
<td>AlSiC</td>
</tr>
<tr>
<td>Pin fin height</td>
<td>6mm</td>
</tr>
<tr>
<td>Pin fin diameter</td>
<td>2mm/1.5mm bottom/top</td>
</tr>
<tr>
<td>DBC in simulation:</td>
<td>Cu/AlN/Cu</td>
</tr>
<tr>
<td></td>
<td>10/25/10 mils</td>
</tr>
<tr>
<td>Power chip</td>
<td>UJN 1202Z, AW1046</td>
</tr>
</tbody>
</table>

Figure 2. 35 Base plate pin fin layout

Figure 2. 36 Regular liquid cooled cold plate

Figure 2. 37 Pin fin of regular liquid cooled baseplate

Figure 2. 38 Special liquid-cooled cold plate

Figure 2. 39 Pin fin of special liquid-cooled baseplate
Simulation boundary conditions include 1) total flow rate: 0.0004 m$^3$/s (400 ml/s); 2) inlet temperature fixed at 20°C; and 3) power dissipation is 50w for each JFET, 20w on each MOSFET. The simulated temperature distributions are shown in Figures 2.42 to 2.45.
The simulated maximum temperatures of each die are listed in Table 2.11. The special design has a more uniform temperature across the baseplate, however the temperature of each die is slightly higher.

**2.4.4 Power Module Electrical Parasitics Evaluation**

For power module designs, it is important to study the power substrate interconnect resistance and its ratio to the total resistance. For the UJN 1202Z JFET chip and USM141 MOSFET chip based 6.5kV power module, each JFET has 12 mOhms on state resistance. Based on the actual bonding pad size on UJN 1202Z die, the maximum number of bond wire and the corresponding current carrying capability are summarized in Table 2.12. A 3D model of one branch of the super-cascode structure (half of the module) is simulated for interconnect resistance. The simulated resistance and its ratio to semiconductor on-state resistance are listed in Table 2.13.

**Table 2. 11 Max chip temperature (chip 1 is closest to inlet)**

<table>
<thead>
<tr>
<th></th>
<th>Chip1</th>
<th>Chip2</th>
<th>Chip3</th>
<th>Chip4</th>
<th>Chip5</th>
<th>Chip6</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max temperature (C) for regular cold plate</td>
<td>46.15</td>
<td>46.62</td>
<td>46.76</td>
<td>46.99</td>
<td>46.91</td>
<td>47.13</td>
</tr>
<tr>
<td>Max temperature (C) for special cold plate</td>
<td>46.96</td>
<td>47.84</td>
<td>47.90</td>
<td>47.94</td>
<td>47.79</td>
<td>47.78</td>
</tr>
</tbody>
</table>

**Table 2. 12 Bondwire options for UJN1201Z chip**

<table>
<thead>
<tr>
<th>Al wire diameter</th>
<th>Single wire current carrying capability (A) [43]</th>
<th>Maximum number of wires for UJN 1202Z bond pad</th>
<th>Total current carrying capability (A)</th>
</tr>
</thead>
<tbody>
<tr>
<td>8 mils</td>
<td>11</td>
<td>6</td>
<td>66</td>
</tr>
<tr>
<td>12 mils</td>
<td>20</td>
<td>4</td>
<td>80</td>
</tr>
<tr>
<td>15 mils</td>
<td>28</td>
<td>3</td>
<td>84</td>
</tr>
<tr>
<td>22 mils</td>
<td>50</td>
<td>2</td>
<td>100</td>
</tr>
</tbody>
</table>
Table 2. Substrate resistance for UJN1201Z based 6.5kV module (only half module)

<table>
<thead>
<tr>
<th>DBC copper thickness (mils)/ Al bondwire diameter (mils)</th>
<th>DBC trace total resistance (mOhms)</th>
<th>Bondwire total resistance (mOhms)</th>
<th>Total interconnect resistance (mOhms)</th>
<th>Interconnect resistance vs power device resistance percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>8/8 (6 wires)</td>
<td>2.6</td>
<td>8.5</td>
<td>11.1</td>
<td>14.8%</td>
</tr>
<tr>
<td>8/12 (4 wires)</td>
<td>2.6</td>
<td>5.7</td>
<td>8.3</td>
<td>11.1%</td>
</tr>
<tr>
<td>8/15 (3 wires)</td>
<td>2.6</td>
<td>4.8</td>
<td>7.4</td>
<td>9.9%</td>
</tr>
<tr>
<td>8/22 (2 wires)</td>
<td>2.6</td>
<td>3.3</td>
<td>5.9</td>
<td>7.9%</td>
</tr>
<tr>
<td>12/8 (6 wires)</td>
<td>1.7</td>
<td>8.5</td>
<td>10.2</td>
<td>13.6%</td>
</tr>
<tr>
<td>12/12 (4 wires)</td>
<td>1.7</td>
<td>5.7</td>
<td>7.4</td>
<td>9.9%</td>
</tr>
<tr>
<td>12/15 (3 wires)</td>
<td>1.7</td>
<td>4.8</td>
<td>6.5</td>
<td>8.7%</td>
</tr>
<tr>
<td>12/22 (2 wires)</td>
<td>1.7</td>
<td>3.3</td>
<td>5.0</td>
<td>6.7%</td>
</tr>
</tbody>
</table>

Considering bond wire redundancy, it is preferable to have as many bond wires as possible. Considering the current carrying capability it’s preferable to have thicker wires. Based on the above tables, 12mil DBC copper with 4 of 12mils Al bondwire in parallel is considered as a preferable design. For this design, the 6.5kV 100A rated module will have a substrate resistance of 3.7 mohms and total R_on of about 42 mohms.

![Figure 2.46 Simplified 3D CAD model for inductance simulation](image)

A simplified model as in Figure 2.46 is created to represent the DBC power traces and internal busbar structure for power loop inductance extraction. The ANSYS Q3D simulation indicates 23nH power loop inductance at 100 kHz. The commercially available 6.5kV 57Pak
IGBT power module typically has a power loop inductance of 50 \( nH \). The current density distribution is plotted in Figure 2.47.

Figure 2.47 Current density plot for internal bus and bondwire

Indents are proposed in the baseplate design to increase the distance between copper traces on PCB and ground. By this method, the effective gate to source parasitic capacitance can be reduced significantly which reduces switching loss.

Figure 2.48 Special baseplate design for minimizing parasitic capacitance

**2.5 Conclusion**

In this chapter, the power module thermal resistance and the widely used thermal spreading angle model are discussed. The 45 degrees fixed-angle thermal spreading model is not an accurate tool for power module thermal design.
A methodology is developed to optimally design a power semiconductor substrate in a multi-physics environment. The heat transfer and structural mechanics physics are coupled in the simulation model to determine the optimal substrate design. The chosen optimization algorithms converged to a set of optimized design parameters. This methodology can be extended to design power modules with any other customized objective functions, design parameters and boundary conditions. With the promising 3-D printing technology, this optimization approach can possibly lead to a non-standard power module structure generation. Such irregular or curved power module structures can be optimized for maximizing thermal, mechanical and electrical performances and minimizing fabrication and material cost.

Finally, a multi-physics simulation based high voltage SiC power module design case has been presented.
Chapter 3. Development of Power Chip on Bus Power Module

3.1 Design Motivation

With the commercialization of wide-bandgap (WBG) power semiconductor devices, the traditional power package has reached its limit to maximize electrical and thermal performance of WBG based power electronic systems. Electrical and thermal limitations due to ceramics, thermal interface material (TIM), flexible welded interconnects (e.g. wire bonds) and use of single-sided cooling is well documented [8, 44]. The widely used direct bonded copper (DBC) substrate and thick metal baseplate account for a significant portion of junction to case thermal resistance. The bond wire can introduce significant amounts of inductance which is harmful during power switching transients. It was established in Chapter 1 the need for ultra-low inductance in the power modules. This meant elimination or minimization of all inductances in the power loop. To increase electrical and thermal performance, planar interconnects and double-sided cooling have become key areas for development. The ultimate approach to minimum inductance is to bring the major electrical current carrying conductors directly into contact with the power semiconductor die, so that they form both the electrical interconnection and the thermal path. The development Power Chip on Bus (PCoB) module demonstrates the absolute minimum loop possible in a multichip power module by direct-connecting electrical and thermal paths to the power semiconductors, an moving the electrical isolation layer, which is typically accommodated by the ceramic in DBC modules, to the Second Level of packaging using dielectric fluid (e.g. air) as electrical insulator.

The PCoB approach is a benchmark to other planar approaches. As discussed earlier, in late 1990’s, GE developed the Power Overlay (POL) package [6]. In 2008, Denso manufactured the double-sided power module for the Lexus LS600h hybrid car power conversion unit [9]. In the
past few years, both industry and academia have shown a growing interest in double-sided power module development [7-19]. Comparisons of PCoB to these is appropriate.

The ideal of PCoB module originated from an H-bridge inverter test many years ago.

The magenta curve is the busbar voltage measured from the busbar tabs and the yellow curve is the current passes one busbar tab, and the green curve is the load current. Due to the interconnect parasitic inductances, the power semiconductor device terminal sees significant voltage spike as in Figure 3.2.

I proposed a new power module combine the DC busbar, power semiconductor and cooling features all together to reduce parasitic and realize double-sided cooling. The DC-link capacitors are mounted around the power devices to minimize local switching loop. The module concept and thermal and electrical simulation are shown in Figures 3.3 to 3.6.
The challenges of development of busbar sandwiched module have been summarized in Figure 3.7.
3.2  PCoB Structure

Elevated temperature caused by power semiconductor heat dissipation introduces mechanical stress in power device and packaging due to coefficients of thermal expansion (CTE) difference between materials. The accumulated stress in each layer reduces reliability and cause power module mechanical failure [45]. The thermal stress issue is more challenging for double-sided power modules than the standard single-sided DBC substrate power modules, because dies are sandwiched by interconnect metal traces on both sides. This is especially an issue for high current modules with double-sided thick copper interconnects and large die area. Additionally, package fabrication and assembly are more complicated with the need for non-standard top-side solderable die, a sophisticated interconnect alignment process, and top-to-bottom voltage isolation.

In order to solve the issues with busbar sandwiched module and maximize the feasibility of developing such type of module in our lab with minimal power devices consumption, the following Power Chip on Bus Module has been developed.
The double-sided air-cooled Power Chip on Bus (PCoB) module developed in this research features liquid-cooled equivalent thermal performance, ultra-low electrical parasitics and reduced stress. The basic topology of the Power Chip on Bus module is shown in Figure 3.8. Thick finned copper acts as both heatsink and busbar. Power dies are electrically attached to two busbar-like power substrates directly. Molybdenum spacers are used as CTE buffer between the die and bottom substrate for reducing thermal-mechanical stress caused by CTE mismatch. The thickness of the molybdenum spacer is optimized through thermal-mechanical finite element analysis (FEA) simulation. Bottom-side die attachment for MOSFET drain and diode cathode is through soldering. Upper-side die attachment is through silver loaded silicone for further thermal-mechanical stress reduction. The gate terminal is connected through polyimide flexible circuit. Electrical isolation between the electrically hot heat sinks to the environment is achieved through an air channel.
3.3 Phase Leg Version PCoB Module

For the targeted EV/HEV motor drive application, PCoB approach is extended to three phase VSI topology. As shown in Figure 3.9, the upper bus is V– and lower bus is V+. Power dies are attached between one center terminal and an upper or lower busbar with the same material selection as in single switch version of PCoB module. The three phase version also uses two Wolfspeed 1200V, 50A SiC MOSFETs and one Wolfspeed 1200V 50A anti-parallel SiC Schottky diode to form six 1200V 100A rated switching units.

![Figure 3.9 Three-phase PCoB module](image1)

![Figure 3.10 Three-phase PCoB current distribution](image2)

ANSYS Q3D simulation indicates that the power loop parasitic inductance across each phase leg (with small difference between center phase leg and outside phase leg) is about 10\( nH \) which is only one third of the Wolfspeed 1200V 50A six pack module. The current density is shown in Figure 3.10. Thermal FEA simulation indicates a junction to ambient thermal resistance of 0.52 to 0.75 C/W (depending on die location) at air flow rate of 30CFM. Wolfspeed’s 6-pack module has an Rjc of 0.4 °C/W, and with added liquid cooling, the total \( R_{ja} \) is 0.6 to 1.0 °C/W. Hence, air cooling is a viable alternative to liquid cooled traditional approaches for EV/HEV motor drive application.
Considering the widely used boost converter stage in EV/HEV motor drive system, PCoB approach is also applied to three phase VSI plus three phase interleaved boost topology. One such phase leg is shown below. Three of the phase legs will form a 30kw rated EV inverter converter system. Each switching unit also includes the same SiC MOSFETs and diodes for 1200V, 100A plus switching capability. The thermal simulation indicates a junction to ambient thermal resistance of about 1.2C/W.

![PCoB VSI + Boost phase leg](image1)

![PCoB VSI+Boost thermal simulation](image2)

**3.4 Design of Single Switch PCoB Module**

The single switch version of PCoB module includes an active switch and an anti-parallel diode. The module is designed for 1200V and 100A. Two Wolfspeed 1200V, 50A SiC MOSFETs (CPM2-1200-0025B) and one Wolfspeed 1200V 50A anti-parallel SiC Schottky diode (CPW5-1200-Z050B) bare dies are chosen for each module.
The designed single switch module with its integrated heatsinks has a dimension of 41 mm by 41 mm by 43 mm and weight of 65 grams. The gate pads of MOSFETs are connected through an integrated 2-layer flexible circuit with 1 oz. copper on each layer. This flexible circuit also compensates the thickness difference between the chosen diode and MOSFET bare dies. The flexible circuit layout includes a Kelvin connection for the source of MOSFETs. The gate and source traces are placed with maximized overlap area to reduce gate loop inductance.
3.5 Power Chip on Bus (PCoB) Module Thermal Performance Evaluation

Heat dissipation affects the device performance and reliability significantly [46]. A detailed 3D CAD model has been created for air-cooled thermal FEA simulation. Heat transfer and laminar flow physics are coupled in this case. Heat transfer in both solid and fluid is included. The FEA model has a mesh of 539158 elements with an average element quality above 0.7 for achieving a reasonable simulation accuracy. In the model, the ambient temperature is fixed at 20°C, 100w power dissipation is assigned to one SiC power die and air flow rate is swept. In order to study the impact of different die sizes, both $5 \times 5 \text{ cm}^2$ and $10 \times 10 \text{ cm}^2$ dies are studied. The junction to ambient thermal resistance is calculated by maximum die temperature minus ambient temperature then divided by power dissipation. For this PCoB design, since the junction to case thermal resistance is only a fraction of junction to ambient thermal resistance, the die size has very small influence to the overall junction to ambient thermal resistance. For the case of 1cm square die under 30 CFM air flow rate, the power dissipation capability is summarized in Figure 3.16. The single switch PCoB module is able to dissipate 122w with a maximal allowed junction temperature of 150°C and ambient temperature of 100°C.
The 5mm by 5mm diode die (CPW5-1200-Z050B) is powered in PCoB module to test thermal dissipation performance. Simulation indicates that under 100w dissipation the maximum junction temperature is within a 2 °C difference from the maximum substrate temperature, thus, a measured maximum substrate temperature is used to estimate the junction to ambient thermal resistance. The thermal test indicates 0.5°C/W junction to ambient thermal resistance at air flow rate of about 15 CFM. The thermal resistance without any active cooling is less than 5°C/W. Figure 3.17 shows the infrared temperature image for 15w dissipation without any active cooling.
For similar die size, the traditional power module using 25 mil AlN substrate with 12 mils copper gives about 0.4°C/W junction to case thermal resistance. Putting the module on a liquid-cooled cold plate through thermal grease interface the total junction to liquid thermal resistance is about 0.6~1.0 °C/w. The double-sided air cooled PCoB module features comparable thermal performance by air cooling.

3.6 Power Chip on Bus (PCoB) Module Thermal-Mechanical Stress

Due to the CTE mismatch, thermal-mechanical stress management is critical for any high current double-sided power module. To reduce the thermal-mechanical stress, two approaches are taken. Molybdenum spacers with low CTE is used as a mechanical buffer soldered between power die and substrate. FEA simulation indicates the influence of thickness of the molybdenum spacer to die maximum stress. Based on simulation result, a customized gold plated molybdenum spacer with a thickness of 0.75mm is fabricated for this project. Upper die attachment is achieved by silver loaded silicone for further thermal-mechanical stress reduction. FEA simulation indicates
the silver loaded silicone reduces the maximum Von Mises stress of the chip from 11.5 MPa to 6.63 MPa, a 40 percent decrease compared to the double-sided tin-lead soldering approach.

Figure 3. 18 Molybdenum thickness influence on die stress

Table 3. 2 Silver Loaded Silicone Properties

<table>
<thead>
<tr>
<th>Property</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal conductivity (w/mK)</td>
<td>12</td>
</tr>
<tr>
<td>Modulus (MPa)</td>
<td>1.8</td>
</tr>
<tr>
<td>Volume resistance (ohm-cm)</td>
<td>$1 \times 10^{-4}$</td>
</tr>
<tr>
<td>Maximum Operation temperature (°C)</td>
<td>260</td>
</tr>
</tbody>
</table>

3.7 Power Chip on Bus (PCoB) Module Electrical Parasitics Study

Electrical parasitics are extracted through ANSYS Q3D extractor. In order to compare with regular power modules, a non-destructive method is used to accurately measure the internal dimensions of regular power modules and a 3D model of a regular SiC six-pack module (Wolfspeed CCS050M12CM2) is generated for parasitics comparison [44]. Both power loop and gate loop parasitic inductances at DC are simulated for PCoB module and a regular SiC six-pack module. As summarized in the following table, PCoB module features lower parasitic inductance.
for both power loop and gate loop. The reduction of gate loop inductance will reduce the gate driver signal ringing and decrease the required external gate resistor value. The switching will be faster and the switching loss will be smaller. Additionally, the reduced power loop inductance will lead to less di/dt induced voltage spike across the switch.

Table 3. 3 Simulated Parasitic Inductance

<table>
<thead>
<tr>
<th></th>
<th>Power loop inductance (nH)</th>
<th>Gate loop inductance (nH)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CCS050M12CM2</td>
<td>35</td>
<td>25</td>
</tr>
<tr>
<td>PCoB module</td>
<td>8</td>
<td>4</td>
</tr>
</tbody>
</table>

3.8 Process Development for Double-Sided Solderable Power Die

Regular power die has an aluminum top-side metallization for wire bonding. In order to have a compatible top-side metal for double-sided all planar interconnect, a fabrication process is developed for customizing power die top metal in our on-campus clean room. Most semiconductor process equipment is designed for processing the whole wafer. In order to have the flexibility to utilize a small number of commercial dies, effort has been made to develop a process on die level.
In this work, E-beam deposition of 300 nm titanium, 300 nm nickel and 1000 nm silver is achieved with good solderability. The first titanium layer is for adhesion. The nickel layer is a barrier preventing diffusion. The solderable top-side metal stack is critical for die mechanical stress [47].

3.8.1 Metallization Process for SiC MOSFET Die

Wolfspeed (CREE) CPM2-1200-0025B 1200V, 50A silicon carbide power MOSFET is chosen for this project. The die size is 6.44 mm by 4.04 mm. The original top-side metal is Al and the back side is Ni/Ag. Due to the relatively small feature size near the gate area, the photo-resist with mask aligner approach is taken. In order to reduce the possibility of the gate to source short during the PCoB assembly process, the designed photo mask leaves a greater distance from gate to source.

![SiC MOSFET die top-side metallization process flow](image)

**Figure 3. 21 SiC MOSFET die top-side metallization process flow**

1) Die cleaning

Acetone is used to clean the surface of die. After the chemical cleaning process, the dies are dried with a nitrogen gun for reducing possible residual.

2) Photoresist application

Negative photoresist JSR NFR 016 D2 is chosen for the process. The photoresist is spin coated on to the dies. To have a more uniform distribution of photoresist on die, the surface profile
of the original die is measured by a profilometer. The source pad is about 4 micron meters lower than the die area has no contact pad. The gate pad is about 500 nano meters higher than the source pad. In the process development, photoresist thickness at different location is measured to make sure spinning rpm profile guarantees reasonable photoresist thickness across the whole die. After the photo resist spinning, a baking process is followed.

![Figure 3. 22 SiC MOSFET die surface profile measurement (not to scale)]](image)

3) Mask alignment and UV exposure

Karl Suss MA6 Aligner is used for mask alignment and ultraviolet light exposure. The UV exposure time is tuned according to photoresist spinning speed.
4) Photoresist development

MF(TM)-319 Developer is used to develop the photoresist. The spinning rpm profile, photoresist exposure time and develop time combination is critical for this process.

As in Figure 3.26, the light yellow part is photoresist, the light silver and gray areas are the original metal pads on MOSFETs. A plasma etch process is applied after photoresist development.
for stripping, etching and cleaning organic contamination. A further chemical etch is followed for removing the aluminum oxide on top of the die. The chemical solution “Aluminum Etch Type A (Phosphoric Acid 40-80%, Acetic Acid 3-20%, Nitric Acid 1-5%)” is used for this purpose. The etching time is carefully tested and chosen to eliminate oxide without etching away the aluminum pad underneath [48]. Each die is etched for 1 min 30sec.

5) E-beam deposition

E-beam deposition approach is used to deposit Ti/Ni/Ag metal on top of the die. E-beam deposition is a type of physical vapor deposition (PVD) method. PVD techniques are generally more versatile then chemical vapor deposition (CVD) methods, allowing for the deposition of many materials [49]. In this work, deposition of titanium, nickel and silver for 300 nm, 300 nm, 1000 nm respectively is achieved with good solderability. Three crucibles inside the E-beam deposition chamber allow for depositing three metals sequentially without opening the vacuum door for changing metal sources.

6) Lift-off

NMP liftoff solution (N-Methyl-2-pyrrolidnone) is used for the lift-off process. The metal deposition on the unwanted regions on top of the die will be etched away during the process. As
in Figures 3.28 and 3.29 below, the newly deposited metal can be seen clearly in contrast with the original metal.

Figure 3.28 Die top-side after lift-off
Figure 3.29 Die top-side after lift-off

7) Process key parameters summary

Table 3.4 Key process parameters summary

<table>
<thead>
<tr>
<th>Die mount</th>
<th>Max photoresist spin speed (rpm)</th>
<th>UV exposure time (s)</th>
<th>Develop time (min)</th>
<th>Lift-off time (hrs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bare die</td>
<td>4000</td>
<td>3.5</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Die soldered on spacer</td>
<td>2000</td>
<td>5.5</td>
<td>6</td>
<td>2~4</td>
</tr>
</tbody>
</table>

3.8.2 Metallization Process for SiC Schottky Diode Die

Wolfspeed (CREE) CPW5-1200-Z050B 1200V, 50A silicon carbide Schottky diode chip is chosen. The die size is 4.9mm by 4.9mm. The original top-side metal is Al and the back side is Ni/Ag. Due to the simple pattern on the top of the die and the relatively large feature size, a set of brass die holder and mask has been applied for this metallization process. The die holder has nine pockets with size and depth matching the geometry of the die. The brass sheet mask is machined to have nine corresponding masks with a deposition area slightly smaller than the original top
metal pad of the die for alignment tolerance and guard ring protection. After die cleaning, the whole setup is placed into E-Beam deposition chamber for sequential Ti/Ni/Ag depositions.

Figure 3. 30 SiC Schottky diode top-side metallization process flow

Figure 3. 31 Diode holder with dies (after deposition)
Figure 3. 32 Diode holder with mask

3.8.3 Examination of Top-side Metal Deposition

Figure 3. 33 Soldering trial

a) Original die  b) Deposited MOSFET die  c) Deposited diode die
Solderability trial has been completed on different samples. When soldering the deposited SiC die with an excess amount of eutectic Sn63Pb37 solder paste, the solder wets very well to the deposited areas. Self-alignment prevents the gate to source short.

To test the current conduction through the new metal deposition, a DBC substrate based test bed has been fabricated as in Figure 3.34. The original diode die top-side is connected though bondwire, deposited dies are connected by soldering the copper strip to the top-side. The test module was measured by Tektronix 371B high power curve tracer with Kelvin connection. For forward conduction up to 100A, the deposited die behaves almost identical to the original die. The change of top-side metallization does not change the resistance much.

3.9 Fabrication and Assembly of PCoB Modules
3.9.1 Key Assembly Steps

The assembly flow is summarized in the following chart.
1) Machining and plating

Ideally, the substrates and heatsinks can be made as one piece for reducing the additional interface. Due to the complexity for machining, heatsinks and substrates are made separately and soldered together for fast prototyping. The wire EDM approach is used for heatsink fabrication. Copper substrates have been fabricated with CNC machining. After the machining, the heatsinks and substrates are electrically plated with nickel for surface protection.

![Figure 3. 37 Heat sinks by wire EDM](image1)

![Figure 3. 38 Heatsinks and substrates after Ni plating](image2)

2) Soldering

A 5-zone reflow oven is used to solder the heatsinks to substrate, gold plated molybdenum spacer to substrate and die to molybdenum spacer. The Sn10/Pb88/Ag2 solder is chosen as a high temperature solder for heatsink soldering. The Sn63/Pb37 solder is used for molybdenum soldering and die attachment. A customized aluminum fixture is used for alignment during soldering.
3) Cast molding and curing

A high resolution 3D printed mold is designed and fabricated for forming the silicone mold for PCoB module encapsulation. The chosen epoxy underfill material features a low coefficient of thermal expansion under glass transition temperature of 145°C. The material properties are listed in Table 3.5. The cast mold is shown in Figure 3.41. The PCoB module after molding process is shown in Figure 3.42.

Table 3.5 Encapsulation under fill material properties

<table>
<thead>
<tr>
<th>Dielectric strength</th>
<th>CTE</th>
<th>Cure time</th>
</tr>
</thead>
<tbody>
<tr>
<td>500 V/mil @AC</td>
<td>10 ppm/°C (&lt;Tg)</td>
<td>15 min @ 150°C</td>
</tr>
</tbody>
</table>

Figure 3. 39 Reflow soldering  
Figure 3. 40 Five zone reflow oven

Figure 3. 41 3D printed mold for cast mold  
Figure 3. 42 PCoB module encapsulation
3.9.2 PCoB Module Voltage Blocking Test

The PCoB module integrates two busbar-like substrates which have been bonded together through a preformed epoxy. The chosen epoxy has a curing temperature of 150°C for 40 minutes and an operation temperature up to 204°C. A test PCoB structure without power die has been made to test the voltage blocking capability. The tested module withstands 2000V easily. Another diode only module has been tested for reverse leakage at 25°C. The leakage current is well within the bare die diode’s datasheet. The diode module blocks 1200V for less than 100µA leakage current.

![Figure 3. 43 PCoB substrate blocking test](image1)

![Figure 3. 44 PCoB module diode blocking test](image2)

3.10 Switching Performance Evaluation

3.10.1 Double-pulse Tester

The inductive-load double-pulse (clamped inductive switching) test circuit has been designed for the power module switching test. The circuit topology is shown in Figure 3.45.
A typical double-pulse test waveform is shown in Figure 3.46. The magenta curve is the gate voltage, the cyan curve is the inductor current, the green curve is the DUT current and the blue curve is the voltage across the DUT. The first pulse width should be chosen based on the targeted switching current value, inductor value and DC bus voltage. The second pulse width is usually much shorter just leaving enough time for the switching ringing to settle down.
3.10.2 Measurement

In double-pulse tests, it is critical to measure current flow through the DUT. Since the SiC power semiconductor has a very fast di/dt capability, the current measurement mechanism needs to have a sufficiently high bandwidth to cover the rising and falling edges of current waveform. Also, the current measurement should be designed to not introduce extra parasitic loop inductance, which worsens the ringing. Different current measurement approaches have been studied in paper [50]. The PCoB provides the ultimate minimum inductance for double-sided modules, and hence benchmarks the fastest switching. In this research, a high speed current shunt has been chosen for the measurement due to its high bandwidth and the ease of very compact integration into the current loop. The A-2-01 current viewing shunt resistor fabricated by T & M Research Products, Inc. has been chosen in the double-pulse tester. The selected shunt resistor has a bandpass of 400MHz which is capable of measuring current rise time of 1 ns. The A-2-01 shunt resistor is able
to dissipate 4 W which corresponds to 20A continuous current measurement and much higher current rating for pulse measurement as in this research. The selected current viewing shunt resistor features a coaxial structure with BNC output connector which minimizes the introduced parasitic inductance. Current enters the structure from the stub at the end.

![Image](91x428 to 521x608)

Figure 3. 47 Current viewing shunt resistor geometry and dimension

The inductor current is measured through the hall sensor based current probe. The DUT gate to source voltage is measured through Tektronix P5200A 50MHz high voltage differential probe and the DUT drain to source voltage is measured through Tektronix THDP0100 100MHz high voltage differential probe.

3.10.3 Double-pulse Tester Board Design

Two different double-pulse tester PCB boards have been designed (Figure 3.48): board A is designed for testing TO247 packaged SiC power MOSFET, board B is designed for testing customized double-sided power chip on bus (PCoB) module. Figure 3.49 diagrams the functions on the tester systems. For board A, 1200V, 25mΩ rated Wolfspeed C2M0025120D SiC MOSFET
has been selected as device under test (DUT). The 1200V, 50A rated Wolfspeed C4D40120D SiC Schottky diode has been used as freewheeling diode for both designs. The gate driver circuits for both board A and B remain the same: Texas Instrument (TI) ISO5852SDW insulated gate driver IC followed by an IXDN614SI current booster IC providing 14 A driving capability for DUT. Murata 2w rated MGJ2D052005SC DC-DC converter provides isolated -5V and 20V outputs from 5V input voltage to drive the DUT. For turn-on, a 10 \( \Omega \) resistor has been used as an external gate resistor. For turn-off, the external gate resistance is realized by two 10 \( \Omega \) resistors in parallel. The schematic and PCB design of the double-pulse testers are included in the appendix. On each board, two 50 \( \mu F \) 900V film capacitors and multiple 1000V rated local ceramics capacitors have been put between DC positive and DC ground in the power loop. A customized 128\( \mu \)H inductor has been assembled and used in the test circuit. An external DSP control board has been connected to the gate driver externally to provide the PWM signal for gate control. The pulse width can be changed through communication between control board and personal computers. The shunt resistor is mounted through a customized copper connector.

Figure 3. 48 Double-pulse tester board A and B
3.10.4 Double-pulse Test Result

For the double-pulse tester board A, the turn-on and turn-off waveforms from a 600V DC bus voltage and 50A switching current, are shown in Figure 3.51 and 3.52. The magenta curve is the gate voltage, the green curve is the DUT current, and the blue curve is the voltage across the DUT. The turn on time is 32 ns and the turn off time is 16 ns; the turn off voltage spikes reach 140V.
Figure 3. 51 Turn-on waveform for double-pulse tester A

Figure 3. 52 Turn-off waveform for double-pulse tester A
For double-pulse tester board A, the turn-on loss is 1.2 mJ and turn-off loss is 0.2 mJ.

Due to the very limited number of the previously mentioned double-sided solderable 25 mOhms Wolfspeed SiC MOSFET die. A new type of Wolfspeed SiC MOSFET die under development with Cu metal on top has been used in the PCoB module for double-pulse test. This device has a much larger active area and input capacitance than the die originally planned to use.

For double-pulse tester board B, the turn-on and turn-off waveforms at 600V DC bus voltage and 47A switching current are shown in Figure 3.54 and 3.55. The blue curve is the gate voltage, the green curve is the DUT current (1A per 10 mV), and the red curve is the voltage across the DUT. The turn-on time is 75 ns and the turn-off time is 25ns; the turn off voltage spikes reaches 120V. The switching is slower than the 25 mOhms TO247 packaged MOSFET because the die used in the tested PCoB module is a much larger die with only 12 mOhms on resistance and about twice input capacitance.
Figure 3. 54 Turn-on waveform for double-pulse tester B

Figure 3. 55 Turn-off waveform for double-pulse tester B
For double-pulse tester board B, the turn-on loss is 1.4 mJ and turn-off loss is 0.4 mJ.

### 3.11 Power Device Temperature Transient

It will be very interesting to study the difference of thermal transient behaviors between conventional power module and double-sided module. For double-sided module, both top and bottom side of power semiconductor die are connected to highly heat-conductive thermal mass which by careful design can possibly absorb large amount of thermal energy during transient overloading condition. To start the study, a parametric quarter-symmetry model of conventional module has been defined and created as in Figure 3.57.
<table>
<thead>
<tr>
<th>Name</th>
<th>Expression</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>I_chip</td>
<td>3</td>
<td>8</td>
</tr>
<tr>
<td>w_chip</td>
<td>3</td>
<td>8</td>
</tr>
<tr>
<td>t_chip</td>
<td>0.15</td>
<td>0.15</td>
</tr>
<tr>
<td>t_solder</td>
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<td>0.1</td>
</tr>
<tr>
<td>keepout</td>
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<td>2</td>
</tr>
<tr>
<td>t_copper</td>
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<td>0.25</td>
</tr>
<tr>
<td>t_dielectric</td>
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<td>0.625</td>
</tr>
<tr>
<td>keepout2</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>t_baseplate</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>freq_sw</td>
<td>10e3</td>
<td>10000</td>
</tr>
<tr>
<td>Duty</td>
<td>0.5</td>
<td>0.5</td>
</tr>
<tr>
<td>TT</td>
<td>1/freq_sw</td>
<td>1E-4</td>
</tr>
<tr>
<td>TT_on</td>
<td>Duty*TT</td>
<td>5E-5</td>
</tr>
<tr>
<td>TT_off</td>
<td>(1-Duty)*TT</td>
<td>5E-5</td>
</tr>
<tr>
<td>I_cond</td>
<td>50</td>
<td>50</td>
</tr>
<tr>
<td>I_leak</td>
<td>100e-6</td>
<td>1E-4</td>
</tr>
<tr>
<td>R_con</td>
<td>25e-3</td>
<td>0.025</td>
</tr>
<tr>
<td>p_con</td>
<td>I_cond^0.2*R_con</td>
<td>62.5</td>
</tr>
<tr>
<td>V_block</td>
<td>800</td>
<td>800</td>
</tr>
<tr>
<td>p_leak</td>
<td>V_block*I_leak</td>
<td>0.08</td>
</tr>
<tr>
<td>E_on</td>
<td>5e-3</td>
<td>0.005</td>
</tr>
<tr>
<td>E_off</td>
<td>2e-3</td>
<td>0.002</td>
</tr>
<tr>
<td>t_rise</td>
<td>70e-9</td>
<td>7E-8</td>
</tr>
<tr>
<td>t_fall</td>
<td>50e-9</td>
<td>5E-8</td>
</tr>
<tr>
<td>p_sw_on</td>
<td>E_on/t_rise</td>
<td>71429</td>
</tr>
<tr>
<td>p_sw_off</td>
<td>E_off/t_fall</td>
<td>40000</td>
</tr>
<tr>
<td>t_tran</td>
<td>5e-9</td>
<td>5E-9</td>
</tr>
</tbody>
</table>

Figure 3. 57 Transient thermal model definition
To study the temperature transient due to switching, the turn-on and turn-off energy have been set to 5 mJ and 2 mJ respectively. And the turn-on and turn-off time is 70 ns and 50 ns respectively. The switching frequency is 10 kHz and the duty cycle is 0.5. The transient temperature curve is shown in Figure 3.60. Even the turn-on and turn-off energy are set to be somewhat higher than real applications, the temperature spikes has a negligible magnitude compared to junction operation temperature under full load.
For temperature transient due to sudden load change, the same model is used. The power
dissipation is a step function which suddenly jumps from 0 watt to 50 watts. To estimate the
influence of increased thermal mass, another model with material thermal capacitance doubled is
simulated. The results of the two simulations are summarized in Figure 3.61.

![Figure 3.61 Transient temperature due to sudden load increase](image)

Doubling the thermal capacitance will increase the thermal transient time constant
significantly. This indicates a much better transient over-current capability for double-sided power
module. However, detailed double-sided module model needs to be created and simulated in the
future.

### 3.12 Conclusion

This chapter proposed a double-sided air-cooled Power Chip on Bus (PCoB) module
structure. This structure features liquid-cooling equivalent thermal capability with low inductance.
The proposed module design has been extended to phase leg topology for EV motor drive
application. A single switch version of PCoB module has been researched in detail which validates
the viability of PCoB module. Extensive multi-physics simulation and verification show less than 10nH power loop and less than 5nH gate loop parasitic inductances. About 0.5 °C/W junction-to-air ambient thermal resistance is achieved for the air-cooled single switch module design. Also, a 260°C die attachment material is introduced along with a process to create double-sided die attachment. 2000V blocking capability is verified through experiment for the proposed package structure. A double-pulse tester has been designed and fabricated to test the switching behavior of the PCoB module. The results indicate good switching performance. However, the PCoB switching performance has not yet been optimized due to the gate driver design and lack of original selected smaller power dies.
Chapter 4. Future Work

Chapter 1 includes SPICE simulations of double pulse test circuit for studying SiC MOSFET transient switching. In future, better SPICE model can be made to include parasitic from double-pulse tester PCB layouts. Such detailed model will be very helpful for optimizing device switching.

Chapter 2 demonstrates an optimization procedure for power module DBC substrate design based on thermal-mechanical FEA simulation. A better optimization model can be made to take care of more complicated thermal-mechanical failure mechanisms and voltage blocking requirement with non-standard geometry generation capability. Also other mode of thermal-mechanical stress can be used for determining the ceramic breakdown criterion such as maximum normal stress on the ceramic to metal interfaces. Double-sided PCoB transient thermal-mechanical study needs to be completed to understand the relation between power module’s thermal capacity and power module maximum current rating and switching frequency. To physically test this, a transient temperature measurement approach also needs to be developed.

Chapter 2 also illustrates the application of a multi-physics simulation based design approach in high voltage SiC power module design. Two different optimization approaches needs to be completed and compared for cold-plate design 1) A FEA based cold-plate design optimization needs to be done to minimize the liquid cooling power with specified inlet temperature, maximum allowable junction temperature and power dissipation. 2) A FEA based cold-plate design optimization needs to be done to maximize the convective heat transfer coefficients.

Chapter 3 introduces the power chip on bus (PCoB) module design. A phase leg module needs to be fabricated to fully demonstrate the improved switching capability. And a PCoB module
based three-phase motor drive system needs to be built to demonstrate the air-cooling inverter system performance.
REFERENCES


[29] Desmond Y.R Chong, W.E. Lee,"Mechanical Characterization in Failure Strength of Silicon Dice” 2004 Inter Society Conference on Thermal Phenomena


[39] X. Li, H. Zhang, P. Alexandrov and A. Bhalla, "Medium voltage power switch based on SiC JFETs," 2016 IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA


Appendix A- Double-sided Power Module Review

Figure A.1 APEI double-sided planar connection power module

Figure A.2-a University of Arkansas double-sided power module

Figure A.2-b University of Arkansas double-sided power module
Appendix B- Multiple-phase-legs Power Chip on Bus (PCoB) Module

Figure B.1 Three-phase PCoB module

Figure B.2 Three-phase PCoB module (transparent view)
Appendix C- Chip Top-side Metallization Process

1) MOSFETs preparation

SiC power MOSFETs are soldered on to gold plated molybdenum spacer for enlarging back side area for handing.

![Figure C.1 SiC die on molybdenum spacer](image)

All dies have been treated with a Al/Al2O3 etching solution (Aluminum Etch Type A) which is made of 40-80% phosphoric acid, 3-20% acetic acid, 1-5% nitric acid. The solution helps to eliminate the aluminum oxide. The etching time is precisely controlled to 1 minute and 30 seconds so that the aluminum pad will not be attacked.

2) Diode holder and metal mask cleaning

Brass diode holder and metal mask are cleaned in acetone before further processing.
3) Photoresist spinning

Negative photoresist JSR NFR 016 D2 is used for metallization.
4) Photo mask application, alignment and UV exposure

With Karl Suss MA6 Mask Aligner is used for photo mask alignment for SiC MOSFETs.
Dies with photoresist are then developed in MICROPPOSIT(TM) MF(TM)-319 Developer for 2 mins.

5) Plasma etch

![Plasma etch system](image)

Figure C.12 Plasma etch system

6) E-Beam deposition

Titanium/Nickel/Silver layers are deposited onto the dies sequentially in the E-Beam deposition chamber with thickness of 300nm, 380nm and 1000nm respectively. It takes about three hours to pump the chamber and three hours to deposit metals.
7) Liftoff

After E-Beam deposition, the dies are immersed in NMP liftoff solution (N-Methyl-2-pyrrolidnone) for metal liftoff process. The immersion time is two hours.
Figure C.17 Die immersed in liftoff solution

Figure C.18 Unwanted metal peels off after liftoff
Appendix D- 3D Printed Part for PCoB Module Testing and Assembling

Figure D.1 3D printed air channel for PCoB module thermal test
Figure D.2 Air channel with PCoB module for thermal test
Figure D.3 3-D printed parts for PCoB cast mold process
Appendix E- Flexible Circuit and PCB Designs

Figure E.1 Top copper layer

Figure E.2 Bottom copper layer

Figure E.3 Board top view

Figure E.4 Board bottom view
Figure E.5 Double-pulse tester detailed schematic

Figure E.6 Double-pulse tester PCB board A layout
Figure E.7 Double-pulse tester PCB board B layout