ABSTRACT

TAN, KAI. Development of Solid State Circuit Breakers for 380V DC Microgrid Protection. (Under the direction of Dr. Alex Q. Huang and Dr. Iqbal Husain).

The DC distribution system is becoming an appealing research spot in recent years and has also been investigated and applied in DC shipboard, airplane system, telecommunication system, DC buildings and DC data centers, etc. However, the protection of DC system is facing several harsh issues including the arcing phenomenon at the time of disconnection, the large and fast inrush current and discharge current generated by distributed capacitance on DC bus, etc. The traditional Miniature Circuit Breaker (MCB), Molded Case Circuit Breaker (MCCB) and fuses are not the qualified candidates for dealing with these new issues. A new protection architecture is proposed for 380V DC Microgrid protection. Three different equipment are proposed, analyzed, developed and tested for different current rating in this paper. A hot-swappable outlet is designed with zero standby power to eliminate the arcing with solid-state devices. Moreover, it is used to isolate the downstream fault with current limiting capability. Then a solid-state node circuit breaker is created with paralleled devices. Interleaved hiccup startup and transient junction temperature monitoring are presented. Finally, a hybrid branch circuit breaker is designed for the high current application. A novel driving strategy based on mechanism analysis is considered and tested for performance enhancement. Besides, multiple solid-state devices are investigated and selected for above circuit breaker applications. Comparison and evaluation based on specifications and experimental results are introduced.

Development of Solid State Circuit Breakers for 380V DC Microgrid Protection

by
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BIOGRAPHY

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CHAPTER 1

Introduction

1.1 Research background

AC power supplies and plugs are widely used nowadays. It is the consequence of a debate of currents: AC (alternating current) versus DC (direct current) between Nikola Tesla and Thomas Edison which took place in the 19th century. The AC system won the war and ruled the platform for electrical transmission across the world in the whole 20th century. But in the 21st century, the DC system has been more and more involved in the electrical system due to the technology revolution. However, in the 21st century, the DC distribution system is becoming more and more utilized in electrical systems due to the development of modern power electronics technology. From a power source point of view, more and more distributed and renewable sources are more DC friendly such as photovoltaic panels. From a power transmission point of view, high voltage DC is the only technology that allows power to be transmitted economically over interstate long distances. From a power user point of view, we are utilizing more and more direct and indirect DC loads in our daily life due to new technologies, such as LED lights, computers, communications and numerous types of batteries used in consumer electronics.

Figure 1.1 shows the DC microgrid in the plan of Future Renewable Electric Energy Delivery and Management System[1]. The DC microgrid system is a port with bi-directional power flow capability and high efficiency since the skip of low voltage DC/AC inverter which is the lowest efficient part in SST. [2]

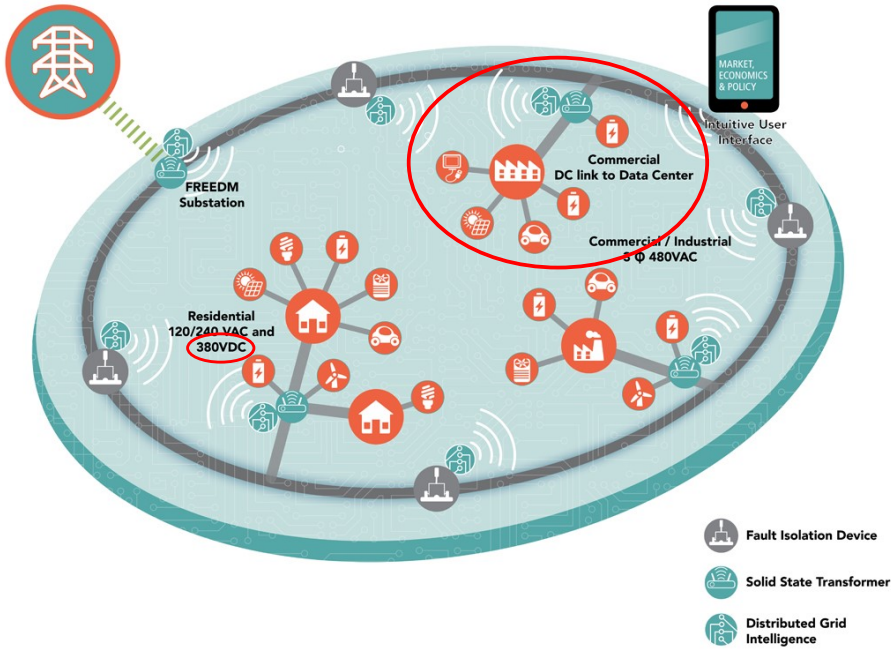


Figure 1.1 DC micro grid in FREEDM systems center

Besides DC microgrid in FREEDM system, the DC distribution system has also been investigated in DC shipboard, airplane system, telecommunication system, DC buildings, and DC data centers, etc. [3]–[15]

1.2 Review of 380V DC Microgrid Eco-System

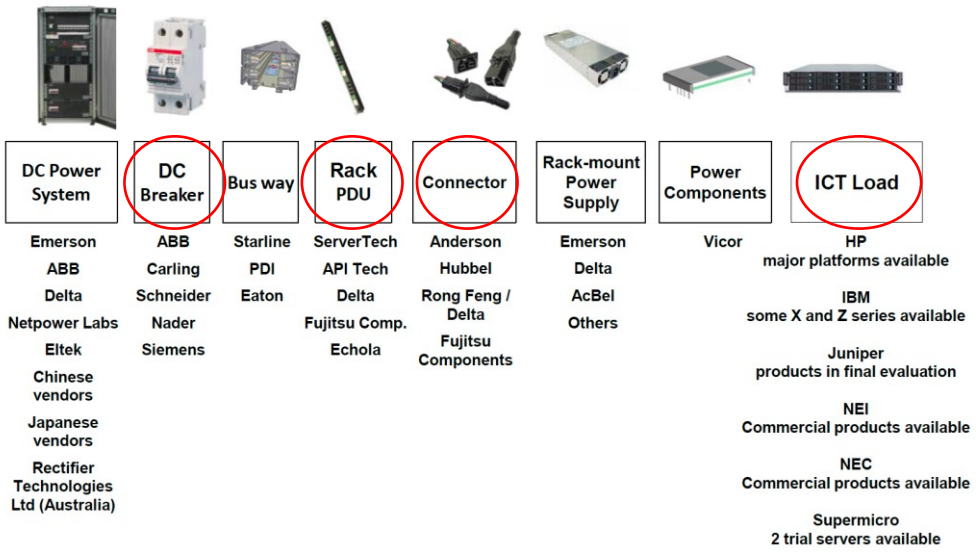


Figure 1.2 Summary of 380V DC eco-systems

For 380V DC system, the eco-system[16] from chip to the grid is being built and developed by many manufacturers. Figure 1.2 shows a brief summary of 8 kinds of equipment. The DC circuit breaker, power distribution strip, connector and ICT load are the equipment our research most interested in.

In Zurich, Switzerland, May 30, 2012, ABB and Green® launched 380V DC data center employing HP servers with ±190V DC bus. HP provided the HVDC-enabled IT for this technology showcase, including servers and storage, such as HP X1800 G2 Network Storage System, HP DL385 servers, and HP Blade System c3000. [7], [12], [14], [17]

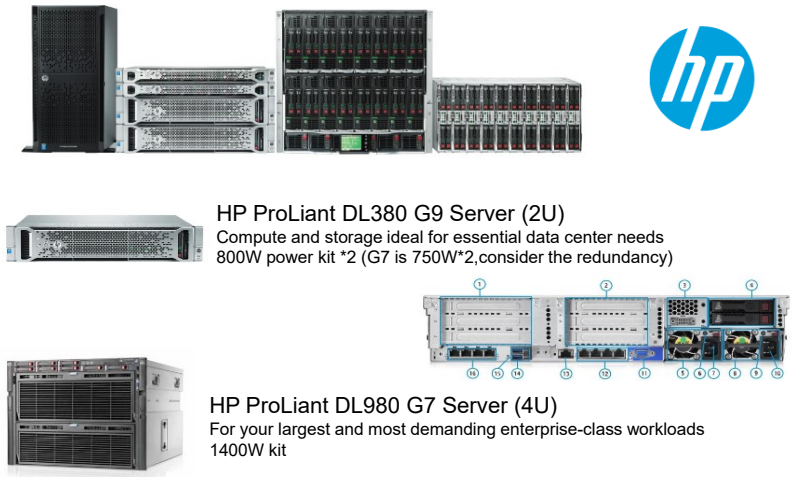


Figure 1.3 HP 2U DL380 servers and 4U 980 servers

The power rating is about 2A for DL380 2U and 3.5A for DL980 4U. Figure 1.4 shows how the servers connected with power strips [16]. Each server is plugged into one socket. About 4 sockets are protected with a circuit breaker or fuse.

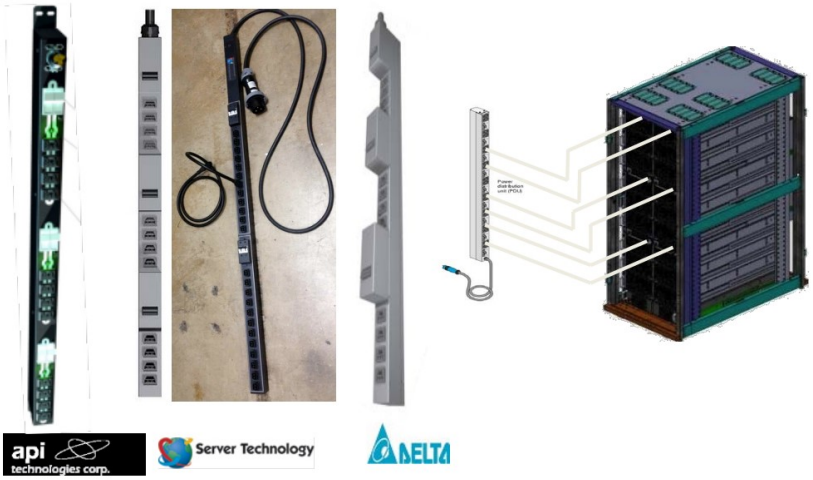


Figure 1.4 DC power strips from multiple manufacturers

1.3 Issues in DC Microgrid Protection and Proposed Solution

Although there are many benefits for applying DC distribution system in above applications. There are several issues in DC system protection which are not critical in AC system. Those issues slow down the speed of DC distribution system development in industry.

1.3.1 Arcing

The first issue is the arcing at the moment of disconnection. The speed and safety of arc extinguishing are very important for both equipment and human safety. This phenomenon in AC system is not as severe as in DC system because of the naturally zero crossing of sinusoidal AC waveform. Figure 1.5 shows the arc behavior in 400V DC system disconnection[15], [18]. Many solutions have been proposed to reduce the arcing both in connector and circuit breakers design. [19]–[21]

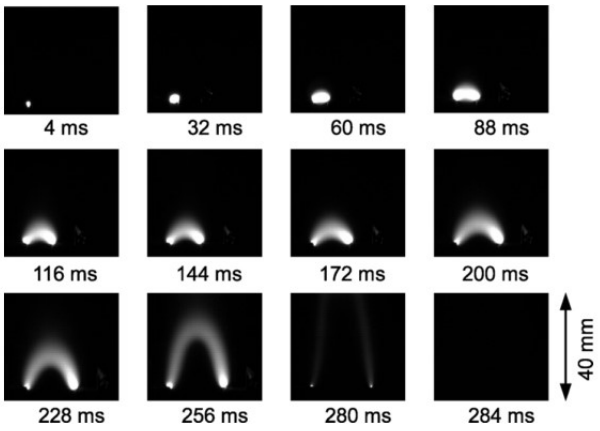


Figure 1.5 Snapshots of arc behavior in 400V DC disconnection[18]

1.3.2 DC Bus Capacitance

The second important issue is the large capacitance connected to the DC bus. It helps to keep the DC voltage stiff with small ripple and filter the high-frequency harmonics to decouple the power with limited line inductance. However, the inrush current may cause unexpected circuit breaker trip when the user's capacitance is connected to the DC grid and bus. And the discharge current from these capacitor components is too large (10kA) and too fast (milliseconds) for molded case circuit breakers (MCCB) when a fault occurs. This kind of current may affect the fault isolation and lead to a large portion of end users in this system losing power. It may also damage the circuit breakers[18], [19], [21], [22]. Figure. 1.6 shows the DC voltage endurance envelope which is proposed by EPRI and IEEE respectively [23], it indicates that each PSU on DC bus need to have a capacitance with the capability of load voltage ride through in a certain time within a certain voltage drop. These capacitance contributes together on DC bus for higher inrush current, discharge current and dissipated energy. [4], [19], [20], [23]–[26].

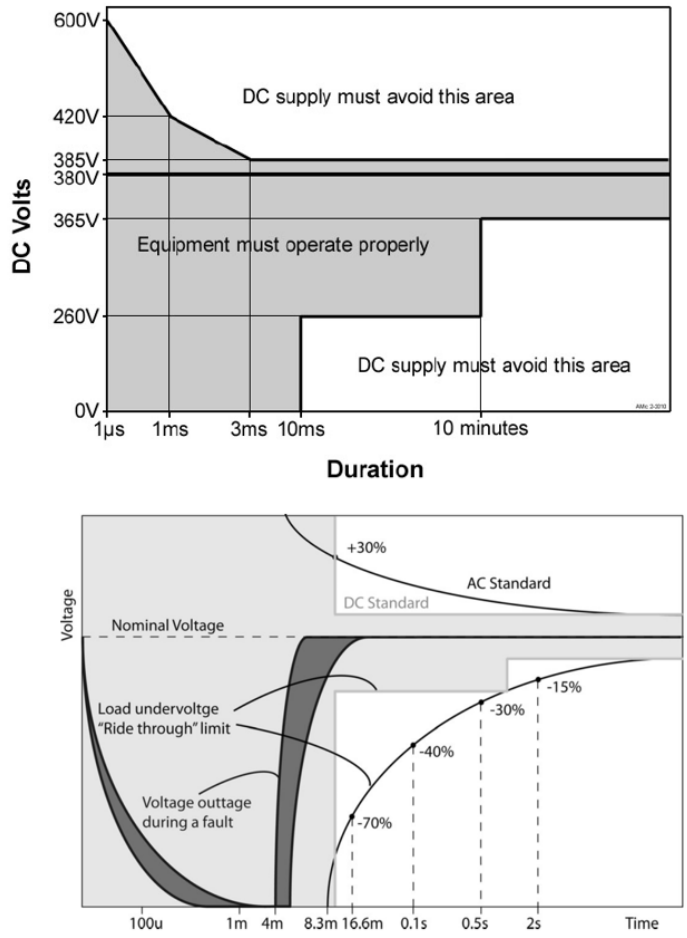


Figure 1.6 DC Voltage endurance envelope proposed by EPRI and IEEE[23]

1.3.3 Protection Speed

Another important aspect is the trip speed of circuit breaker. Figure 1.7 gives the trip curve of a 15A MCCB[27], [28]. The trip speed of 15A MCCB is slow (10~100ms) with a high threshold (500A) once a fault occurs. It will drop the bus voltage to zero since the MCCB cannot isolate and clear the fault rapidly.

All other PSU will also be affected because the long trip time has already exceeded the low voltage ride through capability of PSU. The DC bus voltage will drop to a low value and affect the whole neighborhood. For avoiding this low voltage, all PSU nearby need to have larger capacitance for stronger low voltage ride through capability which deteriorates the second aspect above. In sum, the slow trip speed of traditional mechanical circuit breaker requires larger bus capacitors to meet hold up time requirement for slow fault clear speed.

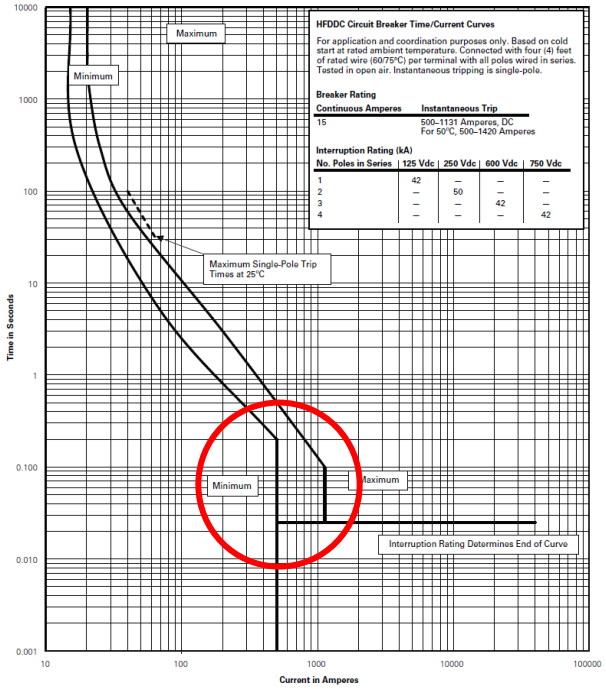


Figure 1.7 15A MCCB trip curve[27]

1.3.4 Proposed solution

Considering all above aspects, a 380V DC system protection architecture is proposed with 3-level hierarchy circuit protection architecture[29]. A DC datacenter application with unidirectional power flow is employed to demonstrate the protection system in Figure 1.8.

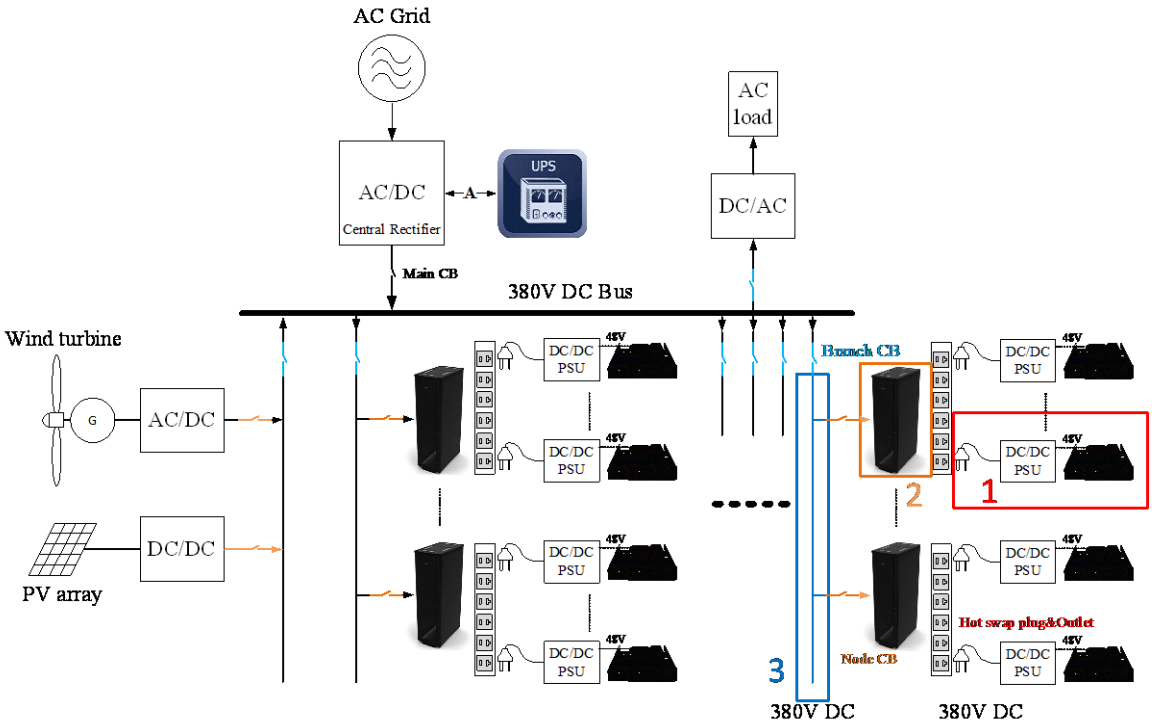


Figure 1.8 Circuit protection hierarchy for DC data center application

1) PSU level 1

Each 2U or 4U server of the data center is connected with a hot-swappable solid state outlet. It has basic overcurrent protection and current limiting capability with the fastest speed to trip the downstream fault in zone 1 without impacting other servers in the neighborhood. The inrush startup capability is designed for capacitive 0-380V startup. More importantly, the outlet extinguishes the arcing with embedded solid state devices makes the plug and unplug similar to traditional AC distribution outlet. The nominal current rating is designed at 5A and 2kW for typical 2U or 4U server PSU unit.

2) Nodes level 2

A node solid state circuit breaker is proposed to trip and limit the overcurrent caused by faults between itself and hot-swap outlet in zone 2. The response time is also very fast in microseconds with arcing been extinguished within solid state devices. It is used to isolate the fault within the node. The current rating is designed at 30A and 12kW, working with 6 outlet slots in a DC power strip.

3) Branch level 3

Finally, a hybrid branch circuit breaker is proposed and designed for large current application and multiple nodes. It is a combination of a fast-mechanical switch and solid-state devices to trip high current (180~200A) without arcing and conduct with low loss. The trip speed is slower than solid state device but faster than other traditional mechanical solutions to limit the discharge current and isolate the fault within the branch as in zone 3. Each branch is isolated with hybrid branch circuit breaker without affecting others.

All three levels proposed have current limiting and tripping with fast speed and arcing free, makes the whole system can have stronger low voltage ride through capability with smaller capacitance.

1.4 Dissertation Outline

In Chapter 2, the critical characteristic, particularly for DC circuit breaker, is identified and defined. Multiple solid state devices are listed as candidates with DC circuit breaker related characteristic evaluation and comparison. Waveforms with the experimental result are shown for demonstration. SiC devices show more outstanding performance than traditional Si rivals in proposed DC circuit breaker applications with lower conducting loss and higher peak power density per die size.

In Chapter 3, a hot-swappable outlet is developed with the innovative scheme with energizing pad to have zero standby power feature. It also helps to avoid the arcing at the time of disconnection. The operation modes are presented with inrush current limiting, dual threshold overcurrent protection and over temperature protection to enhance its safety and reliability. Experimental results are displayed to verify the implementation of all proposed features.

In Chapter 4, the node solid state circuit breaker is proposed and developed. Multi-channel interleaved hiccup startup and dual threshold overcurrent protection are invented and realized with innovated analog driver circuit close loop control. It helps to trip the fault and saturate the current without influencing other nodes in the neighborhood which can reduce the capacitance in all nodes and redefine the voltage endurance envelope without voltage outrage during node fault. This development helps strengthen the robust of DC microgrid and reduce the cost of capacitors and loss on voltage outrage.

In Chapter 5, the hybrid branch circuit breaker is proposed, analyzed and developed for high current application. The cost, conduction loss and volume of solid state device limit it in high current operation. The fast mechanical switch is needed to perform as a main current path. The criteria for the mechanical switch are investigated and defined. The innovative driving strategy is proposed to accelerate the trip speed and reduce the contact resistance. Experimental results of proposed driving strategy are shown with 200A to prove its feasibility. Transient of current commutation is tested and analyzed.

Chapter 6 is the conclusion and the outlook for the future work.

CHAPTER 2

Solid State Devices for DC Circuit Breaker Application

2.1 Introduction and Motivation

In this Chapter, multiple solid-state devices are analyzed and evaluated particularly for 380V DC circuit breaker application. As we known, the characteristics and parameters of solid state devices vary at different static and dynamic conditions. Table 2.1 shows part of common definitions of the majority characteristics of a MOSFET as an example.

Table 2.1 Definitions of MOSFET Parameters

Symbol	Description
$V_{(BR)DSS}$	Drain-source breakdown voltage
$V_{GS(th)}$	Gate threshold voltage
$R_{DS(on)}$	Static drain-source on-resistance
Q_g	Total gate charge
T_j	Max. operating junction temperature
I_D	Drain current (continuous)
$R_{th(j\text{-}case)}$	Thermal resistance junction-case

Most of them are related and determined by the principle of semiconductor physics & devices. These factors affect each other and make the device selection optimization for each hardware design is required.

In traditional switching application, one important method for evaluating MOSFETs is according to Figure of Merit (FOM). It compares the gate charge (Q_g) against the static on-state resistance ($R_{DS(ON)}$).

$$\text{FOM} = Q_g \times R_{DS(ON)} \tag{2.1}$$

In semiconductor devices, the lower the $R_{DS(ON)}$ the higher the Q_g will be. So, this multiplication can be used to have a like-for-like comparison and evaluate certain device technologies.

Some other similar methods for comparing devices were also proposed. The "Baliga high-frequency figure of merit" (BHFFOM) [30] and "new high-frequency figure of merit；" (NHFFOM) [31] use the input capacitance (Ciss) and the output capacitance (Coss) instead of the gate charge (Q_g) to evaluate like-for-like comparison in application with switching loss consideration.

However, the concerns for DC solid state circuit breaker is different with previous FOM consideration. Besides, the new SiC devices introduce some new advantage and good features compare with Si devices. It also needs to be considered with foresight. All three circuit breakers have different requirement because of the hardware design and feature differences which is also need to be considered.

In sum, a new method for analysis, evaluation, and optimization in device selection is proposed and defined based on multiple Si and SiC devices. The different criteria for devices between pure solid state and hybrid circuit breaker application are also presented in this chapter.

2.2 Specific Characteristics for DC Circuit Breaker Application

2.2.1 Typical Operations Stages of DC Circuit Breaker Application

In DC distribution system, there are a lot of capacitive components in each end users to keep the bus voltage stiff with small ripple and filter the high-frequency harmonics cause by switching converters. The inrush current is one issue for capacitance which may cause unexpected circuit breaker trip when the user is connected to the DC distribution system. The second issue caused by these capacitive components is the discharge current for low impedance or short circuit. This current is too large (kA) and rises too fast (in several ms) for both MCB and MCCB when a fault occurs. This kind of current may affect the fault isolation and a large portion of end users in this system are affected. It also may damage the circuit breakers with repeat arc[19][32]–[34].

The proposed operation modes and flowchart is shown in figure 2.1. It can be identified as latch off mode, inrush hiccup startup mode, normally on mode, dual threshold over current trip and over temperature trip.

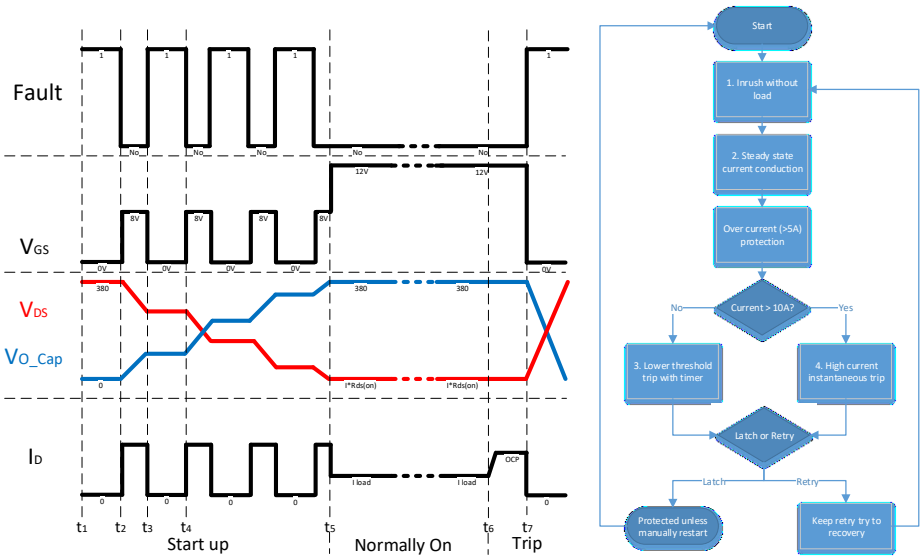


Figure 2.1 Proposed operation strategy for circuit breaker

A. Latching off mode:

Before t_2 and after t_7, the whole circuit breaker is latched off. The devices are controlled in open circuit to trip the main circuit due to over current or over temperature fault. The fault indicator is high to indicate a fault condition.

B. Hiccup startup mode:

At the moment of t_2, the circuit breaker is set up to start manually or remotely with fault been cleared. The sum of the drain to source voltage on devices of two bus is equaled to 380V because the output bus capacitor voltage is zero. The devices are still in off state with only leakage current. From t_2, the control circuit initializes the designed hiccup startup and generates a low V_{GS} close to threshold V_T to ensure the devices works in the saturation region to limit the current with a short pulse (t_2-t_3). The output capacitor is charged a train of pulses like this and its voltage is increased. The drain to source voltage on devices is still large which makes power stress large during the pulse because it operates in saturation. Therefore, the pulse width and the value of limited current need to be designed within the safe operation area (SOA) of the N channel MOSFET device to avoid the device failure due to the excessive power dissipation. After each short pulse, the device is off again from t_3-t_4 to control the average power stress and cool the device down. The voltage on the device and capacitor remain the same during this period.

The current on the drain is sensed with closed-loop control to a given value with adaptive V_{GS}. The on-off hiccup process continues until the voltage of the output capacitor is close to the bus voltage. Then the control circuit fully turns on the N channel MOSFET device with 12V V_{GS} at the moment of t_5. Because the drain to source voltage is already close to zero, there is no inrush current, the normal load current flows continuously.

C. Normally on mode:

The solid-state circuit breaker works in normal conduction mode. The devices keep fully turn on to keep lowest $R_{DS(ON)}$ so the power loss on the solid-state device is minimized.

D. Overcurrent trip:

The strategy is implemented by a controller to monitor over current or short fault. The current threshold I_{Limit} is used to trip the real over current fault and filter nuisance transient noises.

E. Over temperature trip:

The controller is kept monitoring the temperature of the hot spot from the circuit breaker, typically the heat sink on devices. Once the temperature sensor output over the programmed threshold, the circuit breaker is controlled to trip to protect the solid-state devices.

2.2.2 Characteristics criteria for circuit breaker application

One of the most crucial components in DC solid state circuit breaker is the embedded solid-state device. Traditionally, Si devices including MOSFET, IGBT and etc. are considered the best options among all solid state devices in low voltage range[35]–[37]. And a lot of researchers proposed and developed many new designs based on SiC devices due to the development of power devices technology in recent years[32], [38]. For developing the proposed 380V/15A solid state circuit breaker using paralleled devices, the criteria for choosing the solid-state device in proposed design is discussed[39]. From the analysis in the previous section, the most important characteristics of solid state device for 380V DC circuit breaker application are listed:

1. *Static conduction resistance ($R_{DS(ON)}$):*

Low static conduction resistance is one of the most important parameters for the circuit breaker to reduce the steady-state thermal stress and power loss in normally on mode. It directly related to the efficiency of the circuit breaker. For Si IGBT, the initial $V_{CE(SAT)}$ (about 0.7~1V for 600V IGBT) makes the power loss larger than paralleled MOSFET in low current range (<20A) for 380V DC circuit breaker application. It needs a larger heatsink or forced air cooling for IGBT than natural convection. The SiC devices have better static conduction resistance due to the physics characteristic of wide-bandgap material compare with Si. Many manufacturers have released 1200V SiC devices which is a good candidate for circuit breaker application. This value is related to die size which needs to be specified for evaluation.

2. Thermal impedance in steady state and transient state:

The steady state thermal resistance can be calculated with:

$$R_{th} = \frac{L}{kA} \tag{2.2}$$

L is the thickness of the material (cm), A is the area of the material (cm-2), and k is the thermal conductivity ($W \cdot cm^{-1} \cdot K^{-1}$).

For the SiC, this value is about 4.9 and Si is about 1.5 [40], [41]. This makes the steady state thermal resistance of SiC device much better than Si device with same L and A. It also means that the die size of SiC device can be saved to achieve equivalent thermal resistance with larger die size Si device.

For the same heatsink design and power loss, the device junction temperature will be lower if the steady-state thermal resistance is smaller. It means that the smaller steady-state thermal resistance can work with more compact heatsink design to save the cost.

For the transient thermal impedance, the thermal capacitance plays an important role. The larger thermal capacitance makes the transient thermal impedance smaller to have lower junction temperature rise in short pulse during hiccup startup. It will reduce the risk of device failure caused by thermal issue during pulses hiccup startup.

The thermal resistance also contributes to the transient state. The cooling down period can be shorter with smaller thermal resistance to shortening the startup duration.

3. Temperature coefficient in the steady and transient state:

The steady state temperature coefficient is important to achieve evenly current sharing for paralleled operation. The MOSFET device is better than IGBT on this characteristic makes it can be easily used for multiple MOSFET parallel operation to share the large steady-state current and thermal stress.

For the hiccup startup, the saturation current is a function of the drain to source voltage, the gate voltage, and junction temperature:

$$I_D = f(T_J, V_{GS}, V_{DS}) \tag{2.3}$$

The paralleled devices have same VDS and VGS. However, the threshold voltage VT of devices varies in ±1V makes the initial ID on each device are not equal. The larger saturation ID brings larger thermal stress and higher junction temperature with self-heating.

$$P_1 = I_{D1} \cdot V_{DS} > I_{D2} \cdot V_{DS} = P_2 \tag{2.4}$$

This higher junction temperature will affect the value of I_D due to equation 2.3. The temperature coefficient of T_J and V_T need to be a negative feedback to share the I_D to have equally T_J.

4. Temperature range:

The SiC devices can work with much higher junction temperature than Si device, which makes SiC devices have more margin for hiccup startup, over current and over temperature trip and lower risk in failure due to the high junction temperature.

5. Drive circuit power consumption:

The power consumption of driver circuit is a part of total power loss besides the device conduction loss. The normally ON feature of SiC JFET from USCi makes it can consume the least power on driver circuit with 0V VGS. The current driven BJT will consume more power in driver circuit compare with voltage driven MOSFET.

2.3 Candidates for 380V DC Microgrid protection

To develop the proposed solid state circuit breaker using paralleled devices, 4 different solid state devices [42]–[45] are considered as candidates in 380V DC solid state circuit breaker application. The characteristics listed in section III is evaluated among candidates with considering the die size. Table 2.2 lists the 4 devices and their basic characteristics for further evaluation.

Table 2.2 Characteristics of Solid State Devices for DC Circuit Breaker Application

Type	Manufacturer	Part No.	$V_{(BR)DSS}$ (V)	R_{DS}(on) @25 °C(mΩ)	Die Size (mm^2)
Si MOSFET	Infineon	IPW65R019C7	650	19	68.29
Si MOSFET	ST	STY145N65M5	650	14	121.88
SiC MOSFET	WOLFSPEED	C2M0025120D	1200	25	26.02
SiC JFET	USCi	UJN1205K	1200	45	9.42

2.3.1 Characteristics for node solid state circuit breaker

Characteristics and Specifications Analysis and comparison:

1. Static conduction resistance ($R_{DS(ON)}$):

As stated above in section III, the $R_{DS(ON)}$ can be evaluated with considering its die size, the specified value is listed in table 2.3.

Table 2.3 $R_{DS,SP(ON)}$ comparison of 4 candidates

Type	Manufacturer	Part No.	$R_{DS(on)}$ @25 °C(mΩ)	Die Size (Cm^2)	$R_{ds,SP(ON)}$@25 °C(mΩ*cm^2)
Si MOSFET	Infineon	IPW65R019C7	19	0.6829	12.9751
Si MOSFET	ST	STY145N65M5	14	1.2188	17.0632
SiC MOSFET	WOLFSPEED	C2M0025120D	25	0.2602	6.505
SiC JFET	USCi	UJN1205K	45	0.0942	4.239

From Table.3 2, the SiC JFET is the best candidate considering the die size. Value of SiC devices is 1/3 to 1/4 of Si devices. This makes SiC devices very competitive in circuit breaker application with smaller die size and lower power loss compare with Si devices.

2. Thermal impedance in steady and transient state

The typical steady-state thermal resistance is listed in table 3. And specified value is calculated with die size.

Table 2.4 Thermal impedance of 4 candidates

Type	Manufacturer	Part No.	$R_{TH,J\text{-}c}$ (°C/W)	Die Size (Cm^2)	$R_{TH,J\text{-}c(sp)}$ (°C/W *cm^2)
Si MOSFET	Infineon	IPW65R019C7	0.28	0.6829	0.1912
Si MOSFET	ST	STY145N65M5	0.2	1.2188	0.2438
SiC MOSFET	WOLFSPEED	C2M0025120D	0.24	0.2602	0.0624
SiC JFET	USCi	UJN1205K	0.65	0.0942	0.0613

The calculated results are close to previous analysis in section 2.2. The SiC devices have larger thermal conductivity makes its thermal resistance is about 1/3 to 1/4 of Si devices with same die size or SiC devices can have similar thermal resistance with 1/3 to 1/4 die size compared with Si devices.

3. Temperature coefficient in steady and transient state

The all four candidates have positive $R_{DS(ON)}$ -T_J coefficient which is good for steady state current sharing with the paralleled operation. It is shown in Figure 2.2.

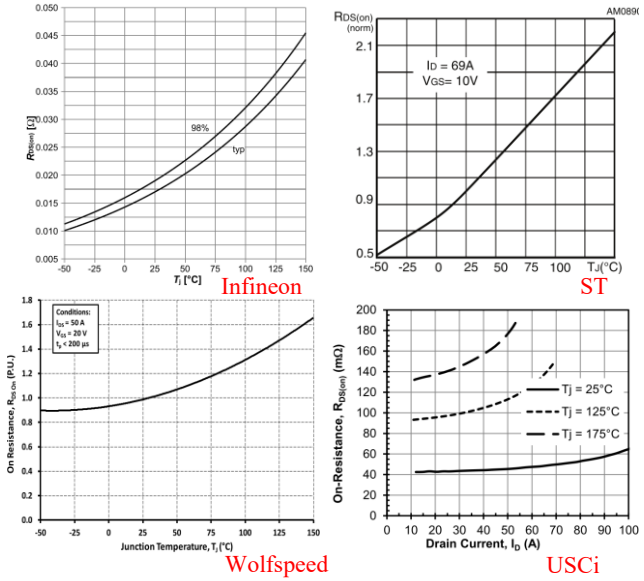
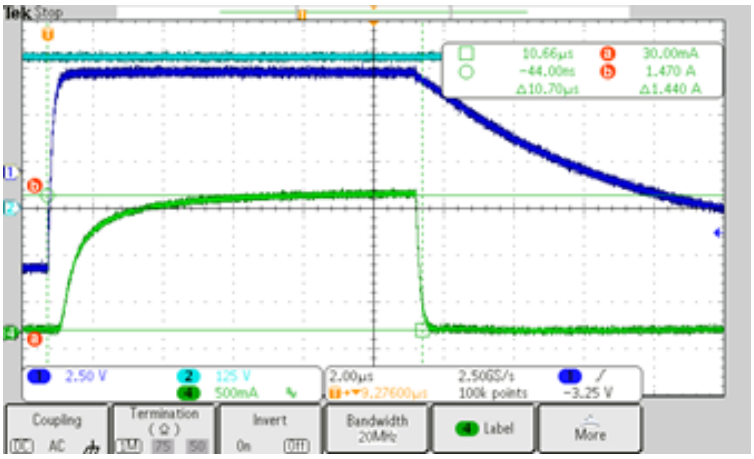


Figure 2.2 $R_{DS(ON)}$-T_J coefficient of 4 candidates for steady state

As analyzed above, the transient I_D-T_J coefficient is very important during hiccup startup with multiple devices parallel. Figure 2.3 shows the test setup with different junction temperature and a typical saturation current waveform with short pulse test with minimum self-heating. The ceramic heat plate is used to heat the junction and a very short pulse (10us) is tested to avoid the temperature rise due to internal power dissipation.

(a)



(b)

Figure 2.3 (a) Short pulse saturation test setup, (b) Typical short pulse test with saturation current

In Figure 2.4, all four devices saturation current is listed under different junction temperature for same V_{GS} in each device itself. The SiC JFET from USCi is the only device has the negative coefficient, which makes it the best option for dynamic current sharing during hiccup startup mode.

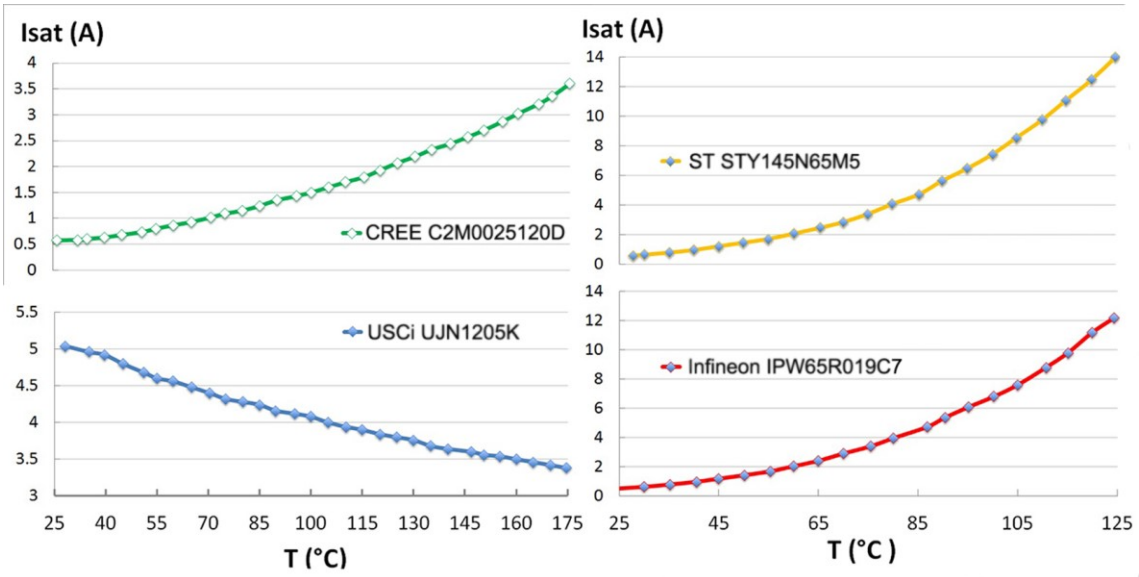


Figure 2.4 Saturation current vs. Junction temperature

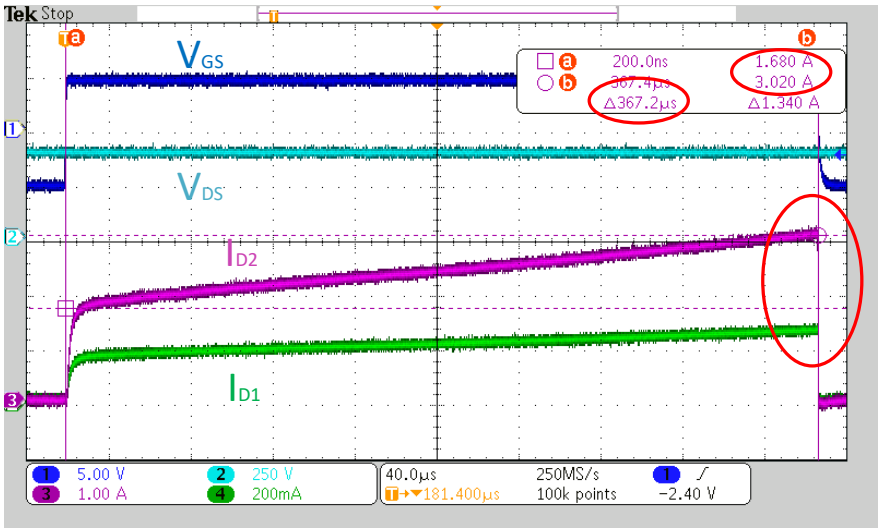


Figure 2.5 Long pulse saturation current sharing of paralleled Si CoolMOS™

Figure 2.5 to 2.7 shows the differences. The Fig. 2.5 shows the current sharing of paralleled Si CoolMOS^{TM} under long pulse self-heating. The saturation current will increase and the current differences between two paralleled MOSFET will become larger, which is dangerous for hiccup startup with multiple devices parallel. The other two devices are similar to Figure 2.5.

It is observed that both Si and SiC MOSFETs show increases current with a constant gate voltage when tested under saturation condition. This is primarily because the threshold voltage dependency on the temperature: V_{GS} decreases with increased temperature. Therefore, Neither Si nor SiC MOSFETs are good to limit inrush current during transient when they are required to operate in the saturation mode. However, it is noticeable that Si MOSFETs have a much stronger temperature dependency compared to the SiC MOSFET. At 175 ^{o}C, saturation currents in the Si MOSFETs have increased to 12-14 A compared to 0.5 A at 25 ^{o}C.

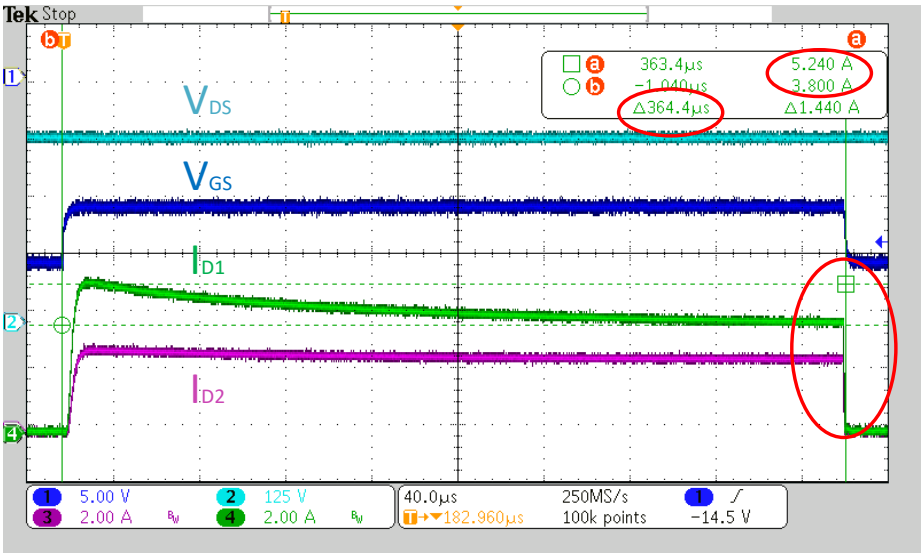


Figure 2.6 Long pulse saturation current sharing of paralleled SiC JFET

Figure 2.6 shows the current sharing of paralleled SiC JFET under long pulse self-heating. The saturation current will decrease and the current differences between two paralleled SiC JFET will become smaller. It is a very good feature for hiccup startup with multiple devices parallel. Fig. 2.7 shows the continuous pulses current sharing of SiC JFET.

On the contrary, the SiC JFET has shown negative temperature dependency of the saturation current, which is desirable for current sharing during hiccup startup operation in solid state circuit breakers.

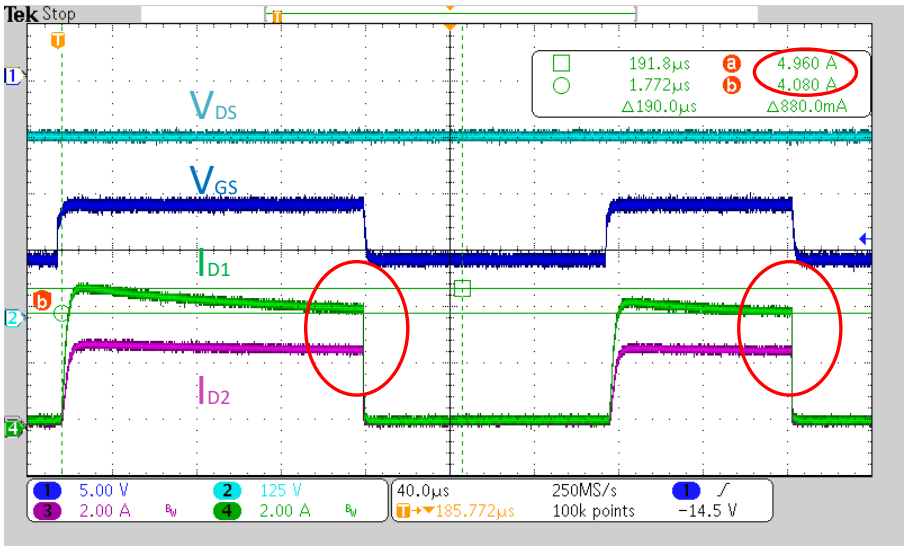


Figure 2.7 Multiple pulse saturation current sharing of paralleled SiC JFET

The SiC devices in candidates obviously have a wider temperature range for safe operation compare with Si devices. And the SiC JFET normally on characteristic consumes lowest driver power compare with other three voltage driven MOSFETs.

The concern for SiC JFET is also its normally-on characteristic. The circuit breaker should be better in OFF state if the grid is from powered off to recover. The standard related to 380V DC solid state circuit breaker application need to be further defined by the whole system.

2.3.2 Characteristics for branch circuit breaker

Different from above application, the paralleled single piece solid state device won't load current in branch circuit breaker during its normally-on status. All thermal related characteristics are also not important.

Generally, the most important characteristic of solid state devices for branch circuit breaker applications is the turn-off capability. It can be interpreted as the maximum current rating that the device can turn off. This section presents comparative test results on turn-off capability of listed candidate devices for branch circuit breaker application in the 380VDC delivery system. Turn-off capability of each device is evaluated and compared for the first time. It also mimics the turn-off condition of the main switch in a DC hybrid circuit breaker as shown in Figure 2.8. The hardware setup is displayed in Figure 2.9.

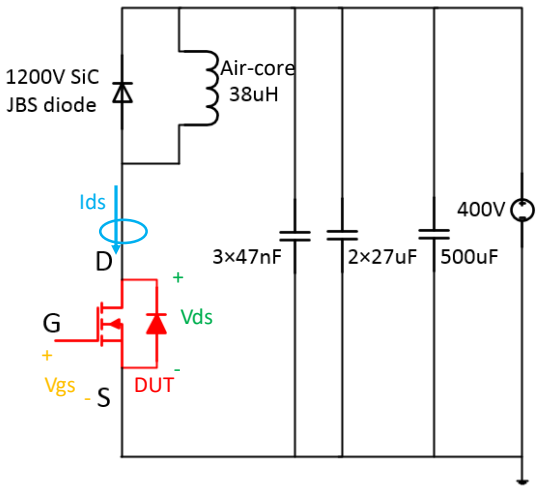


Figure 2.8 Long Pulse Test Circuit for high current turn-off capability under 400V DC bus

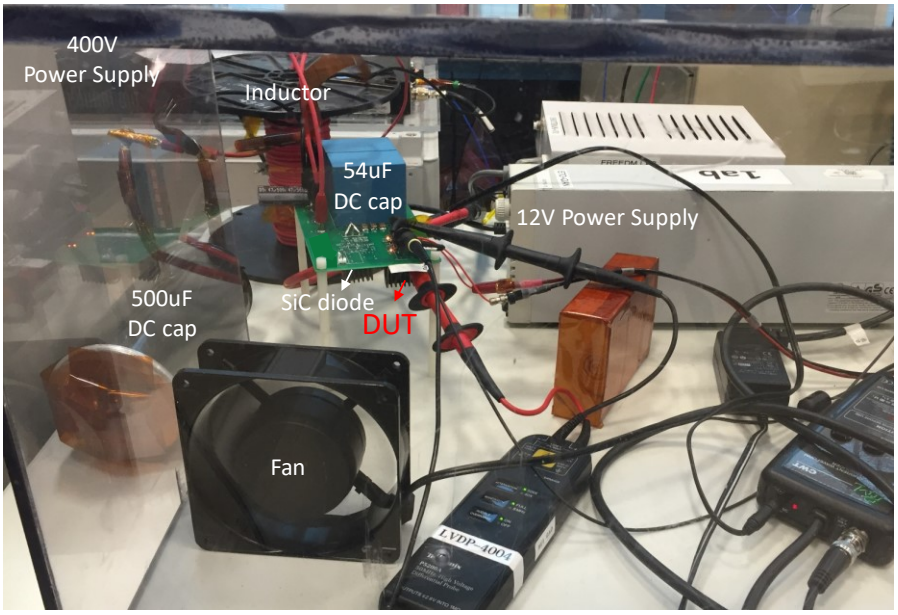
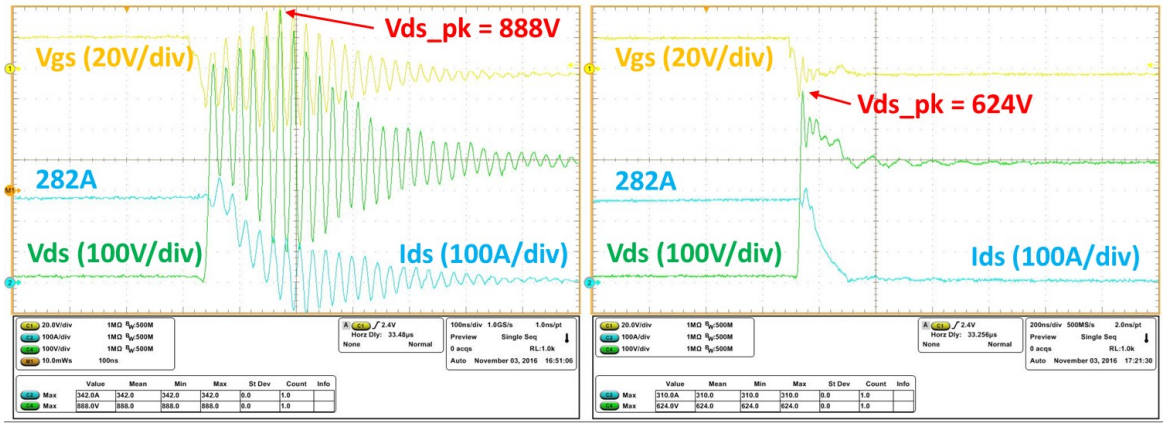


Figure 2.9 Hardware bench setup for high current saturation turn off test

All parameters, such as gate-to-source voltage (V_{GS}) and external gate resistance ($R_{G\_external}$) are selected according to the datasheet of each device based on their normal operation, shown in Table 2.5. One exception is Wolfspeed C2M0025120D. Based on its datasheet, $R_{G\_external}$ need to be 2.5Ω, but it results in large V_{DS} overshoot and ringing under high I_{DS}. Figure 2.10 shows the waveform of turn-off transient under 282A current, and V_{DS} overshoot reaches 888V. For safety consideration, $R_{G\_external}$ is increased to 5Ω, and its corresponding waveform shows that the V_{DS} overshoot is 624V with much less ringing.

Table 2.5 V_{GS} and $R_{G\_external}$ values for each device in long pulse test

Device	Vgs	Rg,ext
Si MOSFET	+10/-5V	5Ω
CoolMOS	+10/-5V	5Ω
SiC MOSFET	+20/-5V	5Ω
SiC JFET	+7/-13V	2.5Ω



Switching waveforms under $R_{g,ext}$ = 2.5Ω Switching waveforms under $R_{g,ext}$ = 5Ω

Figure 2.10 Switching waveforms of C2M0025120D under $R_{G\ external}$ = 2.5Ω and 5Ω

Figure 2.11-2.14 shows the test waveforms for 4 candidates in long pulse over current saturation test with 400V DC bus voltage. The comparison with die size, peak power density, and other characteristics is listed in table 2.6.

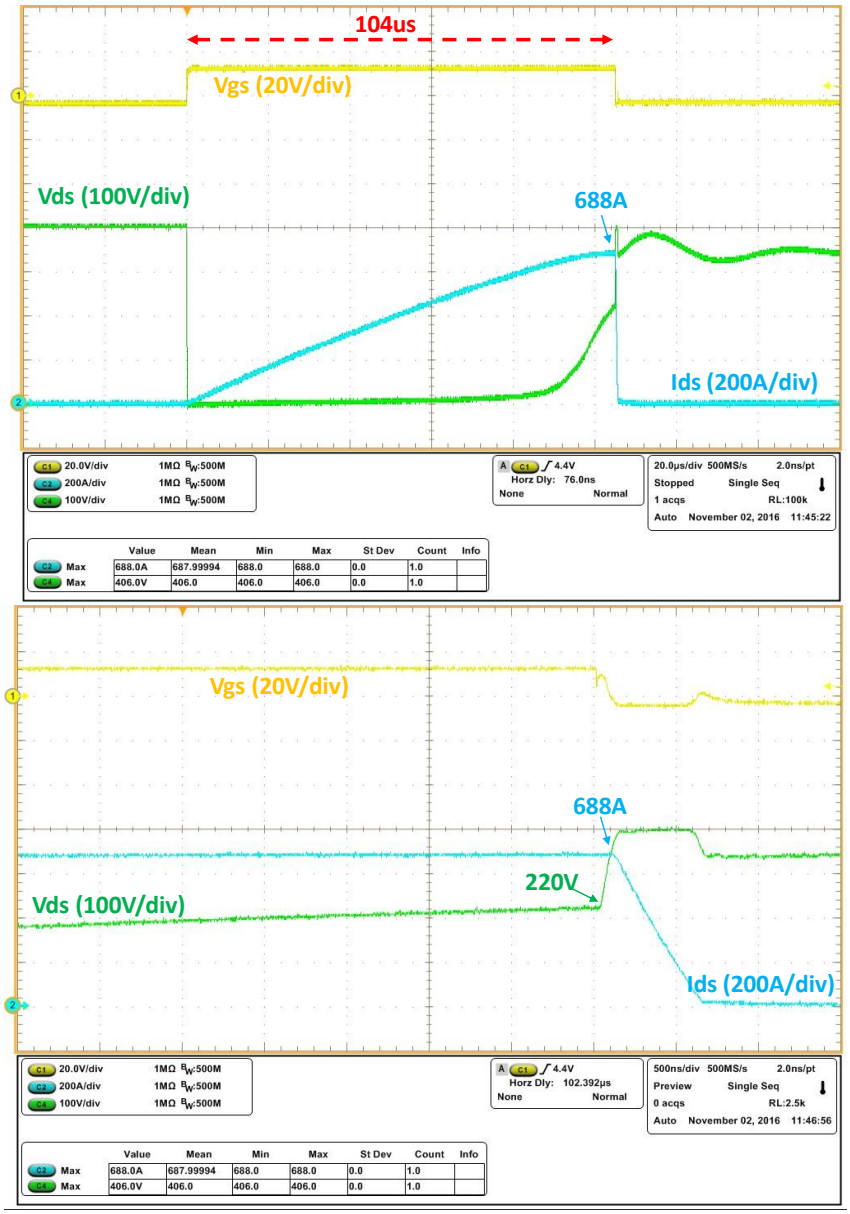


Figure 2.11 Test results of Si MOSFET STY145N65M5 in high current saturation turn off test

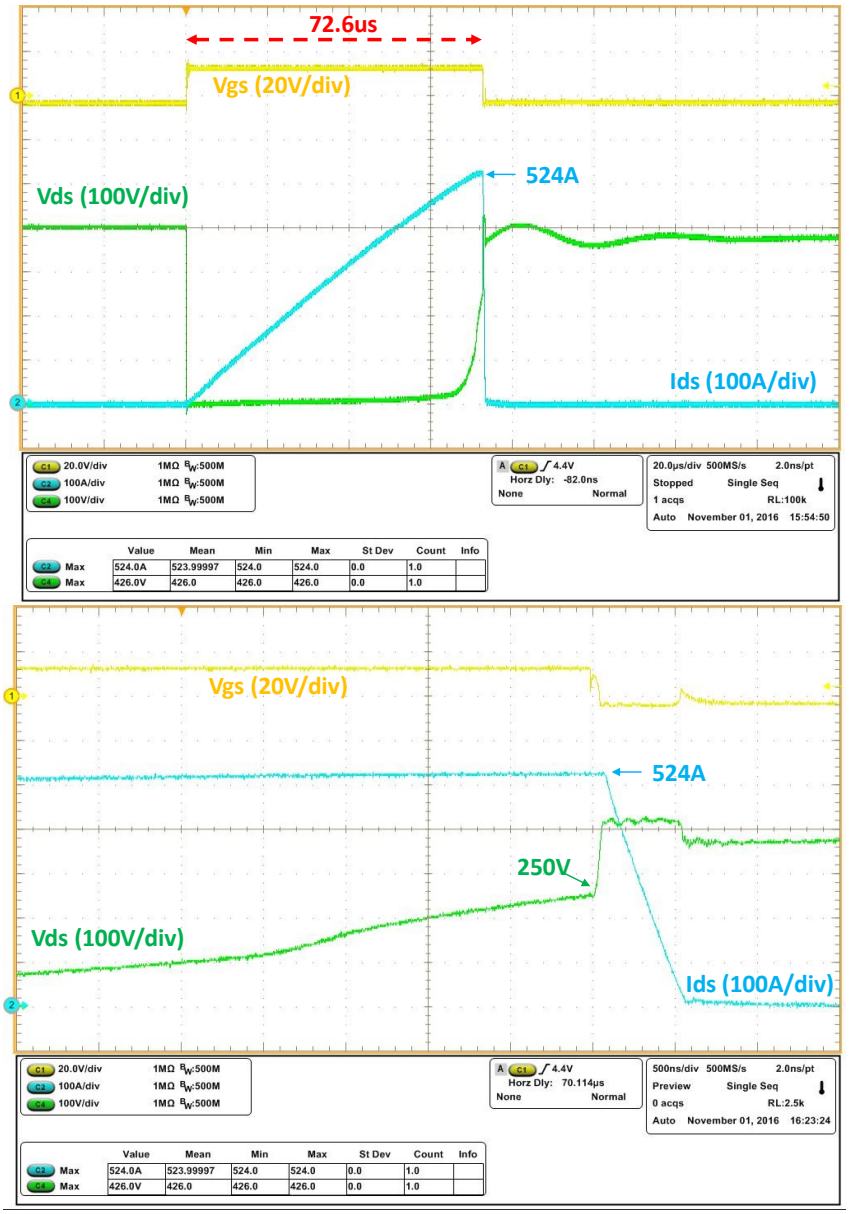


Figure 2.12 Test results of Si MOSFET IPW65R019C7 in high current saturation turn off test

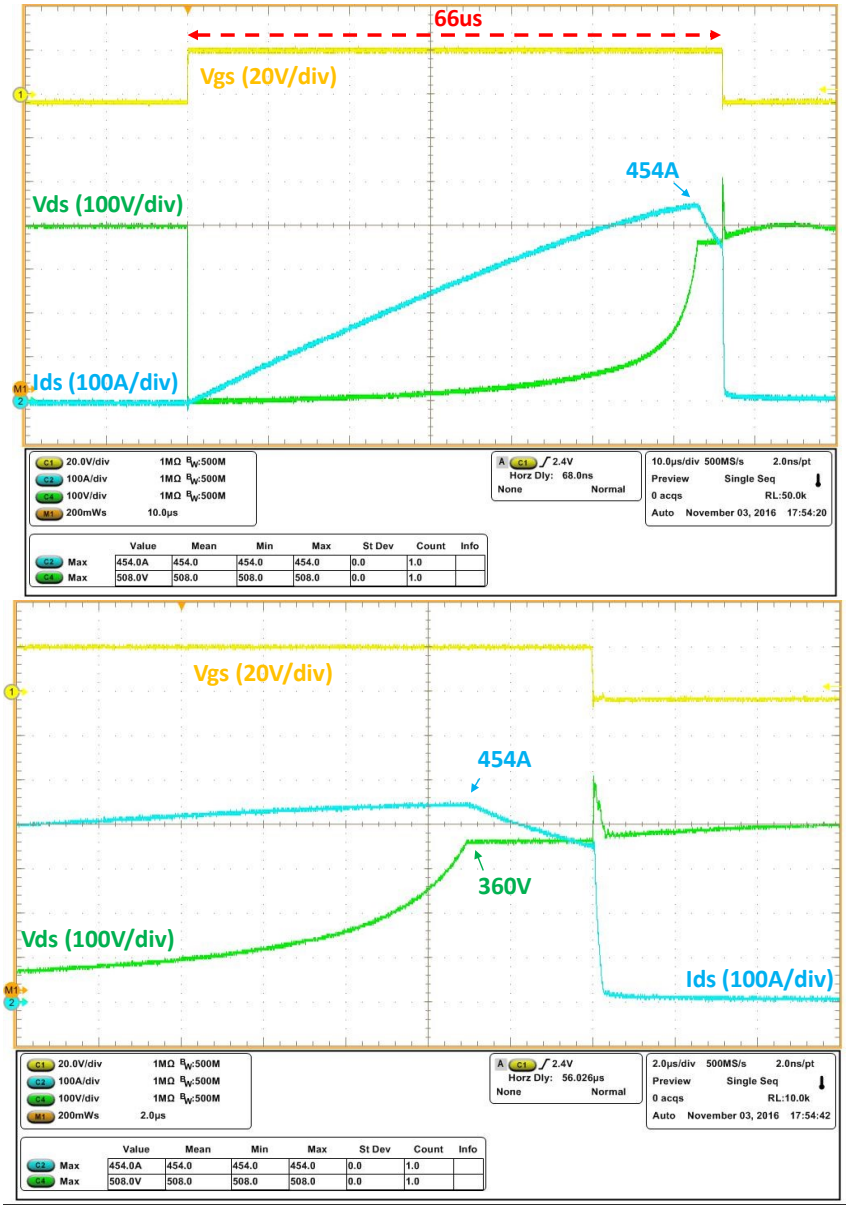


Figure 2.13 Test results of SiC MOSFET C2M0025120D in high current saturation turn off test

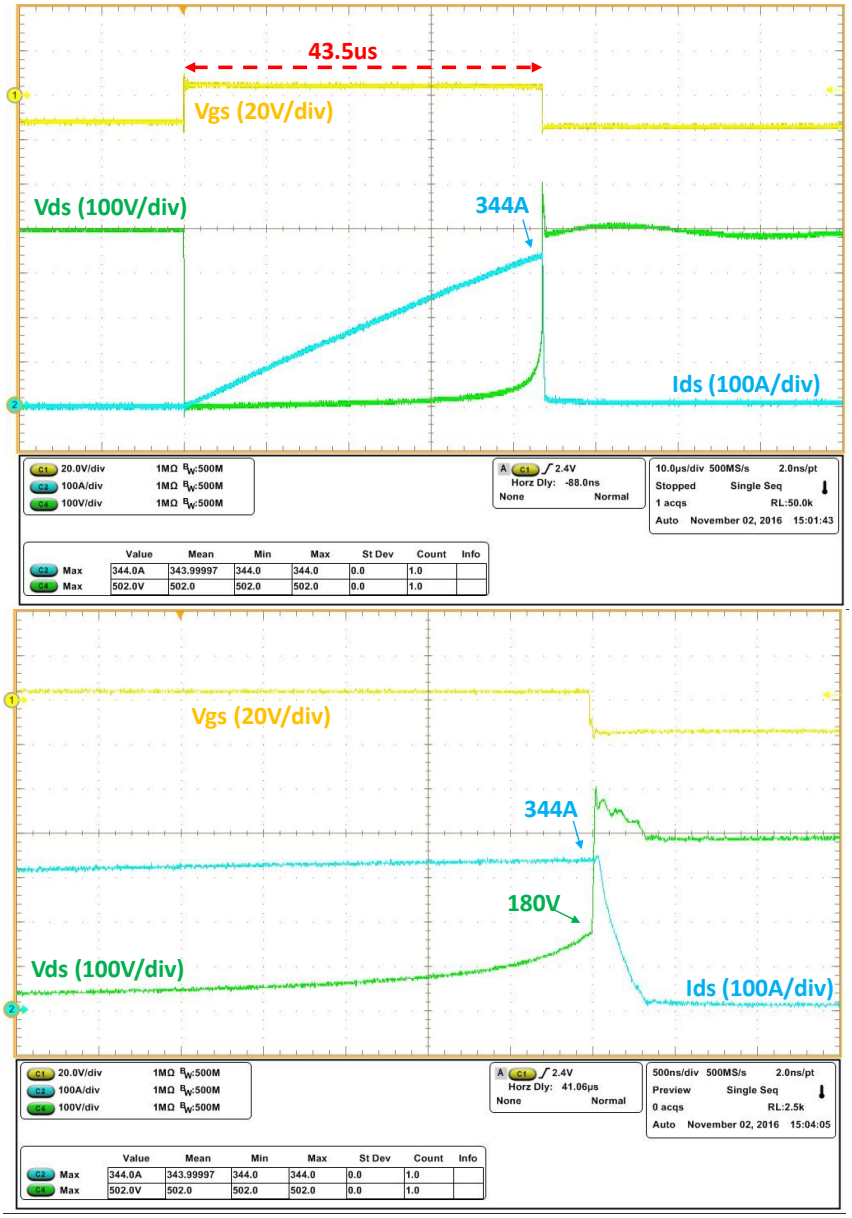


Figure 2.14 Test results of SiC JFET UJN1205K in high current saturation turn off test

Table 2.6 Characteristics of Solid State Devices for Long pulse turn-off test

Type	Manufacturer	Part No.	R_{DS}(on) @25 °C(mΩ)	Ioff(A)	Die Size (mm^2)	Ioff / A (A/mm^2)	Peak P density (VA/mm^2)
Si MOSFET	Infineon	IPW65R019C7	19	524	68.29	7.67325	2762.34
Si MOSFET	ST	STY145N65M5	14	688	121.88	5.6449	2032.16
SiC MOSFET	Wolfspeed	C2M0025120D	25	454	26.02	17.4481	6281.32
SiC JFET	USCi	UJN1205K	45	344	9.42	36.57804	13168.10

In comparison, similarly with $R_{DS(ON)}$, the high current turn-off capability is related to die size. Moreover, the SiC also is better than Si devices in I_{off} per area and Peak power density performance which has excluded the die size influence. In SiC devices, the SiC JFET is the best for characteristic needed for DC circuit breaker application. However, the naturally-on characteristic of SiC JFET needs the driver circuit to be carefully designed to have the breaker tripped off in a fault condition.

2.4 Conclusion and summary

In sum, the criteria of the characteristic for 380V DC circuit breaker is investigated and defined. Four devices are selected as candidates for 380V DC circuit breaker application. Comparison and evaluation of four devices have been analyzed and verified with experiment. The SiC devices perform much better and should be the best solution for DC circuit breaker application in future.

CHAPTER 3

Hot Swappable Outlet for 380V DC System

3.1 Introduction and Motivation

Power outlets and power strips are needed for both traditional 120V/220V AC distribution system and proposed 190V, 270V or 380V DC distribution system. In AC system, the plugs and sockets are mature and regulated with different voltage and current ratings in different countries, such as IEC 60906-1 standard in Europe and NEMA standard in North America. Because of the zero crossing point in each half cycle in AC system, the electrical arc is not a severe problem for 120V or 220V voltage rating. [46]–[49]

However, the electrical arc has become a significant issue in DC power system due to lack of zero crossing point. The arcing and related potential risks of fire and human touch is a primary safety concern in the DC application.

Besides, in DC power system, there are distributed bus capacitance both in the upstream and downstream, especially in DC/DC converter application. Although the distributed capacitance helps to reduce the voltage ripple and decouples the circuit network, the inrush current caused by this capacitance is also an issue during plugin which needs to be taken into consideration and solved properly.

In this chapter, the hardware is designed and implemented for DC outlet and socket application. It can control and limit the inrush current during plugin for startup and eliminate the arcing during unplug for safe disconnection.

3.2 State of Art DC Outlet

3.2.1 Saf-D-Grid® plug and receptacle

(a)

Electrical	
Voltage (AC/DC)	
• UL 1977 / CSA 22.2	600
• IEC	400
Current Rating (Amperes)	40
Wire Range (AWG)	#12 to #18
(mm²)	2.5 to 0.75
Hot Plug Rated	
• 250 cycles	400V @ 440A in-rush
• 250 cycles (UL)	400V @ 20A load
Dielectric Withstanding Voltage	3,300
Operating Temperature (°C)	-20° to 80°
(°F)	-4° to 176°
Fault Current Withstand	
UL 467	14 AWG, 300A, 4 Sec.

(b)

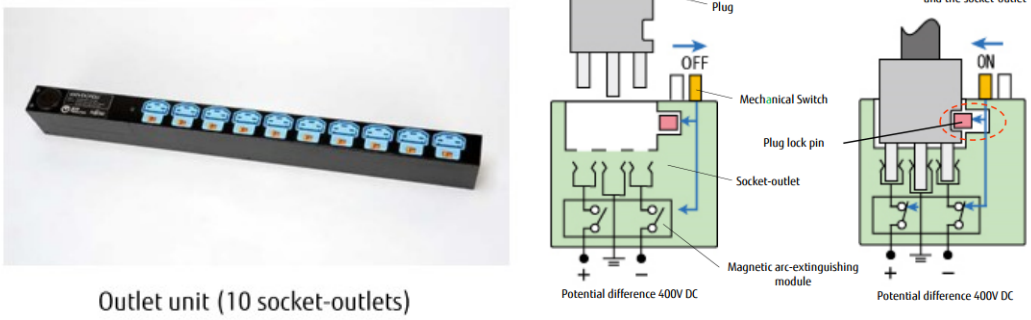
Figure 3.1 (a) Hardware configuration of Saf-D-Grid® Plug and Receptacle
(b) Specifications of Saf-D-Grid® Plug and Receptacle

Currently, there are several solutions and products designed for 380V and similar DC voltage rating. Figure 3.1 shows the hardware and specifications of a Saf-D-Grid® [49]from Anderson Power Products®. The DC voltage and current ratings are 400V and 40A. The design is still optimized only on mechanical design. The designed short receptacle and long plug with Hi Temp Nylon and Polycarbonate housings contain the arc whether connectors are mated or unmated while under load to minimize the risk to operators. The first mate, last break ground contact and integral latch features are considered to enhance the safety and reliability.

However, this design is still based on mechanical optimization so that the arc and sparks still exist to disrupt the contacts time after time. From figure 3.1 (b), 250 cycles is the lifetime of this plug and receptacle under 400V and 20A.

3.2.2 FUJITSU DC outlet

A DC outlet design from FUJITSU® is displayed in Figure 3.2.[50] The voltage and current ratings are 400V and 10A. Major differences between FUJITSU® design and previous Saf-D-Grid® is the sealed magnetic arc-extinguishing module and extra manual switch. The extra manual switch is employed to turn on and off the main circuit in the arc-extinguishing chamber with plug lock. A built-in permanent magnet in arc extinguishing module is used to breaks arc discharge during disconnection. This feature remarkably improves the lifetime to 5000 cycles, compared with the one in figure 3.2 (b). On one hand, it is the permanent magnet that reduces the arc effect and mitigates the welding on the contacts. On the other hand, the 10A current rating is also a reason of longer lifetime compared with 20A in Saf-f-Grid® receptacle.



(a)

Product name		10A-430V DC Socket-outlet for DC power distribution systems
Part number		FCN-961B003-G/1A
Configuration		First make, last break
Rated power	Current	Max. 10A
	Voltage	Max. 430V d.c
Initial contact resistance		50mΩ (1A-6V d.c)
Insulation (adjacent contacts)	Insulation resistance	Max. 5MΩ (1kV d.c)
	Dielectric strength	2500V d.c, 1min.
Inrush current		Max. 300A
Insertion/withdrawal life		5000 cycles
Electrical life (switch)	Rated power	5000 operations
	Inrush (300A)	500 operations
Initial switch operating force		Max. 35N(10mm/min)
Dimension (W × D × H) / Weight		41 × 41 × 49 mm/ 80g

(b)

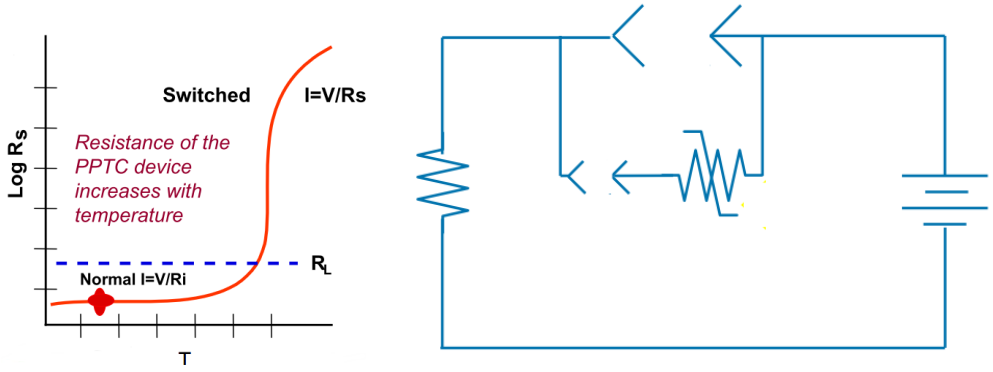
Figure 3.2 (a) Hardware configuration of FUJITSU® DC Outlet
(b) Specifications of FUJITSU® DC Outlet

3.2.3 PPTC solution from TE Connectivity®

Figure 3.3 gives PPTC solution from TE Connectivity®.[48] PPTC stands for Polymer Positive Temperature Coefficient materials. It is a blend of polymer and conductive particles which can create a network of conductive paths. The resistance of PPTC increases with temperature rise.

With such characteristics of PPTC, it is designed to be parallel with the main current path but with the first mate, last break connection. The current in PPTC heat itself to have current limiting capability. During unplugging, the PPTC reduce the final turn off current to shorten the arc between contacts into a safe region. Figure 3.3 (b) shows the comparison of tests results under 550V/20A DC.

Although no further data from reference, there are some issues with this design. The first problem in this design is that the current reduction in the PPTC depends on the temperature and time, therefore both the speed of unplug and the value of load current will have an influence on the result. Another issue lies in that although the high resistance can reduce the current value, the current still exists rather than zero. Consequently, the arc may still exist and will damage the contact.



(a)

(b)

Figure 3.3 (a) Characteristic of PPTC materials and circuit scheme
(b) Comparison of test under 550V / 20A DC

3.2.4 Proposal from Virginia Tech

In 2011, CPES proposed a DC plug and socket in its DC Nano grid system.[51] Figure 3.4 gives more details. The basic idea is to treat the circuit as a buck converter. Extra power pin is necessary for driving circuit. For turn on, increasing the duty cycle makes the output voltage increase from 0 to Vin. For turn off, decreasing the duty cycle makes the output voltage decrease from Vin to 0. Only ideal circuit is proposed and simulated. Too many contacts are needed and the driver scheme is complicated. And the inrush current is not considered with SOA of solid state devices.

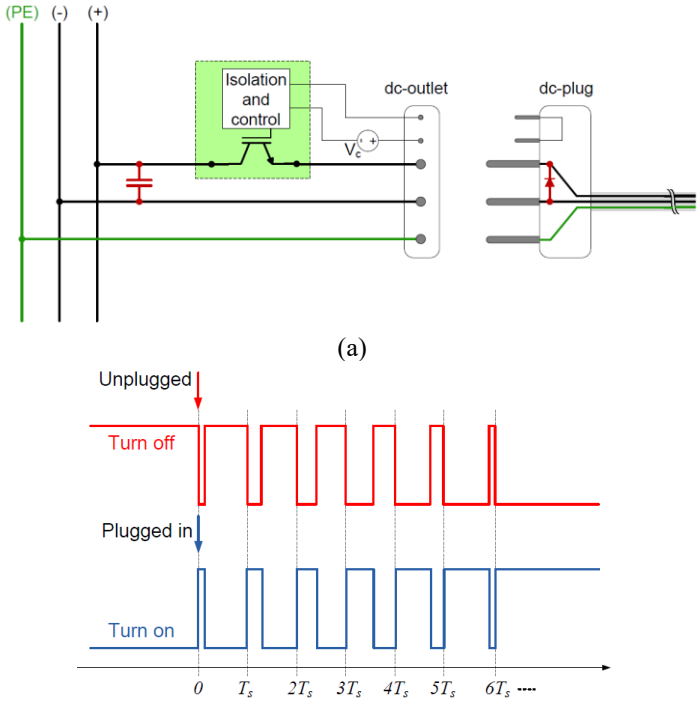
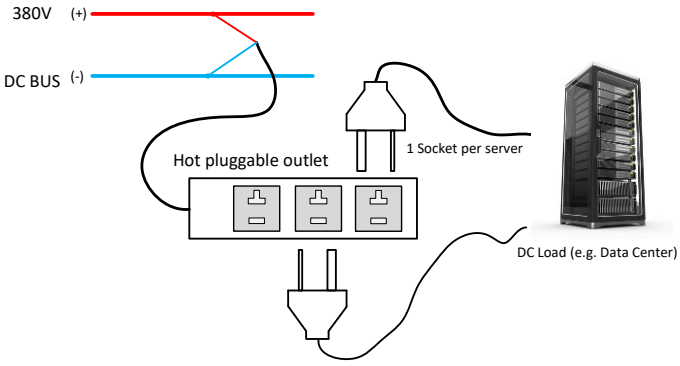


Figure 3.4 (a) Circuit topology of DC outlet
(b) Proposed control scheme

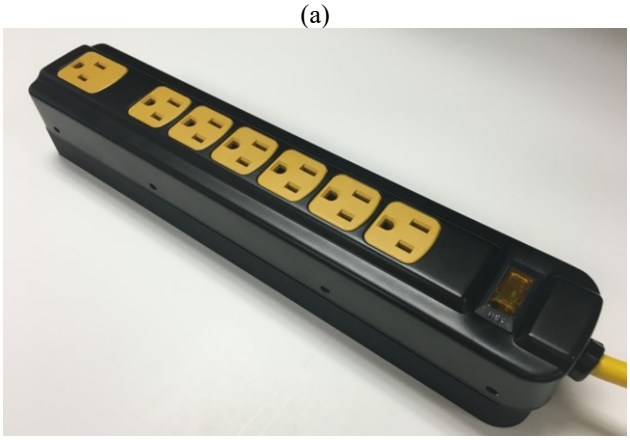
3.3 Design of Hot-Swappable Outlet

3.3.1 Circuit topology

The designed hot-swappable outlet is presented in Figure 3.5. Each socket is designed for 380V DC and 5A nominal current rating, which is about 2kW power rating. It covers most 2U to 4U power supply unit shown in Chapter 1. The earth wire is the default and ignored for showing more details in the diagram.



(a)



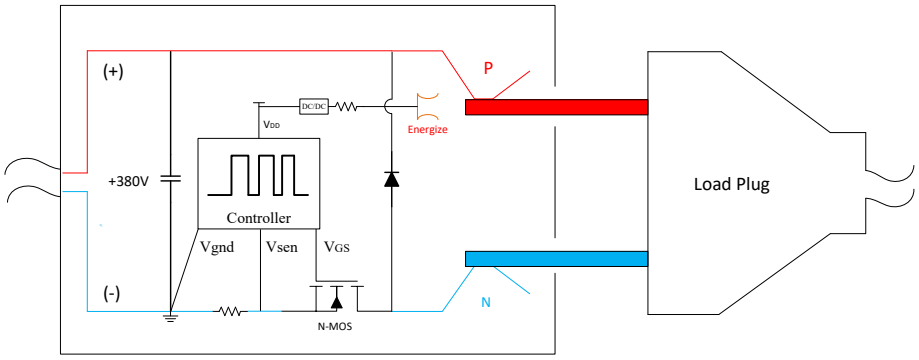
(b)

Figure 3.5 (a) DC hot swappable outlet
(b) Hardware of outlet

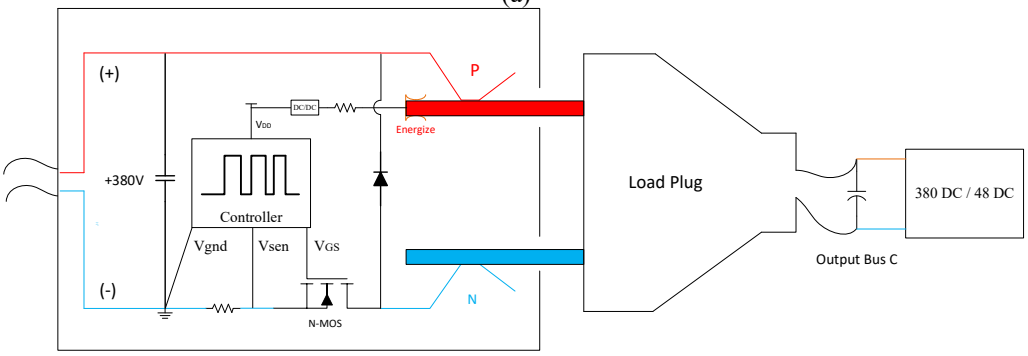
Two major challenges to realize in developing hot pluggable outlet with solid state device in DC distribution system are the inrush current caused by the output bus capacitance in DC/DC converter (shown as in Figure 3.6 (b)) at the time of plugin and the arc discharge at the time of unplugging. The inrush current acts as a short circuit current because the voltage across the capacitor is zero at the moment we plug the bus capacitance into the source. [46] The inrush current is higher if the capacitive load is bigger and as a consequence, will damage the embedded device. It has to be limited in the safe operation area (SOA) of MOSFET when designing and developing the hot-pluggable outlet. The undesired arc discharge phenomenon in DC distribution system will have detrimental effects on both equipment and human safety. It can be avoided by cutting off the current with the embedded solid-state device before disconnecting the main circuit.

One major advantage of the proposed design is that the plug is the same as traditional AC structure. They are both two poles for positive and negative, with one extra pole for the earth. The only requirement for DC is that the two poles should be designed clearly so that they are distinguishable and cannot be inserted in the opposite way. The third earth pole in traditional AC plug can help on this. Besides, NEMA 6-20 T slot is also an option for this purpose.

Given all aspects mentioned above, a zero-standby power, and hot-pluggable outlet is proposed, developed and tested[52]. One topology with an NMOS, power supply circuit, controller, driver and other passive components is shown in Figure 3.6. The PMOS type is also feasible to work with DC source with a similar principle. However, it is not cost-efficient and also low efficiency as device analysis shown in Chapter 2.



(a)



(b)

(c)

Figure 3.6 Topology and state (a) & state (b) of designed
hot swappable outlet with connected 380/48 V DC/DC load
(c) Hardware configuration of embedded hot swappable outlet circuit

3.3.2 Operation Modes Analysis for Hot Swappable Outlet

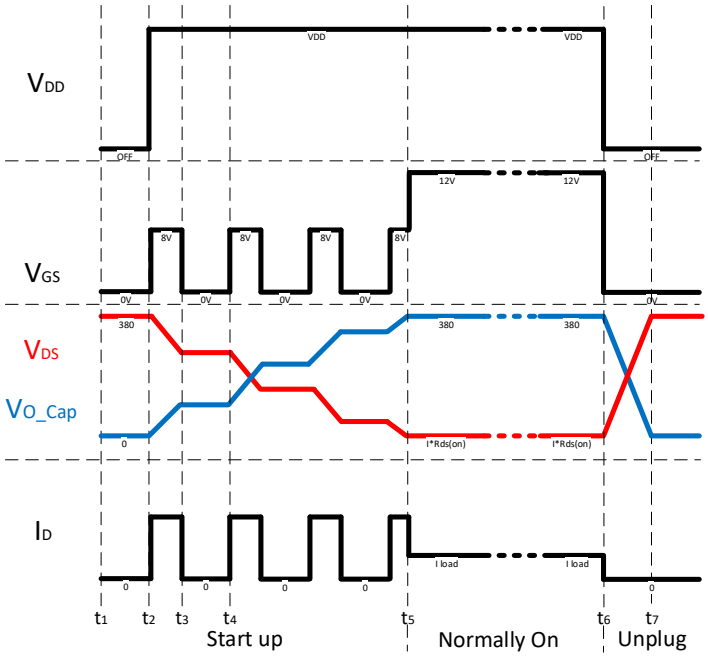


Figure 3.7 Operation modes of proposed outlet

The operation modes are demonstrated in Figure 3.7. They are the standby mode, startup mode, normally on mode and unplug mode.

Standby mode: Before t_1 and no load and plug, the whole circuit in the outlet is not powered since the energized pad is not connected. The NMOS is naturally open circuit because zero gate to source voltage. The power consumption in this mode is zero.

Startup mode: At the moment of t_1, the plug is in (a) position as in Figure 3.6. The drain to source voltage on NMOS is equal to 380V because the bus capacitor voltage is zero. The NMOS is still off with only leakage current (about 10uA). When the plug keeps inserting in, at the moment of t_2, the plug touches the energize pad at the bottom of the outlet (Figure3.6 b). The energize pad is connected to the Positive bus by the red male pin on the plug. The 10kΩ resistor inserted after the energize pad helps to limit the inrush current for a buck converter. The buck DC/DC power supply circuit starts to work and generates V_{DD} for the control circuit. The control circuit starts the designed hiccup startup and generates a low V_{GS} to make the NMOS work in saturation to limit the current within a short pulse (t_2-t_3). The output capacitor charges in this pulse and the voltage start to increase. The drain to source voltage on NMOS is still large which makes power stress large during the pulse within saturation. The pulse width and value of current need to be designed in the SOA of the device to avoid the failure of NMOS due to the large power dissipation. After the short pulse, the device is off again from t_3-t_4 for controlling the average power stress and dissipating thermal. The voltage on the device and capacitor remains no change in this period. These on-off hiccup control with adaptive V_{GS} repeat until the voltage on output capacitor closes to bus input voltage. The control circuit fully turns on the NMOS with 12V or even higher V_{GS} at the moment of t_5. Since the voltage difference is 0 and there is no inrush current, the load current determines the current instead of inrush current saturation.

Normally on mode: The plug remains in position b in Figure 3.6. And the NMOS keeps fully turn-on to get lowest $R_{DS(ON)}$ to reduce power loss on solid state device.

Unplug mode: The plug is unmated and separated from energizing pad and the V_{DD} becomes 0 at t_5. The NMOS is off. There is only leakage current going through the device. The voltage of output capacitor will keep decreasing because of the working converter load until UVLO occurs. The drain to source voltage on NMOS will increase. At the moment of t_7, the plug is fully unplugged with no arc because NMOS is off and only leakage current which is very small. There is also no inrush and arc for the energize pad as the total control circuit power consumption is only about 0.4W which is about 1mA steady state current consuming for 380V.

3.3.3 High Ratio Buck DC/DC Converter PSU

The Driver circuit is powered by a high ration buck DC/DC converter, which is shown in Figure 3.9. The size and footprint are only about 1.25-inch × 0.75-inch. It directly obtains power from energizing pad and negative bus. Input power is 380V and output power is 24V. Switching frequency is 60 kHz. The efficiency of this high ratio buck converter is only about 55% due to the extremely low duty cycle and light load operation.

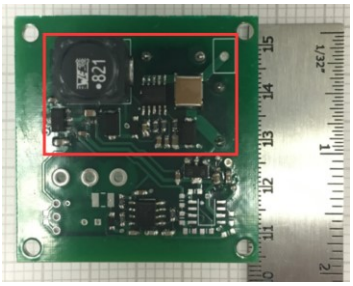


Figure 3.8 Buck converter for supply drive power

3.3.4 Dual Threshold Over Current Protection

Besides normal plugin and unplug features in the traditional outlet, the overcurrent protection on the negative bus can be also implemented at the same time which helps this outlet partially perform as a circuit breaker.

A dual threshold of overcurrent protection strategy is implemented by a controller to monitor over current or short fault. These two thresholds I_{Limit} and I_{SC} are adapted to trip the real over current fault and filter nuisance transient noises.

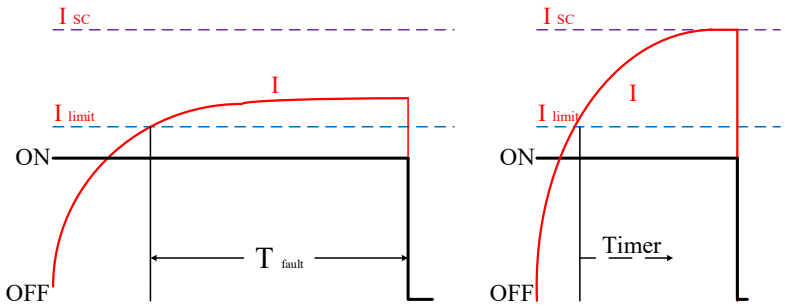


Figure 3.9 Dual thresholds off strategy for over current trip

I_{Limit} – Fault timer runs if $I_{Load}>I_{Limit}$ and the circuit breaker trip when the timer runs out of set up $T_{(fault)}$ which is usually been used to filter nuisance transient noises.

I_{SC} – Short circuit threshold (typically 1.3 to 2.5 times of I_{Limit}). I_{SC} current limiting feature before final 1-10 us instantaneous trip.

The trip time can be very fast with solid state device hardware protection.[35]

3.3.5 Over Temperature Protection

An over-temperature protection is designed to limit the inrush hiccup cycles. The threshold is set with margin to 125℃ as the transient junction temperature is not accurately monitored in hot swappable outlet. The accurate junction temperature is monitored in Chapter 4 with more analysis and experimental results.

3.4 Experimental Results of Hot-Swappable Outlet

Figure 3.10 displays the developed hardware. The NEMA 6-20 T slot is a good candidate can be adopted because it naturally tells the positive and negative bus with two different shapes and the peak of 240V AC is close to 380V DC rating. The embedded circuit is about 1.5-inch square with one TO-247 MOSFET.

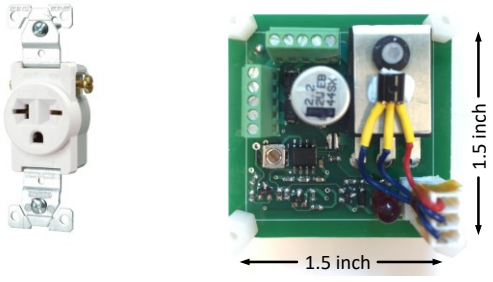


Figure 3.10 Hot pluggable outlet hardware

Figure 3.11 shows the waveforms from t_1 to t_5. The circuit spends about 3ms to start the startup mode after the energize pad get 380V.

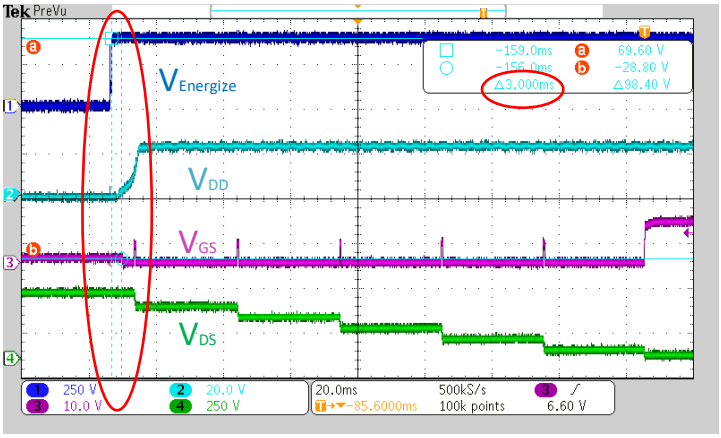


Figure 3.11 Plug in process waveforms of DC hot pluggable outlet

Figure 3.12 presents the full waveform of hiccup startup mode. The inrush current is limited as about 9A as I_D. The V_{GS} is controlled for saturation to charge the output capacitor. The 47uF capacitor on output side takes about 70ms to be charged to 380V. This value can be programmed as long as the power stress of MOSFET is under SOA.

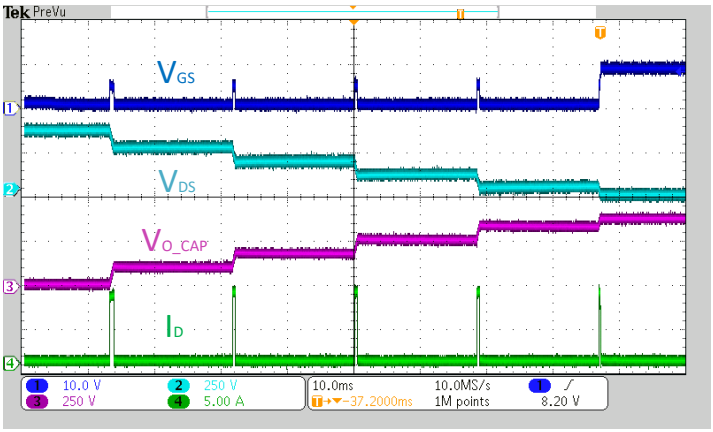


Figure 3.12 Hiccup startup process waveforms of DC hot pluggable outlet

Figure 3.13 shows the thermal image in the steady state of 380V 5A normally on mode. The power loss is about 1W on this device with 33mohm $R_{DS(on)}$ and the hot spot is about 60.5℃ on the thermal pad.

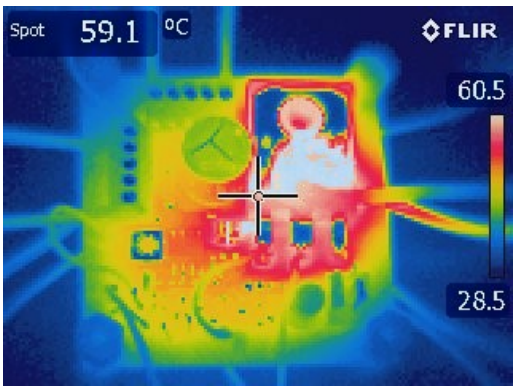


Figure 3.13 Normally on Steady state thermal image

Figure 3.14 shows the unplugging mode. After the energize pad disconnecting, it takes 56ms to fully power off the control circuit and turn off the MOSFET. This value can be reduced by decreasing the capacitance in power supply circuit.

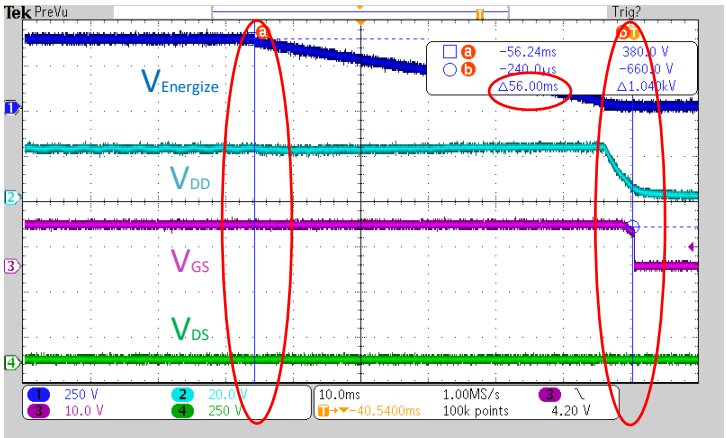


Figure 3.14 Unplug process waveforms of DC hot pluggable outlet

Figure 3.15 shows the waveforms of dual threshold overcurrent protection. From waveforms, we can find that once the sensed current is over $I_{threshold}$ (=5.2A), the controller will trip the circuit after the preset t_{fault} (=680us) timer. Once the controller decides to trip, the circuit only spends about 1us to finish this process like an instantaneous trip.

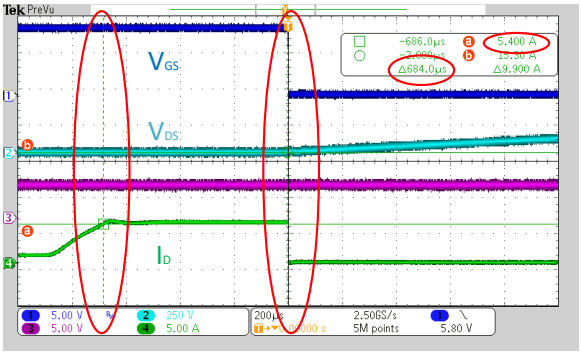


Figure 3.15 Lower threshold with timer over current protection waveforms of DC hot pluggable outlet

Figure 3.16 shows the instantaneous threshold trip with high current.

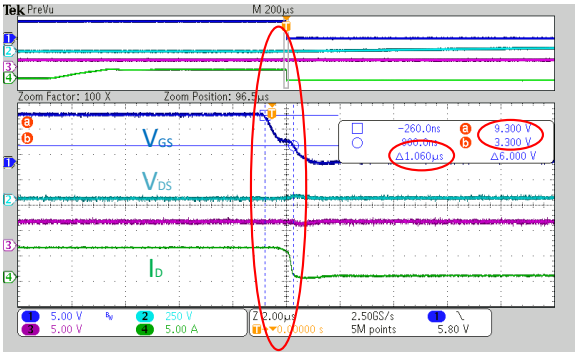


Figure 3.16 instantaneous over current protection waveforms of DC hot pluggable outlet

Figure 3.17 gives the waveforms of over temperature protection. From waveforms, we can find that once the sensed temperature reaches 100℃ (1.23V from Vo of sensor), the circuit will be tripped by the controller in about 1.68 us.

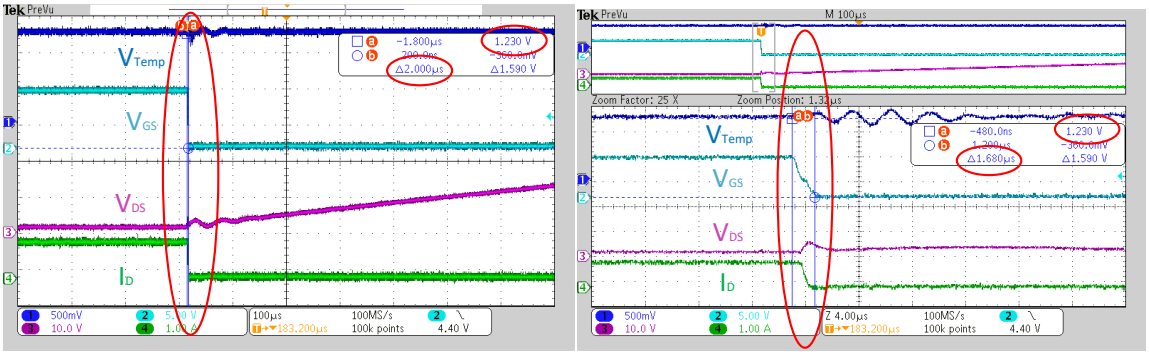


Figure 3.17 Over temperature protection waveforms of DC hot pluggable outlet

3.5 Conclusion and Summary

In sum, a hot-pluggable outlet is proposed and developed for 380V DC distribution system. There are several novel and useful features as follows:

1. The standby power of the outlet is zero because there is no drive power needed and gate voltage can be naturally pulled down to 0V to turn off the embedded MOSFET. The input power for buck converter is zero since the energize pad is not connected during standby.

2. The mechanical structure is novel and simple. The energize pad which is designed at the bottom of the socket makes the plug compatible with traditional 3 pole system (one is earth). Only one pole is used to shorten the positive bus and energize pad. Meanwhile, the bottom energizing pad naturally implements “the last energize, first de-energize” for protecting and safety of device and operator. The similar mechanical structure can be optimized to replace a simple pad as long as the contact sequence is same.
3. The embedded solid-state device helps to limit the inrush current and eliminate the arc with low power consumption. The total power loss from the control circuit and MOSFET are about 1.4W under 380V, 5A which is about a 2kW load.
4. The dual threshold current trip can be realized because of the embedded MOSFET. It notably helps in preventing short circuit and other faults in DC downstream.
5. Under voltage lockout on input bus voltage is designed for isolating the downstream load from the bus for protecting both bus voltage on upstream and load on downstream.
6. Over-temperature protection is designed and embedded for protecting the solid-state device within the thermal limit.

The proposed hot-swappable outlet is designed, analyzed and tested under various scenarios which is a good solution for 380V DC distribution system. Besides, it is worth noticing that the zero-standby power, dual threshold current trip, UVLO and OTP are all excellent advantages and features in DC system.

CHAPTER 4

Solid State Circuit Breaker for 380V DC System

4.1 Introduction and Motivation

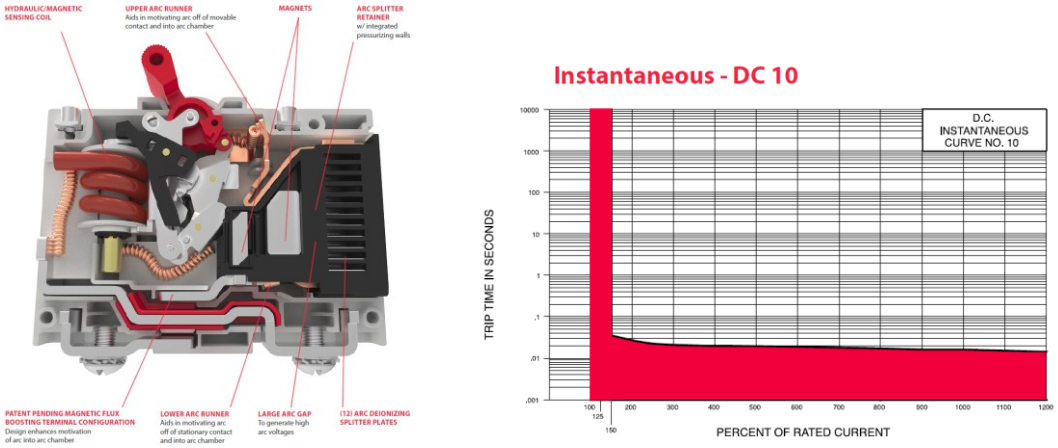
As stated in Chapter 1 and 2, the circuit breaker is a mandatory component and has a significantly vital position in 380V DC power system. The mechanical circuit breaker and fuses are still being used in DC system protection nowadays. The problem of this kind of circuit breaker is the trip speed cannot meet the requirement of system protection in DC system. The trip current threshold is too large compared with the nominal current rating and the speed is almost above 10ms. Another challenge is the arc during contacts breaking in DC system, which limits the lifetime of the mechanical circuit breaker.

Recently, researchers are putting a lot emphasize on investigating on solid state circuit breakers for DC system. One important reason is the performance improvement brought by SiC devices. Moreover, both speed and arc can be avoided by utilizing solid state devices. The only obstacle is that the leakage current (~10uA) of solid state devices cannot supply a physical isolation compared with a mechanical switch.

In this chapter, a solid-state circuit breaker with paralleled devices is proposed, designed and analyzed. The interleaved startup strategy is introduced to improve the thermal stress sharing for reducing the system unreliability. It is also a benefit for enhancing the speed of startup. Additionally, a novel real-time junction temperature monitoring strategy is proposed, analyzed and tested for protecting the embedded solid-state device.

4.2 State of Art DC Circuit Breaker

4.2.1 CX-series DC circuit breakers



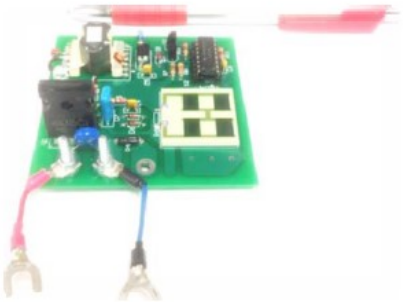
(a) (b)

Figure 4.1 (a) Hardware configuration of CX-series DC circuit breaker
(b) Trip time curve of CX-series DC circuit breaker

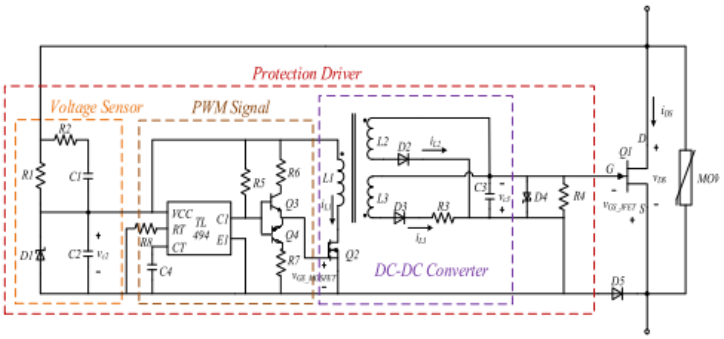
Figure 4.1 shows the latest Hydraulic/Magnetic Circuit Breaker designed specifically for 380V DC system[53]. It has been optimized mainly for solving the arc issue in DC system. Permanent magnets combined with the upper and lower arc runner increase the magnetic blow out force and aid in motivating the arc off of the contacts and into the arc chamber. The arc chamber features arc splitter retainers with integrated pressurizing walls, which facilitates heat transfer from the arc providing additional cooling and allowing quick transition into the magnetically induced by splitter plates. [53]

The optimized arc extenuating system in CX-series reduces the influence of arc during the break and improves the lifetime of the mechanical circuit breaker to 4000-6000 cycles. However, the trip speed is still a concern due to natural characteristics of the mechanical switch. From figure 4.1 (b), the fastest trip speed for 150% current rating is still around 1ms and up to 40 ms with uncertainty.

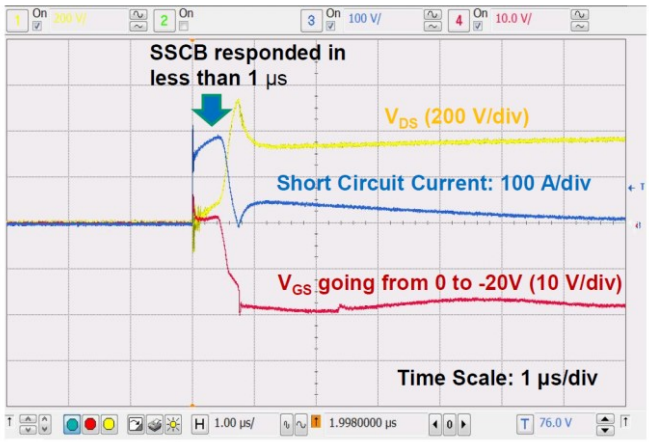
4.2.2 Ultrafast autonomous SiC JFET circuit breaker



(a)



(b)



(c)

Figure 4.2 (a) Hardware of Autonomous SiC JFET circuit breaker
(b) Circuit schematic configuration
(c) Short circuit waveforms of self-powered SiC JFET SSCB

Figure 4.2 shows a self-powered circuit breaker with SiC JFET.[54] As described in Chapter 2, the SiC JFET is very competitive because of its large short circuit current capability and negative temperature coefficient. In the current design, the author utilizes the voltage drop on the device for large fault current (>100A). The 4.5V voltage drop (45mOhm $R_{DS(ON)}$) is used to provide a voltage supply for the local isolated driver circuit to generate a negative V_{GS} to turn off the normally on SiC JFET. This period could be very fast and less than 1us.

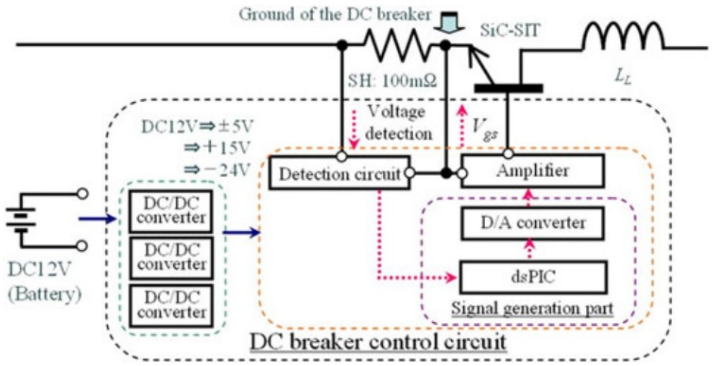
The self-power is the most appealing and innovative feature of this paper. The drive circuit needs no power for the normal operation because of the normally on SiC JFET.

However, the self-power needs two latent premises. The multiplication of the $R_{DS(ON)}$ and threshold current need to be large enough to energize the drive circuit. But for products in the real world, both two parameters are the smaller the better.

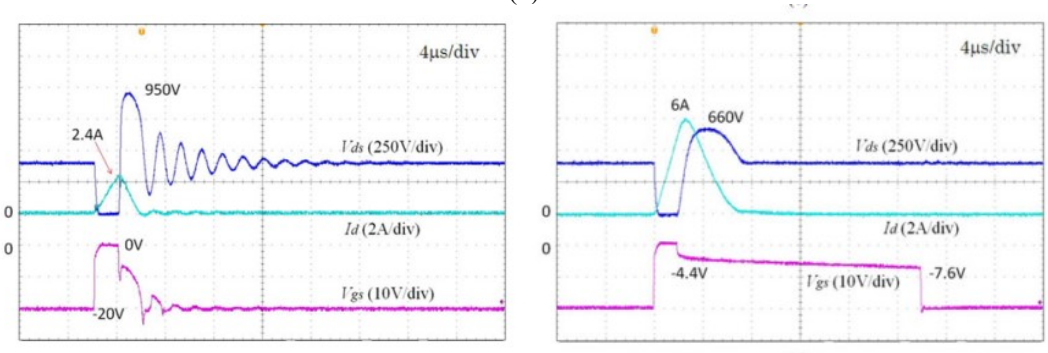
Besides, the large turn-off current causes over voltage spike even with local snubber circuit and MOV in this paper. About 570V drain to source voltage is shown in figure 4.2 (c) for 380V/100A application. Although this is acceptable for 1200V SiC JFET, it should also be accounted for 600V devices in the future. The last issue for this design is the startup is totally neglected for normally on SiC JFET. As analyzed in previous chapters, the inrush circuit could damage the device without control due to the large drain to source voltage. Since the power is self-powered by the overcurrent and no drive power consumption during normally on, the start-up of this circuit will damage the device in real-world DC application.

4.2.3 400V DC SiC-SIT circuit breaker by NTT Japan

(a) Dimension of SiC-SIT CB: 45 mm(W) 100 mm(H) and 370 mm(D)



(b)



(c)

Figure 4.3 (a) Hardware of SiC-SIT NTT DC circuit breaker
(b) Circuit schematic configuration
(c) Experimental waveforms comparison of original and proposed gate voltage

In figure 4.3, a SiC-SIT DC circuit breaker developed by Chiba University and NTT Japan is displayed.[55] The power rating is 400V/12.5A. The most important feature is the programmed slope gate drive voltage for suppressing the overvoltage on V_{DS} during turn-off. Without local snubber circuit, the overvoltage spike can be 950V for only 2.4A turn-off due to large line inductance. With proposed slope gate drive voltage, this overvoltage can be remarkably reduced to 660V with 6A turn-off current and 140uH line inductance. As a result, the price is the increased turn-off speed which is approximate to 22uS.

There are three issues with this design. Firstly, lacking local freewheeling diode and input capacitor makes the device far away from its current turn-off capability. This also sacrifices the trip speed for the low V_{DS} spike. Secondly, extra 12V DC battery is required for supplying the power. At last, the power density of prototype is only $3W/cm^3$.

4.3 Hardware Design and Analysis

4.3.1 Circuit topology

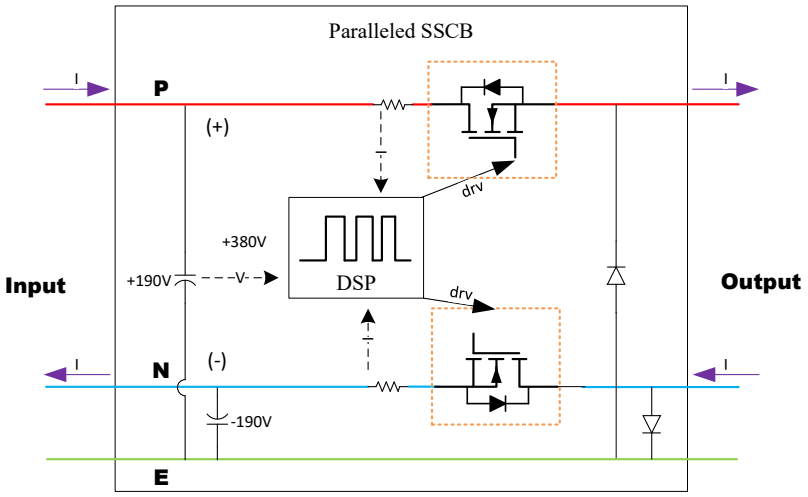


Figure 4.4 Circuit topology of proposed solid state circuit breaker

The main circuit of the designed solid-state circuit breaker for 3 wire 2 phase 380V DC system is shown in figure 4.4.

1. Two paralleled solid-state device modules are located on positive and negative buses for limiting and tripping the current flow.
2. A µController is embedded to control the circuit and make all parameters programmable.
3. Input capacitors and freewheeling diode on the output side is designed to minimize V_{DS} spike.

4. The operation modes are similar to the one in Chapter 3 with inrush startup, normal operation, and dual current thresholds trip.

4.3.2 Interleaved hiccup startup with inrush current strategy

As demonstrated in Chapter 2, most solid-state devices have a positive feedback on saturation current and junction temperature. During paralleled operation, this characteristic will make the saturation current diverge under same gate voltage. The device with the largest saturation current at the beginning will fail in a short period although all other devices are still under low thermal stress.

In order to solve this issue, an interleaved hiccup startup strategy is proposed to share the thermal stress among all paralleled devices. Figure 4.5 gives the details.

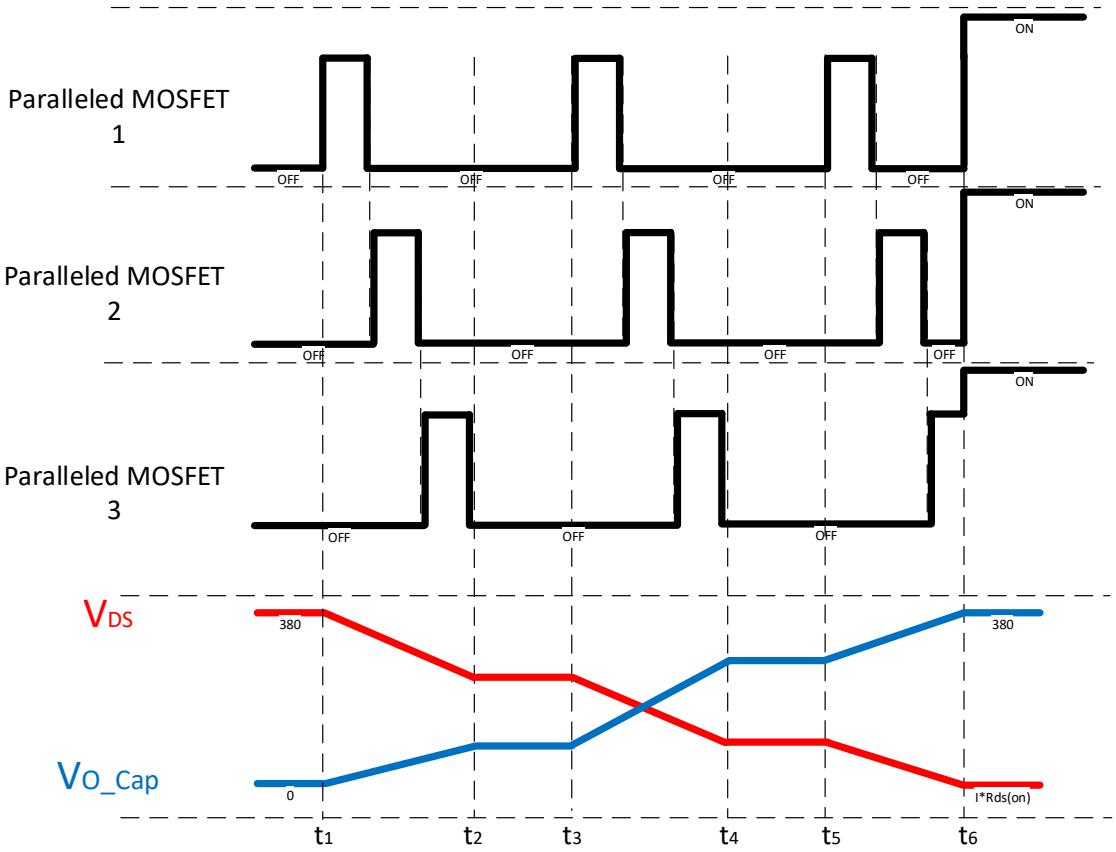


Figure 4.5 Interleaved hiccup startup strategy for multi-channel solid state devices

t_1 - t_2: The whole circuit starts the startup process with saturation current limitation. The paralleled solid-state devices work under saturation mode with closed-loop control till t_2. The output voltage keeps rising due to the limited saturation inrush current. This makes the drain to source voltage on paralleled devices keeps decreasing.

$t_2 – t_3$: All devices are fully turned off because every device is still in cooling mode due to large thermal stress come with saturation pulse. This period is the shorter the better, although still limited by thermal limitation. Both voltages keep the same value as only leakage current exists.

$t_3 – t_4$: Interleaved saturation pulses start to repeat again because the cooling mode ends for the first device. It is the repeat stage of t_1 - t_2.

$t_4 – t_5$: All devices are fully turned off because all of them are in cooling mode. It is also the repeat stage of t_1 - t_2.

$t_5 – t_6$: The interleaved startup repeats again and again until the output voltage reaches input bus voltage. All devices are fully turned-on with high V_{GS} because the saturation mode is no more needed and the V_{DS} is already equal to $I_D \times R_{DS(ON)}$

This strategy is simple and safe for multichannel paralleled solid devices. Each device can use a separate cooling mode to have enough cooling time. Only one DAC channel is equipped with a multiplexer as there is no voltage step between drive voltage of devices.

4.3.3 Transient and steady-state real-time junction temperature monitoring

In this design, the junction temperature of solid state devices changes in a large range during inrush startup. And for most of the operation period, the normally on operation is the dominant mode. One major reason fails the solid-state devices is the thermal stress. So, the reliability of device could be significantly enhanced if the junction temperature is monitored accurately.

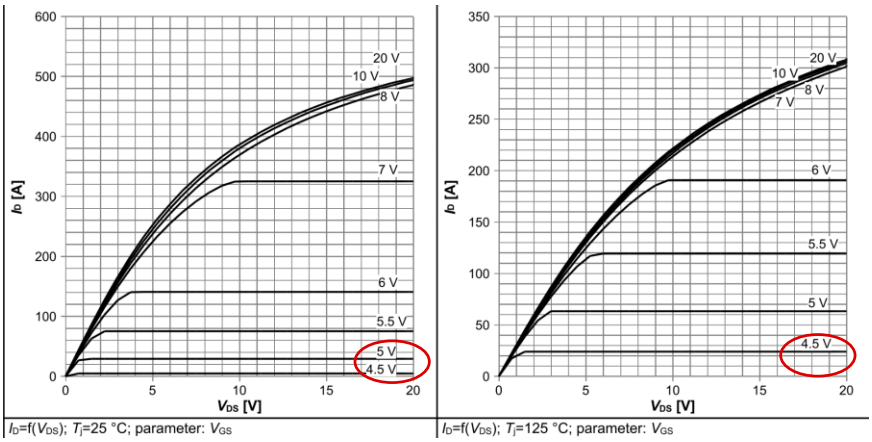


Figure 4.6 Interleaved hiccup startup strategy for multi-channel solid state devices

Figure 4.6 exhibits the saturation curves of the same IPW65R019C7 from Infineon CoolMOS^{TM}. All other devices have a similar characteristic with the exception of the SiC JFET being on opposite trend, which is introduced in Chapter 2.

From this figure, it is evident that the saturation current is associated with the junction temperature, gate voltage V_{GS} and drain to source voltage V_{DS}.

$$I_D = f(T_J, V_{GS}, V_{DS}) \tag{4.1}$$

Obviously, the junction temperature can also be derived as:

$$T_J = f(I_D, V_{GS}, V_{DS}) \tag{4.2}$$

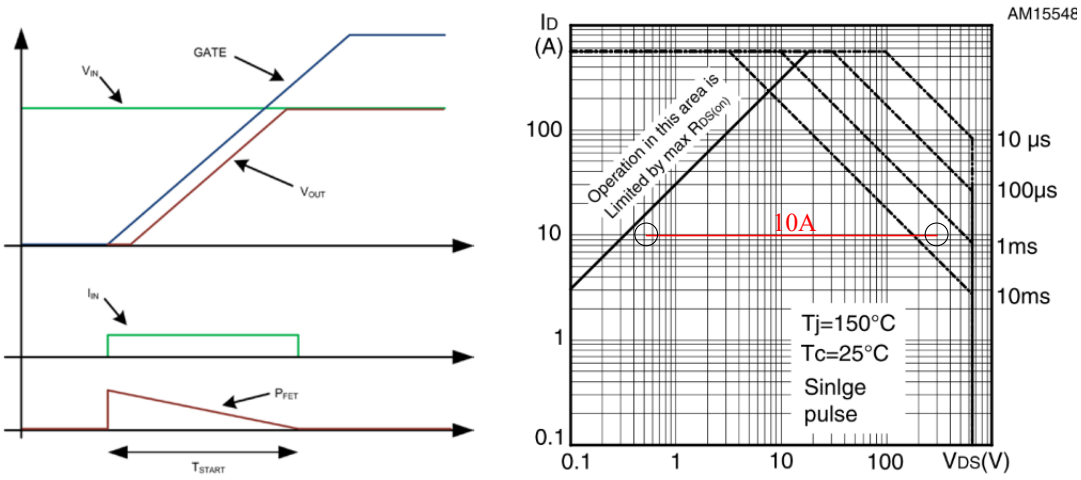


Figure 4.7 Constant ID startup with close loop control strategy

Once constant I startup is utilized within designed SOA, there is one parameter which can be neglected, making equations 4.2 to 4.3.

$$T_J = f(V_{GS}, V_{DS}) \tag{4.3}$$

This is the key equation be used for realizing transient state real-time junction temperature monitoring. More analysis and verification of test results will be shown in section 4.4.

For steady state, one important parameter $R_{DS(ON)}$ helps us to monitor junction temperature, which is widely used to sense I_D in other applications. Figure 4.9 shows such characteristic.

In figure 4.8, the low temperature-coefficient sensing resistor is designed and applied to sense the drain current. Once the accurate I_D is known, the V_{DS} can be measured to calculate the $R_{DS(ON)}$ and then the junction temperature during steady state is obtained.

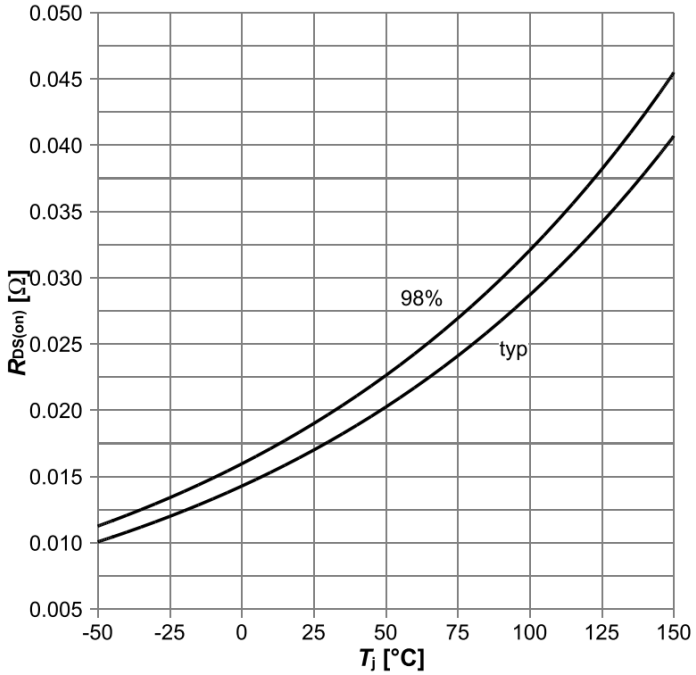


Figure 4.8 $R_{DS(ON)}$ vs. junction temperature

4.3.4 High impedance fault protection

The high impedance fault is a challenge for system protection. It is always treated as regular load by circuit breaker which usually causes a fire hazard with high impedance inflammable hazardous material.

Thanks to the symmetrical 3 wires 2 phase circuit breaker design, the high impedance fault between positive and ground, negative and ground can be sensed and protected as a result of the unbalanced line currents on positive and negative buses.

4.4 Experimental Results of Solid State Circuit Breaker

4.4.1 Hardware design

As mentioned above, 4 paralleled solid-state devices are composed to share the large line current. Figure 4.9 shows the picture of developed solid state circuit breaker hardware and its size.

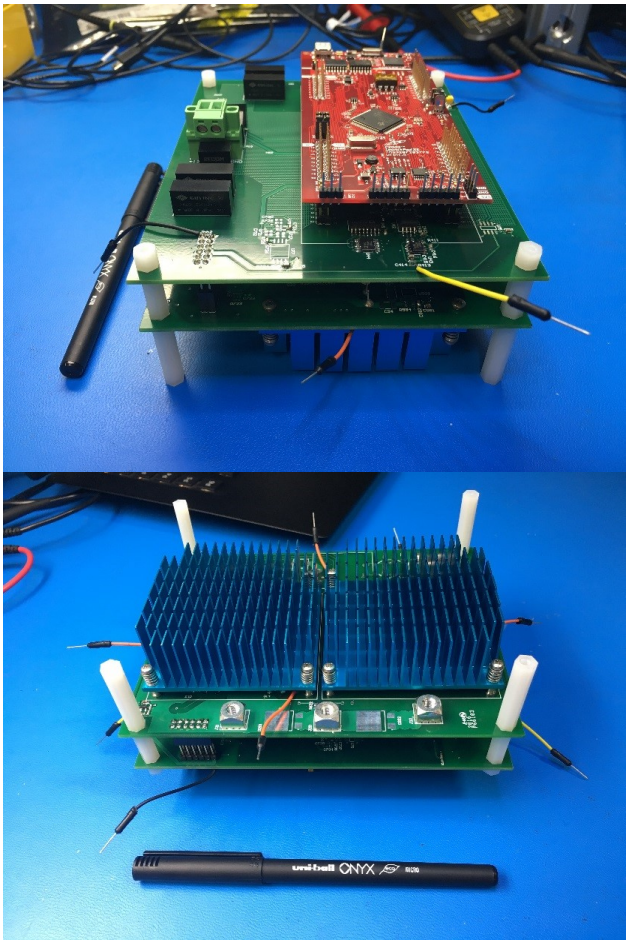


Figure 4.9 Hardware of solid state circuit breaker (140 mm × 110 mm × 40 mm)

Each device is equipped with its own input snubber capacitor, output freewheeling diode, current sensor and driver circuit which make them a single module and easy to scale up.

The power density is about 20W/cm^3 for 380V (±190V) and will be larger when applied with ±380V.

4.4.2 Interleaved hiccup startup with inrush current strategy

The hardware of solid state circuit breaker has been developed with 2 groups of paralleled MOSFET to share specified current to reduce the thermal stress under steady state. However, as analyzed in 4.3.2 and Chapter 2, the inrush current need to be considered with interleaved hiccup strategy due to the positive temperature coefficient during transient current sharing.

In figure 4.10, an interleaved hiccup startup for 190V positive DC bus with 100uF capacitive load and 10A constant current closed-loop control is shown. In each group, 4 devices are closed-loop controlled with constant 10A as figure 4.7.

5 Groups of hiccup pulses have been applied to charge the 100uF capacitor to 190V within 41ms.

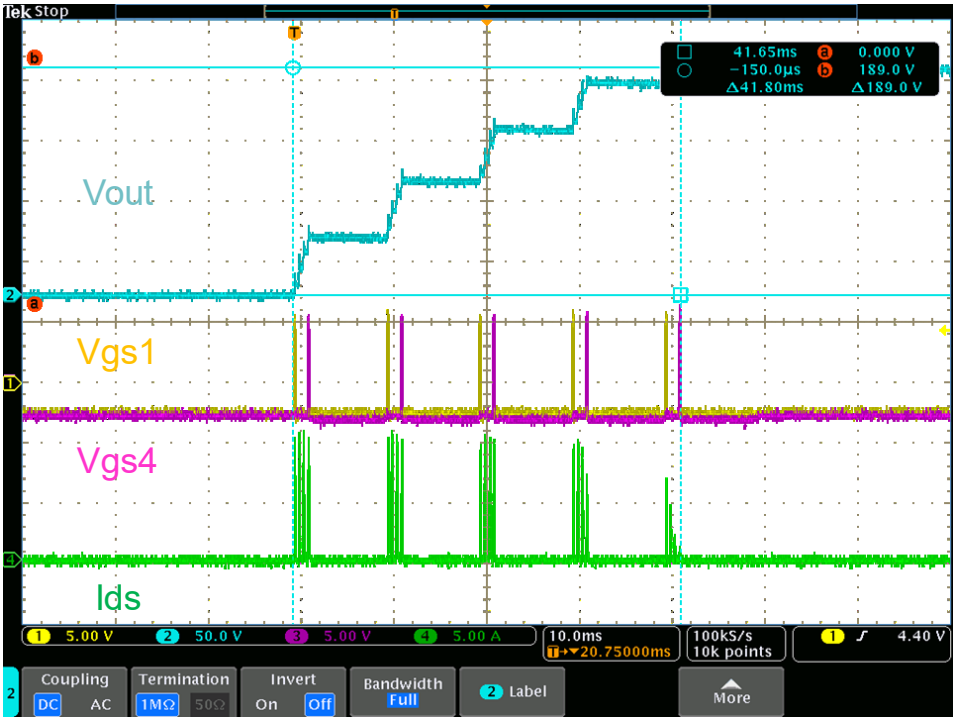


Figure 4.10 Interleaved hiccup close loop startup waveform for 190V/100uF/10A

Figure 4.11 shows one group of saturation current closed-loop control on 10A with 200uS pulse width on every single MOSFET. The gate voltage of the 1st and 4th device is shown in channel 1 and channel 3. They are controlled with an adaptive voltage with DAC on DSP and a related analog drive circuit. The delay of each interleaved pulse is controlled as 500uS.

Figure 4.11 Zoom in multi-channel close loop constant I_D control waveform

Figure 4.12 shows the time delay of each group is 10mS. This delay is the cooldown time for the single device to control the thermal stress. All parameters stated above, such as 10A, 200uS pulse width, 500uS pulse delay and 10mS cooldown time, can be programmed and modified under different load condition.

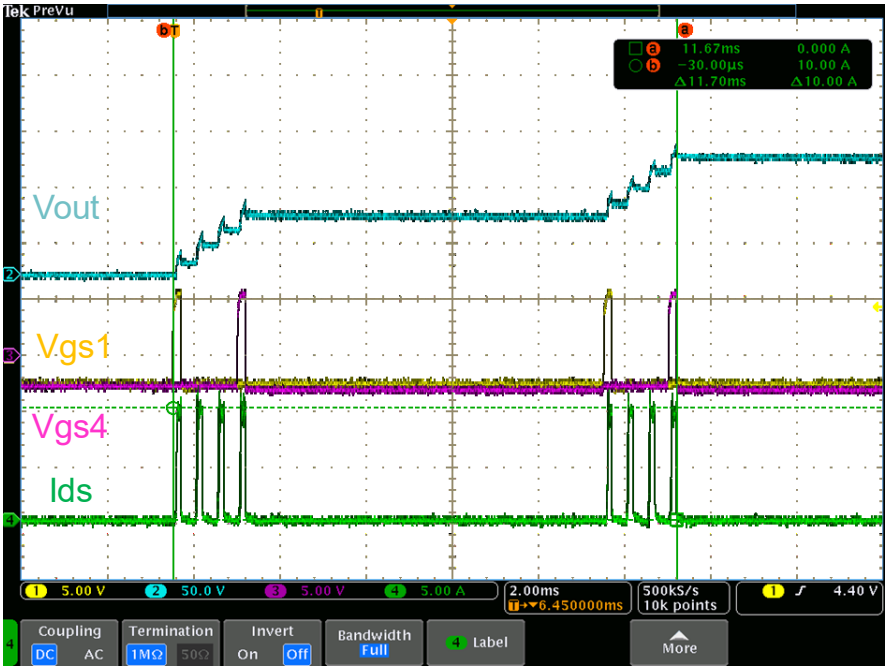


Figure 4.12 Cooldown interval of each group

4.4.3 Steady-state thermal performance

For solid state circuit breaker, most of the working time is normally conducting. So, the temperature rises under heavy load and high current need to be tested.

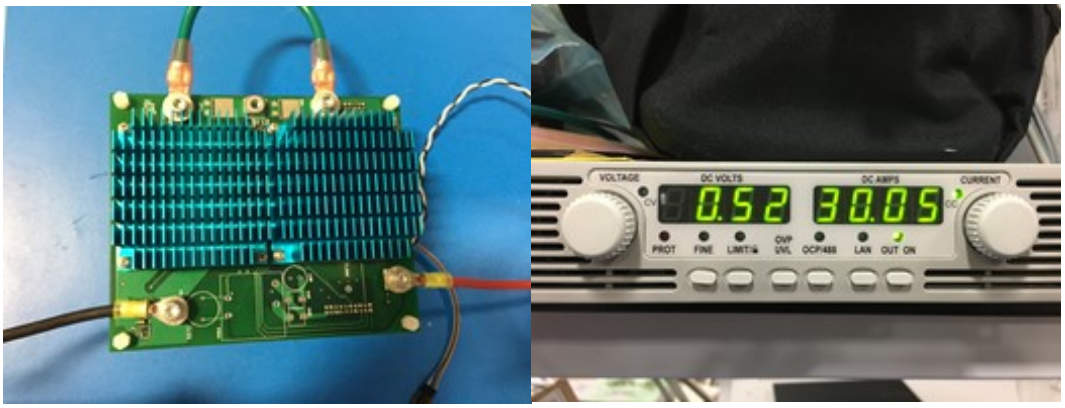


Figure 4.13 Hard configuration of steady state thermal test

Figure 4.13 shows the hardware bench setup and DC power supply.

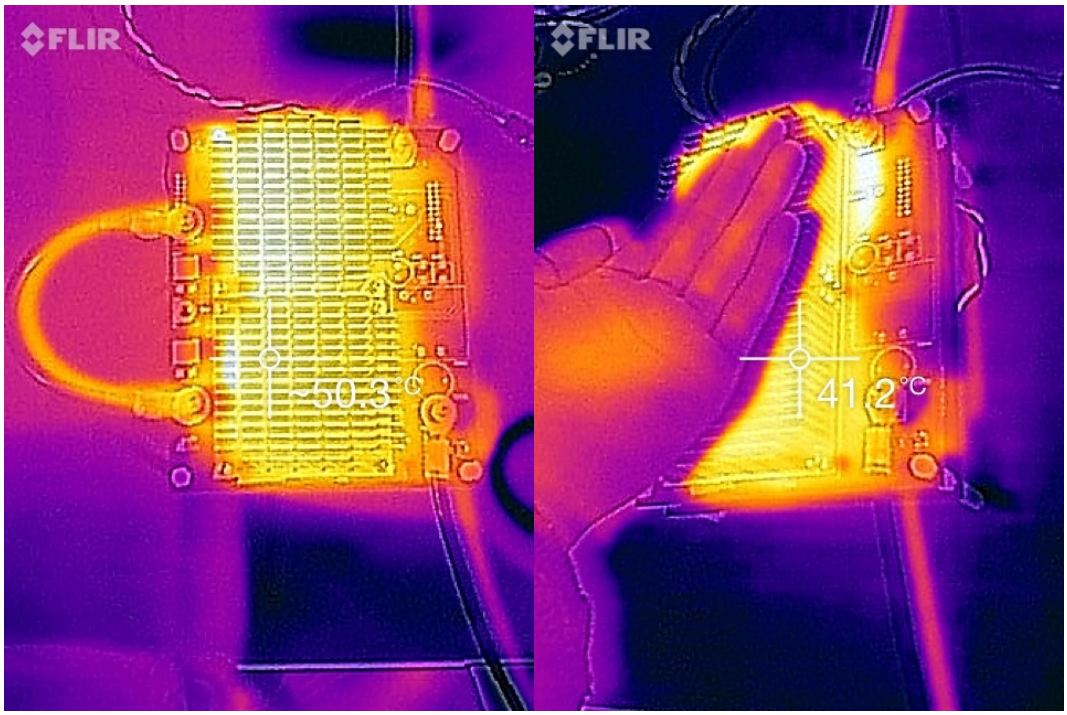


Figure 4.14 Thermal image of heatsink surface view in steady state

As shown in figure 4.14, the steady-state temperature on the heatsink is about 50.3C after 40 minutes with 20C room temperature. It is a safe temperature for human touch. It also means there is enough margin for some other application with severe temperature conditions such as summer in Arizona.

The figure 4.15 shows the side view of the tested solid-state circuit breaker. It shows that the hot spot is on each device.

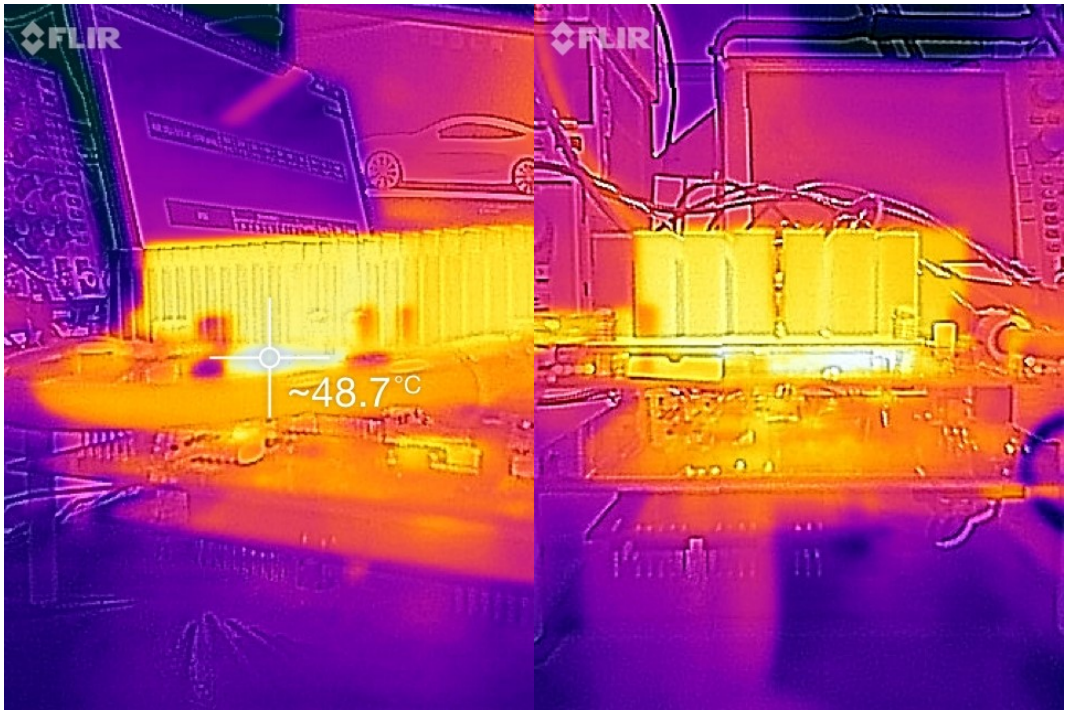


Figure 4.15 Thermal image of side view in steady state

So, the power loss on every single MOSFET can be calculated as in equation 4.4:

$$P_{Single\ MOSFET} = I^2 R_{DS(on)T\_die} = 7.5A^2 \times 17mOhm \times 1.3 = 1.243W \tag{4.4}$$

The junction temperature can be derived with thermal resistance and heatsink temperature:

$$\begin{aligned} T_{Junction} &= \mathrm{P} * R_{th(Die-Heatsink)} + T_{Heatsink} \\ &= 1.243W \times (0.2 + 0.35)\frac{℃}{W} + 50.3℃ = 51℃ \end{aligned} \tag{4.5}$$

4.4.4 Dual threshold overcurrent protection

Similar to design in Chapter 3, the dual threshold overcurrent protection can be also applied to solid state circuit breaker. The DSP calculates the total current flow through 4 paralleled MOSFET and turns off the circuit with programmed time delay. In Figure 4.16, it shows the test results for lower threshold overcurrent protection. The threshold is 32A and load is set to 38A to verify the protection.

The solid-state circuit breaker can filter the shorter intermittent pulses and trip the right long pulse after programmed 800uS.

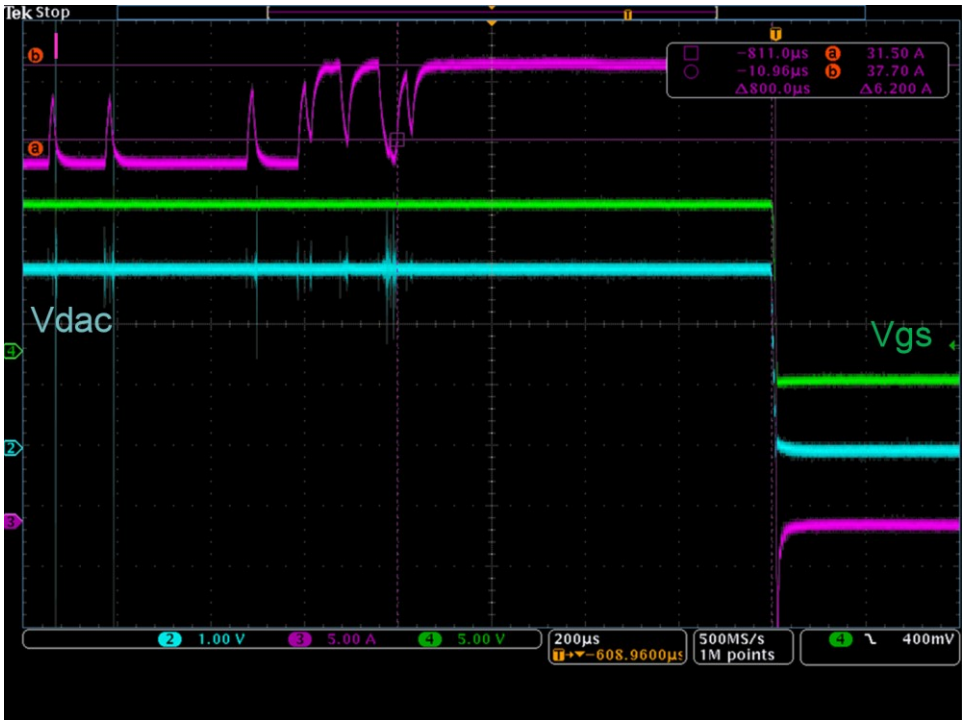


Figure 4.16 Lower threshold OCP with 32A threshold and 800us timer

Figure 4.17 shows the gate voltage change from 12V to -2.5V to trip the breaker.

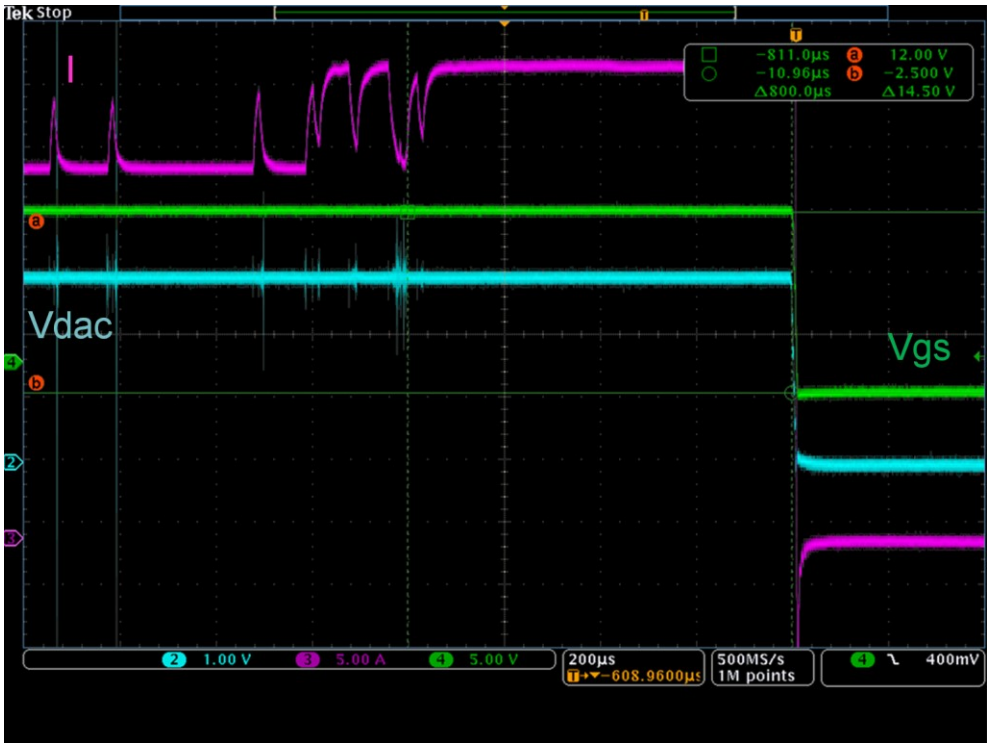


Figure 4.17 Adaptive gate voltage of Si MOSFET as instance

In figure 4.18, the solid-state circuit breaker is tripped with adaptive ramp down digital to analog circuit with 10us time constant to reduce the voltage stress on solid state device. Both current threshold and this ramp speed are also programmable.

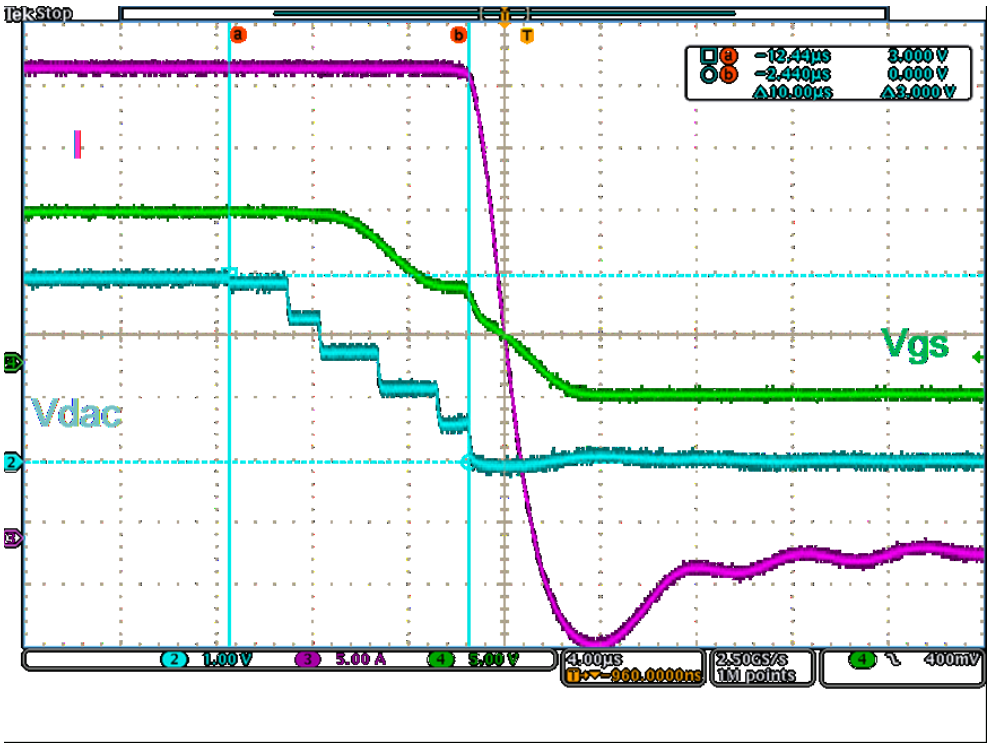


Figure 4.18 Zoom in waveform of programmed adaptive gate voltage in low threshold OCP

In figure 4.19, the high threshold overcurrent protection is demonstrated. The current threshold is programmed as 50A. Once the current hit the high threshold, the solid-state circuit breaker starts the adaptive gate voltage control to saturate the circuit and limit the current with a 200us time delay.

Figure 4.20 shows the adaptive gate voltage is controlled close to 6.6V to control the saturation current close to 50A. And the load voltage decreases because the V_{DS} is not I_D*$R_{DS(ON)}$ during saturation. The power stress on MOSFET is large so the time delay needs to be considered. It is set up as 200us in this case and it is also a programmable variable.

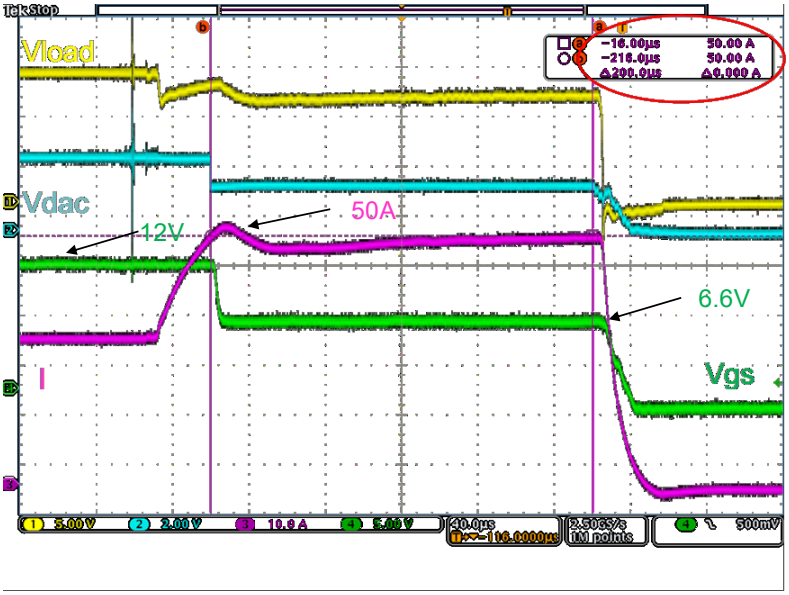


Figure 4.19 High threshold OCP with saturation current close loop control

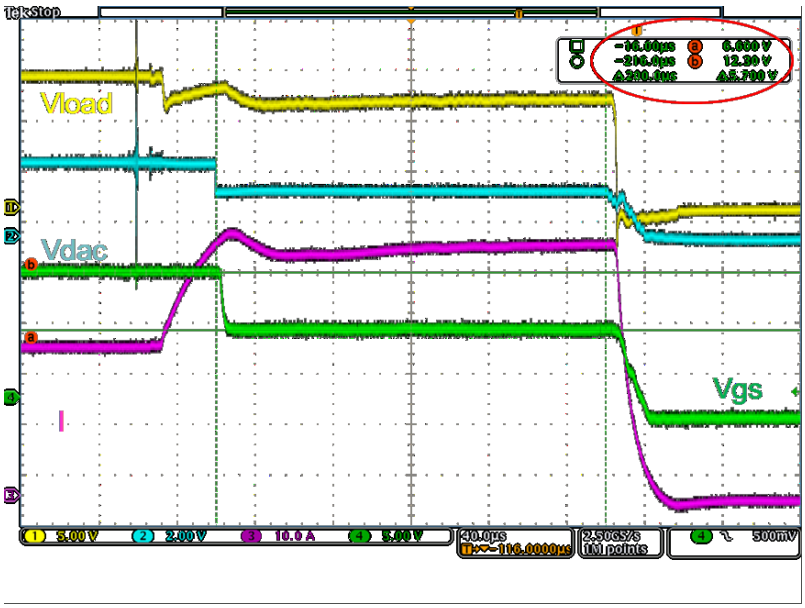


Figure 4.20 Adaptive gate voltage for saturation current control in high threshold OCP

4.4.5 Transient real-time junction temperature monitoring

In the previous description, the junction temperature of the solid device in the transient state can be monitored with equation 4.3 when the saturation current is closed-loop controlled during transient startup.

An experiment has been carried out to verify this proposal. The drain current is set to 7.5A on single device STY139N65M5. The equation 4.6, yields,

$$V_{GS} = f(T_J, V_{DS}) \tag{4.6}$$

Figure 4.21 briefs the experiment, which helps us get obtain the equations 4.3 and 4.6. The short pulse V_{GS} is adopted for getting saturation current I_D=7.5A under various junction temperature T_J and drain to source voltage V_{DS}.

From multiple short pulse tests, a group of data points can be obtained. Corresponding 3D curve fitting is given in figure 4.23.

Although the data lookup table can be used in μController to improve the accuracy, the speed and memory consumption of DSP is unacceptable. Therefore figure 4.23 describes the 3D surface data with linearly polynomial curve fitting.

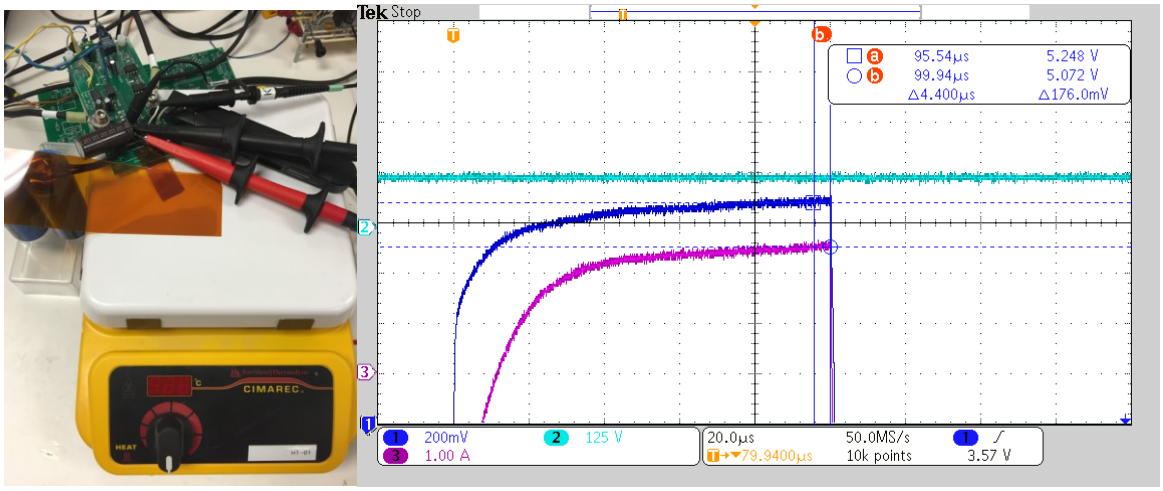


Figure 4.21 Short pulse test with 7.5A I_D and different T_J and V_{DS}

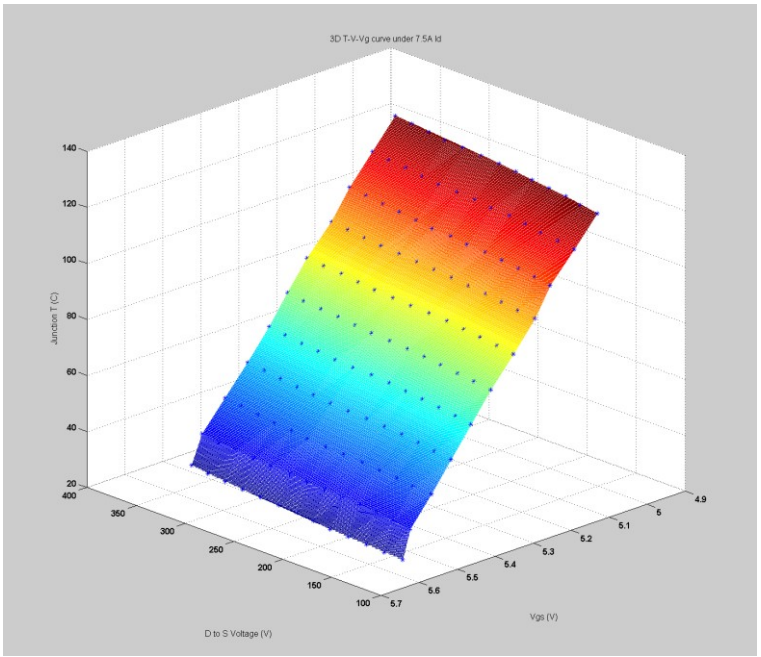


Figure 4.22 Data points from short pulse test for 7.5A and 3D curve fitting result

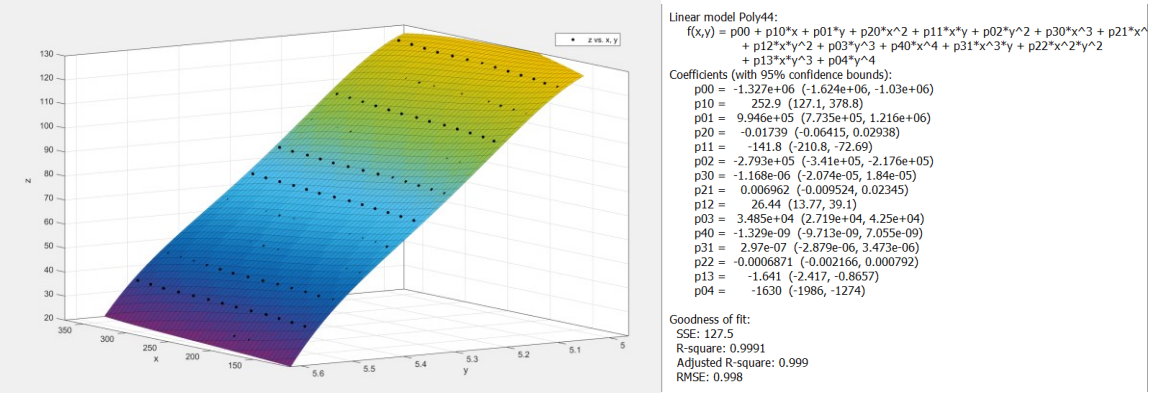


Figure 4.23 3D surface data linear polyfit curve fitting

Although some of the data points are not on the fitting surface of the linear model above, the equations still have the edge for DSP easily processing with fast speed to implement real-time monitoring.

Figure 4.24 gives the V_{GS} and V_{DS} of first saturation pulse with I_D=7.5A being constant. The V_{GS} changes from 5.50V to 5.38V as both junction temperature and the drain to source voltage change on the 3D surface.

The monitored junction temperature is in figure 4.25. The result indicates that the junction temperature changes from 36.28˚ C to 60.99˚ C in coordinated 421us. This monitored temperature can be examined with transient thermal impedance of used device. The comparison is given in figure 4.26.

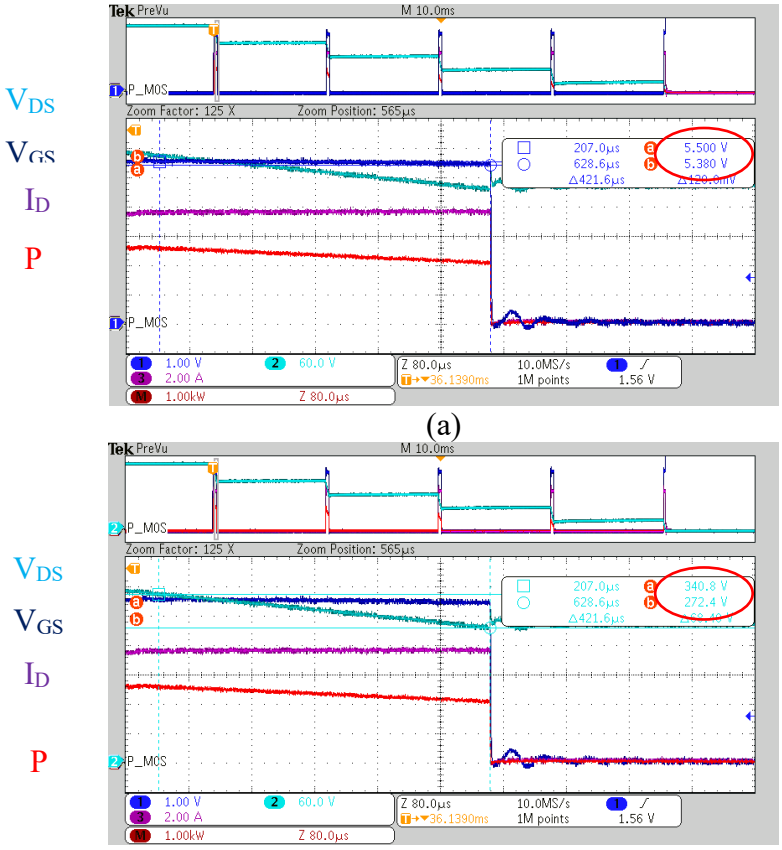


Figure 4.24 V_{GS} and V_{DS} of first saturation pulse

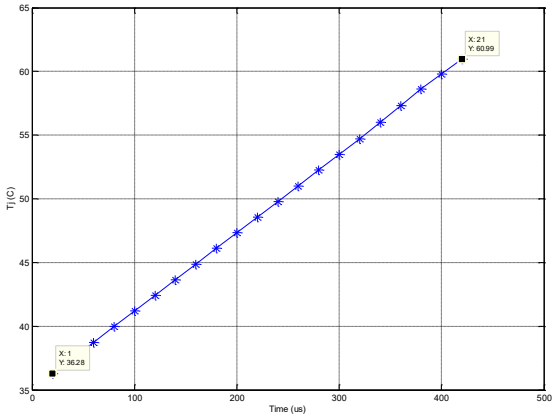
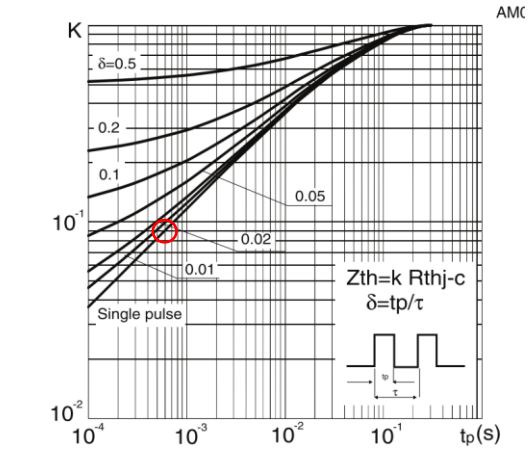
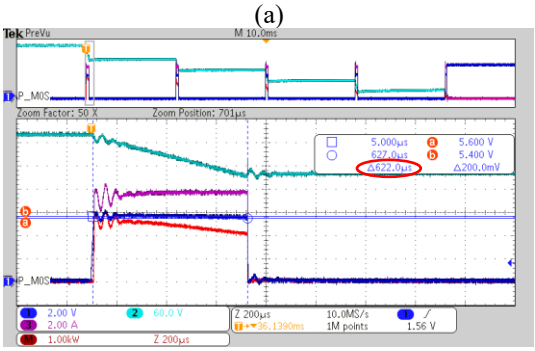


Figure 4.25 Result of transient junction temperature monitoring



(a)



(b)

Figure 4.26 (a) Transient thermal impedance of tested device
(b) Pulse length of first saturation pulse

The theoretical temperature rise can be calculated as:

$$T_J - T_C = K * R_{th(J-C)} * P \tag{4.7}$$

From figure 4.26 (a), K = 0.09 for 600us, $R_{th(J-C)}$ = 0.2˚C/W for STY139N65M5. With P = 2400W, T_C = 20˚C, the resulting T_J equals to 63.2˚C. The accuracy is about:

$$\frac{60.99 - 63.2}{63.2} = 3.5\% \tag{4.8}$$

4.5 Conclusion and summary

To sum up, a paralleled solid-state circuit breaker is introduced and evaluated for 380V/30A application. Several innovations are proposed and realized.

1. The designed circuit breaker can work with 3 wires 2 phase ±190V DC system for input UVLO protection, overcurrent protection between P-N, P-E and N-E buses which makes it an intelligent 3 pole DC circuit breaker. The whole circuit breaker can be easily programmed with multiple parameters under different scenarios and for varies applications in practice.
2. The interleaved hiccup startup for inrush current is proposed for overcoming the positive temperature coefficient for saturation current during parallel operation. It keeps the fast startup speed with averaged thermal stress sharing.
3. The modular design for every single device is optimized with distributed input snubber capacitor, output freewheeling diode, the current sensor circuit and driver circuit. This design can allow symmetrical current path and is easy for measurement for larger current design with the single TO-247 package.
4. A transient and steady-state real-time junction temperature technology is proposed and tested. It is novel and practical for saturation current mode and normally turn-on mode in solid state circuit breaker application.

5. For 3 wire system with 2 group of solid state devices, the unbalanced current can be sensed to detect high impedance fault on P-E and N-E buses. This is a very useful feature, which can prevent potential fire hazard with the inflammable material in practice.

CHAPTER 5

Hybrid Circuit Breaker for 380V DC System

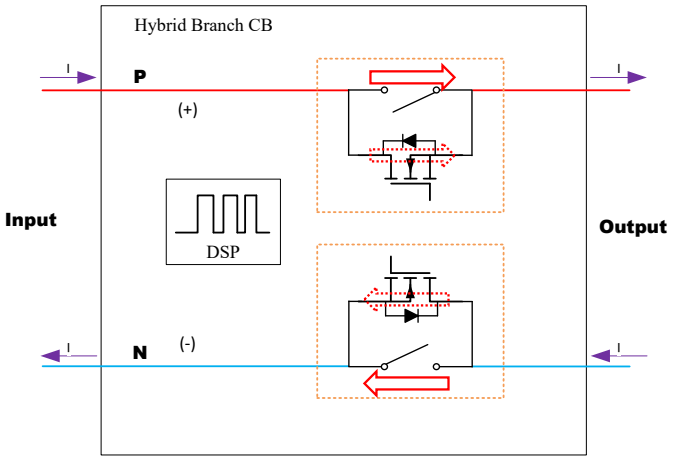
5.1 Introduction and Motivation

In the previous chapter, the pure solid-state circuit breaker is designed with fast trip speed. However, the $R_{DS(ON)}$ is still a parameter limit the current rating of the solid-state device. The approach with paralleled single devices will be bulky and costly for the pure solid-state circuit breaker. In addition, the pure solid-state approach is cost inefficient, especially for bi-directional application with high current. The doubled number of devices consumes double cost, volume, and power dissipation.[56]–[58]

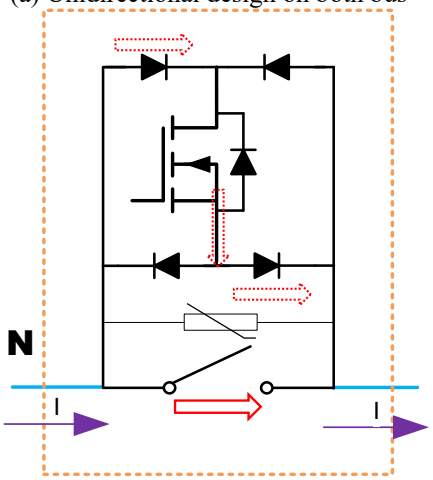
Therefore, a hybrid circuit breaker for the high current branch in 380V DC application is desired and investigated here. Corresponding operation modes and driving strategy are given step by step. The test results show a great performance for high current commutation.

5.2 Hardware Design and Analysis

5.2.1 Circuit topology



(a) Unidirectional design on both bus



(b) bi-directional module on N bus

Figure 5.1 Circuit topology of hybrid branch circuit breaker

The circuit topology is shown in figure 5.1 with both unidirectional design and bi-directional design. The bi-directional can be easily achieved with passive diodes without considering extra control and driver circuits. The solid red arrow shows the main current path for most of the time. The dashed arrow shows the transient current path during us current commutation period. The input capacitor and snubber output diode are neglected which is similar as in Chapter 4.

5.2.2 Coordination control strategy of solid state and mechanical switch

The coordination control is shown in figure 5.2. Similar to solid state circuit breaker, the inrush current is also controlled by paralleled active devices with saturation current limitation. It also helps to prevent the contacts of the mechanical switch and the weak point of the main circuit without large inrush current. The number of paralleled devices can be substantially reduced due to no power dissipation limit anymore on solid state devices but only current turn off limit.

For the trip process, once the controller sensed overcurrent with setup threshold, the fast-mechanical switch starts to turn off. After a certain period, the fault current has commutated into solid state devices and the mechanical switch can withstand 380V, then the solid-state devices start to trip in several microseconds.

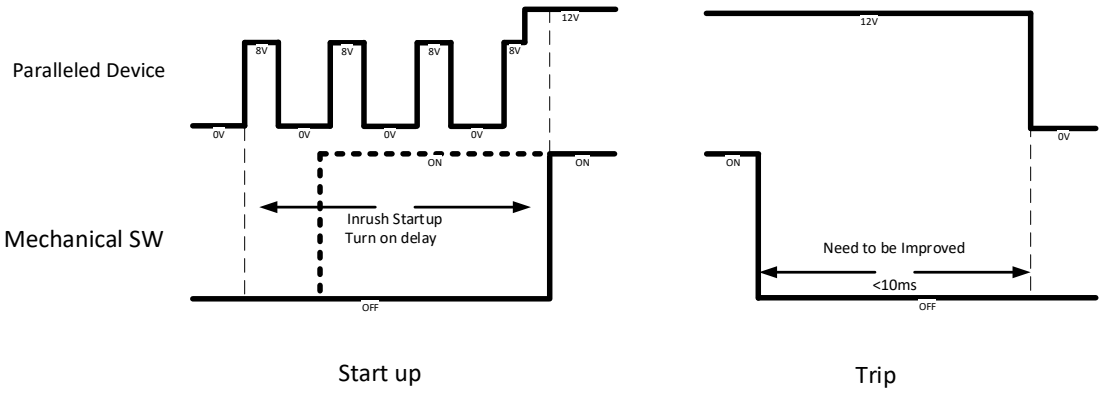


Figure 5.2 Control strategy of hybrid branch circuit breaker

5.3 Fast Mechanical Switch Mechanism and Analysis

The most important component of the circuit breaker in the hybrid branch is the fast-mechanical switch selected for the entire circuit breaker. Among tons of mechanical switches, several features are taken into considerations to select appropriate part of DC circuit breaker application.

5.3.1 Feature analysis for DC circuit breaker application

1. Insulation Capability

For 380V DC application, the first important factor of a mechanical switch is the insulation capability. Although there is no final standard for DC circuit breaker, the insulation capability should be at least higher than paralleled solid-state devices. If 650V device is applied, the steady state dielectric strength between two contacts of the mechanical switch should be at least above 650V. Above that value, the MOV will be active to protect the circuit.

2. Turn off speed

As stated in Chapter 1, the short-circuit current in DC system is much more severe than in traditional AC system due to the energy storage on various capacitance on the bus and lacking zero crossing sinusoidal waveform. This is also one of the reasons that traditional MCCB is not a good option for 380V DC system. In Chapter 3 and 4, the speed of solid state device CB can be in 10us for the instantaneous trip. And the instantaneous CS-Series DC circuit breaker trip speed is about 40ms. So, the trip speed of fast mechanical switch should be much better than this value. The target of current design in this chapter is about 1-2ms.

3. Turn on resistance

The turn-on resistance is one of the advantages of mechanical switch compared with the application of solid state devices in the high current situation. The fast mechanical switch is the main current path during normally-on operation which is the most common state of the hybrid circuit breaker. So, the turn-on resistance determines the power loss and affects the thermal performance and energy efficiency of the circuit breaker.

4. Driving power consumption

For the mechanical switch, most of the candidates need extra power to control and drive them. The normally-on driving power is one important parameter which needs to be emphasized and evaluated.

5. Size and volume

The volume and size comparison is introduced above for mechanical switch and solid-state devices for same resistance rating, which is the advantage of the mechanical switch to defeat solid state devices in the high current application.

6. Cost

The cost is certainly a factor that needs to be compared.

Considering all above aspects, one high current relay[59] in figure 5.3 is chosen.

Figure 5.3 Picture of high current mechanical relay

Table 5.1 shows its specifications.

Table 5.1 Specifications of TE Latching Power Relay

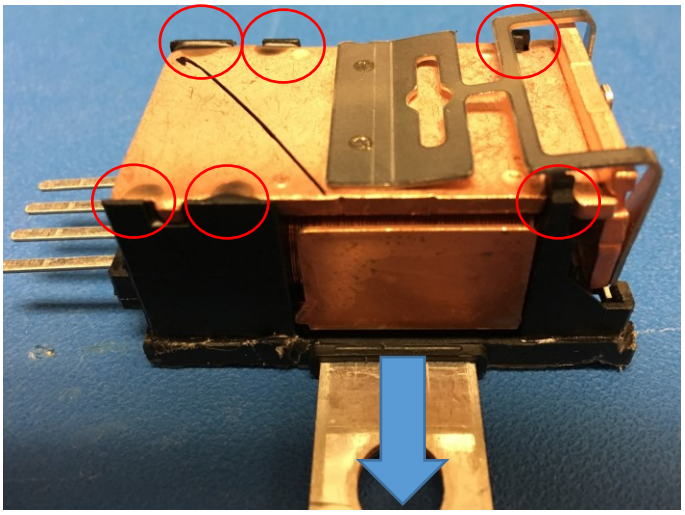
Insulation Data	
Initial dielectric strength between open contacts between contact and coil	 500Vrms 500Vrms
Coil Data	
Magnetic system	Bi-stable (two coil system)
Rated coil voltage	12VDC
Max. coil power	approx. 7W at 20°C for U_{on}/U_{off}
Max. coil temperature	155°C
Contact Data	
Contact arrangement	1 form X, 1 NO DM (bridge)
Initial voltage drop	at 100A <40mV
Rated current: from Terminal B to A, cable 50mm^2	 260A
Limiting continuous current: 23°C 85°C 125°C	 load cable 50mm^2 260A load cable 50mm^2 190A load cable 50mm^2 88A
Contact material	$AgSnO_2$
Contact style	bridge contact
Operate/release time typ.	5ms at 14VDC (coil voltage)

Mechanism of this power relay is analyzed in the following section 5.3.2. The novel driving strategy is proposed and analyzed to improve the performance in section 5.3.3.

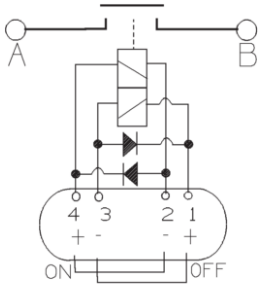
5.3.2 Mechanism analysis of selected high current relay

(a) Current loop analysis

Figure 5.4 shows a hardware configuration of selected relay without an outer enclosure. It is composed of by two parts, which are connected by plastic frame boding at red points firmly.



(a) Hardware configuration

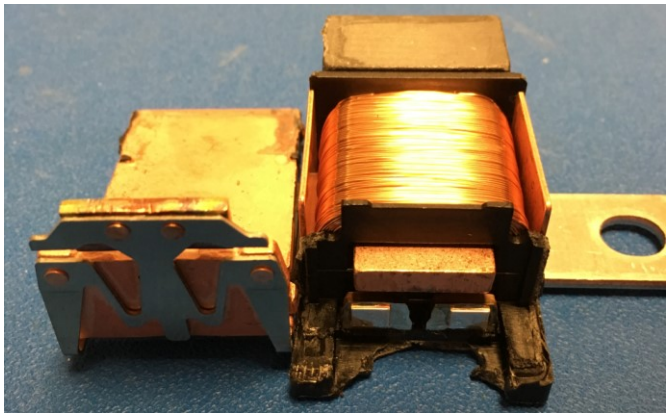


(b) Schematic

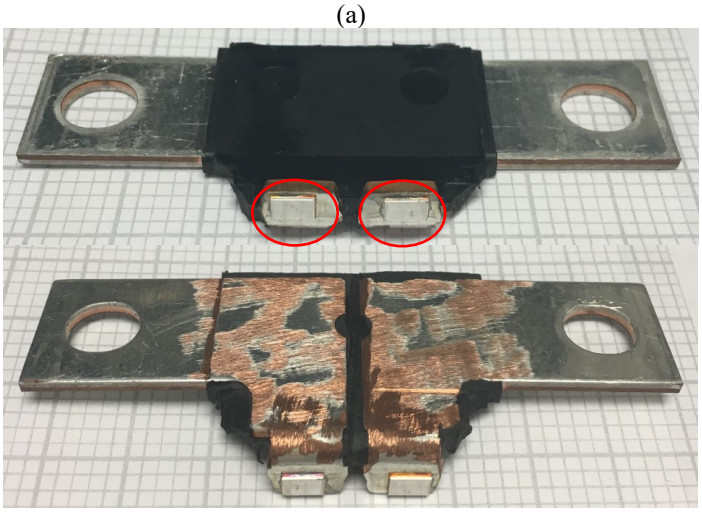
Figure 5.4 Hardware configuration of high current mechanical relay

1. The upper part is coil system with two anti-paralleled freewheeling diodes. The metallic attachment is fixed with the magnetic core to act as a spring for latching. A permanent magnet is inserted into the magnetic path to have a built-in magnetic potential for latching.

2. The lower part is the main current path for 260A. It is formed with two copper bus bars with holes for screw connecting and $AgSnO_2$ contacts.



(a)



(b) Top and bottom side of lower part

Figure 5.5 Hardware configuration of upper part (a) and lower part (b)

(b) Magnetic loop analysis

Before proceeding to modes analysis, the magnetic path is given in figure 5.5 for further analysis. The whole magnetic path is consisting of 5 components.

1. Permanent magnet: have a built-in potential on magnetic force

2. Motionless roof magnetic core: supply a path and attach the metallic frame to provide mechanical force as spring.
3. Dynamic hood magnetic core: attach to the other side of the metallic frame with the different force for a different position.
4. Air gap: the air gap changes the magnetic force when the hood moves to different positions.
5. Coil and coil magnetic core: initiate the alterable electromagnetic force with different pulse voltages.

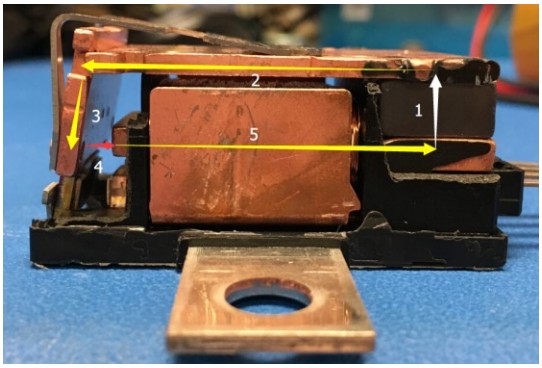


Figure 5.6 Profile of hardware for showing magnetic path

(c) Operation mode analysis:

1. Latching Off

For latching off, there is no electromagnetic since there is no power and voltage from pins. So in the steady-state force is balanced of the hood magnetic core as seen in figure 5.6.

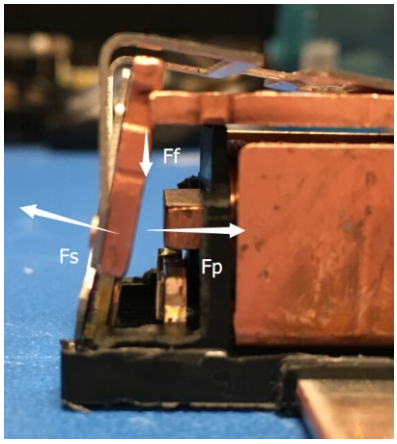


Figure 5.7 Force analysis of latching OFF

$$\overrightarrow{Fp} + \overrightarrow{Fs} + \overrightarrow{Ff} = 0 \tag{5.1}$$

The p indicates the permanent magnetic force, s indicates the force from spring of metallic frame, and f indicates the force downward from the frame point of roof magnetic core. The latching is mainly due to the metallic frame.

2. From off to on transient

With a pulse voltage on coil 1, there will be an electromagnetic force generated to break the balance and attract the dynamic hood magnetic core. The updated force analysis is in figure 5.7. There is:

$$U = I \times R + \frac{d\Phi}{dt} \tag{5.2}$$

The U is the voltage (V), I indicate the current in the coil (A), R is the coil resistance (Ω), Φ is the magnetic flux (Wb). And for Φ:

$$\Phi = \frac{\mathcal{F}}{\mathcal{R}} = \frac{NI}{\mathcal{R}_{core}+\mathcal{R}_{gap}} \tag{5.2}$$

The $\mathcal{R}$ is the magnetic reluctance and it is related to the displacement of movement. N is the turns of the coil and I is the coil current. And for electromagnetic force:

$$F_{coil} + F_p - F_{s\_x} = m\left(\frac{{d_x}^2}{{d_t}^2}\right) \tag{5.3}$$

From above equations, the electromagnetic force F_{coil} is a function of I, x and N.

$$F_{coil} = f(I, x, N) \tag{5.4}$$

This coil electromagnetic force breaks the balance and the permanent magnetic force will also increase because of the smaller air gap. At the meantime, the spring force will also increase and build a new balance in state 3.

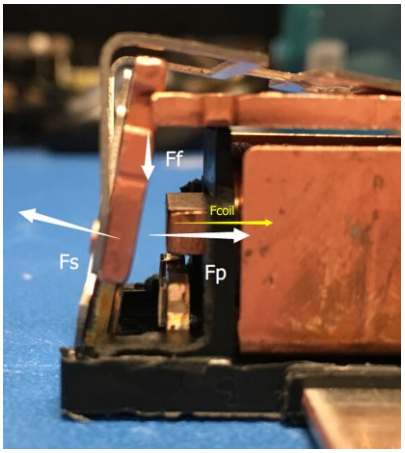


Figure 5.8 Force analysis of OFF to ON

3. Latching On

For latching ON, there is no electromagnetic because there is no power and voltage from pins. So, in the steady-state, the force is balanced of the hood magnetic core as in figure 5.8.

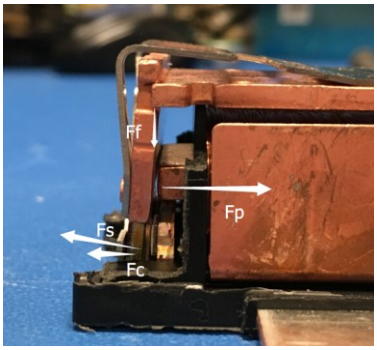


Figure 5.9 Force analysis of latching ON

$$\vec{Fp} + \vec{Fs} + \vec{Ff} + \vec{Fc} = 0 \tag{5.5}$$

The p indicates the permanent magnetic force, s indicates the force from spring of metallic frame, f indicates the force downward from the frame point of roof magnetic core, and c indicates the reactive force from $AgSnO_2$ contact pad. One should pay attention to such problem that both p and s force has changed from latching off because of the change of air gap and shape of the metallic frame.

The c force is very important and associated with the contact resistance. If the new design can supply larger force with larger reactive force on the pad, the contact resistance can be even smaller.

4. From on to off transient

Similarly, as in state 2, the repulsion force brought by pulse current on coil breaks the balance and helps to build a new balance with smaller permanent magnetic force and spring force back to state 1. This force is also a function of I, x and N which is similar to equation 5.4.

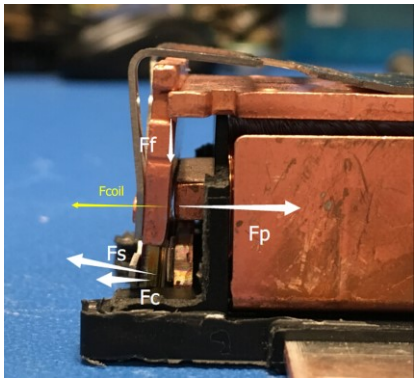


Figure 5.10 Force analysis of ON to OFF

5.3.3 Novel driving strategy with performance enhancement

In 5.3.1, the key features of the mechanical switch in hybrid DC circuit breaker are analyzed for better performance. In this part, a novel driving strategy is proposed to enhance the trip speed and contact resistance based on above discussion.

One of the most important parameters is the trip speed in state 4. The larger coil repulsion electromagnetic force is a way to accelerate this process. From equation 5.4, for larger F, the larger I and N are the only parameters which can be modified with driving circuit. Then the figure 5.10 shows the proposed driving waveform.

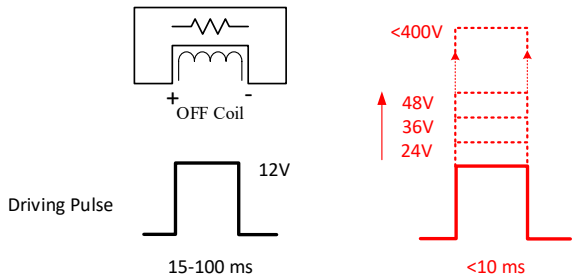


Figure 5.11 official recommended drive waveform and proposed drive waveform

With higher voltage, the coil current I can be increased without changing N to enhance the repulsion electromagnetic force. For proposed hybrid circuit breaker application, the trip speed needs to be within 10ms, hence the pulse width can be shorter to keep the power on coil below maximum coil power which is about 7W for 20 °C. Although the spring force is the final force to keep the relay in latching OFF state, the initiating force determines the speed from ON state to the state which can withstand 380V DC.

For reducing the contact resistance, another driving voltage change is proposed in figure 5.11.

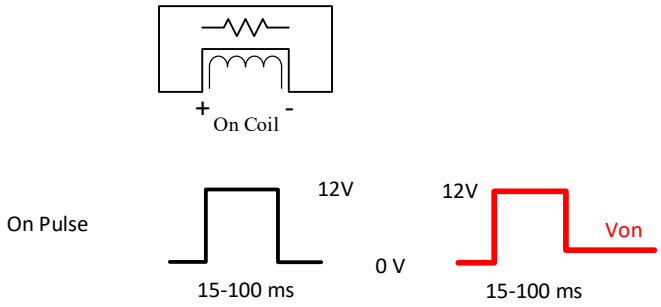


Figure 5.12 Proposed driving scheme to reduce contact resistance

The major difference is to keep a Von after turn on to supply an extra electromagnetic force F_{Von} shown in figure 5.12. This force can help to increase the Fc on contacts to have smaller contact resistance.

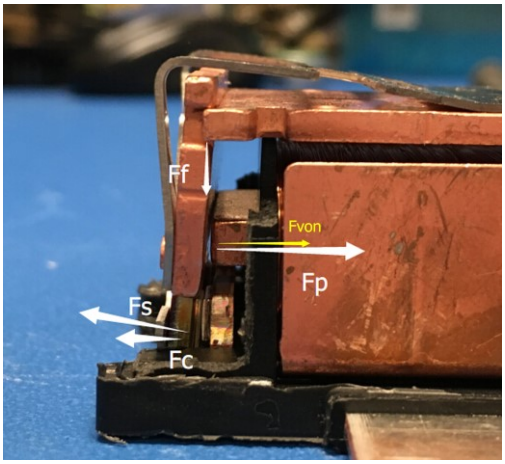


Figure 5.13 Force analysis of ON state with proposed Von

However, this will also induce extra drive power consumption. It should be calculated with power consumption tradeoff analysis as:

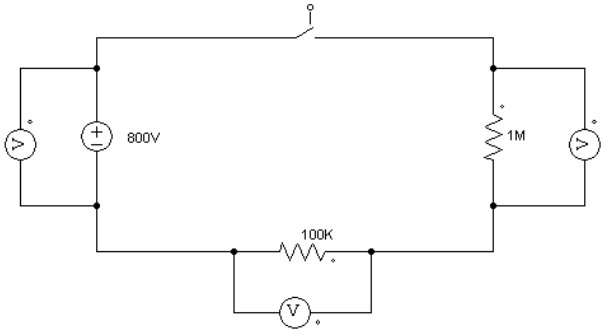
$$\frac{{V_{on}}^2}{4.95} < I^2(400u\Omega - R_{new}) \tag{5.6}$$

The Von is the coil voltage applied for on state, 4.95 ohm is the coil resistance. I indicate the main circuit current, 400uΩ is the contact resistance without change, R_{new} is the new contact resistance. Assuming Von is 2.5V, I is about 190A, then the proposed strategy is cost-efficient if R_{new} is smaller than 365uΩ.

5.5 Experimental Test and Verification

5.5.1 Insulation test and verification

As stated in 5.3.1, the selected mechanical relay should have the capability to physically isolate high voltage during turn off. Figure 5.13 exhibits the insulation test circuit and hardware setup of high voltage in the steady state.

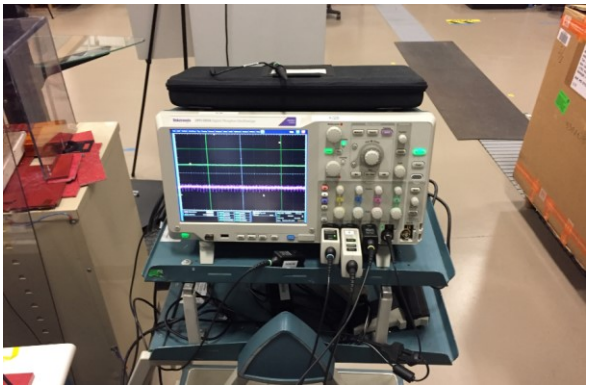


(a) Test circuit schematic

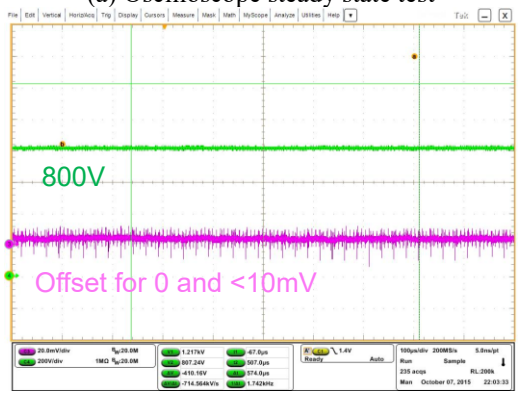
(b) Test circuit setup

Figure 5.14 Steady state insulation test setup

The DC voltage is increased to 800V for 10 minutes to test the insulation during the off state. The 1MΩ is used to protect the power source and 100kΩ resistor is used to test the leakage current value. The waveforms are shown in figure 5.14.



(a) Oscilloscope steady state test



(b) Green is for 1MΩ; pink is for 100kΩ

Figure 5.15 Steady state insulation test voltage drop waveforms

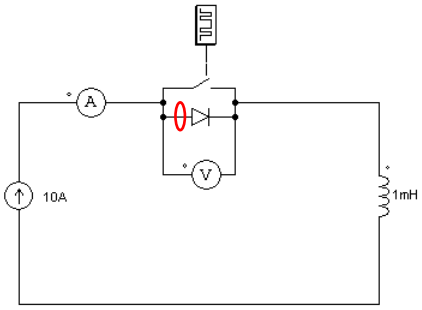
The voltage drop on 1MΩ is kept 800V for 10 minutes and <10mV on 100kΩ to have <0.1uA leakage current for 10 minutes. It is mostly because of the accuracy and offset of the probe.

This test demonstrates that the selected power relay can physically isolate 800V in the steady state which is favorable for 380V DC application.

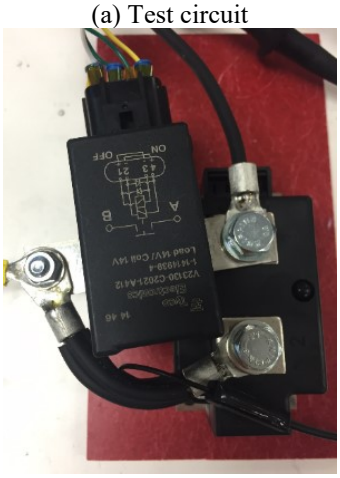
5.5.2 Driving strategy test and verification

The novel driving strategy is tested with the proposal shown in figure 5.10. The idea is to increase the pulse voltage on turn off coil to accelerate the process with larger repulsion electromagnetic force.

The test circuit is shown in presented figure 5.15. A current source is employed to provide current from 30A to 50A. A diode is paralleled with power relay to act as solid-state device for hybrid circuit breaker. The relative hardware setup is given in figure 5.15 (b), with a close loop designed to reduce the loop inductance and a Rogowski current probe adopted to measure the transient current into the diode after current commutation.



(a) Test circuit



(b) Hardware setup

Figure 5.16 test circuit for proposed driving strategy

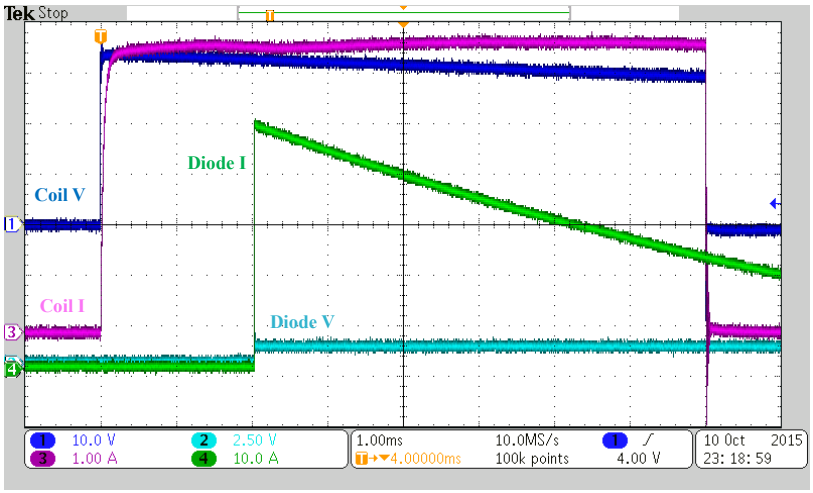


Figure 5.17 Typical turn off transient waveform

Figure 5.16 gives a typical example of a turn-off transient waveform. At 1ms, the pulse voltage is applied to reset coil to start the turn off process. Until 3ms moment, the current is still on power relay so that there is no voltage drop on the diode. At 3ms, the current is commutated into diode so the diode voltage changes to 1V and the transient diode current is shown in channel 4. The current starts to decrease because the Rogowski current probe cannot keep low-frequency component and the current is a DC value in a real circuit.

Figure 5.17 shows the pulse voltage waveforms applied to reset coil for turn off the mechanical switch. 12V to 30.6V with 12ms width and 30.6V to 60.1V with 6ms were tested.

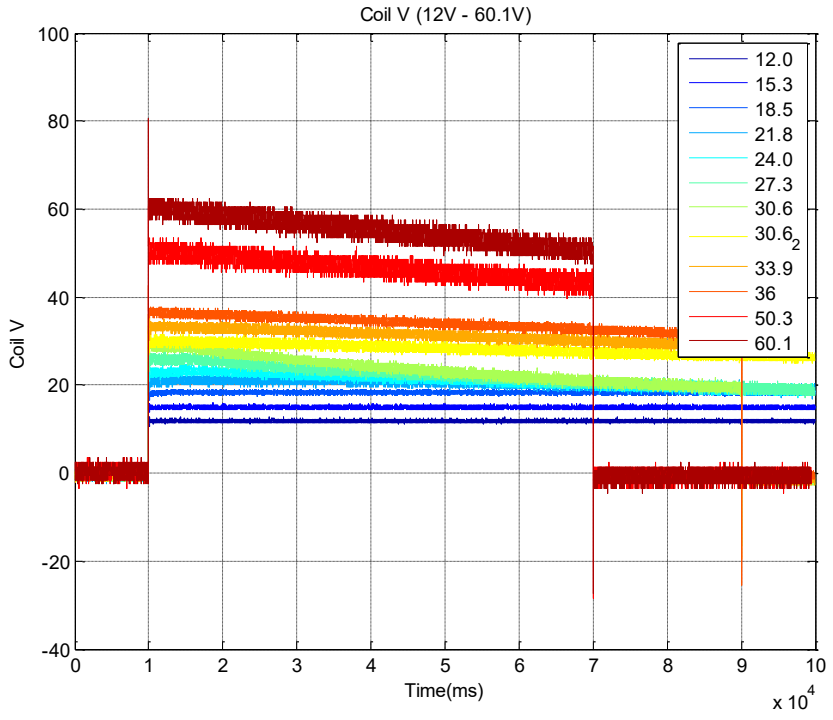


Figure 5.18 Pulse voltage on reset coil

Correspondingly, figure 5.18 shows the current waveforms of reset coil. The current follows the voltage change and contribute to larger magnetic flux. The width of current is the same as the coil voltage pulse width.

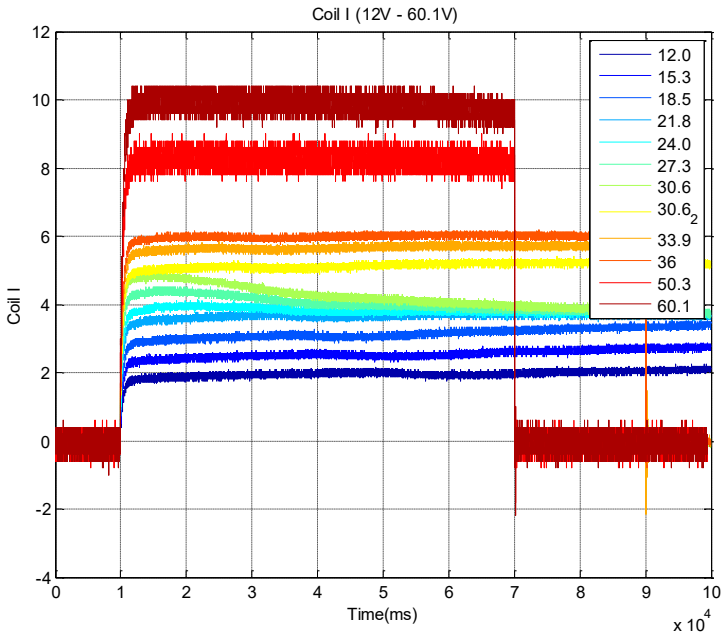


Figure 5.19 The current waveforms on reset coil for 12V to 60.1V

Figure 5.19 presents the sensed main current on the diode similar as in figure 5.16 for demonstrating the trip speed. The active solid-state device can start to act turn-off and trip the whole hybrid circuit breaker once the current is commutated into the paralleled diode. So, the time delay on current commutation represents the trip speed of hybrid circuit breaker as the turn off speed on solid state device can be fast as in 10us.

All pulse voltage starts from 1ms, and the current commutation delay varies from 4.5ms (for 12V) to about 1.5ms (for 60.1V), which verified the proposed driving strategy works.

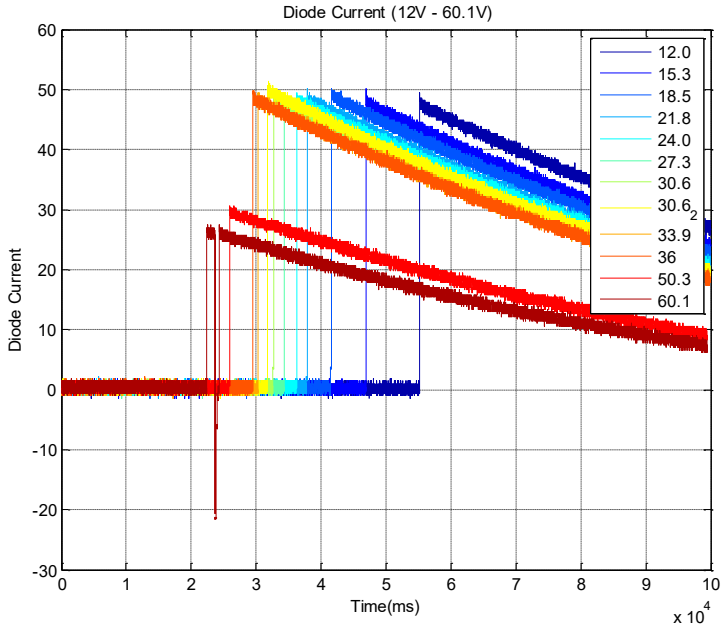


Figure 5.20 The current waveforms on diode for 12V to 60.1V

Figure 5.20 displays the voltage drop waveforms on the paralleled circuit to show the arc voltage. Similar to figure 5.19, the voltage drop is 0V when all current flow through the latching ON state power relay. After current commutation, the voltage drop changes to about 1V since all current is flowing through the paralleled diode after turn off of the mechanical switch. Besides, there is an arc voltage around 8-9V owing to the loop inductance and the phenomenon of arcing during disconnection in DC system. This arc voltage could help to commutate current into paralleled active solid-state devices with the potential difference of the arc voltage and the conductive voltage drop on the solid state circuit.

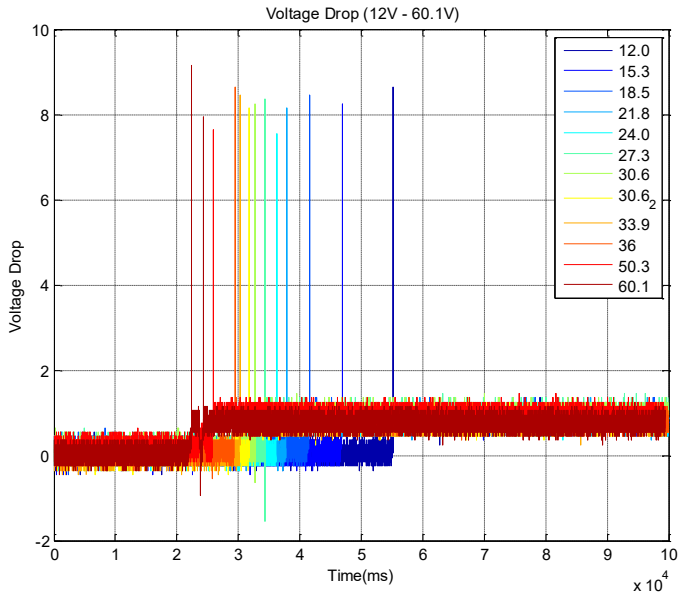


Figure 5.21 The voltage drop on relay for 12V to 60.1V

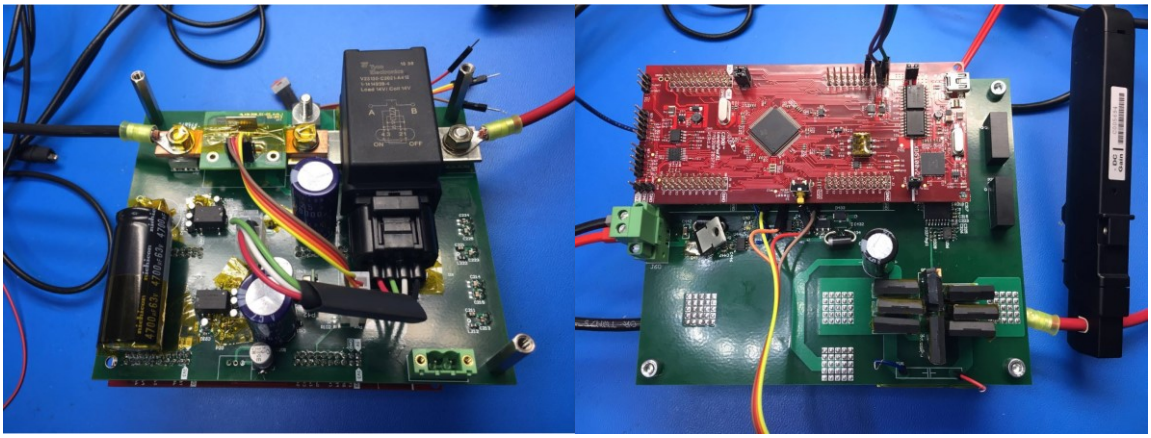


Figure 5.22 Hardware of hybrid branch circuit breaker

Figure 5.21 shows the final hardware development of hybrid branch circuit breaker for 380V DC system with bi-directional power flow capability. It is designed with one active solid-state device and 4 diodes as shown in Figure 5.1(b). The commutation loop has been optimized to be as close as possible for the paralleled fast mechanical switch and solid-state devices to reduce the loop inductance, shown in Figure 5.22.

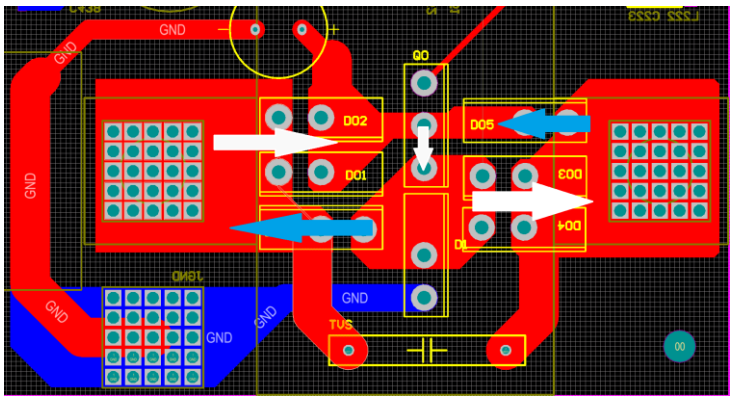


Figure 5.23 Minimized current commutation loop in PCB design

Figure 5.24 shows the difference of turn-off speed of fast mechanical switch with 30V and 50V driving voltage in final hybrid circuit breaker hardware. The values are 2.25ms and 1.61ms which proved the innovated driving strategy. The strategy can be applied to affect the movement of mechanical switch and accelerate the trip speed of hybrid branch circuit breaker.

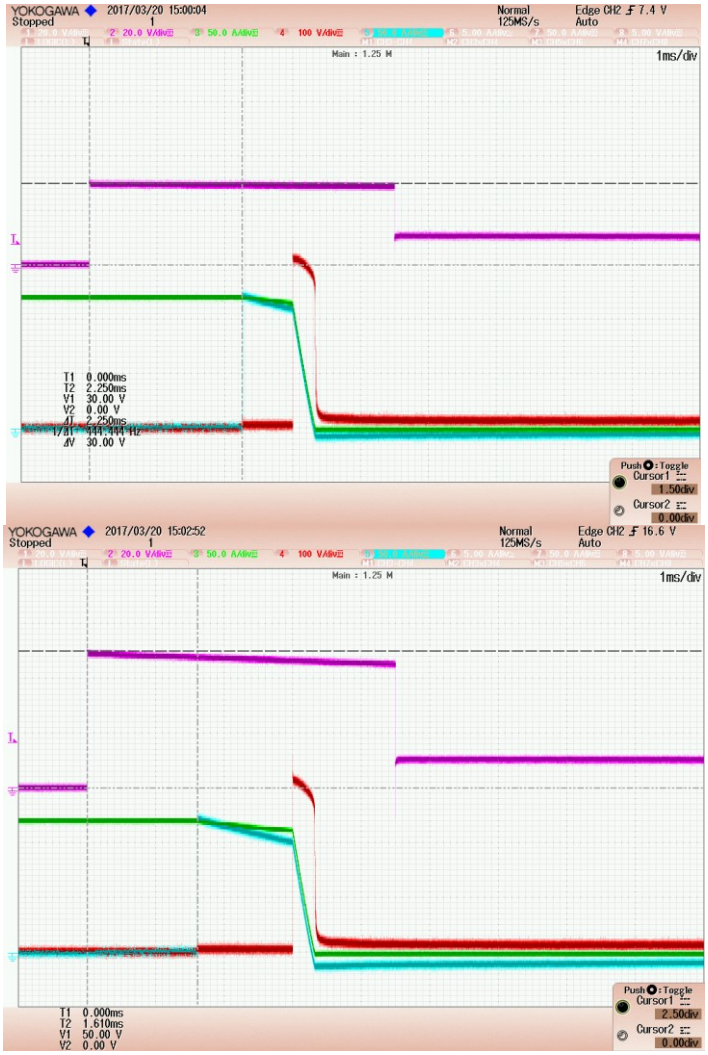


Figure 5.24 The delay of turn off for 30V and 50V

Figure 5.25 shows the trip waveform under 200A and 50V driving voltage on the mechanical switch. The MOSFET is programmed to turn off the whole circuit with 0.4ms endurance time which makes the whole tripping speed is about 2ms. This endurance time can be reduced to several us to accelerate the total trip speed into 1.61ms. Figure 5.26 shows the zoom-in waveform for 200A and 50V test with 1.604ms turn-off speed in the mechanical switch.

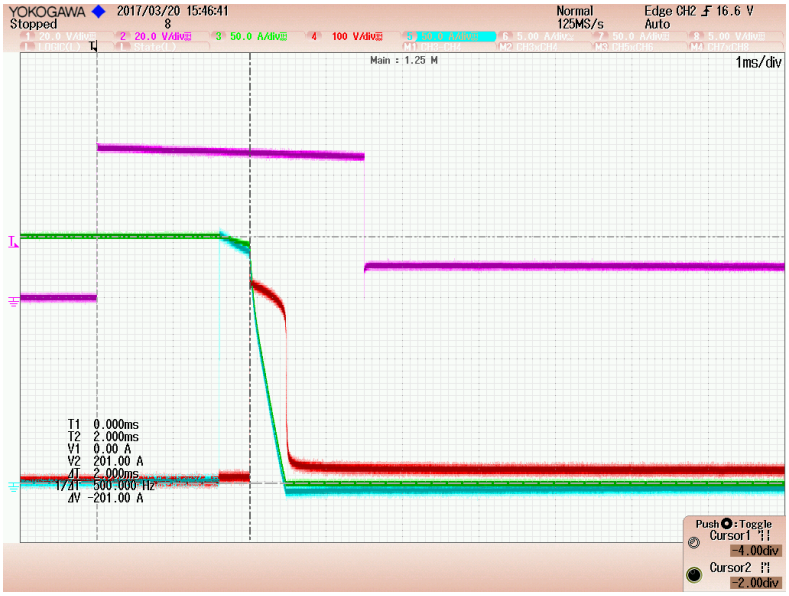


Figure 5.25 The turn off test for 200A and 50V driving voltage

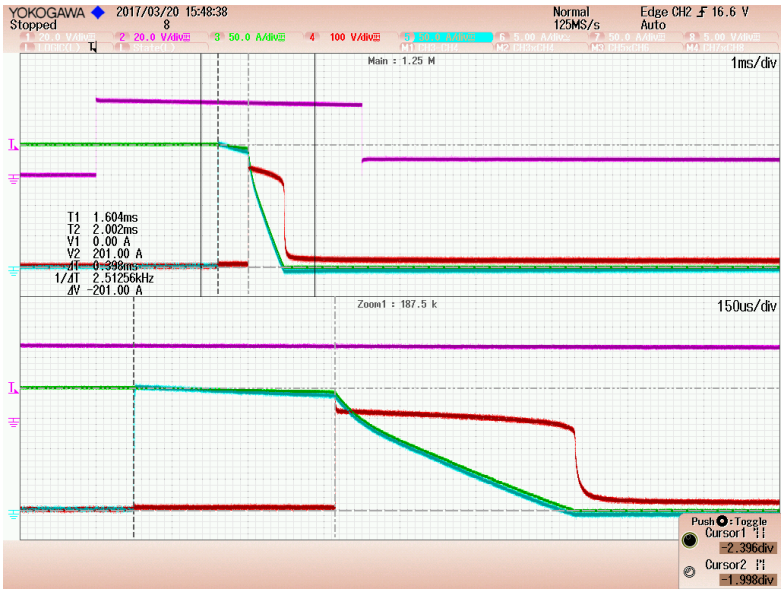


Figure 5.26 Zoom in waveform for 200A and 50V driving voltage

Figure 5.27 shows the test result of HIOKI RM354B Micro resistance meter for conducting resistance on the selected fast mechanical switch. Without any driving voltage, its conducting resistance from B terminal to A terminal is 418.5uΩ. With 5V constant ON driving voltage, its conducting resistance changes to 358.4uΩ which verify the proposed driving strategy. According to equation 5.6, it can save a little power on the main current path under 190A load status. However, this reduced resistance is not always stable as this low value and consume more power on driving circuit under most load status which is smaller than 190A. Besides, it increases the complexity of driver circuit design requirement, so the benefit of constant on driving voltage cannot beat the extra effort on proposed turn on strategy.

Figure 5.27 Conducting resistance on Mechanical relay without driving voltage and with 5V driving voltage

5.5.3 Transient of current commutation test

The current commutation is a transient process occurring in only several microseconds. Some interesting phenomena exist in this short process. 20A to 200A is tested to examine the selected mechanical switch and shows the transient performance.

The first interesting phenomenon is the pre-commutation. Figure 5.28 shows the related waveform. This phenomenon is neglected in previous current delay tests since the time scale is in milliseconds and this transient occurs in microseconds time scale.

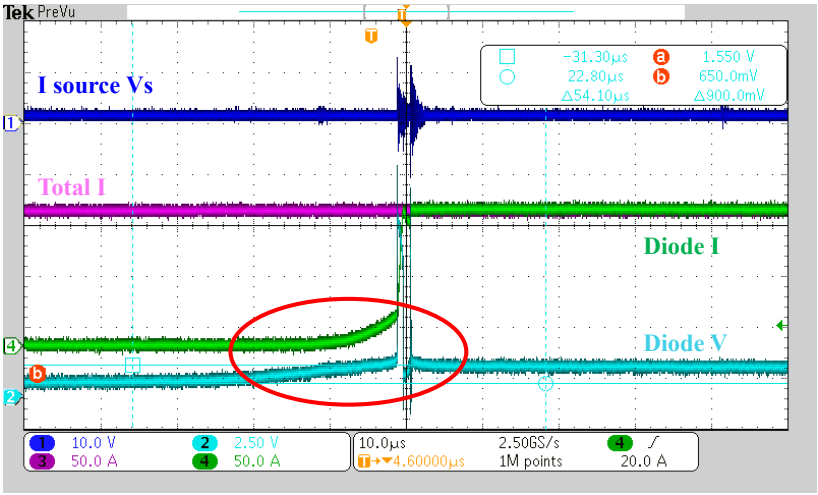


Figure 5.28 Phenomenon of pre-commutation

The current starts to increase slowly before the large current commutation with about 20us in advance and also make the diode voltage increase. The reason lies in the increasing contact resistance on the mechanical switch. When there is the repulsion force but no arc is generated, there is no arc voltage help to commutate dominant current.

The second interesting phenomenon is the current commutation transient process. In figure 5.29, this process is shown with 200A current commutation. This transient waveform gives the explanation that the process is not a one-time commutation. The voltage rises to 12.8V at the beginning and keeps with 7V to 5V due to the current commutation di/dt at a high value. This is mainly because of the influence of the loop inductance. Once the current commutated into the diode, the current between mechanical switch and diode starts to change primarily due to the weak force balance among permanent magnetic, metallic frame spring and repulsion electromagnetic force from the coil. All of them would vary with the air gap.

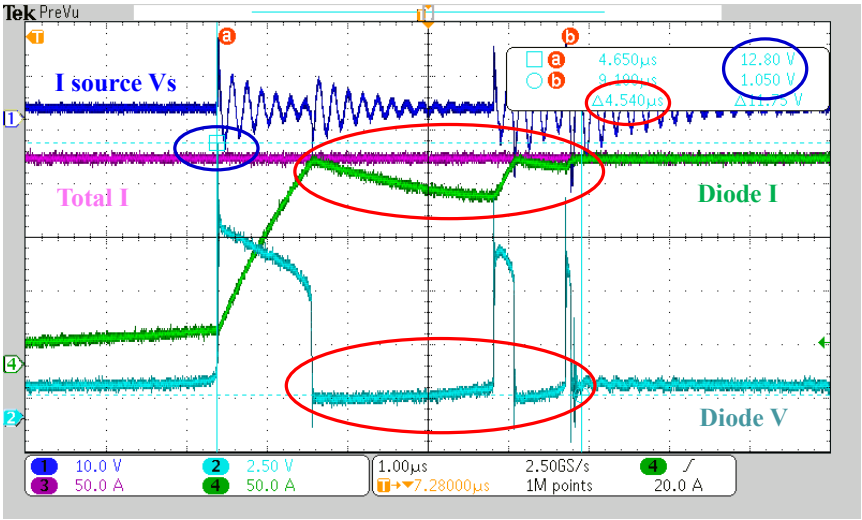


Figure 5.29 Transient process of current commutation

This transient current commutation repeats 2-3 times so that a large current commutated into solid state device circuit in about 4.54 us.

5.6 Conclusion and Summary

In sum, a hybrid branch circuit breaker is proposed, analyzed and partially tested for 380V DC distribution system. Several novel and interesting features are proposed and verified:

1. The hybrid branch circuit is more suitable for high current application compared with the pure solid-state circuit breaker since its advantages on contact resistance, volume and cost of selected mechanical switch.

2. The hybrid branch circuit breaker can be used for bi-directional application with only single solid-state device. The paralleled solid-state circuit does not need to work on the normally-on state to sustain the large thermal stress for high current. The most important characteristic of the paralleled solid-state device is the turn-off capability during high saturation current stress.

3. The criteria of the fast-mechanical switch are defined and explained. A mechanical switch with low driving power consumption is selected for the purpose of 380V/200A hybrid circuit breaker. The operation state and mode are investigated along with force balancing.

4. A novel driving strategy is proposed for selecting a faster mechanical switch in order to accelerate the trip speed and reduce the contact resistance. The test results show that the speed is achieved into 1.6ms from original 5ms. The active trip is verified with 200A and 50V driving voltage. The tripping speed can be about 1.6ms with little driving power consumption.

5. The transient process of current commutation is displayed and studied. The influence of loop inductance is very important and needs to be carefully considered for circuit design.

CHAPTER 6

Summary and Future Work

6.1 Summary

In general, the presented research focused on investigating the protection strategy implemented with novel solid-state circuit breakers. Three different design are introduced for various current rating.

For single load under 2kW, the hot-swappable outlet is proposed with zero standby power consumption. It is particularly mandatory for DC distribution system due to the severe arcing phenomenon in the time of disconnection. The innovative mechanical scheme with energize pad and high ratio buck converter makes the plug need no change from traditional system. Complementary dual threshold over current protection and over temperature protection enhance the reliability and supply extra circuit breaker features.

For multiple loads in a cabinet, a node solid state circuit breaker with paralleled devices is introduced. The interleaved hiccup startup strategy is proposed for dealing with the current diverge at the time of saturation current sharing to protect the solid-state devices with averaged thermal stress. Besides, the novel junction temperature monitoring scheme is analyzed to sense the junction temperature in real-time with high accuracy to implement the over temperature protection without extra T sensor and enhance the device reliability. Moreover, the high impedance fault protection is introduced for 3 wires 2 phase system for system safety improvement.

For high current (200A) application in 380V DC system, the hybrid circuit breaker is designed to replace the solid-state circuit breaker because of the cost, volume and loss limit in solid state device. The criteria of the fast-mechanical switch in the hybrid circuit breaker are investigated and defined. The novel driving strategy is proposed and tested for accelerating the trip speed based on the mechanism analysis. The transient current commutation with the paralleled diode is tested and studied.

Figure 6.1 shows the conclusion of three hardware development for 380V DC microgrid distribution. The fast tripping time and high-power density beat other state of art technology and traditional mechanical MCCB for DC application. Another high current fast mechanical switch which was also developed in FREEDM system center can be used to replace DC system main switch. [60]

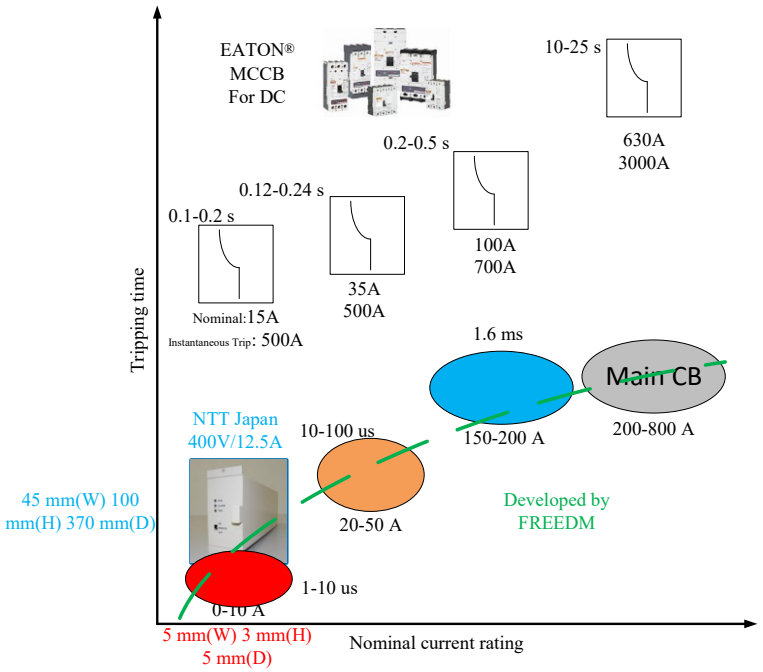


Figure 6.1 Conclusion of 3 different hardware development vs. traditional MCCB for DC application

6.2 Future Work

The future work of this research subject includes following items:

1. The device analysis and evaluation should be improved by considering more scenarios. The Si IGBT for hybrid branch circuit breaker should be analyzed and studied with evaluating the time delay.
2. The Finite Element Analysis (FEA) can be applied to fast mechanical switch to improve its driven strategy in magnetic field analysis. The modeling and analysis of mechanical switch in hybrid circuit breaker can also improve the power density with enhanced fast-mechanical switch design.
3. The components and system level modeling should be analyzed and established for all three developed hardware to evaluate the coordination control and protection in microgrid power system level for all possible scenarios.

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