ABSTRACT

YEH, YI-SHIN. Distributed Beamforming Phased Arrays for Millimeter-Wave Radio. (Under the direction of Brian A. Floyd.)

Future cellular systems should support higher capacity along with faster peak- and edge-data rates. The available bandwidth and reduced wavelength at Ka band (27 to 40 GHz) enable high-throughput communications for fifth-generation (5G) millimeter-wave (mm-wave) networks using compact antenna arrays. In particular, the 28-GHz frequency band is an attractive candidate for 5G cellular networks due to favorable channel characteristics and available spectrum. Link budgets for 28-GHz phased-array transceivers suggest single moderate beamforming for user equipment (one to eight elements, single-beam) and multiple stronger beamforming at the basestation (up to hundreds of elements, multi-beam). As such, fundamental research exploring optimum radio solutions for 5G mm-wave systems at 28 GHz to achieve wide-bandwidth and highly scalable phased-array architectures is needed. Multi-beam support is desirable to service multiple users concurrently with less hardware overhead for future 5G basestations. To enable scalable, wideband, and multi-beam phased arrays, this work investigates and demonstrates novel phased-array beamforming architectures using 130-nm SiGe BiCMOS technology.

First of all, a novel 28-GHz four-element receive beamformer which employs scalar-only weighting functions within each front-end and global quadrature combining is proposed to realize a dual-beam beamforming concept I refer to as “dual-vector distributed beamforming.” Such scalar front-ends can be both area-efficient and wide bandwidth. Differential LNAs and dual-vector variable-gain amplifiers are used to realize each front-end in a compact area of 0.3 mm$^2$. Across four-bit phase settings, each array element achieves a measured 5.1 to 7 dB noise figure, -16.8 to -13.8 dBm input-referred 1-dB compression point, and -10.5 to -8.9 dBm input-referred third-order intercept point. The average gain per element is 10.5 dB at 29.7 GHz, whereas the 3-dB bandwidth is 24.5% (26.5 to 33.9 GHz). Root-mean-squared (RMS) gain and phase errors are less than 0.6 dB and 5.4 degrees across 28-32 GHz respectively, and all four elements provide well-matched and well-isolated
responses. Power consumption is 136 mW per element, equaling 546 mW for the four-element array. With comparison of other RF phased-array receiver front-ends, this work achieves among the lowest area and among the highest fractional bandwidths; however, as can be expected, active phase shifter topologies will consume more power over passive approaches.

Secondly, a novel 28-GHz transceiver array using dual-vector distributed beamforming with a series-fed network is proposed and demonstrated in 130-nm SiGe BiCMOS technology. The dual-vector transceiver array allows the sharing of the combiner between transmit and receive front-ends without switching through use of a series-fed combiner or splitter network. Once again, the dual-vector distributed array employs scalar-only weighting functions within each front end and a global quadrature function, enabling a small footprint for each element and supporting four simultaneous beams. The series feed network also reduces size considerably. In particular, the four-element transceiver array occupies the same area as my previous four-element receive-only array, thereby doubling the integration density. In measurement, each receive front end achieves 8.7 to 11.5 dB gain, 4.5 to 6.9 dB noise figure, -25.4 to -18.4 dBm input 1-dB compression point across 24-28 GHz. RMS gain and phase errors are less than 0.5 dB and 2.1° across 24-28 GHz respectively. Each transmit front end achieves 9.4 to 14.3 dB gain, and 5.5 to 10.6 dBm output 1-dB compression point. RMS gain and phase errors are less than 0.4 dB and 4.2° across 24-28 GHz respectively. The four-element transceiver array occupies 2.9 mm² area and consumes 1.08 W in transmit mode and 0.68 W in receive mode. Compared to the other RF phased-array TRX front-ends, our distributed beamformer achieves the lowest front-end area and array area with comparable RF performances at Ka band; however, the DC power is higher than the passive approaches.

Thirdly, a new 28-GHz hybrid dual-vector distributed phased-array transceiver using mixer-based beamforming is proposed and demonstrated in 130-nm SiGe BiCMOS technology. The hybrid multi-beam transceiver array employs quadrature up- and down-conversion mixers to provide global vector interpolation, allowing the passive hybrid couplers to be eliminated in the signal path and leveraging the quadrature accuracy which is already provided by the local oscillator (LO) network. This can theoretically improve the bandwidth over which quadrature accuracy is maintained. A
A novel distributed active poly-phase filter is proposed to achieve wideband quadrature accuracy in the LO path. Furthermore, the hybrid transceiver array includes on-chip built-in self-test (BIST) networks to enable array-level and element-level test capabilities. In measurement, each receive front end achieves 8.6-dB gain at 29.8 GHz and a 24.5% 3-dB bandwidth (25.2-32.5 GHz), 5.7 to 7.5 dB noise figure, and -18.5 to -16.5 dBm input 1-dB compression point at 28 GHz. RMS gain and phase errors are less than 0.1 dB and 0.8° at 28 GHz respectively. Each transmit front end achieves 18.1 dB at 29.9 GHz, and a 24% 3-dB bandwidth (25.6 to 32.8 GHz), 13.8 to 14.8 dBm output 1-dB compression point, and 17.1 to 18.2 dBm output saturate power at 28 GHz. RMS gain and phase errors are less than 1 dB and 5.6° across 14.1 to 35.4 GHz respectively. The four-element transceiver array occupies 2.9 mm² area and consumes 1.22 W in transmit mode and 0.51 W in receive mode. Compared to the other RF phased-array TRX front-ends, our distributed beamformer achieves the lowest front-end area and array area with comparable RF performances at Ka band; however, the DC power is higher than the passive approaches.

Finally, in addition to the complexities associated with realizing phased arrays, there are distinct challenges associated with mm-wave systems that require high-quality and power-efficient local-oscillator (LO) signals. To obtain low phase noise and wide frequency tuning range, often lower-frequency oscillators are used within the synthesizer and the output signals are then multiplied up to the desired frequency. Higher multiplication ratios allow the oscillator and the prescaler within the phase-locked loop (PLL) to operate at lower frequencies, with multiplication ratios of two, three, and four being common. In this work, a novel, power-efficient topology for a frequency quadrupler is proposed and demonstrated. The circuit achieves high power efficiency at fourth-harmonic output power and high rejection of other undesired output harmonics, known as spurs. Multiple variations of the quadrupler are studied in multiple SiGe BiCMOS technologies for 60 and 80 GHz output frequencies and for a variety of differential and quadrature input excitation approaches. One representative quadrature-balanced result operating at 80 GHz output frequency achieves 11.2-dBm output power, 5.8-% conversion efficiency, and 30-dB harmonic suppression. Compared to the other recently-published quadruplers, this work achieves compelling output power, efficiency,
harmonic suppression, and bandwidth performance.
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by
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DEDICATION

To my grandparents, Meng Yeh and Ching-Zhu Chen,
and
my parents, Chia-Yu Yeh and Ching-Yi Chang,
and
my sister, Ren-Yu Yeh.
Yi-Shin Yeh was born and raised in Tapei City, Taiwan, Republic of China. In 2007, he completed his Bachelor of Science degree in Electronic Engineering Department in Fu Jen Catholic University in New Taipei City, Taiwan. After the graduation, he took the mandatory military service in Air Force, in Taiwan. After spending some time in industry, he joined Stony Brook University as a Masters student in Electrical and Computer Engineering department in 2009. He received his Master of Science degree under the supervision of Professor Milutin Stanacevic in 2011.

Since 2011, he joined Professor Brian Floyd's research group as a doctoral student and has been working in Integrated Circuits and Systems Lab at North Carolina State University (iNCS2). His research interests focus on the RF and analog integrated circuit design and the mm-wave phased-array transceiver for broadband and high data-rate wireless communication.

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1.1 Millimeter-Wave Wireless Communication

Future cellular systems should support higher capacity along with faster peak- and edge-data rates. This need has the potential to be partially met by shifting toward millimeter-wave (mm-wave) frequencies (20–300 GHz) [And14; PK11]. In particular, the 28-GHz frequency band is an attractive candidate for fifth-generation (5G) cellular networks due to favorable channel characteristics and available spectrum [Ran14]. As the transistor cutoff frequencies are greater than 200 GHz for 45-nm CMOS SOI or 130-nm SiGe BiCMOS, highly-integrated and high-performance hardware can be readily realized in silicon [Flo05; Doa05; Nat11; Sar14].

As the carrier frequencies move to the mm-wave region, however, the path loss increases. In
addition, smaller wavelength at mm-wave frequencies reduces the size and effective aperture of the antenna. As a result, the directivity can be improved by the factor of $N$ (numbers of antennas) using antenna arrays at the higher frequencies. However, the beam-width of the radiation pattern becomes narrower as the numbers of the antenna elements increase. To achieve complete mm-wave mobility, beam steering mechanisms are required, usually in the form of phased-arrays. Link budgets for 28-GHz phased-array transceivers [PK11] suggest single moderate beamforming for user equipment (one to eight elements) and multiple stronger beamforming at the basestation (up to hundreds of elements). To understand phased-array transmitter and receiver performance requirements, uplink and downlink budgets are summarized below for 28-GHz operation.

### 1.2 Millimeter-Wave Link Budget Analysis

Wide channel bandwidth at 28-GHz band [PK11; Kha12] enables high capacity as shown by the Shannon's theorem,

$$ C = BW \times \log_2(1 + SNR) = BW \times \log_2\left(1 + \frac{P_{signal}}{P_{noise}}\right) $$

(1.1)

where $BW$ is the channel bandwidth, $SNR$ is the minimum signal-to-noise ratio at the receiver output, $P_{signal}$ is the signal power at the receiver output, and $P_{noise}$ is the total noise power at the receiver output. Note, this is the maximum theoretical data-rate that can be achieved. As the carrier frequency increases from 1 to 28 GHz with fixed fractional bandwidth of 20 %, the bandwidth increases from 200 MHz to 5.6 GHz; however, as the carrier frequencies move to the mm-wave region, the path loss increases due to radiation in the different aperture of an isotropic antenna. The signal path loss, $L_{FS}$, between the feed points of two isotropic antennas in free space can be defined as,

$$ L_{FS} = \left(\frac{4\pi d}{\lambda}\right)^2 $$

(1.2)
where $d$ is the link distance, and $\lambda$ is the wavelength. Therefore, as frequencies increase from 1 to 28 GHz, the path loss, $L$, increases from 92.4 to 121.4 dB with 1 km link distance. This effect of reducing the effective aperture size of the antenna can be defined as follows:

$$A_{\text{eff}} = \frac{\lambda^2}{4\pi} G_A$$

where $A_{\text{eff}}$ is the effective aperture size of the antenna, and $G_A$ is the antenna gain; however, with shorter wavelengths, more antennas can be packed into the same antenna aperture area as the low-frequency single antenna [PK11; Boe14]. As a result, implementing antenna arrays improves the directivity by the factor of $N$ (numbers of antennas) at the higher frequencies.

![Figure 1.1](image)

**Figure 1.1** 28-GHz (a) uplink and (b) downlink link budgets
1.2.1 Effective Isotropic Radiated Power Enhancement in Transmitter Array

First, the number of receive (RX) and transmit (TX) antennas, $N_{RX}$ and $N_{TX}$, need to be determined in the array for the uplink and downlink at 28-GHz basestation, as illustrated in Fig. 1.1. Fig. 1.1 (a) shows the 28-GHz uplink between TX array at an user equipment and RX array at the basestation and Fig. 1.1 (b) shows the 28-GHz downlink between RX array at the user equipment and TX array at the basestation. A link budget analysis for a 28-GHz millimeter-wave mobile broadband (MMB) system based on [PK11; Kha12] shows a minimum of 1 Gb/s for the mobile uplink and 4 Gb/s for the downlink over 0.25 km distance within a 500 MHz bandwidth. With the required minimum signal-to-noise ratio ($SNR$) to achieve desired data rate, the link budget for the power level at RX derived from Friis transmission equation assuming polarization and reflection match,

$$ P_{N,RX} = P_{N,TX} + G_{N,TX} + G_{N,RX} - L_{FS} - L_{M} [dBm] $$

(1.4)

where $P_{N,RX}$ is the total received power by RX antenna array, $P_{N,TX}$ is the total output power generated by the transmitters, $G_{N,TX}$ is the total antenna gain for the transmitters, $G_{N,RX}$ is the total antenna gain for the receivers, $L_{FS}$ is the propagation loss in the free space, and $L_{M}$ is the loss of the link margin for any other losses. In addition, the effective isotropic radiated power ($EIRP$) from a transmitter array with $N_{TX}$ is given by [VG10],

$$ EIRP = P_{N,TX} \cdot G_{N,TX} = (N_{TX} P_{1,TX}) \cdot (N_{TX} G_{1,TX}) [W] $$

(1.5)

where $N_{TX}$ is the numbers of the transmitter, $P_{1,TX}$ is the output power from each transmitter, and $G_{1,TX}$ is the antenna gain of each antenna for the each transmitter. To calculate $EIRP$ in dBm, equation (1.5) can be rewritten as,

$$ EIRP = P_{1,TX} + G_{1,TX} + 20 \cdot \log(N_{TX}) [dBm] $$

(1.6)
Compared to a single-element transmitter at the same frequency, equation (1.5) shows that the EIRP of the transmitter array is improved by a factor of $N_{TX}^2$. As the number, $N_{TX}$, of transmitter elements increases from 2 to 256, the EIRP is improved from 6 to 48 dBm.

### 1.2.2 Input Sensitivity Improvement in Receiver Array

As a result, the link budget for the received power of each receiver derived from equation (1.4) and (1.6) can be written as,

$$ P_{N,RX} = P_{1,TX} + G_{1,TX} + 20 \cdot \log(N_{TX}) + G_{1,RX} + 10 \cdot \log(N_{RX}) - L_{FS} - L_M \ [\text{dBm}] \quad (1.7) $$

$$ P_{1,RX} = P_{N,RX} - 10 \cdot \log(N_{RX}) \ [\text{dBm}] \quad (1.8) $$

where $P_{1,RX}$ is the received power of each receiver, $G_{1,RX}$ is the antenna gain of each antenna for the each transmitter, and $N_{RX}$ is the numbers of the receivers. Compared to a single-element receiver at the same frequency, equation (1.8) shows that the input sensitivity of each receiver is reduced by a factor of $N_{RX}$. Note that, $P_{N,RX}$ is the total received power by the receiver array to meet minimum SNR to achieve the desired channel capacity, $C$, and $P_{N,RX}$ has to meet the input sensitivity of the receiver array which can be shown,

$$ P_{N,RX} \geq -174 + 10 \cdot \log(BW) + NF_{N,RX} + SNR_{N,RX} \ [\text{dBm}] \quad (1.9) $$

where -174 dBm equals the thermal noise in the unit of dBm-per-Hz, $NF_{N,RX}$ the noise figure of the receiver array, and $SNR_{N,RX}$ is the minimum required SNR at the output of the receiver array.

Link budgets for 28-GHz phased-array transceivers [PK11] suggest single moderate beamforming for user equipment (one to eight elements) and multiple stronger beamforming at the base stations (up to hundreds of elements). To understand phased-array transmitter and receiver performance requirements, uplink and downlink budgets are summarized in Table 1.1 and 1.2 for 28-GHz opera-
tion. The uplink and downlink link budgets demonstrate that 256- receive and transmit elements at the basestation are needed to communicate with four-element transmit and receive arrays at the user equipment for a 1-km link range supporting a data rate greater than 2.77 Gb/s. As such, fundamental research exploring optimum radio solutions for 5G mm-wave systems at 28 GHz to achieve wide-bandwidth and highly scalable phased-array architectures is needed.

1.3 Phased-Array Basics: Principle of Operations

The directivity can be improved by implementing antenna arrays at the higher frequencies; however, the beam-width of the radiation pattern becomes narrower as the number of the antenna elements is increased. To achieve flexible mm-wave mobility, beam steering mechanisms are required. Compared to mechanical steering, phased arrays became an attractive alternative solution to provide fast scanning and directive beams. The combining node at the phased-array output is used to sum phased-shifted signals from multiple antenna elements to create a desired beam pattern. Furthermore, the direction and shape of the beam can be electronically scanned by varying the phase and amplitude shifts within each element.

The operating principle of a linear $N$-element phased-array receiver with a phase shifter within each element and a summing network at the array output is illustrated in Fig. 1.2. In the array with $N$ elements spaced a distant $d$ apart, incident waves from the far-zone field with an incident angle $\theta$ arrives at the $N^{th}$ element with a time delay. At the carrier frequency, this time delay between each adjacent element can be represented as a phase difference, $\Delta \psi$, described by the following:

$$\Delta \psi = \kappa d \sin(\theta) = \frac{2\pi d \sin(\theta)}{\lambda}$$

(1.10)

where $\kappa$ equals $2\pi/\lambda$, $d$ is the physical distance between two adjacent antenna, and $\theta$ is the elevation angle relative to broadside. The received signals experience a desired phase shift $\alpha_n$ within each
Figure 1.2 Principle of operations of a linear $N$-element phased-array receiver with a phase shifter within each element and a summing network at the array output

Element and the output signals from each element are combined through a summing network. The combined output signal of the $N$-element array can be represented as the product of the field of a single element pattern, $S_{\text{element}}(\theta)$, and the array factor, $F(\theta)$, of the array [Bal05]. This is referred to as pattern multiplication for an array of identical elements.

The combined output signal, $S_{\text{total}}(\theta)$, of the array response can be described by the following:

$$S_{\text{total}}(\theta) = S_{\text{element}}(\theta) \times F(\theta) = S_{\text{element}}(\theta) \times \sum_{n=1}^{N} a_n e^{j[(n-1)kd\sin(\theta) - \alpha_n]}$$  \hspace{1cm} (1.11)$$

where $a_n$ is the amplitude shift per element, and $\alpha_n$ is the phase shift per element. Let $\psi_n = nkd\sin(\theta) - \alpha_n$ so that the array factor, $F(\theta)$, of the array can be seen that,

$$F(\theta) = \sum_{n=1}^{N} a_n e^{j[(n-1)kd\sin(\theta) - \alpha_n]} = a_n \left[ \frac{\sin(\frac{N}{2} \psi_n)}{\sin(\frac{1}{2} \psi_n)} \right]$$  \hspace{1cm} (1.12)$$

To find the nulls of the array factor where the signals from particular directions add destructively,
(1.12) is set equal to zero. That is,

\[
\sin \left( \frac{N}{2} \psi_n \right) = 0 \Rightarrow \frac{N}{2} \psi_n = \pm n \pi, \ n = 1, 2, 3, \ldots; \ n \neq N, 2N, 3N, \ldots
\]  

(1.13)

To find the maximum value of the array factor where signals from a particular direction add constructively at the array output, the maximum value of (1.12) occurs when

\[
\sin \left( \frac{1}{2} \psi_n \right) = 0 \Rightarrow \frac{1}{2} \psi_n = \pm m \pi, \ m = 0, 1, 2, 3, \ldots
\]  

(1.14)

Thus the number of nulls and the maximum values that can exist will be a function of the antenna distance \( d \) and the phase shift \( \alpha_n \) within an element. As the antenna distance \( d \) is too close, e.g. \( d < \lambda/2 \), strong coupling is introduced between each antenna; however, larger distances, \( d > \lambda/2 \), lead to undesired grating lobes in the pattern. Therefore, \( d = \lambda/2 \) is usually a good compromise for two adjacent antenna distance, leading to,

\[
\psi_n = nkd \sin(\theta) - \alpha_n \Rightarrow \psi_n = n \pi \sin(\theta) - \alpha_n
\]  

(1.15)

Beam steering can be accomplished by electronically varying the phase shift \( \alpha_n \) within an element. To steer the beam to \( \theta \), the range of the phase shift \( \alpha_n \) is described by

\[
\alpha_n = n \pi \sin(\theta) \Rightarrow \alpha_n = \pm n \pi
\]  

(1.16)

Thus, the phase shifter in each element needs to be designed to cover 0 to \( 2\pi \) phase tuning range so that the phased array can provide the maximum gain in a particular direction. Not only element phase shifts are used to steer the pattern, but also element amplitudes are used to shape the pattern, something taper in a form of an amplitude.

Fig. 1.3 plots the normalized pattern of \( S_{total}(\theta) \) as a function of the angle \( \theta \) of arrival incidence.
for a 16-element \((N = 16)\) array to steer \(\theta\) the main lobe from -45 to +45° with \(d = \lambda/2\). The above concept can be applied to the phased-array transmitter with the phase shifter within each element and an input in-phase distribution networks; however, the transmitted signals are combined in the space. The maximum beam can be formed in the angular direction where the signals are added constructively.

![Normalized Patterns](image)

**Figure 1.3** 16-element normalized pattern with uniformly spaced values of \(\theta\) (Step size = 45°)

### 1.4 Challenges and Research Objectives for Millimeter-Wave Phased-Array Systems

For future 5G cellular systems, shifting toward millimeter-wave frequencies to explore available spectrum at the 28-GHz frequency band improves the date rates of wireless communication. The path loss at 28 GHz can be overcome by implementing antenna arrays to realize high antenna gain. In addition, implementing phased array allows beam steering to achieve flexible mm-wave mobility.
Multiple design challenges and tradeoffs still exist for the millimeter-wave phased-array system, and these are described below.

### 1.4.1 Challenges and Research Objectives

Key research objectives which need to be addressed are as follow:

- **Objective 1: Investigate scalable phased-array architectures which consume low area and low DC power.** In the previous section, the link budget analysis in Tables 1.1 and 1.2 suggests that 256- receive and transmit elements at the 5G base station are needed to communicate with four-element transmit and receive arrays at the user equipment for a 1-km 2.77-Gb/s link range. As such, the first research objective is to explore optimum radio solutions for 5G mm-wave systems. Low-area and scalable phased-array architectures allow multiple sub-arrays to be implemented together in a cost-effective manner.

- **Objective 2: Investigate hybrid beamforming architectures which provide multi-beam support.** Multiple beams will be required to service multiple users concurrently for future 5G base station. While this could be supported by pure digital beamforming in a massive multi-input multi-output (MIMO) system, the power consumption and back-end digital processing associated with hundreds of data converters each supporting up to a gigahertz of bandwidth is prohibitive [Pug16]. RF beamforming is both area- and power- efficient; however, the traditional RF beamforming architecture only supports a single-input, single-output (SISO) system. As such it is anticipated that systems may use a hybrid approach composed of multiple sub-arrays employing analog beamforming, which are then connected to radio-frequency (RF) transceiver chains which can then be controlled digitally [Gao16]. As such, the second research objective is to explore a hybrid beamforming architecture, in which each sub-array can support multiple simultaneous beams.

- **Objective 3: Explore wideband phased-array architectures which support high-date rate
and multi-band operations. Several bands for future 5G cellular system have been considered and proposed, including 27.5 to 28.35-GHz and 38.6 to 40-GHz frequency bands[And14; PK11]. A mobile millimeter-wave broadband (MMB) system for 5G communications has been presented in [PK11] for development of high-capacity, high-throughput small cells for mobile broadband. For such 5G basestations, a single millimeter-wave phased-array system should achieve wideband performance for high-data rate and multi-band operation. As such, the third research objective is to explore broadband phased-array architectures which support multi-band operation using a single hardware.

- **Objective 4: Develop calibration methods for the proposed arrays.** High phase and amplitude resolution and accuracy not only reduces the main-beam pointing error but also improves side-lobe reduction [Sad17]. The calibration method is important for any type of phased array. As such, the fourth research objective is to explore calibration techniques for the proposed arrays to achieve low phase error and low amplitude error.

- **Objective 5: Investigate a new topology for millimeter-wave frequency multipliers to achieve high power efficiency and high harmonic suppression in millimeter-wave LO systems.** In addition to the complexities associated with realizing phased arrays, there are distinct challenges associated with millimeter-wave systems, in that they require high-quality and power-efficient local-oscillator signals. To obtain low phase noise and wide frequency tuning range, often lower-frequency oscillators are used within the synthesizer and the output signals are then multiplied up to the desired frequency[Flo08]. Higher multiplication ratios allow the oscillator and the prescaler to operate at lower frequencies, with multiplication factors of two, three, and four being common. These multipliers, in turn, must exhibit wideband and robust operation, provide high output power at the desired harmonic and suppress unwanted harmonics all the while consuming minimal DC power. As such, the fifth research objective is to explore millimeter-wave multipliers which achieve high power efficiency and high harmonic
suppression.

1.4.2 Contributions of This Work

This Ph.D. work advances the-state-of-the-art in phased-array transceivers with four key contributions that are summarized below.

• **Contribution 1: A phased-array receiver with dual-vector distributed beamforming.** The first research contribution is the introduction of a new beamforming architecture for phased arrays which employs scalar-only weighting functions within each front-end and global quadrature combining. We refer to this new type of beamforming concept as “dual-vector distributed beamforming.” Such scalar front-ends can be both area-efficient and wide bandwidth, and the global quadrature combiner outputs can provide dual-beams which could be useful for mm-wave base stations. This concept is demonstrated though the realization of the phased-array receiver with dual-vector distributed beamforming (DVDB).

• **Contribution 2: A phased-array transceiver with series-fed dual-vector distributed beamforming.** The second research contribution is the extension and modification of the DVDB concept to a transmit and receive structure which shares a compact series-fed network and support up to four simultaneous beams. The concept is demonstrated through the realization of the phased-array transceiver with series-fed dual-vector distributed beamforming.

• **Contribution 3: A mixer-based hybrid phased-array transceiver with dual-vector distributed beamforming and built-in self-test network.** The third research contribution is the introduction of a hybrid mixer-based transceiver architecture which enables wideband transceiver operation. In this approach, beamforming is realized at baseband, allowing the global quadrature function to be leverage by the LO signals and downconversion mixers. This concept is demonstrated through the realization of the mixer-based hybrid phased-array transceiver with dual-vector distributed beamforming.
• Contribution 4: A power-efficient frequency multiplier with high harmonic suppression in millimeter-wave local-oscillator generation and distribution. The fourth research contribution is the introduction of a novel architecture for frequency quadraplers which achieve high power efficiency and high rejection of other undesired output harmonics. This can be used to achieve lower power consumption and higher spectral quality in the LO path of mm-wave systems.

1.5 Organization

The dissertation is organized as follows. Chapter 2 presents a novel dual-vector distributed beamforming architecture for phased arrays which employs scalar-only weighting functions within each front-end and global quadrature combining. The chapter begins with studies and comparisons for different architectures of RX beamformers and different topologies of RF phase shifters. A dual-beamforming thoery is introduced for this new architecture. The details of the circuit implementation are then presented for each block in the system. A novel dual-vector VGA is presented to show the necessary pre-distortion and current-steering functions. A four-element 28-GHz phased-array receiver is implemented in GlobalFoundries (GF) 8HP 130-nm SiGe BiCMOS technology. The details of calibration methods and measured results are shown at the end of this chapter to illustrate the capability of the architecture.

Chapter 3 presents a novel phased-array transceiver (TRX) which implements series-fed networks along with dual-vector distributed beamforming. The chapter begins with studies and comparisons for different architectures of TRX phased arrays. A multi- beamforming theory is introduced for this new architecture. The details of the circuit implementation are then presented for each block in the system. A novel transformer-based transmit/receive- (T/R-) switch is presented which achieves a the compact layout and fast switching time. The transceiver front-end with and without T/R- switch is shown and compared with one another. A four-element 28-GHz phased-array
transceiver is implemented in GlobalFoundries (GF) 8HP 130-nm SiGe BiCMOS technology. The details of calibration methods and measured results are shown at the end of this chapter to illustrate the capability of the architecture.

Chapter 4 presents a novel hybrid phased-array transceiver which employs quadrature mixer-based dual-vector distributed beamforming. A mixer-based beamforming theory is introduced for this architecture. The details of the circuit implementation are presented for each block in the system. A built-in self-test (BIST) network is also included in the system. A four-element 28-GHz hybrid phased-array transceiver is implemented in GlobalFoundries (GF) 8HP 130-nm SiGe BiCMOS technology. The details of calibration methods and measured results are shown at the end of this chapter.

Chapter 5 presents a novel millimeter-wave frequency multiplier which employs self-mixing phased-controlled push-push (PCPP) technique with quadrature excitation. A self-mixing PCPP theory with balanced and quadrature excitation is introduced for this topology. The details of the circuit implementation are then presented, including multiple approaches to quadrature excitation. Multiple frequency multipliers have been implemented in GlobalFoundries (GF) 8HP/8XP/9HP SiGe BiCMOS technologies. The details of the measured results are shown at the end of this chapter. Finally, the conclusion and the future works are summarized in the Chapter 6.
Table 1.1 Summary of RX Array Uplink Link Budget at 28-GHz Base-station illustrating in Fig. 1.1 (a)

<table>
<thead>
<tr>
<th><strong>Transmitter array at user equipment</strong></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Numbers of TX elements ( (N_{TX}) )</td>
<td>4</td>
<td></td>
</tr>
<tr>
<td>TX array factor ( (20 \cdot \log(N_{TX})) )</td>
<td>12 dB</td>
<td></td>
</tr>
<tr>
<td>TX ( oP_{1\text{dB}} ) per element</td>
<td>16.9 dBm</td>
<td></td>
</tr>
<tr>
<td>TX output power at 7-dB back out per element ( (P_{1_{TX}}) )</td>
<td>9.9 dBm</td>
<td></td>
</tr>
<tr>
<td>TX antenna gain per element ( (G_{1_{TX}}) )</td>
<td>6 dBi</td>
<td></td>
</tr>
<tr>
<td>TX array EIRP ( (P_{1_{TX}}+G_{1_{TX}}+20\log(N_{TX})) )</td>
<td>28 dBm</td>
<td></td>
</tr>
<tr>
<td>Distance ( (d) )</td>
<td>1 km</td>
<td></td>
</tr>
<tr>
<td>Propagation loss ( (L_{FS}) )</td>
<td>121.4 dB</td>
<td></td>
</tr>
<tr>
<td>Loss margin ( (L_M) )</td>
<td>20 dB</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>Receiver array at basestation</strong></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Data rate ( (C) )</td>
<td>2.77 Gb/s [PK11]</td>
<td></td>
</tr>
<tr>
<td>( SNR_{N, RX} )</td>
<td>12.7 dB [PK11]</td>
<td></td>
</tr>
<tr>
<td>Bandwidth ( (BW) )</td>
<td>1 GHz</td>
<td></td>
</tr>
<tr>
<td>RX-array noise figure ( (N_{F_{N, RX}}) )</td>
<td>6 dB</td>
<td></td>
</tr>
<tr>
<td>Thermal PSD</td>
<td>-174 dBm/Hz</td>
<td></td>
</tr>
<tr>
<td>RX-array input sensitivity ( (P_{N_{RX}}) )</td>
<td>-65.3 dBm</td>
<td></td>
</tr>
<tr>
<td>RX antenna gain per element ( (G_{1_{RX}}) )</td>
<td>24 dBi</td>
<td></td>
</tr>
<tr>
<td>Required RX array factor ( (10 \cdot \log(N_{RX})) )</td>
<td>24.1 dB</td>
<td></td>
</tr>
<tr>
<td>**Required numbers of RX elements ( (N_{RX}) )</td>
<td>256</td>
<td></td>
</tr>
</tbody>
</table>
Table 1.2 Summary of TX Array Downlink Link Budget at 28-GHz Base-station illustrating in Fig. 1.1 (b)

<table>
<thead>
<tr>
<th><strong>Receiver array at user equipment</strong></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Numbers of RX elements (N_{RX})</td>
<td>4</td>
</tr>
<tr>
<td>RX array factor (10 \cdot \log(N_{RX}))</td>
<td>6 dB</td>
</tr>
<tr>
<td>Data rate (C)</td>
<td>2.77 Gb/s [PK11]</td>
</tr>
<tr>
<td>(SNR_{N,RX})</td>
<td>12.66 dB [PK11]</td>
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<tr>
<td>Bandwidth (BW)</td>
<td>1 GHz</td>
</tr>
<tr>
<td>RX-array noise figure (N_{F,RX})</td>
<td>10 dB</td>
</tr>
<tr>
<td>Thermal PSD</td>
<td>-174 dBm/Hz</td>
</tr>
<tr>
<td>RX-array input sensitivity (P_{N,RX})</td>
<td>-61.3 dBm</td>
</tr>
<tr>
<td>RX antenna gain per element (G_{1,RX})</td>
<td>6 dBi</td>
</tr>
<tr>
<td>Distance (d)</td>
<td>1 km</td>
</tr>
<tr>
<td>Propagation loss (L_{FS})</td>
<td>121.4 dB</td>
</tr>
<tr>
<td>Loss margin (L_M)</td>
<td>20 dB</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>Transmitter array at basestation</strong></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Required TX EIRP (P_{N,RX} + L_{FS} + L_M \cdot G_{1,RX} \cdot 10 \cdot \log(N_{RX}))</td>
<td>68 dBm</td>
</tr>
<tr>
<td>TX antenna gain per element (G_{1,TX})</td>
<td>12 dBi</td>
</tr>
<tr>
<td>Required TX output power at 10-dB back out per element (P_{1,TX})</td>
<td>7.9 dBm</td>
</tr>
<tr>
<td>Required TX oP(_{1dB}) per element</td>
<td>17.9 dBm</td>
</tr>
<tr>
<td>Required TX array factor (20 \cdot \log(N_{TX}))</td>
<td>48.1 dB</td>
</tr>
<tr>
<td>Required Numbers of TX elements (N_{TX})</td>
<td>256</td>
</tr>
</tbody>
</table>
CHAPTER 2

DUAL-VECTOR DISTRIBUTED BEAMFORMING RECEIVER WITH SHUNT-FEED NETWORK

2.1 Phased-Array Receiver Overview

This chapter presents a 28-GHz four-channel phased-array receiver in 130-nm SiGe BiCMOS technology for fifth-generation (5G) cellular application. The phased-array receiver employs scalar-only weighting functions within each receive path and then global quadrature power combining to realize beamforming. I discuss both the theory and non-idealities of this architecture and then circuit de-
sign details for a phased-array front-end prototype. Differential LNAs and dual-vector variable-gain amplifiers are used to realize each front-end in a compact area of 0.3 mm\(^2\). Across four-bit phase settings, each array element achieves 5.1 to 7 dB noise figure, -16.8 to -13.8 dBm input-referred 1-dB compression point, and -10.5 to -8.9 dBm input-referred third-order intercept point. The average gain per element is 10.5 dB at 29.7 GHz, whereas the 3-dB bandwidth is 24.5\% (26.5 to 33.9 GHz). Root-mean-squared gain and phase errors are less than 0.6 dB and 5.4 degrees across 28-32 GHz respectively, and all four elements provide well-matched and well-isolated responses. Power consumption is 136 mW per element, equaling 546 mW for the four-element array. Compared to other RF front-ends using an active vector interpolator, this work achieves among the lowest area and among the highest fractional bandwidth; however, as can be expected, active phase shifter topologies will consume more power over passive approaches.

### 2.1.1 Phased-Array Receiver Architecture

Multiple phased-array architectures have been proposed in recent literature [PT12]. At least four popular beamformer architectures can be used to realize a mm-wave phased-array receiver and these will be reviewed below. Two important metrics to consider for a future 5G base station array with a large number of elements (~256) are area and DC power due to the cost of the hardware and the heat dissipation on the chip.

#### 2.1.1.1 Digital-Path Beamforming

First, phased arrays can employ digital phase shifting and combining, as shown in Fig. 2.1(a). This is a flexible approach for multiple-beam operation and is easily reconfigurable into a massive multi-input multi-output (MIMO) system [Rah05; Suy16; Beh07; Zar08; AA11]; however, the power consumption and back-end digital processing associated with hundreds of data converters each supporting up to a gigahertz of bandwidth is prohibitive [Pug16]. In addition, large and power-hungry local oscillator (LO) distribution networks need to be routed to drive in-phase/quadrature-phase
Figure 2.1 Architectures for N-element RX phased arrays with a frequency multiplier in the LO path: (a) the digital beamformer, (b) the baseband beamformer using the baseband phase-shifting approach, (c) the baseband beamformer using the LO phase-shifting approach, and (d) the RF beamformer.

(IQ) mixers in each channel without degrading the IQ accuracy. Further, the overall power and area performance scales linearly with the number of elements, N. Also, each receive chain including the LNA, mixer, and ADC is exposed to large out-of-beam blockers; thus, the linearity must be high for the full chain.
2.1.1.2 Baseband-Path Beamforming

Second, phased arrays can employ baseband (or intermediate-frequency (IF)) phase shifting and combining, as shown in Fig. 2.1(b). This has the benefit of a simple design procedure for the low-frequency phase shifter and combiner [Tab11; KP15]. In addition, a low-frequency phase shifter can achieve a fine phase resolution due to less sensitivity to parasitics. The beam pattern is synthesized using the combined signal at baseband or IF before the inputs of ADC. The requirement of a single ADC in the system saves considerable power; however, baseband beamforming still requires a pair of IQ mixers per element and large LO distribution networks, which are power- and area- hungry. I/Q mismatch can potentially be a critical problem due to complex I/Q LO routings, hence careful I/Q calibration is needed. Furthermore, the I/Q mixers and the low-frequency phase shifter and combiner also need to achieve high linearity for the strong blocker before the beam is formed at the output of the baseband or IF combiner.

2.1.1.3 LO-Path Beamforming

Third, phased arrays can employ LO phase shifting and baseband (or IF) combining, as shown in Fig. 2.1(c). This minimizes degradation to receiver and transmitter performance metrics, such as noise figure (NF), gain, and linearity, due to the phase shifter being realized within the LO path [Jeo08; Gua04; Bab06; Nat06; Nat05; Lo06; Sch08; KH08]. The phase shifters within a large LO distribution network must generate sufficient output power to drive the LO ports of the mixers. In addition, the array still requires N I/Q mixers, resulting in increased area and power consumption. Also, any I/Q imbalance incurred within the complicated LO networks must be calibrated. Furthermore, the I/Q mixers and the low-frequency combiner need to achieve high linearity for the strong blocker since the beam pattern is synthesized at baseband or IF.
2.1.1.4 RF-Path Beamforming

Finally, phased arrays can employ RF phase shifting and combining, as shown in Fig. 2.1(d). This approach is popular, having the fewest number of replicated components in the transceiver array [KR08b; KB08a; YR08; RK09; KR12; KR16; Nat11]. In addition, a single transceiver only needs a single LO path in the system which saves area and power compared to other beamforming architectures. Another advantage is that the beam pattern is synthesized at the output of the RF combiner and before the inputs of both the mixer and the ADC in the receive chain. Spatial filtering rejects out-of-beam interferers at the nulls, which protects the receiver from strong blockers. As a result, due to the simplicity of this architecture and the spatial-interferer rejection, RF beamforming is selected as the starting point of my design to realize a scalable phased array. However, realizing high-performance RF phase shifters and RF power combiners/splitters is a challenging task due to trade-offs between noise figure, gain, linearity, dc power and RF bandwidth.

2.1.2 RF Phase Shifter Topology

RF phase shifters are a critical component in the RF beamformer and can be realized using a number of topologies that can be categorized into passive or active approaches, as shown in Fig. 2.2. These trade-offs are area, loss (or gain), gain variation, phase tuning range, phase resolution, phase variation, RF bandwidth, dc power consumption, noise figure, and signal linearity. In the following, I review four popular RF phase shifter topologies to underscore these trade-offs and then set a foundation for a new topology.

2.1.2.1 Switched-LC Phase Shifter

A passive phase shifter can be composed of cascaded switched high-pass/low-pass inductor-capacitor (LC) networks, as shown in Fig. 2.2(a) [MR08b]. This approach can achieve accurate discrete phase shifts and high linearity; however, each switched LC delayed cell is typically opti-
mized at a single frequency for the desired phase shift. The cascading of multiple stages achieves full 360° phase-tuning range but results into a high loss, e.g., 10 dB at 34 GHz as reported in [MR08b]. The loss and the loss variation across different phase settings must be compensated by adding a variable-gain amplifier (VGA) in the RF chain; however, the passive shifter of switched-LC networks needs to work properly with desired impedance terminations by the addition of multiple inter-stage matching networks. As a result, multiple resonances throughout the RF chain can narrow the 3-dB fractional bandwidth, e.g., 5.9 % in [MR08b] or 10 % in [KR12], and 14.2 % in [Kim13]. Also, cascaded stages result in a generally large area, leading to a large chip size for the full array. In addition, another drawback for this topology is that the insertion phase error cannot be calibrated out if the insertion phase shifts of the phase shifters have errors (i.e., the 90 degree bit achieves only 85 degree discrete
phase shift).

2.1.2.2 Reflection-Type Phase Shifter

Another passive phase shifter topology is the reflection-type phase shifter (RTPS) employing varactor-based tunable reflectors, as shown in Fig. 2.2(b) [Nat11; GN17]. Even though the RTPS can achieve a large phase-shift tuning range in a compact structure without cascading multiple stages, the changing quality-factor of the varactor versus its capacitance can introduce phase-dependent loss if the reflective load is not properly matched, once again necessitating variable-gain compensation [Nat11; TN09]. Inter-stage matching networks need to be added between the RTPS and variable gain amplifier (VGA) shown in Fig. 2.2(b) as a phase-inverting VGA which provides variable gain along with a discrete 180° phase shift in [TN09].

2.1.2.3 Digitally-Controlled Transmission Line Phase Shifter

Another passive phase shifter topology is the digitally-controlled transmission line (t-line) with switchable floating metal strips beneath the signal trace, as shown in Fig. 2.2(c). Shunt switches are inserted at each metal strip either to connect it to ground when turned on or to make it float when turned off. By doing this, the capacitance and the inductance of the tunable t-line can be controlled to achieve a desired phase shift or delay [Yu08; Woo13]. However, a common limiting factor in the accuracy of the tunable t-line is due to the change in the characteristic impedance as a result of switching between two different delay modes in each unit. In addition, the dispersion limits the linearity of the phase versus the characteristic impedance, limiting the overall phase and amplitude accuracy. The proposed structure in [TVG16; Sad17] minimizes dispersion by maintaining the characteristic impedance through switching both inductance and capacitance of the unit cell. VGAs are again used to compensate for loss (6.8/9.3 dB with 185/190° phase-tuning range in [Woo13; TVG16]) and loss variation. Once again, the bandwidth can be limited due to the inter-stage matching networks [Sad17].
2.1.2.4 Cartesian Vector Interpolator

An alternative active phase shifter is the vector interpolator (VI) which creates phase shift and variable gain using weighted in-phase (I) and quadrature-phase (Q) vectors [KR07], as shown in Fig. 2.2(d). Similar to the gain-compensated RTPS, the interpolator requires both a quadrature generator and variable-gain amplifier (VGA), and therefore, as shown in [TN09], the noise figure (NF) and output-referred linearity are similar for both topologies; however, the gain of the VI is slightly better than the RTPS due to elimination of loss associated with the reflected loads. Also, the avoidance of varactors results in an arguably simpler structure. Compared to other passive phase shifters, the switched LC cells and the tunable t-line, the vector interpolation can achieve lower loss and wide $360^\circ$ phase-tuning range with compact area and easy phase/gain calibrations. As a result, the Cartesian vector interpolator is chosen as my design starting point.

2.1.3 Dual-Vector Distributed Beamforming Architecture

Each element of the receive array consists of a low-noise amplifier (LNA) and an RF phase shifter, the vector interpolator, as shown in Fig. 2.3(a). Interpolators have drawbacks, however. First, the need for quadrature generation within each front-end imposes both area and bandwidth penalties. For example, in [Sar14], the 28-GHz quadrature hybrid occupies one-third of the total transmit front-end area including the phase shifter and PA. The phase shifter has a narrow 3-dB fractional bandwidth of 14.3% due to multiple resonances throughout the chain. Furthermore, a second limitation is the crosstalk between the I and Q signal vectors, where the variable-gain of one component (I or Q) can depend on the value of the other component (Q or I). This results in phase and amplitude variation across settings, complicating the control scheme. This issue worsens at higher frequencies due to the reduced output impedance of the transconductors used to form the VGA.

These limitations can be addressed by altering the architecture of the vector-interpolating front-end, as shown in Fig. 2.3(b) and (c). Key functions are color-coded to highlight their new location.
Figure 2.3 Architectures for N-element phased array: (a) traditional vector-interpolation, (b) modified vector interpolation with quadrature splitter and power combiner locations swapped, and (c) proposed dual-vector distributed beamformer, and (d) dual-vector distributed beamformer employing mixer-based quadrature combining. Note that $X_n$ and $Y_n$ refer to signals within the $n^{th}$ element, amplitude weighted according to equation (2.1).

within the system. First, the position of the input quadrature splitter and output combiner are swapped, allowing the outputs of the interpolator to be isolated from each other and reducing crosstalk. A drawback of placing the quadrature combiner last, though, is a 3-dB drop in gain,
as only half the signal power is provided to the desired output. This gain reduction impacts NF. Therefore, second, the quadrature combiner is moved out of each individual element to a single global location. After power combining, the signal-to-noise ratio is increased by the number of elements in the array; hence, a gain reduction here has less impact on the NF. In addition, moving the quadrature from a local location within front-end to the global location at the output of the array improves the bandwidth due to reducing the numbers of inter-stage resonances throughout the RF chain. A similar approach was proposed in [Par05], where the quadrature function was instead realized through a pair of quadrature downconversion mixers (depicted in Fig. 2.3(d)). A benefit of the mixer-based approach is that direct-conversion receivers already must generate accurate quadrature local-oscillator signals, and these can be leveraged to provide the quadrature solution for beamforming. A drawback is that the mixers are exposed to spatial signals located either within the desired beam location or the image location. In contrast, when a quadrature hybrid is used, two concurrent beams are provided and the undesired lobe is eliminated prior to the downconversion.

The proposed new architecture can theoretically achieve broadband performance, compact area, and good RF performance. I refer to this architecture as dual-vector distributed beamforming (DVDB). Dual vector refers to the fact that two signals are generated within each front end. Distributed refers to the fact that the overall beamforming operation is subdivided between scaling functions within each front end and a global interpolation function located after the power combiner. A new circuit of dual-vector VGA (DVGA) is designed to realize amplitude weighting scalar front-end and it potentially provides wider bandwidth with much smaller area than the traditional VI. In the remainder of this chapter, I present (a) beamforming capabilities of the DVDB, (b) new circuit architectures to realize front-end components within the DVDB, (c) a complete four-element DVDB prototype realized in SiGe BiCMOS technology used to validate the architecture, and (d) calibration methodologies for the proposed dual-vector distributed beamformer.
2.2 Dual-Beam Support

In this section, I derive the array factors for the DVDB and show how two simultaneous beams can be supported. One is directed at a given angle and the other is a conjugate beam which is reflected across broadside which I refer to as the “image” pattern. Using this foundation, I then evaluate impact of skew within the dual-vector combining network on the realized array factors.

As discussed in the first chapter, the array factor, \( F(\theta) \), as a function of angle-of-arrival \( \theta \) (zero corresponds to broadside) for an \( N \)-element linear array is [PZ02]

\[
F(\theta) = \sum_{n=1}^{N} e^{j(n-1)\kappa d \sin(\theta)} a_n e^{-j\alpha_n} = \sum_{n=1}^{N} \left( a_n e^{j(n-1)\kappa d \sin(\theta)} \frac{\cos(\alpha_n) - j a_n e^{j(n-1)\kappa d \sin(\theta)} \sin(\alpha_n)}{X_n \ y_n} \right),
\]

where \( \kappa = \frac{2\pi}{\lambda} \), \( d \) is the antenna spacing, \( a_n \) is the amplitude shift per element, and \( \alpha_n \) is the phase shift per element. Phasors \( X_n \) and \( Y_n \) are the Cartesian expansions of the amplitude- and phase-shift for the \( n^{th} \) element, depicting vector interpolation.

For dual-vector distributed beamforming, I apply the summation to all \( X \) and \( Y \) signals and then pass these summations through a global 90° hybrid coupler (Fig. 2.3(c)). For the first coupler output, \( \sum Y \) undergoes a -90° phase shift, yielding a first array factor

\[
F_1(\theta) = \frac{\sqrt{2}}{2} \left( \sum X_n - j \sum Y_n \right),
\]

where summation bounds have been dropped and where the \( \sqrt{2}/2 \) accounts for the power split in the quadrature combiner. This response is equivalent to that in (2.1) with the addition of a scaling factor. To steer the main beam to angle \( \theta_0 \), the phase shifters are set to \( \alpha_n = (n-1)k d \sin(\theta_0) \), leading to a peak directivity of \( N \) at angle \( \theta_0 \) [PZ02]. For the second coupler output, \( \sum X \) undergoes a -90°
phase shift, yielding a second, “image” array factor

\[
F_2(\theta) = \frac{\sqrt{2}}{2} \left( \sum Y_n - j \sum X_n \right) = -\frac{j\sqrt{2}}{2} \left( \sum X_n + j \sum Y_n \right).
\] (2.3)

This image pattern is the conjugate of the \(F_1\) pattern multiplied by a global -90° phase shift. As such, for the same phase shifter settings described above, output two exhibits a peak directivity of \(N\) at angle \(-\theta_0\), \(i.e.,\) reflected across broadside. As can be seen, this architecture can simultaneously support two conjugate beams. This can provide additional capabilities for a MIMO system employing hybrid analog/digital precoding [Gao16], wherein the dual-vector distributed beamformers serve as dual-beam sub-arrays for the system. Multiple dual-output sub-array responses can be combined to synthesize desired patterns. Additionally, a fast, switched-beam capability can be provided, wherein the receiver can quickly switch between two available patterns.

Fig. 2.4(a) and (b) show example normalized patterns from Matlab for \(F_1\) and \(F_2\), respectively, for four and eight-element linear arrays (\(\lambda/2\) spacing) controlled such that beam one steers to +30°. Fig. 2.4(c) and (d) show example patterns for \(\sum X\) and \(\sum Y\), respectively, for these same scenarios, indicating that both exhibit peaks at both desired and conjugate angles. The reasoning follows. Since \(X\) and \(Y\) involve cosine- and sine-weighted signals, Euler’s equation tells us these can be decomposed into phasors directed at both +\(\alpha\) and −\(\alpha\); hence two beams are present. Alternatively, one can simply solve (2.2) and (2.3) for \(\sum X\) and \(\sum Y\), which will be functions of both \(F_1\) and \(F_2\); hence, \(\sum X\) and \(\sum Y\) have peaks at both \(\theta_0\) and \(-\theta_0\).

With this foundation, I now discuss non-idealities for this system. First, both individual \(X\) and \(Y\) signals must ideally be in-phase or 180° out of phase to realize four-quadrant phase shifting. Any local phase deviation incurred as the gain is varied constitutes an effective quadrature error for that individual element, leading to phase and gain errors. Second, the \(\sum X\) and \(\sum Y\) signals must also not experience any global phase error; hence, the power combiners for each must be phase coherent. Any global phase skew, \(\delta\), would result in imperfect cancellation of the undesired pattern.
Figure 2.4 Calculated (a) $F_1$, (b) $F_2$, (c) $\sum X$, and (d) $\sum Y$, when beam one is steered to 30° for $\lambda/2$-spaced linear array with N=4 and N=8. All patterns normalized by N.

Introducing this skew arbitrarily to the $\sum Y$ component in (2.2), we find

$$F'_1(\theta) = \frac{\sqrt{2}}{2} \left( \sum X_n - j e^{j\delta} \sum Y_n \right) = F_1(\theta) \frac{1 + e^{j\delta}}{2} + F_2(\theta) \frac{1 - e^{j\delta}}{2}, \quad (2.4)$$

where $F'_1$ represents the skewed array factor for output one and $F_1$ and $F_2$ represent the ideal array factors without skew. Using this expression, we can solve for a value of $\delta$ that results in a contribution from the undesired pattern which is $R$ decibel below the main desired beam. Note that this contribution can add together with an existing side-lobe at that position, degrading the overall side-lobe performance. Taking the ratio of desired to undesired beam magnitudes and solving for $\delta$, it can be shown that

$$\delta = \cos^{-1} \left( \frac{1 - 10^{-R/10}}{1 + 10^{-R/10}} \right). \quad (2.5)$$

For example, to keep the undesired pattern 25-dB below desired, the global skew between $\sum X$ and $\sum Y$ must be below 6.4°. Fig. 2.5 shows the pattern for $F'_1$ and the scaled versions of $F_1$ and $F_2$.
$F_2$ according to (2.5) with a 6.4° skew for a four-element array steered to 30°. For this simulation, each element’s performance is assumed ideal. Neither quantization error nor statistical variations within each element is included, since both will impact $F_1$ and $F_2$ patterns in the same way. Fig. 2.5 illustrates how the $F_1'$ pattern is composed of the addition of scaled versions of $F_1$ and $F_2$. As will be shown, a skew less than 6.4° is achievable in dual power-combiner designs.

![Skewed Pattern Diagram](image)

**Figure 2.5** Skewed $F_1$ pattern ($F_1'$) with phase skew of 6.4° for four-element array steered to 30°. Scaled versions of the ideal $F_1$ and $F_2$ patterns according to (2.5) included to show components of the skewed pattern.

### 2.3 Dual-Vector Distributed Receiver Array Implementation

A prototype four-element receiver array has been implemented in 130-nm SiGe BiCMOS 8HP technology from GlobalFoundries to indicate performance capabilities of the DVDB. The array block diagram is shown in Fig. 2.6, which I herein refer to as the first generation (Gen-1) sub-array prototype. Four front-ends are combined using a dual-differential Wilkinson power combiner structure. The
\( \sum X \) and \( \sum Y \) outputs are then combined using a differential hybrid coupler. To simplify testing, I have only included the ability to measure output one from the coupler, where output two is terminated on chip. Simulations verify that outputs one and two perform as predicted in (2.2) and (2.3). Indeed, the \( F_2 \) response can be obtained from output one by swapping our definitions, and thereby weighting factors, applied to \( X \) and \( Y \). A chip micrograph is shown in Fig. 2.7. The die size is 7.2 mm\(^2\) including pads and the array area is 3.7 mm\(^2\) excluding pads. A single element (excluding input balun) occupies 0.3 mm\(^2\). The chip consumes 97.5 mW for each front-end and another 40 mW per element for DACs which were not power optimized. The total power dissipation is 546 mW.

A more detailed block diagram of the RF front-end is shown in Fig. 2.8(a). Each front-end requires a low-noise amplifier (LNA) and a dual-vector variable-gain amplifier (DVGA). A fully-differential

![Block diagram of realized four-element phased-array front-end employing dual-vector distributed beamforming for the first-generation (Gen-1) sub-array.](image)

**Figure 2.6** Block diagram of realized four-element phased-array front-end employing dual-vector distributed beamforming for the first-generation (Gen-1) sub-array.
Figure 2.7 Die micrograph of phased-array receiver for the first-generation (Gen-1) sub-array. Die size is 3 x 2.4 mm².

architecture was selected to reduce the impact of finite supply-plane impedance on circuit performance and stability, at the cost of nearly a doubling of the front-end power consumption for the same transistor current density. Fig. 2.8(b) summarizes the performance targets for each element in the front-end to achieve a high dynamic range for the projected 5G basestation application. In the following section, I describe design details for each element in the system.

2.3.1 Low-Noise Amplifier

A fully-differential single-stage LNA is designed for moderate linearity and low noise, and the schematic is shown in Fig. 2.9. A cascode topology is used in the LNA to achieve high gain and high reverse isolation. Transistors $Q_{1-4}$ are biased to achieve a peak $f_t$ of 200 GHz with current density of 1 mA per µm. A degeneration inductor of 115 pH is added to achieve linearity requirement without consuming any voltage headroom. The size of $Q_{1-2}$ is scaled up at a fixed current density to achieve
Figure 2.8 (a) Detailed block diagram of receiver front-end and (b) performance specifications.

good noise and power matching. A spiral transformer is used as an input balun and has a measured insertion loss of 0.8 dB. This balun would likely be eliminated in a final system packaged with differential antennas, improving NF by 0.8 dB. Note, though, that the loss is not de-embedded from any measurement results. A bypass capacitor of $1 \text{ pF}$ is placed at the base terminals of transistors $Q_{3-4}$ to achieve a low-impedance AC ground. Finally, the output LC matching network is designed to directly drive the DVGA input impedance of $54-j108 \Omega$ at 28 GHz and includes a shunt resistor of $350 \Omega$ to broaden the bandwidth. In simulation, the LNA achieves a small-signal gain of 11.2 dB, NF of 4.4 dB, $iP_{1 dB}$ of -4.9 dBm, and $iIP_{3}$ of $+7.3 \text{ dBm}$ all at 30 GHz. The LNA draws 16 mA from a 2.5-V supply (40 mW).

2.3.2 Dual-Vector Variable-Gain Amplifier

Two variable-gain functions are needed for interpolation. These are realized with a single-input, dual-output structure to save both space and power—the dual-vector VGA (DVGA)—the schematic being shown in Fig. 2.10. This structure was originally proposed in [GF15], but is modified here to
work with a single input. The circuit should provide one differential output \(X\) which is weighted according to a \(\cos(\alpha)\) function and another differential output \(Y\) which is weighted according to a \(\sin(\alpha)\) function. This is realized within the circuit through a cascade of a transconductance and two current-steering operations. The first current-mode stage provides a necessary predistortion of

\[
A(\alpha) = G_m \cdot \frac{\sqrt{2}}{2} (|\cos(\alpha)| + |\sin(\alpha)|),
\]

where \(G_m\) represents the transconductance provided by \(Q_1\) and \(Q_2\), and \(\alpha\) is the desired phase shift for a given element. Fig. 2.11(a) shows \(A(\alpha)\) across a single quadrant normalized to the maximum value. Predistortion is provided by \(Q_3\)-\(Q_6\) and controlled through an eight-bit digital-to-analog converter (DAC) and inverse-\(\tanh\) cell \((Q_{15}\)-\(Q_{16}\)). The \(\sqrt{2}/2\) in (2.6) ensures the current-steering function \(|\cos(\alpha)| + |\sin(\alpha)|\) has a maximum value of one. Finally, the absolute values indicate that the function is identical for all four quadrants, with sign switching handled elsewhere. A second
level of current steering is used to direct the current to either outputs $X$ or $Y$. This is ideally realized with a steering function equal to

$$k(\alpha) = \frac{|\cos(\alpha)|}{|\cos(\alpha)| + |\sin(\alpha)|},$$

realized with transistors $Q_7$-$Q_{14}$. Fig. 2.11(b) shows $k$ and $1-k$ across a single quadrant. The $k$-function is controlled through a separate eight-bit DAC and inverse-$tanh$ cell ($Q_{17}$-$Q_{18}$). Output $X$ is given by the cascade of $A$ and $\pm k$ to realize $\pm \sqrt{2} \cdot G_m Z \cos(\phi)/2$, while output $Y$ is given by the cascade of $A$ and $\pm (1-k)$ to realize $\pm \sqrt{2} \cdot G_m Z \sin(\phi)/2$, where $Z$ represents the impedance of the output network. To achieve four-quadrant operation, sign inversion is included within both the $X$ and $Y$ paths using cross-coupled transistors (shown in shaded region of Fig. 2.10).

**Figure 2.10** Simplified schematic of first-generation dual-vector variable-gain amplifier (DVGA).
Figure 2.11 (a) Ideal pre-distortion function $A(\alpha)$ across one quadrant according to equation (2.6) and (b) ideal current-steering functions $k(\alpha)$ and $1-k(\alpha)$ across one quadrant according to equation (2.7).

I now evaluate non-idealities within the DVGA response. Fig. 2.12(a) shows the simulated transfer function of the DVGA to outputs $X$ and $Y$ on a polar plot when $A$ is fixed, the sign of $X$ is inverted, and when $k$ is varied from zero to one. The ideal response is a straight line. As can be seen, the phase deviates as the amplitude is scaled, introducing an amplitude-modulation to phase-modulation (AM-PM) error. This error arises primarily in this circuit due to a changing output impedance of Q7-Q14 as a function of control current. Fig. 2.12(b) shows the polar response of the DVGA across $\alpha$ when only current steering function $k(\alpha)$ is applied and when outputs $X$ and $Y$ are combined using a hybrid coupler. The ideal response is diamond-shaped. From Fig. 2.12(b), the need for amplitude predistortion is clearly demonstrated. Fig. 2.12(c) shows the polar response of the DVGA for the four axis settings ($0^\circ$, $90^\circ$, $180^\circ$, and $270^\circ$), as the predistortion function, $A$, is varied from zero to full scale. This indicates an AM-PM error introduced by $A(\alpha)$. Phase errors introduced in both $k$ and $A$ can be compensated by adjusting $k(\alpha)$. Fig. 2.12(d) shows the polar plot for five-bit phase resolution when predistortion is applied and modified $k$ values are used for compensation, indicating a final equalized response.
Figure 2.12 | Ideal (dashed line) and simulated (solid line) vector response of front-end at 30 GHz with radial axis in linear scale. (a) X and Y current-steering function, $k(\alpha)$ and $1-k(\alpha)$, without 90° hybrid combiner, illustrating AM-PM errors in $k(\alpha)$. (b) $X+jY$ using only current steering together with 90° hybrid combiner, indicating need for amplitude pre-distortion. (c) $X+jY$ response as $A(\alpha)$ is varied from zero to full scale for $0°/90°/180°/270°$ states, illustrating AM-PM errors in $A(\alpha)$. (d) Final phase-shifted results across 32 phase settings, demonstrating equalized response.
The overall circuit was designed to support five-bit phase resolution, with phase states including the axis settings. Since $A(\alpha)$ has its minimum value at 0°, 90°, 180°, and 270°, NF of the DVGA will be highest for these axis settings. Simulations indicate that the DVGA without predistortion applied shows 5.3 dB gain at 0° setting and -2.3 dB gain at 45° setting, where the ideal difference between having all versus half of the current directed to an output would be 6 dB. For these same settings, NF is 8.6 and 14.5 dB, and $iP_{1\text{dB}}$ is +2.7 and +0.9 dBm, respectively. The DVGA draws 16 mA from a 3.3-V supply (52.8 mW) and another 40 mW from two binary-weighted current DACs for the pre-distortion and the current-steering functions.

### 2.3.3 Dual-Differential Wilkinson Power Combiner

The $X$ and $Y$ signals from each front end are individually power combined to provide $\Sigma X$ and $\Sigma Y$ signals. These summations are realized using a two-stage dual-differential Wilkinson structure. Compared to an active combiner structure, passive structures can provide high linearity, high isolation between inputs, bidirectionality, and zero DC power consumption. Key design considerations for the power combiner are achieving (a) identical electrical performances for $X$ and $Y$ signals, (b) high isolation between $X$ and $Y$ traces, and (c) small area.

First of all, the analysis in four different cases for a single differential Wilkinson power combiner is studied in Fig. 2.13. Here, differential and common-mode are used to describe the local phase relationship between the positive and negative signals on the differential transmission line, whereas even and odd-mode are used to describe the global phase relationship between the two inputs to the combiner [Nat11]. For differential-mode input signals of the normal operational mode in the differential array, the differential input impedance at two inputs ports is matched to $Z_0$ for both even- and odd- mode inputs, as shown in Fig. 2.13 (b) and (c). For common-mode input signals as shown in Fig. 2.13 (d) and (e), the common-mode input impedance in both even- and odd-mode inputs should be closed to $Z_0/4$ (if $Z_{even} = Z_0/2\sqrt{2}$), which is not effective open-circuit input impedance. However, the combiner common-mode impedance should have minimum impact on
the performance due to the fact that (1) the LNA and DVGA are differential structures with high common-mode signal rejection, and (2) the common-mode impedance mismatch occurs at the DVGA’s outputs and the combiner’s inputs. As a result, the common-mode signals should be small in our designs.

**Figure 2.13** (a) Schematic of the differential Wilkinson power combiners with isolation resistors of $Z_0=50$-Ω in analysis of (b) differential-mode input signals and even-mode inputs, (c) differential-mode input signals and odd-mode inputs, (d) common-mode input signals and even-mode inputs, and (d) common-mode input signals and odd-mode inputs.

Three possible transmission-line structures have been evaluated using the EMX electromagnetic simulator [Emx]. The first is shown in Fig. 2.14(a), where two edge-coupled coplanar waveguide (CPW) with back-side ground are placed side-by-side with a ground shield in between. The second is shown in Fig. 2.14(b) where $Y$ signals are realized in an inverted edge-coupled CPW with a ground plane above the signals. This is then stacked beneath the $X$ structure to achieve a smaller area. The third is shown in Fig. 2.14(c) where both the $X$ and $Y$ lines are realized with stacked coupled lines and isolated from each other with a center ground shield. The dimensions of each $X$ and $Y$ coupled line in these three structures are chosen to realize a 71-Ω differential characteristic impedance ($Z_{0,\text{diff}}$).
Fig. 2.15 compares the simulated responses for X and Y differential transmission-line test structures of length $\lambda/4$. I compare $Z_{0,\text{diff}}$, the loss of the X and Y lines, and the amplitude and phase differences between X and Y lines. The stacked inverted structure (Fig. 2.14(b)) can achieve half the cross-sectional area for the same $Z_{0,\text{diff}}$ of 71 $\Omega$; however, the simulations show that the X and Y lines have a different loss and phase shift since the lower lines are exposed to the silicon substrate, impacting phase velocity, and are realized in thinner metals, increasing loss. In contrast, both the edge-coupled (Fig. 2.14(a)) and stacked (Fig. 2.14(c)) coupled lines can achieve identical electrical performance for X and Y due to identical cross-sections. Since the stacked structure is larger, I choose the edge-coupled CPW structure.

**Figure 2.14** Cross sections for possible X and Y power combiners to realize 71-\(\Omega\) $Z_{0,\text{diff}}$: (a) parallel edge-coupled CPW with back-side ground (chosen in our design), (b) inverted / non-inverted edge-coupled CPW, and (c) stacked coupled lines.

Fig. 2.16 shows the layout of the two-stage dual-differential power combiner, along with details on the junctions and cross-overs for this structure. The overall area impact of having parallel power combiners necessary for dual-vector distributed beamforming rather than a single power combiner.
Figure 2.15 Simulated results for X and Y parallel edge-coupled (chosen in our design), inverted, and stacked transmission lines for length = λ/4: (a) Z₀,diff, (b) loss, (c) amplitude difference between X and Y, (d) phase difference between X and Y.

used for traditional beamforming is estimated to be an approximate doubling of the combiner area for 28 GHz. Having two side-by-side couplers prevents us from realizing as tight of a meandering. The area penalty depends on the amount of meandering applied to the transmission lines, where less meandering is required at higher frequencies (due to reduced wavelength); hence, the penalty is reduced as you move towards higher frequencies. This area penalty can be eliminated by shifting from a parallel combiner to a series combiner structure and has been incorporated in the second-generation DVDB presented in the following chapter.

EMX simulations indicate a total insertion loss of less than 2.3 dB and return loss for all ports better than 10 dB across 25 to 35 GHz in Fig. 2.17 (a) and (b). The isolation between X₁ and X₂ and between Y₁ and Y₂ is less than 12 dB and the coupling between \( \sum X \) and \( \sum Y_{1-2} \) and between \( \sum Y \) and \( X_{1-2} \) is less than -44 dB across 25 to 35 GHz in Fig. 2.17 (c) and (d). Amplitude and phase differences between any input and the \( \sum X \) and \( \sum Y \) outputs are 0.3 dB and 4.3°, respectively. These errors are depicted in Fig. 2.18, illustrating phase and amplitude differences between all X responses, all Y responses, and between X and Y responses. Errors are depicted in both absolute and root-mean
squared (RMS) terms. The phase error is due to slightly different lengths of coupled lines at the bends and junctions, but this skew is sufficiently low to keep the unwanted conjugate side-lobe 27 dB below the main lobe, using equation (2.5).

2.3.4 Passive Global Quadrature Combiner

The global quadrature combiner is realized using a balanced pair of 90° Lange couplers for differential quadrature summation and then a spiral transformer balun. This topology was chosen over lumped or distributed branchline couplers to achieve a smaller area and chosen over an all-pass filter topology [KR07] to provide less sensitivity to capacitive loading effects. A drawing of the quadrature combiner with output balun is shown in Fig. 2.19. First, an input distribution network is included to fan-out the dual-differential outputs (X, Y, and ̃X, ̃Y) to the couplers, with X and Y provided to one
Figure 2.17 Simulated results for X and Y dual two-stage Wilkinson power combiner: (a) $S_{11}$-to-$S_{66}$, (b) the loss of $S_{31}$-$S_{32}$ for X combiners and the loss of $S_{64}$-$S_{65}$ for Y combiners, (c) $S_{21}$ for the isolation between $X_1$ and $X_2$ and $S_{54}$ for the isolation between $Y_1$ and $Y_2$, (d) $S_{61}$-$S_{62}$ and $S_{34}$-$S_{35}$ for the isolation between X and Y combiners. Note that $X_1$ is $P_1$, $X_2$ is $P_2$, $\sum X$ is $P_3$, $Y_1$ is $P_4$, $Y_2$ is $P_5$, $\sum Y$ is $P_6$, and all ports are terminated with differential 50 $\Omega$ in Fig. 2.16.

Figure 2.18 Simulated mismatch results for X and Y dual two-stage Wilkinson power combiner: (a) $X_i$-to-$X_j$ phase difference, (b) $Y_i$-to-$Y_j$ phase difference, (c) $X_i$-to-$Y_i$ phase difference, (d) $X_i$-to-$X_j$ amplitude difference, (e) $Y_i$-to-$Y_j$ amplitude difference, and (f) $X_i$-to-$Y_i$ amplitude difference. Indices $i$ and $j$ refer to any of the four possible input ports for $X$ or $Y$.

Lange and $\bar{X}$ and $\bar{Y}$ provided to the other. Each Lange coupler is realized with four interdigitated coupled lines on the second-to-top metal layer (E1) over a metal-1 ground plane. This layer has a smaller pitch than the top layer (MA) and can therefore realize higher coupling. Total (unwound)
length of each Lange coupler is 1.25 mm, each line width is 4 µm, and line spacing is 2.3 µm. Each Lange coupler is meandered to save area. The total area of the quadrature combiner is 0.35 mm²—0.19 mm² coming from the two Lange couplers and 0.16 mm² coming from the balun.

EMX simulation results in Fig. 2.20 (a) and (b) indicate a < 2.6-dB insertion loss (1.1 dB from coupler and 1.5 dB from balun), < 1.5 ° IQ phase error between inputs, and < 1-dB IQ amplitude error between inputs across 25 to 35 GHz, all when the coupler is loaded with ideal terminations on all ports (differential 50 Ω at I, Q, and ISO ports for the coupler and a single-end 50 Ω at the transformer output port). Fig. 2.20 (c) shows that the coupler achieves well match of S₁₁–S₃₃ at each port but S₁₁ and S₂₂ have slightly different input impedance between the I and Q ports. The surrounding circuits, however, provide more narrow-band terminations, once the coupler is attached within the array; hence, the quadrature accuracy is reduced. This accuracy will be demonstrated in the measurement section by comparing amplitude and phase between axis settings.

![Figure 2.19 Illustrations of (a) the schematic and (b) the 3D structure of top-level layout of the quadrature combiner composed of an input distribution network, a pair of Lange couplers, and an output transformer. Cross-sections are also provided for the input feed and the Lange.](image)
Figure 2.20 Simulated results of the global quadrature combiner of (a) the magnitudes of $S_{21}$ for the $I$ port, $S_{31}$ for the $Q$ port, and the IQ amplitude error; (b) the phase of $S_{21}$ for the $I$ port, $S_{31}$ for the $Q$ port, and the IQ phase error; and (c) magnitudes of $S_{11}$ for the $I$ port, $S_{22}$ for the $Q$ port, and $S_{33}$ for the output port.

2.4 Measurement Results

2.4.1 Low-Noise Amplifier Characterization

A stand-alone breakout of the LNA has been realized, where the LNA output match is modified to 50 Ω to facilitate measurement. The die photo of the LNA with input and output baluns is shown in Fig. 2.21. Fig. 2.22(a) shows both the simulated and measured scattering parameters and NF versus frequency. Model-to-hardware correlation is good, with a slight deviation in $S_{22}$ coming from the bondpad model. The LNA breakout achieves 10-dB gain, 5-dB NF, and better than 10-dB input return loss at 28 GHz. The 5-dB NF translates to a 4.2-dB NF for the LNA without the balun. Linearity results are shown in Fig. 2.22(b) and (c), indicating greater than -5-dBm input-referred 1-dB compression point (iP$_{1dB}$) and +3.9-dBm input-referred third-order intercept point (iIP$_3$). The differential LNA draws 18.5 mA from a 2.5-V supply (46.3 mW) with higher current used to improve linearity.
**Figure 2.21** Die micrograph of low-noise amplifier. Die size is 0.75 x 1.0 mm\(^2\).

**Figure 2.22** Measured and simulated LNA results: (a) S-parameters and noise figure, (b) iIp\(_3\) at 30 GHz, and (c) iP\(_{1dB}\) at 30 GHz.

### 2.4.2 Dual-Vector Receiver Calibration Methodology

The phase and amplitude of each element is controlled through two eight-bit DACs to realize pre-distortion and current-steering functions. Here I describe the methodology for determining the proper control settings. During the measurement, I first choose DAC settings of the current-steering function \(k(\alpha)\) to achieve the desired five-bit phase response without turning on pre-distortion. Once the minimum gain is determined from these 32 responses, I then equalize all other gains to this lower value using the predistortion control DAC for \(A(\alpha)\). Since there is slight phase deviation due to
the predistortion (illustrated in Fig. 2.12(c)), the current-steering function is adjusted accordingly, where the amount of adjustment is only a few least significant bits (LSBs).

Fig. 2.23(a) and (b) show the comparison between ideal, simulated, and measured pre-distortion and current-steering functions over eight phase states within one quadrant, where the other three quadrants have the similar result. The current settings for the measurements are plotted assuming ideal DAC performance (25-µA LSB). From Fig. 2.23, I can conclude a few things. First, the overall amplitude is set by the front-end’s gain at 45°. Second, the amount of predistortion needed for the axis settings is larger than predicted, which will lead to poorer NF performance along the axes (0, 90, 180, and 270° phase settings). This reduction comes from lower signal amplitude at the 45° setting arising from the phase deviations of X and Y as a function of $k(\alpha)$. This phase offset between X and Y reduces the amplitude of the combined signal. With lower amplitude at 45°, the axis settings must be reduced further to equalize. Finally, at 45°, the required weighting between X and Y is unequal. This accounts for the amplitude-phase dependency within the DVGA, illustrated in Fig. 2.12.

**Figure 2.23** Comparison between ideal, simulated, and measured (a) pre-distortion function $A(\alpha)$ and (b) current-steering functions $k(\alpha)$ and $1-k(\alpha)$ over eight phase states of $\alpha$ within one quadrant.
2.4.3 Single Receiver Front-End Characterization

A single front-end breakout was realized for test purposes. This breakout includes the active front-end plus the differential quadrature power combiner. A die micrograph of the breakout is shown in Fig. 2.24. The area of the front end including the quadrature hybrid is 1.08 mm$^2$ without pads. Notably, the area of the combiner is nearly identical to that of the active circuits, pointing to the front-end area savings possible by switching to dual-vector distributed beamforming.

![Die micrograph of receiver front-end. Die size is 1.8 x 1.2 mm$^2$.](image)

All measurements were performed through wafer probing. $S$-parameter, gain/phase responses, isolation, and channel matching measurements were taken using a two-port Agilent E8361C 67-GHz network analyzer in Fig. 2.25. Fig. 2.26 (a) shows the measured phase of $S_{21}$ of the single-channel receiver front-end across phase settings. The RMS phase error after calibration is $<5.4^\circ$ at 28 to 32 GHz. Fig. 2.26(b) and (c) shows the differential nonlinearity (DNL) and integral nonlinearity (INL) of the phase responses, indicating errors less than ±0.5 LSB. The measured gain ($|S_{21}|$) across 32 phase states is shown in Fig. 2.27(a) indicating an average peak gain of 10.5 dB at 29.7 GHz with a 24.5% 3-dB bandwidth of 26.5 to 33.9 GHz. The RMS gain error after calibration is $<0.9$ dB across 25 to 35
Fig. 2.25 S-parameters measurement setup for receive front-end.

GHz. Fig. 2.27(b) and (c) show the magnitude of $S_{21}$ and gain deviation from the average gain over 32 phase settings at 29 to 31 GHz. The gain deviation is less than ±1 dB and can be improved by further adjustment of the pre-distortion. Input and output return losses are greater than 10 dB across the band, shown in Fig. 2.28. The measured s-parameters match simulations, with all simulation results depicted in these figures with dashed lines. Finally, to evaluate the quadrature accuracy within the front-end, I compare the amplitude and phase difference between axis settings (0° and 90°). Fig. 3.46 (a) and (b) show measured phase error less than 5° and amplitude error less than 0.8-dB from 16 to 33.6 GHz.

The noise performance is taken using a Keysight 346CK01 noise diode and a Rohde & Schwarz FSUP-43 signal-source analyzer in Fig. 2.30. As indicated earlier, the noise performance along the axis settings will be worse due to the attenuation needed for predistortion, which accentuates the noise in the final current-steering stage. This issue can be mitigated by avoiding the axis settings altogether, as I reported in [Yeh16]. Thus, I can revert the array to four-bit performance and skip every other state to reduce the maximum NF by about one decibel. Here, I present both the five-bit
Figure 2.26 Measured (a) $S_{21}$ phase response and RMS phase errors versus frequency across 32 phase settings for the receiver front-end with DVGA calibrated for 30-GHz operation, (b) $S_{21}$ phase DNL, and (c) $S_{21}$ phase INL.

Figure 2.27 Measured (a) $S_{21}$ gain response and RMS gain errors versus frequency across 32 phase settings for the receiver front-end with DVGA calibrated for 30-GHz operation, (b) $S_{21}$ gain, and (c) gain deviation.

and four-bit results to illustrate the trade-offs. Fig. 2.31(a) shows the simulated and measured NF versus frequency across all 32 states (5-bits). The measured NF is 5.6 to 8.6 dB. Fig. 2.31(b) shows the NF across both 4-bit (solid symbols) and 5-bit (empty plus solid symbols) phase settings at 29 to 31 GHz, clearly indicating how the NF rises for settings closer to the axes. To improve the noise performance, the DVGA architecture could be altered such that the predistortion function is
Figure 2.28 Measured (a) $S_{11}$ and (b) $S_{22}$ magnitude responses over 32 phase settings for the receiver front-end.

Figure 2.29 Measured IQ (a) phase and (b) amplitude errors for the front-end at $0^\circ$ and $90^\circ$ phase settings without pre-distortion.

realized with increased $G_m$ rather than decreasing RF current, although this would slightly impact the interstage matching between the LNA and DVGA.

Swept-power measurements are taken with an Agilent E8257D signal generator providing the input and an Agilent N1913A power meter and an Agilent N8488A power sensor for the output. Third-order intermodulation (IM3) measurements are taken using a second HP 83650B signal generator and a Rohde & Schwarz FSUP-43 signal-source analyzer in Fig. 2.32. As shown in Fig. 2.33(a) and
Figure 2.30 Noise measurement setup for receive front-end.

Figure 2.31 Measured and simulated (a) noise figure across frequency over 32 phase settings and (b) noise figure across 32 phase settings at 29-31 GHz (solid symbols are for 4-bit results and empty symbols are for 5-bit results).

(b), the measured $iP_3$ and $iP_{1dB}$ of the front-end are -10.6 to -5.7 dBm and -16.8 to -12.9 dBm, respectively. Fig. 2.33(c) and (d) show $iP_3$ and $iP_{1dB}$ across both 4-bit (solid symbols) and 5-bit (empty plus solid symbols) phase settings at 29-31 GHz. The $iP_3$ behavior is inverse to that of the NF behavior, indicating that the overall dynamic range of the front end is relatively constant across 32 phase settings.
Figure 2.32 Linearity measurement setups of (a) one-tone power sweep and (b) two-tone power sweep for receive front-end.

Figure 2.33 Measured and simulated (a) iIP3 and (b) iP1dB across frequency over 32 phase settings. Measured (c) iIP3 and (d) iP1dB across 32 phase settings at 29-31 GHz (solid symbols are for 4-bit results and empty symbols are for 5-bit results).

2.4.4 Four-Element Receiver Array Characterization

The block diagram and die photograph for the four-element receiver array are shown in Figs. 2.6 and 2.7. Now that individual front-end element is fully characterized, I measure the element-to-element matching as well as the isolation between elements. First, for matching, I compare the responses of all four chains at 90° phase setting. The results are shown in Fig. 2.34, where the data are normalized
to the response in the first element. This indicates RMS phase and gain mismatch errors of $<5^\circ$ and 0.6 dB, respectively. Low RMS phase and gain mismatch errors are achieved due to low mismatch between each receive channel and low amplitude and phase imbalance in the two-stage dual $X$ and $Y$ Wilkinson power combiners.

Isolation measurements demonstrate how the phase settings of an adjacent (aggressor) element affects the phase response of a given (victim) element. The coupling errors are obtained by measuring the response of element two at 0° phase setting when the settings of element one are changed across 32 phase states. The measured results in Fig. 2.35(a) and (b) show $<4.2^\circ$ of RMS phase isolation error and $<0.5$ dB of RMS gain isolation error at 25 to 35 GHz due to low magnetic coupling, low substrate coupling, and high combiner isolation between each receiver channel. In addition, Fig. 2.35(c) shows the isolation between non-adjacent elements, which improves, as expected.

![Figure 2.34](image)

**Figure 2.34** Measured element-to-element phase and gain matching, channels 1-4, at 90° setting.

## 2.5 Chapter Summary

My first research goal was to explore easily scalable phased-array architectures that have wide RF bandwidth capabilities while supporting multi-band operation and multi-Gb/s data rate commu-
Figure 2.35 Channel-to-channel isolation demonstrated through measured phase and gain errors in channel 1 as channels 2, 3, and 4 are swept across all phase settings. Channel 1 is held at 0° setting.

communication for future 28-GHz 5G systems. These have the potential to be met through the use of a dual-vector distributed beamformer. Key contributions in this chapter are (a) proposal of a novel dual-vector distributed beamforming architecture, (b) investigation of the calibration methodology for the proposed dual-vector distributed beamformer, and (c) experimental validation using a circuit prototype. In particular, a four-element dual-vector phased-array receiver has been demonstrated in 130-nm SiGe BiCMOS technology operating from 25 to 35 GHz. The design relies on dual-vector scalar-only weighting functions within each front-end to reduce size to 0.3 mm$^2$ per chain and increase fractional bandwidth to 24.5% (26.5 to 33.9 GHz). Each array element achieves 5.1 to 7 dB (5.1 to 8.5 dB) NF, -16.8 to -13.8 dBm (-16.4 to -12.9 dBm) $iP_{1dB}$, and -10.5 to -8.9 dBm (-10.4 to -6.8 dBm) $iIP_3$ across 4-bit (5-bit) phase settings. Average gain is 10.5 dB at 29.7 GHz and power consumption is 136 mW per element. Compared to other front-ends in Table 2.1, this work achieves among the lowest area and among the highest fractional bandwidths. As can be expected, active phase shifter topologies will consume more power over passive approaches. While dual-vector distributed beamforming eliminates the quadrature coupler from each front end, this area savings may be negated by the increased area in a dual parallel power combiner. This issue is addressed in
the following chapter, where I investigate dual series-combiner structure for DVDBs and evaluate for both receiver and transmitter arrays.
Table 2.1 Comparison of RF Phased-Array Receiver Front-Ends

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<td>26-28</td>
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<td>4-bit</td>
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<td>( V_{\text{Control}} )</td>
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<td>&lt; 4</td>
<td>&lt; 1</td>
<td>&lt; 3.9</td>
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<tr>
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<td>10</td>
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<td>20</td>
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<tr>
<td>Gain Error (dB)</td>
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<td>&lt; 0.5</td>
<td>&lt; 0.6</td>
<td>&lt; 0.35</td>
<td>&lt; 0.5</td>
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<td>NF (dB)</td>
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<td>7.8-9.5</td>
<td>4-4.7</td>
<td>3.8</td>
<td>6</td>
<td>5.3-6.9</td>
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<td>-22 to -19</td>
<td>-8</td>
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<td>-34 to -26</td>
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<tr>
<td>iIP3 (dBm)</td>
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<td>-12 to -9</td>
<td>0.5</td>
<td>-20</td>
<td>-</td>
<td>-</td>
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<td>DC Power (mW)</td>
<td>136.5 (97.5 w/o DACs)</td>
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<td>42</td>
<td>33</td>
<td>48.6</td>
<td>66.3</td>
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<td>RX Front-end Area (( mm^2 ))</td>
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<td>0.34**</td>
<td>1.24*</td>
<td>0.33*</td>
<td>0.77*</td>
<td>0.68*</td>
</tr>
</tbody>
</table>

* Estimated area per front-end element.
** Estimated area excluding any input balun per front-end element.
3.1 Phased-Array Transceiver Overview

This chapter presents a 28-GHz four-element phased-array transceiver in 130-nm SiGe BiCMOS technology for 5G cellular application. Once again, the array employs scalar-only weighting functions within each front end and a global quadrature function, enabling a small footprint for each element; however, a dual-vector series-fed network is employed to eliminate the area penalty associated
with dual-vector power combining. Measurements show that each receive front-end achieves 8.7 to 11.5 dB gain, 4.5 to 6.9 dB noise figure, -25.4 to -18.4 dBm input 1-dB compression point, and < 0.5-dB/2.1° RMS gain/phase error at 24 to 28 GHz. Each transmit-front end achieves 9.4 to 14.3 dB gain, 5.5 to 10.6 dBm output 1-dB compression point, and < 0.4-dB/4.2° RMS gain/phase error at 24 to 28 GHz. The four-element transceiver array occupies an area of 2.9 mm² and consumes 1.08 W in transmit mode and 0.68 W in receive mode.

3.1.1 Phased-Array Transceiver Architecture

Once again, the available bandwidth and reduced wavelength at Ka band (27-40 GHz) enable high-throughput communications for 5G mm-wave networks using compact antenna arrays. For these systems, wide-bandwidth, low-area, and scalable phased-array transceiver arrays are required. Transceiver arrays are used for time-division duplexing (TDD) in which only receivers or transmitters are operating at one time in the desired frequency band. Although the receiver (RX) and transmitter (TX) arrays can be built using two separate chips [Nat11; VG10; Sha13; Nat05; Gua04], integrating the TX and RX together is a desirable approach to save area and DC power consumption [Boe14; Coh13; Kim12] while allowing the sharing of multiple circuits, including the PLL, bias networks, and the on-chip digital SPI. Furthermore, transceiver arrays allow sharing of a single antenna array, saving space and simplifying the package and board designs.

As discussed in the previous chapter for receivers, four popular beamformer architectures that can be realized as a mm-wave phased-array transceiver (TRX) are RF-path, LO-path, BB-path, and digital-path beamforming. A summary of recent phased-array transceivers can be found in [PT12; Pug16]. Two important metrics to consider for a future 5G base station utilizing a large number of elements (~256) are the area and DC power consumption. These, in turn, set the cost and heat dissipation for the chip. RF beamforming is once again popular as it has the fewest replicated components in the receive and transmit chains. For this reason as well as the spatial-interferer rejection that occurs prior to mixing, RF beamforming is selected using the DVDB architecture.
Once the array is expanded to include both transmit and receive functions, there are important trade-offs with respect to bidirectionality of phase-shifting and combining networks. For example, the RF-path beamformer can be implemented by using passive or active phase shifter approaches, as shown in Fig. 3.1. The receive and transmit front-ends can share a single passive and bi-directional power combiner/splitter network as shown in Fig. 3.1(a). Here, multiple transmit/receive (T/R) switches are used to switch operation between the RX and TX modes. The phase shifter is passive and bidirectional and can be shared in both TX and RX modes [KR16; Kim12; Gha12; Liu16]. However, even for a single TRX front-end, the cascading of LC networks and VGAs can consume large areas of 12.76 mm$^2$ in [Gha12], 7 mm$^2$ in [Liu16], 1.75 mm$^2$ in [KR16], and 1.62 mm$^2$ in [Kim12]. Such a large area makes the scaling to a large array prohibitive. An alternative phase-shifting approach is the active vector interpolator, which creates phase shift and variable gain using weighted in-phase (I) and quadrature-phase (Q) vectors [Gol13; Ina13], as shown in Fig. 3.1 (b). Due to their uni-directionality, separate phase shifters are needed in both TX and RX front-ends, which doubles the area.

**Figure 3.1** RF-path architectures for the N-element TRX phased arrays using (a) bi-directional passive phase shifter and (b) uni-directional active phase shifter.
In the previous chapter, I demonstrated a 28-GHz dual-vector distributed beamformer (DVDB) receiver that employs scalar-only weighting functions within each front-end and global quadrature combining to realize beamforming [Yeh17a]. The hardware achieved good RF performance and supported two simultaneous beams; however, the architecture requires dual-differential power combiners which can be large if implemented in a shunt or parallel tree fashion. In this chapter, the goal is to investigate alternative combiner structures that are area efficient and then extend the DVDB into a full transceiver.

Fig. 3.2(a) illustrates the dual-vector distributed transceiver architecture including dual-vector scalar front-ends, dual-power combining or splitting networks, and a global quadrature combiner or splitter. In the RX mode, described in Fig. 3.2(b), down-conversion mixers at the output port of the 90° coupler are enabled and up-conversion mixers at the isolation port of the 90° coupler are disabled. The $\sum X$ and $\sum Y$ signals are fed to the $I$ and $Q$ ports of the 90° coupler. A main beam ($\sum X - j\sum Y$) is formed at the coupler output and is fed to the input of the down-conversion mixers. An image beam ($\sum Y - j\sum X$) is formed at the isolated output and dissipated in a termination resistor.

In TX mode, described in Fig. 3.2(b), down-conversion mixers at the isolated port of the 90° splitter are disabled and up-conversion mixers at the input port of the 90° splitter are enabled. The baseband IQ signals are up-converted to an RF signal that is further split into $I$ and $Q$ RF signals at the $I$ and $Q$ output ports of the 90° splitter. In either RX or TX mode, the $\sum X$ and $\sum Y$ signals are then distributed through the array and attached to each individual DVDB transmit/receive front-end.

Even though the dual-vector scalar front-end and a single global quadrature combiner/splitter can improve the area and the bandwidth of the array, the DVDB transceiver architecture has several design challenges and drawbacks. First, dual-differential power combining networks that provide $\sum X$ and $\sum Y$ signals are needed in the system. Parallel combining/splitting networks [Kim12; Kan09; Gol13] result in a low phase/amplitude mismatch between each TX or RX path and provide excellent isolation between input/output elements; however, their area is large due to the need for multiple $\lambda/4$ t-lines. For example, the dual-differential combiner of the DVDB RX array in the previous
chapter occupied 1.38 mm², or 45 % of the total array area [Yeh17a]. Smaller dual-differential combiners are required. Second, multiple T/R switches are needed between the front-end ports and the combining/splitting ports, which consumes area, complicates RF signal routing, and reduces bandwidth. Third, the frequency range over which the I and Q achieve accurate gain and phase matching within the 90° combiner/splitter can be limited by any narrow-band terminations at any of the four ports. This complicates calibration across frequency.

**Figure 3.2** (a) Block diagram of a dual-vector distributed architecture for an N-element TRX phased array using dual-vector VGAs, dual- power combiners/splitters, and a global quadrature combiner/splitter; and illustrations of the global 90° combiner/splitter in the dual-vector distributed architecture for (b) RX-mode and TX-mode operation.

### 3.1.2 Dual Series-Fed Power Combining and Splitting Approach

The above design challenges and limitations of the above design can be addressed by altering the architecture of the DVDB to include a dual series-fed power combining and splitting structure, as shown in Fig. 3.3. The series-fed approach in phased arrays has been demonstrated previously.
by multiple investigators, including a more recent version in [Nat07]. In a series-fed approach, a single combiner can be shared between transmit and receive front-ends without switching through a parallel coupling between the RX or TX and the feed line, where the parasitics of the RX or TX front-end are absorbed within the distributed line. The dual series-fed network is color-coded red for $\sum X$ and blue for $\sum Y$ within Fig. 3.3. Simple coplanar transmission lines (t-lines) with a desired characteristic impedance ($Z_0$) and length between each channel ($l_0$) are used to realize the feed network. Up- and down-conversion mixers can be placed on either end of the line, but in Fig. 3.3 they are represented as termination resistors at the output or input ports of the 90° combiner/splitter.

In the RX mode, shown in Fig. 3.3(a), each receiver front-end receives the input signal and generates dual in-phase output signals, $X_n$ and $Y_n$, scaled in a Cartesian manner to achieve the desired phase shift setting. The $X_n$ and $Y_n$ output signals are coupled into the dual-series-combiner and propagate along the t-lines in both directions. A 90° phase shift is then added to $\sum Y$ to yield a global vector interpolation at the output of the coupler. As discussed in the previous chapter, quadrature-combined signals can be used to realize a main beam ($\sum X - j \sum Y$) and an image beam ($\sum Y - j \sum X$). Note that in the RX mode, the opposite end of the series combiner is terminated, though an additional hybrid coupler and receiver can be placed at this end to allow for multi-beam operation, as will be discussed shortly.

In the TX mode, shown in Fig. 3.3(b), the global input RF signal is split into in-phase and quadrature-phase signals using the 90° splitter. These quadrature signals are then distributed across the array using the series splitter network. Note that this is the exact same network as used in the RX mode. The $I$ and $Q$ inputs for each transmit front-end are progressively tapped off (or coupled off) of the line into each TX front-end. Within each front-end, vector interpolators are used to weight the $I$ and $Q$ signals to achieve the desired phase shift setting. Similar to the receiver operation, the transmitter can support two beams, a main beam and an image beam, by using both of the input ports of the global hybrid coupler. Furthermore, couplers can be placed on both ends of the line to support four simultaneous beams, as will be discussed shortly.
The dual series-fed network provides several advantages, as follows. (1) It consumes much less area than a parallel network; (2) it allows wider bandwidth due to absorption of the parasitic capacitance into the t-lines and thereby the elimination of matching networks between the line and each front-end; (3) the T/R switch is no longer needed at the ports of the combining/splitting networks, which not only saves area but also improves the bandwidth; (4) high isolation between RX or TX elements can be achieved without the need of isolation arms; and (5) it provides broadband terminations for the passive hybrid couplers, which improves the bandwidth of the IQ phase and amplitude accuracies. Drawbacks are the phase and amplitude offsets that occur due to the signal distribution along a lossy series feed. This must be calibrated out to minimize the phase and amplitude mismatches between each RX and TX.

Figure 3.3 RF-path architectures for the four-element TRX phased array using dual series-fed power combining/splitting networks in (a) RX-mode and (b) TX-mode.
3.2 Multi-Beam Support

In the previous chapter, I presented a theory for dual-beam support within the DVDB. Here, I extend this theory for a series-fed DVDB and show how the forward and reverse propagation modes allow for four-beam support. First the derivation assumes a series-fed network with traditional phase shifters. Then, I modify the result for dual-vector beamforming. Assuming RX-mode operation, the received signal of the first element experiences a phase shift of $\alpha_1$. This signal is equally split at the output of the first element and propagates in both directions of the series combiner to outputs labeled $A$ and $B$, as shown in Fig. 3.4. The signal propagating towards output $A$ experiences additional phase shifts of $(N-1) \times \phi$ and an amplitude loss of $A^{N-1}$ due to the physical distance of the cascaded series-fed transmission lines (t-line) between each element. In contrast, the signal propagating towards output $B$ experiences no additional phase shift or amplitude loss, as it is closest to output $B$. For the $N^{th}$ element, the signal propagates towards output $A$ with no phase shift and no amplitude loss but towards output $B$ with phase shifts of $(N-1) \times \phi$ and amplitude loss of $A^{N-1}$.

I now review the beamforming operation to illustrate the beams that are formed at outputs $A$
and $B$. Array factors, $F_{OUTA}(\theta)$ and $F_{OUTB}(\theta)$, as functions of angle-of-arrival $\theta$ (zero corresponds to broadside) for an N-element linear array using the series-fed network are

$$F_{OUTA}(\theta) = \sum_{n=1}^{N} e^{j(n-1)\kappa d \sin(\theta)} a_n e^{-j\alpha_n A(N-n)} e^{j(N-n)\phi},$$

(3.1)

$$F_{OUTB}(\theta) = \sum_{n=1}^{N} e^{j(n-1)\kappa d \sin(\theta)} a_n e^{-j\alpha_n A(n-1)} e^{j(n-1)\phi},$$

(3.2)

where $\kappa$ equals $2\pi/\lambda$, $d$ is the antenna spacing of $\lambda/2$, $a_n$ is the amplitude shift per element, $\alpha_n$ is the phase shift per element, $A$ is the uniform amplitude loss of the series t-line between each element, and $\phi$ is the uniform phase shift of the series t-line between each element. To steer the main beam to angle $\theta_A$ at the output $A$, the phase shifters are set to $\alpha_n = (n-1)\kappa d \sin(\theta_A) + (N-n)\phi$, leading to a peak directivity of $N$ at angle $\theta_A$ if there is no amplitude loss ($A = 1$) between each element. For this element phase weighting, the second beam at output $B$ has its peak directivity at an angle of $\theta_B = \arcsin\left(\frac{\kappa d \sin(\theta_A)-2\phi}{\pi}\right)$.

The dual-beam system using the series-fed network can be extended into the multi-beam system by applying the dual-vector distributed concept. In particular, the presence of hybrid couplers at points $A$ and $B$ allows generation of two additional beams—a main beam and an image beam. In Fig. 3.5(a), the signal that arrives at angle $\theta$ is received, weighted, and combined at the output of $OUTA_1$ of the left $A$ coupler. With the same phase setting within each element, the signal is also weighted, and combined at the output of $OUTB_1$ of the right $B$ coupler in Fig. 3.5(b). The array factor, $F_{OUTA_1}(\theta)$ and $F_{OUTB_1}(\theta)$, as functions of angle-of-arrival $\theta$ (zero corresponds to broadside) for an N-element linear array using a series-fed approach are

$$F_{OUTA_1}(\theta) = \sqrt{2} \sum_{n=1}^{N} \left( a_n e^{j(n-1)\kappa d \sin(\theta)} \cos(\alpha_n) - j a_n e^{j(n-1)\kappa d \sin(\theta)} \sin(\alpha_n) A(N-n) e^{j(N-n)\phi} \right).$$

(3.3)
Figure 3.5 Dual-vector distributed array using series-fed networks when the signals are collected at (a) the outputs of the $A$ coupler and (b) the outputs of the $B$ coupler.

$$F_{OUTB_i}(\theta) = \frac{\sqrt{2}}{2} \sum_{n=1}^{N} \left( X_n e^{j(n-1)\kappa d \sin(\theta)} \cos(\alpha_n) - j X_n e^{j(n-1)\kappa d \sin(\theta)} \sin(\alpha_n) \right) A^{(n-1)} e^{j(n-1)\phi}, \quad (3.4)$$

where the $\sqrt{2}/2$ accounts for the power split in the quadrature combiner, $\kappa$ equals $2\pi/\lambda$, $d$ is the antenna spacing of $\lambda/2$, $\theta$ is the arrival angle, $a_n$ is the amplitude shift per element, $\alpha_n$ is the phase shift per element, $A$ is the uniform amplitude loss of the series $t$-line between each element,
and $\phi$ is the uniform phase shift of the series t-line between each element. Signals $X_n$ and $Y_n$ are the Cartesian expansions of the amplitude- and phase-shift for the $n^{th}$ element, depicting vector interpolation. To steer the main beam to angle $\theta_0$ at the first output of the left $A$ coupler, the phase shifters are set to $\alpha_n = (n - 1)kd \sin(\theta_0) + (N - n)\phi$, leading to a peak directivity of $N$ at angle $\theta_0$ if there is no amplitude loss ($A = 1$) between each element, i.e., reflected across broadside. Note that Euler’s formula shows that

$$\cos(\alpha_n) = \frac{e^{j\alpha_n} + e^{-j\alpha_n}}{2}, \quad (3.5)$$

$$\sin(\alpha_n) = \frac{e^{j\alpha_n} - e^{-j\alpha_n}}{2j}, \quad (3.6)$$

This illustrates why there are two peaks for the combined signals of $\sum X_n$ and $\sum Y_n$ due to the equations 3.5 and 3.6, which I discussed in the previous chapter.

Now I revise the patterns of $\sum X_n$ and $\sum Y_n$ to account for the progressive phase shift of $\phi$ due to the series-fed network. The array factors of $\sum X_n$ and $\sum Y_n$ at the first output of the $A$ coupler are shown as follows

$$F_{OUTA, X_n}(\theta) = \frac{1}{2} \sum_{n=1}^{N} a_n A^{(N-n)} \left( e^{j((n-1)kd \sin(\theta)+(N-n)\phi+a_n)} + e^{j((n-1)kd \sin(\theta)+(N-n)\phi-a_n)} \right), \quad (3.7)$$

$$F_{OUTA, Y_n}(\theta) = \frac{1}{2j} \sum_{n=1}^{N} a_n A^{(N-n)} \left( e^{j((n-1)kd \sin(\theta)+(N-n)\phi+a_n)} - e^{j((n-1)kd \sin(\theta)+(N-n)\phi-a_n)} \right) \quad (3.8)$$

Once the desired phase shift of $\alpha_n = (n - 1)kd \sin(\theta_0) + (N - n)\phi$ is applied into the array factors of phase-shift $\sum X_n$ and $\sum Y_n$, the main beam is fixed but the image beam is shifted due to the phase shift $\phi$ of the series-fed network. For dual-vector distributed beamforming, we apply the summation to all $X$ and $Y$ signals and then pass these summations through a global $90^\circ$ hybrid coupler. For the first output of the left $A$ coupler, $\sum Y_n$ undergoes a $-90^\circ$ phase shift, yielding a first
array factor of the desired main beam

\[
F_{OUT A_1}(\theta) = \frac{\sqrt{2}}{2} \sum_{n=1}^{N} A^{N-n} e^{j(N-n)\phi} (X_n - j Y_n) = \frac{\sqrt{2}}{2} \sum_{n=1}^{N} a_n A^{N-n} e^{j((n-1)kd \sin(\theta)+(N-n)\phi-a_n)},
\]

(3.9)

which is identical to the equation 3.1 except the magnitude is scaled by \(\sqrt{2}/2\) due to the power split.

For the second output of the left A coupler, \(\sum X_n\) undergoes a -90\(^\circ\) phase shift, yielding a second, "image" array factor

\[
F_{OUT A_2}(\theta) = -j\frac{\sqrt{2}}{2} \sum_{n=1}^{N} A^{N-n} e^{j(N-n)\phi} (X_n + j Y_n) = -\frac{j\sqrt{2}}{2} \sum_{n=1}^{N} a_n A^{N-n} e^{j((n-1)kd \sin(\theta)+(N-n)\phi+a_n)},
\]

(3.10)

This image pattern is the conjugate of the \(F_{OUT A_1}\) pattern multiplied by a global -90\(^\circ\) phase shift. As such, for the same phase shifter settings described above, the second output of the A coupler exhibits a peak directivity of \(N\) at angle of \(\theta'_0 = \arcsin\left(\frac{-(kd \sin(\theta_0)-2\phi)}{\pi}\right)\).

On the other side of the first output of the right B coupler in Fig. 3.5(b), \(\sum Y_n\) undergoes a -90\(^\circ\) phase shift, yielding a third array factor from the equation (3.4)

\[
F_{OUT B_1}(\theta) = \frac{\sqrt{2}}{2} \sum_{n=1}^{N} A^{(n-1)} e^{j(n-1)\phi} (X_n - j Y_n) = \frac{\sqrt{2}}{2} \sum_{n=1}^{N} a_n A^{(n-1)} e^{j((n-1)kd \sin(\theta)+(n-1)\phi-a_n)},
\]

(3.11)

As such, for the same phase shifter settings described above, the first output of the B coupler exhibits a peak directivity of \(N\) at angle of \(\theta''_0 = \arcsin\left(\frac{+kd \sin(\theta_0)-2\phi}{\pi}\right)\), which is the image beam of the second output of the A coupler. For the second output of the B coupler, \(\sum X_n\) undergoes a -90\(^\circ\) phase shift, yielding a fourth, "image" array factor

\[
F_{OUT B_2}(\theta) = -j\frac{\sqrt{2}}{2} \sum_{n=1}^{N} A^{(n-1)} e^{j(n-1)\phi} (X_n + j Y_n) = -\frac{j\sqrt{2}}{2} \sum_{n=1}^{N} a_n A^{(n-1)} e^{j((n-1)kd \sin(\theta)+(n-1)\phi+a_n)},
\]

(3.12)

This image pattern is the conjugate of the \(F_{OUT B_1}\) pattern multiplied by a global -90\(^\circ\) phase shift. As such, for the same phase shifter settings described above, the first output of the B coupler exhibits...
a peak directivity of $N$ at angle of $\theta_0'' = \arcsin\left(\frac{-kd \sin(\theta_0)}{\pi}\right) = -\theta_0$, which is the image beam of the first output of the $A$ coupler. As can be seen, this architecture can simultaneously support four beams. This can provide additional capabilities for an MIMO system employing hybrid analog/digital precoding [Gao16], wherein the dual-vector distributed beamformers serve as multi-beam sub-arrays for the system. Multiple multi-output sub-array responses can be combined to synthesize desired patterns. Additionally, a fast, switched-beam capability can be provided, wherein the receiver can either quickly switch between four available patterns or use all four patterns simultaneously.

![Figure 3.6](image)

**Figure 3.6** Calculated (a) $F_{OUT A_1}$, (b) $F_{OUT A_2}$, (c) $\sum X$ at $OUT A$, and (d) $\sum Y$ at $OUT A$, when beam one is steered to $-30^\circ$ with the phase shift $\phi$ of 0-30° and with the no amplitude loss of $A = 1$ for $\lambda/2$-spaced linear array. All patterns normalized by $N=16$.

Figs. 3.6(a) and (b) show examples of normalized patterns from Matlab for $F_{OUT A_1}$ and $F_{OUT A_2}$, respectively, for 16-element series-fed linear arrays ($\lambda/2$ spacing) controlled such that beam one steers to -30°. Figs. 3.6(c) and (d) show examples of patterns for $\sum X$ and $\sum Y$, respectively, for these same scenarios, indicating that both exhibit peaks at both desired angle and conjugate angle with the series-fed phase shift $\phi$ of 0 to 30°. Figs. 3.7(a) and (b) show examples of normalized patterns for $F_{OUT R_1}$ and $F_{OUT R_2}$, respectively, for 16-element series-fed linear arrays ($\lambda/2$ spacing) controlled such that beam one steers to -30°. Fig. 3.7(c) and (d) show example patterns for $\sum X$ and $\sum Y$, 70
Figure 3.7 Calculated (a) $F_{OUTB_1}$, (b) $F_{OUTB_2}$, (c) $\sum X$ at $OUTB$, and (d) $\sum Y$ at $OUTB$, when beam one is steered to $\theta = -30^\circ$ with the phase shift $\phi$ of 0-30° and with the no amplitude loss of $A = 1$ for $\lambda/2$-spaced linear array. All patterns normalized by $N=16$.

respectively, for these same scenarios, indicating that both exhibit peaks at both desired angle and conjugate angle with the series-fed phase shift $\phi$ of 0 to 30°. Figs. 3.8(a) and (b) show examples of normalized patterns for $F_{OUTA_1}$, $F_{OUTA_2}$, $F_{OUTB_1}$, and $F_{OUTB_2}$, respectively, for 16-element linear arrays ($\lambda/2$ spacing) controlled such that beam one $F_{OUTA_1}$, steers to $\theta = -30^\circ$ with the phase shift $\phi$ of 0 and 30°.

Figure 3.8 Calculated $F_{OUTA_1}$, $F_{OUTA_2}$, $F_{OUTB_1}$, and $F_{OUTB_2}$, when beam one $F_{OUTA_1}$, is steered to $\theta = -30^\circ$ (a) with the phase shift $\phi$ of 0° and (b) with the phase shift $\phi$ of 30°. There is no amplitude loss of $A = 1$ for $\lambda/2$-spaced linear array. All patterns normalized by $N=16$.  

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With this foundation, we can now discuss non-idealities for this system. First, both individual X and Y signals must experience the amplitude loss due the physical length of the series-fed t-lines. Introducing this amplitude loss arbitrarily to the four patterns in (3.9, 3.10, 3.11, 3.12), we find...
that any amplitude loss, $A$, would result in degradation of the main desired beam and imperfect cancellation of the undesired pattern. Figs. 3.9(a) and (b) show examples of normalized patterns experiencing the amplitude loss of $A=0.9$ to 1 for $F_{OUTA_1}$ and $F_{OUTA_2}$, respectively, for 16-element series-fed linear arrays ($\lambda/2$ spacing) controlled such that beam one steers to -30°. Figs. 3.9(c) and (d) show examples of patterns for $\sum X$ and $\sum Y$, respectively, for these same scenarios, indicating that both exhibit peaks both at the desired angle and the conjugate angle with the series-fed phase shift $\phi$ of 30°. Fig. 3.10(a) and (b) show example normalized patterns experiencing the amplitude loss of $A=0.9$ to 1 for $F_{OUTB_1}$ and $F_{OUTB_2}$, respectively, for 16-element series-fed linear arrays ($\lambda/2$ spacing) controlled such that beam one steers to -30°. Figs. 3.10(c) and (d) show examples of patterns for $\sum X$ and $\sum Y$, respectively, for these same scenarios, indicating that both exhibit peaks at both desired angle and conjugate angle with the series-fed phase shift $\phi$ of 30°.

### 3.3 series-fed Dual-Vector Distributed Transceiver Array Implementation

A DVDB transceiver array was designed and fabricated in 130-nm SiGe BiCMOS 8HP from Global-Foundries. The block diagram of this “second generation (Gen-2)” of the transceiver array is shown in Fig. 3.11. In the sub-array, four transmit front-ends and four receive front-ends are interdigitated, sharing dual-series feed networks and a global hybrid coupler. To simplify testing, the $\sum X$ and $\sum Y$ outputs of the dual-series-fed networks are combined and terminated using one differential hybrid coupler on one side. The other side of the series-fed network is terminated with differential 100 Ω resistors, which improves the bandwidth of quadrature accuracy due to the broadband terminations for the passive hybrid couplers. A chip micrograph of the TRX array is shown in Fig. 3.12 and the die size is 6.9 mm$^2$ including pads and 2.9 mm$^2$ excluding pads. A single element occupies 0.2/0.15 mm$^2$ for an RX/TX front-end. The total power dissipation is 1080/680 mW in the TX/RX modes.

A block diagram and the performance target of the RX front-end was shown previously in
Fig. 2.8, and the diagram and performance targets for the TX are shown in Fig. 3.13, both for 5G basestation application. Each TX front-end requires a power amplifier (PA) and a vector-interpolating RF phase shifter. A fully differential architecture is selected to reduce the impact of finite supply-plane impedance on circuit performance and stability, at the cost of nearly a doubling of the front-end power consumption for the same transistor current density. The following section describes the design details for each element in the system.

![Figure 3.11](image)

**Figure 3.11** Block diagram of realized four-element phased-array transceiver employing series-fed distributed beamforming for the Gen-2 sub-array.

### 3.3.1 Transformer-Based T/R Switch

In multi-antenna time-division duplex (TDD) systems, integrated T/R switches allow sharing of a single antenna array with RX and TX arrays. This reduces the size of the antenna array and simplifies the board-level or package-level design complexity. In this section, I present a 28-GHz T/R switch for potential use in the DVDB transceiver array.
Figure 3.12 Die micrograph of four-element phased-array transceiver for the Gen-2 sub-array.

Figure 3.13 (a) Detailed block diagram of transmitter front-end and (b) TX performance specifications.

Single-pole double-throw (SPDT) T/R switches have been widely used in wireless communication systems [Par08; MR08a; Poh12; HR05]. The traditional SPDT switch for mm-wave bands, shown in Fig. 3.14(a), consists of a long quarter-wave t-line to translate a short to open as a shunt switch is turned on. Achieving an ideal ground is challenging due to the finite $R_{on}$ of the large switch. Large
\(C_{off}\) needs to be resonated out by a shunt inductor (L) which narrows bandwidth and increases area. Here, a transformer-based SPDT switch is proposed to provide good isolation without using a large shunt switch while shortening the length of the \(\lambda/4\) t-line to \(\lambda/8\), as shown in Fig. 3.14(b).

Fig. 3.15 (a) shows the simplified schematic of the transformer-based SPDT T/R switch. The symmetric design of the SPDT switch consists of a \(\lambda/8\) t-line, a transformer, and a shunt saturated SiGe HBT switch in each TX and RX path. The transformer serves two important purposes. First, it allows reduction of the t-line length and second, it allows resonance of the switch’s shunt capacitance in the off state. Control voltages for \(V_{TX}\) and \(V_{RX}\) are applied to the base resistors of the switches to select TX or RX mode operation, with 2.5 V used for the on state and 0 V used for the off state. A series of base choke resistors of \(R_1\) are used as AC-blocking RF with value of 1.4 kΩ. Higher \(R_1\) is preferred to prevent power loss from coupling from collector to base terminals. This improves insertion loss (IL). However, higher \(R_1\) results in higher DC voltage drop due to base current, which requires higher control voltages to completely turn on the switch. In addition, high \(R_1\) slows the 10%-to-90% turn-on switching time (\(T_{sw}\)) due to the high RC time constant of \(R_1\) and parasitic base capacitance of the switch [Par08]. The proper sizing of the switches \(Q_1\) and \(Q_2\) is determined based on the trade-off of the on-resistance (\(R_{on}\)) in the saturated region and off-capacitance (\(C_{off}\)) in the cut-off region. Lower \(R_{on}\) is preferred for better isolation preventing power leakage in the two operation modes. The emitter length of switches \(Q_1\) and \(Q_2\) is chosen as 5 \(\mu m\) with \(R_{on}\) of 17.1 Ω and \(C_{off}\) of 15.1fF. The small size of switches with low parasitic base capacitance of 2.8 fF also improves the switching time \(T_{sw}\) to be less than 4 ps. EM simulation shows that the \(\lambda/8\) t-line with \(Z_0\) of 51 Ω achieves a loss of 0.1 dB at 28 GHz and its cross-section is shown in Fig. 3.16. The stacked transformer is designed with two-turn primary inductance of 620 pH with peak Q of 12.3 and two-turn secondary inductance of 620 pH with peak Q of 9.2. The simulated loss of the transformer is 0.85 dB with coupling factor K of 0.82 at 28 GHz. The majority of the insertion loss of the SPDT switch comes from the transformer loss.
Figure 3.14 (a) A SPDT based on quarter-wave (λ/4) t-lines and shunt switches, and (b) a proposed SPDT based on λ/8 t-lines, transformers, and shunt switches.

Figure 3.15 (a) simplified schematic of transformer-based SPDT and (b) its transmit- and receive-mode operation.

3.3.2 Transceiver Front-End

The block diagram and the schematic of the transceiver front-end consisting of the receiver front-end (left), dual-series-fed t-lines (center), and transmitter front-end (right), are shown in Fig. 3.17. Both the receiver and transmitter front-ends share a single global quadrature combiner/splitter (top). The following section describes details for each circuit block in the front-end.
3.3.2.1 Transmitter Front-End

The transmitter front-end consists of a phase shifter and a power amplifier (PA), as shown in Fig. 3.17. The detailed schematic of the phase shifter is shown in Fig. 3.18 and it consists of in-phase (I) and quadrature-phase (Q) variable-gain amplifiers (VGAs) with current summing, and two binary-weighted current DACs. In the TX mode, the inputs of the I and Q VGAs are directly connected to the differential I/Q series feed network driven by a global quadrature splitter. The input capacitance of the $G_m$ stage ($Q_{1-4}$) is absorbed into the series feed network; hence, no resonant input matching is required. The amplitudes of I and Q signals are weighted by current-steering cross-coupled transistors $Q_{5-12}$, according to $\cos(\alpha_n)$ and $\sin(\alpha_n)$ functions, respectively, where $\alpha_n$ is the desired phase shift of the $n$th element. The weighted I and Q signals are combined in current domain and flow into a common-base stage, $Q_{13-14}$, which provides a low impedance at its emitter nodes. An inter-stage transformer $M_2$ translates impedance and drives the PA with compact layout.

The single-stage power amplifier (PA) employs a balanced cascode biased in Class-AB and sized to enable $>17$-dBm $P_{1dB}$ summarized in in Fig. 3.13 (b). The detailed schematic of the PA is shown in Fig. 3.19 (a). The PA is driven directly by an inter-stage transformer $M_2$ from the VI output. To achieve a desired 17-dBm $P_{1dB}$, the size of the PA is chosen as 9.4 $\mu$m with eight fingers for the
Figure 3.17 Block Diagram and Schematic of transceiver front-end in the Gen-2 subarray, with receiver front-end (left), series-fed network (center), and transmitter front-end (right).

bottom and top NPN devices of Q$_{1-4}$. The bottom devices of Q$_{1-2}$ are biased through a current mirror and the base voltage of 1.7 V for the top devices Q$_{3-4}$ is provided by the output of unity-gain feedback OPAMP using the same current mirror. The OPAMP can prevent the reference current, $I_{ref}$, from flowing into the bases of the Q$_{3-4}$, which causes the drop of the $I_{ref}$. The knee voltage of the cascode PA is approximately 0.9V and the supply voltage is 3.3 V. As a result, the output voltage
amplitude is 2.4 V, corresponding to a peak collector voltage of 5.7 V and a peak collector-to-base voltage of 4 V. The breakdown voltages of the PA should be limited by the $BV_{CBO}$ of 6 V due to the high impedance at the collector of the bottom devices $Q_{1-2}$, rather than the $BV_{CEO}$ of 1.8 V due to the AC short at the bases of the top devices $Q_{3-4}$. Therefore, this high voltage swing can be handled properly by the high $f_t$ NPN in SiGe 8HP technology. As a result, the output current amplitude is set to be 42 mA, dictated by a 17-dBm $oP_{1dB}$ target (21 mA on each side resulting in 0.28 mA/$\mu$m.)

With the calculated values of 2.4-V voltage amplitude and 42-mA current amplitude, the optimum fundamental impedance of $R_{opt}$ is 57 Ω. A load-pull simulation in Fig. 3.19 (b) shows that the optimum fundamental impedance for $>17$-dBm $oP_{1dB}$ is located on the 50-Ω circle which is close to the calculated load-line value. Fig. 3.19 (b) also indicates that $>18$-dBm $oP_{1dB}$ can be achieved with an optimum $Z_{opt}$ of $30+j40$ Ω at the fundamental frequency of 28 GHz. Finally, with the device size and operating current, the optimum impedance $Z_{opt}$ can be set and provided through an output transformer $M_1$ with optimal output loading condition and single-ended output.
3.3.3 Receive Front-end

The receiver (RX) front-end consists of a low-noise amplifier (LNA) and a dual-vector variable gain amplifier (DVGA), as shown in Fig. 3.17.

The schematic of the Gen-2 LNA is shown in Fig. 3.17 and the design is almost identical with the Gen-1 LNA except the collector inductors. The output collector spiral inductors are replaced with coplanar transmission lines, $T_{1-2}$, with 181 pH and Q of 12.8. In this way, the area of the coplanar transmission lines can be smaller than the spiral inductors, reducing the physical distance between RX and TX front-ends. In simulation, the LNA achieves a small-signal gain of 15.7 dB, NF of 3.8 dB, $iP_{1dB}$ of -5.8 dBm, and $iP_3$ of 5.9 dBm, all at 28 GHz. The LNA draws 16 mA from a 3.3-V supply (52.8 mW).

Compared to our prior work with the Gen-1 DVGA designs, the Gen-2 DVGA is modified, merging the required pre-distortion function of the DVGA with the transconductance ($G_M$) cell to save headroom. In addition, the large NF variation of the Gen-1 DVGA across the phase states is due
to the use of the cross-coupled common-base configuration as the predistortion cell. Merging
the $G_m$ cell and the predistortion cell into a single block with the cross-coupled common-emitter
configuration can minimize the NF variation across the phase states. A detailed schematic of the
Gen-2 DVGA with DACs is shown in Fig. 3.20. The DVGA $G_m$ is boosted by mutual coupling of $M_0$
between the input series base inductors and emitter inductors [Zha14]. During pre-distortion, Q3
and Q4 are turned on and controlled by DAC_A to reduce the input signal. At the phase settings of $0^\circ$, $90^\circ$, $180^\circ$, and $270^\circ$, the pre-distortion cells of Q3-4 are turned on the most with the strongest pre-
distortion signals so that a big portion of the RF currents from the $G_M$ cells of Q1-2 are canceled. This
leads to poor linearity performance at large-signal operation. At the phase settings of $45^\circ$, $135^\circ$, $225^\circ$,
and $315^\circ$, the pre-distortion cells of Q3-4 are completely turned off without the pre-distortion signals
so that the linearity is higher. The pre-distorted signal is then split and weighted by current-steering
cells Q5-12. Each RX front end creates two in-phase signals, $X_n$ and $Y_n$, which are weighted according
to $\cos(\alpha_n)$ and $\sin(\alpha_n)$, where $\alpha_n$ is the desired phase shift of the n$^{th}$ element. A common-base stage,
Q13-16, is used at the outputs to minimize the phase variation due to the finite output impedance of
Q5-12 when $X_n$ and $Y_n$ currents are steered. Outputs of the DVGA are combined through the dual
(X/Y) series feed network, with the output parasitic capacitance absorbed into the line to avoid any
need for resonant matching. Note that the 3.3-V supply voltage for the DVGAs is provided through
these series feed networks and the global quadrature combiner/splitter.

3.3.4 Transceiver Front-End with Asymmetric Transformer-Based T/R Switch

The block diagram of the transceiver (TRX) front-end is shown in Fig. 3.21 (a). The TRX front-end
consists of an asymmetric transformer-based T/R switch, a receiver (RX) front-end, and transmitter
(TX) front-end, X/Y series-fed networks, and a single quadrature combiner/splitter. The co-design
of the LNA, PA, and T/R switch enables the incorporation of the switch matching network into the
design of LNA and the PA, minimizing area and loss.

The schematic of the asymmetric transformer-based T/R switch is shown in Fig. 3.21 (b) and (c).
When compared with the symmetric transformer-based T/R switch in the previous section, this approach is a fully differential design for the differential LNA and the balanced PA. Also, one $\lambda/8$ t-line is eliminated on the TX side, which not only reduces area but also improves the TX’s output power.

In the RX mode in Fig. 3.21 (b), the PA is powered down, the LNA is powered up, and the shunt switches at the input of the LNA are switched off. The switches are implemented with 5-$\mu$m NPN transistors of $Q_1$ and $Q_2$ and 1.4-k$\Omega$ resistors of $R_1$ and $R_2$ at the base terminal. The small size of the switch reduces the off parasitic capacitance $C_{\text{off}}$ that can be resonated out by the secondary inductor of the LNA input transformer $M_{\text{LNA}}$. The small $C_{\text{off}}$ of 15.1 fF also can improve the switch time between the RX and TX modes due to a small $RC$ time constant. The RX input matching network consists of input capacitors, the PA output transformer $M_{\text{PA}}$, a differential $\lambda/8$ t-line, and the LNA input transformer $M_{\text{LNA}}$. This network also provides the input noise and power matching for the LNA, as shown in Fig. 3.21 (a). Even though this asymmetric approach improves the area and the switch time, the RX noise figure is degraded mainly due to the losses of the two transformers.
\[ M_{LNA} \text{ and } M_{PA} \text{ and the RF leakage signal flowing into the big parasitic capacitance at the output of the switched-off PA.} \]

In the TX mode in Fig. 3.21 (c), the PA is powered up and the LNA is powered down. The shunt switches at the input of the LNA are switched on with an on-resistance \( R_{on} \) of 17.1 \( \Omega \). Since the shunt switches are located at the secondary inductor of \( M_{LNA} \), an AC ground is provided through the center tap of the primary inductor of \( M_{LNA} \) so that the good isolation from the PA’s output to the LNA’s input can be isolated well due to the high input impedance \( Z_{in} \) of the \( \lambda/8 \) t-line, as shown in Fig. 3.21 (b). As a result, the RF leakage from the switched-on PA output to the switched-off LNA input can be minimized to improve the TX’s output power. The TX output matching network consisting of output capacitors and the transformer \( M_{PA} \) translates the differential outputs to the single-end output and provides the optimal impedance for the balanced PA to achieve the required output power. The approach of the asymmetric transformer-based T/R switch leads to area reduction, switch-time improvement, and TX output power enhancement but RX NF degradation.

**Figure 3.21** (a) Block diagram of the transceiver front-end with the asymmetry T/R switch, and the operations in (b) RX mode and (c) TX mode.
Figure 3.22 (a) the noise and power matching for the LNA input in RX mode at 23-33 GHz and (b) high input impedance $Z_{ISO}$ looking into the $\lambda/8$ t-line in the TX mode at 23-33 GHz.

### 3.3.5 Dual-series-fed Power Combiners/Splitters

The 3D structure of the dual-differential series-fed network and cross-sections of the parallel edge-coupled CPW are illustrated in Fig. 3.23. The geometry of the series lines is chosen to realize a differential 100-$\Omega$ impedance. One side of the series combiner is terminated with differential 100-$\Omega$ resistors and the other with the quadrature hybrid. Note that it is possible to terminate both ends of the series network with hybrid couplers and thereby increase the number of beams from two to four; however, this does lead to a narrower bandwidth for quadrature accuracy. In this prototype, we chose to realize only single-beam support to simplify testing.

### 3.3.6 Passive Global Quadrature Combiner

The global quadrature combiner/splitter is realized using a pair of 90° Lange couplers for quadrature generation and then a transformer balun. The schematic and the 3D structure of the global quadra-
Figure 3.23 Illustration of 3D views of dual-differential series-fed power combiners/splitters, and the cross sections of parallel edge-coupled CPW with back-side ground to realize 100-Ω $Z_{0,diff}$.

ture combiner/splitter are shown in Fig. 3.24. The couplers are modified for the differential 100 Ω terminations in the Gen-2 sub-array. At the isolation ports of the couplers, the isolation resistors are merged with bias tees to provide the 3.3-V supply voltages for four DVGAs during RX-mode operation. Note that the isolation ports of the coupler can be taken as the second input/output ports to obtain the second image beam. The central tap of the secondary inductor of the transformer is also attached to the 3.3-V supply voltages for supplying four DVGAs. The transformer balun is used for translating differential ports to a single-ended port for measurement purposes.

3.4 Measurement Results

3.4.1 T/R Switch Characterization

A single-pole double-throw switch has been realized in 0.13-μm SiGe BiCMOS 8HP technology from Global Foundries. A chip micrograph is shown in Fig. 3.25. The die size is 0.53 mm$^2$ including pads and the switch area is 0.11 mm$^2$ excluding the pads. The chip consumes 1.7 mW power. All
Figure 3.24 Illustrations of (a) the schematic and (b) the 3D structure of top-level layout of quadrature combiner composed of an input distribution network, a pair of Lange couplers, RF chokes, and an output transformer.

Figure 3.25 Die photograph of a single-pole double-throw (SPDT) T/R switch measurements were performed through wafer probing. S-parameters were taken using a two-port Agilent E8361C 67-GHz network analyzer. The measured S-parameters of the SPDT are well matched with simulation results shown in Fig. 3.26. In the RX mode, the measured insertion loss (IL) is 2 dB at 31 GHz with $V_{TX} = 2.5$ V and $V_{RX} = 0$ V, as shown in Fig. 3.26 (a). The measured 1-dB and 3-dB IL
bandwidths are from 19.6 to 35.8 GHz and from 14.7 to 41 GHz, covering the K- and Ka- bands. In the TX mode, the measured IL is 2.4 dB at 28.8 GHz slightly higher than IL in RX mode with isolation of 17.5 dB from the TX to RX ports at $V_{TX} = 0$ V and $V_{RX} = 2.5$ V. The return losses (RL) of more than 10 dB are achieved from 20 to 41.8 GHz at antenna port and from 20.7 to 26.9 GHz at the RX and TX ports. The insertion losses in both RX and TX modes can be improved by reducing the loss of the transformers and improving the RL at RX and TX ports.

Figs. 3.27 (a) and (b) show the one-tone power-sweeping measurement of SPDT in the receive mode at 28 GHz. The measured output power agrees with simulation as the input power varies from -6 to 15 dBm. Due to limitation of maximum power generation, the $iP_{1dB}$ of 21.4 dBm is predicted by simulation. Fig. 3.27 (c) shows that SPDT achieves $iIP_3$ of 32.9 dBm with the fundamental tone at 28 GHz with 10 MHz frequency offset.

This works demonstrates the transformer-based SPDT T/R switch prototype at Ka-band applications in the 130-$\mu$m SiGe BiCMOS technology. The 1:1 transformer is implemented to shorten the quarter-wave t-line into half length of $\lambda/8$ while using the small shunt switches with fast switching time $T_{sw}$. The measured results are summarized in Table 3.1.

![Figure 3.26](image.png)

**Figure 3.26** Simulated (dashed) and measured (solid) S-parameters of SPDT in (a) receive mode and (b) transmit mode
3.4.2 Power Amplifier Characterization

A stand-alone PA breakout consisting of the PA core and input and output baluns was measured. The die photo of the PA with input and output baluns is shown in Fig. 3.28. For small-signal characterization, Fig. 3.29(a) shows the measured scattering parameters with $> 20\text{-dB } S_{21}$ over wide frequencies and Fig. 3.29(b) shows the two-tone measurement of $+33\text{-dBm output-referred third-order intercept point (oIP}_3$) at 28 GHz with 100 MHz offset frequency. For large-signal characterization, wafer-level measurements in Fig. 3.30 show the PA gain, output power, and power-added efficiency (PAE) across input power and frequency. The PA achieves 21.2-dB gain, 14.8-dBm $\text{oP}_{1\text{dB}}$, and 38.9% peak PAE at 28 GHz. At $\text{oP}_{1\text{dB}}$, the PA consumes 161 mW from a 3.3-V supply.

3.4.3 Single-Element Transceiver Front-End with T/R Switch Characterization

A chip micrograph of the transceiver front-end with the asymmetric T/R switch is shown in Fig. 3.31. The die size is 2.8 mm$^2$ including pads. The chip consumes 318.5 mW in transmit mode and 157
Table 3.1 Comparison of SPDT T/R switches

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<td>-4.3 to -1.6</td>
<td>1.9 (NF 13.1 dB)</td>
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<td>20.3 to 58</td>
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<td>0.55**</td>
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* Simulated results. ** Estimated area excluding the pads.

mW in receive mode.

3.4.3.1 Transmitter Front-End with T/R Switch Characterization

Measured phase of the RX front-end with T/R switch across 32 phase settings is shown in Fig. 3.32 and Fig. 3.33. Fig. 3.32 (a) shows the measured phase of \(S_{21}\) of the single-channel receiver front-end across phase settings and the RMS phase error is less than 5.6° across 16-32.4 GHz. Fig. 3.32 (b) shows the differential nonlinearity (DNL) and integral nonlinearity (INL) of the phase responses, indicating errors less than ±0.6 LSB. The average peak gain is 28.9 dB at 20.1 GHz and 22.4 dB at
28 GHz in Fig. 3.33 (a). This frequency shift is due to mistuning of the inter-stage matching at the vector interpolator’s output. After calibration, the RMS gain error is less than 1 dB across 16-33.4 GHz. Figs. 3.33(b) and (c) show the magnitude of $S_{21}$ and gain deviation from the average gain over 32 phase settings at 24 to 28 GHz. The gain deviation is less than ±1 dB and can be improved by further biasing adjustment of the VGAs. Furthermore, to evaluate the quadrature accuracy within the front-end, we compare the amplitude and phase difference between axis settings (0° and 90°). Figs. 3.34 (a) and (b) show measured phase error less than 3° from 20.1 to 30.9 GHz and amplitude
Figure 3.30 Gen-2 PA measured (a) $oP_{1dB}$, gain, and PAE responses vs. frequency, and (b) $P_{out}$, gain, and PAE responses vs. $P_{in}$ at 28 GHz.

Figure 3.31 Die micrograph of the transceiver front-end with the asymmetry T/R switch. Die size is 2 x 1.4 mm$^2$.

error less than 1-dB from 16 to 30.4 GHz. The NF is 17.5-23.9 dB at 24-28 GHz across 32 phase settings, shown in Figs. 3.35(a) and (b). Due to the mistuning in the interpolator, the measured TX $oP_{1dB}$ and $P_{SAT}$ is reduced to 4.4 to 8.3 dBm and 14.9 to 18.5 dBm, at 24-28 GHz across 32 settings, as shown in Figs. 3.35 (c) and (d). The TX output power performance can be improved by fixing
the mistuned inter-stage matching between interpolator and PA, allowing the PA to be driven into compression.

**Figure 3.32** TX font-end with T/R- switch measured results for (a) $S_{21}$ phase response and RMS phase errors versus frequency across 32 phase settings, (b) $S_{21}$ phase DNL, and (c) $S_{21}$ phase INL at 24-28 GHz.

**Figure 3.33** TX font-end with T/R- switch measured results for (a) $S_{21}$ gain response and RMS gain errors versus frequency across 32 phase settings, (b) $S_{21}$ gain, and (c) gain deviation at 24-28 GHz.
Figure 3.34 Measured IQ (a) phase and (b) amplitude errors for the TX font-end with T/R- switch at 0° and 90° phase settings.

Figure 3.35 TX font-end with T/R- switch measured results for (a) noise figure versus frequency, (b) noise figure versus 32 phase states at 24-28 GHz, (c) oP₁dB versus the input power at 24 GHz and (d) oP₁dB versus frequency and versus 32 phase states.

3.4.3.2 Receiver Front-End with T/R Switch Characterization

Turning to the TX front-end, the gain and phase across 32 phase settings have been measured and are shown in Fig. 3.36(a). After calibration, the RMS phase error is less than 5.6° across 23.9-31.4 GHz. Figs. 3.36(b) and (c) show the differential nonlinearity (DNL) and integral nonlinearity (INL) of the phase responses, indicating errors less than ±1 LSB. The average peak gain is 6.3 dB at 25.6 GHz with a 43.4% 3-dB bandwidth of 20.4-31.5 GHz in Fig. 3.37(a). After calibration, the RMS gain error is
less than 1 dB across 16-34.6 GHz. Figs. 3.37(b) and (c) show the magnitude of \( S_{21} \) and gain deviation from the average gain over 32 phase settings at 24 to 28 GHz. The gain deviation is less than ±1 dB and can be improved by further adjustment of the pre-distortion. Furthermore, to evaluate the quadrature accuracy within the RX front-end, we compare the amplitude and phase difference between axis settings (0° and 90°). Figs. 3.38 (a) and (b) show measured phase error less than 3° from 25.6 to 30.5 GHz and amplitude error less than 0.8-dB from 16 to 30.5 GHz. The NF is 6.7-10.4 dB at 24-28 GHz across 32 phase settings, as shown in Figs. 3.39(a) and (b). The \( \text{IP}_{1\text{dB}} \) are -15.6 to -10.3 dBm at 24-28 GHz across 32 settings, as shown in Fig. 3.39(c).

Figure 3.36 RX front-end with T/R- switch measured results for (a) phase of frequency responses versus 32 phase states, (b) phase DNL, and (c) phase INL at 24-28 GHz.

3.4.4 Single-Element Transmitter Front-End Characterization

Due to the loss of the T/R switch, the noise figure of the receiver front-end and the output power of the transmitter front-end both are degraded. As a result, the transceiver front-ends in the Gen-2 array are implemented without the use of the T/R switch. For the TX front-end, the gain and phase for element one TX (closest to hybrid) across 32 phase settings have been measured. Fig. 3.40 (a) shows the measured phase of \( S_{21} \) of the single-channel receiver front-end across phase settings
Figure 3.37 RX front-end with T/R- switch measured results for (a) gain of frequency responses versus 32 phase states, (b) $S_{21}$ gain, and (c) gain deviation at 24-28 GHz.

Figure 3.38 Measured IQ (a) phase and (b) amplitude errors for the RX front-end with T/R- switch at 0° and 90° phase settings.

and the RMS phase error is $<5.6^\circ$ across 22.5-32.7 GHz. Fig. 3.40 (b) shows the differential nonlinearity (DNL) and integral nonlinearity (INL) of the phase responses, indicating errors less than $\pm0.8$ LSB. The average peak gain is 18.1 dB at 21 GHz and 10 dB at 28 GHz in Fig. 3.41 (a). This frequency shift is due to mistuning of the inter-stage matching at the vector interpolator’s output. After calibration, the RMS gain error is less than 1 dB across 15.9-34 GHz. Figs. 3.41(b) and (c) show the magnitude of $S_{21}$ and gain deviation from the average gain over 32 phase settings at 24 to 28 GHz. The gain deviation is less than $\pm1$ dB and can be improved by further biasing the adjustment
of the VGAs. To evaluate the quadrature accuracy within the front-end, we compare the amplitude and phase difference between axis settings (0° and 90°). Fig. 3.42 (a) and (b) show measured phase error less than 13.5° and amplitude error less than 1.4-dB from 16 to 40 GHz.

Due to the mistuning in the interpolator, the measured TX oP1dB and P_{SAT} is reduced to 5.5 to 10.6 dBm and 12.5 to 19.6 dBm at 20-28 GHz across 32 settings, as shown in Figs. 3.43 (a) and (b). The TX output power performance can be improved by fixing the mistuned inter-stage matching between interpolator and PA, allowing the PA to be driven into compression. Finally, the single-channel TX front-end occupies an area of 0.15 mm² excluding output GSG pads with 218 mW power consumption, excluding currents of biasing circuits.

### 3.4.5 Single-Element Receiver Front-End Characterization

The measured phase of the receiver front-end for element one (closest to hybrid) across 32 phase settings is shown in Fig. 3.44(a). After calibration, the RMS phase error is less than 5.6° across 19-34.4 GHz. Fig. 3.44(b) and (c) shows the differential nonlinearity (DNL) and integral nonlinearity (INL) of the phase responses, indicating errors less than ±0.5 LSB. The average peak gain is 11.5 dB at 25 GHz with a 21.6% 3-dB bandwidth of 22.8-28.2 GHz, as shown in Fig. 3.45(a). After calibration, the RMS
gain error is less than 1 dB across 13-36.1 GHz. Fig. 3.45(b) and (c) show the magnitude of $S_{21}$ and gain deviation from the average gain over 32 phase settings at 24 to 28 GHz. The gain deviation is less than ±1 dB and can be improved by further adjustment of the pre-distortion. Finally, to evaluate the quadrature accuracy within the RX front-end, we compare the amplitude and phase difference between axis settings (0° and 90°). Figs. 3.46 (a) and (b) show measured phase error less than 2.3° and amplitude error less than 0.8-dB from 16 to 33.6 GHz. The NF is 4.5-6.9 dB at 24-28 GHz across
Figure 3.42 Measured IQ (a) phase and (b) amplitude errors for the TX front-end at 0° and 90° phase settings.

Figure 3.43 Element-one TX front-end measured results for (a) oP_{1dB} versus the input power at 24 GHz, and (b) oP_{1dB} versus frequency and versus 32 phase states.

32 phase settings, as shown in Figs. 3.47(a) and (b). The iP_{1dB} and iIP_{3} are -25.4 to -18.4 dBm and -15.1 to -9.1 dBm, respectively at 24-28 GHz across 32 settings, as shown in Fig. 3.47(c) and (d). The single-channel RX front-end occupies an area of 0.2 mm² excluding input GSG pads with 121.5 mW power consumption, excluding currents of biasing circuits.
Figure 3.44 Element-one RX front-end measured results for (a) phase of frequency responses versus 32 phase states, (b) phase DNL, and (c) phase INL at 24-28 GHz.

Figure 3.45 Element-one RX front-end measured results for (a) gain of frequency responses versus 32 phase states, (b) $S_{21}$ gain, and (c) gain deviation at 24-28 GHz.

3.4.6 Four-Element Transceiver Array Characterization

A chip micrograph of the four-element array was shown in Fig. 3.12. The die size is 6.9 mm$^2$ including pads and the active array area is 2.9 mm$^2$. The chip consumes 1.08 (0.87) W in transmit mode and 0.68 (0.49) W in receive mode including (excluding) the currents of biasing circuits.
3.4.6.1 Transceiver Array Isolation Characterization

The complete four-element array has been characterized to reveal element-to-element isolation. Measurements demonstrate how the phase settings of adjacent elements affect the phase response of a given element, obtained by measuring the response of the first element at 0° phase setting when the settings of all other elements are changed across 32 states. The measured results in Figs. 3.48 (a) and (b) show that both RX front-ends achieve less than 1° of RMS phase-isolation error and less than
0.1 dB of RMS gain-isolation error for 16-40 GHz. The measured results in Fig. 3.49 (a) and (b) show that both TX front-ends achieve less than 1° of RMS phase-isolation error and less than 0.2 dB of RMS gain-isolation error for 16-40 GHz. The TRX array achieves excellent element-to-element isolation without the use of an isolation arm in the series-fed networks with low magnetic coupling, low substrate coupling, and high combiner isolation between each RX or TX channel.

Figure 3.48 Measured responses of RX element one at 0° setting while RX element two to four are swept across 32 settings for (a) measured phase and RMS phase errors and (a) measured gain and RMS gain errors of RX isolation.

3.4.6.2 Transceiver Array Mismatch Characterization

The gain and phase mismatch of the four-element transceiver array are measured at 0° phase setting. The phase and gain of three elements are referenced to the element that has the lowest gain at 28 GHz. The phased array shows less than 5° of RMS phase mismatch error and less than 0.6 dB of RMS gain mismatch error at 26.7-29.1 GHz for both RX and TX elements (see Figs. 3.50 and Fig. 3.51 (a) and (b)). These show that the phase and gain offsets due to the physical length of the series feed network can be calibrated out across the desired frequency range. Fig. 3.52 and Fig. 3.53 both show that the measured average results after phase/gain equalizations of the four RX and TX channels.
Figure 3.49 Measured responses of TX element one at 0° setting while RX element two to four are swept across 32 settings for (a) measured phase and RMS phase errors and (a) measured gain and RMS gain errors of TX isolation.

Figs. 3.52 (a) and (b) show that less than 5° of RMS phase errors and less than 0.8 dB of RMS gain errors for the four RX elements at 25 to 35 GHz. Figs. 3.53 (a) and (b) show that less than 5° of RMS phase errors and less than 0.5 dB of RMS gain errors for the four RX elements at 25 to 31 GHz.

Figure 3.50 Measured gain and phase responses of RX element one to three are referred to RX element four at 0° setting. (a) Measured phase and RMS phase and (b) measured gain and gain errors of RX mismatch.
Figure 3.51 Measured gain and phase responses of RX element one to three are referred to TX element four at 0° setting. (a) Measured phase and RMS phase and (b) measured gain and gain errors of TX mismatch.

Figure 3.52 Measured (a) RMS phase errors of RX 1-4 elements and (b) averaged gain and RMS gain error after phase/gain equalizations of the four RX elements.

3.5 Chapter Summary

This chapter has demonstrated a four-element phased-array transceiver in 130-nm SiGe BiCMOS technology at Ka band for potential 5G cellular network application. A series feed network is implemented and shared between both the TX and RX front-ends without the use of T/R switches to reduce array size. In addition, the phase/gain offsets between each TX and RX element can be
Figure 3.53 Measured (a) RMS phase errors of TX 1-4 elements and (b) averaged gain and RMS gain error after phase/gain equalizations of the four TX elements.

calibrated out within the desired frequency range. The measured results are summarized in Table 3.2. Compared to the other references, our distributed beamformer achieves the lowest front-end area and array area with comparable RF performances at Ka band; however, the DC power is higher than the passive switched-LC approaches.
Table 3.2 Comparison of RF Phased-Array TRX Front-Ends

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* SPDT included in the designs.

* DC power excluding biasing circuits and DACs.

** Estimated area excluding all pads.

− Estimated area excluding the series-fed t-lines and the 90° couplers.
4

HYBRID PHASED-ARRAY TRANSCEIVER WITH MIXER-BASED DUAL-VECTOR DISTRIBUTED BEAMFORMING AND BUILT-IN SELF-TEST NETWORK

4.1 Hybrid Phased-Array Transceiver Overview

This chapter presents a 28-GHz hybrid phased-array transceiver using mixer-based dual-vector distributed beamforming in 130-nm SiGe BiCMOS technology for 5G cellular application. The
hybrid transceiver array employs quadrature up- and down-conversion mixers to provide the global vector interpolation. The passive hybrid couplers are eliminated in the signal path to improve the bandwidth of the quadrature accuracy. A novel distributed active poly-phase filter is proposed to achieve wideband quadrature accuracy in the local-oscillation signal path. Furthermore, the hybrid transceiver array includes on-chip built-in self-test (BIST) networks to enable element-level and array-level self-test measurement. In measurement, each receive front-end achieves 8.6 gain at 29.8 GHz, a 24.5% 3-dB bandwidth (25.2-32.5 GHz), 5.7 to 7.5 dB noise figure, and -18.5 to -16.5 dBm input 1-dB compression point at 28 GHz. RMS gain and phase errors are less than 0.1 dB and 0.8° at 28 GHz respectively. Each transmit-front end achieves 18.1 dB at 29.9 GHz, a 24% 3-dB bandwidth (25.6 to 32.8 GHz), 13.8 to 14.8 dBm output 1-dB compression point, and 17.1 to 18.2 dBm output saturate power at 28 GHz. RMS gain and phase errors are less than 1 dB abd 5.6° at 14.1-35.4 GHz. The four-element transceiver array occupies 2.9 mm² area and consumes 1.22 W in transmit mode and 0.51 W in receive mode.

4.1.1 Hybrid Phased-Array Transceiver Architecture

In the previous section, we have demonstrated a dual-vector 28-GHz phased-array transceiver that employs scalar-only weighting functions within each front-end, dual- series-fed transmission-line (t-line) networks, and global quadrature combining to realize beamforming [Yeh17b]. Adopting series-fed networks saves significant area when compared to a parallel network, where the 1.38 mm² of the Gen-1 parallel network [Yeh17a] is reduced to 0.33 mm² for the Gen-2 series network [Yeh17b]. The Gen-2 four-element transceiver array occupies the same area as our Gen-1 four-element receive-only array, thereby doubling the integration density. However, although adopting series-fed networks provides broadband terminations for the passive hybrid couplers, it results in different quadrature phase and amplitude accuracies in the RX and TX modes at the desired frequencies. In the previous section, to evaluate the quadrature accuracy within the front-end, we compared the amplitude and phase difference between axis settings (0° and 90°). In the RX mode,
Figs. 3.46 (a) and (b) showed measured phase error less than 0.3° and amplitude error less than 0.2-dB at 28 GHz; however, in the TX mode, Figs. 3.42 (a) and (b) showed measured phase error of 12.4° and amplitude error of 1.2-dB at 28 GHz. The different quadrature accuracies are due to the different capacitive loading effects on the series-fed t-lines. In the RX mode, the small output parasitic capacitance of the DVGA with high output impedance can be absorbed into the series-fed t-line without decreasing the characteristic impedance $Z_0$ of the t-lines too much. When the array is switching to the TX mode, the larger input parasitic capacitance of the vector interpolator is loading the series-fed t-lines and decreasing the $Z_0$ of the t-lines. As a result, the passive hybrid couplers are terminated with a lower impedance than the desired differential 100 Ω in the TX mode so that the quadrature accuracy of the passive hybrid coupler is degraded. The poor quadrature accuracy directly impacts the phase and gain accuracies of the front-ends across different states so that additional calibration steps are required to minimize the phase and gain errors. Therefore, an improved broadband quadrature accuracy is desired. An alternative is to realize the quadrature function using a pair of quadrature down-conversion mixers (depicted in Fig. 2.3(d)) [Par05; Mon17].

A benefit of the mixer-based approach is that direct-conversion receivers already must generate accurate quadrature local-oscillator signals, and these can be leveraged to provide the quadrature solution for beamforming. A similar approach has been proposed in [Par05; Mon17]; however, the design is for the receiver phased array, not for the transceiver phased array. Also, that work does not explore or exploit multiple simultaneous beams using a single set of VGAs per element. Finally, the presence and implication of an image beam in $\sum X$ and $\sum Y$ were not investigated in that prior work. In this chapter, we explore the mixer-based approach to realize the broadband hybrid phased-array transceiver with wideband quadrature LO generation.

Fig. 4.1 (a) shows how the passive hybrid couplers are replaced with a pair of down-conversion quadrature mixers for the RX. The down-conversion mixers are placed on one side of the terminations of the dual- series-fed networks and the other side is terminated with resistors. In the RX mode, four-element receivers are turned on and the received signals are combined through the
dual-series-fed networks. The combined $\sum X$ and $\sum Y$ RF signals can be used to generate dual-beam patterns. The $\sum X$ and $\sum Y$ RF signals are down-converted into baseband (BB) signals by the down-conversion quadrature mixers and the BB signals are further combined at the inputs of the BB quadrature amplifiers. As a result, the final main beam of $\sum X - j\sum Y$ is formed at the BB domain. However, a drawback of the mixer-based approach is that the mixers are exposed to spatial signals located either within the desired beam location or the image location. Thus, the down-conversion quadrature mixers need to achieve high linearity due to the potential interference received by the image beam.

Fig. 4.1 (b) shows the array operating in the TX mode. A pair of up-conversion quadrature mixers is used to up-convert the baseband quadrature signals into RF quadrature signals. The same dual-series-fed networks used for the RX can also be shared with the TX front-ends due to their bidirectionality. As before, the up-conversion mixers can be placed on one side of the dual-series-fed networks and the other side is terminated with the down-conversion quadrature mixers. The up-converted quadrature RF signals are distributed within the series-fed networks and drive the input of each TX. Note that the RF quadrature accuracy relies on the BB and LO quadrature accuracy so that the different capacitance loading effect between RX and TX modes does not degrade the quadrature accuracy. My research efforts in this chapter focus on (1) improving the bandwidth of the transceiver to achieve multi-band operation and high data rate performance, (2) investigating mixer-based global interpolation for broadening the RF bandwidth, and (3) developing broadband solutions for quadrature LO generation. A new architecture for fully integrated transceiver phased arrays has been developed to achieve the above goals. I refer to this architecture as a *hybrid phased-array transceiver with mixer-based dual-vector distributed beamforming.*
Figure 4.1 Hybrid RF/BB-path architectures for the four-element TRX phased array using dual- and series-fed power combing/splitting networks in (a) the RX mode, and (b) the TX mode.

4.2 Mixer-Based Beamforming Theory

The mixer-based dual-vector phase-shifting method can be understood within a single-element receiver front-end, as shown in Fig. 4.2 (a). In the previous section, we showed that the X and Y signals at the DVGA’s outputs can be represented as \( \cos(\alpha) \cdot S_{in}(t) \) and \( \sin(\alpha) \cdot S_{in}(t) \), where \( S_{in}(t) \) is the received RF input signal, and \( \alpha \) is the phase shift per element. The received RF signal of \( S_{in}(t) \) can be represented as \( a \cdot \cos(2\pi f_{RF} t) \), where \( f_{RF} \) is the RF carrier frequency and \( a \) is the amplitude of the input signal and \( a \) is normalized to be 1. The quadrature LO signals, \( LO_I \) and \( LO_Q \), can be represented as \( \cos(2\pi f_{LO} t) \) and \( \sin(2\pi f_{LO} t) \), where \( f_{LO} \) is the LO carrier frequency. Thus, the BB quadrature signals, \( V_{BBI}(t) \) and \( V_{BBQ}(t) \), in the time domain can be represented as

\[
V_{BBI}(t) = \cos(2\pi f_{LO} t) \cos(2\pi f_{RF} t) \cos(\alpha) - \sin(2\pi f_{LO} t) \cos(2\pi f_{RF} t) \sin(\alpha) \quad (4.1)
\]

\[
V_{BBQ}(t) = \sin(2\pi f_{LO} t) \cos(2\pi f_{RF} t) \cos(\alpha) + \cos(2\pi f_{LO} t) \cos(2\pi f_{RF} t) \sin(\alpha) \quad (4.2)
\]

Equations (4.1) and (4.2) can be further simplified. Due to the frequency down-conversion, the high frequency component of \( f_{LO} + f_{RF} \) can be removed and the low frequency component of \( f_{BB} = f_{LO} \)
- $f_{RF}$ remains in the equations. The BB quadrature signals, $V_{BBI}(t)$ and $V_{BBQ}(t)$, in the time domain can be represented as

$$V_{BBI}(t) = \frac{1}{2} \left[ \cos(2\pi f_{BB} t) \cos(\alpha) - \sin(2\pi f_{BB} t) \sin(\alpha) \right] \quad (4.3)$$

$$V_{BBQ}(t) = \frac{1}{2} \left[ \sin(2\pi f_{BB} t) \cos(\alpha) + \cos(2\pi f_{BB} t) \sin(\alpha) \right] \quad (4.4)$$

Equations (4.3) and (4.4) can be further converted into a rectangular form in the phasor domain. The BB quadrature signals, $V_{BBI}$ and $V_{BBQ}$, in the phasor domain can be represented as

$$V_{BBI} = \frac{1}{2} [\cos(\alpha) - j\sin(\alpha)] \quad (4.5)$$

$$V_{BBQ} = \frac{j}{2} [\cos(\alpha) - j\sin(\alpha)] \quad (4.6)$$

which indicates that the each complex weight can be realized using the DVGA followed by a quadrature down-conversion [Par05]. The absolute normalized magnitude is constant and is given by $\sqrt{\cos(\alpha)^2 + \sin(\alpha)^2} = 1$. The phase shift $\alpha$ is given by the ratio of the IQ amplitudes, $\alpha = \tan^{-1}(\frac{\sin(\alpha)}{\cos(\alpha)})$.

Since the signs of X and Y signals can be switched at the DVGA's outputs, a full 360° phase tuning range can be achieved at the given frequency within a single-element receiver.

Next, we consider the beamforming math for the N-element phased-array receiver in Fig. 4.2 (b). The combining networks represented as $\sum$ can use either parallel combining networks without phase offset between each element ($\phi = 0^\circ$) or series-fed combining networks with phase offset between each element ($\phi \neq 0^\circ$). The combined $X_n$ and $Y_n$ RF signals can be represented as $\sum X_n$ and $\sum Y_n$. Phasors $X_n$ and $Y_n$ are the Cartesian expansions of the amplitude- and phase-shift for the $n^{th}$ element, depicting vector interpolation. The combined RF signals of $\sum X_n$ and $\sum Y_n$ are multiplied with the local-oscillation (LO) quadrature signals and further down-converted and combined at the BB quadrature signals. The beamforming BB quadrature signals, $V_{BBIn}$ and $V_{BBQn}$, in the phasor
Figure 4.2 Block diagrams of (a) a single-element dual-vector receiver and (b) N-element dual-vector phased-array receiver using mixer-based quadrature interpolation.

The domain can be represented as

\[ V_{BB\text{I}} = V_{LOI} \sum X_n - V_{LOQ} \sum Y_n \]  

(4.7)

\[ V_{BB\text{Q}} = V_{LOQ} \sum X_n + V_{LOI} \sum Y_n \]  

(4.8)

where \( V_{LOI} \) is the in-phase LO signal and \( V_{LOQ} \) is the quadrature LO signal. For derivations of the frequency translation, the combined RF signals of \( \sum X_n \) and \( \sum Y_n \) are converted into the time domain and they can be represented as

\[ V_{\sum X_n}(t) = \sum \left[ \cos(\alpha_n)\cos(2\pi f_R F t + \beta_n) \right] \]  

(4.9)

\[ V_{\sum Y_n}(t) = \sum \left[ \sin(\alpha_n)\cos(2\pi f_R F t + \beta_n) \right] \]  

(4.10)

where \( \beta_n \) is the time delay due to the antenna spacing (d) and \( \beta_n = (n-1)\kappa d \sin(\theta) \), \( \kappa = \frac{2\pi}{\lambda} \), \( \alpha_n \) is the amplitude shift per element, \( \theta \) is the arrival angle (zero corresponds to broadside), and \( \alpha_n \) is the phase shift per element. The beamforming BB quadrature signals, \( V_{BB\text{I}}(t) \) and \( V_{BB\text{Q}}(t) \), in
the time domain can be represented as

\[ V_{BBI_n}(t) = \cos(2\pi f_{LO} t)\sum X_n(t) - \sin(2\pi f_{LO} t)\sum Y_n(t) \]  
\[ V_{BBQ_n}(t) = \sin(2\pi f_{LO} t)\sum X_n(t) + \cos(2\pi f_{LO} t)\sum Y_n(t) \]  

Equations (4.11) and (4.12) can be further simplified. The high frequency component of \( f_{LO} + f_{RF} \) can be removed and the low frequency component of \( f_{BB} = f_{LO} - f_{RF} \) remains in the equations. The combined BB quadrature signals for the main beam, \( V_{BBI_n}(t) \) and \( V_{BBQ_n}(t) \), in the time domain can be represented as

\[ V_{BBI_n}(t) = \frac{1}{2} \left\{ \sum [\cos(\alpha_n)\cos(2\pi f_{BB} t + \beta_n)] - \sum [\sin(\alpha_n)\sin(2\pi f_{BB} t + \beta_n)] \right\} \]  
\[ V_{BBQ_n}(t) = \frac{1}{2} \left\{ \sum [\cos(\alpha_n)\sin(2\pi f_{BB} t + \beta_n)] + \sum [\sin(\alpha_n)\cos(2\pi f_{BB} t + \beta_n)] \right\} \]  

Equations (4.13) and (4.14) can be further converted into a rectangular form in the phasor domain. The BB quadrature signals, \( V_{BBI} \) and \( V_{BBQ} \), in the phasor domain can be represented as

\[ V_{BBI} = \frac{1}{2} \left\{ \sum X_{BB_n} - j \sum Y_{BB_n} \right\} \]  
\[ V_{BBQ} = \frac{1}{2} \left\{ j \sum X_{BB_n} + \sum Y_{BB_n} \right\} = \frac{j}{2} \left\{ \sum X_{BB_n} - j \sum Y_{BB_n} \right\} \]  

where \( \sum X_{BB_n} + \sum Y_{BB_n} \) is the main beam formed at the BB frequency. Note that the image beam of \( \sum X_{BB_n} + \sum Y_{BB_n} \) can be obtained by switching the sign of \( V_{LOQ}(t) = \sin(2\pi f_{LO} t) \). Thus, the combined BB quadrature signals for the image beam, \( V_{BBI_n} \) and \( V_{BBQ_n} \), in the phasor domain can be represented as

\[ V_{BBI_n} = \frac{1}{2} \left\{ \sum X_{BB_n} + j \sum Y_{BB_n} \right\} \]  
\[ V_{BBQ_n} = \frac{1}{2} \left\{ -j \sum X_{BB_n} + \sum Y_{BB_n} \right\} = -\frac{j}{2} \left\{ \sum X_{BB_n} + j \sum Y_{BB_n} \right\} \]
As a result, the main beam and the image beam can be selected at the \(BB_I\) and \(BB_Q\) outputs by simply switching the sign of the \(LO_Q\) without changing the settings of the front-ends. However, the BB quadrature accuracy and the dual-beam selection both depend on the matching and the quadrature accuracy at quadrature LO signals. Therefore, wideband quadrature LO generation is required in the RX-array system.

For the single-element transmitter, active quadrature up-conversion is implemented to eliminate the use of the passive and narrowband quadrature couplers. Fig. 4.3 (a) shows the block diagram of a single-element dual-vector transmitter using mixer-based quadrature generation. The BB quadrature signals, \(V_{BBI}(t)\) and \(V_{BBQ}(t)\), can be represented in the time domain as \(\cos(2\pi f_{BB}t)\) and \(\sin(2\pi f_{BB}t)\), where \(f_{BB}\) is the baseband frequency. The LO quadrature signals, \(V_{LOI}(t)\) and \(V_{LOQ}(t)\), can be represented in the time domain as \(\cos(2\pi f_{LO}t)\) and \(\sin(2\pi f_{LO}t)\), where \(f_{LO}\) is the LO carrier frequency. Up-converted RF quadrature signals, \(V_{RFI}(t)\) and \(V_{RFQ}(t)\), in the time domain are represented as

\[
V_{RFI}(t) = -\cos(2\pi f_{LO}t) \cos(2\pi f_{BB}t) + \sin(2\pi f_{LO}t) \sin(2\pi f_{BB}t) = -\cos(2\pi f_{RF}t)
\]

(4.19)
\[ V_{RFQ}(t) = \sin(2\pi f_{LO} t) \cos(2\pi f_{BB} t) + \cos(2\pi f_{LO} t) \sin(2\pi f_{BB} t) = \sin(2\pi f_{RF} t) \] (4.20)

where \( f_{RF} \) is the RF carrier frequency \( (f_{RF} = f_{LO} + f_{BB}) \) and amplitude are again normalized. With perfect quadrature accuracy and matching, the image signal at the frequency of \( f_{image} = f_{LO} - f_{BB} \) is completely cancelled. Ideally, the up-converted RF signals have a 90° difference with equal amplitude. The VGAs within the vector interpolator (VI) weight the amplitudes of I and Q signals according to \( \cos(\alpha) \) and \( \sin(\alpha) \) functions, respectively, where \( \alpha \) is the desired phase shift per element. The weighted I and Q signals are combined at the outputs of the VGAs to achieve the desired phase shift at the VI’s output. Interestingly, by switching the sign of either the \( V_{LOI}(t) \) or \( V_{LOQ}(t) \) signal, the single-sideband (SSB) signals can be selected.

The up-converted RF quadrature single-sideband signals, \( V_{RF_{LSSB}}(t) \) and \( V_{RF_{QSSB}}(t) \), in time domain can be represented as

\[ V_{RF_{LSSB}}(t) = -\cos(2\pi f_{LO} t) \cos(2\pi f_{BB} t) - \sin(2\pi f_{LO} t) \sin(2\pi f_{BB} t) = -\cos(w_{RF_{L}} t) \] (4.21)
\[ V_{RF_{QSSB}}(t) = -\sin(2\pi f_{LO} t) \cos(2\pi f_{BB} t) + \cos(2\pi f_{LO} t) \sin(2\pi f_{BB} t) = \sin(w_{RF_{L}} t) \] (4.22)

where \( f_{RF_{L}} \) is the RF sideband frequency \( (f_{RF_{L}} = f_{LO} - f_{BB}) \). As a result, the RF quadrature accuracy and the sideband selection both depend on the matching and the quadrature accuracy at quadrature LO and BB signals. Thus, the wideband quadrature LO generation is also required in the TX-array system. Fig. 4.3 (b) shows the block diagram of an N-element dual-vector transmitter using mixer-based quadrature generation. Once we understand the phase-shifting method for the single-element transmitter, the phase-shifted signals from each TX can be spatially combined in the free space to achieve the beamforming at the desired angle.
4.3 Mixer-Based Hybrid Transceiver Array Implementation

A new architecture for a fully integrated transceiver phased array is shown in Fig. 4.4. We refer to this architecture as a hybrid phased-array transceiver with mixer-based dual-vector distributed beam-forming. Fig. 4.4 shows the block diagram of the fully integrated hybrid phased-array transceiver composed of five main circuit blocks: (1) the four-element TRX scalar array with the dual-series-fed combiners/splitters, (2) the quadrature down-conversion mixers, (3) the quadrature up-conversion mixers, (4) the distributed quadrature LO, and (5) the on-chip built-in-self-test (BIST) network that consists of a single series-fed t-line, two SPDT switches, 20-dB couplers at the RX inputs and TX outputs, 15-dB couplers at the power detector inputs, two power detectors, and quadrature down-conversion mixers. Two variants have been redesigned. First, a revised version of the Gen-2 array is implemented, where the transceiver front-ends are modified and the BIST networks are included. This is referred to as a Gen-2p5 array. Second, the complete transceiver is redesigned, including mixers, referred to as a Gen-3p5 array. This hybrid transceiver array has been designed and fabricated in 130-nm SiGe BiCMOS 8HP from GlobalFoundries. The die photo of the hybrid array is shown in Fig. 4.5 with the die size of 4 x 3.3 mm².

A breakout of the Gen-2p5 transceiver array with a passive quadrature hybrid couplers is designed for the test evaluation of the TRX phase/gain performances. It is the updated version of the Gen-2 transceiver array. The Gen-2p5 transceiver array with the passive quadrature couplers is also implemented with the on-chip BIST network shown in Fig. 4.6. Four transmit front-ends and four receive front-ends are interdigitated, sharing dual-series feed networks and a global hybrid coupler. To simplify testing, the ∑X and ∑Y outputs of the dual-series-fed networks are combined and terminated using one differential hybrid coupler on one side. The other side of the series-fed network is terminated with differential 100Ω resistors. The BIST networks shown in Fig. 3.11 consists of a single series-fed t-line, 20-dB couplers at the RX inputs and TX outputs, 15-dB couplers at the power detector inputs, and a total of three power detectors. A chip micrograph of the TRX array with BIST
networks in Fig. 4.7 shows that the die size is 3.3 x 2.7 mm² including pads. The following is the description for each of the circuit blocks.

**Figure 4.4** Gen3p5 block diagram of realized four-element hybrid phased-array transceiver employing mixer-based series-fed distributed beamforming with on-chip BIST network.

### 4.3.1 Transceiver Front-End

The block diagram and the schematic of the transceiver front-end consisting of a receiver front-end (left), dual-series-fed t-lines (center), and a transmitter front-end (right), are shown in Fig. 4.8. Both
the receiver and transmitter front-ends share a single global quadrature combiner/splitter (top). The following section describes details for each circuit block in the front-end.

4.3.1.1 Transmitter Front-End

The transmitter front-end consists of a phase shifter and a power amplifier (PA), as shown in Fig. 4.8. A detailed schematic of the phase shifter is shown in Fig. 4.9 and it consists of in-phase (I) and quadrature-phase (Q) variable-gain amplifiers (VGAs) with current summing, and two binary-weighted current digital-to-analog converters (DAC). The design of the phase shifter is almost
Figure 4.6 Gen2p5 block diagram of realized four-element phased-array transceiver employing series-fed distributed beamforming with on-chip BIST network.

Figure 4.7 Die micrograph of four-element phased-array transceiver employing series-fed distributed beamforming with on-chip BIST network. Die size is 3.3 x 2.7 mm².
Figure 4.8 Block diagram of transceiver front-end used in both the Gen2p5 and Gen3p5 subarrays, with receiver front-end (left), series feed network (center), and transmitter front-end (right).

identical with the Gen-2 phase shifter in the TX front-end except for the modified DACs, the modified $G_m$ stages ($Q_{1-4}$), and the modified inter-stage transformer $M_2$. The amplitudes of I and Q signals are weighted by current-steering cross-coupled transistors $Q_{5-12}$ and the base terminals of $Q_{5-12}$ are controlled through the eight-bit $DAC_I$ and $DAC_Q$ and inverse-tanh cells ($Q_{15-18}$) with series resistors $R_{1-4}$. The series resistors $R_{1-4}$ are added to compensate for the reduced currents within the $DAC_I$ and $DAC_Q$. Furthermore, tail currents for the $G_m$ stages ($Q_{1-4}$) are removed to improve the voltage headroom. The $G_m$ transistors ($Q_{1-4}$) can be biased at the class AB mode to improve the vector interpolator’s output power performance. In addition, the inter-stage transformer $M_2$ was modified to resonate at the desired frequency.

The single-stage power amplifier (PA) employs a balanced cascode biased in Class-AB and sized to enable $>17$-dBm $o P_{1dB}$. A detailed schematic of the PA is shown in Fig. 4.10 (a). The design of the PA is almost identical with the Gen-2 PA in the TX front-end except for the modified current-mirror biasing circuits, the modified common-base stage ($Q_{3-4}$), and the modified output transformer $M_1$. The bottom devices of $Q_{1-2}$ are biased through a current mirror connecting to the center of the secondary inductance of $M_2$. The current-mirror biasing circuits are modified by adding the feedback
capacitor of 3.3 pF to improve their stability. Furthermore, the sizes of the common-base transistors, \( Q_{3-4} \), are decreased to reduced the parasitic capacitance. As a result, the output transformer \( M_1 \) has to be adjusted for the output desired impedance at 28 GHz. A load-pull simulation in Fig. 3.19 (b) shows that the optimum fundamental impedance for > 20-dBm \( oP_{1dB} \) is located on 35.5-\( \Omega \) circle, which is close to the calculated load-line value of 28.6 \( \Omega \). Fig. 3.19 (b) also indicates that > 21-dBm \( oP_{1dB} \) also can be achieved with the optimum \( Z_{opt} \) of 35.5+j35 \( \Omega \) at the fundamental frequency of 28 GHz. Finally, with the device size and operating current, the optimum impedance \( Z_{opt} \) can be set and provided through an output transformer \( M_1 \) with optimal output loading condition and single-ended output.

**Figure 4.9** Detailed schematics of the vector interpolator with DACs used in the Gen-2p5 and Gen-3p5 subarrays.

### 4.3.1.2 Receiver Front-End

The receiver (RX) front-end consists of a low-noise amplifier (LNA) and a dual-vector variable gain amplifier (DVGA) , as shown in Fig. 4.8 (a). The schematic of the Gen-3p5 LNA is shown in Fig.
4.11 and the design is identical with the Gen-2 LNA except for the modified length of the collector inductors that are implemented with the coplanar transmission lines, $T_{1-2}$, with 97.5 pH and peak Q of 13.5. Fig. 4.8 (b) shows the input noise and impedance matching of the LNA from 18 to 38 GHz. In the simulation, the LNA achieves the small-signal gain of 6.8 dB, NF of 3.8 dB, and $iP_{1dB}$ of 5.2 dBm all at 28 GHz. The LNA draws 12 mA from a 3.6-V supply (43.2 mW).

Compared to our prior work with the Gen-1 and Gen-2 DVGA designs, the DVGA used in the Gen-2p5 and Gen-3p5 arrays is modified, adding switchable degeneration inductance of $M_1$ and $M_2$ for high- and low- gain operations, and adding the linearizer of $Q_{3-6}$ for $IM_3$ cancellation [FC11; Bal12]. In addition, the large linearity variation of the Gen-2 DVGA across the phase states is due to the use of merging the predistortion cell with a $G_m$ cell into a single block with the cross-coupled common-emitter configuration. The detailed schematic of the Gen-3p5 DVGA with DACs is shown in Fig. 4.12. The DVGA $G_m$ ($Q_{1-2}$) is boosted by mutual coupling $M_{1-2}$ between the input series base inductors and emitter inductors [Zha14]. The $G_m$ cell is degenerated by the switchable inductors of the secondary inductance of transformers $M_{1-2}$. In high-gain mode, the control voltage of $B_0$...
is high so that the degeneration inductors are set to a low inductance value of 83.9 pH with $Q$ of 3.3 and $K$ of 0.2 at 28 GHz. However, in the low-gain mode, the control voltage of $B_0$ is low so that the degeneration inductors are set to high inductance value of 121 pH with $Q$ of 10.6 and $K$ of 0.19 at 28 GHz. Switched gain-mode operation provides the flexibility to optimize the constant gain performance across phase states during calibration. Predistortion is provided by $Q_{7-10}$ and controlled through an eight-bit digital-to-analog converter ($DAC_A$) and inverse-$tanh$ cell ($Q_{23-24}$) with series resistors $R_{1-2}$. A linearizer cell is added to improve $IP_3$ of the DVGA and it consists of the cascode cell $Q_{3-6}$ with a switched-capacitance tank for the $IM_3$ phase adjustment and controllable tail current for the $IM_3$ amplitude adjustment. Since the $G_m$ cell is linearized by the degeneration inductors, the non-linear components are mostly generated by the pre-distortion cell $Q_{7-10}$ so that the linearizer’s output is connected to the predistortion cell’s output with opposite phase connection for $IM_3$ cancellation. The pre-distorted signal is then split and weighted by current-steering cells $Q_{11-18}$.

Each RX front-end creates two in-phase signals, $X_n$ and $Y_n$, which are weighted according to $cos(\alpha_n)$ and $sin(\alpha_n)$, where $\alpha_n$ is the desired phase shift of the $n^{th}$ element. The current-steering cells are controlled through an eight-bit digital-to-analog converter ($DAC_{XY}$) and inverse-$tanh$ cell ($Q_{25-26}$) with series resistors $R_{3-4}$. To achieve four-quadrant operation, sign inversion is included within both the $X$ and $Y$ paths using cross-coupled transistors (shown in shaded region of Fig. 4.12). A common-base stage, $Q_{19-22}$, is used at the outputs to minimize the phase variation due to the finite output impedance of $Q_{11-18}$ when $X_n$ and $Y_n$ currents are steered. Outputs of the DVGA are combined through the dual ($X/Y$) series feed network, with the output parasitic capacitance absorbed into the line to avoid any need for resonant matching. Note that the 3.6-V supply voltage for the DVGAs is provided through these series feed networks and the global quadrature combiner/splitter.
4.3.2 Dual-Series-Fed Power Combiners/Splitters

For the mixer-based hybrid TRX array in Fig. 4.4, one side of the series combiner is terminated with the inputs of quadrature down-conversion mixers and the other side is terminated with the outputs of the up-conversion mixers. For coupler-based TRX array in Fig. 4.6, one side of the series combiner is terminated with differential 100-Ω resistors and the other side is terminated with the quadrature hybrid. Note that it is possible to terminate both ends of the series network with hybrid couplers and thereby increase the number of beams from two to four; however, this does lead to a narrower bandwidth for quadrature accuracy. In this prototype, we chose to realize only single-beam support to simplify testing.
4.3.3 Direct Up-Conversion Quadrature Mixers

Active quadrature up-conversion is implemented to eliminate the use of the passive and narrowband quadrature couplers. A similar approach was given in [Nat05] but a two-step up-conversion architecture was implemented to minimize local-oscillation (LO) pulling from the PAs. In this work, direct up-conversion quadrature mixers were designed for the transmitter with RF and LO frequencies of 28 GHz and BB frequencies of DC to 500 MHz. Fig. 4.13 shows the block diagram of the direct up-conversion quadrature mixers used in the Gen-3p5 subarrays, which consists of a baseband (BB)
The tasks of the direct up-conversion quadrature mixers are to up-convert the BB quadrature signals to RF quadrature signals and to achieve high RF output power, low LO feedthrough, and low image sidebands.

The schematic of the BB-to-RF up-conversion quadrature mixers is shown in Fig. 4.14. These mixers are Gilbert-type mixers. The $BB_1$ and $BB_Q$ inputs are fed into the linearized $G_M$ stages and convert the BB voltages into BB currents. The BB currents are split and fed into the commutator, switching transistors $Q_1$-$Q_{16}$. To obtain low self-mixing and low LO-to-RF feedthrough, the LO signals are isolated from the RF and BB signals within the commutator using symmetric layout and ground shielding [Fuj17]. The DC voltage at the base terminals of the commutators is biased through the center tap of the secondary inductor of the LO amplifier’s output transformer. The up-conversion RF currents are summed through the common-base (CB) stage ($Q_{17}$-$Q_{20}$) as current summers, which provides low input impedance looking into the emitter nodes. The combined RF signals drive the RF output amplifiers through the transformers $M_1$ and $M_2$. 

Figure 4.13 Block diagram of direct up-conversion quadrature mixers used in the Gen-3p5 subarrays.
The schematic of the baseband linearized $G_M$ is shown in Fig. 4.15 (a). The baseband differential signals are fed into the PMOS source followers ($M_1$ and $M_2$) and the followers drive the second stage of the common-emitter stage of $Q_1$ and $Q_2$ with degeneration resistors of 50 Ω. The $IM_3$ linearizer of $Q_3$ and $Q_4$ with degeneration resistors of 400 Ω is added to improve the linearity. The tail currents within the BB $G_M$ cell can be controlled through the current-mirror biasing. The schematic of the RF output amplifier is shown in Fig. 4.15 (b). The RF output amplifier is a modified version of the white follower in [Flo08] with the degeneration resistors of 56 Ω. This RF output amplifier needs to provide broadband matching for the terminations of the series-fed transmission lines. In the TX mode, $V_G$ is low and the switch is turned off. The output impedance of the RF output amplifier is matched to differential 100 Ω through degeneration resistors. In the RX mode, $V_G$ is high and the switch is turned on. The output impedance of the RF output amplifier is also matched to differential 100-Ω through degeneration resistors and the switch. In addition, the RF output amplifier needs to generate more than 5-dBm output power to drive the four-element TX front-ends into saturation, which is very challenging in this type of amplifier. The up-conversion quadrature mixers including the RF output amplifiers achieve simulated 5.5/5.5-dBm $P_{SAT}$, 4.8/4.8-dBm $oP_{1dB}$, 11.9/12-dBm $oIP_3$, 50.9/63.5-dBm $oIP_2$, -43.8/-42.7-dBm LO-to-RF leakage, and -26/-53.6-dBm sideband image with 272.4 mW DC power all at 28 GHz at the $RF_I/RF_Q$ outputs.

4.3.4 Direct Down-Conversion Quadrature Mixers

A pair of quadrature down-conversion mixers can be used to form a beam at BB/IF in the receive mode. The mixer-based interpolation can leverage existing (wideband) quadrature LO to achieve broadband performance [Par05]. However, a drawback is that the mixers are exposed to spatial signals located either within the desired beam location or the image location in the receive mode. As a result, the mixers need to achieve high linearity. Three different mixer topologies are considered to achieve good linearity performance. In this work, direct down-conversion quadrature mixers were designed for the receiver with RF and LO frequencies of 28 GHz and BB frequencies of DC to
Figure 4.14 Block diagram of direct up-conversion quadrature mixers used in the Gen-3p5 subarrays.

Figure 4.15 Schematics of (a) the linearized BB $G_M$ stage, and (b) the RF output amplifier.
500 MHz. Both passive polyphase mixers and active quadrature mixers are compared to see the
tradeoffs of the system performances.

4.3.4.1 Passive Polyphase Mixers

Figure 4.16 (a) Block diagram of direct down-conversion passive 4-phase mixers, and (b) a simplified
model of the 4-phase passive mixers with $C_{in} \sim \infty$, $\gamma_N=1$, and $Z_{SH} \sim \infty$.

Mixer-first receivers offer wide frequency tuning range and tunable input impedance through
the frequency translation properties provided by passive N-phase mixers. A 20-30 GHz mixer-
first receiver has been implemented in 45-nm SOI CMOS technology in [WF16] and the receiver
employs four-phase passive mixing with an input inductor to realize tunable impedance matching
up to 30 GHz and -13 to -9.3-dBm $iP_{1dB}$ with 41-mW DC power consumption. Such wideband,
low-power, and high-linearity performances for the N-phase passive mixers are attractive for our
mixer-based approach. Fig. 4.16 (a) shows the block diagram of the direct down-conversion passive
two-phase mixers which are designed in 120-nm SiGe BiCMOS technology. The passive mixers
provide frequency-translated input impedance due to bidirectional mixing. Specifically, the input
impedance for the single-port passive N-phase mixers can be expressed as [WF16; MA12]

\[ Z_{in} = \frac{1}{j \omega C_{in}} \| (R_{SW} + \gamma_N Z_{BB} \| Z_{SH}) \]  (4.23)

where \( R_{SW} \) is the switch resistance, \( Z_{BB} \) is the baseband termination impedance, \( \gamma_N \) represents the conversion loss of the mixer, \( Z_{SH} \) is the harmonic re-radiation impedance, and \( C_{in} \) is the parasitic capacitance of the mixer. For the first-order analysis, we can assume that there is no input parasitic capacitance \( C_{in} \), no conversion loss of the mixer (\( \gamma_N = \frac{1}{N} \)), and no harmonic re-radiation impedance (\( Z_{SH} \sim \infty \)). Thus, the input impedance \( Z_{in} \) for the single-port passive N-phase mixers can be simplified to be approximately equal to \( R_{SW} + \frac{Z_{BB}}{N} \). As a result, ideally, if there is no switch resistance \( R_{SW} \) for the switches, the input impedance of the mixers is \( \frac{Z_{BB}}{N} \), which is set by the baseband feedback resistors of the BB transimpedance amplifiers (TIA). Fig. 4.16 (b) shows the simplified model of the four-phase passive mixer. The switches are modeled as a switch resistance, \( R_{SW} \). The input ports are modeled as current sources of \( I_{\Sigma X} \) and \( I_{\Sigma Y} \), which are down-converted by the switches using 25% LO duty cycle pulses. The down-converted currents are fed into the baseband feedback resistance \( Z_{BB} \) and generate the baseband quadrature voltages, \( V_{BBI} \) and \( V_{BBQ} \). The BB quadrature signal phasor, \( V_{BBI} \) and \( V_{BBQ} \), can be represented as

\[ V_{BBI} = \frac{1}{2} I_{\Sigma X} - j I_{\Sigma Y} \times \frac{Z_{BB}}{N} \]  (4.24)

\[ V_{BBQ} = \frac{j}{2} I_{\Sigma X} - j I_{\Sigma Y} \times \frac{Z_{BB}}{N} \]  (4.25)

where \( \sum X_n - j \sum Y_n \) is the main beam formed at the BBI and BBQ outputs. Once the BB quadrature signals, \( V_{BBI} \) and \( V_{BBQ} \), are obtained, they can be used to determine the RF X and Y signals, which are up-converted from the BBI and BBQ outputs. They can be represented as

\[ V_{RFX} = I_{\Sigma X} R_{SW} + I_{\Sigma X} - j I_{\Sigma Y} \frac{Z_{BB}}{N} \]  (4.26)
\[ V_{RFY} = i \sum Y R_{SW} + i \sum X_n - j \sum Y_n Z_{BB} N \] (4.27)

where \( Z_{inX} \) is the input impedance into the \( \sum X \) port, and \( Z_{inY} \) is the input impedance into the \( \sum Y \) port. If \( R_{SW} \) is zero, the second beam of the \( \sum X \) and \( \sum Y \) signals is cancelled at the baseband and only the main beam is re-up-converted to the RF ports. Thus, the passive mixers should not suffer the linearity issue due to the interference received in the second image beam, as long as \( R_{SW} \) is small.

In 120-nm SiGe BiCMOS technology, the \( R_{SW} \) could be varied from 10 to 50 \( \Omega \). Larger switches result in smaller \( R_{SW} \) but increase the \( C_{in} \). Fig. 4.20 (a) shows the block diagram of the down-conversion passive four-phase mixers with baseband TIAs. The feedback resistors, \( R_{fb} \), can be varied from 1 to 10 k\( \Omega \) for adjustment of the conversion gain, the bandwidth, and \( S_{11} \). The baseband shunt capacitors, \( C_{BB} \), also can be varied from 100 to 300 fF for bandwidth adjustment. Fig. 4.20 (b) shows the schematic of the differential four-phase passive mixers that are driven by 25\% duty cycle LO. The input inductors, \( L_1 - L_2 \), provide input matching to resonate out the input parasitic capacitance from the switches. The switches \( M_1 - M_8 \) are 120-nm triple-well NFET transistors with a bulk voltage of 1.2 V and an N-well voltage of 2.5 V.

The beamforming simulation is done using PSS and PAC analyses in Cadence with ideal 25\% duty cycle LO. Fig. 4.18 (a) shows the \( \sum X \) and \( \sum Y \) beamforming versus arrival angle \( \theta \) in the RF domain as the width of the switches is varied from 16 to 30 \( \mu m \) to represent different \( R_{SW} \). The simulation shows that dual beams of \( \sum X \) and \( \sum Y \) patterns are formed at \( \theta = \pm 22.5^\circ \). The voltage difference is only 160 mV at \( \theta = -22.5^\circ \) as the switch width is increased from 16 to 30 \( \mu m \). The image beam still exists in the RF domain before the input of the mixers. Increasing the width of the switch might improve the image-beam cancellation but will worsen the input impedance tuning range. Also, it becomes more difficult for the 25\% duty cycle LO generation circuits to drive the larger switches. The image-beam cancellation could be possible if the mixer designs move to a more advanced CMOS processes.

The \( \sum X \cdot j \sum Y \) beamforming at the BB I and Q outputs is also shown in Fig. 4.18 (b). The
simulation shows the beam is formed at $\theta=22.5^\circ$ for the $\sum X-j\sum Y$ at the baseband I and Q outputs. However, in this design, the passive polyphase mixer is not chosen because the designs of the passive polyphase mixer are still challenging in 120-nm BiCMOS technology. In summary, the passive polyphase filter can achieve tunable $S_{11}$ and good linearity with low DC power itself but the linearity can be limited by the baseband amplifiers and the DC power could be consumed mostly by both LO and BB circuits.

Figure 4.17 (a) Block diagram of direct down-conversion passive four-phase mixers with baseband TIAs, and (b) the schematic of the differential passive four-phase mixers driven by 25 % duty cycle LO.

4.3.4.2 Active Quadrature Mixers

An alternative is to build linear active mixers for the system requirement. The $G_M$-free current-mode active mixer in [Fuj17] is attractive due to its high linearity of 1-dBm $iP_{1dB}$ at mm-wave frequencies; however, the $\sum X$ and $\sum X$ series-fed network needs to be terminated with a broadband 100-\(\Omega\)
**Figure 4.18** (a) Block diagram of direct down-conversion passive four-phase mixers with baseband TIAs, and (b) the schematic of the differential passive four-phase mixers driven by 25% duty cycle LO.

It is very challenging to provide such a broadband termination or input match (i.e. $S_{11}$) for this $G_M$-free current-mode active mixer. Another solution is to build a linearized-$G_M$ active mixer with negative resistor-feedback for better linearity and broadband $S_{11}$ [FC11]. This is the approach used in Gen-3p5 array. Fig. 4.19 shows that a block diagram of the direct down-conversion quadrature mixers used in the Gen-3p5 array. It consists of a RF $G_m$ stage, down-conversion quadrature mixers, BB current summers, and BB output emitter followers. The direct down-conversion quadrature mixers must down-convert the RF signals to BB quadrature signals with low self-mixing and low DC offset at BB outputs.

The schematic of the RF-to-BB down-conversion quadrature mixers is shown in Fig. 4.20 and these mixers are Gilbert-type mixers. The $RF_x$ and $RF_y$ inputs are fed into the linearized $G_M$ stages and convert the RF voltages into RF currents. The RF currents are split and fed into the commutator, switching transistors $Q_1$-$Q_{16}$. To obtain low self-mixing and low DC offset, the LO signals are isolated from the RF signals within the commutator using symmetric layout and ground shielding [Fuj17]. The DC voltage at the base terminals of the commutators is biased through the center tap of the
secondary inductor of the LO amplifier’s output transformer. The down-conversion BB currents are summed through the low-pass RC loads with 112-Ω resistor and 285-fF capacitor. The combined BB signals drive the BB emitter followers.

The schematic of the RF linearized $G_M$ is shown in Fig. 4.21 (a) [FC11]. The RF differential signals are fed into the common-emitter stage of $Q_1$ and $Q_2$ with degeneration resistors of 30 Ω. The cross-coupled feedback RC network with series 92-Ω resistor and 710-fF capacitor is to provide differential 100-Ω impedance for the terminations of the series-fed t-lines. The $IM_3$ linearizer of $Q_3$ and $Q_4$ with degeneration resistors of 60 Ω is added to improve the linearity. The switched capacitors attached to the emitters of the linearized cell is to adjust the phase of the $IM_3$ components. The tail currents within the RF $G_M$ cell can be controlled through the current-mirror biasing. The schematic of the BB emitter followers is shown in Fig. 4.21 (b). The low output impedance of the emitter follower is sufficient to drive the loads at the BB frequencies. The down-conversion quadrature mixers including the emitter followers achieve simulated -0.1/-0.5-dBm $IP_{1dB}$, 8.9/9.4-dBm $IP_3$, 46.9/47.3-dBm $IP_2$, -56.7/-58.9-dBm LO-to-BB leakage, 17.1/16.7-dB NF, and 5.7/7.8-mV DC offset with 226.9 mW output power all at 28 GHz at the $BB_I/BB_Q$ outputs.

**Figure 4.19** Block diagram of direct down-conversion active quadrature mixers used in the Gen-3p5 subarrays.
4.3.5 Distributed Quadrature LO Generation

In the previous section, both up-conversion and down-conversion mixers required the wideband quadrature LO generation for the sideband selection (TX) and the image beam selection (RX). Also, both the TX RF and the RX BB quadrature accuracies rely on the LO quadrature accuracy. In addition, both up-conversion and down-conversion mixers need to be driven with enough LO power for the mixing function. Thus, the quadrature LO signals need to achieve not only broadband quadrature accuracy but also large output LO power performance. The broadband quadrature accuracy can be achieved by using the multiple-stage poly-phase filter (PPF) or the static frequency divider. However, cascading multiple stages of the PPF result into the high loss in mm-wave frequencies [Kul13]. Adding multiple LO amplifiers can compensate for the loss but increases the DC power consumption.
In addition, even though the static frequency divider can achieve extreme wideband quadrature signals, the double input frequency for the LO signal is needed so that higher-frequency LO signals can be generated from the VCO, but high frequency VCO provides poor phase noise and tuning range in the system [Flo08]. Further, the high-frequency divider consumes considerable DC power especially in the mm-wave frequencies. As a result, a novel wideband quadrature LO solution needs to be developed for the need of the system.

Fig. 4.22 shows the block diagram of the novel distributed PPF (DPPF) to provide wideband quadrature LO signals for both up-conversion and down-conversion mixers. The DPPF consists of the input base-feed t-line, a unit cell of the active PPF, the current-mode passive PPF, the I and Q collector t-lines, and the LO amplifiers. The goal for the DPPF is to generate > 0-dBm output power for the I and Q outputs to drive the mixers from 25 to 35 GHz. Furthermore, the DPPF is able to provide the sign switch for the I and Q signals, which allows the side-band selection for the TX and the image beam selection for the RX. The broadband quadrature accuracy can be provided through
the active PPF cell embedding with current-mode passive PPF. The distributed-type amplification is chosen to achieve the broadband gain and output power performance [Poz90]. However, the traditional distribution amplifier performs broadband low-pass gain response and also the gain decreases as the frequency increases. In order to maintain the broadband gain and output power responses, the band-pass LO amplifier needs to be cascaded with the distributed amplification to cover the bandwidth from 20 to 40 GHz.

Fig. 4.23(a) shows the schematic of the LO amplifier. The cascode topology with transistors $Q_1 - Q_4$ is chosen for the better isolation and higher gain performance. A feedback resistor of 125 $\Omega$ with a series capacitor of 710 fF provides differential 100-$\Omega$ input matching for the terminations of the IQ collector t-lines. The center tap of the secondary inductance of the transformer provides the bias voltage $V_B$ for the common-mode voltage of the mixers’ LO ports. The distributed PPF consists of multiple stages of the unit cells of the active PPF. The schematic of the unit cell of the active PPF is shown in Fig. 4.23(b). The unit cell of the active PPF is composed of the $G_m$ cell of $Q_1-Q_2$, a current-mode passive PPF, and current-split cross-coupled transistors $Q_3-Q_{10}$ for the I and Q paths. The base terminals of the cross-coupled transistors $Q_3-Q_{10}$ can be sign-switched by the control voltages of $V_{CI}$ and $V_{CQ}$. The supply voltage of 3.3 V is provided through the collector t-lines from the center tap of the primary inductor of the transformer $M_1$ in Fig. 4.23(a).

The passive PPF is driven in the current domain instead of the voltage domain [CL10]. Two different modified topologies of the passive PPF are designed to achieve wideband quadrature accuracy. Fig. 4.23(c) shows the schematic of the tunable passive PPF with the tunable capacitance ($C_{Diode}$) implemented with the reverse-biased havar diodes, which achieves a capacitance range of 70-160 fF at 28 GHz. Through tuning of the capacitance, the quadrature offset at a given frequency can be adjusted. The diodes are connected with two series AC-coupling capacitance ($C_{big}$) of 1 pF to block the DC voltages. The cathodes of the diodes are connected to a tuning voltage through an RF choke ($R_{big}$) of 9 k$\Omega$, whereas the anode is grounded also through an RF choke ($R_{big}$). The resistors ($R_1$) of 161 $\Omega$ provide the DC current path to the $G_m$ stage of $Q_{1-2}$ and the cross-coupled
transistors of $Q_{3-10}$. The interconnections modeled with $T_{1-4}$ at the quadrature outputs results into several crosses with different length, which leads to different parasitic capacitance and inductance. Carefully parasitic extraction with EM simulation needs to be considered to achieve good quadrature accuracy over frequencies. The in-phase and quadrature-phase currents are split and flow into the cross-coupled transistors of $Q_{3-10}$.

Fig. 4.23(d) shows the schematic of the second topology of the passive PPF. It is basically two type-$a$ PPFs in [Kul13] merged into a single parallel structure to achieve constant quadrature phase across frequency. The resistors ($R_1$) of 5 $\Omega$ provide the DC current path to the $G_m$ stage of $Q_{1-2}$ and the cross-coupled transistors of $Q_{3-10}$. The capacitors of $C_1$ and $C_2$ are chosen differently as 92.4 fF and 123.8 fF to compensate for the parasitic capacitance and inductance in the layout. This new new design is more compact than the tunable structure even with two passive PPFs. Finally, the DPPF including the second passive PPF achieves simulated 1.8-dBm $oP_{1dB}$ at 28 GHz at the $BB_I/BB_Q$ outputs with 192-mW DC power. The quadrature phase and amplitude errors are less than 5° from 20 to 30 GHz and 1.6 dB from 18 to 37 GHz.

Figure 4.22 Schematics of (a) the LO amplifier, (b) the active PPF, (c) the tunable passive PPF, and (d) the current-mode passive PPF
Figure 4.23 Schematics of (a) the active PPF, (b) the tunable passive PPF, and (c) the modified passive PPF

4.3.6 On-chip Built-In Self-Test Circuit Network

The silicon based phased arrays have been demonstrated in transmit and receive modes for millimeter-wave applications in previous sections. One of the key bottlenecks of RFIC-based phased arrays is the S-parameter testing of so many different channels on a single chip. In fact, the millimeter-wave phased-array measurement is expensive and time consuming. Thus, the use of on-chip built-in self-test (BIST) would not only lower the testing cost, but also allow excitation of all elements at once for capturing the on-chip array factor with high accuracy. In addition, the BIST circuit network...
should not occupy a large area of the chip and should not degrade the RF performance of the chip when it is not used. In this work, the hybrid phased-array transceiver contains the on-chip BIST circuit network to enable both the traditional BIST approach using quadrature down-conversion mixers [Ina12; Kim13; Ina13] and the new BIST approach using the code-modulated embedded test (COMET) [Gre16].

4.3.6.1 Built-In Self-Test Circuit Building Blocks

Fig. 4.4 shows the block diagram of the fully integrated hybrid phased-array transceiver containing the on-chip built-in-self-test (BIST) network. The BIST circuit building blocks consist of a single-ended series-fed t-line, two SPDT switches, two power detectors (PD), 20-dB couplers at the RX inputs and TX outputs, 15-dB couplers at the power detector inputs, and quadrature down-conversion mixers. Fig. 4.24 (a) shows the cross section of the BIST t-line, which is built using a CPW configuration using the LY layer for the BIST signal surrounded by the ground plane (MQ-LY) and the supply plane (MA-E1). The BIST transmission line needs to feed multiple TRX channels with the capacitive 20-dB coupler shown in 4.24 (b). The geometry of the BIST t-line is chosen to achieve 54.9-Ω Z₀, 0.4-dB loss at 28 GHz and for a channel-to-channel spacing length of 410 μm. The BIST t-line’s Z₀ is chosen as higher than 50 Ω to compensate the additional capacitive loading from the couplers, which lowers the overall Z₀ of the BIST t-line.

The capacitive 20-dB coupler in Fig. 4.24 (b) is implemented by moving up the BIST t-line to the E1 layer and enlarging the coupling capacitance underneath the RF t-line on MA layer. The overlap area of 37.5 × 38μm² determines the coupling value of -24.4 dB (all ports matched) and -18.4 dB (GSG port open circuited) at 28 GHz. The higher coupling for the open-circuited GSG port is due to the reflected signal. The BIST coupler has very little effect on the S-parameters of the RF CPW t-line with the loss of < 0.1 dB. Thus, the RX’s NF and TX’s output power should be only degraded less than 0.1 dB due to the loss of the coupler. The second capacitive 15-dB coupler for the power detector is shown in Fig. 4.24 (c). The coupling value is dependent on the overlap area between
the BIST t-line on the LY layer and the coupling layer on the LY and MQ layers. The overlap area of $12.5 \times 160\mu m^2$ determines the coupling value of -14.1 dB (all ports matched) at 28 GHz. The power detector is placed at the bottom-center of the coupler and the detector input is attached directly to the coupler port on the MQ layer.

The SPDT switches are used to switch the BIST signal either coupled from the external LO signal or injected from the external RF BIST signal through wafer probing. The schematic of the SPDT switch is shown in Fig. 4.25 (a). The design of the SPDT switch is based on the transformer-based concept using the transformers, $M_1$-$M_2$, and reduced $\lambda/8$ t-lines, $T_2$-$T_3$. The series inductors, $L_1$ and $L_2$, are to resonate out the parasitic capacitance of the off-switches, $Q_1$-$Q_4$. When the BIST signal is coupled from the 20-dB coupler at the LO inputs, the control voltage of $V_G$ is high and $V_{Gb}$ is low. The coupled BIST signal passes through the switch from port 3 to port 1 and then feeds multiple channels in the array. The leakage signal from port 3 to port 2 would not be reflected due to the termination resistor, $R_{Term}$ of 59 $\Omega$. When the BIST signal is injected from external RF signal through the wafer probing, the control voltage of $V_G$ is low and $V_{Gb}$ is high. The injected BIST signal is passing through the switch from port 2 to port 1 and then feeds multiple channels in the array. The leakage signal from port 2 to port 3 is shorted to ground through the on switch, $Q_4$, so that the injected signal would not couple into the LO circuits. The SPDT switch achieves 2.4-dB loss and > 20-dB isolation with all three ports matched to 50 $\Omega$ at 28 GHz.

Another key building circuit block is the power detector shown in Fig. 4.25 (b). The power detector is connected to the output coupled port of the 15-dB coupler. For this circuit, a common-emitter topology, $Q_1$, biased in a non-linear region of operation to perform the squaring function was chosen with a low-pass RC output filter to remove the higher frequency components. Additionally, the 1$^{st}$ and 2$^{nd}$ notch filters are included to further attenuate the fundamental (28 GHz) and the second harmonic (56 GHz) frequencies from the outputs of the power detector. The replica circuit of the transistor $Q_2$ with the low-pass RC network is added to provide the reference voltage. It allows the desired output DC voltage to subtract the DC component from the reference voltage.
4.3.6.2 Built-In Self-Test RX-Mode Operation in Mixer-Based Transceiver Array

Fig. 4.26 presents the BIST RX-mode operation with an integrated quadrature down-conversion mixers. In this case and during BIST RX-mode operation, the LO signal is given externally at the port 1 (P1) into the DPFF circuit, which generates the quadrature LO signals to drive the I/Q down-converter. The input LO signal also propagates through the base t-line of the DPFF and is coupled
Figure 4.25 Schematics of (d) SPDT switch, and (e) the power detector with 1st and 2nd output notch filters.

into the BIST t-line through the LO 20-dB coupler at the termination. The SPDT switch on the top-right corner is switched to the port of the LO 20-dB coupler so that the coupled BIST signal can be fed into the 20-dB couplers at RX’s inputs. The coupled BIST signal is color coded in red to show the propagation in the direction of P1 (LO for RX)-P2 (RX1)-P3 (RX3)-P4 (RX4)-P5 (RX2)-P6 (BIST RF IN 2RF Term). The simulated insertion loss/phase is 49.1 dB/-207.3 % from the P1 to P2, 51.2 dB/-305.1 % from the P1 to P3, 54.3 dB/-532.5 % from the P1 to P4, 55.2 dB/-632.3 % from the P1 to P5 at 28 GHz. The BIST network not only measures phase/gain responses of the individual element, but measures the on-chip array factor through exciting four elements at once; however, the four-element receivers need to be equalized to calibrate out the phase and amplitude offsets due to the series-fed t-lines. For the one-element RX BIST measurement, the coupled BIST signal is amplified and phase-shifted through individual receive front-end and down-converted into the baseband (BB) I/Q outputs through the I/Q down-converter. Note that the BIST systems are based on the homodyne approach, and therefore the down-converter I/Q outputs are mostly at DC. The I and Q DC data are then processed externally to obtain the normalized amplitude and phase response using the standard formulas $A = \sqrt{T^2 + Q^2}$ and $Phase = \tan^{-1}(\frac{Q}{I})$ [Ina12; Kim13]. For the four-element RX BIST measurement, the four-element receivers need to be equalized for the phase and gain responses first and then the receiver output signals are combined through the $\sum X$.
and $\sum X$ series-fed combiners. The combined $\sum X$ and $\sum X$ signals are down-converted into the baseband (BB) I/Q outputs through the I/Q down-converter.

In fact, the BIST signal can also be coupled and propagate in the opposite direction of P1(LO for RX)-P5(RX2)-P4(RX4)-P3(RX3)-P2(RX1)-P7(BIST $RF_{IN1}RTerm$) through different states of the SPDT switches. The simulated insertion loss/phase is 52.2 dB/-127.6 % from the P1 to P5, 52.3 dB/-244.3 % from the P1 to P4, 57.2 dB/-468.2 % from the P1 to P3, 55.5 dB/-602.5 % from the P1 to P2 at 28 GHz. In addition, the BIST signal can be injected externally from either P7 ($RF_{IN1}RTerm$) or P6 ($RF_{IN2}RTerm$) through wafer probing, if the power-sweeping BIST measurement needs to be conducted.

![Diagram of BIST operation in the RX mode for the Gen-3p5 hybrid transceiver array.](image)
4.3.6.3 Built-In Self-Test TX-Mode Operation in Mixer-Based Transceiver Array

Fig. 4.27 presents the BIST TX-mode operation with two integrated power detectors. The BIST measurement in the TX mode is based on the code-modulated embedded test (COMET) technique proposed in [Gre16]. In this case and during BIST TX-mode operation, the LO signal is given externally at the port 1 (P1) into the DPFF circuit, which generates the quadrature LO signals to drive the I/Q up-converter. The I/Q BB signals are given externally and are up-converted to I/Q RF signals by the I/Q up-converter. The I/Q RF signals are fed into the series-fed t-lines and drive the inputs of the transmitter front-ends. The RF signal within individual element is code-modulated through the phase shifter and gets amplified by the PA. The output signal from each PA's output is coupled into the BIST t-line through the 20-dB coupler. Ideally, the coupled RF signals should be split equally into two directions on the BIST t-line. The combined signals are detected at the inputs of two power detectors where one is placed next to the RX1 input and another is placed next to the TX1 output. If the combined signals are added in phase, the maximum DC output voltage is obtained from the power detector's outputs. If the combined signals are cancelled completely, the minimum DC output voltage is obtained from the termination resistors at P6 and P7 with minimum reflection through the SPDT switches. The high isolation of the SPDT switches prevents the leakage signals into the LO inputs of the DPFF. For the coupled RF signals propagating to the port 6 (P6), the simulated insertion loss/phase is 32.1 dB/71.7 % from the P1 to P6, 34.5 dB/-24.8 % from the P2 to P6, 36.8 dB/-257.1 % from the P3 to P6, 39 dB/-355.1 % from the P4 to P6 at 28 GHz. For the coupled RF signals propagating to the port 7 (P7), the simulated insertion loss/phase is 33 dB/25.5 % from the P4 to P7, 34.2 dB/-81.7 % from the P3 to P7, 37.7 dB/-309.6 % from the P2 to P7, 39 dB/-409.1 % from the P1 to P7 at 28 GHz. The BIST network can measure the on-chip array factor by exciting four elements at once; however, the four-element transmitters need to be equalized to calibrate out the phase and amplitude offsets due to the series-fed t-lines. The coupled RF signals on the BIST t-line are combined through the
series-fed BIST t-line and are detected by the two power detectors, which provide squaring function of the coded-modulated RF signals. Since the coupled RF signals are coded by the phase shifters, the DC output voltages from the power detectors need to be decoded through the post-data processing [Gre16].

Figure 4.27 BIST operation In the TX mode for the Gen-3p5 hybrid transceiver array.

4.3.6.4 Built-In Self-Test Operation in Coupler-Based Transceiver Array

Fig. 4.28 presents the BIST operation with three integrated power detectors for the Gen-2p5 coupled-based TRX array. The BIST measurement in both the TX and RX modes is based on the code-modulated embedded test (COMET) technique proposed in [Gre16]. During BIST RX-mode operation in Fig. 4.28 (a), the BIST signal is given externally either at the port 1 (P1) or at the port 6 through
wafer probing. The BIST signal propagating on the BIST t-line is coupled into the RX inputs through the 20-dB couplers. The coupled RF signal within an individual RX element is code-modulated through the DVGA and the coded output signals from each DVGA's output are combined through \( \sum X \) and \( \sum Y \) series-fed combiners and the global quadrature combiner. The BIST network can measure the on-chip array factor by exciting four elements at once; however, the four-element receivers need to be equalized to calibrate out the phase and amplitude offsets due to the series-fed t-lines. The combined signal is detected by a power detector placed at the output port 7 of the global quadrature combiner. Since the combined RF signals are coded by the DVGAs, the DC output voltages from the power detector need to be decoded through the post-data processing \([\text{Gre16}]\).

During BIST TX-mode operation in Fig. 4.28 (b), the RF signal is given at the port 7 of the input of the quadrature splitter and fed to the inputs of each TX element through the series-fed t-lines. The RF signal within the individual TX element is code-modulated through the phase shifter and the coded signal is amplified by the PA. The PA output signal is coupled into the BIST t-line through the 20-dB coupler. Ideally, the coupled RF signals should be split equally into two directions on the BIST t-line. The combined signals are detected at the inputs of two power detectors where one is placed next to the RX1 input and another is placed next to the TX1 output. If the combined signals are added in phase, the maximum DC output voltage is obtained from the power detector's outputs. If the combined signals are cancelled completely, the minimum DC output voltage is obtained from the PD's outputs. The coupled RF signals are further propagated to the termination resistors at P1 and P7 with minimum reflection. The BIST network can measure the on-chip array factor by exciting four elements at once; however, the four-element transmitters need to be equalized to calibrate out the phase and amplitude offsets due to the series-fed t-lines. The coupled RF signals on the BIST t-line are combined through the series-fed BIST t-line and are detected by the two power detectors, which provide the squaring function of the coded-modulated RF signals. Since the combined RF signals are coded by the DVGAs, the DC output voltages from the power detector need to be decoded through the post-data processing \([\text{Gre16}]\).
Figure 4.28 BIST operations in (a) the RX mode and (b) the TX mode for the Gen-2p5 transceiver array.

4.4 Measurement Results

4.4.1 Power Amplifier Characterization

The 28-GHz PA is designed and fabricated in GlobalFoundries 8HP 0.12-µm SiGe BiCMOS technology. A stand-alone PA breakout consisting of the PA core and input and output baluns was measured. The die photo of the PA with input and output baluns is shown in Fig. 4.29. For small-signal characterization, Fig. 4.30(a) shows the measured scattering parameters with > 10-dB $S_{21}$ over wide frequencies with the peak gain of 25.5 dB at 10.3 GHz and the gain of 12.2 dB at 28 GHz. Fig. 4.30(b) shows the measured $S_{21}$ versus input power at 28 GHz with good linear phase and gain responses.

For large-signal characterization, wafer-level measurements in Fig. 4.31 show the PA gain, output power, and power-added efficiency (PAE) across input power and frequency. The PA achieves 13-dB gain, 16.5-dBm $O_{1dB}$, and 22.4% peak PAE at 28 GHz. the PA achieves +24.2-dBm output-referred third-order intercept point (oIP$_3$) at 28 GHz with 100-MHz offset frequency. Finally, the PA consumes 238.1 mW from a 3.3-V supply. The measured results of Gen-2 and Gen-2p5 PAs are summarized in Table 4.1.
Figure 4.29 Die photographs of the power amplifiers used in the Gen2p5 and Gen-3p5 subarrays.

Figure 4.30 PA measured S-parameter results (a) versus frequency and (b) versus input power at 28 GHz.

4.4.2 Distributed Quadrature LO Characterization

4.4.2.1 Distributed Tunable Poly-Phase Filter

The 28-GHz distributed tunable PPF (DTPPF) is designed and fabricated in GlobalFoundries 8HP 0.12-µm SiGe BiCMOS technology. A chip micrograph of the DTPPF is shown in Fig. 4.32. The die size is 2.4 mm² including pads. All measurements were performed through wafer probing. S-parameter and gain/phase response measurements were taken using a two-port Agilent E8361C 67-GHz network analyzer. Fig. 4.33 (a) show the measured S-parameters for the I and Q outputs
when $V_{\text{tune}}$ is 0 V. The DPPF achieves 7.1- and 6.8-dB gain of $S_{21}$ and $< -10$-dB $S_{11}$ from 24.7 to 33.6 GHz and $< -10$-dB $S_{22}$ from 28 to 40 GHz for both I and Q paths. The measured $S_{11}$, $S_{21}$, and $S_{22}$ also has good agreement with I and Q paths.

Fig. 4.33 (b) shows the measured gain of $S_{21}$ for the I and Q outputs when $V_{\text{tune}}$ varies from 0 to 3.6 V. The DPPF achieves 0.31- to 0.36-dB IQ gain difference at 28 GHz across $V_{\text{tune}}$ of 0 to 3.6 V. The DTPPF achieves the IQ phase difference of 91.5° with 0-V $V_{\text{tune}}$ at 28 GHz. However, the phase tuning range is only 6.4° at 28 GHz across $V_{\text{tune}}$ of 0 to 3.6 V. The phase tuning range across frequencies with the desired 90° quadrature phase difference is from 24.7-27.4 GHz. The narrow phase tuning range is due to the large fixed parasitic capacitance in the layout. Swept-power measurements are taken with an Agilent E8257D signal generator providing the input and an Agilent N1913A power meter and an Agilent N8488A power sensor for the output. The DTPPF generates the output saturated power of 3 and 2.2 dBm at 28 GHz for the I and Q outputs as shown in Fig. 4.34 (a).

The 3-dB bandwidth of the output saturation power is from 21.9 to 32.8 GHz for the I output and from 21.2 to 35.9 GHz for the Q output in Fig. 4.34 (b). Finally, the DTPPF consumes 445 mW with
Table 4.1 Comparison of Gen-2 and Gen2p5 PA

<table>
<thead>
<tr>
<th>Reference</th>
<th>Gen-2 PA</th>
<th>Gen-2p5 PA</th>
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<tr>
<td>DC Supply (V)</td>
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<td>3.3</td>
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<tr>
<td>DC power (mW)</td>
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<td>238.1</td>
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<tr>
<td>Freq. (GHz)</td>
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<td>24, 26, 28</td>
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<tr>
<td>S₁₁ (dB)</td>
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<td>-10.4, -9.7, -9.1</td>
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<td>S₁₂ (dB)</td>
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<td>S₂₁ (dB)</td>
<td>21.6, 22, 21.2</td>
<td>16.8, 14.9, 13</td>
</tr>
<tr>
<td>S₂₂ (dB)</td>
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<td>-2, -2.1, -2.5</td>
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<tr>
<td>oP₁₁dB (dBm)</td>
<td>14.2, 14.4, 14.8</td>
<td>17.4, 17.4, 16.5</td>
</tr>
<tr>
<td>Pₛ₅₅ (dBm)</td>
<td>20.8, 20.5, 19.3</td>
<td>19.8, 20.2, 18.9</td>
</tr>
<tr>
<td>Peak PAE (%)</td>
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<td>33.2, 29.8, 22.4</td>
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<tr>
<td>PAE at oP₁₁dB (%)</td>
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<td>21.2, 18.5, 16.7</td>
</tr>
<tr>
<td>PAE at 7-dB backoff (%)</td>
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<td>5.5, 4.9, 5</td>
</tr>
<tr>
<td>oI₃ at 10 MHz (dBm)</td>
<td>30.3, 30.8, 34.1</td>
<td>25.4, 25, 24.2</td>
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<tr>
<td>oI₃ at 100 MHz (dBm)</td>
<td>33, 31.8, 36.2</td>
<td>26.5, 25.5, 24.9</td>
</tr>
</tbody>
</table>

3.6-V supply voltage.

4.4.2.2 Distributed Poly-Phase Filter

The second breakout of the 28-GHz modified distributed PPF (DPPF) is designed and fabricated in GlobalFoundries 8HP 0.12-µm SiGe BiCMOS technology. A chip micrograph of the DPPF is shown in Fig. 4.35. The die size is 2.07 mm² including pads. Fig. 4.36 (a) show the measured S-parameters for the I and Q outputs when V₉C is 3.6 V and V₉BG is 1.2 V. The DPPF achieves 1.4- and 1.6-dB gain of S₂₁ and < -10-dB S₁₁ from 27.6 to 35.5 GHz and < -10-dB S₂₂ from 28.4 to 40 GHz for both I and Q paths. The measured S₁₁, S₂₁, and S₂₂ also has good agreement with I and Q paths.
Figure 4.32 Die photographs of the distributed quadrature LO generation using the tunable PPF.

Figure 4.33 Measured results of the distributed PPF of (a) the S-parameters of for the I and Q outputs, and (b) the I and Q amplitude and phase difference, when $V_{\text{tune}}$ varies from 0 to 3.6V.

Fig. 4.36 (b) shows the measured gain of $S_{21}$ for the I and Q outputs when $V_{CC}$ is 3.6 V and $V_{BG}$ is 1.2 V. The DPPF achieves less than 1-dB IQ gain difference from 24.6 to 30.4 GHz. The DPPF achieves the IQ phase difference of 73° at 28 GHz. However, both the measured IQ phase and gain differences have good agreement with the simulated results. The shifted IQ phase difference at 28 GHz is due to different length of interconnection transmission lines in I and Q paths in the breakout.
Figure 4.34 Measured results of the distributed tunable PPF of (a) the gain and output power responses versus the input power at 28 GHz for both I and Q outputs, and (b) the output saturation power responses versus the frequency for both I and Q outputs.

chip, which is different layout from the DPFF in the array chip. The DPPF generates the output saturated power of 5.1 and 5.4 dBm at 28 GHz for the I and Q outputs as shown in Fig. 4.37 (a). The 3-dB bandwidth of the output saturation power is from 21.2 to 31.7 GHz for the I output and from 22.9 to 33.8 GHz for the Q output as shown in Fig. 4.37 (b). Finally, the DTPPF consumes 218 mW with 3.6-V supply voltage.

Figure 4.35 Die photographs of the distributed quadrature LO generation using the modified PPF.
Figure 4.36 Measured results of the distributed modified PPF of (a) the S-parameters of for the $I$ and $Q$ outputs, and (b) the $I$ and $Q$ amplitude and phase difference.

Figure 4.37 Measured results of the distributed tunable PPF of (a) the gain and output power responses versus the input power at 28 GHz for both $I$ and $Q$ outputs, and (b) the output saturation power responses versus the frequency for both $I$ and $Q$ outputs.
4.4.3 Four-Element Transceiver Array with Lange Couplers Characterization

A breakout of the Gen-2p5 transceiver array with a passive quadrature hybrid couplers is designed for the test evaluation of the TRX phase/gain performances. It is the updated version of the Gen-2 transceiver array. The chip-on-board (CoB) PCB board photo for the Gen-2p5 array is shown in Fig. 4.38 with the board size of 4.3 x 4.3 inch².

![Image of Gen-2p5 chip-on-board PCB design]

Figure 4.38 Gen-2p5 chip-on-board PCB design with a board size of 4.3 x 4.3 inch².

4.4.3.1 Transmit Front-End Characterization

For the TX front-end, the gain and phase for element one TX (closest to hybrid) across 32 phase settings was measured. To evaluate the quadrature accuracy within the front-end, we compare the amplitude and phase difference between axis settings (0° and 90°). Figs. 4.39 (a) and (b) show measured phase error less than 7.9° and amplitude error less than 1-dB at 28 GHz, when either
only the element-one TX is turned on or when the four-element TXs are all turned on. Fig. 4.40 (a) shows the measured phase of $S_{21}$ of the single-channel receiver front-end across phase settings and the RMS phase error is $<5.6^\circ$ across 14.1-35.4 GHz. Fig. 4.40 (b) shows the differential nonlinearity (DNL) and integral nonlinearity (INL) of the phase responses, indicating errors less than $\pm0.2$ LSB. The average peak gain is 18.1 dB at 29.9 GHz and 16.7 dB at 28 GHz in Fig. 4.41 (a), when only the element-one TX is turned on. The 3-dB bandwidth is from 25.6 to 32.8 (24%). After calibration, the RMS gain error is $<1$ dB across 13.5-36 GHz. Figs. 4.42(b) and (c) show the magnitude of $S_{21}$ and gain deviation from the average gain over 32 phase settings at 26 to 30 GHz. Figs. 4.43(b) and (c) show the measured $S_{11}$ and $S_{22}$ are less than -10 dB from 10 to 40 GHz and 31.4 to 36.5 GHz. Figs. 4.44(b) and (c) show the measured $S_{21}$ phase and gain responses versus input power from -25 to 0 dBm. $S_{21}$ phase and gain responses remain relatively linear as the input power increases from -25 to 0 dBm.

The measured TX $O_{1dB}$, $P_{SAT}$, and peak PAE versus frequency at the $0^\circ$ phase setting is shown in 4.45 (a). The element-one TX front-end achieves higher than 11-dBM $O_{1dB}$, 16-dBM $P_{SAT}$, and 13-% peak PAE from 22 to 30 GHz. The measured TX $O_{1dB}$, $P_{SAT}$, and PAE versus input power at the $90^\circ$ phase setting is shown in 4.45 (b). The element-one TX front-end achieves 14.9-dBM $O_{1dB}$, 18.2-dBM $P_{SAT}$, and 14.5-% peak PAE from 28 GHz. The Gen-2p5 TX output power performance is much improved by fixing the mistuned inter-stage matching between interpolator and PA in the Gen-2 array. The measured TX $O_{1dB}$, $P_{SAT}$, PAE versus 32 phase states at 26 to 30 GHz is shown in 4.46 (a) and (b). The output noise is -125 to -117 dBm/Hz at 22-32 GHz across 32 phase settings, shown in Fig. 4.47(a) and (b). Finally, the single-channel TX front-end occupies an area of 0.15 mm$^2$ excluding output GSG pads with 304 mW power consumption, excluding currents of biasing circuits.

4.4.3.2 Receive Front-End Characterization

For the RX front-end, the gain and phase for element one RX (closest to hybrid) across 32 phase settings was measured. To evaluate the quadrature accuracy within the RX front-end, we compare the amplitude and phase difference between axis settings ($0^\circ$ and $90^\circ$). Figs. 4.48 (a) and (b) show
measured phase error less than 0.8° and amplitude error less than 0.1-dB at 28 GHz, when either only the element-one RX is turned on or when the four-element RXs are all turned on. The measured phase of the receiver front-end for element one across 32 phase settings is shown in Fig. 4.49(a).
Figure 4.41 Element-one TX front-end measured results for (a) $S_{21}$ gain response and RMS gain errors versus frequency across 32 phase settings, and (b) averaged $S_{21}$ gain response and RMS gain errors versus frequency, when other three elements of the TX front-ends are off and on.

Figure 4.42 Element-one TX front-end measured results for (a) $S_{21}$ gain and (b) $S_{21}$ gain deviation at 26-30 GHz, when other three elements of the TX front-ends are off.

After calibration, the RMS phase error is $<5.6^\circ$ across 16-31.4 GHz. Figs. 4.49(b) shows the differential nonlinearity (DNL) and integral nonlinearity (INL) of the phase responses, indicating errors less than $\pm 0.4$ LSB. The average peak gain in high-gain mode is 8.6 dB at 29.8 GHz with a 24.5% 3-dB bandwidth of 25.2-32.5 GHz in Fig.4.50(a). After calibration, the RMS gain error is $<1$ dB across 12.2-38 GHz. Fig. 4.51 (b) shows the magnitude of $S_{12}$ and gain deviation from the average gain over 32 phase settings at 26 to 30 GHz. The gain deviation is less than $\pm 0.4$ dB and can be improved by further adjustment of the pre-distortion. Figs. 4.52(b) and (c) show the measured $S_{11}$ and $S_{22}$ are
Figure 4.43 Element-one TX front-end measured results for (a) $S_{11}$ and (b) $S_{22}$ responses versus frequency across 32 phase settings, when other three elements of the TX front-ends are off.

Figure 4.44 Element-one TX front-end measured results for $S_{21}$ (a) phase and (b) gain responses versus input power across 32 phase settings at 28 GHz, when other three elements of the TX front-ends are off.

less than -10 dB from 16.9 to 40 GHz and 22.6 to 40 GHz. Furthermore, the NF in the high-gain and low-gain modes is 5.2-7 and 5-7.2 dB at 28 GHz across 32 phase settings, shown in Fig. 4.53(a) and (b).

The $iP_{1dB}$ in the high-gain and low-gain modes are -15.4 and -13.4 dBm, respectively at 28 GHz
Figure 4.45 Element-one TX front-end measured results for (a) oP$_{1\text{dB}}$, $P_{\text{SAT}}$, peak PAE versus frequency at the 0° setting, and (b) $P_{\text{OUT}}$, gain, PAE versus the input power at the 90° setting at 28 GHz, when other three elements of the TX front-ends are on.

Figure 4.46 Element-one TX front-end measured results for (a) oP$_{1\text{dB}}$ and $P_{\text{SAT}}$ versus 32 phase states at 26 to 30 GHz, and (b) peak PAE and PAE at oP$_{1\text{dB}}$ versus 32 phase states at 26 to 30 GHz, when other three elements of the TX front-ends are on.

at the 0° phase setting, as shown in Fig. 4.54(a). The iP$_{1\text{dB}}$ in the high-gain and low-gain modes across 32 phase settings at 26-28 GHz are shown in Fig. 4.54(b). Finally, the single-channel RX front-end occupies an area of 0.2 mm$^2$ excluding input GSG pads with 125.7 mW power consumption,
Figure 4.47 Element-one TX front-end measured results for (a) output noise versus frequency and versus 32 phase states, and (b) output noise versus 32 phase states at 26 to 30 GHz, when other three elements of the TX front-ends are off.

excluding currents of biasing circuits.

Figure 4.48 Measured IQ (a) phase and (b) amplitude errors for the RX front-end at 0° and 90° phase settings, when other three elements of the RX front-ends are on.
Figure 4.49 Element-one RX front-end measured results for (a) $S_{21}$ phase response and RMS phase errors versus frequency across 32 phase settings in the high- and low-gain modes, (b) $S_{21}$ phase DNL, and (c) $S_{21}$ phase INL at 26-30 GHz in the high-gain mode, when other three elements of the RX front-ends are on.

Figure 4.50 Element-one RX front-end measured results for (a) $S_{21}$ gain response versus frequency across 32 phase settings in the high-gain mode, (b) $S_{21}$ average gain response and RMS gain errors versus frequency in the high- and low- gain modes, when other three elements of the RX front-ends are on.
Figure 4.51 Element-one RX front-end measured results for (a) $S_{21}$ gain response and RMS gain errors versus frequency across 32 phase settings, (b) $S_{21}$ gain, and (c) gain deviation at 26-30 GHz all in the high-gain mode, when other three elements of the RX front-ends are on.

Figure 4.52 Element-one RX front-end measured results for (a) $S_{11}$ and (b) $S_{22}$ responses versus frequency across 32 phase settings.

4.4.4 Four-Element Transceiver Array Characterization

A chip micrograph of the four-element array was shown in Fig. 3.12. The die size is 6.9 mm$^2$ including pads and the active array area is 2.9 mm$^2$. The chip consumes 1.08 (0.87) W in transmit mode and 0.68 (0.49) W in receive mode including (excluding) the currents of biasing circuits.
Figure 4.53 Element-one RX front-end measured results for (a) noise figure versus frequency across 32 phase settings in the high-gain mode and (b) noise figure versus frequency across 32 phase settings in the low-gain mode, when other three elements of the RX front-ends are off.

Figure 4.54 Element-one RX front-end measured results for (a) $iP_{1dB}$ versus frequency at 0° setting in the high- and low-gain modes and (b) $iP_{1dB}$ versus 32 phase settings in the high- and low-gain modes at 26-30 GHz, when other three elements of the RX front-ends are on.
4.4.4.1 Transceiver Array Isolation Characterization

The complete four-element array has been characterized to reveal element-to-element isolation. Measurements demonstrate how the phase settings of adjacent elements affect the phase response of a given element, obtained by measuring the response of the first element at 0° phase setting when the settings of all other elements are changed across 32 states. The measured results in Figs. 4.55 (a) and (b) show that both TX front-ends achieve less than 1.1 ° of RMS phase-isolation error and less than 0.2 dB of of RMS gain-isolation error for 16-40 GHz. The measured results in Fig. 4.56 (a) and (b) show that both RX front-ends achieve less than 1° of RMS phase-isolation error and less than 0.2 dB of of RMS gain-isolation error for 16-40 GHz. The TRX array achieves excellent element-to-element isolation without the use of an isolation arm in the series-fed networks with low magnetic coupling, low substrate coupling, and high combiner isolation between each TX or RX channel.

Figure 4.55 Measured responses of TX element one at 0° setting while TX element two to four are swept across 32 settings for (a) measured phase and RMS phase errors and (a) measured gain and RMS gain errors of TX isolation.
Figure 4.56 Measured responses of RX element one at 0° setting while RX element two to four are swept across 32 settings for (a) measured phase and RMS phase errors and (a) measured gain and RMS gain errors of RX isolation without pre-distortion.

4.4.4.2 Transceiver Array Mismatch Characterization

The gain and phase mismatch of the four-element transceiver array are measured at 0° phase setting. The phase and gain of three elements are referenced to the element that has the lowest gain at 28 GHz. The phased array shows less than 5° of RMS phase mismatch error and less than 1.2 dB of RMS gain mismatch error at 26.6-29.8 GHz for all four TX elements (see Figs. 4.57 (a) and (b). The phased array shows less than 5° of RMS phase mismatch error and less than 0.4 dB of RMS gain mismatch error at 26.7-30 GHz for all four RX elements (see Figs. 4.58 (a) and (b). These show that the phase and gain offsets due to the physical length of the series feed network can be calibrated out across the desired frequency range. Fig. 4.59 and Fig. 4.60 both show that the measured average results after phase/gain equalizations of the four TX and RX channels. Figs. 4.59 (a) and (b) show that less than 5° of RMS phase errors and less than 0.6 dB of RMS gain errors for the four TX elements at 16 to 32 GHz. Figs. 4.60 (a) and (b) show that less than 6.2° of RMS phase errors and less than 0.9 dB of RMS gain errors for the four RX elements at 16 to 32 GHz.
Figure 4.57 Measured gain and phase responses of TX element one to three are referred to TX element four at 0° setting. (a) Measured phase and RMS phase and (b) measured gain and gain errors of TX mismatch.

Figure 4.58 Measured gain and phase responses of RX element one to three are referred to RX element four at 0° setting. (a) Measured phase and RMS phase and (b) measured gain and gain errors of RX mismatch.
4.4.5 Four-Element Transceiver Array with Up- and Down-Conversion Mixers Characterization

The complete transceiver is redesigned, including mixers, referred to as a Gen-3p5 array. This hybrid transceiver array has been designed and fabricated in 130-nm SiGe BiCMOS 8HP from
GlobalFoundries. The chip-on-board (CoB) PCB board photo for the Gen-3p5 array is shown in Fig. 4.61 with the board size of 4.4 x 4.3 inch².

![Gen-3p5 Chip-on-Board PCB Design](image)

**Figure 4.61** Gen-3p5 chip-on-board PCB design with a board size of 4.4 x 4.3 inch².

### 4.4.5.1 Transmitter Characterization

Swept-power measurements are taken with an Agilent E8257D signal generator providing the LO input, a second HP 83650B signal generator providing the BB input, a Rohde & Shwarz FSUP-43 signal-source analyzer, an Agilent N1913A power meter and an Agilent N8488A power sensor for the RF output in Fig. 4.62. The output power performance of the transmitter (TX) for element four (closest to up-conversion mixers) is characterized and measured at 0° setting. As shown in Fig. 4.63(a) and (b), the measured RF $P_{\text{OUT}}$ and PAE of the element-four transmitter achieves higher than 17.5 dBm and 11.1 % with a LO input power of > 9.4 dBm. The transmitter achieves 13.4-dBm $O_1$, 17.3-dBm $P_{\text{SAT}}$, 10.6-% peak PAE with 28-GHz LO input frequency and 100-MHz BB input...
frequency, as shown in Fig. 4.64(a). The LO leakage power and the sideband image power are less than -9 and -17 dBm versus a BB input power, as shown in Fig. 4.64(b). The measured TX \( \text{OP}_{1\text{dB}} \), \( P_{\text{SAT}} \), and peak PAE versus frequency at the 0° phase setting is shown in 4.65 (a). The element-four TX achieves \( \text{OP}_{1\text{dB}} \) of 11.2-13.7 dBm, \( P_{\text{SAT}} \) of 14.4-17.3 dBm, and peak PAE of 4.8-10.5 % from 26 to 32 GHz. The measured \( P_{\text{SAT}} \) versus LO input frequency with 100-MHz BB input frequency and 9.3 dBm BB input power is shown in 4.65 (b). The element-four TX achieves peak \( P_{\text{SAT}} \) of 17.5 dBm at 28.1 GHz with 3-dB BW of 20.6 % from 26 to 31.8 GHz. Finally, the transmitter chain consumes 464.5 mW per element and the full TX array consumes 1.86 W with 3.6-V supply voltage.

Figure 4.62 One-tone power measurement setup for the transmitter.

4.4.5.2 Receiver Characterization

Swept-power measurements are taken with an Agilent E8257D signal generator providing the LO input, a second HP 83650B signal generator providing the RF input, a Rohde & Shwarz FSUP-43 signal-source analyzer for the BB output in Fig. 4.66. The conversion gain performance of the receiver
Figure 4.63 Element-four transmitter measured results for (a) RF $P_{\text{OUT}}$ at 28.1 GHz and PAE versus LO input power at 28 GHz, and (b) LO leakage power at 28 GHz and side-band image power at 27.9 GHz versus LO input power at 28 GHz and at 0° setting, when all four elements of the TX front-ends are on.

Figure 4.64 Element-four transmitter measured results for (a) $oP_{1\text{dB}}$ at 28.1 GHz, up-conversion gain, and PAE versus BB input power at 100 MHz, and (b) LO leakage power at 28 GHz and side-band image power at 27.9 GHz versus BB input power at 100 MHz and at 0° setting, when all four elements of the TX front-ends are on.
Figure 4.65 Element-four transmitter measured results for (a) $\text{oP}_{1\text{dB}}$, $P_{\text{SAT}}$, and peak PAE versus LO input frequency with 100-MHz BB input frequency, and (b) LO leakage power and side-band image power versus LO input frequency with 100-MHz BB input frequency and at $0^\circ$ setting, when all four elements of the TX front-ends are on.

(RX) for element one (closest to down-conversion mixers) is characterized and measured at $45^\circ$ setting without the need of pre-distortion. The BBI $iP_{\text{dB}}$ and conversion gain in the high-gain and low-gain modes are -18.5 and -16.4 dBm, and 10.6 and 9.3 dB, respectively at 28-GHz LO frequency, as shown in Fig. 4.67(a). The BBQ $iP_{\text{dB}}$ and conversion gain in the high-gain and low-gain modes are -18.5 and -17.4 dBm, and 11.6 and 9.2 dB, respectively at 28-GHz LO frequency, as shown in Fig. 4.67(b). The peak conversion gain at BBI outputs in high- and low-gain modes is 13 dB at 26.9 GHz with a 30.4% 3-dB bandwidth of 22.7-30.9 GHz and 12.2 dB at 26.2 GHz with a 31.3% 3-dB bandwidth of 22.5-30.7 GHz in Fig.4.68(a). The peak conversion gain at BBQ outputs in high- and low-gain modes is 13.9 dB at 26.6 GHz with a 30.8% 3-dB bandwidth of 22.7-30.9 GHz and 11.6 dB at 26.6 GHz with a 23.3% 3-dB bandwidth of 23.4-29.6 GHz in Fig.4.68(b). The $iP_{1\text{dB}}$ versus LO input frequency in the high-gain and low-gain modes is shown in Fig. 4.69(a) and (b). Finally, the single-channel RX front-end occupies an area of 0.2 mm$^2$ excluding input GSG pads with 125.7 mW power consumption, excluding currents of biasing circuits.
Finally, the receiver chain consumes 296.4 mW per element and the full RX array consumes 1.19 W with 3.6-V supply voltage.

**Figure 4.66** One-tone power measurement setup for the receiver.

### 4.5 Chapter Summary

This chapter has demonstrated a four-element phased-array transceiver in 130-nm SiGe BiCMOS technology at Ka band for potential 5G cellular network application. The key contributions in this chapter are (1) the mixer-based approach is used for global interpolation with broadband quadrature LO, (2) a novel distributed IQ LO is developed for the wideband tunable quadrature generation, and (3) a built-in self-test network is implemented in the array. The benefits of using this architecture are to achieve wide bandwidth performance with much smaller and compact area. The capabilities of switching image beam selection for the RX array and the sideband selection for the TX can be achieved in the array.
Figure 4.67 Element-one receiver measured results for (a) BBI $P_{\text{OUT}}$ and down-conversion gain at 100-MHz BB output frequency versus RF input power at 28.1 GHz in both high- and low-gain modes, and (b) BBQ $P_{\text{OUT}}$ and down-conversion gain at 100-MHz BB output frequency versus RF input power at 28.1 GHz in both high- and low-gain modes, when all four elements of the RX front-ends are on.

Figure 4.68 Element-one receiver measured results for (a) BBI conversion gain at 100-MHz BB output frequency versus LO input frequency in both high- and low-gain modes, and (b) BBQ conversion gain at 100-MHz BB output frequency versus LO input frequency in both high- and low-gain modes, when all four elements of the RX front-ends are on.
Figure 4.69 Element-one receiver measured results for (a) BBI i_{P_{1dB}} at 100-MHz BB output frequency versus LO input frequency in both high- and low-gain modes, and (b) BBQ i_{P_{1dB}} at 100-MHz BB output frequency versus LO input frequency in both high- and low-gain modes, when all four elements of the RX front-ends are on.
This chapter presents V- and W-band frequency quadruplers in GF 8HP/8XP/9HP SiGe BiCMOS technologies. The circuit employs cascode stacks comprising an in-phase class-C common-emitter and anti-phase class-AB cascode devices to obtain current pulses at x4 frequency. Four such cascodes driven with differential and tunable quadrature increase the 4th harmonic output power while
suppressing all other harmonics by 20 dB or more. The V-band frequency quadrupler with differential quadrature excitation achieves measured >7.4-dBm 4\textsuperscript{th} harmonic output power, >5.2% power efficiency for the core of the multiplier, >22-dB harmonic suppression, and 24.3-% 3-dB bandwidth from 44.8 to 57.2 GHz. The W-band frequency multiplier with differential quadrature excitation generates >11.2/11.5 dBm output power with >30/22 dB harmonic suppression. Power efficiency is >5.8/6.8% for the multiplier core with the active PPF and with QVCO.

5.1 Millimeter-Wave LO Overview

Fig. 5.1 shows four different beamformer architectures that require local-oscillator (LO) generation and distribution blocks in the system. For the LO generation within these four beamformers, high-quality LO signals are required with having low phase noise and low undesired spurs. Also, the LO generation blocks must provide signals with high output power levels while dissipating minimum power consumption. As shown in Figs. 5.1 (a) to (c), the power consumption and area of the LO distribution network can increase dramatically as the number of elements in the phased array increases. In this chapter, I discuss the architectural trade-offs for mm-wave LO networks. Also, I discuss the key individual building blocks of the frequency multiplier, the frequency divider, and the quadrature generation circuits in the LO generation and distribution. Voltage-controlled oscillators (VCOs) are not discussed, as they are the subject of a separate research project and outside the scope of this particular thesis.

5.1.1 Millimeter-Wave LO Generation Options

Millimeter-wave radios and radars require high-quality and power-efficient LO signals. Fig. 5.2 shows a general block diagram of mm-wave LO generation consisting of a phase locked loop (PLL), a VCO, a frequency multiplier, and a frequency divider. Here, the VCO generates a system LO signal whose frequency is multiplied up by a factor of $M$ for the mm-wave transceiver blocks (to drive
mixers, for example) and divided down by a factor of $D$ for the PLL block. A number of choices exist for the mm-Wave LO generation, including selection of the frequency multiplication factor ($M$), the frequency division factor ($D$), and the fundamental oscillation frequency ($f_{\text{VCO}}$) of the VCO. The multiplied LO frequency ($f_{\text{MULT}}$) and the divided LO frequency ($f_{\text{DIV}}$) can be expressed as follows:

$$f_{\text{MULT}} = f_{\text{VCO}} \times M$$  \hspace{1cm} (5.1)$$

$$f_{\text{DIV}} = f_{\text{VCO}} \div D$$  \hspace{1cm} (5.2)$$

Table 5.1 summarizes the LO frequency ($f_{\text{VCO}}$) for multiplication factors between one and 16 and division factors between 16 and one for use in either 28-GHz 5G cellular bands, 60-GHz ISM bands, or 80-GHz FMCW radar bands. The plans are labeled as $A$ through $F$. There are various trade-offs in choosing values of $M$ and $D$. To obtain low phase noise and wide tuning range, often lower frequency oscillators are used within the synthesizer and the output signals are then multiplied up to the desired frequency [Flo08]. A higher multiplication ratio allows the oscillator and frequency divider (or prescaler) to operate at lower frequencies and to achieve better power and performance; however, a higher multiplication ratio increases the number of the stages of the frequency multipliers, which generally increases the spurious content in the final LO output signal. However, a lower multiplication ratio improves the undesired harmonic suppression due to the use...
of fewer multiplication stages, while the higher frequency oscillator and prescaler result in generally worse phase noise due to low $Q$ of the LC tank. In particular, the quality factor ($Q$) of the tank begins to be dominated by the lossy varactor, whose $Q$ is reduced at higher frequencies. Also, the VCO tuning range is generally reduced due to the fact that fixed parasitic capacitance consumes a larger portion of the total tank capacitance. Finally, the design of the frequency divider is more challenging at the higher frequency due to the trade-offs between power consumption and the frequency locking range for static and dynamic frequency dividers. If a wide-band static frequency divider is used, it consumes considerable power as the frequency increases. If the dynamic frequency divider is used, it saves power but narrows the locking range at the higher frequency.

In this work, frequency plan $D$ is selected with $M = 4$ and $D = 4$ to realize the mm-wave LO generation. In 80-GHz FMCW and 60-GHz WiGig applications, the VCO can therefore be designed at 20 and 15 GHz, respectively, to achieve the required phase noise and wide tuning range at lower power consumption. Also, the 20- and 15- GHz frequency multiplier and divider can achieve good power efficiency at the desired output harmonic with relatively low undesired output harmonics. Finally, the fact that the VCO operates at a different frequency from the PA's output frequency minimizes the LO pulling from the large signals of the PAs.

![Figure 5.2 General block diagram of millimeter-wave LO generation with phase locked loop (PLL), voltage controlled oscillator (VCO), frequency multiplier, and frequency divider.](image)

Figure 5.2 General block diagram of millimeter-wave LO generation with phase locked loop (PLL), voltage controlled oscillator (VCO), frequency multiplier, and frequency divider.
Table 5.1 Frequency plans for millimeter-wave LO generation versus $N$ and $M$

<table>
<thead>
<tr>
<th>Plan</th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>F</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mult. (M)</td>
<td>1</td>
<td>2</td>
<td>3</td>
<td>4</td>
<td>8</td>
<td>16</td>
</tr>
<tr>
<td>Div. (D)</td>
<td>16</td>
<td>8</td>
<td>6</td>
<td>4</td>
<td>2</td>
<td>1</td>
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</table>

**5G Cellular Bands (28 or 39 GHz)**

<table>
<thead>
<tr>
<th>$f_{MULT}$ (GHz)</th>
<th>28/39.2</th>
<th>27/39.6</th>
<th>28/39.2</th>
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</thead>
<tbody>
<tr>
<td>$f_{DIV}$ (GHz)</td>
<td>1.75/2.45</td>
<td>1.5/2.2</td>
<td>1.75/2.45</td>
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<tr>
<td>$f_{VCO}$ (GHz)</td>
<td>28/39.2</td>
<td>14/19.6</td>
<td>9/13.2</td>
</tr>
</tbody>
</table>

**ISM Bands for 57-64 GHz**

<table>
<thead>
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<th>63</th>
<th>60</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{DIV}$ (GHz)</td>
<td>3.75</td>
<td>3.5</td>
<td>3.75</td>
</tr>
<tr>
<td>$f_{VCO}$ (GHz)</td>
<td>60</td>
<td>30</td>
<td>21</td>
</tr>
</tbody>
</table>

**FMCW Radar Bands for 76-81 GHz**

<table>
<thead>
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<th>$f_{MULT}$ (GHz)</th>
<th>80</th>
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<th>80</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{DIV}$ (GHz)</td>
<td>5</td>
<td>4.5</td>
<td>5</td>
</tr>
<tr>
<td>$f_{VCO}$ (GHz)</td>
<td>80</td>
<td>40</td>
<td>27</td>
</tr>
</tbody>
</table>

5.1.2 Millimeter-Wave LO Distribution Options

Once a high-quality LO signal is generated, the next step is to find ways to distribute the LO signal from the main LO generation block to the local individual elements. The LO distribution network usually consumes a large portion of the DC power consumption within the system. There are multiple strategies that can be used to distribute an LO signal, which provide trade-offs between routing complexity, DC power consumption, minimum LO power for the mixers, and the area. The first LO distribution option in Fig. 5.3(a) is to use one central PLL and VCO to generate the LO signal at the lower fundamental local oscillation frequency ($f_{VCO}$). Then the LO signal is multiplied up to
to be at $M \times f_{VCO}$ by the frequency multiplier. The higher frequency LO signal is then distributed to each individual element through the LO distribution network. The power consumption of this first LO-distribution option can be expressed as:

$$P_{Total} = P_{VCO} + P_{Div} + P_{PreAmp} + P_{Mult} + N \times P_{PostAmp} + N \times P_{Buffer} \quad (5.3)$$

where $P_{Buffer}$ is the power consumption of the LO buffers, $P_{PostAmp}$ is the power consumption of the additional post-amplifier, $P_{VCO}$ is the power consumption of the VCO, $P_{Div}$ is the power consumption of the frequency divider, $P_{PreAmp}$ is the power consumption of the additional pre-amplifier, and $P_{Mult}$ is the power consumption of the frequency multiplier. I assume a power consumption for each block in the LO distribution network based on [Fuj17; Wan14], as summarized in Table 5.2. Note that the power consumption of the PLL, the phase shifter, and the mixers are not included in the calculation of the power consumption of the LO distribution network.

### Table 5.2 DC power consumption of building blocks in LO distribution networks

<table>
<thead>
<tr>
<th>At 25°C</th>
<th>DC power consumption* in [Fuj17; Wan14]</th>
</tr>
</thead>
<tbody>
<tr>
<td>20-GHz VCO</td>
<td>200 mW</td>
</tr>
<tr>
<td>20-to-5-GHz static frequency divider ($D = 4$)</td>
<td>80 mW</td>
</tr>
<tr>
<td>20-GHz pre-amplifier</td>
<td>50 mW</td>
</tr>
<tr>
<td>20-to-80-GHz frequency multiplier ($M = 4$)</td>
<td>70 mW</td>
</tr>
<tr>
<td>80-GHz post-amplifier</td>
<td>70 mW</td>
</tr>
<tr>
<td>80-GHz LO buffer</td>
<td>70 mW</td>
</tr>
</tbody>
</table>

* The power consumption of the PLL, the phase shifter, and the mixers is not included in the calculation of the LO distribution network.

To begin the analysis, I assume that the mixer in each individual element requires a minimum of +5-dBm LO power ($P_{MIXER}$) at 80 GHz ($M=4$ and $f_{VCO}=20$ GHz). I also assume that the (optional)
phase shifter and the LO buffer achieve a cascaded 10-dB gain (0 dB from the phase shifter and 10 dB from the buffer) and saturated output power of 5 dBm at 80 GHz. As a result, more than -5-dBm of $P_{1\rightarrow N}$ is required at the input of the phase shifter within each individual element. An additional post-amplifier (in green) with 10-dB gain is needed to achieve the required -5-dBm LO power at 80 GHz. Therefore, a minimum input power of -15 dBm is required to drive the post-amplifier into saturation after the LO signal is split. For the array with $N=16$, cascading four stages of the H-tree power splitting network is required for the 1-to-16 LO power distribution. If the loss for each stage of the dividing network is 2 dB at 80 GHz, the total loss plus 3-dB power split of the four-stage power dividing networks is 20 dB. As a result, the required output power, $P_{MULT}$, generated by the frequency multiplier should be > 5 dBm, which is already very challenging at 80 GHz. In addition, the frequency multiplier usually suffers from low conversion gain, meaning more input power $P_{VCO}$ is needed at the fundamental frequency to drive the multiplier into saturation. Therefore, an additional 20-GHz pre-amplifier (in grey) is usually needed to provide the +5-dBm input power at 20 GHz. According to the required LO power within each stage, the total calculated power consumption of the first LO distribution option can be as high as 2.64 W for $N=16$. Although the benefit of distributing the LO signal at the higher frequencies is area efficiency for the LO distribution network, the high loss must be compensated by adding post-amplifiers, resulting in higher power consumption.

The second LO-distribution option is to distribute the LO signal at the lower frequency of $f_{VCO}$ and then the LO signal is locally multiplied up by the frequency multiplier with a factor of $M$ within an individual element, as shown in Fig. 5.3(b). The same assumptions can be applied into the analysis of the second option. The mixers in the individual element require a minimum of 5-dBm LO power of $P_{MIXER}$ at 80 GHz. The (optional) phase shifter and the LO buffer achieve 10-dB gain at 80 GHz so that greater than -5 dBm of $P_{MULT}$ is required at the output of the frequency multiplier. This is easier than the first option, where the multiplier output power is essentially distributed across the array. The minimum $P_{1\rightarrow N}$ is also greater than -5 dBm with 0-dB conversion gain for the frequency multiplier. At the lower frequency, the loss of each stage of the power divider is reduced
to approximately 1 dB at $f_{VCO}$ of 20 GHz. As a result, the total loss plus 3-dB power split of the four-stage dividing networks is 16 dB. The VCO therefore needs to generate $> 11$ dBm output power at 20 GHz. Therefore, a two-stage pre-amplifier (in grey) is required to buffer the VCO’s output. The power consumption of the second option can be expressed as:

$$P_{Total} = P_{VCO} + P_{Div} + 2 \times P_{PreAmp} + N \times P_{Mult} + N \times P_{Buffer}$$  \hspace{1cm} (5.4)

As a result, the total calculated power consumption of the second LO-distribution option is 2.62 W, while N=16. The benefit of distributing the LO signal at the lower frequencies reduces the loss of the LO distribution network but the area could be large.

In both options, the power consumption of the LO distribution network is similar. Notice that the frequency multiplier plays the important role of providing power-efficient performance for the LO distribution network. If the power efficiency of the frequency multiplier can be improved, the overall DC power of the LO distribution network can be reduced by eliminating the number of the stage of the pre-amplifier operating at $f_{VCO}$ or the post-amplifier operating at $M \times f_{VCO}$.

For example, in the first LO-distribution option in Fig. 5.3(a), if the output saturated power of the frequency multiplier can be improved to 10 dBm at 80 GHz with the same DC power consumption of 70 mW, the number of the post-amplifiers can be reduced to eight ($N/2$). The overall power consumption can be reduced to 2.08 W, which is a 21% improvement of DC power consumption in the LO distribution network.

### 5.1.3 Research Objectives for Millimeter-Wave Frequency Multiplier

The frequency multipliers in the LO system must exhibit wideband and robust operation, provide high output power, and suppress unwanted harmonics while consuming minimal power. As just mentioned, higher multiplication ratios allow the oscillator and prescaler to operate at lower frequencies, with $M=2, 3, \text{ or } 4$ common. For x4 multiplication, cascaded doublers [For09; Hac02] can
be employed. The doubler can be implemented with a self-mixing doubler [Hac02] in Fig. 5.4(a), an unbalanced doubler using nonlinear class-B/C stages [Fag00], or a balanced doubler using the push-push technique [Hun05] in Fig. 5.4(b). For the direct x4 multiplication, a multiplier using nonlinear class-B/C stage [Kuo10] in Fig. 5.4(c) or using the linear superposition (LS) technique [Hua08] in Fig. 5.4(d) can be employed; however, most of them generally offer very low power efficiency due to the need for saturated multiple stages, low fourth-harmonic output power, or significantly amplified fundamental input or fourth-harmonic output signals. Fig. 5.5 summarizes the fourth-harmonic $P_{\text{out}}$ and power efficiency ($\eta$) versus fourth-harmonic output frequency of state-of-the-art frequency quadruplers in SiGe and CMOS technologies. Quadrupler cores based on cascaded self-mixing doublers, direct x4 using class B/C amplifiers, or direct x4 using the LS technique have been reported with fourth-harmonic $P_{\text{out}}$ and power efficiency ($\eta$) of -4 dBm and 0.5% at 77 GHz [For09], -10 dBm and 0.9% [Kuo10] at 60 GHz, or -46 dBm and 0.0002% at 324 GHz [Hua08], respectively. Alternatively, a phase-controlled push-push (PCPP) topology can be used, employing stacked transistors driven out-of-phase with an overlapping conduction angle. As will be seen, this circuit can achieve a higher power efficiency of 9% excluding input buffers and 1.6% including input buffers [Wan12] with output power of -2.4 dBm at 129 GHz; however, the original design suffers from high harmonic generation at the second and sixth harmonics, requiring large output notch filter(s),
which decreases the output power due to the loss at the desired fourth harmonic. An alternative of improving wideband harmonic rejection is to use switchable bandpass filters [Chu17]; however, the fourth-harmonic output power is also degraded due to the loss from the switches and the bandpass filters. The research goal in this chapter is to achieve highly efficient frequency multiplication with low unwanted harmonics in the mm-Wave LO generation and distribution systems.

In the following sections, I present a theory and design methodology for self-mixing phased-controlled push-push frequency multipliers and then hardware results for SiGe BiCMOS quadruplers operating at 60 or 80 GHz output frequencies. These multipliers exhibit excellent power efficiency and low spurious content, while operating over a wide frequency range. As such, they are ideal solutions for general-purpose mm-wave LO generation systems.

5.2 Self-Mixing Phased-Controlled Push-Push Technique

A frequency multiplier based on the self-mixing phase-controlled push-push (PCPP) method was originally proposed in [Wan12]. A key benefit of using the self-mixing PCPP technique to directly synthesize the fourth harmonic is a substantially enhanced power efficiency; however, the prior work required bulky filters to eliminate spurs. In this work, I present a topology based on quadrature balancing which cancels unwanted harmonics while reinforcing the wanted harmonic.

5.2.1 Balanced Push-Push Method

To understand the theory behind the PCPP topology, I begin with an analysis of a single non-linear device, as shown in Fig. 5.6 (a). The base-bias voltage in an NPN bipolar transistor must be equal or less than the turn-on or threshold voltage \( V_t \). Thus, the transistor conducts only during the positive half of the excitation cycle, and the collector conducts in pulses; the shape of the pulses is approximately a rectified cosine. The duty cycle of the pulses varies with the DC base bias \( V_B \); if \( V_B = V_t \), the duty cycle is 50 %, but if \( V_B < V_t \), the transistor is turned off over most of the excitation
Figure 5.4 Millimeter-wave frequency quadruplers implemented with (a) cascaded self-mixing doublers, (b) cascaded push-push doublers, (c) a direct x4 multiplier using nonlinear class-B/C stage, and (d) a direct x4 multiplier using linear superposition (LS) technique.

Fig. 5.6 (a) shows the input voltage waveform of $V_{IN}$ with $V_B$ of 0.8 V and the peak-to-peak voltage swing of 0.4 V and the collector output current waveform of the transistor. The collector current peaks at the value $I_{max}$, and the current pulses have the time duration $t_0$, which is equal or less than the period of the input voltage excitation of $T$. If the collector current is modeled as a train cycle. The duty cycle then is less than 50%.
Figure 5.5 (a) $4^{th}$ $P_{out}$ and (b) $4^{th}$ efficiency ($\eta$) versus $4^{th}$ output frequency of state-of-the-art frequency quadruplers in SiGe (in red) and CMOS (in blue) technologies.

Figure 5.6 The simplified schematics and the timing diagrams running at 1 kHz for (a) the single non-linear transistor, and (b) the push-push doubler with differential excitation.

of rectified cosine pulses in Fig. 5.6 (a), using a Fourier series expansion, it can be represented as

$$I_c(t) = I_0 + I_1 \cos(w_p t) + I_2 \cos(2w_p t) + \ldots$$  \hspace{1cm} (5.5)

When $n \geq 1$, the coefficients are

$$I_n = I_{max} \frac{4t_0}{\pi T} \left| \frac{\cos(n\pi t_0/T)}{1-(2n\pi t_0/T)^2} \right|$$  \hspace{1cm} (5.6)
where $I_n$ is the $n^{th}$ harmonic current component, $I_{\text{max}}$ is the maximum current, $t_0$ is the length of the pulse, and $T$ is the period of the input fundamental frequency. When $n=0$, the coefficient is

$$I_0 = I_{\text{max}} \frac{2t_0}{\pi T} \quad (5.7)$$

To maximize the $n^{th}$ harmonic output power efficiency, we must maximize $I_n$ by adjusting $t_0/T$. Thus, we need to adjust $V_B$ so that $I_c$ has the desired period of conduction $t_0$. Selecting $t_0/T$ to achieve an acceptable trade-off between gain and output power is an important part of the design process.

A balanced frequency doubler is shown in Fig. 5.6 (b) [Hun05]. The base voltage $V_B$ of the transistors $Q_{1-2}$ is also biased to be equal or less than the turn-on voltage $V_t$ and is driven by differential input signals at 0° and 180°. The output current currents $I_{C1}$ and $I_{C2}$ are summed at the collector nodes of $Q_{1-2}$. Fig. 5.6 (b) also shows that the differential input voltage waveforms with the base voltage of 0.8 V and the peak-to-peak voltage swing of 0.4 V and the collector output current waveforms of the transistors. Each transistor of $Q_1$ or $Q_2$ only turns on at the half cycle of the input excitation but the output current currents of $I_{C1}$ and $I_{C2}$ are 180° out-of-phase due to the input differential excitation. Thus, the summed current can be represented as

$$I_0 = I_{\text{max}} \frac{4t_0}{\pi T} \quad (5.8)$$

$$I_n = 0, \ n \text{ is odd} \quad (5.9)$$

$$I_n = I_{\text{max}} \frac{8t_0}{\pi T} \left| \cos \left( n \pi t_0/T \right) \right| \left( 1 - \left( 2n \pi t_0/T \right)^2 \right)^{1/2}, \ n \text{ is even} \quad (5.10)$$

The odd-harmonic currents are canceled while the even-harmonic currents are added in-phase so that the maximum current $I_{\text{MAX}}$ is doubled. In [Hun05], to maximize the second harmonic current $I_2$, the conduction duty cycle ($t_0/T$) of each transistor $Q_1$ and $Q_2$ is 0.32, which results in a
conduction angle of 115.2° and makes $I_0/I_2$ equal to 0.74.

5.2.2 Balanced Self-Mixing Phase-Controlled Push-Push Method

![Figure 5.7](image.png)

**Figure 5.7** The simplified schematics and the timing diagrams running at 1 kHz for (a) the self-mixing phase-controlled cascode circuit, and (b) the self-mixing phase-controlled push-push (PCPP) cascode circuits with differential excitation.

To generate strong fourth-harmonic current $I_4$, a cascode transistor can be added on the top of the non-linear transistor to perform the self-mixing function of the rectified current. Transistors $Q_1$ and $Q_2$ form a single phase-controlled “unit-cell” cascode circuit, as shown in Fig. 5.7(a). The bottom transistor $Q_1$ that acts as the rectified circuit is driven with the input signal and biased in class-C for $<180°$ conduction angle ($\alpha$). The class-C current pulse is generated from the bottom transistor $Q_1$ with the $V_{B1}$ of 0.8 V. The top transistor is driven with the inverted input signal and biased in class-AB for $>180°$ conduction angle ($\beta$). When the base of the top transistor $Q_2$ is biased at $V_{B2}$ of 1.1 V, the collector voltage $V_{C1}$ follows the top input voltage of $V_{IN2}$ of the top transistor. Due to the opposite phase of the $V_{IN2}$, the class-C current generated from the bottom device is suppressed at the peak. The suppression region needs to fail well within the center of the conduction angle $\alpha$ of the bottom transistor $Q_1$. Thus, the overlap between the top and bottom conduction angles
results in two conduction regions for the cascode, or effectively two current “pulses” per half-cycle of the input. In Fig. 5.7(a), these pulses are labeled as “1” and “2”. To model these “M”-shaped current pulses, the rectified current generated from the bottom transistor $Q_1$ can be multiplied with an opposite-phase input voltage at the fundamental frequency due to self-mixing stage of the top transistor $Q_2$.

### 5.2.3 Quadrature Self-mixing Phase-controlled Push-push Method

In Fig. 5.7(b), the addition of an anti-phase unit cell $Q_3$ and $Q_4$ results in pulses “3” and “4”, providing the x4 multiplication while adding even-order harmonics and suppressing odd-order harmonics. Our biasing condition is opposite to that discussed in [Wan12], and results in higher output power generation due to stronger more well-defined x4 current pulses.

The circuit as described will generate $2^{nd}$ harmonics, caused by any mismatch between the two current pulses generated within a single unit cell. To suppress these harmonics, we extend the design to have quadrature excitation. Namely, two additional unit cells ($Q_5$-$Q_8$) are added driven with balanced quadrature input signals, as shown in Fig.5.8 (a). The $Q/Q$ unit cell generates pulses at positions 2 and 3, whereas the $Q/Q$ unit-cell generates pulses at positions 1 and 4, all of which reinforce the $4^{th}$ harmonic signal. Accurate quadrature alignment of the input signals results in cancellation of the $2^{nd}$ (and $6^{th}$) harmonics as any pulse imbalance is now equalized through the addition of two mismatched pulses. Fig.5.8 (b) shows that the $2^{nd}$, $6^{th}$, and $10^{th}$ harmonics are canceled out of phase but the $4^{th}$ and $8^{th}$ are added in phase. Since the $8^{th}$ harmonic frequency is far away from the $4^{th}$ harmonic frequency, the $8^{th}$ harmonic should be suppressed and filtered significantly by the output matching network. As a result, no harmonic filters are required as found in [Wan12]. This reduces the loss of the output matching network at the $4^{th}$ harmonic frequency and improves $4^{th}$ harmonic power efficiency.
Figure 5.8 (a) The simplified schematics and the timing diagrams running at 1 kHz for the PCPP cascode circuits with quadrature excitation, and (b) the harmonic output power versus output harmonics with differential and quadrature input excitations

5.3 Frequency Multiplier Implementation

Multiple variants of the multiplier have been designed and fabricated in different processes using GlobalFoundries 8HP, 8XP, and 9HP SiGe BiCMOS technologies for 60-GHz WiGi and 76-to-81-GHz radar applications. These allow exploration of the topology across frequency and technology. Two possible block diagrams for the quadrature-balanced frequency quadruplers are shown in Fig.5.9. Differential quadrature signals can be generated at the input using an input transformer followed by a tunable poly-phase filter, as shown in Fig.5.9(a). Alternatively, a quadrature voltage-controlled oscillator (QVCO) can be used, as shown in Fig.5.9(b). In either case, the I and Q signals are buffered using variable-gain amplifiers (VGA) and then fed into the quadrature frequency quadrupler having an embedded current-reuse output amplifier. Here, I will investigate both approaches for quadrature generation and multiplier excitation.

5.3.1 Wideband Differential Quadrature Generation

Generating quadrature phases can be accomplished with a 90° coupler [Yeh17a] or a 90° hybrid [CF06]. Although couplers and hybrids made of distributed components can achieve very low loss
Figure 5.9 Block diagram of frequency multipliers using (a) tunable differential quadrature generator, and (b) quadrature VCO

at 10-20 GHz, they are large and suffer from limited bandwidth of quadrature accuracy. A 90° hybrid [CF06] can be realized with lumped components to reduce area [Vog92]; however, the bandwidth of quadrature accuracy is decreased and the hybrid also requires wideband terminations at each port. The following subsections discuss the wideband differential quadrature generation using either a tunable poly-phase filter (PPF) [YF15], a static frequency divider in Appendix-A [Fuj17], or a quadrature VCO in Appendix-B [Sch08].

5.3.1.1 Passive Tunable Polyphase Filter

As will be shown, high harmonic rejection within the multiplier is derived from the use of accurate and wideband quadrature signals. The PPF can generally achieve wideband performance with sufficient quadrature accuracy by cascading two or more stages [Kul13]; however, cascading multiple stages of the filters suffer from very high loss at mm-wave frequencies. To achieve wideband quadrature accuracy using a single-stage design, a type- $a$ PPF with constant quadrature amplitude in [Kul13] is modified such that the capacitors are realized with reverse-biased Schottky diodes to provide tunability of quadrature phase versus frequency, as shown in Fig. 5.10(a). This is investigated using GF SiGe 9HP technology. The Schottky diodes are implemented for a tunable capacitance
range of 28 to 50 fF and Q > 40 at 15 GHz. Through tuning of the capacitance, the quadrature offset at a given frequency can be adjusted. The cathodes of the diodes are connected to a tuning voltage through the center tap of the input transformer, whereas the anode is grounded through an RF choke ($R_{big}$). The image rejection ratio (IRR) is a function of quadrature signal amplitude and phase mismatch and is defined by [Kau08]

$$\text{IRR} = \frac{1 + 2 \cdot \alpha \cdot \cos(\theta) + \alpha^2}{1 - 2 \cdot \alpha \cdot \cos(\theta) + \alpha^2}$$

where $\alpha$ is quadrature amplitude mismatch and $\theta$ is quadrature phase mismatch. As shown in Fig. 5.10(b), the pole of the PPF can be tuned from 10 to 18 GHz for $V_{\text{tune}}$ varying from 0.1 to 3.3 V in the simulation. Estimated insertion loss for the filter is 14 dB at 15 GHz. Following the PPF, $I$ and $Q$ variable-gain amplifiers (VGA) are included to compensate for the loss and drive the multiplier into saturation. The VGAs employ impedance-matched differential cascodes and have a simulated 15-dB gain and +9-dBm saturated output power with DC power consumption of 50 mW.

**Figure 5.10** (a) A transformer and tunable PPF with Schottky diodes in GF 9HP technology (b) simulated image-rejection ratio (IRR) and IQ phase difference.
5.3.1.2 Active Tunable Polyphase Filter

In the previous section, two $I$ and $Q$ VGAs are needed to compensate the loss from the a single-stage PPF. These VGAs have to provide enough output power, greater than 5 dBm, to drive the frequency multiplier into saturation. This leads to a degradation of the overall power efficiency in the LO generation due to the high DC power consumption of the two $I$ and $Q$ VGAs. An alternative is to drive the PPF in the current-domain instead of in the voltage domain [CL10].

Here, a new circuit called the active poly-phase filter is introduced to merge a passive PPF and two pre-amplifiers into a single structure with a single input and dual- $I$ and $Q$ outputs. A schematic is shown in Fig. 5.11 (a). The modified tunable passive PPF in Fig. 5.11 (b) is realized in the current domain at the collectors of the $G_m$ stage of $Q_{1−2}$. The tunable passive PPF with fixed capacitance ($C_1$) of 0.1 pF and the tunable capacitance ($C_{Diode}$) implemented with the reverse-biased hyper-abrupt varactor (havar) diodes achieves a capacitance range of 160-220 fF at 20 GHz. Through tuning of the capacitance, the quadrature offset at a given frequency can be adjusted. The diodes are connected with two series AC-coupling capacitance ($C_{big}$) of 1 pF to block the DC voltages. The cathodes of the diodes are connected to a tuning voltage through an RF choke ($R_{big}$) of 4 kΩ, whereas the anode is grounded also through an RF choke ($R_{big}$). Resistors ($R_1$) of 54 Ω provide the DC-current path to the $G_m$ stage of $Q_{1−2}$ and the cross-coupled transistors of $Q_{3−10}$. The interconnects are modeled with $T_{1−4}$ at the quadrature outputs results into several crosses with different length, which leads to different parasitic capacitance and inductance. Careful parasitic extraction with EM simulation is needed to achieve good quadrature accuracy over frequencies.

The in-phase and quadrature-phase currents are split and flow into the cross-coupled transistors of $Q_{3−10}$. The base voltages of the transistors $Q_{3−10}$ are controlled by inverse- $tanh$ diodes implemented with transistors $Q_{11−14}$. The voltages of $V_{CI}$ and $V_{CQ}$ vary from 0 to 2.5 V to control the gain response of $I$ and $Q$ VGAs with the reference voltage ($V_{Ref}$) of 1.5 V. A supply voltage of 3.3 V is provided through the primary inductor of the output transformers of $M_{2−3}$. 

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As shown through simulation in Fig. 5.12(a), the pole of the PPF can be tuned from 15.3 to 22 GHz for $V_{\text{tune}}$ varying from 0.1 to 3.3 V. The I and Q phase tuning range is $20^\circ$ at 20 GHz. Fig. 5.12(b) shows that simulated $S_{21}$ and $S_{31}$ magnitude responses are 4.6 and 4.9 dB at 20 GHz when $V_{\text{tune}}$ is 3.3 V.

### 5.3.2 Self-Mixing Phase-Controlled Push-Push Frequency Multiplier Core

The frequency multiplier using self-mixing phase-controlled push-push (PCPP) method was originally proposed in [Wan12]. This work demonstrates a frequency multiplier which achieves 9% (1.6% including input buffers) power efficiency at 1.6 V, with a -2.4 dBm output power at 131 GHz. However, the frequency multiplier produces strong undesired 2$^{nd}$ and 6$^{th}$ harmonics at the output. Here, I introduce and demonstrate a quadrature-balanced PCPP structure that can achieve good efficiency and good harmonic suppression, using circuits realized in GF BiCMOS 8HP, 8XP, and 9HP technologies.

#### 5.3.2.1 Balanced Frequency Quadrupler Using Output Notch Filters

A circuit schematic for a balanced frequency quadrupler driven with an input pre-amplifier is shown in Fig. 5.13. For measurement purposes, an input LC balun is employed to convert the single-ended input to a differential output for the input differential pre-amplifier. The LC balun consists of a low-pass filter ($L_1$=400 pH and $C_3$=170 fF) and a high-pass filter ($C_2$=160 fF and $L_2$=400 pH). The phase difference is approximately $180^\circ$ with an amplitude difference of -1 to 3 dB from 18 to 22 GHz. The input pre-amplifier is used to generate enough output power of $>-3$ dBm to drive the frequency multiplier into saturation at the fundamental frequency of 20 GHz and also to provide the isolation between the VCO and the multiplier. Differential cascode circuits ($Q_{1-4}$) are selected for better gain and isolation. An LC network, consisting of $L_3$=430 pH, $R_1$=800 Ω, and $C_{4-7}$=350 fF, is used to match to differential 50 Ω for the input of the multiplier. Simulations show that the preamplifier provides -3.5-dBm output power and 8.5-dB gain at 20 GHz. The 3-dB bandwidth is
Figure 5.11 Schematics of (a) an active poly-phase filter and (b) a tunable passive poly-phase filter in GF 8XP technology

22% from 17.8 to 22.3 GHz, covering the operating region of the VCO. The circuit consumes 16 mW with 2.5-V supply voltage at 27°C.

A schematic of the frequency multiplier is shown in Fig. 5.13. An inter-stage matching network
consisting of $T_{2-5}$ is used to maximize power transfer from the preamplifier to the multiplier. The multiplier core consists of two unbalanced PCPP unit cells. The bottom transistors of $Q_{5,7}$ with a size of 24 $\mu$m are biased at the Class-C region through a current-mirror circuit connecting at $V_{C1}$ while the top devices of $Q_{6,8}$ with size of 16 $\mu$m are biased at the Class-AB region through another current-mirror circuit connecting at $V_{C2}$. Transmission lines (t-line) $T_{6,7}$ are inserted to provide necessary phase adjustment to achieve $180^\circ$ out of phase for the inputs of the top and bottom devices. Fig. 5.14(a) shows that the maximum simulated 4$^{th}$ output power of 2.4 dBm occurs for a 75-$\mu$m length phase-shifting t-line. The self-mixing currents are combined at the collector nodes of $Q_{6,8}$ and then flow into the common-base (CB) stage amplifier of $Q_9$, which has a size of 36 $\mu$m. The CB stage is added to provide a low impedance for summing the current at the emitter node of $Q_9$.

The two phase-controlled cascode circuits can be used to cancel odd harmonics and add even harmonics at the output by applying the opposite sine signals at the inputs. Thus the even harmonics are dominant at the output, especially the second and sixth harmonic signals. A quarter-wavelength open-circuit stub can be used to suppress all undesired even harmonics at the output. However,
the length of the quarter-wavelength open-circuit stub is too big to be implemented at this second-harmonic frequency. Thus, a stub terminated by a capacitor can be used to minimize the size [Ito06]. By appropriately choosing the length of the stub and the capacitance, a zero is produced at a desired frequency. In this design, the output matching networks are composed of two notch filters to suppress the second and sixth harmonics. The second-harmonic notch filter is formed by the t-line of $T_9$ with a series $C_{12}=300 \text{ fF}$ to reduce the quarter-wavelength t-line at the second harmonic frequency. The sixth-harmonic notch filter is implemented with a quarter-wavelength open stub at the sixth harmonic frequency. At the fourth harmonic frequency, the second-harmonic notch filter should ideally be open and the sixth-harmonic notch filter should be part of the matching network with other matching components of $T_{8,11,12}$, $R_4$, $C_{13}$, and $C_{pad}$. The simulated insertion loss of the notch filters is shown in Fig. 5.14 to achieve $>23$-dB suppression the both second and sixth harmonic frequencies; however, the loss of the filters is around 2.5 dB at the fourth harmonic frequency.

A 80-GHz self-mixing phase-controlled push-push (PCPP) frequency quadrupler with output second- and sixth-harmonic notch filters is designed and implemented in 120-nm SiGe BiCMOS GF 8HP technology. In simulation, the quadrupler with the input preamplifier achieves a peak fourth-harmonic output power of 5.2 dBm, a gain of 18.8 dB, and PAE of 3.65% at 80 GHz. The harmonic suppression is higher than 24 dB for first to eighth harmonics at 20-GHz input fundamental frequency.

5.3.2.2 Quadrature Frequency Quadrupler Using Tunable Differential Quadrature Excitation

An alternative method for suppressing undesired even harmonics is to excite the frequency quadrupler with differential quadrature inputs in Fig. 5.8 (a). The schematic of the frequency multiplier with differential quadrature input excitation is shown in Fig. 5.8. The bottom transistors of $Q_{1,3,5,7}$ with a size of 12 $\mu$m are biased at the Class-C region through a current-mirror circuit connecting at $V_{B1}$ while the top devices of $Q_{2,4,6,8}$ with a size of 8 $\mu$m are biased at the Class-AB region through another
current-mirror circuit connecting at $V_{B2}$. The self-mixing currents are combined at the collector nodes of $Q_{2,4,6,8}$ and flow into the common-base (CB) stage amplifier of $Q_9$ with a size of 40 $\mu$m. Adding the CB stage provides a low impedance for summing the current at the emitter node of $Q_9$.

In Fig.5.15, to increase fourth-harmonic output power, notch filters at that frequency consisting of $T_3$ and $C_3$ have been added to the bases of each top transistor to reduce collector-to-base feedback [Hun05]. Fig.5.16 (a) shows the simulated $S_{21}$ of the fourth notch filter to achieve > 20 dB suppression at 80 GHz. Fig.5.16 (b) shows the fourth output power versus the fundamental input power for the
frequency quadruplicator with or without the fourth notch filter. The fourth-harmonic output power can be improved by at least 5 dB for the quadruplicator including the fourth notch filter at 80 GHz.

Since the pulses are derived from overlapping conduction angles, it is imperative to have proper phase alignment for the quadrature drive signals. To this end, transmission lines $T_6-T_9$ are used to align the opposite phases at the bases of the cascode [Wan12]. Fig.5.17 (a) shows the fourth $P_{out}$ versus the length of the phase-shifter t-lines $T_6-T_9$ with and without the fourth input notch filter. Adding the fourth input notch filter could introduce additional insertion phase shift at 20 GHz so that the length of the phase-shifter t-lines can be shortened. Fig.5.17 (b) shows the fourth $P_{out}$ versus the length of the inter-connect t-lines $T_{10}-T_{11}$ with the fourth input notch filter. The length of t-lines $T_{10}-T_{11}$ should be as short as possible for combining fourth-harmonic currents in phase. Also, the biasing of the top and bottom transistors is critical such that the two conduction angle overlap regions result in phase-optimized x4 operation. The output signals from the quadruplicator are summed in the current domain and fed to a common-base output buffer whose output load is optimized for maximum power generation. Embedding this output amplifier within the multiplier
provides higher output power and improved efficiency through current re-use.

An 80-GHz self-mixing phase-controlled push-push (PCPP) frequency quadrupler with differential quadrature excitation is designed and implemented in both SiGe BiCMOS GF 8XP and 9HP technologies. Two approaches for generating the differential quadrature input signals are explored, namely using the QVCO described in Appendix A and using the PPF described in previous sections. The frequency quadrupler with the input active PPF in GF 8XP technology achieves a simulated peak fourth-harmonic output power of 3.6 dBm, a gain of 13.6 dB, and PAE of 1.2% at 80 GHz. The harmonic suppression is higher than 20 dB for first to eighth harmonics at 20-GHz input fundamental frequency.

![Simplified schematic of the frequency quadrupler](image)

**Figure 5.15** Simplified schematic of the frequency quadrupler
Figure 5.16 (a) Simulated $S_{21}$ of the 4$^{th}$ input notch filter and (b) simulated 4$^{th}$ $P_{out}$ versus fundamental $P_{in}$, with/without the 4$^{th}$ input notch filter.

Figure 5.17 (a) Simulated 4$^{th}$ output power of the quadrupler versus the length of the phase-shifter t-line with and without 4$^{th}$-notch filter, and (b) 4$^{th}$ output power of the quadrupler versus the length of the inter-connect t-lines ($T_{10}$ and $T_{11}$) with 4$^{th}$-notch filter

### 5.4 Measurement Results

Many different variants of the quadrature generation circuits and the frequency multipliers have been fabricated in different processes using GlobalFoundries 8HP, 8XP, and 9HP SiGe BiCMOS
technologies. The measured results for each variant are presented in the following sections.

5.4.1 20-GHz Active Tunable Polyphase Filter Characterization

A 20-GHz active tunable PPF is designed and fabricated in GlobalFoundries 8XP 0.12-µm SiGe BiCMOS technology. The process features high-performance NPN transistors with $f_T/f_{MAX}$ of 250/315 GHz, along with 120-nm CMOS and a full suite of passives. A chip micrograph of the active PPF is shown in Fig. 5.18. The die size is 0.84 mm$^2$ including pads. All measurements were performed through wafer probing. $S$-parameter and gain/phase responses measurements were taken using a two-port Agilent E8361C 67-GHz network analyzer.

Figs. 5.19 (a) and (b) show the measured gain of $S_{21}$ for the $I$ and $Q$ outputs when $V_{tune}$ (for adjustment of quadrature) is varied from 0 to 3.6 V. The active PPF achieves 2.1- and 1.8-dB gain at 20 GHz and < 0.3-dB gain variations across $V_{tune}$ of 0 to 3.6V. Fig. 5.19 (c) shows 0.1- to 0.3-dB $IQ$ gain difference at 20 GHz across $V_{tune}$ of 0 to 3.6V. Fig. 5.19 (d) shows the phase tuning range of 22.3° at 20 GHz across $V_{tune}$ of 0 to 3.6 V; however, the desired 90° quadrature phase difference is shifted down to lower frequencies of 12 to 18 GHz. This frequency shift is due to an inaccurate parasitic extraction of the different length interconnects of $T_{1-4}$ in Fig. 5.11 (b). The active PPF achieves the $IQ$ phase difference of 83.6° with $V_{tune}$ of 3.6 V at 20 GHz.

Figs. 5.20 (a) and (b) show that the $S_{21}$ gain for both $I$ and $Q$ outputs can be varied to achieve > 20-dB gain adjustment when the control voltages of $V_{C_I}$ and $V_{C_Q}$ vary from 0 to 3.3 V with 1.5-V reference voltage at 20 GHz.

Swept-power measurements are taken with an Agilent E8257D signal generator providing the input and an Agilent N1913A power meter and an Agilent N8488A power sensor for the output. The active PPF generates the output saturated power of > -5 dBm at 15 to 22 GHz, as shown in Figs. 5.21 (a) and (b). The output power difference between the $I$ and $Q$ outputs is less than 1 dB from 15 to 23 GHz in Fig. 5.21 (b). Finally, the active PPF consumes 111.5 mW with 3.3-V supply voltage.
Figure 5.18 Die micrograph of the active PPF. Die size is 0.88 x 0.95 mm².

Figure 5.19 Measured results of the 20-GHz active tunable PPF of (a) the gain response of $S_{21}$ for $I$ output, (b) the gain response of $S_{21}$ for $Q$ output, (c) the $I$ and $Q$ amplitude difference, and (d) the $I$ and $Q$ phase different, when $V_{tune}$ varies from 0 to 3.6V.

5.4.2 80-GHz Balanced Frequency Quadrupler with Output Notch Filter Characterization

The balanced frequency quadrupler with the output second and sixth notch filters were designed and fabricated in GlobalFoundries 0.12-µm SiGe BiCMOS 8HP technology. The process features high-performance NPN transistors with $f_T/f_{MAX}$ of 200/265 GHz, along with 120-nm CMOS and a full suite of passives. Chip micrographs of the balanced frequency quadruplers with/without an input pre-amplifier are shown in Figs. 5.22(a) and (b). The die sizes are 0.94 and 0.84 mm² including
Figure 5.20 Measured results of the 20-GHz active tunable PPF of (a) the gain/phase response of $S_{21}$ for $I$ output, and (b) the gain/phase response of $S_{21}$ for $Q$ output, when $V_{CI}$ and $V_{CQ}$ vary from 0 to 3.3 V with a 1.5-V reference voltage.

Figure 5.21 Measured results of the 20-GHz active tunable PPF of (a) the gain and output power responses versus the input power for both $I$ and $Q$ outputs, and (b) the output power responses and output power difference versus the frequency for both $I$ and $Q$ outputs.

pads. The frequency quadrupler was measured through wafer probing. The input was provided through a 67-GHz Agilent signal generator of E8257D, whereas the output was measured using a Rohde and Schwarz FSW 43-GHz signal source analyzer (with harmonic mixers for 50-110 GHz harmonic measurement). The signal analyzer’s power was calibrated against a power meter with 1.85-mm and WR-10 power sensors to obtain accurate harmonic power readings.

Fig. 5.23 shows the measured fourth harmonic output power, the conversion gain, and the power
efficiency ($\eta$) versus the 4th harmonic output frequency for an input power level of -11 dBm. The efficiency includes the power consumption of both the multiplier core and the preamplifiers. The quadrupler provides $> 0$ dBm output power over 81.2 to 84 GHz, with power efficiency $> 1.2\%$ over this range at 25°C. The peak output power of 2.3 dBm occurs at 82 GHz with the power efficiency of 1.8%. The performance at 125°C is observed at lower frequencies, owing to a downshifting of the resonances in the quadrature generator. The peak output power of -2.7 dBm occurs at 78 GHz with the power efficiency of 0.5% at 125°C. Output power, conversion gain, instantaneous DC power, and power efficiency are plotted versus input power in Fig. 5.24 for 81-GHz output frequencies. The maximum fourth harmonic output power of 2.8/-4.8 dBm at 81 GHz occurs at an input power of -11 dBm, giving 13.8/-6.2-dB conversion gain and 1.9/0.3% power efficiency at 25/125°C.

All harmonics from the 1st through 5th that lie below 110 GHz were measured. The 3rd harmonic is not shown here but the frequency multiplier also achieves good 3rd harmonic suppression. Figs. 5.25(a) and (b), shows the the both odd- and even-order harmonics versus fundamental input frequency with 0 dBm input power at 25°C and at 125°C. Harmonic suppression $> 20$ and $> 40$ dB is obtained at 25°C and at 125°C for all undesired tones over the fundamental input frequency range from 19 to 21 GHz.

### 5.4.3 60-GHz Quadrature Frequency Quadrupler with Passive Tunable PPF Characterization

The circuit is designed and fabricated in IBM 0.1-µm SiGe BiCMOS 9HP technology. The process features NPN transistors with $f_T/f_{MAX}$ of 300/360 GHz, along with 90-nm CMOS and a full suite of passives. The frequency quadrupler was measured through wafer probing. The input was provided through a 67-GHz Agilent signal generator of E8257D, whereas the output was measured using a Rohde and Schwarz FSW 43-GHz signal source analyzer (with harmonic mixers for 50-110 GHz harmonic measurement). The signal analyzer's power was calibrated against a power meter with 1.85 mm and WR-10 power sensors to obtain accurate harmonic power readings. A chip micrograph
Figure 5.22 Die micrograph of the 80-GHz frequency quadrupler (a) with the input pre-amplifier and (b) without the input pre-amplifier.

Figure 5.23 (a) Measured 4\textsuperscript{th} \( P_{\text{out}} \), (b) 4\textsuperscript{th} gain, (c) instantaneous \( P_{\text{DC}} \), and (d) 4\textsuperscript{th} \( \eta \) vs. 4\textsuperscript{th} \( F_{\text{out}} \) with 1\textsuperscript{st} \( P_{\text{in}} \) of -11-dBm at 25\(^{\circ}\)C and 125\(^{\circ}\)C.

of the frequency quadrupler with the passive tunable PPF is shown in Fig. 5.26. The die size is 1.4 mm\(^2\) including pads. The measured DC power of the circuit is 18.4 mW with 3.3-V supply voltage for the quadrupler core and 47.8 mW with 2.5-V supply voltage for the IQ pre-amplifiers.

A sweep of the top and bottom transistor bias conditions was performed to investigate the overall sensitivity to these parameters. Fig. 5.27 shows the 4\textsuperscript{th} harmonic output power and efficiency contours versus external bias control voltages \( V_{BG1} \) and \( V_{BG2} \) for the the bottom and top transistors.
biasing conditions for 54.8-GHz operation. The selected bias condition ($V_{BG1}=1.2V$ and $V_{BG2}=1.8V$) is indicated on the plot and corresponds to class-C operation of the lower device and class-AB operation of the upper device. Automatic amplitude control loops could be used to optimize these bias conditions. If the bottom device is operated in class-AB and the top device is operated in class-C, corresponding to the upper left portion of these curves, lower output power and lower efficiency result.

Fig. 5.28 shows the measured $4^{th}$ harmonic output power, the conversion gain, and the power
efficiency ($\eta$) versus the $4^{th}$ harmonic output frequency for an input power level of -2.9 dBm. The efficiency includes the power consumption of both the multiplier core and the preamplifiers. The quadrupler provides > 7–dBm output power over 48 to 56 GHz, with power efficiency > 3% over this range. The 3-dB bandwidth is 44.8-to-57.2 GHz (24.8%). Better performance is observed at lower frequencies, owing to a downshifting of the resonances in the quadrature generator. Output power, conversion gain, instantaneous DC power, and power efficiency are plotted versus input power in Fig. 5.29 for 50-, 54.8-, and 60-GHz output frequencies. The maximum $4^{th}$ harmonic output power of 8.2 dBm at 50 GHz occurs at an input power of -8.8 dBm, giving 17-dB conversion gain and 4.4% power efficiency.

All harmonic performance, all harmonics from the $1^{st}$ through the $8^{th}$ which lie below 110 GHz were measured. Fig. 5.30(a), shows both the odd- and even-order harmonics versus input power for a 54.8-GHz and 60-GHz $4^{th}$-order output. Harmonic suppression > 25 dB is obtained for all undesired tones over the expected input power range from -5 to 5 dBm. Fig. 5.31(b) shows how the tunable PPF is used to optimize the $2^{nd}$ and $6^{th}$ harmonic suppression for 54.8-GHz and 60-GHz operation.

Figure 5.26 Die micrograph of the 60-GHz frequency quadrupler with the passive tunable PPF. Die size is $1.4 \times 1 \text{ mm}^2$. 
Figure 5.27 (a) Measured $4^{th}$ $P_{out}$ and (b) $4^{th}$ $\eta$ vs. bias control voltages for bottom ($V_{BG1}$) and top ($V_{BG2}$) transistors at the $4^{th}$ $f_{out}$ of 54.8GHz with a $P_{in}$ of 0dBm

Figure 5.28 Measured $4^{th}$ output power ($P_{out}$), gain, and efficiency ($\eta$) of the quadrupler for an input power ($P_{in}$) of -2.9 dBm

5.4.4 80-GHz Quadrature Frequency Quadrupler with Active Tunable PPF Characterization

The frequency quadrupler with the tunable quadrature generator is designed and fabricated in IBM 0.12-µm SiGe BiCMOS 8XP technology. The purpose is to target W-band FMCW radar application. The output frequencies of the frequency quadrupler are designed to be 76 to 81 GHz. The process
features NPN transistors with \( f_T / f_{MAX} \) of 250/300 GHz, along with 120-nm CMOS and a full suite of passives. A chip micrograph of the frequency quadrupler with the active tunable PPF is shown in Fig. 5.32. The die size is 1.4 mm\(^2\) including pads. The frequency quadrupler was measured through wafer probing. The input was provided through a 67-GHz Agilent signal generator of E8257D, whereas the
output was measured using a Rohde and Schwarz FSW 43-GHz signal source analyzer (with harmonic mixers for 50-110 GHz harmonic measurement). The signal analyzer’s power was calibrated against a power meter with 1.85-mm and WR-10 power sensors to obtain accurate harmonic power readings. The measurement setups for the desired 4th-harmonic power and for the other undesired harmonic power are shown in Fig. 5.33.

A sweep of the top and bottom transistor bias conditions was performed to investigate the overall sensitivity to these parameters. Fig. 5.34 shows the 4th harmonic output power and efficiency contours versus external bias control voltages $V_{BG1}$ and $V_{BG2}$ for the the bottom and top transistors biasing conditions for 80-GHz operation. The selected bias condition ($V_{BG1} = 0.4V$ and $V_{BG2} = 1.7V$) is indicated on the plot and corresponds to class-C operation of the lower device and class-AB operation of the upper device. Automatic amplitude control loops could be used to optimize these bias conditions. If the bottom device is operated in class-AB and the top device is operated in class-C, corresponding to the upper left portion of these curves, lower output power and lower efficiency result.

Figure 5.31 Measured harmonic $P_{out}$ at an $f_{in}$ of (a) 13.7 and (b) 15 GHz vs. $V_{tune}$ of the tunable PPF with a $P_{in}$ of 7dBm
Fig. 5.35 (a) shows the measured 4th harmonic output power ($P_{out}$), the conversion gain, and the power efficiency ($\eta$) versus the 4th harmonic output frequency for an input power level of 1.2 dBm at 25°C. Fig. 5.35 (b) also shows the 4th-harmonic $P_{out}$ and 4th-harmonic $\eta$ including the DC power of the quadrupler only at 25, 85, 125°C. The efficiency includes the power consumption of both the multiplier core and the preamplifiers.

The quadrupler provides > 8.2 dBm output power over 75.2 to 82.8 GHz, with power efficiency > 2.4% over this range. The 3-dB bandwidth is 75.6 to 82.8GHz (9.1%). Output power, conversion gain, instantaneous DC power, and power efficiency are plotted versus input power in Fig.5.36 for 78-, 80-, and 82-GHz output frequencies. The maximum 4th harmonic output power of 10.4 dBm at 80 GHz occurs at an input power of 1.2 dBm, giving 9.2-dB conversion gain and 4- % and 5 % power efficiencies with and without including the DC power of the active PPF.

All harmonics from the 1st through the 5th that lie below 110 GHz were measured. The 6th harmonic cannot be measured due to the measurement constraint. Fig. 5.38(a), shows both the odd- and even-order harmonics versus input power for an 80-GHz 4th-order output. Harmonic suppression > 20 dB is obtained for all undesired tones over the expected input power range from -15 to 15 dBm. Fig. 5.38(b) shows how the tunable PPF is used to optimize the 2nd harmonic suppression for 80-GHz operation. Since the quadrature accuracy is shifted to the lower frequencies from 12-18 GHz, the 2nd harmonic suppression versus the tunable voltage $V_{tune}$ is not obvious at a 20-GHz fundamental input signal; however, the 2nd harmonic power decreases as $V_{tune}$ increases to 3.6 V, which matches to the measured results of the active PPF. Finally, the measured DC power of the circuit is 52.8 mW with 4.0-V supply voltage for the quadrupler core and 59.8 mW with 2.5-V supply voltage for the active PPF.

5.4.5 80-GHz Quadrature Frequency Quadrupler with QVCO Characterization

The frequency quadrupler with the QVCO is designed and fabricated in IBM 0.12-µm SiGe BiCMOS 8XP technology. The purpose is to target W-band FMCW radar application. The output frequencies
Figure 5.32 Die micrograph of the 80-GHz frequency quadrupler with the active PPF. Die size is 1.4 x 1 mm².

Figure 5.33 Power- and frequency-swept measurement setup of (a) the desired 4ᵗʰ harmonic output and (b) the undesired low-frequency harmonic outputs for the frequency multiplier of the frequency quadrupler are designed to be 76 to 81 GHz. The 20-GHz QVCO was designed by another PhD student, Weihu Wang, in our group. The process features NPN transistors with $f_T/f_{MAX}$ of 250/300 GHz, along with 120-nm CMOS and a full suite of passives. A chip micrograph of the frequency quadrupler with the QVCO is shown in Fig. 5.39. The die size is 1.4 mm² including pads. The frequency quadrupler was measured through wafer probing. The output was measured using a Rohde and Schwarz FSW 43-GHz signal source analyzer (with harmonic mixers for 50-110 GHz harmonic measurement). The QVCO is biased through the off-chip low-noise regulator and
Figure 5.34 (a) Measured 4\textsuperscript{th} $P_{\text{out}}$ and (b) 4\textsuperscript{th} $\eta$ including DC power of frequency quadrupler only vs. bias control voltages for bottom ($V_{BG1}$) and top ($V_{BG2}$) transistors at 4\textsuperscript{th} $f_{out}$ of 80GHz with a $P_{in}$ of 1.2dBm

Figure 5.35 (a) Measured 4\textsuperscript{th} output power ($P_{\text{out}}$), gain, efficiency ($\eta$) including DC power consumption of both the active PPF and the frequency quadrupler, and $\eta$ including DC power consumption of the quadrupler only for an input power ($P_{in}$) of 1.2 dBm at 25\degree C and (b) measured 4\textsuperscript{th} $P_{\text{out}}$ and 4\textsuperscript{th} $\eta$ at 25, 85, and 125\degree C.

batteries to achieve good phase noise performance.

Fig. 5.40 (a) shows the measured 4\textsuperscript{th} harmonic output power ($P_{\text{out}}$), and the power efficiency($\eta$) versus the 4\textsuperscript{th} harmonic output frequency at 25\degree C. The efficiency includes the power consumption
Figure 5.36 Measured (a) 4\textsuperscript{th} output power ($P_{\text{out}}$), (b) gain, (c) efficiency ($\eta$) with active PPF; and (d) $\eta$ including DC power consumption of the quadrupler only versus an input power ($P_{\text{in}}$) at 4\textsuperscript{th} $f_{\text{out}}$ of 78, 80, and 82 GHz at 25 °C.

Figure 5.37 Measured (a) 4\textsuperscript{th} output power ($P_{\text{out}}$), (b) gain, (c) efficiency ($\eta$) including dc power consumption of both the active PPF and the frequency quadrupler; and (d) $\eta$ including dc power consumption of the quadrupler only versus an input power ($P_{\text{in}}$) at 4\textsuperscript{th} $f_{\text{out}}$ of 80 GHz at 25, 85, and 125 °C.

of the multiplier core, the IQ preamplifiers, and QVCO. Fig. 5.35 (b) also shows the 4\textsuperscript{th}-harmonic $P_{\text{out}}$ and 4\textsuperscript{th}-harmonic $\eta$ including the DC power of the quadrupler only at 25, 85, 125 °C. The quadrupler provides $>8.2\text{dBm}$ output power over 75 to 82.9 GHz, with power efficiency $>3.9\%$ over this range. The 3-dB bandwidth is 75 to 83 GHz (10.1%). The 4\textsuperscript{th}-harmonic phase noise is also measured to show less than $-115 \text{dB/Hz}$ at 75 to 86 GHz with 10 MHz offset as the QVCO tuning voltage $V_{\text{tune}}$ varies from 0 to 3 V in Fig. 5.42 (a). The QVCO is biased at different $R_{\text{DAC}}$ and the base
Figure 5.38 Measured harmonic $P_{\text{out}}$ at an $f_{\text{in}}$ of 20 GHz versus (a) $P_{\text{in}}$ with $V_{\text{tune}}$ of 3.6 V, and (b) $V_{\text{tune}}$ of the tunable PPF with an $P_{\text{in}}$ of 1.2 dBm at 25°C.

Voltage $V_B$ to optimize the phase noise. The minimum phase noise of -126.1 dBC/Hz is achieved at 75 GHz with 10 MHz offset at 25°C. The maximum QVCO gain $K_{\text{VCO}}$ is around 7 Hz/V at $V_{\text{tune}}$ of 1.8 V. Fig. 5.36

All harmonics from the 1st through the 5th that lie below 110 GHz were measured. The 6th harmonic is not able to be measured due to the measurement constraint. Fig. 5.43 shows both the odd- and even-order harmonics versus input power for a 80-GHz $4^{th}$-order output. Harmonic suppression > 15 dB is obtained for all undesired tones over $V_{\text{tune}}$. Fig. 5.38(b) shows how the QVCO is used to optimize the 2nd harmonic suppression for 80-GHz operation. The 2nd harmonic suppression versus the tunable voltage $V_{\text{tune}}$ is excellent due to the differential quadrature signals from the QVCO; however, the 5th harmonic power is dominant at the output due to imperfect cancellation. Finally, the measured instantaneous DC power of the circuit is 211.2 mW with 4.0-V supply voltage for the quadrupler core, 59.4 mW with 2.7-V supply voltage for the $IQ$ preamplifiers and 76.4 mW with 2.7-V supply voltage for the QVCO.
Figure 5.39 Die micrograph of the 80-GHz frequency quadrupler with the QVCO. Die size is 1.4 x 1 mm².

Figure 5.40 (a) Measured 4ᵗʰ $P_{out}$ and 4ᵗʰ $\eta$ vs. 4ᵗʰ $f_{out}$ with a $P_{in}$ of 1.2dBm at 25 °C, and (b) measured 4ᵗʰ $P_{out}$ and 4ᵗʰ $\eta$ including DC power of frequency quadrupler only vs. QVCO tuning voltage $V_{tune}$ with an $P_{in}$ of 1.2dBm at 25, 85, 125 °C.

5.5 Chapter Summary

The key contributions in this chapter are to propose novel architecture of the frequency quadrupler to achieve high suppression of undesired output harmonics with differential quadrature input excitation and investigation of the methods of the desired 4ᵗʰ-harmonic generation with optimum
biasing conditions and the unwanted output harmonic cancellation. A power-efficient V-band frequency quadrupler implemented in GF 8HP, 8XP, and 9HP SiGe BiCMOS has been presented. Compared to the other references, the multiplier operates over V- and W- frequency bands. The V-band frequency multiplier in [YF15] generates >7.4 dBm output power with >22 dB harmonic
suppression. Power efficiency is >5.2% for the multiplier core. The W-band frequency multiplier with differential quadrature excitation generates >11.2/11.5 dBm output power with >30/22 dB harmonic suppression. The power efficiency is >5.8/6.8% for the multiplier core with the active PPF and QVCO. Our performance is benchmarked against recently published quadruplers in Table 5.3, showing that our circuit achieves compelling output power, efficiency, harmonic suppression, and bandwidth performance.
Table 5.3 Reported Performance of Frequency Quadruplers

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<tr>
<th>Reference</th>
<th>DIVATO2</th>
<th>AKMTO1p5</th>
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<th>[Wan12]</th>
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<td>24.8/ (44.8−57.2)</td>
<td>36/ (52−75)</td>
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* Calculated with instantaneous $P_{DC}$ (mW) of buffers.
** Calculated with instantaneous $P_{DC}$ (mW) of both buffers and QVCO.
The 28-GHz frequency band is an attractive candidate for fifth-generation (5G) cellular networks due to favorable channel characteristics and available spectrum. Link budgets for 28-GHz phased-array transceivers suggest single moderate beamforming for user equipment (one to eight elements) and multiple stronger beamforming at the basestation (up to hundreds of elements). As such, fundamental research exploring optimum radio solutions for 5G-mm-wave systems at 28 GHz to achieve wide-bandwidth and highly scalable phased-array architectures is needed. In addition, multi-beam support will be required to service multiple users concurrently for future 5G basestations. To enable scalable, wideband, and multi-beam phased arrays, this Ph.D. works investigates the novel phased-array beamforming architectures in 130-nm SiGe BiCMOS technology for fifth-generation (5G) cellular application.
First of all, my research goals are to explore easily scalable phased-array architectures that have wide RF bandwidth capabilities while supporting multi-band operation and multi-Gb/s data rate communication for future 28-GHz 5G systems. These have the potential to be met through the use of a dual-vector distributed beamformer. A novel dual-vector distributed beamforming architecture has been proposed. The calibration methodology for the proposed dual-vector distributed beamformer was investigated through experimental validation using a circuit prototype. In particular, a 28-GHz four-element dual-vector phased-array receiver has been demonstrated in 130-nm SiGe BiCMOS technology operating from 25 to 35 GHz. The design relies on dual-vector scalar-only weighting functions within each front-end to reduce size to 0.3 mm² per chain and increase fractional bandwidth to 24.5% (26.5 to 33.9 GHz). Each array element achieves 5.1 to 7 dB (5.1 to 8.5 dB) NF, -16.8 to -13.8 dBm (-16.4 to -12.9 dBm) IPdB, and -10.5 to -8.9 dBm (-10.4 to -6.8 dBm) IP3 across 4-bit (5-bit) phase settings. The average gain is 10.5 dB at 29.7 GHz and power consumption is 136 mW per element. Compared to state-of-the-art receiver front-ends, this work achieves among the lowest areas and among the highest fractional bandwidths. As can be expected, active phase shifter topologies will consume more power over passive approaches. While dual-vector distributed beamforming eliminates the quadrature coupler from each front end, this area savings may be negated by the increased area in a dual parallel power combiner. This issue is addressed in the following chapter, where I investigate dual series-combiner structure for DVDBs and evaluate for both receiver and transmitter arrays. This work has been published in [Yeh16; Yeh17a].

In addition, the 28-GHz four-element phased-array transceiver using dual-series-fed t-line networks has been demonstrated in 130-nm SiGe BiCMOS technology for potential 5G cellular network application. My research efforts in this work have focused on improving the bandwidth of a transceiver for achieving multi-band operation and high data rate performance. The series-fed network is implemented and shared between both the TX and RX front-ends without the use of T/R switches to reduce array size. The series-fed network also reduces the size of the TRX front-end and the power combining/splitting networks for enabling large and scalable sub-arrays. In addition,
the phase/gain offsets between each TX and RX element can be calibrated out within the desired
frequency range. Measurements show that each receive front-end achieves 8.7 to 11.5 dB gain,
4.5 to 6.9 dB noise figure, -25.4 to -18.4 dBm input 1-dB compression point, and < 0.5-dB/2.1°
RMS gain/phase error at 24 to 28 GHz. Each transmit front end achieves 9.4 to 14.3 dB gain, 5.5
to 10.6 dBm output 1-dB compression point, and < 0.4-dB/4.2° RMS gain/phase error at 24 to 28
GHz. The four-element transceiver array occupies 2.9 mm² area and consumes 1.08 W in transmit
mode and 0.68 W in receive mode. Compared to the state-of-the-art TRX front-end, our distributed
beamformer achieves the lowest front-end area and array area with comparable RF performances
at Ka band; however, the DC power is higher than the passive switched-LC approaches. This work
has been published in [Yeh17b].

Furthermore, the 28-GHz hybrid phased-array transceiver using mixer-based distributed beam-
forming has been demonstrated in 130-nm SiGe BiCMOS technology for potential 5G cellular
network application. The key contributions in this works are (1) the mixer-based approach is used
for global interpolation with broadband quadrature LO, (2) a novel distributed poly-phase filter is
developed for the wideband tunable quadrature generation, and (3) a built-in self-test network is
implemented in the array to enable COMET built-in self-test measurement. The benefits of using
this architecture are wide bandwidth performance with much smaller and compact area. The ca-
pabilities of switched image beam selection for the RX array and the sideband selection for the TX
can be achieved in the array. Each receive front-end achieves 8.6 gain at 29.8 GHz, a 24.5% 3-dB
bandwidth (25.2-32.5 GHz), and < 0.1-dB/0.8° RMS gain/phase error at 28 GHz. Each transmit
front-end achieves 18.1 dB at 29.9 GHz, a 24% 3-dB bandwidth (25.6 to 32.8 GHz), and < 1-dB/5.6°
RMS gain/phase error at 14.1-35.4 GHz.

Finally, a novel topology of the frequency quadrupler has been proposed and built to achieve
high undesired output harmonic suppression with differential quadrature input excitation, and
the methods of the desired 4^{th}-harmonic generation with optimum biasing conditions and the
unwanted output harmonic cancellation have been investigated. Power-efficient V- and W-band
frequency quadruplers are implemented in GF 8HP, 8XP, and 9HP SiGe BiCMOS. The V-band frequency multiplier generates >7.4dBm output power with >22-dB harmonic suppression. The power efficiency is >5.2% for the multiplier core. The W-band frequency multiplier with differential quadrature excitation generates >11.2/11.5 dBm output power with >30/22 dB harmonic suppression. Power efficiency is >5.8/6.8% for the multiplier core with the active PPF and with the QVCO. Our performance is benchmarked against recently published quadruplers, showing that our circuit achieves compelling output power, efficiency, harmonic suppression, and bandwidth performance. This work has been published in [YF15].
BIBLIOGRAPHY


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A.1 40-GHz Static Frequency Divider

In-phase and quadrature-phase signals could also be generated using a static frequency divider driven at twice the desired frequency. Note that this tends to somewhat defeat the purpose of using a multiplier; however, the results are included here for completeness.

Fig. A.1 (a) shows a block diagram of a divided-by-two (2:1) frequency divider employing current-mode logic (CML). The static 2:1 divider, shown in Figs. A.1 (a) and (c), consists of two CML D-latches in a master-slave configuration [RZ04; Wur00]. Cascading two level-sensitive D-latches in a master-slave configuration results in an edge-triggered D-flip-flop (DFF). Connecting the outputs of a DFF back to its inputs with inverted phase results in a toggle flip-flop. The static 2:1 divider can operate
in one of two modes. The first mode is the latching mode, while the second is an injection-locked mode. The latching mode occurs when the input clock signals of $CLK$ and $CLK_b$ have large enough voltage swings. The injection locking mode of operation occurs when no input clock signals are present or the signal swings are very small, approximately equal at the common-mode value. For LO quadrature generation, the differential VCO can generate large enough output swings to drive the inputs of the divider. Thus, the divider should be operating at the latching mode. Here, $Q_{5,6,20,21}$ act as an evaluation state when the D-latch is transparent, and the regenerative pair $Q_{7,8,22,23}$ acts as a hold stage when the latch is opaque. Fig. A.1 (b) shows the timing operation for the 2:1 divider. For $CLK=$high during the timing $t_{0-1}$, the master latch is transparent and the slave latch is opaque. Thus, $I$ and $I_b$ take the values of $Q_b=$high and $Q=$low through the master latch but $Q$ and $Q_b$ remain the same at the slave latch when $I=$high and $I_b=$low vary. For the $CLK=$low during the timing $t_{1-2}$, the master is opaque and the slave is transparent. Thus, $I=$high and $I_b=$low are passing to $Q$ and $Q_b$ through the slave latch, but $I$ and $I_b$ remain the same at the master latch when $Q_b=$low and $Q=$high vary. For the $CLK=$high during the timing $t_{2-3}$, $I$ and $I_b$ take the values of $Q_b=$low and $Q=$high through the master latch but $Q$ and $Q_b$ remain the same at the slave latch when $I=$low and $I_b=$high vary. For the $CLK=$low during the timing $t_{3-4}$, $I=$low and $I_b=$high are passing to $Q$ and $Q_b$ through the slave latch, but $I$ and $I_b$ remains the same at the master latch when $Q_b=$high and $Q=$low vary. Thus, for every clock cycle $T$, the output is toggled, resulting in a divide-by-two operation. Also, the outputs of $I$ and $Q$ at the divide-by-two frequency achieve 90° phase difference, which has very wideband quadrature accuracy.

The second mode of operation for the static 2:1 divider is the injection locking mode, when no input clock signals are present or the signal swings are very small, approximately equal at the common-mode value. Thus, both the master and slave D-latches are semi-transparent, allowing signals to propagate through both latches. The 2:1 divider can act as a two-stage ring oscillator with the phase-inverted feedback loop. Consider the case when $CLK$ and $CLK_b$ are held at a constant and equal value. The tail currents from $Q_{13}$ and $Q_{28}$ are equally split into $Q_{3,4}$ and $Q_{18,19}$. Cross-
coupled transistors $Q_{7-10}$ and $Q_{22-25}$ can be represented as negative resistances. The loop gain of the divider can be calculated in the phase-inverted feedback loop. For oscillation to begin, the phase of T should be $360^\circ$ and the loop gain should be greater than 1 for the Barkhausen criterion. For this ring oscillator, the propagation is delayed or the oscillation frequency is determined by charging and discharging the RC loads with the total tail currents from $Q_{13}$ and $Q_{28}$. The frequency locking range of the divider can be determined by reducing the input signal level across the frequencies. The term of the input sensitivity of the divider can be defined such that the minimum input clock signal level for the divider to operate is between the latching mode and the injection lock mode. The input sensitivity of the divider will be shown in the measurement section later. The benefit of using the 2:1 static divider is the extreme wideband quadrature accuracy but it requires twice the input frequency and consumes considerable DC power.

**A.1.1 40-GHz Static Frequency Divider Characterization**

The divider circuits are designed and fabricated in GlobalFoundries 0.12-$\mu$m SiGe BiCMOS 8HP technology. The process features high-performance NPN transistors with $f_T/f_{MAX}$ of 200/265 GHz, along with 120-nm CMOS and a full suite of passives. The 16:1 static frequency divider of the cascading four-stage 2:1 frequency divider shown in in Fig. A.2(a) was measured through wafer probing when one of the differential outputs of the divider is terminated with a 50-Ω resistor. The input was provided through a 67-GHz Agilent signal generator, whereas the output was measured using a Rohde and Schwarz FSW 43-GHz signal source analyzer. Chip micrographs of the the 16:1 frequency divider with/without an input LC balun are shown in Figs. A.2(b) and (c). The die size is 0.63 mm$^2$ including pads.

Fig. A.3(a) shows the measured input sensitivity versus the input frequencies at 25°C to 125°C. The input sensitivity is measured by reducing the input power level until the first stage of the 16:1 divider is operating in the injection locking mode. Fig. A.3(a) shows the locking range of the divider is from 5 to 49 GHz and from 11 to 42 GHz with the input power of > 0 dBm at 25°C and 125°C. The
Figure A.1 (a) Block diagram, (b) timing diagram, and (c) schematic of the divided-by-two (2:1) static frequency divider.

16:1 divider achieves a self-oscillation frequency of 38.2 to 44.1 GHz without the input signal with 3 to 3.6-V supply voltages and at 25°C to 125°C in Fig. A.3(b). The maximum input frequency of the 16:1 divider is from 42.7 to 50.3 GHz with 3 to 3.6-V supply voltages and at 25°C to 125°C, as shown in Fig. A.3(c). Finally, the measured DC power of the 16:1 divider is 124 mW and 170 mW with 3.3-V supply voltage at 25°C and 125°C.
Figure A.2 (a) Block diagram of the divide-by-16 (16:1) static frequency divider and die micrographs of (b) the 16:1 frequency divider with an input LC balun, and (c) the 16:1 frequency divider without an input LC balun.

Figure A.3 Measured results of the 16:1 frequency divider with an input balun for (a) the input sensitivity versus input frequencies, (b) the self-oscillation frequency $F_{OSC}$, (c) the maximum input frequency $F_{MAX}$, and (d) the total DC power consumption versus supply voltages at 25°C, 60°C, 90°C, and 125°C.
APPENDIX

B

RING-TYPE LC QUADRATURE VOLTAGE CONTROLLED OSCILLATOR

Work reported in this section was conducted by Weihu Wang as part of his dissertation research.

B.1 Quadrature Voltage Controlled Oscillator Topology

As requested by the frequency quadrupler, quadrature VCOs can generate quadrature signals with a 3dB phase noise benefit compared to their differential counterparts, due to the injection lock of two differential resonators. Using injection of numerous phases, this 3dB phase noise benefit can be superimposed for exceptional phase noise with a trade-off of power consumption, especially
for an advanced technology node featuring lower breakdown voltages. Unfortunately, the noise benefit in practice may be less than 3dB if active injection is used involving transistors, because the injecting transistors themselves introduce additional loss and phase inaccuracy. A better method is to use passive injection in the form of transformers, diodes, transistor bulk or with harmonic injection. These are high-order resonators that sometimes make the VCO designs more complicated if combined with other techniques. Thus we proposed a capacitive injection mechanism featuring an improved transconductance, resulting in a ring-type LC resonator as shown in Fig. B.1.

The LC tank in each branch is connected to the in-phase collector, and is also coupled to the quadrature emitter through a feedback capacitor $C_1$, forming a ring-type structure. Differential inductors are used across the out-of-phase branches, thus ensuring the correct phase relations for a unique oscillation mode. The resonant frequency of this tank is in the form of

$$\omega_0 = \frac{1}{\sqrt{L(C_{var} + C_{fix})}}. \quad (B.1)$$

Clearly, a smaller feedback capacitor $C_1$ is beneficial not only for tuning range but also for reducing the extra loading to the LC tank from the bias network. In this study, we will first observe its transconductance and $C_{fix}$ using small-signal analysis and then evaluate its phase noise performance using large-signal analysis.

**B.2 Ring-Type LC Quadrature Voltage Controlled Oscillator Implementation**

To demonstrate its operation and phase noise, a ring-type LC quadrature VCO prototype is built in 20 GHz range in GlobalFoundries 8XP 130-nm SiGe BiCMOS Technologies. The technology offers high-frequency, low-current heterojunction bipolar transistor (HBT), a high-Q accumulation-mode MOS varactor, as well as an aluminum alloy, which are suitable for achieving low phase noise and
high power efficiency in VCO. The complete schematic of the quadrature VCO is shown in Fig. B.2, where design details are illustrated for the passive and active devices. The passive devices include two identical low-loss transformers and engineered varactor banks aimed at consistent Q across the wide tuning range coverage. The active devices include the transistors and feedback capacitor network and the adjustable biasing network.

**B.2.1 AC-shorted Transformer**

An AC-shorted transformer LC tank introduced in [Wan14; Fuj17] is utilized here to expand the continuous tuning range of the VCO and make it suitable for FMCW radars. The differential transformers are built in adjacent top aluminum levels with 4 $\mu$m and 1.4 $\mu$m thickness each, and the gap between those two levels is 4 $\mu$m. The transformer is analyzed using a Momentum 3D Planar EM Simulator. In the area beneath the transformer, deep trench isolation is planted in row and column shapes to reduce the eddy current induced within the surface of the substrate, and the lowest copper level “$M_1$” is drawn with shredded shielding shape to control the parasitic coupling. As an initial trial, a rough size of a 200 pH octagon inductor is used to find the optimum width for an inductor occupying a single metal level. This practice is repeated for both inductor windings, and the width is found to be 20 $\mu$m for the topmost level winding $L_1$ and 30 $\mu$m for the second top level $L_2$. After
that, the two individual inductor windings are stacked together to increase their mutual coupling, which is to improve the Q of the equivalent inductor if they were AC-shorted on the edges. The make them AC-shorted, high-Q Metal-Insulator-Metal (MIM) capacitors \( C_{big} \) are sized with a large length-to-width ratio and placed such that the distance from the transformer edges to the transistor node is shortened. Also, the MOS varactor banks can be placed underneath the AC-shorted MIM capacitors given that enough margin is reserved for parasitic capacitance. Later on when the active circuit is completed, the transformer outer dimension is stretched while keeping the winding widths constant to obtain the correct oscillation frequency.

### B.2.2 Constant-Q Varactor Tank

The problematic variation of phase noise within the wide tuning range of a VCO is addressed as due to the differences in tank Q as well as the oscillating frequency. For bipolar VCOs, the unequal oscillation amplitude within each band causes a bias current sweet spot that is unfortunately dependent on the tuning voltage or oscillation frequency, thus making it difficult to control the bias in real time. In this study, an equalizing topology is utilized to make the oscillation swing consistent with tuning range. However, we need to clarify what causes phase noise inconsistency over tuning range before we can give a solution. The possible choices includes the inconsistency caused by the varying passive Q, varying oscillation voltage, varying bias current, and varying signal power level.

To answer this, we first notice that the phase noise can be due to different causes. If other noise sources have been well controlled, and at the top of the remaining noise list is the inherent noise due to an undesired forward bias of the base-collection junction, then we need to restrain the situation when the swing amplitude is too large. This has to be done in a way to avoid introducing more noise sources into the VCO and avoid reducing passive Q. The first option is to use an extra clamp diode to restrain the extra noise amplitude, which introduces extra noise. The second option is to adjust the bias current in real time to maintain the same oscillation amplitude at the presence of the changing passive impedance, but this approach requires a low-noise op-amp to be used. The third option is
to maintain the same parallel tank resistance such that it only requires a constant bias current to maintain the oscillation amplitude. This requires us to design a constant parallel tank resistance of $R_p$ across tuning range.

The varactor bank is an essential part of the LC tank via coupling through the AC-shorted capacitors and the magnetic coupling. The main varactor $C_{var}$ is implemented as a thick-oxide n-type MOS capacitor (double-gate, DGNCAP) and contributes about 90% of the total varactor capacitance. The DGNCAP is used as the main varactor because it has a higher Q than the regular thin-oxide MOS capacitor (NCAP). Its drain-source connection is directed towards the center such that the parasitic capacitance between the drain-source and the substrate is not placed in parallel to the varactor. The DGNCAP has a large tuning capacitance to provide continuous tuning range for FMCW operation, but the drawback is an excessive change of oscillation amplitude at different location of the tuning range. This is bad because an extra large amplitude causes forward bias of the HBT base-collector junction, leading to phase noise deterioration. To deal with this, the amplitude is decreased at the higher-Q end of the tuning range of the main varactor by placing a low-Q NCAP and resistor pair in parallel with the main varactor. With respect to the main DGNCAP varactor, the NCAP is connected in reverse, such that it effectively lowers the Q when the main varactor is high and avoids reducing the Q when the main varactor is low. Two such reversely connected NCAP are placed in series to match the breakdown voltage of the main DGNCAP, and parallel resistors are also used to ensure the oscillation voltage drop on each NCAP is equal. The result of this experiment is not ideal by using sophisticated varactor banks. In simulation, the oscillation amplitude is equalized after adding the reversely connected NCAP varactors, but the optimum bias current is still not consistent for each point on the tuning range. On the higher oscillation frequency, a lower amplitude is required to obtain the lowest phase noise, whereas higher oscillation amplitude is required on the lower end. To obtain the effect of consistent phase noise instead of amplitude, more reversely connected NCAP varactors are needed and the entire tuning range is reduced.
B.2.3 QVCO Active Core Optimization

To obtain stable operation, the feedback capacitor $C_1$ is chosen to ensure start-up on the low frequency end, where varactor Q is high, and the capacitor size is increased by a margin. The interconnect from the feedback capacitor $C_1$ to the collector and emitter needs some attention, as the geometric distance between the collector and emitter of neighboring branches is long to cope for the required space of the biasing circuit. Since for $C_1$ we are using MIM capacitors on the top metal levels, the interconnect is also implemented on these top metal levels, and their length is kept the same. The symmetry of layout results in relatively good phase accuracy, which allows the subsequent frequency quadrupler stage to produce high output power.

The phase noise of QVCO has a significant contribution from the base resistance. To suppress this contribution, bypass capacitors are added at each base node, and the transistor length can be increased at the 20 GHz frequency range, depending on the requirement of the fixed capacitance size. The output of the oscillation is taken from the collectors close to the transformer edges that are close to the center to keep the length of the interconnect nearly the same.

The biasing of the QVCO core is achieved using a fixed voltage on the base and the tail resistance degeneration to adjust the bias current. The voltage bias at the base node can be implemented with very low noise. The degeneration resistors are controlled by MOSFET switches, and the resistors are sized such that the bias current follows binary code to save the number of bits. Both the resistors and MOSFET switches have large width and length to suppress flicker noise. For on-wafer measurement, all of these bias and supply voltages are fed from external regulated power supplies, and the degeneration resistors are controlled by shift registers such that only one extra pad is needed.
Figure B.2 Detailed schematic of the Ring-Type LC QVCO.