ABSTRACT

ZHOU, QIANLAI. 7.2 kV Solid State Transformer Based on 15 kV SiC MOSFETs and A Novel Single Stage AC-AC Converter. (Under the direction of Dr. Alex Q. Huang.)

Solid state transformer (SST) is considered an emerging and disruptive power electronics technology for medium voltage (MV) (2 kV-35 kV) applications including smart distribution system, traction transformer, ship power and renewable energy. SST concept is proposed that aims to replace conventional line frequency transformer (LFT), providing many advanced features such as VAR compensation, voltage regulation, fault isolation, and DC connectivity. However, many challenges related to high voltage stress, efficiency, reliability, protection and insulation must be addressed before the technology is ready for deployment.

Three-stage SST with ac-dc-dc-ac scheme is the most widely studied and adopted approach since it can achieve most of the smart features and owns best control flexibility. However, the major disadvantage of this scheme is reduced efficiency due to multiple stages of power conversion. In addition, complex circuit and control configurations limit the system power density. Direct AC-AC converter, named as direct AC-AC transformer (DACX), with one stage of power conversion is desirable in MV applications where higher efficiency is preferred and only limited smart features are needed. In general, two major technical challenges in MV direct AC-AC converter needs to be addressed: (1) wide voltage range leads to a much more complex ZVS circumstance, (2) requirement in capacitance reduction to reduce unwanted reactive power and MV capacitor’s size/weight.

A novel current fed series resonant converter (CFSRC) is proposed for the first time that can address many technical challenges in DACX applications. (1) It helps MV MOSFETs achieve ZVS operation under wide input voltage and load range. Thus, higher switching frequency can be achieved. (2) This topology helps minimize system total required
capacitance, which helps improve system power density and reduce unwanted reactive power. Theoretical time domain analysis and fundamental harmonic approximation (FHA) are conducted, providing design equations for switching frequency selection.

The 15 kV SiC MOSFETs developed by Wolfspeed enable simple and robust two-level DACX where the peak voltage stress is less than 12 kV. Chapter 3 revisited the characterizations of 15 kV SiC MOSFETs including switching loss, $R_{on}$, thermal, output charge and package. ZVS design of 15 kV SiC MOSFET is studied and analyzed under wide input voltage condition (0 to 10 kV). Constant deadtime strategy is proposed, with which ZVS can be realized at most of high voltage range. Partial discharge occurs when input voltage is low. However, only neglectable associate switching loss will be generated if deadtime and $L_m$ are properly designed. Detailed analysis of ZVS behavior under wide range of voltage conditions and detailed calculation of associated loss from partial ZVS are presented. System parameters including $L_m$ and $t_{\text{dead}}$ are optimized based on tradeoff between turn on loss and conduction loss.

Resonant capacitors are distributed on both sides of the transformer to minimize number of MV MF SiC MOSFETs. Inherent cycle by cycle current-limit capability is achieved by paralleling diodes on low voltage (LV) resonant capacitors. The theoretical analysis and design of DACX under overload and short circuit conditions are conducted. Equation for peak current calculation under short circuit is also provided. The calculation results show that the peak current is a function of the input voltage, resonant inductance and primary resonant capacitance. With proper design of the resonant tank, the expected peak MV MOSFETs current under 7.2 kV short circuit will be less than 40 A.
A full-scale and compact SSTs that converts 7.2 kV AC to 240 V AC is developed and tested from 600 kW to 12 kW. ZVS operation of the MV MOSFETs is verified from light load to heavy load. This is the highest reported voltage rating for two-level based power converters without device series connection. The developed SST has achieved a peak efficiency of 97.8%, which is a significant improvement from previously developed three stage SSTs. 15 kV MOSFET is utilized to reach its full voltage, frequency and power potential of 10 kV, 100 kHz and 20 kW, respectively, in DACX applications. Short circuit is conducted under 3 kV peak input voltage condition. The peak current of MV MOSFETs under this test is 13 A, which is consistent with theoretical analysis.
7.2 kV Solid State Transformer Based on 15 kV SiC MOSFETs and A Novel Single Stage AC-AC Converter

by
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To my parents

Yingqi Zhu and Xiaoling Wang
BIOGRAPHY

Qianlai Zhu was born in Wenzhou, China, in 1988. He received the B.S. degree in electrical engineering from Zhejiang University, Hangzhou, China, in 2010. From 2010 to 2013, he was an Electrical Engineer with the Delta Electronics Co., Shanghai China, where he was engaged in design and implementation of server power supply and automotive onboard charger. Currently he is pursuing the Ph.D. degree in the Department of Electronic and Electrical Engineering at the North Carolina State University. His research interests include Solid State Transformer design and implementation; AC-DC converter, DC-DC converter and direct AC-AC converter design.
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I would like to express my sincere thanks to my advisor, Dr. Alex Q. Huang, for his patience with me. Thank him for his mentorship, encouragement and support during the past five years here at FREEDM system center, NC state university. I especially appreciate and respect Dr. Huang for his broad vision and insight understanding of technology, as well as his greatly personalities.

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Chapter 1. Introduction

1.1 Introduction to Solid State Transformer Concept

In recent years, there has been a growing interest in replacing the traditional bulky low frequency (LF) transformers (LFT) with solid state transformer (SST) in medium voltage (MV) (2 kV-35 kV) applications. Due to its benefits in size and weight reductions, as well as a number of smart functionalities, SST concept is increasingly investigated and implemented in many applications such as smart grid, traction drive and renewable energy systems shown in Figure 1-1 [1]-[4]. SSTs play crucial role to connect different loads, AC or DC systems and offer galvanic isolation, voltage regulation and fault current limitation.

![Figure 1-1 SSTs application Areas](image_url)
Magnetic transformer’s area product is inversely proportional to its operation frequency. Increasing frequency enables significant reduction in transformer volume and weight. The basic idea is use semiconductor power devices to generate medium frequency (MF) (several kHz to tens of kHz) voltages, step up/down them through MF transformer, and reshape them back to LF voltages. To accomplish this, semiconductor devices, gate drivers, inductors, capacitors and control system are needed to form a compact system. With the help of power electronics technology, many attractive features that is not available in LFTs, including VAR compensations, voltage regulation, fault isolation and DC link, can be realized in SSTs [1]-[4].

Power electronics technology has been well established in low voltage (LV) applications with voltage that is less than 1 kV. However, the application of this technology in MV applications is still far from mature and many challenges need to be solved before commercializing this new concept. Current researches mainly focus on semiconductor device, topology and control design.

1.2 Literature Review

Different power conversion topologies and applications of SST family have been implemented and presented [1]-[12]. The primary research targets are to achieve high efficiency, reliability, functionality and power density, while maintain low cost.

Many well-known MV SST designs are depict in Figure 1-2, including designs by Alstom [5], Bombardier [6], UNIFLEX [7], ABB PETT [8], EPRI [9], GE Global Research [10], ETH [11] and the FREEDM system center [12]-[14].
Figure 1-2 MV prototypes with key parameters by leading research groups

Table 1-1 Summary of Previous Developed Prototypes

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The qualitative comparison for medium voltage prototypes are summarized in Table 1-1. The table shows that these developed prototypes offers attractive features such as Var compensation, fault isolation and so on.

On the other hand, these accomplished works still cannot match conventional LFT in performance of efficiency, cost and life time performance at current stage.

1.2.1 Topology State of the Art

So far, the literatures on SST design show a variety of technical approaches. Five different power conversion topologies of the SST family have been implemented and presented in MV applications as depicted in Figure 1-3 [6]-[15].

Type D is the most widely studied and adopted approach since it can achieve most of the smart features such as VAR compensation, voltage regulation, fault isolation, and DC connectivity [3]. However, the major drawbacks of Type D are reduced efficiency due to multiple stages power conversion and reduced reliability due to complex hardware configuration and control [7], [15]. Furthermore, previous research has shown that the input AC-DC stage normally operates under hard switching condition, the switching frequency is greatly limited by huge amount of switching loss, which in turn limits the power density. Current built SSTs based on this topology report overall system efficiency lower than 95%.

Types B and C are topologies that adopt two-stage configurations, which can achieve higher efficiency compared to Type D due to one less stage of power conversion. However, DC voltage needs to be generated inside the system, which create some obstacles in design. The isolated stages in Type B needs to have wide input voltage ZVS capability and wide
voltage gain capability [16], [17], which requires complex control and PWM modulation. In Type C topology, MV AC-DC stage still exists, which greatly limits the switching frequency and efficiency performance. The isolated DC-AC stage also requires specific control or PWM modulation to realize soft switching and wide voltage gain [18], [19].

Type E is proposed in paper [20] and is named as isolated front end (IFE) approach. Which is suitable for MV AC to LV DC power supply applications. The first stage directly converts MV AC voltage to LV half sinusoidal voltage. This stage is designed at an optimized point to achieve high efficiency and simple control configuration. The grid current power factor correction and output voltage regulation is carried out by a second, non isolated conversion stage on the LV side.

Type A topology, named as direct AC-AC transformer (DACX) in this dissertation, is an attractive approach since only one stage of power conversion is needed. This approach directly converts MV AC voltage to LV ac voltage without converting to DC voltage. There are two types of Type A topologies. Type A-1 use four-quadrant switches on both sides of the transformer to directly converting power. Type A-2 is actually an extension of Type A-1, in which bidirectional AC voltage is rectified and unfolded by input and output LF unfolding bridges. The HF stage of Type A-2 only sees unidirectional voltage, thus simple switches can be used and HF switches numbers can be reduced to half. The system configuration of Type A is much simplified and MV MF power devices numbers is also minimized compared to previous topologies, which potentially enables better efficiency, higher reliability and is more cost effective.
Although several studies have indicated that Type A topology offers best efficiency performance, little attention has given to this topology in MV applications due to its lacking functionalities and design challenges.

### 1.2.2 Modular and Two-level Approach

The most popular distribution voltage in the United States is the 15 kV class and the most common 15 kV voltage is 12.47 kV, which has a phase voltage of 7.2 kV. One grand challenge for the SST is to achieve MV input voltage such as 7.2 kVac in single phase smart grid

![Topology classification](image)
application. No commercial power devices are currently available to handle the associated peak voltage stress.

Modular multilevel configurations are widely used to address this issue in which low voltage converters or devices are connected in series to share the voltage and power [5]-[13].

Modular approach solves the voltage or current stress problems, especially enables low voltage devices to accomplish power conversion in medium voltage applications. However, it also brings many problems. For example, to avoid power and voltage balancing problems, additional balancing circuits and control strategies are needed [15]. Furthermore, the resulting SST is typically very complex due to the complex system configuration and control schemes, numerous gate drivers and isolated power supplies. System reliability is low if redundancy is not carefully considered.

Due to the significantly increased bandgap and peak electric field stress, new MV power devices based on SiC material with significant higher voltage rating, such as the 15 kV SiC MOSFETs and 15 kV SiC IGBT, have been developed and demonstrated [21]-[27]. They can enable simple and robust two-level SST in 7.2 kV applications where the peak voltage stress is less than 12 kV. Compared to IGBT, the SiC MOSFET shows a much lower switching loss. This overall lower switching loss and ZVS capability enables higher switching frequency in MV converters, leading to smaller system volume and higher power density. SST based on high voltage SiC power devices is therefore a very attractive technical approach. With two-level configuration, the system complexity and control scheme will be simplified.
The 15 kV SiC MOSFET developed by Cree allows simple and robust two level SST in 7.2 kV applications where the peak voltage stress is less than 12 kV. But research on this devices in continuous MV operation is still not enough.

1.3 Research Scope and Objectives

Based on previous statements, a two level, Direct AC-AC converter, offers perhaps the best performance in efficiency and reliability. The target of this dissertation is to design and implement a two level DACX based on the 15 kV SiC MOSFETs, achieving good performance in terms of efficiency, switching frequency and functionality.

Although many researches have been done on type A SSTs, there are still many areas needs more researches and improvement. Several practical challenges arise when introduce two level Type A topology into MV applications.

Topology investigation: Zero voltage switching (ZVS) is the key to achieve high switching frequency. Hard switching in MV applications will significantly limit the switching frequency due to the energy loss from device’s output charge [28]. It is crucial to select a proper topology that helps realize ZVS in MV DACX applications. In direct AC-AC converter, the input voltage varies from zero to peak AC voltage every LF cycle. The changing of device voltage stress, together with the nonlinear output charge of MOSFET, make it difficult to achieve ZVS operation. In addition, capacitance in the direct AC-AC converter will result in unwanted reactive power, which will affect the power factor. On the other hand, film capacitors are preferred in MV applications for their longer lifetime, higher ripple current capability, non-polarized and higher voltage rating comparing to electrolytic capacitors. However, the low
energy density of film capacitors normally results in large volume. The high voltage insulation also leads to larger volume and weight, which limits the system power density. There is a strong desire for a topology that can help reduce required system capacitance.

15 kV SiC MOSFET investigation and utilization: Previous studies have characterized this device thoroughly and have proven the voltage blocking capability of this device up to 12 kV [22]. However, the achieved continuous operation of this device is still lower than 6 kV [14], and the highest achieved switching frequency is 40 kHz with ZVS operation [14]. The main challenges in reaching higher operation voltage include ZVS operation range, poor and/or unproven reliability of the prototype device and its associated package. Much better auxiliary circuits such as driving circuit and auxiliary power supplies must also be designed to handle the high isolation voltage as well as high common mode voltage range. More research works need to be done to utilize this device to its full voltage, frequency and power potential. Furthermore, in direct AC-AC applications, designers must also face a new and significant challenge in realizing ZVS over a wide input voltage range (from 0 V-10 kV). More investigation and researches are required to properly implement this device in MV DACX applications.

Current limit capability investigation: The ability to protect the power system from load disturbances is another function that distinguishes SSTs from the conventional low frequency transformer. Fault current limiting capability is a very desired property in MV applications. It is important to design and investigate the current limiting capability of DACX when overload happens.
The primary objective of this research work is to design and implement a two level direct AC-AC SST for 7.2 kV application with high efficiency performance and power density. This dissertation offers comprehensive design guidelines for MV DACX design in terms of topology investigation, ZVS design and current limiting design. Offering guidelines for studying and utilizing SiC MOSFETs devices to its full switching frequency, voltage and power potential in MV DACX.

1.4 Dissertation Outline

This dissertation is organized into 6 chapters.

Chapter 2 proposed a novel current fed series resonant converter (CFSRC) for direct AC-AC applications, which not only able to achieve ZVS operation across wide input voltage and load range, but also minimize the total capacitance required in the system. The detailed theoretical analysis and operation principle of proposed circuit are conducted based on time domain analysis and fundamental harmonic approximation (FHA). Equations on current zero crossing, gain property are provided for design reference.

Chapter 3 first revisits the 15 kV SiC MOSFET’s characteristics. Providing comprehensive design guidelines on utilizing the device to its full switching frequency and power potential in MV DACX in terms of ZVS implementation, loss optimization, thermal management and device utilization

Chapter 4 is devoted to the analysis and design of the proposed circuit under over load conditions and short circuit condition. Design equation for peak current under short circuit is carried out to guide resonant tank parameter design.
Chapter 5 elaborated the system hardware development. Experiments for steady state operation are conducted under 7.2 kV conditions to verify the circuit operation principle. Test result under light load and heavy load conducted to verify ZVS operation. Short circuit is conducted at 3 kV peak voltage to verify the overload current limiting capability.

Chapter 6 summarizes the whole dissertation and give comments on the future work.
Chapter 2. Current Fed Series Resonant Converter for Direct AC-AC Application

2.1 Introduction of Direct AC-AC Converter

The most adopted type D SSTs offers many functionalities such as Var compensation on the input side or a 400V DC port for other purpose connection. However, three stages of power conversion limits its efficiency performance. Direct AC-AC converter only has one stage of power conversion, which is desirable in MV applications where higher efficiency is preferred and full smart features are not needed.

![Figure 2-1 Direct AC-AC Operating Principle](image)

Direct AC-AC converter with galvanic isolation is first proposed by William McMurray in 1970. Detail circuit is shown in Figure 2-1, in which four-quadrant thyristors are used to develop
an electronic transformer [29]. Low frequency input AC voltage is directly chopped into high frequency waveform with semiconductor devices. A high frequency transformer then converts this high frequency waveform to the secondary side. Semiconductor devices on the secondary side will reshape the high frequency waveform back into low frequency AC voltage. Four quadrant switches are used, operating in complementary mode with 50% duty-cycle in this application. This topology can be recognized as hard switching dual active bridge circuit. Power and voltage is controlled based on the phase shift between primary bridge and secondary bridge. All devices in this topology operate under hard switching conditions.

In direct AC-AC configurations, ac voltage is directly processed into high frequency voltage, so there is no need of DC capacitors in the system. The control and design of the high frequency isolation stage is critical. The overall system configuration is very simple, which contributes to better reliability. Single stage of power conversion also leads to higher efficiency.

In recent years, many works have been done to introduce direct AC-AC converter into MV applications, most of which are designed based on modular structure. These research works mainly focus on topology and control design. To the author’s best knowledge, none of previous finished research work on DACX has experimental results on voltage over 2 kV.

This dissertation’s target is to design and implement a two level DACX for 7.2 kV applications. It is crucial to find a suitable topology that is suitable for both high voltage and wide input voltage. There are several challenges in topology selection need to be addressed.
2.1.1 Review on ZVS Topologies for Direct AC-AC Converter

The first challenge comes from wide input voltage range, which requires the selected topology to realize ZVS operation over wide range of voltage. This is drastically different from DC-DC converter. At 7.2 kV input condition, semiconductor devices need to process voltage that is changing from 0 V to 10 kV every line frequency cycle. The selected topology need to obtain zero voltage switching (ZVS) across extremely wide voltage and load conditions.

Great efforts have been devoted to address the ZVS challenges in DACX. Paper [30] proposed a direct AC-AC converter based on dual active bridge (DAB) topology for MV application. Detail circuit is shown in Figure 2-2, in which four-quarter devices are adopted.

Figure 2-2 Dual Active Bridge based AC-AC converter circuit used in [30]
Dual active bridge (DAB) circuit is a popular topology in DC-DC applications with relative good ZVS capability and controllability. However, when applied it in direct AC-AC applications, this circuit shows some limitations. This circuit has drawbacks of limited ZVS range. ZVS might be lost at light load or low input voltage conditions. In addition, the turn off current is high in this circuit, especially when load is heavy, which might contribute to higher switching loss and limit converter’s efficiency performance. Additional auxiliary circuit or complex control scheme can be used to extend the ZVS range in DAB [31],[32], but may lead to higher conduction loss. Due to the concern of complex ZVS circumstance, DAB topology is not adopted in this dissertation’s research.

Figure 2-3 SST with direct AC-AC isolated front end based on SRC circuit [11]
Series resonant converter (SRC) is another popular circuit that is widely adopted in DC-DC applications. ZVS of this topology is independent of load conditions, which means that if ZVS is achieved at one load point, it can be achieved across entire load range. When applied SRC in DACX, more research works are needed to investigate the ZVS behavior of SRC over wide range of input voltage. An Isolated Front End (IFE) SST based on series resonant (SRC) topology is proposed in [33] and the detail circuit is shown in Figure 2-3. The circuit is a modular based direct AC-AC converter that converts AC input voltage to a half sinusoidal voltage. SRC circuit is used in the isolated front stage to achieve ZVS operation of the primary switches under wide input voltage range. This paper uses a modular based input series output parallel structure with each stage’s operating of 900 V.

From previous statements, SRC circuit is more attractive in DACX application for its non-load dependent ZVS capability. However, besides ZVS operation, other challenges need to be addressed before applying SRC circuit in direct AC-AC converter.

2.1.2 Review on Capacitance Reduction Methods

The second challenge for DACX is that a proper topology is needed to reduce the total capacitance in the system.

There is no DC voltage inside DACX, thus no DC capacitor is needed. Capacitance inside system will lead to unwanted reactive power and this reactive power might affect input power factor performance. Equation (2.1) calculates the reactive power that is generated by system capacitance, which shows that the reactive power is proportional to square of the input voltage. In MV applications, the voltage is extremely high, which means that a small amount of
capacitance will result in large reactive power. For example, if the applied input voltage is 7.2 kV, a capacitance value of 50 nF will generate 1 kW reactive power.

\[ Q = \frac{V_{ac}^2}{X_c} = V_{ac}^2 \omega_{line} C_{total} \tag{2.1} \]

LLC type SRC is selected as the topology in this research work for its ZVS capability. However, conventional SRC circuit normally has large capacitance, which is not applicable in our application due to the reactive power consideration. More investigation into SRC circuit is needed.

Typical conventional SRC circuit for DC-DC application is shown in Figure 2-4. Both the input side and output side of the circuit are large DC capacitors. These capacitors are used to carry and filter the large ripple current from the resonant tank. This is named as voltage fed series resonant converter (VFSRC) since both side of the converter can be regarded as voltage sources. The AC equivalent circuit model based on FHA analysis is shown in Figure 2-4, which indicates that the resonant tank is powered by two voltage sources. The equivalent resonant frequency of the circuit is derived as

\[ f_r = \frac{1}{2\pi \sqrt{L_r C_r}} \tag{2.2} \]

When the circuit’s switching frequency is selected at this resonant frequency, the system gain equals to 1 and this gain is independent of load conditions. Switching frequency is normally chosen around the resonant frequency for high efficiency performance.

\[ f_{sw} = f_r \tag{2.3} \]
Typical operation waveforms of VFSRC at its resonant frequency are shown in Figure 2-5. Turn off current of VFSRC is listed in (2.4), in which the turn off current is the function of input voltage, switching frequency and magnetizing current. As long as the input voltage, $L_m$ and switching frequency are constant, this turn off current is constant and is independent of load conditions. This property is the major advantage of SRC circuit over DAB circuit.
\[ I_{Lm}(V_{ds}) = \frac{V_{ds}T_s}{8L_m} \]

Table 2-1 Electrolyte and Film Capacitor Comparison Summary

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Electrolyte capacitor</th>
<th>Film Capacitor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Capacitance density</td>
<td>High (3×Film)</td>
<td>Low</td>
</tr>
<tr>
<td>ESR mΩ</td>
<td>High (10~15×Film)</td>
<td>&lt; 2 mΩ typical</td>
</tr>
<tr>
<td>Ripple Current</td>
<td>Low</td>
<td>2×Electrolyte</td>
</tr>
<tr>
<td>Voltage</td>
<td>550V Max</td>
<td>Up to 1500VDC</td>
</tr>
<tr>
<td>Resistance to overvoltage</td>
<td>50 V Surge</td>
<td>1.5 × rated for 10 s</td>
</tr>
<tr>
<td>Polarity</td>
<td>Polarized DC only</td>
<td>Nonpolarized</td>
</tr>
<tr>
<td>Life time</td>
<td>&lt; 80000HRS</td>
<td>&gt; 200000HRS</td>
</tr>
<tr>
<td>Failure Mode</td>
<td>Rupture/Short</td>
<td>Open circuit</td>
</tr>
<tr>
<td>Construction</td>
<td>Liquid or gel can leak</td>
<td>Dry</td>
</tr>
</tbody>
</table>

ZVS capability over wide load range makes SRC circuit an attractive topology. However, for conventional VFSRC, large capacitance is normally required for ripple current filtering, especially in high power applications such as the low voltage (LV) side of MV converter. In LV DC-DC conditions, electrolytic capacitors are normally chosen to absorbing rippling current and provide DC voltage due to their 3 times higher energy density than film capacitors. Thus, VFSRC circuit is not a good choice in DACX.
When it comes to the medium voltage, case is slightly different. The much higher voltage level also results in large impact on the capacitors that can be used.

Table 2-1 provides the comparison summary between electrolytic capacitor and film capacitor. In DACX applications, electrolytic capacitor is not applicable since electrolytic capacitor can only handle polarized DC voltage. In addition, electrolytic capacitors normally have limited lifetime (less than 80000HRS), low voltage stress and low ripple current capability. Thus, for MV DACX applications, electrolyte capacitor is not applicable.

In contrast, film capacitor offers much longer lifetime (over 100000HRS) and 2 times higher ripple current density, which are very attractive. Furthermore, film capacitor owns very low ESR, much higher voltage rating and has open circuit failure mode, which make it very suitable for MV applications. The drawback of film capacitor is its low energy density, which is typical one third of electrolyte capacitor. Low energy density result in larger volume and weight when comparing to electrolyte capacitor with same value. As voltage rating increases, film capacitor’s volume and weight also increase dramatically due to the high voltage insulation requirement. Capacitor’s volume has become an important limitation that limit the MV converter power density.

On effective way to solve this issue is reducing the required capacitance inside system. This idea is coordinate with previous requirement that trying to limit system reactive power. Reducing the required system capacitance enables an all film capacitor MV DACX, which helps improve system lifetime performance and power density.

Many research works have been done on investigating methods to reduce the required capacitance in DC or AC systems.
Paper [35] introduced a ripple eliminator circuit into rectifier circuit to reduce system DC capacitance. The detail circuit is shown in Figure 2-6. Ripple current is transferred into auxiliary capacitor during operation, which helps reduce the required DC capacitance. However, this method requires additional switches, passive components and control circuits, which is not practical in MV applications.

Figure 2-6 Rectifier circuit with ripple eliminator to reduce capacitance
Series resonant converter with inductive output filter or LC output filter are proposed in [36], [37] to reduce the ripple current of the output capacitor, which helps reduce output capacitance. Detail circuit and inductor current are provided in Figure 2-8. This method is useful in capacitance reduction since the added inductor helps reduce current ripple that flows into capacitors. However, it brings new issue. Since full bridge is used in this circuit, the resonant tank current is directly related to the output inductor current. As can be seen from the inductor waveform, the current inside the resonant tank is clamped by output current during operation. This square current is much different from the original desired sinusoidal like current in conventional SRC circuit. The ZVS properties of SRC is greatly affected by the added input and output inductor.

Figure 2-7 SRC circuit with LC filter on output side
Previous research shows that adding inductor helps reduce current ripple, which helps reduce capacitance. At the same time, the resonant current inside resonant tank should not be affected by the added inductor. Paper [38] proposed an input current fed (ICF) cell as shown in Figure 2-8, which is named as input current fed cell. The capacitor $C_r$ in this cell not only works as a resonant capacitor to achieve resonant current inside resonant tank, but also works as a decoupling capacitor that helps decouple the input DC current and resonant current. With this ICF cell, ZVS on and ZCS off for switches can be realized and system capacitance can be minimized.

2.2 Proposed CFSRC

2.2.1 Proposed Current Fed Series Resonant Converter (CFSRC)

The ICF cell in Figure 2-8 can be extended into half bridge ICF cell as shown in Figure 2-9.
In this dissertation, a symmetric half bridge Current-Fed SRC (CFSRC) based on half bridge ICF cell is proposed for MV direct AC-AC application. Detail circuit is shown in Figure 2-9. This approach shows many benefits when applied in DACX.

Firstly, this approach helps minimize the total capacitance in the system. Since the proposed SRC is based on current fed, the input and output side current ripple is filtered with inductors, thus only minimum value of capacitance is needed in the system. Reactive power generated by capacitance in AC system is also minimized. Film capacitor can be used instead of aluminum capacitors for longer life cycle performance while high power density is still achievable.

Secondarily, both sides of the circuit adopt half bridge structure with split capacitors forming a bridge leg. These capacitors help decoupling the MF resonant current inside the resonant tank and LF current on input/output side. Therefore, sinusoidal shape of current waveform is still achieved in resonant tank, ZVS conditions is similar to conventional VFSRC and can be achieved across wide voltage and load range.
First harmonic approximation (FHA) is a powerful tool to analyze resonant converters near resonant frequency [39], [40].

Figure 2-10 shows the circuit and its AC equivalent circuit. The resonant tank can be regarded as powered by input and output current sources.

![Circuit and Equivalent Small Signal Model of Current Source SRC](image)

**Figure 2-10 Circuit and Equivalent Small Signal Model of Current Source SRC**

### 2.3 Proposed Direct AC-AC Converter

Based on the proposed CFSRC circuit, detail DACX system configuration can be derived.

Figure 2-11 shows the proposed circuit configuration 1, which is based on Type A-1 structure. Four-quadrant switching cells are used in this case. Bidirectional power flow is realizable in this configuration. Half bridge structure is adopted to reduce the numbers of MF MV SiC MOSFETs. There are four MF MV SiC MOSFETs in total in the proposed system.
To further reduce the number of MF MV SiC MOSFETs, configuration 2 based on Type A-2 is proposed Figure 2-12. This circuit consists of a MV LF folding stage that converts LF MV ac voltage to half sinusoidal voltage. The second stage adopts MF series resonant converter to convert half sinusoidal MV to half sinusoidal LV. The final stage is an unfolding stage that converts the LV half sinusoidal voltage back into LF AC voltage. The input and output stages operate at line frequency, thus there is only conduction loss exist in these two stages. The MF MV stage only need to deal with unidirectional voltage, so simple MOSFETs can be used in the MF stage. The system contains a minimum number of 15 kV SiC MOSFETs- $P_1$ and $P_2$.

Figure 2-11 Proposed Configuration 1
If only unidirectional power flow is needed, configuration 2 can be further simplified into configuration 3. In which the LF input folding bridge is replaced with a diode bridge. This
structure can be used to block the bidirectional power if the reverse power conversion needs to be avoided.

With two level single stage system configuration, many potential advantages can be achieved. Since only one stage of power conversion is required, high efficiency can be achieved.

In this dissertation, configuration 3 will be used as an example to illustrate the detail design and implementation of DACX for 7.2 kV application.

2.3.1 Operation Principle

The proposed CFSRC circuit is similar to conventional VFSRC.

![Figure 2-14 Circuit of Current Source SRC](image_url)
Figure 2-15 shows the detailed operation waveforms for the proposed CFSRC. It can be found that the operating principle is similar to VFSRC. The only difference is the operation of resonant capacitor. In VFSRC, resonant capacitor participates in resonant during all times of switching cycle. While in CFSRC, resonant capacitor such as Crs1 will only join resonant during half of switching cycle. It is clamped by output current during the other half switching cycle.
2.3.2 Time Domain Analysis

There are two operation modes within half switching cycle.

Mode 1 \([t_0 \sim t_1]\): This mode begins when \(P_2\) turns off at time \(t_0\). The resonant current \(i_{rp}\) is negative and starts to charge the output capacitance \(C_{oss2}\) of \(P_2\) and discharge the output...
capacitance $C_{oss1}$ of $P_1$. This mode is a transient mode important for achieving the ZVS operation for $P_1$.

Mode 2 $[t_1 \sim t_2]$: At time $t_1$, the voltage on $C_{oss1}$ is discharged to 0 and resonant current $i_{rp}$ flows through $P_1$’s body diode. $P_1$ turns on after $t_1$ with ZVS, and $i_{rp}$ resonates to its positive half cycle. The equivalent circuit for time interval $[t_1 \sim t_2]$ is shown in Figure 2-16. The input and output inductors are treated as two current sources, $i_{Lin}$ and $i_{Lo}$. The current difference between $i_{Lin}$ and $i_{rp}$ flows into $Crp1$, while the difference between $i_{rp}$ and $i_{Lo}$ goes into $Crs1$. The other resonant capacitors, $C_{rp2}$ and $C_{rs2}$, are clamped by $i_{Lin}$ and $i_{Lo}$, respectively.

In Mode 2, the resonant tank contains four components: $L_{rp}$, $L_{rs}$, $C_{rp1}$ and $C_{rs1}$. The equivalent resonant frequency of the resonant tank is derived as:

$$\omega_r = \frac{1}{\sqrt{L_r C_r}}$$  \hspace{1cm} (2.5)

where $C_r = \frac{C_{rp1} C_{rs1,eq}}{C_{rp1} + C_{rs1,eq}}$, $L_r = L_{rp} + L_{rs,eq}$

$$C_{rs1,eq} = \frac{C_{rs1}}{n^2}, \text{ and } L_{rs,eq} = n^2 L_{rs}.$$  

Transient interval Mode 1, and the magnetizing current in $L_m$ are neglected in the following analysis for simplification. The equivalent differential equation during Mode 2 is derived in (2.6).

$$\int_0^t \frac{i_{rp1}(\tau) d\tau}{C_{rp1}} = L_r \frac{di_{rp}(t)}{dt} + \int_0^t \frac{i_{crs1,eq}(\tau) d\tau}{C_{rs1,eq}}$$  \hspace{1cm} (2.6)

At steady state, input power equals to output power if we ignore power loss inside system, so we can assume that $i_{Lin} = \frac{1}{n^2} i_{Lo}$. Equation (2.6) can be simplified.
\[ \frac{d^2 i_{rp}(t)}{dt^2} + \omega_r^2 i_{rp}(t) = \omega_r^2 i_{Lin} \]  

2.7

The solution for the resonant current can be derived

\[ i_{rp}(t) = I_r \sin(\omega_r t + \varphi) + i_{Lin} \]  

2.8

The resulting resonant current for Mode 2 is drawn in green curve in Figure 2-17, which contains a resonant tank frequency component and a DC bias current of \( i_{Lin} \). Note that the resonant tank time interval \( T_r/2 \) is not equal to the current zero crossing time interval \( T_{sw}/2 \) in Figure 2-17. This is very different with conventional VFSRC. This is due to the DC bias current, \( i_{Lin} \), introduced into the resonant current. Unity gain can only be achieved if the
switching frequency, $f_s$, is selected right at the current zero crossing. This frequency is the real 
equivalent resonant frequency, $f_{zc}$, for the CFSRC.

The operation principle of the other half switching cycle $t_2$–$t_4$ is symmetric to $t_0$–$t_2$ and the 
resonant current for a full switching cycle is derived in equation (2.9). The result resonant 
current during entire switching cycle is drawn as red curve in Figure 2-17. In which the 
switching frequency is selected right at the current zero crossing. The result current has 
sinusoidal shape.

$$i_{rp}(t) = \begin{cases} 
I_r \sin(\omega_r t - \varphi) + i_{Lin}, & 0 \leq t \leq T_s/2 \\
i_r \sin(\omega_r t - 3\varphi) - i_{Lin}, & T_s/2 \leq t \leq T_s 
\end{cases}$$  \hspace{1cm} (2.9)

To find the value of unknown parameters in equation (2.9), zero-crossing constraint of the 
resonant current is used

$$i_{rp}(0) = I_r \sin(\varphi) + i_{Lin} = 0$$ \hspace{1cm} (2.10)

The equation for current that flows through primary side capacitor $C_{rp1}$ is derived in 
equation (2.10).

$$i_{crp1}(t) = \begin{cases} 
-i_r \sin(\omega_r t + \varphi), & 0 \leq t \leq T_s/2 \\
_i_{Lin}, & T_s/2 \leq t \leq T_s 
\end{cases}$$ \hspace{1cm} (2.11)

The charging and discharging balance of the primary side capacitor, $C_{rp1}$, is also applied. 
Equation (2.12) is derived from (2.10) and (2.11).

$$\tan(\varphi)\left(\frac{2\varphi}{\pi} + 1\right) = \frac{2}{\pi}$$ \hspace{1cm} (2.12)
Solving (2.12) provides a phase shift, \( \varphi = 0.458 \). The relationship between \( \omega_{zc} \) and \( \omega_r \) is then derived in (2.13).

\[
f_{zc} = \frac{f_r \pi}{\pi + 2\varphi} = 0.774 f_r
\]

2.13

The result shows that the CFSRC’s zero crossing frequency, \( \omega_{zc} \), is 0.774 times of the resonant tank frequency, \( \omega_r \). Switching frequency, \( f_s \), should be selected equal to \( f_{zc} \) to achieve unity gain.

### 2.3.3 Fundamental Harmonic Approximation

In addition to the time domain analysis, analysis based on FHA method is also conducted for verification.

The secondary side current can be represented with a switching frequency sinusoidal current \( i_{r,F}(t) \). The current flow through secondary side resonant capacitor \( C_{rs1} \) can be describe in equation

\[
I_{cr1}(t) = \begin{cases} 
  i_{r,F}(t) - I_o, & 0 \leq t \leq T_s/2 \\
  -I_o, & T_s/2 \leq t \leq T_s 
\end{cases}
\]

2.14

Equation (2.15) can be derived based on \( C_{rs1} \)'s charging and discharging balance.

\[
i_{r,F}(t) = \pi I_o \sin(\omega_s t)
\]

2.15
The secondary side half bridge mid terminal voltage $V_{ac}$ in Figure 2-18 is provided in equation (2.16). The waveform of $V_{ac}$ is drawn in Figure 2-21.
\[ V_{ac}(t) = \begin{cases} V_{crs1}(t), & 0 \leq t \leq T_s/2 \\ -V_{crs2}(t), & T_s/2 \leq t \leq T_s \end{cases} \]  \hspace{1cm} (2.16)

Currents that flow through secondary capacitors \( C_{rs1} \) and \( C_{rs2} \) are listed in equation (2.17) and (2.18):

\[ I_{cr1}(t) = \begin{cases} \pi I_o \sin(\omega_s t) - I_o, & 0 \leq t \leq T_s/2 \\ -I_o, & T_s/2 \leq t \leq T_s \end{cases} \]  \hspace{1cm} (2.17)

\[ I_{cr2}(t) = \begin{cases} -I_o, & 0 \leq t \leq T_s/2 \\ -\pi I_o \sin(\omega_s t) - I_o, & T_s/2 \leq t \leq T_s \end{cases} \]  \hspace{1cm} (2.18)

Figure 2-20: Secondary side resonant capacitor voltage
During half of the switching cycle, the secondary capacitor \( C_{rs1} \) are discharging with the output current. Therefore, the capacitor ripple voltage on these secondary resonant capacitors is derived as

\[
\Delta V_{crs} = \frac{T_s I_o}{2C_{rs}} = \frac{\pi I_o}{\omega_s C_{rs}} \tag{2.19}
\]

The voltage waveforms of secondary resonant capacitors \( C_{rs1} \) and \( C_{rs2} \) are shown in Figure 2-20. The total voltage VCT shown in same figure is the combination of voltages on \( C_{rs1} \) and \( C_{rs2} \). This figure shows that although voltage on resonant capacitor has large ripple voltage, these ripple voltages will cancel each other and form a low ripple voltage output voltage. This figure also shows that \( C_{rs1} \) and \( C_{rs2} \) not only act as resonant capacitors, but also work as filter capacitors to the output side.

Voltages equations on these capacitors can be derived as

\[
V_{cr1}(t) = \begin{cases} 
\frac{V_o}{2} - \frac{\Delta V_{crs}}{2} + \frac{\pi I_o}{\omega_s} \left( 1 - \cos(\omega_s t) \right) - I_o t \frac{1}{C_{rs}}, & 0 \leq t \leq T_s/2 \\
\frac{V_o}{2} + \frac{\Delta V_{crs}}{2} - I_o \left( t - \frac{T_s}{2} \right) \frac{1}{C_{rs}}, & T_s/2 \leq t \leq T_s 
\end{cases} \tag{2.20}
\]

\[
V_{cr2}(t) = \begin{cases} 
\frac{V_o}{2} + \frac{\Delta V_{crs}}{2} - I_o t \frac{1}{C_{rs}}, & 0 \leq t \leq T_s/2 \\
\frac{V_o}{2} - \frac{\Delta V_{crs}}{2} + \frac{\pi I_o}{\omega_s} \left( 1 + \cos(\omega_s t) \right) - I_o \left( t - \frac{T_s}{2} \right) \frac{1}{C_{rs}}, & T_s/2 \leq t \leq T_s 
\end{cases} \tag{2.21}
\]

The detail expression for \( V_{ac} \) is derived as
\[ V_{ac}(t) = \begin{cases} 
\frac{V_o}{2} - \frac{\pi I_o (\cos(\omega_s t))}{\omega_s C_{rs}} + \frac{\Delta V_{crs}}{2} - \frac{I_o t}{C_{rs}}, & 0 \leq t \leq T_s/2 \\
-\frac{V_o}{2} - \frac{\pi I_o (\cos(\omega_s t))}{\omega_s C_{rs}} - \frac{\Delta V_{crs}}{2} + \frac{I_o (t - T_s/2)}{2}, & T_s/2 \leq t \leq T_s 
\end{cases} \tag{2.22} \]

where \( \Delta V_{crs} = \frac{\pi I_o}{\omega_s C_{rs}} \) is the ripple voltage of capacitors \( C_{rs1} \) and \( C_{rs2} \).

Investigating equation (2.22), voltage \( V_{ac} \) can be divided into three parts: (i) a square waveform, \( V_{sq}(t) \), (ii) a cosine waveform, \( V_{cos}(t) \), and (iii) a triangular waveform, \( V_{tri}(t) \). \( V_{ac} \) and the three associated components, expressed mathematically in (2.23) – (2.25), are drawn in Figure 2-21.

Figure 2-21 \( V_{ac} \) and its three elements composition.
\[ V_{sq}(t) = \begin{cases} \frac{V_o}{2}, & 0 \leq t \leq T_s/2 \\ -\frac{V_o}{2}, & T_s/2 \leq t \leq T_s \end{cases} \]  

\[ V_{cos}(t) = \frac{-\pi I_o \cos(\omega_s t)}{\omega_s C_{rs}} \]  

\[ V_{tri}(t) = \begin{cases} \frac{\Delta V_{crs}}{2} + \frac{-I_o t}{C_{rs}}, & 0 \leq t \leq T_s/2 \\ -\frac{\Delta V_{crs}}{2} + \frac{I_o(t - \frac{T_s}{2})}{C_{rs}}, & T_s/2 \leq t \leq T_s \end{cases} \]

FHA method is used to find the fundamental harmonic of the three derived elements. Fundamental components of each component are provided in (2.26) – (2.28). The associated fundamental curves are drawn Figure 2-22.

\[ V_{sq,F}(t) = \frac{2V_o}{\pi} \sin(\omega_s t) \]  

\[ V_{cos}(t) = \frac{-\pi I_o \cos(\omega_s t)}{\omega_s C_{rs}} \]  

\[ V_{tri,F}(t) = \frac{4I_o}{\pi \omega_s C_{rs}} \cos(\omega_s t) \]  

The resulting half bridge voltage can be simplified as

\[ V_{ac,F}(t) = V_{sq,F}(t) + V_{cos}(t) + V_{tri,F}(t) \]
The impedance seeing from the half bridge can be found through dividing $V_{ac,F}$ by $i_{r,F}(t)$. Three equivalent components can be found as shown in Figure 2-23, a resistor, a capacitor, and an inductor.

The value of each component is found in (2.30) – (2.32).

\[ R_{ac} = \frac{V_{sq,F}(t)}{i_{r,F}(t)} = \frac{2}{\pi^2} R_o \quad \text{(2.30)} \]

\[ C_{eqs} = \frac{i_{r,F}(t)}{dV_{cap}(t)/dt} = C_{rs} \quad \text{(2.31)} \]

\[ L_{eqs} = \frac{V_{tran,F}(t)}{di_{r,F}(t)/dt} = \frac{4}{\pi^2 \omega_s^2 C_{rs}} \quad \text{(2.32)} \]

Figure 2-22 Fundamental components approximation.
After completing the same analysis on the primary side, the AC equivalent circuit for the proposed CFSRC is shown in Figure 2-24. Different from VFSRC circuit, where the resonant capacitors are $2C_{rp}$ and $2C_{rs_{eq}}$, the result resonant capacitors in proposed CFSRC are $C_{rp}$ and $C_{rs_{eq}}$. This is because during operation, only one resonant capacitor on each side participate.
in resonant. However, CFSRC introduced two additional inductor components, $L_{eqp}$ and $L_{eqs}$, into the circuit. These two inductors are associated with the capacitor on each side.

The equivalent total resonant inductance of the whole system is

$$L_{eq} = L_{eqs} + L_{eqp} + L_r = \frac{4}{\pi^2 \omega_s^2} \frac{1}{C_{r,eq}} + L_r$$  \hspace{1cm} 2.33

Where

$$L_{eqs} = \frac{4}{\pi^2 \omega_s^2}, L_{eqp} = \frac{4}{\pi^2 \omega_s^2}.$$  

$$R_{ac} = n^2 \frac{2}{\pi^2} R_o, C_{eqp} = C_{rp}, C_{eqs} = \frac{1}{n^2} C_{rs}$$

The system equivalent resonant frequency is then obtained as

$$\omega_{zc}^2 = \frac{1}{C_r L_{eq}} = \frac{1}{C_r \left( \frac{4}{\pi^2 \omega_s^2} \frac{1}{C_r} + L_r \right)}$$  \hspace{1cm} 2.34

Notice that (2.32) contains a switching frequency, $\omega_s$, and a system equivalent resonant frequency, $\omega_{zc}$. If the switching frequency is selected to be the same as the equivalent resonant frequency, $\omega_{zc} = \omega_s$. Equation (2.35) can be derived.

$$f_{zc} = \sqrt{\frac{1 - \frac{4}{\pi^2}}{\sqrt{C_r L_r}}} = \frac{0.771}{\sqrt{C_r L_r}} = 0.771 f_r$$  \hspace{1cm} 2.35

This result is consistent with the result obtained in time domain analysis, which indicates that the proposed CFSRC circuit equivalent system resonant frequency is 0.771 times of the resonant tank frequency. The switching frequency should be selected at frequency, $f_{zc}$, to achieve unity system gain.
2.3.4 Voltage Gain Investigation

Base on the FHA method, a relevant AC equivalent circuit of the proposed CFSRC is derived in Figure 2-24. In order to derive the voltage gain equation for the proposed circuit, a more accurate AC equivalent circuit that contains magnetizing inductance $L_m$ is provided in Figure 2-25 for voltage gain investigation.

Parameters in Figure 2-25 are $R_{ac} = n^2 \frac{2}{\pi^2} R_o$, $C_{eqp} = C_{rp}$, $C_{eqs} = \frac{1}{n^2} C_{rs}$

$$L_{eqs} = \frac{4}{\pi^2 \omega_s^2 c_{eqs}}$$

$$L_{eqp} = \frac{4}{\pi^2 \omega_s^2 c_{eqp}}$$

$L_{rp}$ and $L_{rs}$ are equivalent leakage inductance distributed on two sides of the transformer.

Total equivalent voltage gain can be calculated as

$$M = \frac{\omega L_m R_{ac}}{j(\omega^2 (L_m L_{ik} + L_{ik} L_{ik} + L_m L_{ik}) - \frac{L_m + L_{ik}}{C_{eqp}} + \frac{L_m + L_{ik}}{C_{eqs}} + \frac{1}{\omega^2 C_{eqp} C_{eqs}} + R_{ac}(\omega^2 L_m + L_{ik}) - \frac{1}{\omega^2 C_{eqp}})}$$ \hspace{1cm} 2.36
Where \( L_{tkp} = L_{eqp} + L_{rp}, L_{tkp} = L_{eqs} + L_{rs} \).

(a) Type 2

(b) Type 3

(c) Type 4

(d) Type 5

Figure 2-26 A family of circuit based on ICF cell
2.3.5 Extension Application of ICF Cell

The introducing of HF ICF cell into SRC doesn’t affect the resonant tank current shape. However, it will affect the equivalent zero current crossing frequency.

In practical applications, the HF ICF cell can be used together with conventional voltage fed bridge cell.

Table 2-2 Current Zero Crossing Equivalent Frequency

<table>
<thead>
<tr>
<th>Symbol</th>
<th>$C_{rp_{eq}}$</th>
<th>$C_{rs_{eq}}$</th>
<th>$C_{eq}$</th>
<th>$L_{eq}$</th>
<th>$f_{zc}$</th>
<th>Gain</th>
</tr>
</thead>
<tbody>
<tr>
<td>CFSRC</td>
<td>$C_{rp}$</td>
<td>$C_{rs}$</td>
<td>$\frac{C_{rp}C_{rs}}{C_{rp} + C_{rs}}$</td>
<td>$\frac{4}{\pi^2\omega_s^2} \frac{1}{C_{eq}} + L_r$</td>
<td>$\sqrt{1 - \frac{4}{\pi^2} \frac{1}{C_{eq}L_r}}$</td>
<td>1</td>
</tr>
<tr>
<td>Type 2</td>
<td>$2C_{rp}$</td>
<td>$C_{rs}$</td>
<td>$\frac{2C_{rp}C_{rs}}{2C_{rp} + C_{rs}}$</td>
<td>$\frac{4}{\pi^2\omega_s^2} \frac{1}{C_{rs_{eq}}} + L_r$</td>
<td>$\sqrt{1 - \frac{2k - 1.4}{2k} \frac{1}{\pi^2}} \frac{1}{\sqrt{C_{eq}L_r}}$</td>
<td>1</td>
</tr>
<tr>
<td>Type 3</td>
<td>$C_{rp}$</td>
<td>$C_{rs}$</td>
<td>$\frac{C_{rp}C_{rs}}{C_{rp} + C_{rs}}$</td>
<td>$\frac{4}{\pi^2\omega_s^2} \frac{1}{C_{rs_{eq}}} + L_r$</td>
<td>$\sqrt{1 - \frac{k - 1.4}{k} \frac{1}{\pi^2}} \frac{1}{\sqrt{C_{eq}L_r}}$</td>
<td>2</td>
</tr>
<tr>
<td>Type 4</td>
<td>$C_{rp}$</td>
<td>$2C_{rs}$</td>
<td>$\frac{2C_{rp}C_{rs}}{C_{rp} + 2C_{rs}}$</td>
<td>$\frac{4}{\pi^2\omega_s^2} \frac{1}{C_{rp_{eq}}} + L_r$</td>
<td>$f_{eq} = \sqrt{1 - \frac{4}{\pi^2} \frac{1}{k}} \frac{1}{\sqrt{C_{eq}L_r}}$</td>
<td>1</td>
</tr>
<tr>
<td>Type 5</td>
<td>$C_{rp}$</td>
<td>$C_{rs}$</td>
<td>$\frac{C_{rp}C_{rs}}{C_{rp} + C_{rs}}$</td>
<td>$\frac{4}{\pi^2\omega_s^2} \frac{1}{C_{rp_{eq}}} + L_r$</td>
<td>$f_{eq} = \sqrt{1 - \frac{4}{\pi^2} \frac{1}{k}} \frac{1}{\sqrt{C_{eq}L_r}}$</td>
<td>0.5</td>
</tr>
</tbody>
</table>

A family of SRC circuits based on HF ICF cell and voltage based bridge are provide in Figure 2-26 (a)- (d). All circuits here reserves AC shape current in resonant tank. Which not only helps realize ZVS operation of primary side switches over wide load range, but also helps obtain low turn off current to minimize switching loss. The ac equivalent circuits based on FHA method are provided as well. These derived circuit can be useful in practical applications.
For example, if a MV to LV DC-DC converter is required. HF ICF cell can be used on MV side to minimize the required MV capacitors in system. Voltage based bridge cell can be used on LV side to offer constant DC voltage.

The current zero crossing frequency of these derived circuits are provided in Table 2-2.

### 2.4 Conclusion

A two level, single stage AC/AC converter, offers the best performance in efficiency and reliability in MV applications. This chapter proposes a single stage, direct AC-AC converter based on symmetric half bridge Current-Fed SRC (CFSRC) topology. The proposed topology offers two attractive properties in MV applications. 1) enables ZVS operation across wide voltage range and entire load range, which means higher switching frequency can be achieved for higher power density. 2) minimize the total capacitance in the system, which not only helps achieve high power density, but also enables the use of film capacitors instead of aluminum capacitors to improve the system life cycle. The operation principle of the proposed CFSRC is analyzed in detail. Equivalent zero crossing frequency is analyzed for the first time in both time domain and frequency domain. The design equations are derived to accurately select the switching frequency.
Chapter 3.  15 kV SiC MOSFETs Revisit and ZVS
Design Over Wide Voltage Range

3.1 Introduction

One of the advantage of the SSTs is the switching frequency can be pushed higher, thus lower transformer size and higher power density can be achieved.

Silicon power device such as Si IGBTs were widely used in MV applications in previous researches [5][6][8]. Figure 3-1 shows a 6500 V/600 A Si IGBT module from ABB. However, the maximum blocking voltage of Si IGBTs is limited to 6.5 kV due to the peak electric field strength limit of Si material. Conduction loss will substantially increase if device is designed for even higher voltages. The achieved operation switching frequency of previous developed prototypes on IGBT are lower than 5 kHz due to the relative slow turn off characteristics (known as current tail).

Figure 3-1 6500 V / 600 A IGBT from ABB
Due to almost ten times higher peak electric field strength in SiC when compared to Si, SiC power devices with much higher blocking voltage have been developed and demonstrated in recent years. The blocking voltage ranges from 10 kV to 24 kV based on unipolar (i.e. SiC MOSFET) and bipolar (i.e. SiC IGBT/ETO) conduction mechanisms [44]. Although not yet commercially available, they can enable a simpler and robust two-level SST in 7.2 kV applications where the peak voltage stress is less than 12 kV. As a comparison, Si power MOSFETs are typically designed with a blocking voltage less than 1200V.

![Figure 3-2 I-V curve comparison of 15-kV SiC P-GTO, IGBT, and MOSFET at 25 C and 125 C. [59]](image)

Figure 3-4 shows the forward conduction characteristics comparison of the 15-kV P-GTO, IGBT and MOSFET. P-GTO and IGBT show lower voltage drop in higher current
applications. However, MOSFET operates as a unipolar conduction device, which shows a large reduction in switching loss compared with bipolar device IGBT and switching speed can be much faster.

Therefore, the 15 kV SiC MOSFET developed by Wolfspeed is a very promising device that cannot only achieve high voltage blocking but also high switching frequency. This device shows obvious advantages over SiC IGBT or SiC GTO when implemented in medium voltage low current applications.

Some preliminary works including double pulse test, $R_{on}$ and thermal tests were carried out to characterize the 15 kV SiC MOSFET thoroughly [14], [22]. The voltage blocking capability of this device has been proven up to 12 kV. However, only few research groups have implemented this device into continuous operation. So far, highest achieved continuous operation voltage of this device in AC-DC or DC-DC circuit is 6 kV [28]. The highest achieved frequency of this device is 40 kHz in ZVS DC-DC circuit.

The main challenges in reaching higher operation voltage include ZVS operation range, poor and/or unproven reliability of the prototype device and its associated package. Much better auxiliary circuits such as driving circuit and auxiliary power supplies must also be designed to handle the high isolation voltage as well as high common mode voltage range.

In direct AC-AC applications, different from DC-DC application, designers must also face a new and significant challenge, which is realize ZVS of MV devices across wide input voltage range (from 0V-10kV). To the author’s best knowledge, none of previous research has ever apply this device in direct AC-AC converters, not to mention the target of 7.2 kV operation of this dissertation. Utilizing this device in 7.2 kV direct AC-AC applications with high
frequency, high efficiency and reliable performance is significant. More researches need to be done to accomplish the target.

This chapter will first revisit the characterization of the 15 kV SiC MOSFET including switching model, $R_{on}$ model and thermal model. After which the 15 kV SiC MOSFET will be used as an example to provide comprehensive design guidelines for utilizing it to its full voltage, switching frequency and power potential in 7.2 kV AC-AC applications in terms of ZVS implementation, loss optimization, thermal management and device utilization.

![Image](image.png)

(a) packaged module  
(b) die dimension [47]

**Figure 3-3 15 kV SiC MOSFET**

### 3.2 15kV SiC MOSFET Revisit

The 15 kV SiC MOSFET developed by Wolfspeed uses a DMOS device structure similar to that shown in Figure 3-3 [47]. The chip size has a dimension of 8.1mm×8.1mm in which
5.95×5.95 is the active area that conducts current. The device is packaged with a single side cooling capability as shown in Figure 3-3. The module is fabricated on AlN board for voltage insulation requirement and is mounted on heatsink for cooling.

![Graph showing the on-state resistance model](image)

**Figure 3-4 On-state resistance of the 15 kV SiC MOSFET modules [14]**

Before implementing this device in MV SSTs, accurate device conduction loss, switching loss and thermal models need to be developed.

### 3.2.1 On-State Resistance Model

The measured and modeled conduction resistance model curves of the device at 20V gate to source voltage are drawn in Figure 3-4.

The $R_{on}$ equation is derived as
\[ R_{on} = R_0 \left( \frac{T_j}{T_0} \right)^{3.5} \]

Where \( R_0 = 0.875 \Omega \), \( T_0 = 348.16 \text{K} \)

Its room temperature on-resistance is much higher than low voltage devices due to the extremely high blocking voltage. It also increases quickly as temperature increases. This is typically for all unipolar devices such as the MOSFET, but the rate of increase for 15 kV device is substantially higher than 1200 V SiC MOSFET. This is due to the fact that the 15 kV device on resistance is dominated by the drift layer resistance in Figure 3-4. Due to the large on resistance, a single chip MOSFET is only capable to operate under relative low current conditions due to the conduction loss. Ideally applications will be those requiring high voltage and low current, such as a single phase SST in the range of 10 to 50 kVA.

![Figure 3-5 10 kV/120 A SiC MOSFET Module][10]

For high power applications, many MOSFET dies can be packaged in parallel to form a single MOSFET module. Figure 3-5 shows a 10 kV /120 A SiC power module that is proposed
in paper [10], in which 12 dies of 10 kV / 10 A MOSFETs are packaged paralleled to enable higher power converting.

In this dissertation, since the power target is 20 kW, only single die packaged power module is sufficient.

3.2.2 Device Packaging Consideration

![Diagram](image)

(a) packaging with silicon and JBS diodes

![Diagram](image)

(b) single switch package

Figure 3-6 15 kV SiC MOSFET packaging types
The 15 kV SiC MOSFET has an integrated body diode that can be used as the freewheeling diode in converter applications. Applying a positive gate voltage will enable the MOSFET to operate as a synchronous rectifier. This capability is a direct advantage of the MOSFET when compared with an IGBT which must have a paralleled freewheeling diode.

However, there may be a need to connect a separate SiC JBS diode with the 15 kV SiC MOSFET for several reasons. The body diode of the 15 kV SiC MOSFET does not turn on until a forward voltage higher than 3.2 V. This higher forward drop will result in higher conduction loss. Applying a gate voltage to operate it as a synchronous rectifier can lower the conduction loss to the same level as that of the forward direction with a resistance shown in Figure 3-4. This strategy can only happen after the deadtime period. Another more important reason is the poorer diode reverse recovery performance associated with the SiC PN junction diode if substantial carriers are injected by the PN junction. The forward conduction of the PN junction may also cause significantly device degradation (loss of the forward blocking capability and/or increase of the $R_{on}$) [48],[49]. Many research on this degradation has been conducted with several literatures indicated that the issue has been largely solved in 1200V SiC MOSFET. For the tested 15 kV SiC MOSFET, however, there is a significantly degradation observed if the body diode conducts.

For above reasons, the 15 kV SiC MOSFET prototype device should be used without the body diode conduction. A silicon diode is generally connected in series with the MOSFET to prevent the body diode from conducting, while a 15 kV SiC JBS diode is placed in paralleled to conduct the reverse current. Figure 3-6 (a) shows the device package, which is used in most
previous applications. However, these two added devices may affect the device performance as well as system designs.

The output charge $Q_{oss}$ of the 15 kV MOSFET, hence the associated loss $E_{oss}$, can be accurately measured with a novel method proposed in paper [27]. The upper curve in Figure 3-8 shows the output charge of the device up to 12 kV with a paralleled JBS diode, which has a significant higher $Q_{oss}$ than the MOSFET alone (lower curve). The $Q_{oss}$ model for the MOSFET plus JBS diode is derived as, unit is nC.

$$Q_{oss\_combine}(V_{ds}) = 11.43 \sqrt{V_{ds}} + 36 \cdot V_{ds} \ (nC)$$ \hspace{1cm} 3.2

At 11 kV, the total $Q_{oss}$ of the SiC MOSFET alone is around 700 nC, while the output charge of the JBS diode is around 900 nC at this point. The test result indicates that the output charging in JBS diode is even larger than that in MOSFET. In hard switching conditions, the added output charge will increase the hard switching $E_{on}$ loss. In ZVS converter, larger output charge requires higher turn off current or longer deadtime to discharge, either way it will in higher conduction loss for the system.

What’s more, this solution has some more drawbacks. First of all, this structure requires additional cost in device and packaging. Packaging three devices into single module may introduce additional risk of failure. Furthermore, the added silicon diode will not only cause additional conduction loss, but also will experience avalanche breakdown during every switching cycle [28].
Figure 3-6 (b) shows the 15 kV SiC MOSFET packaging that will be adopted in this dissertation. Single die is packaged on a copper substrate. The whole device is then mounted on AlN substrate, which offers higher than 12 kV voltage insulation.

The measured and modeled output charge curves of a single MOSFET and the combination structure are plotted in Figure 3-8. The \( Q_{\text{oss}} \) model equation of the single die module is expressed in (3.3),

\[
Q_{\text{oss, single}}(V_{ds}) = 4.08 \sqrt{V_{ds}} + 24.8 \cdot V_{ds} \cdot (nC) \tag{3.3}
\]

This dissertation will prove that, in a well-designed AC-AC converter with ZVS operation, body diode conduction of the MOSFET can be avoid if deadtime and system parameters are properly designed. So that the anti-parallelled SiC JBS diode can be eliminated. This will lower the semiconductor cost, increase system reliability and reduce system conduction loss.

3.2.3 Switching Loss Model

The SiC MOSFET has very fast switching speed capability because it is a unipolar switch with no current tail. The switching time is typically less than 500 ns as shown in Figure 3-7 in which the dynamic turn-on and turn-off waveforms under 8 kV/8A conditions are shown. However, this high switching speed does not directly translate to high switching frequency. In MV applications, the energies stored in the output capacitance of the devices is extremely high, which will result in large turn-on loss if the stored energies are not carefully recovered. An accurate \( Q_{\text{oss}} \) and \( E_{\text{oss}} \) model is critical for converter design.
**Turn-on Loss:** The minimum turn on energy under hard switching condition is the energy stored in the output charge of the device. Additional turn-on loss occurs due to the controlled \( \frac{dl}{dt} \) and \( \frac{dV}{dt} \) which results in a large voltage and current overlap during the turn-on, as shown in Figure 3-7.

For the packaged 15 kV SiC MOSFET device. If the associated energy \( E_{oss} \) is directly released to the device during the hard turn on, it will result in a substantial turn on loss.

![Waveforms](image)

(a) Turn on  
(b) Turn off

Figure 3-7 Turn on and turn off waveforms under 8 kV/8 A condition
**Turn-off Loss:** Since the load current for the 15 kV MOSFET is low, the turn-off process is dominated by the charging of the output capacitance of the MOSFET as well as the discharge of the associated freewheeling diode and load parasitic capacitance. This is clearly shown in Figure 3-7.

This process is almost lossless ($E_{\text{off}}=0$) since the energy is simply stored in the output capacitance and stored energy is $E_{\text{oss}}$. Hence the turn-off loss of the 15 kV SiC MOSFET can be modeled as zero. Similar situation can also happen in lower voltage SiC MOSFETs if the turn-off process is dominated by the load current determined charging of $C_{\text{oss}}$ of the switch, the freewheeling diode and the load parasitic capacitance [46].
Figure 3-9 The $E_{on}$ and $E_{off}$ of the 15 kV SiC MOSFET [52]
The measured $E_{on}$ and $E_{off}$ at 4 kV condition are shown in Figure 3-9 when compared with a 6.5 kV Si IGBT under similar test condition. The $E_{on}$ loss shown includes the $E_{oss}$ loss as well as the voltage and current overlap loss which has a strong dependence on the gate driving condition or $R_g$ value. Compared with the IGBT, the SiC MOSFET shows a much lower total loss. This overall lower switching loss enables higher switching frequency in MV converters under hard switching conditions, leading to smaller system volume and higher power density. Hard switching based AC-DC converter based the 15 kV MOSFET has been reported in [13], [28] which has a switching frequency of 6 kHz and a DC link voltage of 6 kV.

If the DC link voltage increases to 12 kV, the $E_{oss}$ loss remains close to zero while the $E_{on}$ loss increases substantially, as shown in Figure 3-9. This will limit the maximum switching frequency if the MOSFET operates in hard switching condition.

**ZVS Turn-on:** The switching frequency can be increased by recycling the output charge energy $E_{oss}$ back to the load and/or source through the well-known zero voltage switching technique. The basic idea is to use the inductive energy stored in an inductor to discharge the $C_{oss}$ of the device during the deadtime. A minimum amount of current is needed in the inductor and a typical ZVS criteria is shown in (3.4) where $Q_{oss}(V_{ds})$ corresponds to the charge in the $C_{oss}$ of the device prior to the discharge

$$I_{off}(V_{ds})t_{dead} \geq Q_{oss}(V_{ds})$$  \hspace{1cm} 3.4

60
With a combination of intrinsic capability (unipolar device vs. bipolar device) and circuit technique (ZVS vs. hard switching), the unique opportunity with the 15 kV SiC MOSFET can be summarized as a significantly increased operational Voltage $\times$ Frequency figure of merit (FOM) when compared with Si IGBT. This FOM is directly related to the MV converter performance. The higher the FOM, the better. The 15 kV SiC MOSFET device can achieve a FOM several hundred times higher than MV Si IGBT power devices. For example, the author’s group have already achieved steady operation of the 15 kV SiC MOSFET at 40 kHz under 10 kV/20 kW condition hence the FOM number is 400 Mhz-Volt. Additional analysis shown in
this chapter suggest that operation beyond 100 kHz is also feasible hence the FOM is increased to more than 1 GHz-Volt, which is 200 times higher than the typical 5 MHz-Volt capability of a Si IGBT device.

### 3.2.4 Thermal Consideration

In this dissertation, the 15 kV SiC module is mounted on a natural cooling heatsink without fan (see Figure 3-4), which has a measured junction to air thermal resistance of 1.5 °C/W. All the device utilization figures in section III is based on this thermal model. If a better cooling system such as forced air or water is adopted, the thermal resistance will be much lower and higher power capability can be further obtained.

### 3.3 ZVS Design Based on 15 kV SiC MOSFET

In this dissertation, the operation frequency is selected constant at the equivalent resonant frequency for unity gain and high efficiency performance.

With constant operation frequency, the ZVS condition is only associated with input voltage, magnetizing current, and deadtime. The turn off current of CFSRC is

\[ I_{Lm}(V_{ds}) = \frac{V_{ds}T_s}{8L_m} \]

3.5

This current is independent of the load condition and is used to discharge and charge the output charge, \( Q_{oss} \), of the SiC MOSFETs switches, \( P_1 \) and \( P_2 \), during deadtime. The full voltage ZVS constraint is obtained in (3.6).
Adaptive deadtime scheme: The orange and blue curves in Figure 3-12 are two critical deadtime curves versus a line frequency ac voltage under two different $L_m$ cases. If deadtime is designed based on these critical value, adaptive deadtime scheme is required. Figure 3-12 shows that at low input voltage conditions, a large deadtime is required to realize the ZVS operation. An accurate instantaneous voltage sensor and good phase lock loop are also required to accurately select the deadtime value; otherwise, the circuit may lose ZVS in steady state and dynamic conditions.

Constant deadtime scheme: On the other hand, switching losses on MV devices decrease rapidly as $V_{ds}$ decreases. In a practical design, it is possible for the MOSFETs to experience hard switching at low voltage conditions as long as the total power loss is low.

![Figure 3-11 Typical operation waveforms](image-url)
To simplify the deadtime control complexity, a constant deadtime scheme is proposed and is drawn as the pink curve in Figure 3-12. The value of this deadtime is designed to guarantee the ZVS operation of the MOSFETs under most high voltage conditions. Only when input voltage is under certain low level, the offered deadtime is not long enough to fully discharge the $Q_{oss}$ and minor switching loss may be generated. The detailed principle for partial discharge operation is drawn in Figure 3-13.

When partial discharge happens, the residual $Q_{oss}$ can be calculated as $Q_{res}(t) = Q_{oss}(t) - It_{dead}$.
The corresponding residual voltage at that point can be derived based on equation (3.7).

\[ V_{\text{res}}(t) = \left( \frac{-4.08 + \sqrt{4.08^2 + 4 \cdot 0.0248 Q_{\text{rest}}(t) \cdot 10^9}}{2 \cdot 0.0248} \right)^2 \]  \hspace{1cm} 3.7

The turn on power loss under this situation can be calculated with equation (3.8).

Figure 3-13 Partial discharge theory.

Figure 3-14 Partial discharge theory.
\[ P_{on} \approx f_{SW} \cdot 2f_{line} \int_{0}^{\frac{1}{2f_{line}}} V_{res}(t)Q_{res}(t)\,dt \]  

Figure 3-14 shows the residual charge, \( Q_{res} \), and voltage, \( V_{res} \), versus the input voltage under different deadtime conditions. Figure 3-15 displays the results of turn on loss versus deadtime under different \( L_m \) conditions with a 40 kHz switching frequency. The curves show that the turn on loss decreases dramatically as the deadtime increases or \( L_m \) decreases. If the deadtime and \( L_m \) values are properly selected, the turn on loss will be small even if partial soft-switching happens.

![Figure 3-15 Residual Q and voltage versus input voltage.](image-url)
Figure 3-16  Turn on loss vs deadtime at 40 kHz.
3.4 System Loss Calculation

3.4.1 Conduction Loss

Figure 3-17 shows a typical waveform of CFSRC converter. RMS current on the MV side can be calculated with equations from (3.9) to (3.11) [53], [54].

\[
i_{r,p}(t) = \sqrt{2} I_{RMS,P} \sin(\omega_0 t + \varphi) \quad 3.9
\]

\[
i_{LM,p}(t) = -\frac{V_{in}T_0}{8L_m} + \frac{V_{in}}{2L_m} T \quad 3.10
\]

\[
I_{RMS,P} = \sqrt{\frac{\pi^2 I_o^2}{2n^2} \left(\frac{T_s}{T_s - 2t_d}\right)^2 + \left(\frac{V_{in}T_0}{8L_m}\right)^2} \quad 3.11
\]
From the equation, it is easy to tell that when deadtime is increasing or $L_m$ decreasing, the overall RMS current will increase.

Increasing deadtime or decreasing magnetizing inductance help to reduce the turn on loss. However, smaller magnetizing inductance leads to larger circulating and RMS current in the circuit. Longer deadtime also leads to higher RMS current. Both methods will cause larger conduction loss in the circuit. The $L_m$ and $t_{\text{dead}}$ selection is actually a trade-off between switching loss and conduction loss.

During normal operation, the current through primary side MOSFET can be represented as

$$i_{P1}(t) = \begin{cases} i_{r,p}(t), & 0 \leq t \leq T_s/2 \\ 0, & T_s/2 \leq t \leq T_s \end{cases}$$

RMS current in MOSFET during line frequency cycle can be calculated as

$$I_{P1,\text{RMS}}(t) = \sqrt{2f_{\text{line}} \int_{0}^{T_s/2} i_{P1}(t)^2 dt}$$

RMS current on secondary MOSFET can be calculated with similar equations.

The on-state resistance, $R_{on}$, and thermal models of 15 kV SiC MOSFET can be found in [22] for conduction loss calculation.

Loss on MOSFETs can be derived based on the following equations.

$$P_{MV,\text{con}} = I_{RMS,QP}^2 R_{ds,\text{on,MV}}$$

$$P_{LV,\text{con}} = I_{RMS,QS}^2 R_{ds,\text{on,LV}}$$

The overall semiconductor loss versus magnetizing inductance and deadtime are depicted in Figure 3-18. This figure is based on 7.2 kV, 13 kW, and 40 kHz conditions. When $t_{\text{dead}}$ is
short and $L_m$ is large, overall loss increases as turn on loss increases. Conversely, when $t_{dead}$ is long and $L_m$ is small, overall loss is also high due to the increasing of conduction loss.

Optimized parameters can be chosen based on Figure 3-18, and the $L_m$ and $t_{dead}$ values are selected as 20 mH and 1.5 $\mu$s respectively for the 15 kV SiC MOSFET based primary side.

![Figure 3-18 Total CFSRC semiconductor loss versus magnetizing inductance and deadtime.](image)

### 3.4.2 Transformer Loss Calculation

For cost and performance considerations, E100/28/60 ferrite core is selected to build the transformer. Inside structure design is made in order to support higher than 20 kV primary to
secondary insulation. High voltage insulation Litz wire are used on the MV side to support high layer to layer insulation requirement.

Figure 3-19 shows the transformer hardware.

![Figure 3-19 Transformer](image)

The voltage-second added on the transformer primary side is

\[ \gamma(t) = \frac{1}{2} |V_{inac}(t)| \frac{T_{sw}}{2} \]  \hspace{1cm} (3.16)

The associated flux density can be calculated as

\[ \Delta B_{\text{peak}}(t) = \frac{\gamma(t)}{2N_pA_{eT}} \]  \hspace{1cm} (3.17)

For the selected R material, the core loss equation can be found in the manufacture brochure.

\[ P_{CT}(t) = \frac{3.53f^{1.42}\Delta B_{\text{peak}}(t)^{2.88}}{1000} mW/cm^3 \]  \hspace{1cm} (3.18)
Since the input voltage is a sinusoidal waveform. The flux versus time also shows a half sinusoidal shape as shown in Figure 3-21.

The core loss equation is listed as

\[ P_{\text{core}} = P_{C_{T, \text{avg}}} V_{T} N_{\text{pair}} \]  

3.19
Winding loss can also be calculated with following equations.

\[
R_{tp,dc} = \frac{MLT \ast N_p}{S_{eqp}} \tag{3.20}
\]

\[
R_{tp,ac} = 1.5R_{tp,dc} \tag{3.21}
\]

\[
R_{ts,dc} = \frac{MLT \ast N_s}{S_{eqs}} \tag{3.22}
\]

\[
R_{ts,ac} = 1.5R_{ts,dc} \tag{3.23}
\]

\[
P_{winding} = I_{RMS,Tp}^2 \ast (R_{tp,dc} + R_{tp,ac}) + I_{RMS,TS}^2 \ast (R_{ts,dc} + R_{ts,ac}) \tag{3.24}
\]

3.5 Device Switching Frequency and Power Utilization

Previous results show that switching loss on MV device is almost zero with proper \(L_m\) and deadtime design. This indicates that potentially higher switching frequencies can be realized with this MOSFET. The currently selected deadtime of 1.5 \(\mu\)s is 6% of the switching duty cycle. With given deadtime, increasing switching frequency will lead to higher RMS current and result in larger conduction loss. The SiC MOSFET on-resistance model can be found in [22]. When the 15 kV SiC MOSFETs are mounted on a heatsink without fan, with overall junction to air thermal resistance is 1.5 \(^\circ\)C/W.

The ceiling on the switching frequency is decided by the deadtime and conduction loss. Deadtime is set to be constant at 1.5us for ZVS operation. As can be seen from equation (.), as switching frequency goes higher, the equivalent RMS current through device goes higher at same load condition, which contributes to larger conduction loss and higher die temperature.
In our case, frequency ceiling is set at 100 kHz as a tradeoff between power and switching frequency.

![AC-AC Resonant Converter Using 15kV SiC MOS](image)

Figure 3-22 15kV SiC MOSFET junction temperature versus power with different $f_s$ and $V_{MV}$.

To fully utilize the 15 kV SiC MOSFETs in direct AC-AC application based on the switching and conduction model, a series of optimized designs are provided in Figure 3-22 with the $V_{MV}$ ranging from 3.6 to 7.2 kV AC and the switching frequency, $f_s$, from 20 to 100 kHz. Each point in Figure 3-22 represents an optimized pair of magnetizing inductance and
deadtime design that minimized the overall losses on the MV SiC MOSFETs in the system. It illustrates that a potential switching frequency of 100 kHz and a power over 20 kW can be achieved based on this device at 7.2 kV condition.

3.6 Conclusion

This chapter revisited the characterizations of 15 kV SiC MOSFET thoroughly including switching, $R_{on}$, thermal and output charge model based on our package. Single die package is selected to reduce output charge. Paralleled JBS is not needed since with proper ZVS design, no freewheeling diode will flow through body diode of MOSFET.

ZVS design of 15 kV SiC MOSFET is studied and analyzed under wide input voltage range condition 0 to 10 kV). Constant deadtime strategy is select for control simplification. When proper deadtime is selected, ZVS can be realized at high voltage. Partial discharge occurs at low voltage but only neglectable associate switching loss will be generated.

System parameters including $L_m$ and $t_{dead}$ are optimized based on tradeoff between turn on loss and conduction loss. Optimal SST parameters are selected.

To fully utilize the potential of the switching and power capability of a single die 15 kV SiC MOSFET, a device utilization figure is developed. It illustrates that a potential switching frequency of 100 kHz and a power over 20 kW can be achieved based on this device at 7.2 kV condition.
Chapter 4. Over-load and Short Circuit Current Limiting of the Proposed CFSRC

4.1 Introduction

4.1.1 Introduction to Fault Current Limitation in MV Applications

The ability to protect the power system from load disturbances is another function that distinguishes SSTs from the conventional low frequency transformer. Fault current limiting capability is a very desired property in MV applications.

In MV distribution systems, when short circuit happens, the current under this circumstance is a function of the voltage and the inductance reactance of the distribution system. Utilities normally manage fault current by means of specifying a higher impedance substation transformer, or by removing part of the circuit with open tie [55]. Adding reactor is an additional option to limit currents. However, it is not cost effective to increase the inductance reactance to too high merely for short circuit current limiting purpose. In addition, increasing impedance will affect the system stiffness performance and other performance including voltage sag, harmonic and voltage regulation [56].

Several advanced fault current limiter (FCL) devices have been designed and introduced into grid. (1) Impedance insertion FCLs include arrester, saturating reactor and superconducting elements. (2) Switching action FCLs solid stage FCL [60].
After fault happens, conventional AC system or newly designed SSTs need mechanical or power electronics based circuit breaker to interrupt fault current, which could take several line voltage cycles.

A SST with inherent current limiting capability can bring fundamental changes in how we design the feeder protection system. This dissertation proposes a novel solution into direct AC-AC system, which enables cycle by cycle current limiting even under short circuit conditions. In this chapter, the operation principle of the proposed circuit under over load and short circuit conditions will be studied and analyzed in detail.

4.1.2 SRC Current Limit Review

For series resonant converters, the switching frequency is normally selected close to resonant frequency to enable high efficiency performance. Therefore, the impedance of the resonant tank is close to zero. When over load or short circuit happens, the low impedance will result in extremely large circulating current in the circuit.

Several methods have been proposed in previous works to help VFSRC limit current during over load conditions [57],[58]. The basic concept is limiting the current by increasing the impedance of the resonant tank during over load condition.

One approach to increase the impedance of the resonant is increasing switching frequency. Impedance of the resonant tank is extremely large if switching frequency is pushed to much higher than the resonant frequency, thus limiting the current. However, this method is not applicable in MV applications due to the maximum switching frequency limitation of the MV power semiconductor switches as well as the risk of large amount of hard switching loss.
Furthermore, this method requires sensors to accurately sense the fault condition, which may take several switching cycles before taking action.

Paper [57] shows another effective impedance enhancing method in SRC type of circuit by taking resonant capacitors out of operation during partial of time. This can be done by paralleling diode with the resonant capacitors. Figure 4-1 and Figure 4-2 shows two typical circuits.

Figure 4-1 VFSRC with split resonant cap and diodes at output side

Figure 4-2 VFSRC with split resonant cap and diodes at input side
With this method, it is possible to realize cycle by cycle current limiting. During normal operation, the impedance of the resonant is close to zero since switching frequency is selected around the resonant frequency. Whenever short circuit happens at the output side, the resonant capacitors will be bypassed by their paralleled diodes. AC equivalent circuit after short circuit shows that only resonant inductor remains in the circuit. The high impedance of the resonant inductor helps limit the current. This method shows a faster response since once output is shorted, capacitors are bypassed immediately, enables cycle by cycle current limiting.

In the proposed direct AC-AC circuit, the case is relatively different and several challenges exist when apply the diode clamping method. 1) The proposed CFSRC is different from VFSRC, operation principle of the CFSRC under overload conditions needs more analysis. 2) Resonant capacitors are distributed on both sides of the transformer. It is not cost effective to parallel MV diodes on MV side only for OCP concern.

4.2 Proposed CFSRC with Inherent Current Limitation

4.3 Circuit Configuration

The proposed half bridge CSSRC converter is shown in Figure 4-3, which contains only two MV MF switches. The resonant capacitors are split into two pairs of twin capacitors and distributed symmetrically on MV and LV sides.

Two low voltage diodes-$D_1$ and $D_2$ are paralleled on LV resonant capacitors for OCP. Resonant capacitor $C_{rp1}$ and $C_{rp2}$ are designed intentionally larger then $C_{rs1}$ and $C_{rs2}$ for two reasons, 1) achieving higher resonant tank impedance during over load condition to limit the circuit current 2) decrease the ripple voltage on $C_{rp1}$ and $C_{rp2}$ to decrease the voltage stress on
MV devices $P_1$ and $P_2$. During an overload condition, the LV resonant capacitors are bypassed by the diode to increase the resonant tank impedance and, thus, limit the current.

Figure 4-3 Proposed CFSRC with split resonant cap on both side and clamping diodes at output side
Figure 4-4 Operation waveforms under over load condition
Figure 4-5 Operation waveforms under over load condition
4.3.1 Operation Principle under Over Load Condition

Figure 4-4 presents the detailed operation waveforms under over load condition.

The average voltage on capacitors equals to half of the output voltage, which will not increase with load increasing. Under over load conditions, both the resonant currents that flow into $C_{rs1}$ and $C_{rs2}$ increase. The ripple voltage on $C_{rs1}$ and $C_{rs2}$ will increase with the increasing load. During operation, once $V_{cr1}$ or $V_{cr2}$ are discharged to zero and tends go negative, the paralleled diodes $D_1$ and $D_2$ start conducting. $C_{rs1}$ and $C_{rs2}$ will therefore be bypassed.

Primary switches $P_1$ and $P_2$ operate in complement mode. Only half of the switching cycle operation will be discussed in this dissertation since waveforms are symmetric.

Mode 1 [$t_0 \sim t_1$]: This mode begins when the $I_{rs}$ reaches zero and starts to increase in positive direction. Voltage added on primary side of resonant tank is $v_{tp} = -v_{crp2}$. $I_{rs}$ is clamped by output current $I_o$, $C_{rs2}$ is linearly discharged with the output current. $I_{rs}$ is increasing but still lower than $I_o$. $D_1$ conducts the current difference between $I_{rs}$ and $I_o$, thus the voltage on $C_{rs1}$ is clamped at zero during this interval. Voltage on $C_{rs1}$ is always zero. This mode ends when $V_{cr2}$ is discharged to zero.

Equivalent circuit in this mode is shown in Figure 4-5 (a), with which equations can be derived as

$$\frac{dv_{crp}(t)}{dt} = \frac{1}{C_{rp}}(I_{in} - i_{rp}(t))$$  \hspace{1cm} 4.1

$$\frac{dv_{crs}(t)}{dt} = \frac{1}{L_{r,eq}}v_{crs}(t)$$  \hspace{1cm} 4.2

Where the initial conditions are $i_{rp}(t_0) = 0$, $v_{crp1}(t_0) = v_{crp}(t_0)$, $v_{crs1}(t_0) = 0$
Result differential equation is derived as

$$\frac{d^2 i_{rp}(t)}{dt^2} + \frac{i_{rp}(t)}{L_{r_{eq}}C_{rp}} = \frac{1}{L_{req}} \frac{I_{in}}{C_{rp}}$$  \hspace{1cm} 4.3$$

This equation is solved with common solutions

$$i_{rp}(t) = -I_{in} \cos(\omega_{r1}(t - t_0)) + \frac{v_{crp}(t_0)}{Z_{r1}} \sin(\omega_{r1}(t - t_0)) + I_{in}$$  \hspace{1cm} 4.4$$

$$v_{crp}(t) = I_{in}Z_{r1} \sin(\omega_{r1}(t - t_0)) + v_{crp}(t_0) \cos(\omega_{r1}(t - t_0))$$  \hspace{1cm} 4.5$$

Where $\omega_{r1} = \frac{1}{\sqrt{L_{r_{eq}}C_{rp}}}$, $Z_{r1} = \sqrt{\frac{L_{r_{eq}}}{C_{rp}}} = L_{r_{eq}} \omega_{r1} = \frac{1}{\omega_{r1}C_{rp}}$

Mode 2 [$t_1 \sim t_2$]: This mode begins when the voltage on $C_{rs2}$ is discharged to zero. $D_2$ start to conduct. Since the resonant current $I_{rs}$ is still lower than $I_o$, $D_1$ still conducts and the equivalent circuit is shown in Figure 4-5 (b), which is the same with mode 1. During this time interval, the current and voltage equation is same with those in mode 1. This mode ends when $I_{rs}$ equals $I_o$.

Mode 3 [$t_2 \sim t_3$]: At time $t_2$, $I_{rs}$ equals to $I_o$ in value, $D_1$ is disabled and current start to flow into $C_{rs1}$. $C_{rs1}$ joins the resonant and $I_{rs}$ resonant to higher value. The equivalent circuit model is drawn in Figure 4-5 (c), which is same with the normal load operation.

Initial conditions for this mode are $i_{rp}(t_2) = 0$, $v_{crp1}(t_2) = v_{crp1}(t_2)$, $v_{crs1}(t_2) = 0$

Operation equation for this mode are derived

$$\frac{dv_{crp1}}{dt} = \frac{1}{C_{rp}} (I_{in} - i_{rp}(t))$$  \hspace{1cm} 4.6$$

$$\frac{dv_{crs1}}{dt} = \frac{1}{C_{rs1}} (n_i_{rp}(t) - I_o)$$  \hspace{1cm} 4.7$$
\[
\frac{di_{rp}(t)}{dt} = \frac{1}{L_{r,eq}} v_{crp1}(t) - \frac{1}{L_{r,eq}} v_{crs1}(t)
\]  

4.8

Which will result in

\[
\frac{d^2i_{rp}(t)}{dt^2} + \frac{i_{rp}(t)}{L_{r,eq}C_{eq}} = \frac{1}{L_{r,eq}} \frac{I_{in}}{C_{rp}} + \frac{I_{o,eq}}{L_{r,eq}C_{rs}}
\]  

4.9

Assume the relationship between primary and secondary side capacitors are

\[
\frac{C_{rs,eq}}{C_{rp} + C_{rs,eq}} = k_1 \quad \frac{C_{rp}}{C_{rp} + C_{rs,eq}} = k_2
\]  

4.10

\[C_{eq} = k_1 C_{rp} \quad C_{eq} = k_2 C_{rs,eq}\]

Equation (4.9) is formed into (4.10)

\[
\frac{d^2i_r(t)}{dt^2} + \omega_r^2 i_r(t) = \omega_r^2 (k_1 I_{in} + k_2 I_{o,eq})
\]  

4.11

Where \(C_{eq} = \frac{C_{rp} C_{rs,eq}}{C_{rp} + C_{rs,eq}} \omega_r = \frac{1}{\sqrt{L_{r,eq} C_{eq}}} Z_r = \frac{L_{r,eq}}{C_{eq}} = L_{r,eq} \omega_r = \frac{1}{\omega_r C_{eq}}\)

Common solution of the resonant current and capacitor voltage are derived in (4.12) and (4.13).

\[i_{rp}(t) = k_1 (I_{o,eq} - I_{in}) \cos(\omega_r(t - t_2)) + \frac{v_{crp}(t_1)}{Z_r} \sin(\omega_r(t - t_2)) + k_1 I_{in} + k_2 I_{o,eq}\]  

4.12

\[v_{crp1}(t) = -k_1^2 (I_{o,eq} - I_{in}) Z_r \sin(\omega_r(t - t_2)) + k_1 v_{crp}(t_1) [\cos(\omega_r(t - t_2))]\]  

4.13

\[+ \frac{k_2 (I_{in} - I_{o,eq}) (t - t_2)}{C_{rp}} + k_2 v_{crp}(t_2)\]
\[ v_{crs1}(t) = k_1 k_2 Z_r (l_{o_{eq}} - l_{in}) \sin(\omega_r(t - t_2)) - k_2 v_{crp}(t_1)[\cos(\omega_r(t - t_2)) - 1] \quad 4.14 \]
\[ + \frac{k_1(l_{in} - l_{o_{eq}})(t - t_2)}{C_{rs}} \]

Mode 4 \([t_3 \sim t_4]\): \(P_1\) is turned off at time \(t_3\), the primary current has to go through the body diode of \(P_2\), the voltage that is added on the primary \(v_{tp} = -v_{crp2}\). This sudden change of voltage direction force \(i_{rs}\) to decrease rapidly. This mode ends when \(i_{rs}\) equals to zero.

Equivalent circuit for mode 4 is shown in Figure 4-5 (d) and equations are derived as

\[ \frac{d v_{crp2}(t)}{dt} = \frac{1}{C_{rp}} (l_{in} + i_{rp}(t)) \quad 4.15 \]
\[ \frac{d v_{crs1}(t)}{dt} = \frac{1}{C_{rs}} (i_r(t) - l_0) \quad 4.16 \]
\[ \frac{d i_{rp}(t)}{dt} = - \frac{1}{L_{r_{eq}}} v_{crp2}(t) - \frac{1}{L_{r_{eq}}} v_{crs1_{eq}}(t) \quad 4.17 \]

Equation (12) is formed into (13)

\[ \frac{d^2 i_r(t)}{dt^2} + \omega_r^2 i_r(t) = \omega_r^2 (-k_1 l_{in} + k_2 l_{o_{eq}}) \quad 4.18 \]

Common solutions are derived

\[ i_{rp}(t) = (i_{rp}(t_3) + k_1 l_{in} - k_2 l_{o_{eq}}) \cos(\omega_r(t - t_3)) \]
\[ - \frac{v_{crp2}(t_3) + v_{crs2_{eq}}(t_3)}{Z_r} \sin(\omega_r(t - t_3)) - k_1 l_{in} + k_2 l_{o_{eq}} \quad 4.19 \]
\[ v_{crp2}(t) = k_1 \left( (i_r(t_3) + k_1 l_{in} - k_2 l_{o_{eq}}) Z_r \sin(\omega_r(t - t_3)) + k_1 v_{crp2}(t_3) \right) \]
\[ + v_{crs2_{eq}}(t_3) [\cos(\omega_r(t - t_3)) - 1] + \frac{k_2 (l_{in} + l_{o_{eq}})(t - t_3)}{C_{rp}} + v_{crp}(t_3) \quad 4.20 \]
\[
v_{crs1eq}(t) = k_2 Z_r (i_r(t_3) + k_1 l_{in} - k_2 l_{eq}) \sin(\omega_r(t - t_3))
\]
\[
+ k_2 \left( v_{crp2}(t_3) + v_{crs2eq}(t_3) \right) \left[ \cos(\omega_r(t - t_3)) - 1 \right]
\]
\[
- \frac{k_1 (l_{in} + l_{eq})(t - t_3)}{C_{rs}} + v_{crs1}(t_3)
\]

The operation current for all these four modes can be summarized as

\[
i_{crp}(t) = \begin{cases}
-l_{in}\cos(\omega_r(t-t_0)) + \frac{v_{crp1}(t_0)}{Z_{r1}}\sin(\omega_r(t-t_0)) + l_{in}, t \in [0, t_2] \\
k_1 (l_{eq} - l_{in})\cos(\omega_r(t-t_2)) + \frac{v_{crp1}(t_2)}{Z_r}\sin(\omega_r(t-t_2)) + k_1 l_{in} + k_2 l_{eq}, t \in [t_2, t_3] \\
(i_{rp}(t_3) + k_1 l_{in} - k_2 l_{eq})\cos(\omega_r(t-t_3)) - \frac{v_{crp2}(t_3) + v_{crs2eq}(t_3)}{Z_r}\sin(\omega_r(t-t_3)) - k_1 l_{in} + k_2 l_{eq}, t \in [t_3, t_4] \\
\end{cases}
\]

\[
v_{crp1}(t) = \begin{cases}
-l_{in}Z_{r1}\sin(\omega_r(t-t_0)) + v_{crp1}(t_0)\cos(\omega_r(t-t_0)), t \in [0, t_2] \\
k_1 l_{in}Z_r\sin(\omega_r(t-t_2)) + k_1 v_{crp1}(t_2)[\cos(\omega_r(t-t_2)) - 1] + \frac{k_2 (l_{in} - l_{eq})(t - t_2)}{C_{crp}} + v_{crp1}(t_2), t \in [t_2, t_3] \\
-\frac{k_1^2 (l_{eq} - l_{in})Z_r \sin(\omega_r(t-t_2))}{C_{crp}}, t \in [t_3, t_4] \\
\end{cases}
\]

\[
v_{crs1eq}(t) = \begin{cases}
0, t \in [0, t_2] \\
k_1 k_2 Z_r (l_{eq} - l_{in})\sin(\omega_r(t-t_3)) - k_2 v_{crs1}(t_3)[\cos(\omega_r(t-t_3)) - 1] + \frac{k_1 (l_{in} - l_{eq})(t - t_3)}{C_{rs}}, t \in [t_2, t_3] \\
+ k_2 Z_r (i_{rp}(t_3) + k_1 l_{in} - k_2 l_{eq})\sin(\omega_r(t-t_3)) + k_2 \left( v_{crp2}(t_3) + v_{crs2eq}(t_3) \right) \left[ \cos(\omega_r(t - t_3)) - 1 \right] - \frac{k_1 (l_{in} + l_{eq})(t - t_3)}{C_{rs}} + v_{crs2eq}(t_3), t \in [t_3, t_4] \\
\end{cases}
\]

The operation principle of the overload conditions is complex. Short circuit is the worst case when overload happens. If the peak current during short circuit can meet the peak current requirement, then there won’t be current problem in overload condition.

### 4.3.2 Operation Principle under Short Circuit Condition

Short circuit is the worst case when a fault happens. The detailed operation waveforms of the proposed circuit under this condition are depicted in Figure 4-6.
The equivalent circuit during time \([t_1 \sim t_2]\) at short circuit condition is given in Figure 4-7. During this interval, since the output voltage is short to zero, the secondary side capacitors are bypassed by their paralleled diodes. The equivalent differential equation during this interval is in (4.22) where \(\omega_{r1} = \frac{1}{\sqrt{L_r C_{rp}}}\). Only the primary side resonant capacitors remain in the circuit.

\[
\frac{d^2 i_{rp}(t)}{dt^2} + \frac{i_{rp}(t)}{L_r C_{rp}} = \frac{i_{Lin}}{L_r C_{rp}}
\]  

4.22

Figure 4-6 Operation waveforms under short circuit condition.
Under short circuit condition, there is no power transferred to the output, so the input current is close to zero and can be neglected. Therefore, equation (4.22) can be simplified into (4.23).

\[
\frac{d^2 i_{rp}(t)}{dt^2} + \frac{i_{rp}(t)}{L_r C_{rp}} = 0
\]

The common solution for (4.23) is derived in (36) and (37). To solve these equations, initial conditions \(i_r \left( \frac{T_s}{2} \right) = I_r, \ v_{crp} \left( \frac{T_s}{2} \right) = V_{crp,t0}\), and charging balancing of the capacitors in (38) are used.

\[
i_{rp}(t) = -I_{r,t0} \cos(\omega_{r1}(t - t_0)) + \frac{V_{crp,t0}}{Z_{r1}} \sin(\omega_{r1}(t - t_0))
\]

\[
v_{crp}(t) = I_{rp,t0}Z_{r1} \sin(\omega_{r1}(t - t_0)) + V_{crp,t0} \cos(\omega_{r1}(t - t_0))
\]

\[
\int_{t_0}^{t_0 + \frac{T_s}{2}} \left[ I_r Z_{r1} \sin(\omega_{r1}(t - t_0)) + V_{crp,t0} \cos(\omega_{r1}(t - t_0)) \right] dt + \frac{T_s}{2} V_{crp,t0} = \frac{V_{in}}{2} T_s
\]

If we set the relationship between primary and total equivalent capacitor to be \(C_{rp} = k C_{req}\), (39) is derived based on results from Section II.
\[ \varphi(k) = \omega_r \left( \frac{T_s}{2} \right) = \frac{1.292\pi}{\sqrt{k}} \quad 4.27 \]

The peak current of primary side versus the input voltage and coefficient \( k \) can be derived as

\[ I_{\text{peak}}(k) = \frac{V_{\text{in}} \sin(\varphi(k))}{Z_{r1}} \left( 1 + \cos(\varphi(k)) \right) + \frac{2\sin(\varphi(k))}{\varphi(k)} \quad 4.28 \]

where \( Z_{r1} = \sqrt{\frac{L_r}{C_{rp}}} \)

Equation (40) dictates the design criteria for short circuit current limiting, in particular the resonant tank components, \( L_r \) and \( C_r \). The peak current under short circuit depends on the \( L_r \) value and distribution of the resonant capacitors.

Figure 4-8 shows the peak current curves versus the \( k \) value under different voltage conditions. Increasing \( k \) helps reduce the peak current at short circuit conditions. If \( k \) and \( L_r \) are designed properly, current can be limited within desirable range.

However, increasing \( k \) will result in larger capacitor values and leads to higher reactive power.

The equivalent capacitance of resonant capacitors that contributes to reactive power can be calculated in equation

\[ C_{\text{reactive}} = 0.5(C_{rp} + C_{rs,eq}) = 0.5 \frac{k^2}{k - 1} C_{req} \quad 4.29 \]

Result reactive power caused by resonant capacitors is

\[ Q = \frac{V_{\text{ac}}^2}{X_c} = 0.5 \frac{k^2}{k - 1} C_{req} V_{\text{ac}}^2 \omega_{\text{line}} \quad 4.30 \]
$k$ is selected to be 4 in this design, with an excepted peak current around 33 A at 10 kV peak voltage condition.

![Graph showing peak current versus $k$ at different peak voltage conditions.](image)

Figure 4-8 Peak current versus $k$ at different peak voltage conditions.

### 4.4 Resonant Tank Design Consideration

The resonant tank design is also important. The system operates at constant frequency that is close to the resonant frequency to achieve high efficiency performance. Two criteria need to be met for proper operation.

1) Resonant Capacitor Design
As mentioned before, the voltage on the secondary resonant capacitors should not exceed the output voltage during normal operation.

\[
C_{rs} \geq \frac{I_{o,peak} T_s}{2 V_{o,peak}}
\]

2) Overload Protection Consideration

\[
L_r \leq \frac{4 \omega_s}{\pi V_{in}} I_{limit}
\]

For the overload protection consideration, a larger inductance value helps reduce the overload peak current. A small short circuit peak current means a large \(L_r\) and leads to a small \(C_r\). However, \(C_r\) cannot be too small as (40) needs to be satisfied.

4.5 Conclusion

This chapter introduced a novel approach that helps the proposed DACX to obtain inherent current limiting capability during overload conditions. Inherent cycle by cycle current limiting is achieved by paralleling diodes only on LV resonant capacitors. The operation principle under overload and short circuit conditions are conducted in detail. The equation for peak current calculation under short circuit is also provided for resonant tank design. The calculation result shows that increasing MV resonant capacitance helps reduce peak current under short circuit. A proper coefficient that indicates the distribution of resonant capacitance is selected, with which the peak circulating current is expected to be lower than 35 V under short circuit condition at 10 kV input voltage.
Chapter 5. Hardware Development and Experimental Verification

5.1 Hardware Development

In order to verify the operation principle discussed in previous chapters, a 7.2 kV SST prototype based on two level direct AC-AC structure is designed and developed. The prototype is designed to convert single phase 7.2 kV / 60 Hz input voltage to 240V /60 Hz with a target power of 13 kW. The switching frequency is selected at 40 kHz to achieve high system power density.
System parameters and components are designed and selected based on analysis in Chapter 3 and Chapter 4. Table 5.1 summarizes the key system components and specifications. The prototype uses two 15 kV/10 A SiC MOSFETs on the MF MV side and 1200 V/300 A SiC MOSFETs modules on the HF LV side. Total system equivalent capacitance seen from the input side in the whole system are limited at 48 nF.

The whole control system is based on a DSP TMS320F28377D. Control board is shown in Figure 5-1. All the signals including gate driver, sensing and communication are transferred and received through fiber optic to satisfy high voltage insulation requirement.
Figure 5-2 shows the detailed circuit diagram, which contains only two 15 kV SiC MOSFETs: $P_1$ and $P_2$. The first stage is a MV LF rectifier that converts LF MV AC voltage to a half sine wave. The second stage adopts the half-bridge CFSRC to achieve ZVS operation and minimize the system capacitance. Resonant capacitors are split into two pairs of capacitors and distributed symmetrically on the MV and LV sides. Two diodes, $D_1$ and $D_2$, are paralleled with the LV resonant capacitors for over current protection. Resonant capacitors, $C_{rp1}$ and $C_{rp2}$, are designed intentionally larger than $C_{rs1}$ and $C_{rs2}$ for two purposes: (1) to achieve higher resonant tank impedance during overload condition to limit the circuit current and (2) decrease the ripple voltage on $C_{rp1}$ and $C_{rp2}$ to decrease the voltage stress on MV devices, $P_1$ and $P_2$. The final stage is a LF unfolding stage that converts the LV half sine voltage to LF AC voltage. No TLSS AC-AC converter has been reported with MV experimental results prior to this dissertation. Design is difficult due to limited understanding of the problem.

CONCEPT power supply ISO51251-120 is used to offer DC power for the gates drivers with and isolation capability higher than 12 kV.
Figure 5-2 shows the overall system diagram.

Figure 5-3 shows the state machine designed for the designed SST. There are mainly four states.

**Initials State**: When controller is powered on, the system enters this state. In this state, all the drivers for all stages are at off state. This state is like wait for command state.

**Standby State**: When the system has no error and on off switch is triggered, the system enters this state and waiting for the input voltage to come.

**Normal State**: When the system was in standby state, and the ac input voltage exceed the value it desires, the system will enter normal operation state and all the switches are switching regularly.
Fault State: When the emergency stop button is triggered at any condition, the system enters into fault state and won’t go out unless all fault and voltage are cleared.

Figure 5-6 shows the final assembled system hardware. The SST is assembled into a very compact metal box. In which fiber glass are used to guarantee the insulation among all high voltage points.

The system hardware is packaged within a very compact enclosure with a dimension of 30 inches×24 inches×10.5 inches.
5.1.1 Delta-sigma Based Fiber Optical High Voltage Sensor

For high voltage application, voltage sensing is critical for feedback and protection as the insulation and speed requirements are high. In reference [4], commercial voltage sensor is used to sense the high voltage, which is costly and large in size. To improve the speed and to reduce a cost, a fast voltage sensor based on fiber optical sensor is proposed, which can achieve an isolation capability higher than 10kV with much small size and cost.

A traditional high voltage sensor is shown in Fig. 9, which has a voltage rating of 4.2kVdc and cost $560 each. In this dissertation, a fast voltage sensor based on fiber optical sensor is proposed in Fig.9, which can achieve an isolation capability higher than 15kV with much small
size and cost ($50). The basic idea is using delta-sigma modulator to transfer voltage signal through fiber optics.

Figure 5-4 shows the test result for the proposed high isolation voltage sensor. The sensed signal follows the original signal very well. Even at sharp rising edge, the delay sensing delay is only 70us. In our case, this voltage sensor is used to sense the DC bus voltage and use it for feedback and protection. As the crossing frequency of the voltage loop is set to 10Hz, 70us sensing delay won’t affect the feedback and protection performance.
Figure 5-5 Source signal vs sensed signal by high proposed voltage sensor.

Figure 5-6 Hardware structure of 7.2kV TLSS SST.
5.2 Experimental Verification

5.2.1 Steady State Test

Experiments were carried out to verify analysis and principle in previous chapters.

In the steady state test, the experiments is conducts with an input voltage of 7.2 kV / 60 Hz and output voltage of 240V /60 Hz. The output full load resistance is set to be 4 Ω in order to achieve load of 13 kW.

![Steady state operation waveforms at \( V_{M1} = 7.2 \) kV, \( P_o = 6 \) kW](image)

Figure 5-7 Steady state operation waveforms at \( V_{M1} = 7.2 \) kV, \( P_o = 6 \) kW

Figure 5-7 (a) show the system operation waveforms at 7.2 kV AC, 6 kW condition with the output voltage of 230 V AC. The yellow and purple waveforms are the input voltage and output voltage, respectively. The input and output voltages are in phase.
Figure 5-8 Steady state operation waveforms
Figure 5-9 Steady operation waveforms.
Figure 5-8 (b) (c) show the system operation waveforms at 7.2 kV AC, 13 kW condition with an output voltage of 230 V AC.

Figure 5-9 (a) (b) are the magnified view of the switching cycle waveforms with a switching frequency of 37 kHz. The blue waveform is the $V_{ds}$ voltage of the MOSFET that verifies the ZVS operation at 10kV. Operation waveforms of this prototype under a very light load of 600 W is given in Figure 5-9 (d) in which the ZVS is still well realized. These proves the ZVS capability of LLC type SRC circuit across wide load range.

Efficiency curves of the proposed prototype tested under 3.6 kV and 7.2 kV input voltage conditions are shown in Figure 5-10 (a). An efficiency curve of a Type D SST using the same MOSFETs is added for comparison [28]. The efficiency for the proposed SST at 7.2 kV is shown in red curve and is higher than 97% under most of the load conditions. This figure shows an obvious improvement in efficiency from a Type D topology to Type A topology. Best converter in terms of efficiency.

Loss breakdown under 7.2 kV/12 kW, listed in Figure 5-10 (b), indicates that conduction loss on the LV side needs to be reduced further in order to achieve even higher efficiency.
(a) Measured MV TLSS-SST efficiency, $V_{MI} = 3.6$ & 7.2 kV, $P_o$ from 600 W to 12 kW

367W Calculated Overall Loss @ 7.2kVac/12kW

(b) Converter loss breakdown, $V_{MI} = 7.2$ kV, $P_o = 12$ kW

Figure 5-10 Test efficiency result and loss breakdown
5.2.2 Short Circuit Experimental Verification

In the hardware setup, only one 15 kV / 10 A die is packaged in our module. Under short circuit conditions, the device works under high current turn off condition, which might cause turn off loss. When short circuit happens at 7.2 kV, the turn off current will exceed 30 A, which is not acceptable for a single die device. In experiment, short circuit tests are conducted with a peak voltage of 2 kV and 3 kV.

Figure 5-11 (a) and Figure 5-12 (a) shows the transient moment when short circuit happens. The output voltage is pulled to zero within 1 μs, and the current limiting circuit reacts immediately. The peak current is limited to within 13 A at 3 kV peak voltage as shown in Figure 5-12 (b), which matches the calculated result.

![Figure 5-11 Short circuit waveforms at 3 kV peak input voltage](image-url)
Figure 5-12 Short circuit waveforms at 3 kV peak input voltage - 2
5.3 Conclusion

In this chapter, a fully functional and compact SST that converts 7.2 kV AC to 240 V AC is developed to verify the theoretical analysis in previous chapters. Normal operation is conducted at 7.2 kV input voltage with load condition varies from 1 kW to 12 kW. ZVS operation of MV MOSFETs are achieved over wide load range. This is the highest reported voltage rating for two-level based power converters without device series connection. The achieved efficiency is higher than 97% over wide load range. Short circuit protection is verified at 3 kV peak input voltage condition. The cycle by cycle inherent current capability is verified with a peak MV switch current of 13 A. The peak current under 7.2 kV short circuit condition is expected to be less than 35 A, which is very attractive in MV applications.
Chapter 6. Conclusion and Future Work

6.1 Contributions Summary

To the author’s best knowledge, this is the first time a two level based converter achieve an operation voltage of 7.2 kV without device series. It is also the first time SiC MOSFETs is implemented into MV DACX.

The main contributions of the dissertation are:

In Chapter 2, a novel current fed series resonant converter (CFSRC) is proposed for DACX applications, which helps (1) achieve ZVS operation under wide input voltage and load range conditions, enables switching frequency as high as 100 kHz even under 7.2 kV operation condition. (2) minimize system total required capacitance, which helps improve system power density and enables all film capacitors system for longer life time performance. Analysis of the CFSRC are conducted based on time domain and first harmonic approximation (FHA) methods, providing equations for circuit design.

Chapter 3 revisited the characterizations of 15 kV SiC MOSFETs thoroughly including switching, $R_{on}$, thermal and output charge model based on our package. ZVS design of 15 kV SiC MOSFET is studied and analyzed under wide input voltage range (0 to 10 kV) based on constant deadtime. When proper deadtime is selected, ZVS can be realized at high voltage range. Partial discharge occurs when input voltage is low but only neglectable associate switching loss will be generated. System design and optimization, as well as device utilization are conducted in this chapter, providing comprehensive design guideline for utilizing 15 kV
MOSFETs to its full voltage, switching frequency and power potential in MV DACX application.

Chapter 4 is devoted to the analysis and design of the DACX under overload and short circuit conditions. The calculation results show that the corresponding peak current under overload condition is a function of the voltage, resonant inductance $L_r$ and distribution of the resonant capacitance. Equation for peak current calculation under short circuit is also provided for resonant tank design. Proper resonant tank parameters and distribution of resonant capacitance is designed to achieve low peak current under overload conditions, as well as small generated reactive power. The peak circulating current is expected to be lower than 35 A under short circuit condition at 7.2 kV operation voltage.

Chapter 5 elaborated the system hardware development of a DACX that converts 7.2 kV AC to 240 V AC is developed and tested from 1 kW to 12 kW. ZVS operation of the MV MOSFETs are verified over wide load range. This is the highest reported voltage rating for two-level based power converters without device series connection. The developed SST has achieved a peak efficiency of 97.8 %, which is a significant improvement from previously developed three stage SSTs. 15 kV MOSFET is utilized to reach its full voltage, frequency and power potential of 10 kV, 100 kHz and 20 kW, respectively, in DACX applications. Short circuit is conducted with a peak input voltage of 3 kV, the result peak current of 13 A consistent with thermotical analysis. The peak current under 7.2 kV short circuit condition is expected to be less than 35 A, which is very attractive in MV applications.
6.2 Future Work

The voltage regulation capability and regulating strategy will need to be conducted. Variable frequency control combining phase shift may be attractive to limit frequency range while obtain wide gain capability.

Bidirectional power flow capability of the proposed DACX should be analyzed. A proper power flow control methodology should be proposed.

Experiments on the proposed DACX are conducted with resistive load. This circuit is able to operate under inductive or capacitive load conditions. The operation of the circuit under non-unit power factor needs to be studied and analyzed.
REFERENCES


[14] Li Wang; Qianlai Zhu; Wensong Yu; Alex Huang "A Medium Voltage Medium Frequency Isolated DC-DC Converter Based on 15 kV SiC Mosfets"; IEEE Journal of Emerging and Selected Topics in Power Electronics; Year: 2016, Volume: PP, Issue: 99;Pages: 1 - 1, DOI: 10.1109/JESTPE.2016.2639381


[28] Qianlai Zhu; Li Wang; Liqi Zhang; Wensong Yu; Alex Q. Huang, “Improved medium voltage AC-DC rectifier based on 10kV SiC MOSFET for Solid State Transformer (SST)” Applied Power Electronics Conference and Exposition (APEC) 2016 IEEE Pages: 2365 – 2369.


[46] Li, Xuan; Zhang, Liqi; Guo, Suxuan; Lei, Yang; Huang, Alex Q.; Zhang, Bo, "Understanding switching losses in SiC MOSFET: Toward lossless switching," in Wide Bandgap Power Devices and Applications (WiPDA), 2015 IEEE 3rd Workshop on , vol., no., pp.257-262, 2-4 Nov. 2015


