ABSTRACT

AZAM, FAISAL. AlGaN/GaN MOSHFETs using ALD Dielectrics: A Study in Performance and Reliability. (Under the direction of Dr. Veena Misra).

Gallium Nitride is the most promising semiconductor material for both microwave and power switching applications. Due to its excellent carrier mobility, high current density, high breakdown voltage, and high temperature operation AlGaN/GaN devices are extremely attractive for the next generation of power devices in the 100–650 V range [49]. The increasing demand for more efficient transistors, higher output power density, higher input impedance, and higher blocking voltage potential has led to the research and development of GaN over last two decades. Since the 1st demonstration of a GaN high electron mobility transistor (HEMT) in 1993 [8], GaN-based RF power devices have made substantial progresses including steadily improved growth techniques, material qualities, enhanced processing technologies, and more optimum device designs. More recently, advancement of insulating gate and field-management technologies based on the GaN HEMT structure has resulted in 600 V and above power switching transistors. The trend of the GaN-based device is towards higher output power density, higher Power-Added-Efficiency (PAE), higher operation frequencies and improved reliability. In order to achieve these requirements, novel device designs and processing technologies are being developed.

The greatest impediment for the industry-wide adoption of GaN technology has been, and remains, achieving a high level of reliability and stability concurrently with high performance operation. The focus of my research has been to improve upon these weaknesses and provide a forward momentum for the technology. The devices we worked on were normally-on (depletion-mode), lateral AlGaN/GaN MOSHFET at 600 V rating. This class of device is an important target for

solar inverters, motor drives, electric-vehicle charging, for use in solid state transformer (SST), distributed energy storage devices (DESD), telecom DC-to-DC conversion, and military applications.

We approached from various technological solutions standpoint to address some of the core challenges. In particular, we investigated ALD dielectrics and their impact on the gate and access region of the transistor. The ALD chemistry and effect of oxidants were studied in great detail. We explored effect of annealing ambient on improving traps. Device design considerations were also taken into account and optimized such as, dielectric thickness, gate-to-drain separation, *etc*. We stressed the devices by making them undergo temperature and bias acceleration tests and followed a comprehensive characterization suite to evaluate the health of the device. Our efforts materialized in seeing improvements in several of the performance and reliability metrics. With the enhancements proven in this work and directions suggested, GaN technology not only provides more efficacy and solid potential for the near-term applications but also paves the way for energy internet in the long run.

AlGaN/GaN MOSHFETs using ALD Dielectrics: A Study in Performance and Reliability

by
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DEDICATION

It is to commemorate her unconditional love, affection, and support that I dedicate this dissertation to my mother, *Farida Banu*.

BIOGRAPHY

Faisal Azam was born in Bangladesh. He received his Bachelor's degree in Electrical Engineering from the University of Cincinnati, OH, in 1998 and Masters in Electrical Engineering from Rensselaer Polytechnic Institute, NY, in 2000.

He joined IBM Microelectronics, Fishkill, NY, in year 2000 as a device characterization engineer where he worked on bulk silicon and silicon-on-insulator (SOI) technologies optimizing performance, yield, and reliability objectives. He also played an integrated role in qualifying advanced CMOS logic and eDRAM products from post tape-out through ramp-up until release to production.

In year 2007, Faisal joined Samsung Austin Semiconductor, TX, as a process integration device engineer where he was responsible for test, characterization, qualification and technology transfer of CMOS logic and flash memory devices.

Faisal returned to school in 2014 and pursued Doctor of Philosophy in Electrical Engineering at North Carolina State University. He joined the Future Renewable Electric Energy Delivery and Management (FREEDM) Systems Center as a graduate research assistant under the direction of Dr. Veena Misra. His research focused on improving performance and reliability of AlGaN/GaN MOSHFETs using high-*k* ALD dielectrics.

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Thanks to my mother, Farida Banu, for her unwavering support and compromise. I also want to thank my sisters, Shireen Chowdhury and Sharmeen Hassan, for their encouragement. Finally, thanks to my wife, Tamanna Rahman, for uplifting my spirit when I needed it most.

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CHAPTER 1: Introduction

1.1 Review of GaN Technology

More than half the electricity produced in the USA is one way or another controlled by power semiconductor devices. Qorvo projects that by 2030, as much as 80 percent of the electricity generated will pass through one or more power conversion stages from generation to consumption (a 30 percent increase from today) [1]. This directly translates to a high demand for switching devices. According to Yole Développement, the market for power electronics approaches $18 billion by year 2020 (Figure 1.1) [2]. That's a large industry and there is a lot of competition to provide high performance products at a low cost. The basic requirements for semiconductors used in power conversion are efficiency, reliability, controllability, and cost effectiveness. Without these attributes, a new device structure would not be economically viable.

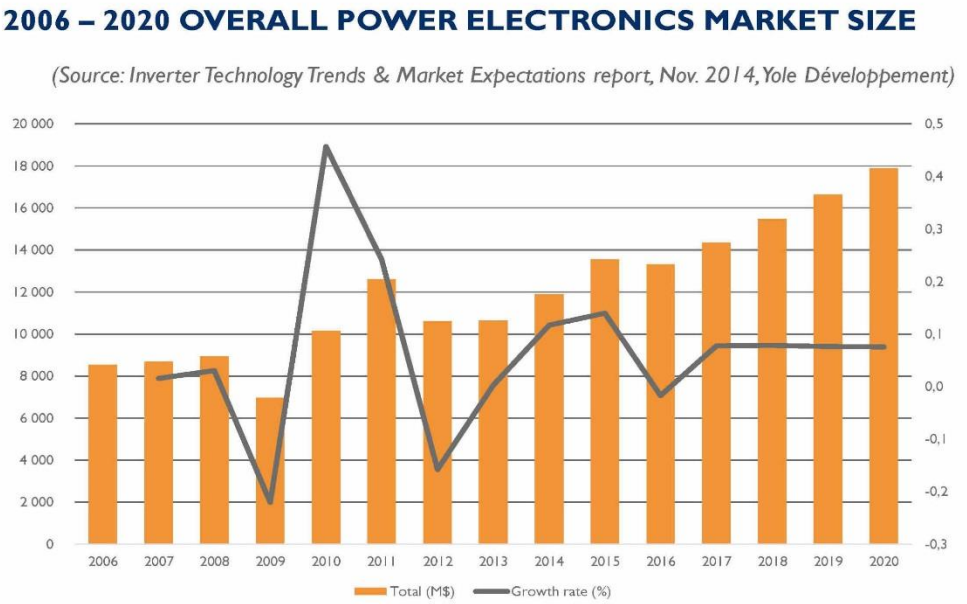


Figure 1.1: Power electronics market expectation by Yole Développement [2].

Silicon is still dominating as a power semiconductor device. However, it is rapidly approaching theoretical limitation making it difficult for further efficiency [1]. There have been efforts to push beyond limits of Si by novel device structures such as, insulated-gate bipolar transistor (IGBT) and superjunction (SJ) MOSFETs [3]. Yet there is an increasing need for devices with higher blocking voltage capacity to be used in domestic appliances, motor drives, hybrid and electric vehicles, railway, and very high power capacity energy transmission. The tradeoff between two most fundamental parameters, specific on-state resistance (R_{on}) and off-state breakdown voltage (BV), is critical for power switching applications. Figure 1.2 shows the theoretical limitation of these metrics for Si, SiC and GaN devices [4]. For a given voltage rating, R_{on} of GaN based devices is nearly three orders of magnitude lower than that of Si and it also surpasses the limit of SiC, indicating its great potential in high voltage and high power density applications.

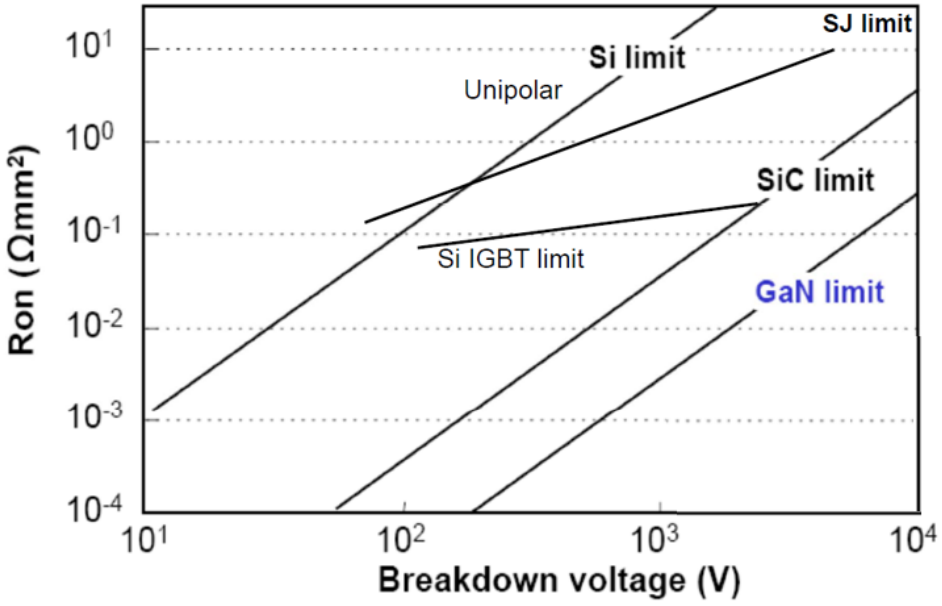


Figure 1.2: Theoretical on-resistance vs. blocking voltage capability for Si, SiC, and GaN based power devices [4].

Ron and BV are related by the equation (1.1) [5] where the denominator, commonly known as Baliga's Figure of Merit (BFOM), is a strong indicator for how suitable a material is for power switching applications.

$$R_{ON} = \frac{4BV^2}{\mu\varepsilon E_c^3} \tag{1.1}$$

where BV is the breakdown voltage, μ is the mobility, ε is the dielectric constant, and E_c is the critical electric field for breakdown.

Table 1.1 also compares various figures of merit of the three semiconductors [6]. The Baliga's Figure of Merit (BFOM) represents the on-state resistive loss, and Baliga's high-frequency figure of merit (BHFFOM) represents switching loss. In Table 1.1, these figures of merit have been normalized to Si performance and are shown for comparison. GaN devices outperform existing Si and SiC devices for most power conversion applications except at extremely high temperatures where SiC trumps all other materials [1].

Table 1.1: Comparison of material parameters of Si, SiC and GaN [6].

	Si	4H-SiC	GaN
Bandgap E_g (eV)	1.1	3.3	3.4
Electric breakdown field E_{CRIT} (MV/cm)	0.3	2.2	3.3
Relative dielectric constant ε_r	11.9	10.1	9
Saturation velocity, v_{sat} (10^7 cm/s)	1	2	3
Electron mobility μ_n (cm^2/V-s)	1350	900	1150 – 2000*
Thermal conductivity λ (W/cm-K)	1.5	4.9	2.3
BFOM ratio ($\alpha\ \mu\varepsilon E_C^3$), relative to Si	1	223	850 – 1480*
BHFFOM ratio ($\alpha\ \mu E_C^2$), relative to Si	1	45	98 – 170*
Max est. operating temperature, Tmax (°C)	200	500	700

Note: * values correspond to two-dimensional electron gas (2DEG) properties at the AlGaN/GaN interface.

It's the wide bandgap (3.4 eV) that allows GaN to have high critical field (> $3x10^6$ V/cm) and stability at high temperatures [10]. GaN having 10 times higher breakdown strength compared to Si means that 10 times the operating voltage can be applied to GaN devices compared to Si devices for a given device dimension. Additionally, the ability to form a high density two-dimensional electron gas (2DEG) in the GaN near the AlGaN/GaN heterointerface by polarization doping allows for very high electron mobility (μ_n) while maintaining a high sheet charge density (n_s) in the drift region [14]. This means lower specific on-state resistance R_{on} which further scales with the length of the device drift region necessary to maintain a given breakdown voltage. The more compact GaN devices feature much lower R_{on} compared to Si devices. Thus, GaN devices enable high breakdown voltages and high current levels simultaneously and feature small semiconductor areas. This essentially translates to high switching frequencies at high power levels. Figure 1.3 shows prospects of wide bandgap (WBG) semiconductor transistors in the high-power, high-frequency domain for near-term applications [7].

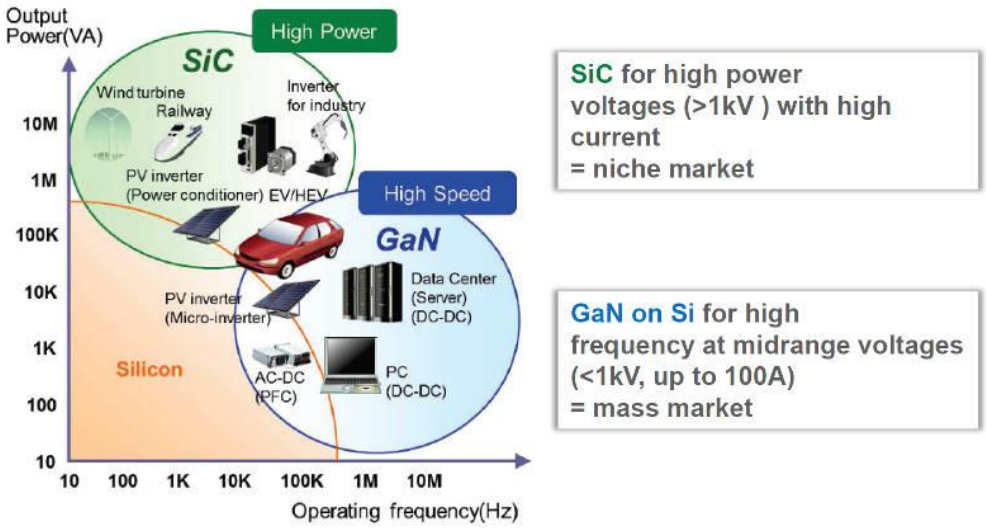


Figure 1.3: Prospects of wide bandgap semiconductor transistors [7].

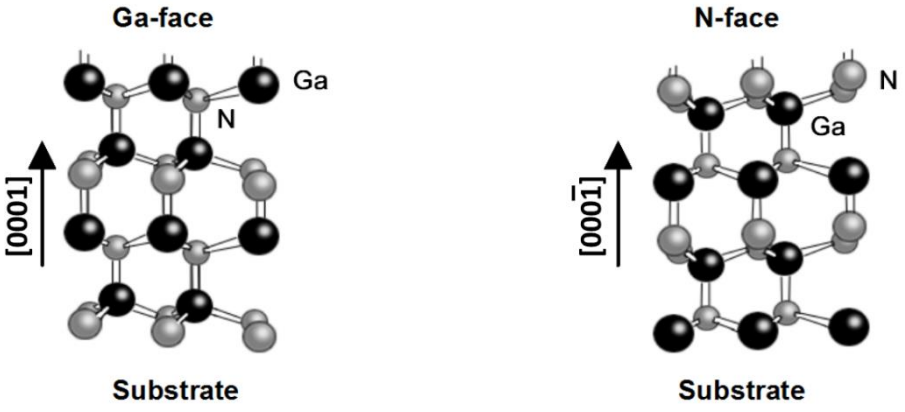
1.2 GaN Crystal Structure and Polarization

GaN can exist in either a cubic crystal structure (zinc blende phase) or a hexagonal (Wurtzite) crystal structure [10], [66], the latter being chemically stable and mechanically robust. The polar hexagonal crystal structure is of most technological interest. More specifically, GaN-based materials has two types of polarization that makes the structure distinctive [14].

1.2.1 Spontaneous polarization, P_{SP}:

This is intrinsic property of the material. There is a strong polar bond between Ga and N atoms. The polarity could be either Ga-faced or N-faced, as shown in Figure 1.4. Currently all high--quality material is grown with Ga polarity in the [0001] direction (*c*-axis) [11]. The polarization is described by equation (1.2) [14].

$$P_{SP}(x) = -0.052x - 0.029 \tag{1.2}$$



(a) (b)

Figure 1.4: The Wurtzite geometric structure of GaN Crystal (a) Ga-faced and (b) N-faced [14].

1.2.2 Piezoelectric polarization, P_{PE}:

This results from mechanical strain between AlGaN/GaN heterojunction layers. When AlGaN is grown on top of GaN, due to lattice mismatch (2.4% difference between AlN and GaN at room temperature [66]), AlGaN biaxially stretches outward causing a tensile strain [117], [126]. This is illustrated in Figure 1.5. The polarization is described by equation (1.3) [14].

$$P_{\mathrm{PE}} = 2\frac{a-a_0}{a_0}\left(e_{31} - e_{33}\frac{C_{13}}{C_{33}}\right) \tag{1.3}$$

where a is the lattice constant of the strained layer, a_0 is the length of GaN hexagonal edge, e_{31} and e_{33} are the piezoelectric coefficients, and C_{13} and C_{33} are elastic constants.

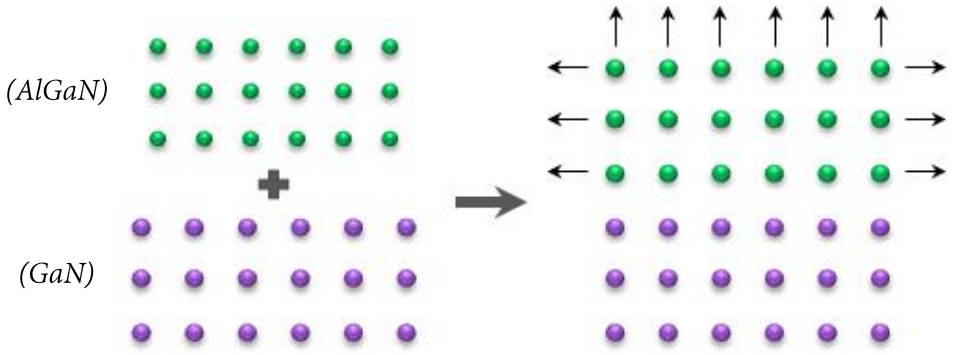


Figure 1.5: Animation depicting AlGaN stretching outward when brought into contact with GaN.

1.2.3 Two-dimensional electron gas (2DEG):

The two polarizations added together results in a net positive charge at the $Al_xGa_{1-x}N$/GaN heterointerface as shown in Figure 1.6(a) [11]. Simultaneously, electrons are attracted at the surface by the positive polarization charge in order to maintain charge neutrality in the structure,

and form 2DEG under the AlGaN barrier. This is shown in Figure 1.6(b). The total polarization charge is given by equation (1.4) [14],

$$\sigma_P = \left(P_{SP} + P_{PE}\right)_{Al_xGa_{(1-x)}N} - \left(P_{SP} + P_{PE}\right)_{GaN} \tag{1.4}$$

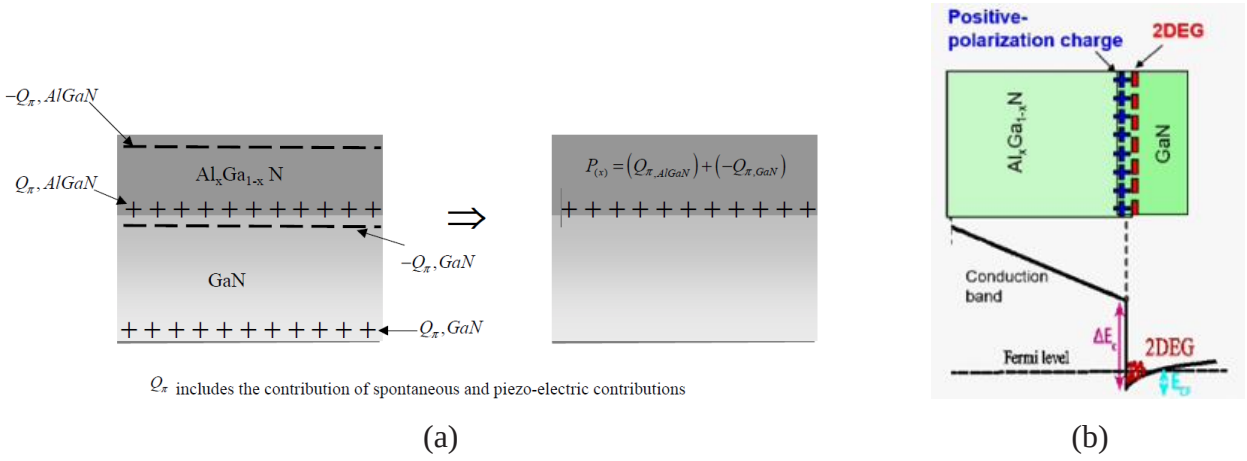


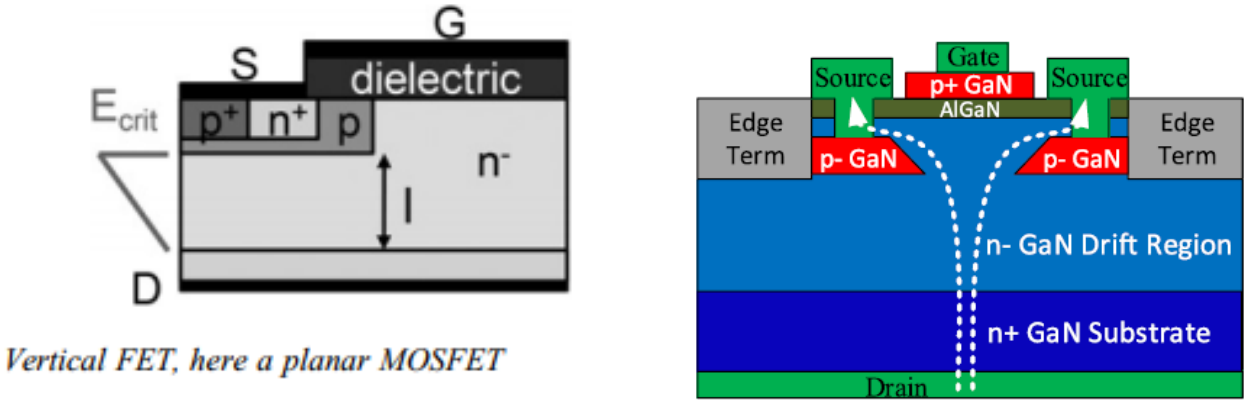
Figure 1.6: (a) Net positive charge at the AlGaN/GaN interface caused by the sum of spontaneous and piezoelectric polarization [11] and (b) 2DEG formation and corresponding conduction band energy profile [95].

The disparate polarization-induced 2DEG effectively reduces on-resistance and thus power loss. A typical sheet carrier density (n_s) of 10^{13} cm^{-2} and electron mobility of 2000 cm^2/V-s have been reported in the 2DEG [9], [14]. The consequential high concentration of electrons with very high mobility makes AlGaN/GaN heterostructure a high electron mobility transistor (HEMT). Confinement of the 2DEG close to the interface and n_s are sensitive to different physical properties such as, AlGaN composition, polarity, strain, barrier thickness, *etc*. Brown *et al.* [90] has cited, for 25% Al-content, the critical thickness beyond which 2DEG forms is around 6 nm.

1.3 GaN Transistors

1.3.1 Vertical GaN FET:

Usually, the choice for a high power device is a vertical drift region. The R_{on} is much lower. Also, since the high electrical field of the active area does not reach the surface, BV achieved can be much higher (> 1200V) [124]. Additionally, the vertical architecture virtually eliminates current collapse, while enhancing switching speeds and thermal handling capabilities [1]. However, the vertical devices necessitate high quality, thick epitaxial layers, and conductive substrates as well as a conductive interface [124]; *i.e.*, a homo-epitaxy on expensive bulk GaN. Hence, lateral FET is a more pragmatic solution.



(a) (b)

Figure 1.7: (a) Vertical FET [124] and (b) Vertical GaN-on-GaN normally-off JFET [50].

1.3.2 Lateral GaN HEMT:

Most of the GaN devices available today are lateral heterojunction field-effect transistors (HFETs), also known as high electron mobility transistors (HEMTs) [50]. Figure 1.8 shows cross-section of a lateral GaN HEMT which can be grown on sapphire, SiC, or Si, with Si providing the most cost

effective option. The AlGaN/GaN structure creates 2DEG with a high sheet carrier density ($1x10^{13}$ cm^{-2}) and a high electron mobility (2000 cm^2/V-s) [9] which effectively produces a low specific on-resistance. However, because of the native 2DEG channel, the HFET is inherently a depletion-mode (normally-on) device. Another weakness of the HEMT structure is high gate leakage. Also, AlGaN surface states and traps in the access regions increase the dynamic on-state resistance [50].

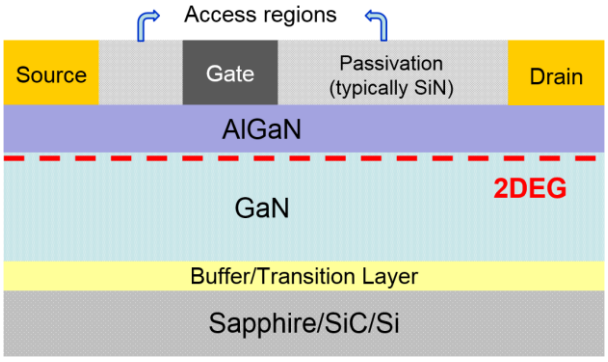


Figure 1.8: Cross-section of a lateral GaN HEMT (not drawn to scale).

For lateral GaN HEMTs with GaN-on-silicon epiwafers, operating voltages are typically limited to 650 V or less [1]. For higher voltage applications, switching from silicon to SiC substrates overcomes this limitation. However, other than the increased cost due to expensive substrate, the lateral device size also needs to be increased to support higher voltages. In which case, superior vertical device architecture provides a better option.

1.4 GaN HEMT Operation Mode

Zero bias: When gate bias (V_{GS}) = drain bias (V_{DS}) = 0V, with the 2DEG present.

On-state: When V_{DS} applied, current starts to flow between source and drain. The exact mechanism of conduction through the AlGaN layer is unknown. However, after annealing, a strong structural changes occur in the Ti/Al/Ni/Au metal stack, and a Schottky to ohmic transition is observed in the temperature range of 600–800 °C. Commonly, it is assumed that the formation of a TiN metallic compound during annealing, driven by the outdiffusion of nitrogen atoms from GaN, leaves behind high concentration of nitrogen vacancies below the interface, causing the GaN to be heavily doped n-type [115], [128]–[130]. Thus favoring the tunneling process of electrons through the AlGaN barrier and ohmic contact formation.

Off-state: A sufficiently negative V_{GS} needs to be applied to the gate to deplete the 2DEG underneath. This condition is also referred to as pinch-off.

Blocking mode: This is a more realistic situation when devices are used in power switching applications. The biasing condition is similar to off-state with a much higher bias applied to the drain. This forms a virtual gate which causes additional depletion of 2DEG in the drift region. The high voltage is supported by the space between gate and drain.

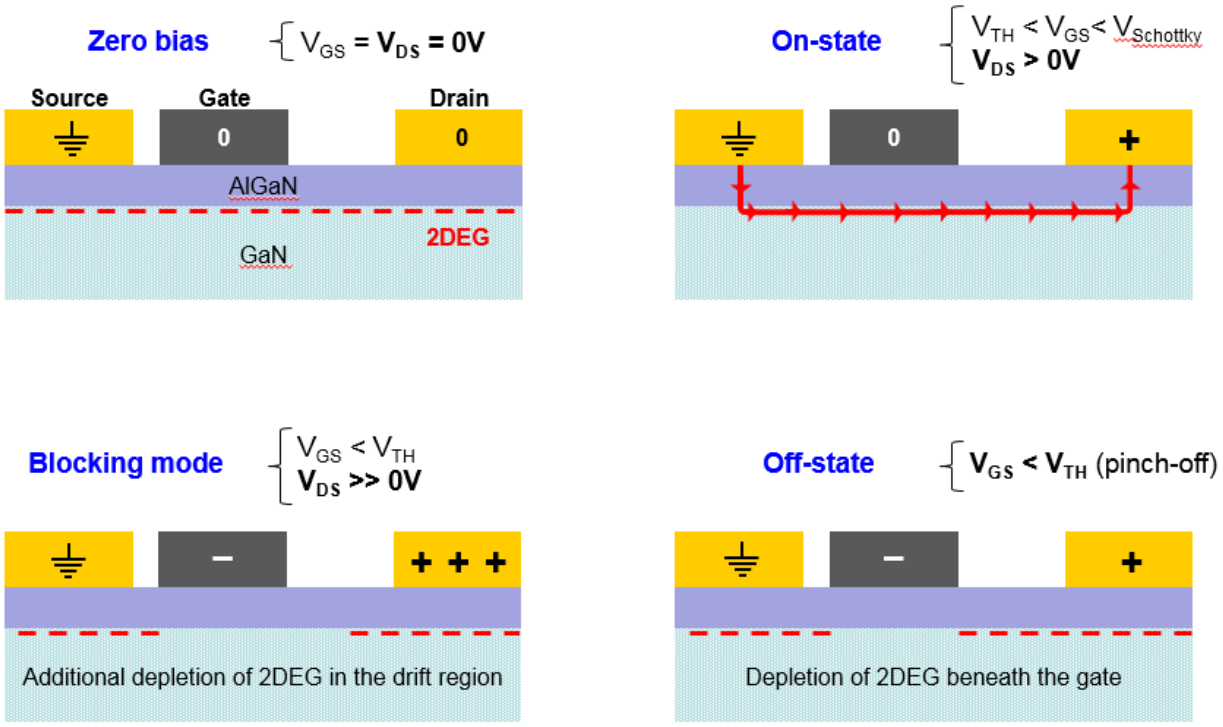


Figure 1.9: GaN HEMT operation modes, starting with the top left going in a clockwise direction: zero bias, on-state, off-state, and blocking mode.

1.5 Key Technological Issues

In spite of the great potential of GaN-on-Si high voltage transistors, its application to power electronics is currently limited by important challenges. The major issues are discussed below.

1.5.1 High gate-leakage current

A conventional heterojunction-field-effect transistor (HFET) device with Schottky gate suffers large gate-leakage current that limits device performance. The leakage gets worse as temperature is elevated. In particular, the gate leakage deteriorates the transistor characteristics by increasing the subthreshold current and shunting the gate to channel capacitance [39]. Both these factors decrease the maximum output power. Also, high leakage promotes defects and further gate leakage

until time-dependent dielectric breakdown (TDDB) occurs. Hence, a reduction in gate leakage can potentially delay TDDB and improve life.

Using a metal-oxide-semiconductor HFET (MOSHFET) structure with gate dielectric is a very effective way to reduce gate-leakage current [13]. The gate metal is isolated from the AlGaN barrier layer by a dielectric film such as SiO_2, Al_2O_3, HfO_2, and so forth, as seen in Figure 1.10. Hence, the MOSHFET gate behaves more like a MOS gate structure rather than a Schottky barrier gate in regular HFETs.

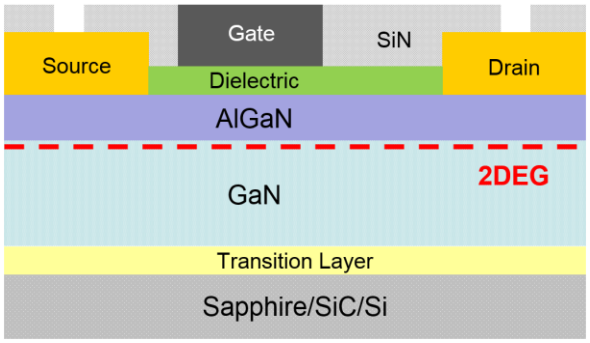


Figure 1.10: Cross section of a lateral GaN HFET with gate dielectric (MOSHFET structure).

A properly designed AlGaN barrier layer is fully depleted by electron transfer to the adjacent GaN layer. Therefore, the gate insulator in the MOSHFET couples with the AlGaN epilayer, ensuring very low gate-leakage current and allows for a large negative to positive gate voltage swing [88]. Data shows MOSHFET gate-leakage current can be up to six orders of magnitude smaller than for a regular HFET with similar gate dimensions [13].

1.5.2 High electric field

In the off-state and blocking mode, there is a high electric field near the gate edge on the drain side, due to the sharp edges of a rectangular gate. This could generate high energy carriers (hot electrons) that can be trapped in the passivation layer, AlGaN barrier layer, or in the interface between these layers. They could widen the surface depletion region thereby leading to degradation in DC and RF performance. Also, high electric field can cause gate breakdown that can be attributed to the generation of defects induced by the electric field; when the density of these defects becomes sufficiently high, a percolative conductive path is formed, and gate leakage current sharply increases [49].

Device design improvements (Figure 1.11) comprising gate and source-connected field plates are an effective way to reduce the electric field [116], thereby reducing trapping effect and increasing breakdown voltages [12], [13]. This further suppresses the increase in on-state resistance as well as gate leakage degradation. Generally, the longer the field plate, the more output power can be achieved. However, the capacitance between gate-connected field plate and drain becomes gate-to-drain capacitance that can lower switching frequencies [13]. Also, the source-connected field plate can add parasitic capacitance to the device input.

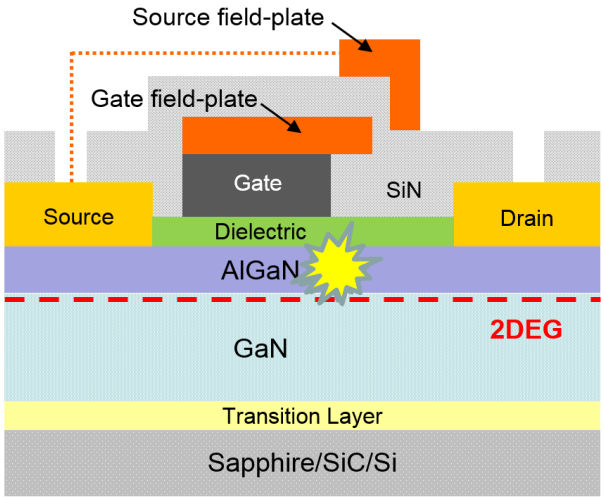


Figure 1.11: Cross section of a lateral GaN MOSHFET with gate-connected and source-connected field plates.

1.5.3 Normally-on transistor

For power switching applications, normally-off operation with the threshold voltage above 3V is strongly required in order to prevent the mis-operation caused by noises [12], [90], [91]. GaN inadvertently conducts electrical current. The 2DEG in a HEMT device requires a negative gate bias to turn off the conduction current, thus, presenting the conventional AlGaN/GaN HEMT devices as normally-on or depletion-mode devices. If the gate fails current will continue to flow. Normally-off devices or enhancement-mode (E-mode) AlGaN/GaN HEMTs can greatly simplify circuit designs, improve system reliability, and provide fail-safe operation [90]. Various techniques have been developed to achieve an E-mode device. The common solutions are:

(a) **Recessed Schottky gate** [12] – For thick AlGaN layers, Fermi level is pinned by the surface donors. This creates the 2DEG. If the barrier underneath the gate is reduced to a thickness of a few nanometer (typically 3–5 nm) [116], no polarization induced 2DEG can be formed. Gate recessing is often combined with gate dielectric isolator techniques [92]. In terms of reliability

these devices may be critical, since the gate is separated from the channel only by a few nanometer. This leads to large electrical fields at the drain side edge of the gate unless other precautions are taken [116]. Recessed-gate technique can be used to modulate V_{TH}, however it may come at the cost of performance degradation and non-uniformity [90], [100].

(b) p-GaN gate [50] – The placement of localized negative charges underneath the gate metal shifts the conduction band of the channel region above the Fermi level and thus creates normally-off behavior. Essentially, channel is depleted by the high built-in potential of the P-N junction. Persistent negative charges can be introduced by p-type doped GaN or AlGaN layers [116]. Using this structure the threshold voltage value obtained is usually low, around 1V [90], [124].

(c) Fluorine-based plasma treatment [94] – The negatively charged fluorine ion incorporation by implantation into the AlGaN barrier layer. The charge drives away the 2DEG and shifts the gate-threshold voltage to slightly above 0V with the maximum gate voltage around 1V [124]. Reliability issues may arise since F^- incorporation is not stable at high electric fields unless special precautions are taken [116]. While Fluorine plasma treatment was introduced to provide negative charge, it may affect device uniformity and stability [90], [100].

(d) Inversion-type E-mode MISHFET [93] – The AlGaN barrier layer is completely removed, hence no 2DEG, in the gate region. The gate is placed directly on top of the GaN channel layer and separated by a suitable gate insulator such as, SiO_2, Si_3N_4, Al_2O_3 [116]. Therefore, if the gate is forward biased, an inversion layer is formed under the isolator leading to a current flow. All degradation effects associated with a defect creation in the strained AlGaN barrier layer

(*e.g.*, inverse piezoelectric effect [112]) may be reduced in this case. However, since this approach requires a recess, uniformity is questionable.

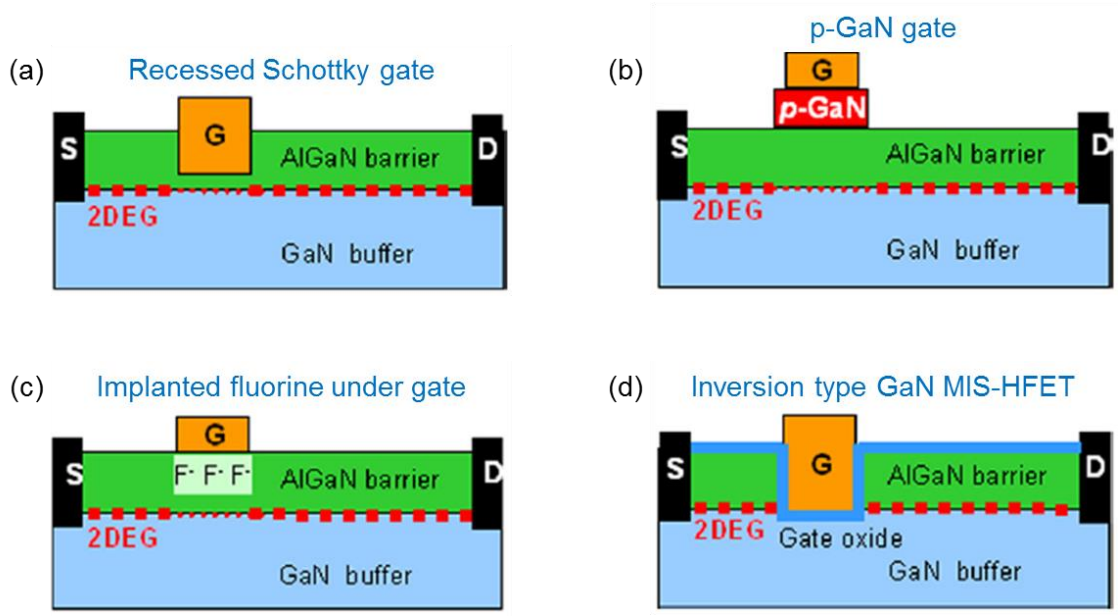


Figure 1.12: Schematic cross section of common normally-off technological solutions [116].

An alternative solution is a cascode hybrid E-mode structure shown in Figure 1.13 [52], which is currently the most commercially viable solution [48]. In this configuration, the source of the high-voltage AlGaN/GaN HEMT is connected to the drain of the low-voltage Si power MOSFET and the gate of the high-voltage HEMT is connected to the source of the Si power MOSFET which serves as the ground or reference terminal. The device can be controlled by biasing the gate of the Si power MOSFET while the drain of the GaN HEMT is connected to the load and the output power source.

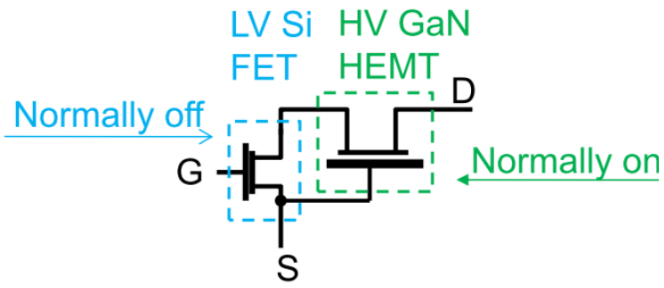


Figure 1.13: Cascode hybrid E-mode structure [52].

In this circuit, the Si MOSFET is turned on with a positive voltage on the gate. When the depletion-mode GaN transistor's gate voltage goes to near-zero volts, it turns on. Current can now pass through the depletion-mode GaN HEMT and the MOSFET, which is connected in series with the GaN HEMT. When the voltage on the MOS gate is removed, a negative voltage is created between the depletion-mode GaN transistor gate and its source electrode, turning the GaN device off. The drawbacks of cascode circuit configuration are switching speed limitation [50], larger area, power loss due to more transistors, and a max operating temperature of 150 °C due to silicon junction [96]. Cascode configuration is practical for larger than 200 V rating [10]. At such high voltage rating the low voltage MOSFET does not add significantly to the on-resistance of the cascode circuit.

1.5.4 DC/RF dispersion or, current collapse or, dynamic $R_{DS(ON)}$

Current collapse is a phenomenon whereby the drain current decreases as a result of electron trapping into the AlGaN surface states [11]. This is perhaps the most critical reliability concern. The main cause of dispersion effects originates from the presence of trap centers related to surface, bulk, and interface states [13]. These trapping states are assumed to be associated with surface states created by dangling bonds, threading dislocations accessible at the surface, and ions

absorbed from the ambient environment [26]. In the off-state, electrons from the gate are injected into the empty surface donors required to maintain a 2DEG. These surface states, when filled with electrons, create a layer of charge at or near the surface that act as a virtual gate and deplete the 2DEG in the high field region between the gate and drain. Figure 1.14(a) depicts the mechanism of $R_{DS(ON)}$ increase and Figure 1.14(b) shows simulated graphical effect. In the on-state, under AC drive, the electrons contained in the surface layer get detrapped; however, cannot fully modulate the channel charge due to long-time constant of the donor traps that range from seconds to microseconds [26]. This results in a reduced channel current and higher on-resistance (symptoms of dispersion), and an increase in knee voltage [104].

The mechanism is understood as a transient and recoverable reduction in drain current response; a finite time required by the surface traps to respond to an external voltage step. Similar degradation is also observed via threshold voltage shift, gate-lag and drain-lag transients. This increases on-resistance and therefore, limits device performance. Although transient, this effect can cause the device to excessively self-heat and fail prematurely [67]. Furthermore, electrons can be trapped in the AlGaN barrier layer itself or in the GaN buffer layer below. Hence, the trap density can increase as the device ages, making the dynamic $R_{DS(ON)}$ effect worse. The effect is compounded at elevated temperatures [25]. The high energy electrons can generate traps, further promoting charge trapping. There are also reports that claim the dispersion effects may be irreversible if certain critical electrical fields are exceeded [116].

The magnitude of current collapse is strongly dependent on the electric field at the gate-edge where electrons can be accelerated [53]. Surface passivation, or surface treatments, can be effective at reducing the surface trap density and thereby reducing hot-electron degradation [53].

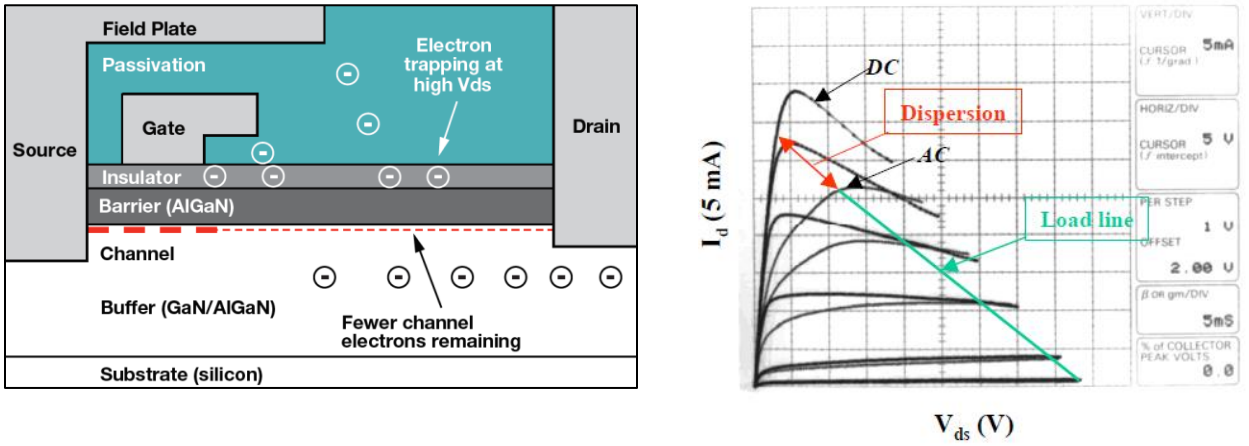


Figure 1.14: (a) Schematic cross-section of a GaN device showing mechanism of $R_{DS(ON)}$ increase [67] and (b) dispersion between the large signal AC and DC HEMT characteristics simulated by a 80 μs pulse on the gate [11].

Passivation of AlGaN surface by using different dielectrics has been found to eliminate the dispersion effect. For instance, SiN passivation has been shown to be more effective than SiO_2, HfO_2, and Al_2O_3 passivated devices at minimizing traps and reducing current collapse [27], [106]. If used in the gate region however, the higher dielectric permittivity of Si_3N_4 (7.5) vs. SiO_2 (3.9) causes threshold voltage (V_{TH}) increase to be higher.

Device design improvements using gate and source field plates are an effective way to reduce the electric field thereby suppressing the increase in on-state resistance. Surface passivation, or surface treatments, can also be effective at reducing the surface trap density and thereby reducing hot-electron degradation. The use of a conducting substrate acting as a backside field plate helps to mitigate electron trapping in the buffer region beneath the channel [53]. It was reported that dynamic $R_{DS(ON)}$ was much improved with GaN devices built on conductive silicon substrates compared to GaN devices built on non-conductive sapphire substrates. In addition, better confinement of electrons in the potential well and overall improvement in the material quality of AlGaN/GaN epitaxial layers are important to combat dynamic $R_{DS(ON)}$.

One of the technological solutions that have been proposed as a possible cure for this detrimental effect consists of using GaN/AlGaN/GaN epitaxial structures with a thin (typically 3–5 nm) n-type-doped GaN cap layer. It has been suggested to act as a "surface-charge-control" layer that reduces the effect of surface polarization charge [108], [119], [120]. However, Meneghesso *et al.* disputes such claim being concrete [105]. Degradation under RF drive has also been correlated to different epi structures comprising the AlGaN/GaN HFET. For example, reducing the AlGaN barrier thickness significantly improved device reliability. This improvement is attributed to a more stable material structure with less lattice strain in the AlGaN barrier layer.

1.5.5 Hot electron effect

A permanent device degradation after high V_{DG} stress under on-state conditions has been attributed to the presence of hot electrons [126]. In a GaN HEMT device where extremely high electric field may be present, electrons can gain sufficient high energy to escape the channel and get trapped in the AlGaN layer under the gate, or in the gate-drain region where the electric field is maximum, either at the surface or within the passivation layer, or in buffer traps [125] [127]. This is illustrated by Figure 1.15. These "hot electrons" may form the so called virtual gate [102] and deplete channel carriers, thereby increase drain series resistance.

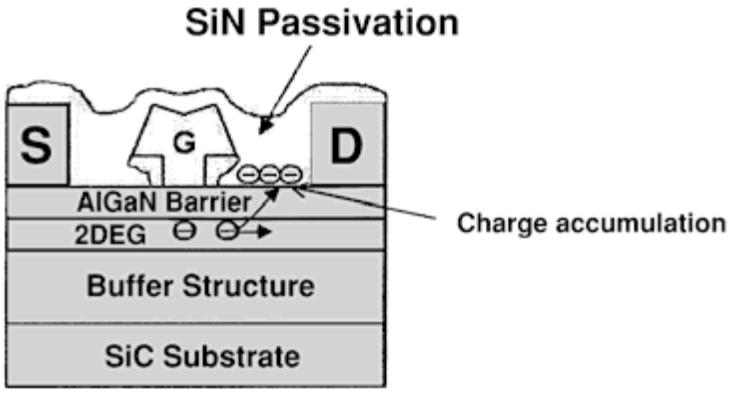


Figure 1.15: Hot electron tunneling into the passivation layer under high stress condition [127].

Hot electron effects, with generation of deep levels and trapping of electrons in the dielectrics or/and at surfaces and interfaces under the gate as over the gate-drain access region may occur both, during off-state tests or (more frequently) during semi-on and on-state tests [125].

The term "hot electrons" refers to non-equilibrium electrons which acquire kinetic energy values sufficient to overcome potential energy barriers, be injected into buffer, barrier or insulating layers and be trapped there, break atomic bound and create interface states or activate traps. According to the various experimental conditions, material properties and device weaknesses, hot electrons may give rise both to parametric, gradual, permanent or recoverable positive or negative threshold voltage shifts and/or to decrease of transconductance [125]. Hot electron effects can be evaluated by means of electroluminescence microscopy and spectroscopy.

1.5.6 Inverse piezoelectric effect

This degradation is related to strain relaxation theory driven by electric fields [112]. GaN HEMTs are predicated on the piezoelectric properties of the material in conjunction with spontaneous polarization. The electric field generated between AlGaN and GaN as a result of strain caused by

the lattice mismatch allows high electron channel densities to form at the AlGaN/GaN interface. Under large reverse gate stress, the high vertical electric fields concentrated at the gate edge on the drain side can increase the tensile strain in the AlGaN barrier layer due to the inverse piezoelectric effect. When a critical drain-gate voltage V_{DG} is reached and the mechanical stress becomes excessive, strain can relax through crystallographic defect formation, such as dislocations [112], [113], [117], [118]. These defect states not only degrade I_{DS} and R_{DS} by trapping electrons but also aid trap-assisted electron tunneling between gate and channel through the AlGaN barrier, effectively lowering the Schottky barrier height of the gate. The effect is illustrated in Figure 1.16.

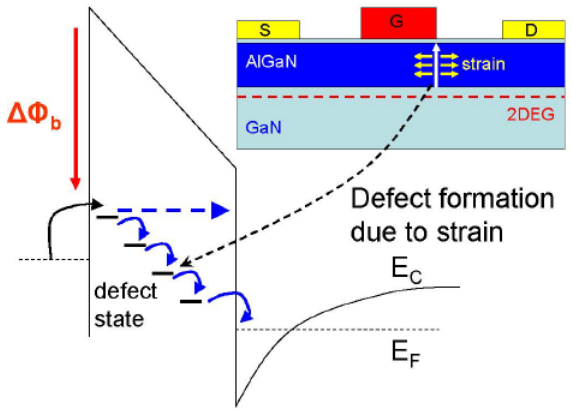


Figure 1.16: I_{GS} degradation mechanism for reverse bias stress. Crystallographic defects produced by the inverse piezoelectric effect provide a leakage path across the AlGaN barrier [113].

In order to prevent this mode of I_{GS} degradation, it is necessary to reduce the elastic energy and the vertical electric field in the AlGaN barrier. Device designs that mitigate the electric field should also improve the reliability due to this mechanism. Examples are GaN cap, surface passivation, field plates, slanted gates, and gate corner rounding [117].

1.5.7 Post-stress reliability, long-term stability

GaN devices have a tendency to show performance degradation post-stress that may be recoverable or sometimes irrecoverable [114]. Surface charge plays a major role yet the trapping mechanism is not fully understood. The trapping and detrapping effects may lead to significant device drift, with change in the threshold voltage and transconductance [118]. Pre-existing deep levels on the surface, at interfaces, within the GaN buffer, and within the semi-insulating substrate can originate from threading dislocations, impurities, ligands, and oxide-defects. These can degrade both the static and dynamic performance, promoting metastable charge-trapping effects, threshold-voltage instabilities, and on-resistance increase [25]. There may be process-induced instabilities, especially in connection with compensating species (Fe or C), contaminants like H, F, O, or defects [125]. Also, after device operation, increased trapping behavior has been observed. At the present time, physical understanding of the fundamental mechanisms behind device degradation is still insufficient. The "virtual gate" effect proposed by R. Vetury et al. is usually used to explain device degradation [102].

In MOSHFETs, threshold voltage instabilities and Time Dependent Dielectric Breakdown (TDDB) depend on the chosen gate dielectric material and on the related deposition techniques [49]. A high quality gate insulator with a high breakdown voltage is needed. Time dependent degradation can be induced by trap creation and formation of conductive percolative paths between gate and channel [125]. Research has focused on reducing or eliminating device drift and leakage currents under the high field and high power conditions associated with device operation [13]. Techniques include improving material quality (reducing defect density) of both substrates and epitaxial layers, surface passivation to combat current collapse and suppress gate-leakage current, and device/process engineering to reduce peak electric fields in the channel.

The group III-nitride semiconductors have been considered an ideal candidate for high temperature (T_{CH} > 300 °C) electronic devices due to their large band gap and resulting low thermal carrier generation rate [25], [51]. On the other hand, thermal and self-heating effects are very pronounced in any power semiconductor device [85]. Lateral devices have poor thermal handling capability due to the silicon substrate [1]. Degradation in DC characteristics at elevated temperatures has been reported. Current collapse has been shown to worsen with increasing temperature [25]. The positive temperature dependent R_{ON} increase could represent a serious issue for GaN-based electronics, which are supposed to be operated in high-temperature conditions. Such switching characteristics or the transient characteristics at high temperatures have not been well documented. Moreover, the mechanisms responsible for reliability issues have not yet been fully established given the complexity of interface states [101]; however, remain a critical concern preventing widespread adoption of GaN technology. Devices for power switching applications must demonstrate long-term stability; in particular they should maintain good current blocking capabilities in the off-state, constant threshold voltage, low static and dynamic on-resistance.

1.6 Project Goals and Thesis Outline

This dissertation focuses on performance and reliability enhancement of normally-on AlGaN/GaN lateral MOSHFETs for high voltage switching applications. There was considerable focus on the development of the device process as well as gaining an understanding of device operation and the parameters that affect device performance.

This chapter (Chapter 1) covers the essential background on GaN-based transistors. Material properties and merits are reviewed. Device principals and operation modes are outlined. The key challenges with GaN devices are discussed in details.

Chapter 2 provides an overview on choice of dielectric materials for GaN MOSHFETs along with ALD technique. Device fabrication and characterization methods are also discussed.

Chapter 3 provides investigation of ALD oxidants. Devices are characterized in DC, large-signal microwave power, and under stress. Process optimization through use of O_3 oxidant provides improved DC and RF performance along with enhanced reliability compared to water oxidant based devices.

Chapter 4 presents a systematic study of AlGaN/GaN MOSHFETs as a function of dielectric thickness, gate-to-drain distance, and temperature. A comprehensive electrical DC characterization is performed, and an optimal dielectric thickness is recommended.

Chapter 5 presents investigation of high temperature annealing ambient, nitrogen (N_2) and forming gas (FG). Devices are characterized in DC, large-signal microwave power, as a function of temperature, and under stress.

Chapter 6 concludes with summary of the results obtained and outlook for future work towards further optimization of GaN MOSHFETs.

CHAPTER 2: Dielectrics, Fabrication Methods, and Experimental Procedures

2.1 Choice of Dielectric Materials

There has been a lot of research effort for GaN-based metal-oxide-semiconductor (MOS) devices due to reduced gate leakage, greater voltage swings, higher drain current, higher transconductance, and better thermal stability compared with the Schottky-gate devices. In addition, dielectric used as surface passivation minimizes the current collapse that originates from surface traps.

However, finding the most appropriate dielectric materials is challenging and often involves a compromise of the required properties such as, permittivity, conduction/valence band offsets, breakdown strength, thermal stability, and interface trap density. A high dielectric constant is preferred to preserve maximum channel control but a large conduction band offset (CBO) is favorable to reduce gate leakage currents. Typically, the bandgaps of insulators show inverse relation to dielectric constants, *i.e.* the larger the *k* value, the smaller the bandgap. Figure 2.1 shows the requirements of dielectrics on AlGaN/GaN in the gate and passivation regions.

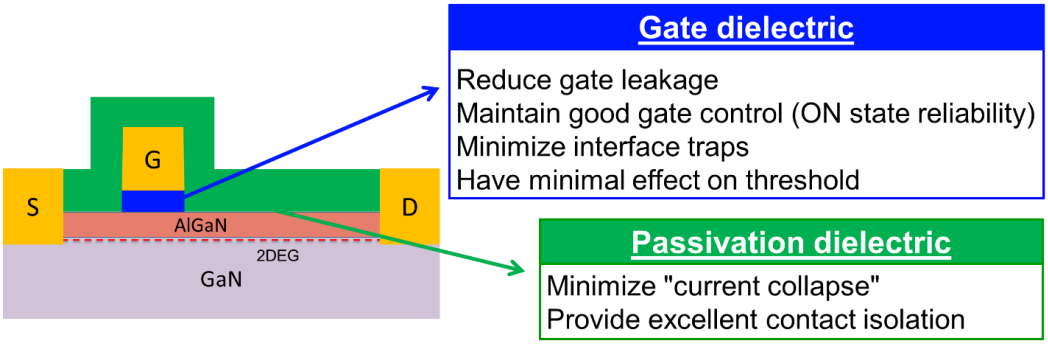


Figure 2.1: Objective of dielectric on AlGaN/GaN in the gate and passivation regions.

2.1.1 Requirements for the Gate dielectric:

For any gate insulator candidate being considered, there should be a large dielectric bandgap leading to sufficient conduction band offset to GaN to ensure a significant barrier height (> 1 eV) needed for low gate leakage currents [37], [66]. A large CBO prevents tunneling of electrons through the dielectric and reduces electron trapping which can cause time-dependent dielectric breakdown [89]. For example, SiO_2 on GaN has a large CBO of 2.56 eV [75].

A high dielectric constant is preferred to maximize gate control over the channel and increase transconductance [98], [107]. Example of high-k dielectrics are Al_2O_3 (ε_r = 9.6) and HfO_2 (ε_r = 18.5) [21]. For the depletion-mode HEMT, insertion of a gate insulator shifts device threshold voltage (V_{TH}) towards the negative direction due to the decreased gate barrier capacitance. Dielectrics with relatively low-*k* characteristics, such as, SiO_2 and Si_3N_4 (ε_r = 3.9 for SiO_2 [21] and 7.5 for Si_3N_4 [66]), cause large negative V_{TH} shifts [107]. A high-*k* dielectric as the gate oxide material to replace SiO_2 (or Si_3N_4) not only minimizes V_{TH} shift but also allows the physical thickness of the oxide to be increased, thereby reducing the gate leakage current, while maintaining or increasing capacitance per unit area of the gate oxide.

2.1.2 Requirements for the Passivation dielectric:

In the access area the primary objective is to effectively passivate surface states and minimize interface traps with AlGaN/GaN. The interface states cause various operational stability and reliability issues in GaN-based MOSHFETs such as threshold voltage instability and current collapse phenomenon [76].

2.1.3 Choice of Candidates for the Gate Oxide and Passivation:

Table 2.1 lists physical parameters of some of the popular dielectrics on AlGaN/GaN. A brief description of the dielectrics follow.

Table 2.1: Summary of the physical parameters of various dielectrics relative to GaN [21], [66], [75].

Dielectric	Dielectric constant [21], [66]	Energy band gap (eV) [66]	Conduction band offset to GaN (eV) [75]
ALD SiO_2	3.9	9.0	2.56
ALD $Al2O_3$	9.6	8.0	1.96
ALD HfO_2	18.5	5.8	1.51
ALD HfAlO	14.0	6.4	1.61
PECVD Si_3N_4	7.5	5.3	1.30

Silicon dioxide (SiO_2), Silicon nitride (Si_3N_4)

On AlGaN/GaN, the most extensively researched dielectrics are SiO_2 [65] and Si_3N_4 [64] which have been considered both as gate insulators and channel passivation layers [101]. Their appeal is largely related to their current widespread use in Si-based technologies, and thus they are well-understood materials. Furthermore, they have been proven effective at reducing leakage current by ~4 orders of magnitude.

The main advantage of SiO_2 is its high conduction band offset to GaN (2.56 eV) [75] that makes it very effective at suppressing gate leakage. On the other hand, Si_3N_4 has a higher dielectric constant (7.5) at the expense of the band gap (5.3 eV). Si_3N_4 is advantageous because it passivates nitrogen-vacancy related defects on the AlGaN surface during dielectric growth [101]. Ultimately, this results in a lower D_{it} and reduced DC/RF dispersion. For example, the D_{it} of Si_3N_4/GaN was found ~6 times lower than the D_{it} of SiO_2/GaN. Therefore, SiO_2 has been associated with displaying poor gate-lag characteristics [22]. On the contrary, while Si_3N_4 helps to alleviate the

problem of current collapse, it suffers from large reverse leakage current due to having smaller conduction band offset to GaN (1.3 eV) [101]. Also, Si_3N_4 dielectric has been found to deteriorate breakdown characteristics. [72].

Aluminum oxide (Al_2O_3)

Amorphous Al_2O_3 is one of the leading candidates for insulators in GaN-based devices because of the wide band gap (8 eV), sufficient permittivity (9.6), high breakdown field (10 MV/cm), high thermal (~ 900 °C) and chemical stability on AlGaN [21], [24], [66], [75], [91]. Al_2O_3-passivated AlGaN/GaN exhibits excellent performance in suppressing gate leakage, likely a result of the large conduction band offset to GaN (1.96 eV), and reducing current collapse due to relatively low interface state density [21]. However, the dielectric constant of Al_2O_3 is still relatively low in comparison with other materials [75], and thus, Al_2O_3-passivated devices may also be characterized by large threshold voltage shift and lower transconductance [24], [43]. Ye *et al.* [24] reported a midgap interface trap density of 16nm ALD-Al_2O_3/GaN at the range of 10^{11}–10^{12} cm^{-2} eV^{-1}.

Hafnium oxide (HfO_2)

Amorphous HfO_2 have shown significant promise because of their high permittivity (18.5) and sufficient band gap (5.8 eV) [21], [23], [65], [66]. For this reason, HfO_2 is currently used to replace SiO_2 as the gate insulator in Si-based MOSFET fabrication, which allows for device scaling [43]. Its conduction band offset to GaN is 1.51 eV [75], which could fulfill the prerequisite for good gate dielectric, which requires a CBO of at least 1 eV to ensure a substantially low gate leakage [37], [66].

Transistors with HfO_2 exhibited high drain current, low on-resistance, low leakage currents, and great immunity to current collapse [23], [72]–[74]. The HfO_2 passivation is believed to greatly reduce the surface trap density and improve reliability [74], [75]. Chang *et al.* [44] reported 14.8 nm thick ALD-HfO_2/GaN with a high drain current ($I_{DS,\ max}$ ~ 230 mA/mm), low gate leakage current density (10^{-8} A/cm^2), low interfacial density ($5-8 \times 10^{11}$ cm^{-2} eV^{-1}), and negligible current collapse. Although it is possible to achieve a lower gate leakage with Al_2O_3 gate oxide (owing to larger CBO to GaN), HfO_2 still provides adequate low gate leakage while resulting in a less threshold-voltage shift and higher transconductance compared to Al_2O_3 [43].

The drawback of HfO_2 dielectric is that it is less thermally and chemically stable than Al_2O_3, where amorphous HfO_2 crystallizes into predominantly monoclinic polycrystalline films on Si at only 400 °C [75]. This is disadvantageous as crystalline structures are more likely to contain grain boundaries, which enhance leakage.

Hafnium aluminum oxide (HfAlO)

Another solution is to use ternary compounds on AlGaN such as HfAlOx [63], HfSiOx [75], or, use a stack gate structure (*e.g.*, HfO_2/Al_2O_3) [71] to obtain a good trade-off between dielectric constant and conduction band offset and achieve better chemical and thermal stability. For example, Yue *et al.* [71] fabricated a stack gate structure with HfO_2/Al_2O_3-passivated AlGaN/GaN MOSHFET using ALD. Their device had minimal C-V hysteresis, a small threshold voltage shift, a maximum drain current of 800 mA/mm, a peak transconductance of 150 mS/mm, and leakage current at least six orders of magnitude smaller than an unpassivated HEMT. Furthermore, as long as the device surface was properly passivated, the device did not show current collapse.

In summary, there have been some significant strides in mitigating reliability issues with dielectric passivation schemes and gate dielectrics, but there is still no perfect solution. The complexity of this issue is intricately linked to the reciprocal nature of the dielectric constant and band gap and may also be related to the different mechanisms responsible for gate leakage and current collapse. MOSHFETs using insulators, including SiO_2 [65], Si_3N_4 [64], Al_2O_3 [24], [43] as the gate dielectrics, have shown to alleviate gate leakage and drain current collapse but at the expense of a significant decrease in device transconductance [24], [43], [64] and a large negative shift in threshold voltage [64]. The large V_{TH} shift is due to its relatively small dielectric constant and the interfacial and volumetric charges [73], [74]. Usage of dielectrics with higher permittivity could help solve these problems, because larger dielectric constant could result in more efficient conductivity modulation [37], thus a smaller decrease in transconductance and a moderate increase in the threshold voltage could be expected in MOSHFETs with high-*k* gate dielectric, such as HfO_2 and HfAlO alloy.

2.2 Atomic Layer Deposition (ALD)

ALD is a thin film deposition technique that is based on the sequential use of a gas phase chemical process on a substrate. Using precursors, one at a time in a sequential pulse, through the repeated exposure and self-saturated chemisorption, a thin film is slowly deposited. It is a well-established method and can provide several advantages such as low-temperature processing, 3D conformal deposition, good uniformity, and precise thickness control [21]. Therefore, by using ALD it is possible to deposit high-quality gate dielectrics as well as passivation layers on AlGaN/GaN substrates with low defect density resulting in performance enhancement and better long-term reliability of the device [17].

In ALD of metal oxides, one growth cycle consists of an exposure to metal precursor, a purge period, an exposure to oxygen precursor, and a second purge period, illustrated in Figure 2.2 [87]. Thus, each cycle results in a monolayer coverage of the sample surface. Typical deposition rates are 1A/cycle and 10 nm/hr. The deposition process involves a repeated cyclic execution of four steps:

1. During the first step, metal precursors are introduced into the reactor. Sufficient time is provided for the precursor molecules to get chemisorbed on the hydroxylated/oxidized surfaces of the substrate. This is a self-limited reaction which stops once the entire surface is saturated by the precursor molecules.
2. The unreacted precursor molecules are purged from the reactor by an inert gas like N_2.
3. Following purge, an oxidant is introduced and reacts with the new surface functional groups formed from the previous pulse. Common oxidants include H_2O or O_3 in a thermal ALD process, or atomic oxygen in a plasma ALD process. Given sufficient time, this precursor oxidizes the new surface and eliminates the organic ligand as a gaseous by-product.
4. Once the reaction is completed, the unreacted precursors and the gaseous by-products are purged out of the chamber. By this purging process, excess reactants do not contribute to additional film growth.

Depending on the reactivity of the metalorganic precursor, multiple oxidizing chemistries may be required to ensure completeness of the oxidizing step. Also, an optimization of the ALD process recipe is required to ensure sufficient precursor quantity and reaction time for each precursor step. This may also require heating the precursor cylinder to increase the vapor pressure. Details of the

specific precursors and the recipe conditions used for different ALD dielectrics are provided in Table 2.2.

Table 2.2: ALD deposition conditions used for different dielectrics.

Dielectric	*Metalorganic precursor*	*Oxidizing precursor*	*Metalorganic precursor cylinder temperature*	*Chamber temperature*
HfO_2	Tetrakis-dimethyl-amino-hafnium (TDMAH)	H_2O or O_3	75 °C	200 °C
SiO_2	3-amino-propyl-triethoxy-silane (APTS)	H_2O, O_3	100 °C	150 °C

This cyclic self-terminating process enables precise control of the monolayer thickness, large area film uniformity, highly conformal and pinhole-free film deposition [17], [73]. ALD also enables low temperature processing [17], [66]. Therefore by using ALD it is possible to achieve low density of interface states resulting in performance enhancement of the device. For example, Lee *et al.* [17] reported a charge density of 8.73 x 10^{10} cm^{-2} for ALD SiO_2 compared to 3.49 x 10^{11} cm^{-2} observed for PECVD SiO_2. A drawback of ALD is that it is a relative slow process. However, the deposition temperature should be kept at higher than the minimum required temperature for the reaction to occur on the substrate surface. Too low deposition temperature results in a thermally activated chemisorption as well as decrease in the deposition rate. On the other hand, if the deposition temperature is too high, chemical bonding cannot sustain. In this work, ALD dielectric films were deposited in a commercial Savannah S100 system from Cambridge Nanotech. Details on the system and chamber design are available in [47].

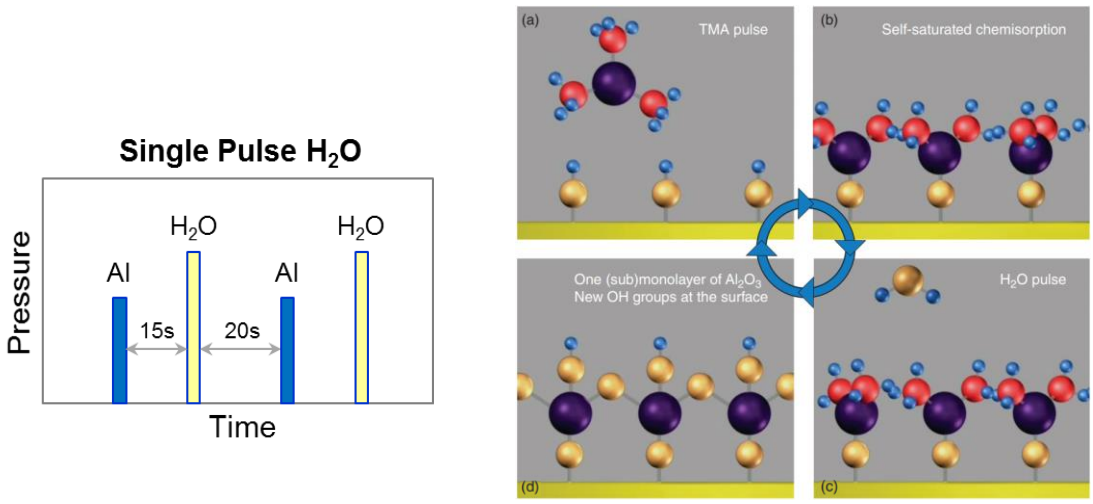


Figure 2.2: ALD Pulse sequence and the process for deposition of Al_2O_3 using TMA and H_2O [87].

2.3 Transistor Fabrication

This section presents the details of transistor fabrication. GaN-based materials can be grown on Si, sapphire (Al_2O_3), or SiC (6H-SiC) substrates [12], [13]. While high quality GaN epitaxial layers can be realized using relatively cheap, semi-insulating sapphire substrate it is considered to be disadvantageous due to low thermal conductivity (0.5 W/cm-K [111]). SiC substrates have high thermal conductivity (4.9 W/cm-K [111]) however, are not cost effective (100x Si) [124]. Si substrate, which is typically used [50], on the other hand, allows for low-cost, large diameter, and acceptable thermal conductivity (1.5 W/cm-K [21]) while tolerating increase in defect densities due to lattice and thermal mismatch [49]. Of course, the ideal solution would be homo-epitaxy, that is, GaN grown on bulk GaN, as it allows for homo-epitaxy without any mismatches between substrate and epitaxial layer. This would offer the lowest density of dislocations and thus, the highest epitaxial quality. However, bulk GaN is only available in small wafer diameters and still expensive at 1000x Si, even when compared with SiC at 10x [124]. In order to deposit GaN epitaxial layer on the substrate, a buffer layer must be deposited that provides strain relief between

GaN and the heterogeneous material. This buffer layer typically includes several thin layers of GaN, AlGaN, and AlN [50].

2.3.1 Substrate properties

Devices were fabricated on AlGaN/GaN heterostructure grown on Si <111> substrate, provided by NTT Advanced Technology Corporation. Table 2.3 outlines the epi-layer structure. The GaN cap improves dynamic reliability of the HFET device [108], [119], [120]. Figure 2.3 shows a schematic of a typical substrate with Si (111).

Table 2.3: Epi-layer structure of the vendor substrate.

(set point)

Layer	Material	Al composition	Thickness (nm)	Dopant	Doping (cm^{-3})
5	i-GaN	-	2	-	-
4	i-AlGaN	0.25	20	-	-
3	i-GaN	-	300	-	-
2	i-GaN (C-doped)	-	~3900	-	(*)
1	Buffer layer (C-doped)	-			
Substrate	Si				

(*) NTT-AT standard high resistivity condition.

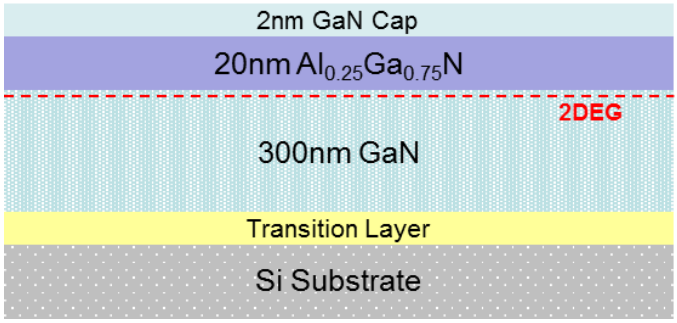


Figure 2.3: Simple schematic of the AlGaN/GaN substrates procured from vendor, as listed in Table 2.1.

2.3.2 Surface cleaning

GaN surface is typically contaminated with high concentrations of structural defects, point defects, surface contamination, and native oxide [101]. Gallium nitride forms a thin native oxide of mostly Ga_2O_3 [109] in air ambient which impacts the dielectric/GaN interface for a deposited dielectric. Cleaning and surface processing is therefore an important step in device fabrication. Multiple surface cleaning techniques have been reported in literature with the most common chemical cleans consisting of NH_4OH or HCl followed by HF chemistries [110]. Furthermore, device structure requires the deposition of a passivation scheme, gate dielectric, and/or ohmic contact on the surface, which induces interface gap states as well as additional defect damage depending on the deposition process. The GaN samples in subsections 2.3.3 and 2.3.4, whenever possible, underwent solvent and acid clean to ensure the surface was kept as free of defects as possible. For each of the process steps outlined below, with an exception of post-dielectric deposition, the samples were exposed to acetone, methanol, isopropanol for 10 min each followed by $HCl:H_2O$ (1:1) for 1 min and HF 1% for 1 minute. This clean process has been found to reduce the surface carbon and native oxide concentrations [121].

2.3.3 HFET fabrication flow

The HFET fabrication process flowchart and animation are illustrated in Figure 2.4, and Figure 2.5 and comprises of the processes explained here.

1. **Isolation:** A deep mesa etch was performed to isolate the active area (eliminates the 2DEG) by using $SiCl_4/Cl_2$ reactive ion etching (RIE).

2. **Ohmic contact:** Source and drain ohmic electrodes were formed by patterning, sputter deposition of Ti/Al/Ni (20/100/20 nm) followed by e-beam evaporation of Ti/Au (5/100 nm), lift-off, and thermally alloyed by rapid thermal annealing (RTA) at 850 °C for 30 sec in an N_2 ambient. The ohmic contact resistance was extracted from transmission line model (TLM) measurements, on test structures fabricated alongside MOSHFETs.

3. **Gate metal:** Un-annealed gate electrode was formed by RF sputtering TaN/W (50/90 nm) and N-Methyl-2-pyrrolidone (NMP) lift-off.

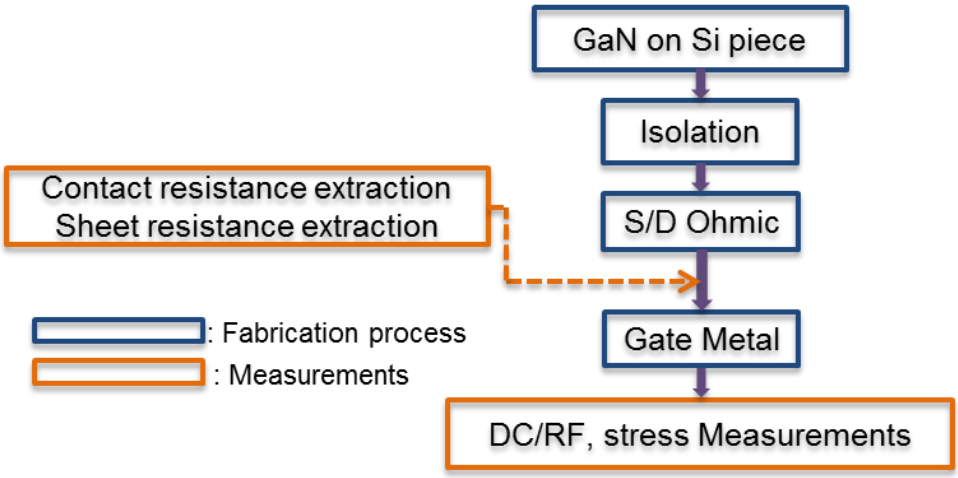


Figure 2.4: Lateral HFET fabrication process and measurement flow.

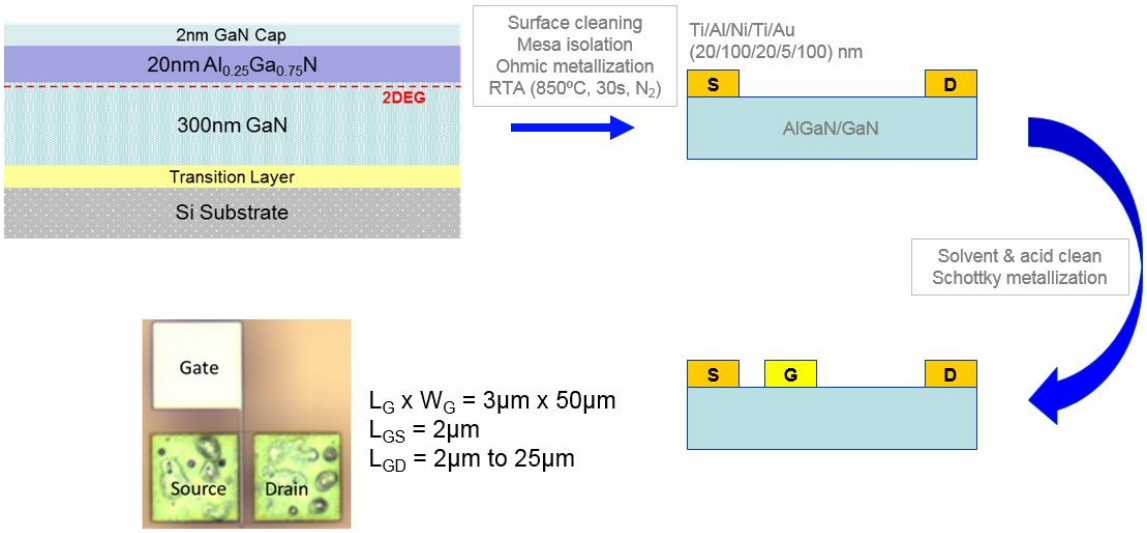


Figure 2.5: Simple schematic showing the HFET fabrication flow and topography of the fabricated line device. L_G = gate length, W_G = gate width, L_{GS} = gate-source spacing, L_{GD} = gate-drain spacing.

2.3.4 MOSHFET fabrication flow

The MOSHFET fabrication process flowchart and animation are illustrated in Figure 2.6, and Figure 2.7 with stages 1, 2 and 3 in common with HFET process flow in Figure 2.3. The main difference here is that before the formation of the gate metal, a gate dielectric is deposited and annealed. The additional processes are listed below.

1. **Dielectric deposition and post-deposition anneal (PDA):** Prior to the dielectric deposition, the AlGaN/GaN substrate was ultrasonic cleaned with acetone, methanol and isopropanol followed by wet HCl, HF clean. Gate dielectric was deposited by ALD. The oxide formation can result in reduced interface quality with a deposited dielectric. Hence, following the ALD deposition, densification of the oxide was achieved by rapid thermal annealing (RTA) using Jipelec JetFirst 100 RTA system at 600 °C for 60 sec in N_2 ambient, unless otherwise noted. Physical thickness of the dielectrics after ALD process was measured using variable angle spectroscopic ellipsometer on monitor Si wafers.

2. **Contact hole:** Since source/drain ohmic contacts had insulator on top, holes were etched through the insulator by BCl_3 RIE.

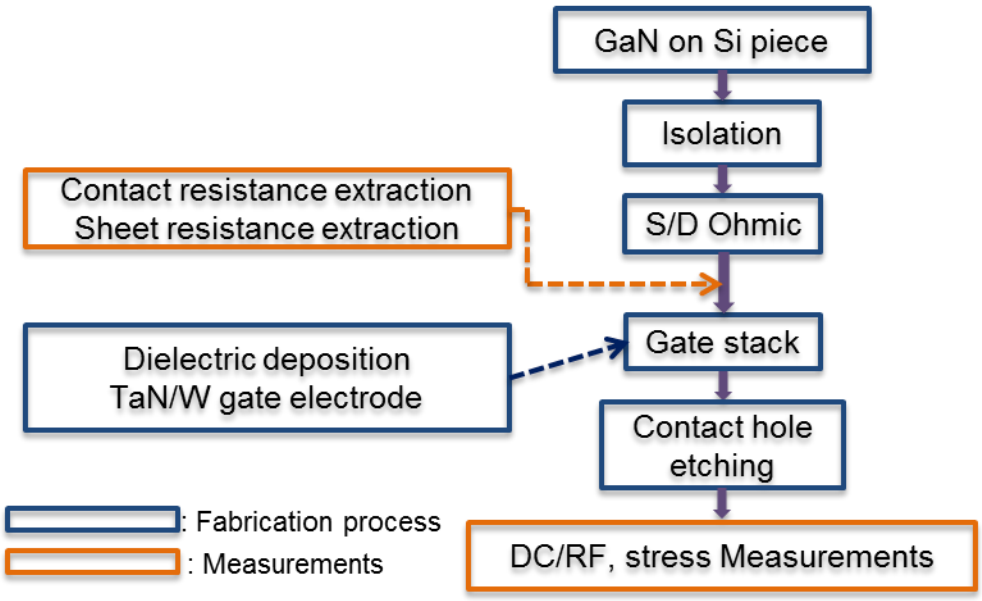


Figure 2.6: Lateral MOSHFET fabrication process and measurement flow.

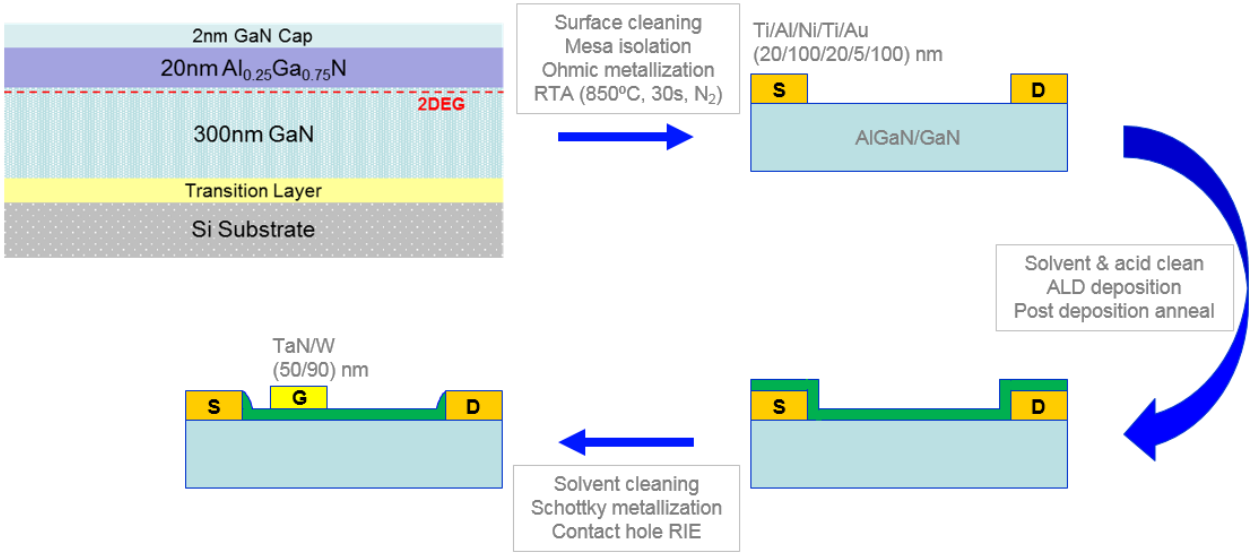


Figure 2.7: Simple schematic showing the MOSHFET fabrication flow.

2.4 Analytical Characterization Methods

The ALD metal oxide films were investigated with a variety of material characterization methods to verify the quality of the film and the deposition process. The material analysis methods are described in this section.

2.4.1 Variable Angle Spectroscopic Ellipsometry (VASE)

Spectroscopic ellipsometry is an optical technique used to determine dielectric properties and thickness of films. In this technique, a beam of monochromatic light is incident on the sample and reflects either off the film surface or the underlying silicon substrate, depending on the wavelength and the transmission characteristics of the film. Polarization and phase shift data is collected for a range of wavelengths to determine the complex reflectance ratio of a material system. The complex reflectance ratio, ρ, is composed of an *s* component, oscillating perpendicular to the plane of incidence; and a *p* component, oscillating parallel to the plane of incidence. In Eq. 2.1, tan(Ψ) is the amplitude ratio upon reflection and Δ is the phase shift [122].

$$\rho = \frac{r_p}{r_s} = tan(\Psi)e^{i\Delta} \tag{2.1}$$

Ellipsometery measurements were used with a Cauchy model to determine the thickness of the deposited films. A Woolam VASE was used to take measurements at an angle of 75° from the substrate normal over wavelengths from 500-750 nm for thickness measurements.

2.4.2 X-Ray Diffraction (XRD)

The XRD analysis in this work was done in grazing angle (GA-XRD) using Rigaku Smart Lab X-ray diffractometer with parallel beam optics. XRD is a useful tool to extract the crystallographic information of a material. During XRD, x-rays at different incident angle are injected into the material and the reflected x-ray is analyzed by a detector. Only short wavelength x-rays (in the range of a few angstroms) are used so that the wavelength of x-rays is comparable to the size of atoms in the sample under observation. Commonly, Cu and Mo are used as the x-ray source which emits 8 keV and 14 keV x-rays with corresponding wavelengths of 1.54 and 0.8 respectively [123]. The energetic x-rays can penetrate into the materials under observation, and provide desired information about the material.

The x-ray have known characteristic wavelength (λ). When they are incident on a sample, they get reflected and the reflected spectra is analyzed by a detector to determine the crystalline state of the material. If the rays fall on the sample at an angle θ, the Bragg's law can be written as:

$$2d\sin\theta = n\lambda \tag{2.2}$$

where d is the inter-atomic distance in the material. If the material is crystalline, and the distance between the atoms are integral multiple of λ, then the x-ray received at the detector will have a constructive interference at certain angle θ thereby resulting in a peak in the received signal. On the other hand, amorphous materials will have only the destructive interference of the x-rays at the detectors, hence no peaks will be observed. Depending upon the location of peaks along the θ axis (usually 2θ is used for convenience), one can determine the materials in the sample as well as its crystal information. Similarly, in poly-crystalline materials, several peaks are observed in the XRD analysis.

2.5 Electrical Characterization Methods

Characterization of the devices was performed by electrical characterization systems along with physical characterization systems. Electrical characterization was performed with Keithley 4200–SCS parameter analyzer, HP 4284A precision LCR meter. Electrical characterization provides the information of device behavior such as current-voltage relationship, capacitance-voltage relationship, *etc*.

2.5.1 Experimental setup

On wafer characterization of the fabricated devices is performed on a versatile Cascade probe station that is connected with Keithley 4200–SCS parameter analyzer. The chuck on the probe station is connected to temperature controller unit that regulates its temperature from 23 °C to 250 °C. A chamber that enables performing measurements with the device under nitrogen. The station is placed on a vibration-free air-table. The probe needles are capable of low noise gate leakage measurements (fA range). The station is also capable of high voltage measurements up to 200 V with a safety interlock capability. The 4200–SCS is controlled by a Windows OS PC through a GPIB connection.

2.5.2 Capacitance-Voltage measurements

An HP 4284A LCR meter is used for high frequency capacitance-voltage profiling which is capable of measuring frequencies in the 20 Hz – 1 MHz range. These Capacitance-Voltage (or CV) measurements are used to characterize MOS capacitors and calculate parameters such as dielectric constant, layer thickness, threshold voltage, and interface traps.

2.5.3 Current-Voltage measurements

Electrical measurements were carried out using a Keithly 4200 SCS characterization system in conjunction with a Cascade Model 11000 probe station equipped with a chuck capable of measurement temperatures up to 200 °C. The Keithley 4200-SCS is a versatile IV measurement tool capable of 2 W of power with currents in the 10 pA - 1A range and a maximum applied voltage of 200 V. This tool is also capable of applying stress currents/voltage (stress time > 500 ms) in conjunction with IV measurements. This is useful for high drain voltage stress measurements. Current-voltage (or IV) measurements are performed to understand transistor behavior and evaluate the device transfer characteristics.

2.5.4 Pulsed-IV measurements

At any applied bias voltage, a pulsed-IV meter measures the current response of the transistor to an applied voltage perturbation. In this work, we use a pulsed-IV meter to measure the source-drain current response to a gate voltage perturbation. These measurements are useful for reliability and interface traps characterization [21]. Figure 2.8 shows a schematic of the custom built pulsed-IV measurement setup comprising of the following elements.

1. Gate pulse voltage source (HP 8112A): This instrument is used to apply a gate pulse train with a voltage range of (-16 V, 16 V) and a resolution of 0.2 V. A rise time of 100 ns ensures minimum ripple in measured transient currents. The maximum pulse period is 990 ms.

2. DC drain voltage source (HP 8116A): While this instrument can be used to apply pulses as well, here it is used to apply a DC drain voltage in the range (-16 V, 16 V) with a resolution

of 0.2 V.

3. Source resistor: The use of a source resistor helps in making a low noise source voltage measurement and current estimation ($I_{SOURCE} = R_{SOURCE} * V_{SOURCE}$). The value of the source resistor, R_{SOURCE} = 10 Ω, is chosen to be much smaller than that of the transistor devices fabricated using the methods in section 2.3 (> 50 Ω).

4. Oscilloscope (Tektronix TDS-420): A powerful oscilloscope with a full bandwidth of 50 MHz is used to acquire gate, drain and source voltage waveforms with a minimum time resolution of 1 ns and a 16-bit Analog-to-Digital-Converter (ADC) accuracy. Measurement error due to thermal noise at low voltages is reduced by averaging over multiple acquisitions of the gate pulse train.

5. Desktop computer: Custom designed software compiled with Visual C++ is used to control the oscilloscope and the voltage sources using GPIB interfaces and generate transient current waveforms or pulsed-IV curves. The software is capable of acquiring and stitching together waveforms over multiple timescales for high temporal resolution. Algorithms are built in to automatically estimate the required sense voltage range for maximum voltage/current resolution. Moving average filters are used to further improve measurement noise immunity.

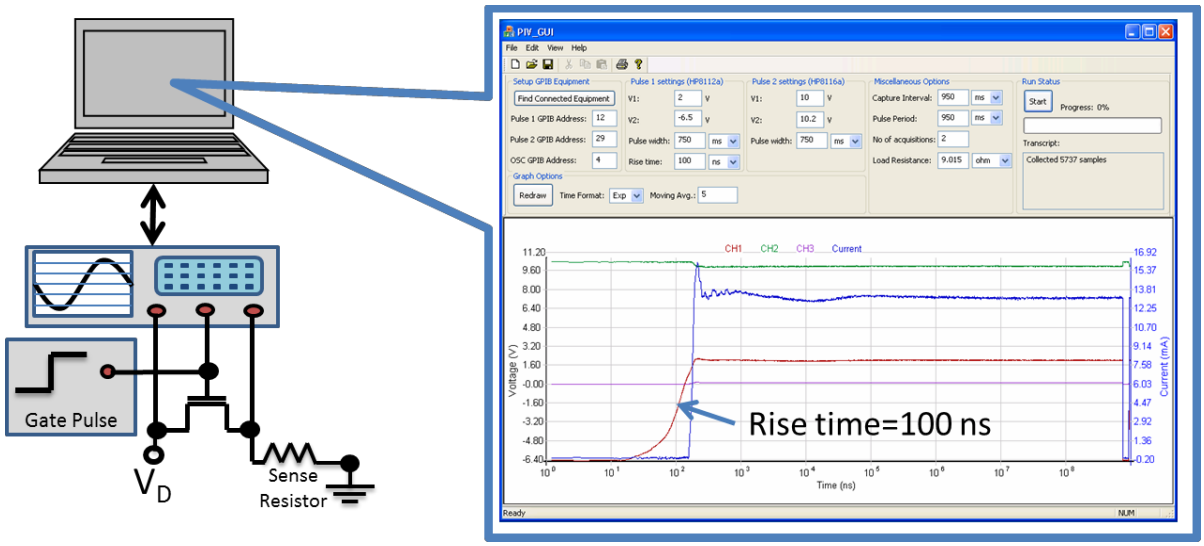


Figure 2.8: Simple schematic of the custom built pulsed-IV setup with an oscilloscope and a pulse generator [21]. Also shown is the custom designed software graphical user interface on a PC to control the instruments and acquire the transient current response.

2.5.5 Reliability tests

The greatest impediment today preventing the wide deployment of the GaN technology is its limited electrical reliability. Kim *et al.* [111] reported degradation characteristics of AlGaN HEMTs under various stress conditions such as DC stress and RF input drive stress at room temperature. At the present time, there is insufficient understanding about the fundamental mechanisms limiting reliability. Most of the GaN related degradation mechanisms are believed to be triggered by high electric fields [112], [116] and the issue exacerbates if the operation voltage increases to several hundreds of volts. One of the prerequisites for a successful implementation of GaN power electronics is the capability of developing these devices for reliable operation at different higher voltage classes established in power electronics such as 250 V, 600 V, and 1200 V in future [116].

The goals of a qualification program are two-folds: (i) to continuously drive optimization in device design, manufacturing, and material growth; and (ii) to meet and exceed the reliability levels that designers have come to expect from silicon MOSFETs. The primary source is the testing of large populations of parts, over long time intervals, under the same stress conditions that are industry standard for silicon devices. Other sources include accelerated stress testing, and analysis of field applications. The Joint Electron Device Engineering Council (JEDEC) standards for testing power transistors, such as Si MOSFETs and IGBTs, generally include high-temperature reverse bias (HTRB), high-temperature gate bias (HTGB), high-temperature storage (HTS), temperature cycling (TC), high-temperature high-humidity reverse bias (H3TRB), unbiased autoclave (AC), moisture sensitivity level (MSL), and electrostatic discharge (ESD) testing [50], [114]. The methods are well established and data has been collected over many years.

For silicon qualification the standard stress is run for 1000h, at a junction temperature of at least 125 °C. An activation energy of 0.7 eV is assumed, giving a temperature acceleration factor of 78.6 [67]. This makes a 1000h stress at a junction temperature (T_j) of 125 °C equivalent to nine years of use at T_j = 55 °C. Devices are qualified at their maximum operating voltage. For discrete power FETs, this is usually chosen to be 80 percent of the minimum breakdown voltage specification. This means that there is no voltage acceleration built into the qualification test condition and acceleration is achieved by temperature alone. This has important implications for power devices, since T_j is higher than 55 °C, typically above 75 °C. According to Tim McDonald from Infineon Technologies [69], to qualify GaN on Silicon it is insufficient to follow the existing "JEDEC standards" qualification matrix for Silicon. A different set of reliability qualification standards may be required for GaN HEMTs and even then the qualification process will likely be different for lateral and vertical GaN power devices. A path to developing new standards

specifically designed for GaN devices has been proposed in [169], [170]. Also, there are available reports on how to evaluate GaN device reliability from companies such as Texas Instrument, Infineon Technologies, and EPC [67]–[70]. In our long-term accelerated experiments, we have implemented the testing criteria specified below.

i) High Temperature Gate Bias (HTGB)

Temperature = 150 °C, V_{GS} = 7 V over V_{TH}, V_{DS} = 0.1 V, stress duration = 1000 sec.

HTGB is a stability test whereby device is subjected to a gate-source high bias (92% or 96% of $V_{GS,max}$) at the maximum rated temperature [70]. For instance, when the transistor is in the on-state with gate bias significantly higher than V_{TH} value and drain and source shorted to ground, at an elevated temperature of 150 °C. There are several mechanisms that can contribute to the failure during HTGB stress at high gate voltage. The dominant failure mechanism is an increase in off-state drain leakage resulting from gate stress induced by extended operation at high gate voltage and is highly accelerated with gate voltage. Other degradation effects include dielectric failure, and gate sidewall rupture.

ii) High Temperature Reverse Bias (HTRB)

Temperature = 150 °C, V_{GS} = 3 V below pinch-off, V_{DS} = 150 V, stress duration = 1000 sec.

HTRB is a stability test whereby device is subjected to a drain-source high bias (80% of the rated drain-source voltage) at the maximum rated temperature [70]. For instance, when the transistor is in the off-state, in voltage blocking mode with drain biased at 200 V and gate and source shorted to ground, at an elevated temperature of 150 °C. The dominant failure mechanism is a dynamic upward shift of the on-resistance, $R_{DS(ON)}$ due to high electric field. The effect is caused by electron

trapping near the conductive channel (2DEG) and in the deep buffer layers of the GaN epitaxial film. The drain bias also accelerates other degradation effects including inverse piezoelectric effect, GaN oxidation and surface dissolution, time dependent dielectric breakdown induced by defects percolative path formation, and threshold voltage shifts due to trapping [125].

2.6 Summary

In this chapter, we have discussed selection of dielectric for the gate and passivation regions of the GaN MOSHFET devices. The chapter also reviewed the fabrication and characterization methods used for this dissertation work. In order to study degradation phenomena of GaN devices, we have developed a pulsed-IV characterization setup. Successive chapters will explain more about the results obtained from HFET and MOSHFET devices using the techniques from this chapter.

CHAPTER 3: A Unified Dielectric Solution for AlGaN/GaN MOSHFET Gate and Access Regions

3.1 Introduction

GaN based transistors have been intensively reported as strong contenders for power switching and radio frequency (RF) applications [11]–[13] owing to their excellent material properties such as wide bandgap, large critical electric field, high electron mobility, high saturation velocity, and high-density two-dimensional electron gas (2DEG) induced by spontaneous and piezoelectric polarization effects [14]. However, the power performance of AlGaN/GaN heterojunction field-effect transistor (HFET) is limited by the Schottky gate which suffers from high gate leakage [17], [29], drain current collapse [26], [33], and poor long-term stability. Replacing the Schottky gate with a metal-oxide-semiconductor (MOS) structure can suppress gate leakage [13], [15]. Also, surface passivation techniques using various dielectrics have improved current collapse by reducing the density of surface states. However, several challenges still need to be resolved with the MOSHFET structure. Specifically, optimizing the dielectric material such as to reduce leakage current, eliminate current collapse, reduce capacitance–voltage (CV) hysteresis and many others, which are all, in part, a result of large interface trap densities associated with the interface between the dielectric and AlGaN [75]. Typically, two different dielectrics are used for the gate and access regions of the MOSHFET. In the gate region, the objective is to reduce leakage, minimize interface traps, maintain good gate control (on-state reliability), and to have minimal effect on threshold voltage especially when the device is stressed. In the access region, the objective is to minimize current collapse, and to provide excellent contact isolation. As this chapter shows, with proper gate stack engineering a unified dielectric solution can be achieved for the transistor.

Several groups have reported ALD SiO_2 [17], Al_2O_3 [24], HfO_2 [17], [23], [42], [44], [37]–[39], [74], [75], and HfAlO [75] as preferred choice for gate dielectrics. On the other hand, current collapse has been largely addressed by using PECVD Si_3N_4 [26], [27] in the access area of the MOSHFET. Low-*k* SiO_2 [22], [27], [28] and high-*k* dielectrics, such as HfO_2 [23], [42], [44], [37]–[39], [74], and HfAlO [22] also have been studied and have demonstrated the ability to decrease dispersion. Liu *et al.* [23], [37], [38] reported high drain current, low gate leakage, large gate voltage swing, and great immunity to current collapse on AlGaN/GaN high electron mobility transistors (HEMTs) when HfO_2 used as gate and access area dielectric, deposited by reactive sputtering. Kawano *et al.* [42] reported sufficient low gate leakage current and large conductance with HfO_2 gate and access area dielectric, deposited by pulsed laser deposition (PLD). Tokranov *et al.* [39] reported low gate leakage and low density of interface states using HfO_2 as gate dielectric and surface passivation, deposited by a reactive e-beam evaporation in ultra-high vacuum.

Atomic layer deposition (ALD) has proven the best technique to deposit dielectrics since it provides uniform, conformal, high quality films with precise monolayer thickness control [17]. Moreover, ALD without plasma induced damage helps maintain a low defect density in AlGaN/GaN bulk. Promising results for ALD HfO_2 have been reported by both Xin *et al.* [74] and Chang *et al*. [44]. However the role of oxidants has not yet been explored and could provide an effective route in further improving dielectric reliability. In this study, we deposited high-*k* HfO_2 as gate dielectric and surface area passivation using ALD technique and investigated two types of oxidants, namely, water (H_2O) and ozone (O_3) and their effect on the electrical characteristics of the transistor. Ozone oxidant is believed to optimize process conditions since water-based ALD HfO_2 can introduce hydroxyl ions (OH^-) that can be a source of trapped charges [18], [34]. The

DC performance, current dispersion characteristics, and reliability (*e.g.*, high temperature operation, V_{TH} variability) of the MOSHFET were evaluated. As will be discussed, our results showed, ozone-based ALD HfO_2 was effective in providing superior characteristics in both, gate and access regions.

3.2 Experimental Procedures

3.2.1 Device fabrication

MOSHFET devices were fabricated on AlGaN/GaN on Si substrate samples according to the process flow outlined in chapter 2, section 2.3.4. The ohmic contact resistance from transmission line model (TLM) measurements were deduced in the 10^{-5} $\Omega \cdot cm^2$ range and sheet resistance around 600 Ω/sq. This ensured good ohmic characteristics for the devices. A 20 nm thick HfO_2 gate dielectric was deposited by using a Cambridge Nanotech thermal ALD system. The precursors used were tetrakis(dimethylamino)hafnium (TDMAH), precursor with oxidant, either H_2O or O_3, at a temperature of 200 °C. HfO_2 was used as the gate dielectric as well as the passivation layer. The deposition process using each oxidant were carried out under the same conditions, such as chamber pressure, pulse time, and substrate temperature. Post deposition anneal (PDA) was performed by 60 sec RTA at 600 °C in N_2 ambient. Physical thickness of the dielectrics after ALD process was measured using variable angle spectroscopic ellipsometer (VASE) on monitor Si wafers. Film thickness of HfO_2 with water oxidant measured at 20.05 nm and that with ozone oxidant measured at 19.88 nm. A Schottky gate HFET was also fabricated as controls, according to the process flow outlined in section 2.3.3. Figure 3.1 shows the schematic cross-section of the fabricated device with a gate length (L_G) of 3 μm, gate width (W_G) of 50 μm, gate-to-source

separation (L_{GS}) of 2 µm. A matrix of seven MOSHFET devices are fabricated where gate to drain separation (L_{GD}) varies from 2 µm to 25 µm. Table 3.1 shows the device fabrication process summary. A single dielectric solution for both gate and passivation greatly simplifies the fabrication process. Grazing angle X-ray Diffraction (GA-XRD) was performed using Rigaku SmartLab X-ray diffractometer with parallel beam optics. DC IV measurements were performed using Keithley 4200−SCS and CV measurements were performed using HP 4284A precision LCR meter. Current collapse was measured via pulsed I_{DS}−V_{DS} using HP 8112A, HP 8116A pulse generators and a Tektronix TDS−420 oscilloscope.

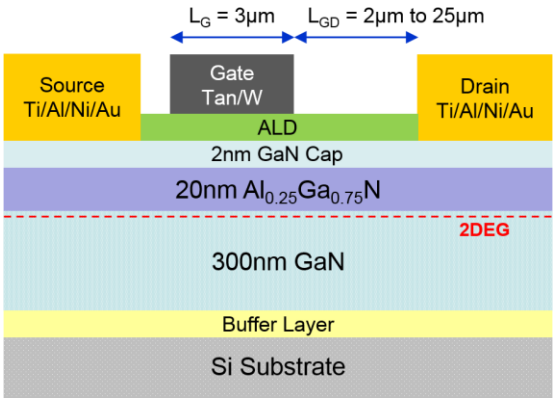


Figure 3.1: Schematic cross-sectional view of the fabricated AlGaN/GaN MOSHFET [16].

Table 3.1: Device fabrication process summary

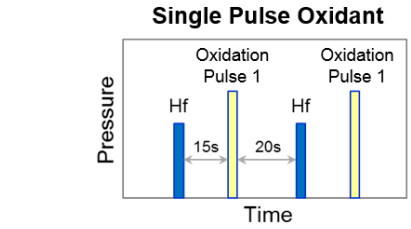
Gate length x width (L_G x W_G) = 3 µm x 50 µm
Gate-to-source separation (L_{GS}) = 2 µm
Gate-to-drain separation (L_{GD}) = 2 µm to 25 µm

Mask	Process step	Process detail	Thicknes
1	Mesa isolation	RIE $SiCl_4/Cl_2$	430nm
2	Ohmic metallization	Ti/Al/Ni/Ti/Au	245nm
	Ohmic RTA	850 °C, 30sec, N_2	
	ALD dielectric deposition	HfO_2 (TDMAH + O_3/H_2O) @ 200 °C	20nm
	PDA	600 °C, 60sec, N_2	
3	Schottky metallization	TaN/W	140nm
4	Ohmic cnt window	RIE BCl_3	20nm

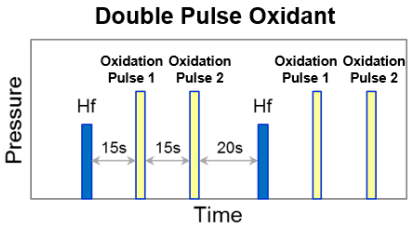
3.2.2 Design of experiment

We deposited a 20nm ALD HfO_2 with an 8-way oxidation split, as shown in Figure 3.2. H_2O and O_3 oxidants were investigated for the ALD deposition. In addition to single pulse of H_2O and O_3 oxidants, we also explored double-pulse and modified the order of the oxidants, such as O_3−O_3, H_2O−H_2O, H_2O−O_3, and O_3−H_2O. Finally, the role of PDA was investigated also in order to explore the role of microstructure on dielectric quality. In many cases, amorphous materials are

preferred to crystalline, since crystalline materials may be characterized by grain boundaries [101]. These defects serve as tunneling paths or trapping states and thus mitigate the effectiveness of the dielectric. Single crystal structures, on the other hand, may be promising but often require high temperature deposition as well as consideration of the lattice mismatch between the semiconductor and insulator. If lattice is not well matched it may result in a high concentration of structural defects at the interface.



GaN	PDA
Single Pulse H2O (SPH)	Yes
Single Pulse H2O (SPHN)	No
Double Pulse H2O-H2O (DPHH)	Yes
Double Pulse H2O-Ozone (DPHO)	Yes



GaN	PDA
Single Pulse Ozone (SPO)	Yes
Single Pulse Ozone (SPON)	No
Double Pulse Ozone-Ozone (DPOO)	Yes
Double Pulse Ozone-H2O (DPOH)	Yes

Figure 3.2: Split table and animation showing examples of single-pulse and double-pulse oxidant ALD HfO_2 process.

3.3 Physical Characterization of ALD HfO_2 Film

The crystalline structure of the ALD dielectrics were analyzed by grazing angle X-ray diffraction (XRD) measurements. Figure 3.3 shows comparison of the XRD spectra for ALD HfO_2 using H_2O oxidant, O_3 oxidant, and reference from JCPDS card no. 04-005-6162 (relative intensity vs. angle 2-Theta). Both films showed representative monoclinic HfO_2 characteristics. Both process conditions showed peak intensities at 18°, 32° and 36° corresponding to (100), (111), and (200) phase. However, peaks for HfO_2 with O_3 oxidant were suppressed at 25°, 28°, 39°, and 41°

corresponding to 011, $\bar{1}11$, 021, and $\bar{2}11$, especially in the case of O_3 oxidant. This could be attributed to the fine grain size, preferred orientation or less crystalline nature originated from the strong oxidation during the ALD reaction. It is clear that O_3 with its high volatility is a strong reactant for the ALD process [30].

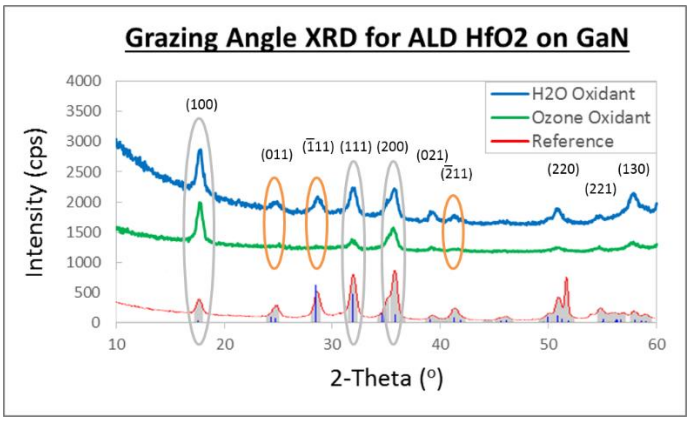


Figure 3.3: Comparison of the XRD spectra for ALD HfO_2 using H_2O oxidant, O_3 oxidant, and JCPDS reference [16].

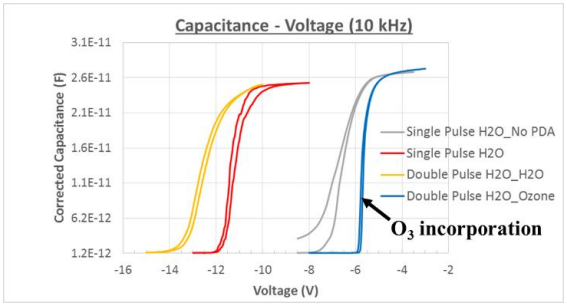
3.4 Electrical Characterization of ALD-HfO_2 MOSHFET

3.4.1 Capacitance-voltage (CV) characteristics

The CV characterization, shown in Figure 3.4, was performed on MOS capacitors with 100 µm x 100 µm square area. The sharp transition from 2DEG accumulation to depletion demonstrates unpinning of the Fermi level at the HfO_2/HEMT interface, indicating a high quality interface status [24]. Capacitance plateaus due to the 2DEG located at the AlGaN/GaN interface. Figure 3.4(a) shows CV for ALD HfO_2 resulting from H_2O incorporation either as a single-pulse oxidant or as the first oxidant in a series of double-pulse splits. Two primary observations are i) the threshold voltage (V_{TH}) variation extends over a large range, -6V to -14V, and ii) the devices that incorporate

O_3 oxidant shows half the hysteresis compared to the devices that do not. The hysteresis values were around 0.2V and 0.1V when H_2O and O_3 precursors were used, respectively. This is consistent with studies on Silicon where Park *et al*. [32] showed that HfO_2 film deposited using O_3 ALD oxidant exhibited superior electrical properties than that grown with H_2O ALD oxidant, including fixed charge density, interface trap density, leakage current density and hysteresis. Kim *et al*. [35] also reported Al_2O_3 films grown on Si substrates using O_3 as oxidant to show smaller hysteresis, lower leakage current density, and higher breakdown field strength compared to those using H_2O as oxidant. The Al_2O_3 films grown using O_3 oxidant was found to contain less defects in comparison with films using H_2O oxidant. The hysteresis of a MOS capacitor is attributed to the trapping and detrapping of charges related to film defects that slowly respond to a voltage sweep. It was also reported that AlGaN surface may be effectively passivated by supplying only O_3 without inducing damage, which leads to improved interface quality [20]. Figure 3.4(b) shows CV graphs with ALD HfO_2 resulting from O_3 incorporation either as a single-pulse oxidant or as the first oxidant in a series of double-pulse splits. For this split group the V_{TH} variation was very low, -6V to -4V, and hysteresis values remained small, validating the earlier observation. The V_{TH} shift towards positive voltage direction has been reported in ALD films deposited using O_3 as an oxidant [20].

(a)



(b)

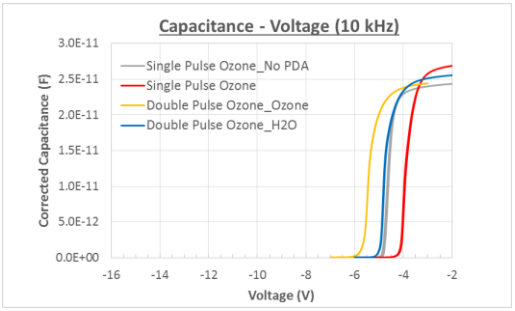
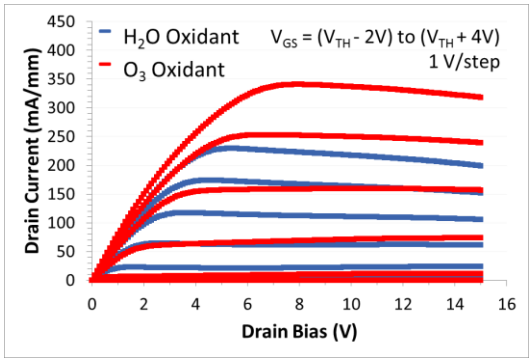


Figure 3.4: CV characteristics of oxidant splits (a) H_2O incorporation either as a single-pulse oxidant or as the first oxidant in a series of double-pulse splits, and (b) O_3 incorporation either as a single-pulse oxidant or as the first oxidant in a series of double-pulse splits.

3.4.2 DC current-voltage (IV) characteristics

Devices with L_G x W_G = 3 x 50 µm, L_{GS} = 2 µm, and L_{GD} = 15 µm were characterized for their performance. As shown in Figure 3.5(a), good saturation and pinch-off characteristics were obtained. The negative output conductance under high gate biases ($V_{GS} - V_{TH} >> 0$) is due to self-heating; however, the effect is lot less pronounced here owing to the good thermal conductivity of the Si substrate compared to other substrates, such as sapphire [24]. MOSHFETs with O_3 oxidant exhibited a maximum saturation drain current ($I_{DS,max}$) of 340 mA/mm at a gate bias of +4V. Whereas, MOSHFETs with H_2O oxidant exhibited $I_{DS,max}$ of 240 mA/mm at the same bias condition. The higher $I_{DS,max}$ of O_3 oxidant based MOSHFETs is attributed to cleaner interface with less surface states affecting the 2DEG. The values of specific on-resistance ($R_{on,sp}$) were extracted from the linear region of the I_{DS}–V_{DS} curves at V_{GS} 3V over pinch-off bias. $R_{on,sp}$ was plotted as a function of L_{GD}, as shown in Figure 3.5(b). The devices with L_{GD} = 15 µm showed 20% lower $R_{on,sp}$ when O_3 used as oxidant vs. H_2O, decreasing from 4 mΩ·cm^2 to 3 mΩ·cm^2. This is a significant enhancement in performance that should directly translate to lower conduction loss; *i.e.*, higher efficiency in power switching applications.

(a)



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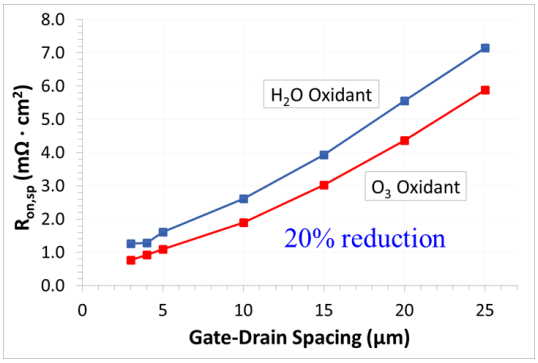


Figure 3.5: Comparison of two oxidants for (a) output characteristics (I_{DS}–V_{DS}), and (b) extracted specific on-resistance of the AlGaN/GaN MOSHFETs [16].

For the device transfer characteristics, the transconductance (g_m) and threshold voltage (V_{TH}) were investigated as a function of gate bias V_{GS}. Figure 3.6 shows I_{DS}–V_{GS} and corresponding intrinsic transconductance. V_{TH} is defined as the gate voltage (V_{GS}) at which the drain current (I_{DS}) = 1 mA/mm. The results were compared with an unpassivated AlGaN/GaN HFET. The negative shift in the V_{TH} of MOSHFETs is due to the decreased gate barrier capacitance. However, the devices using H_2O oxidant realized much larger V_{TH} increase compared to the devices using O_3 oxidant. The V_{TH} values were -12.1V, -4.75V, -2.95V for MOSHFET using H_2O oxidant, MOSHFET using O_3 oxidant, and HFET, respectively. The large negative V_{TH} increase in the case of H_2O oxidant is attributed to incorporating higher density of positive ions, probably hydrogen, during deposition [20]. The additional surface charge at the HfO_2/AlGaN interface decreases the voltage drop across the AlGaN barrier layer thus increasing the threshold voltage. The higher density of positive ions can be explained by the ALD chemistry whereby employing O_3 as an oxygen precursor reduces the hydroxyl impurities (OH^-) and residual hydrogen, which leads to the reduced bulk and interface traps [18]–[20], [30]–[32], [34]. Niinistö *et al.* [31] and Kim *et al.* [35] reported superior HfO_2 film quality with reduced H contents when O_3 used as oxygen precursor instead of H_2O.

Using the same principles, the V_{TH} shift towards less negative direction has been reported in the case of ALD films employing O_3 oxidant [20]. This causes the devices with O_3 oxidant to exhibit higher current and lower R_{on}. The peak transconductance value achieved for devices using O_3 oxidant was higher at 112.66 mS/mm compared to 81.38 mS/mm for devices using H_2O oxidant or, 81.38 mS/mm for the unpassivated HFET. An unpassivated HFET with higher density of surface traps depletes 2DEG in the drift region hence, transonductance degraded. Using O_3 oxidant also helped to reduce gate leakage (I_{GS}), as shown in Figure 3.7. At 6V below pinch-off bias gate leakage for devices with H_2O oxidant was $1.7x10^{-4}$ A/cm^2 whereas that in devices with O_3 oxidant was $5.4x10^{-6}$ A/cm^2, larger than an order of magnitude difference, owing to cleaner interface and bulk quality of the film. This is consistent with other references where 1−2 order reduction in leakage current density was reported due to O_3 oxidant [34]–[36]. While the leakage current values in our experiment were on par with other publications [42], [43], it is worth mentioning that some authors have reported even lower gate leakages [23], [44], [45]. The better leakage characteristics are likely due to the lower temperature processing of HfO_2 to avoid crystallization and high level of residual carbon impurity at the interface [40], [41].

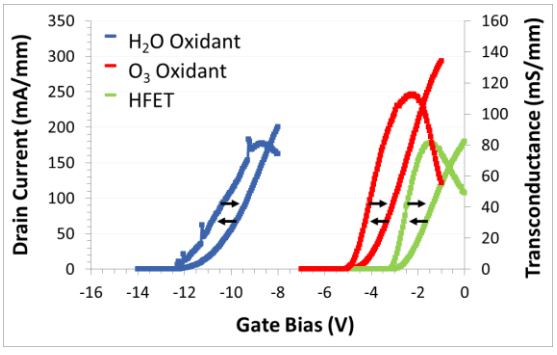


Figure 3.6: Comparison of the transfer characteristics for AlGaN/GaN MOSHFETs using H_2O oxidant, O_3 oxidant, and an unpassivated HFET [16].

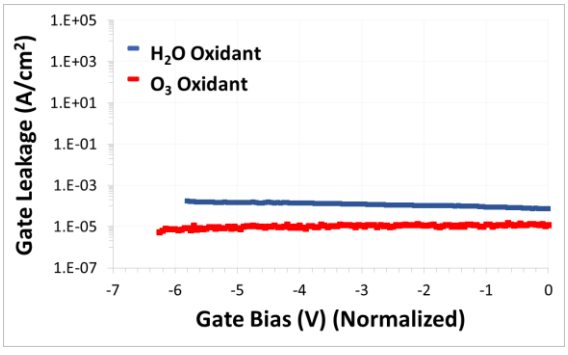


Figure 3.7: Comparison of the MOSHFET gate leakage between two oxidants.

3.4.3 Temperature dependence

We also conducted a temperature study where transistor DC characteristics were evaluated while temperature was increased from room temperature (~23 °C) up to 200 °C. Figure 3.8 shows $R_{on,sp}$, threshold voltage, peak transconductance, gate leakage, and drain leakage variation as a function of temperature. The two oxidant groups were found equivalent for variation in peak transconductance, gate leakage, and drain leakage as a function of temperature. However, MOSHFETs with O_3 oxidant demonstrated less R_{on} and V_{TH} variation compared to that with H_2O oxidant. The effect of traps exacerbates at elevated temperature. Hence, it is important for a transistor to start with a cleaner surface, as provided in the case of O_3 oxidant, in order to avoid the repercussions of hot electron effects and traps with increasing temperature.

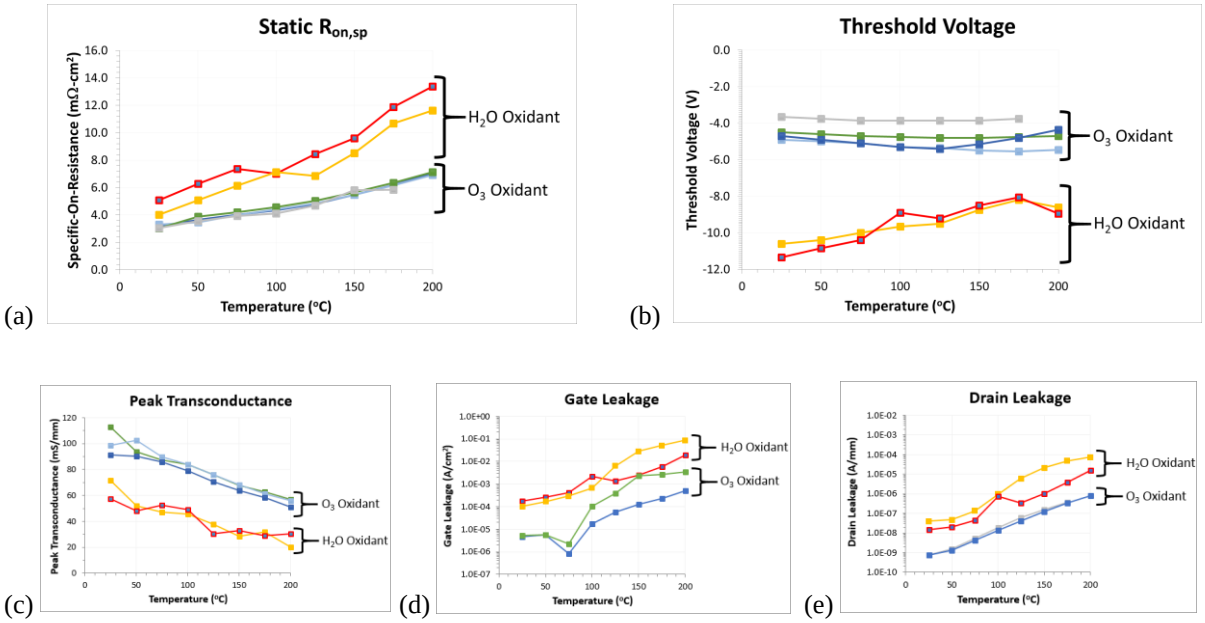


Figure 3.8: Comparison of two oxidants for (a) static R_{ON} variation, (b) V_{TH} variation, (c) peak transconductance variation, (d) gate leakage variation, and (e) drain leakage variation of the AlGaN/GaN MOSHFETs as a function of temperature.

3.4.4 High temperature reverse bias (HTRB) stress test

We carried out HTRB stress experiments on the GaN MOSHFETs with DC reverse-bias drain acceleration. The devices have been electrically stressed in the off-state (gate-to-source bias, V_{GS}, 3V below V_{TH}) with drain-to-source bias V_{DS} = 150V at environmental temperature of 150 °C. This is one of the key tests to evaluate long-term reliability of power devices. It is worth noting that the Joint Electron Device Engineering Council (JEDEC) standard for HTRB test is 1000 hours to reflect standard operation over 10 years. In our study, the stress time was increased up to 1000s.

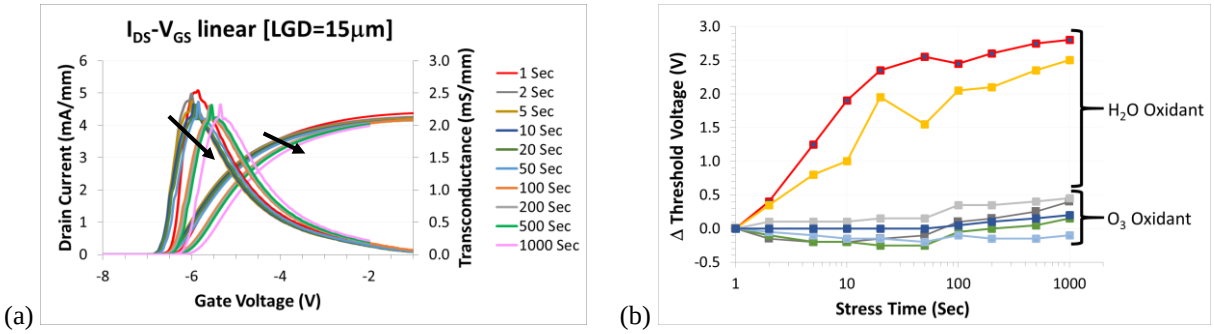


Figure 3.9: (a) A typical transfer and transconductance curves during HTRB stress, and (b) comparison of the MOSHFET ΔV_{TH} as a function of HTRB stress time between the two oxidant groups [16].

Figure 3.9(a) shows a typical transfer characteristics in the linear region where transconductance g_m decreases and threshold voltage V_{TH} shifts positive after HTRB stress. This observation is consistent with what other authors have reported [114]. However, Figure 3.9(b) shows a significant difference in V_{TH} stability between the two oxidant types. A high interface trap density is the leading cause of threshold voltage instability [75]. A significant device drift, with change in the threshold voltage and transconductance can be correlated to material quality (pre-existing deep levels on the surface and at interfaces) or process-induced instabilities, especially in connection with compensating species (Fe or C), contaminants like H, F, O, or defects [125]. The variation in

V_{TH} corresponds to the reduction of the 2DEG in the channel. We postulate that the positive shift in the transfer curve is attributed to negative impurity ion trapping at the interface (*e.g.*, hydroxyl ion), during stress, that is dominant in the case of H_2O oxidant. For the devices with O_3 oxidant, the reduced interface states led to more stable V_{TH} even at longer stress duration. A minimal V_{TH} drift (< 0.5V) was achieved under stress in the case of O_3 oxidant as compared to a much larger V_{TH} drift (2.5V) in the case of H_2O oxidant. These results clearly portray that using ozone oxidant is effective both in reducing the HfO_2/AlGaN interface states and improving the electrical reliability properties of the MOSHFETs.

3.4.5 DC/RF dispersion / current collapse – gate lag measurement

Current collapse also known as dynamic on-resistance is a critical reliability metric for GaN devices which essentially means a decrease in the maximum drain current together with an increase in the knee voltage and the on-resistance when the devices operate under large-signal microwave frequencies or pulsed conditions. Gate lag measurement is sensitive to surface states and thus helps evaluate the passivation region of the GaN device. We used a custom configuration to assess current collapse. A HP pulse generator was used to apply short pulses to the gate, with a rise time of 100 ns, to turn the device from off-state to on-state. The devices were biased in the saturation region with the drain voltage held at a constant DC 10 V throughout the measurement. A Tectronix oscilloscope was used to monitor gate, drain, and source voltage waveforms and to study drain current response. The set-up is shown in the Figure 3.10. In theory, the pulsed drain current during on state should be identical to the DC value. However, owing to the surface trapping and detrapping of electrons, HEMTs and MOSHFETs both display a lag in current recovery between DC and pulsed-mode data.

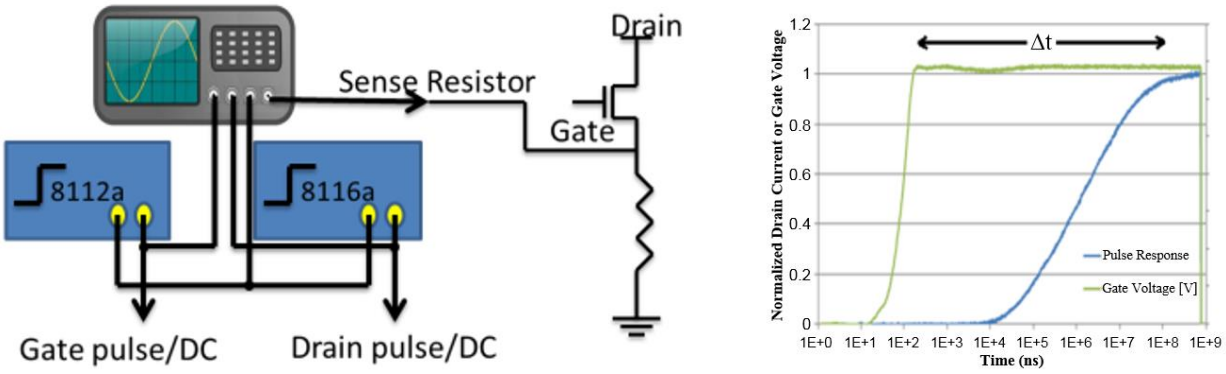


Figure 3.10: Hardware test configuration to measure current collapse. Graph on the right shows example gate pulse with a sharp rise time and drain current response recovering to steady state value.

Figure 3.11(a) shows current collapse of the test samples at room temperature. A significant delay in drain current recovery is observed in the case of unpassivated HEMT. A MOSHFET structure is effective at passivating the surface traps and thereby reducing hot-electron degradation. Devices with H_2O oxidants showed slightly better current collapse recovery compared to the unpassivated HEMT. Devices with O_3 oxidants showed significant improvements. Specifically, H_2O oxidant took 20 ms to achieve 90% drain current recovery whereas O_3 oxidant took around 0.1 ms to achieve 90% drain current recovery; an extraordinary 200x improvement. This supports the hypothesis made by other authors where ALD dielectric film using O_3 oxidant was found to produce less interface trap density compared to H_2O oxidant [32], [34]. Figure 3.11(b) shows DC/RF dispersion tests performed at an elevated temperature (150 °C) where devices with O_3 oxidants consistently outperformed H_2O oxidant counterparts.

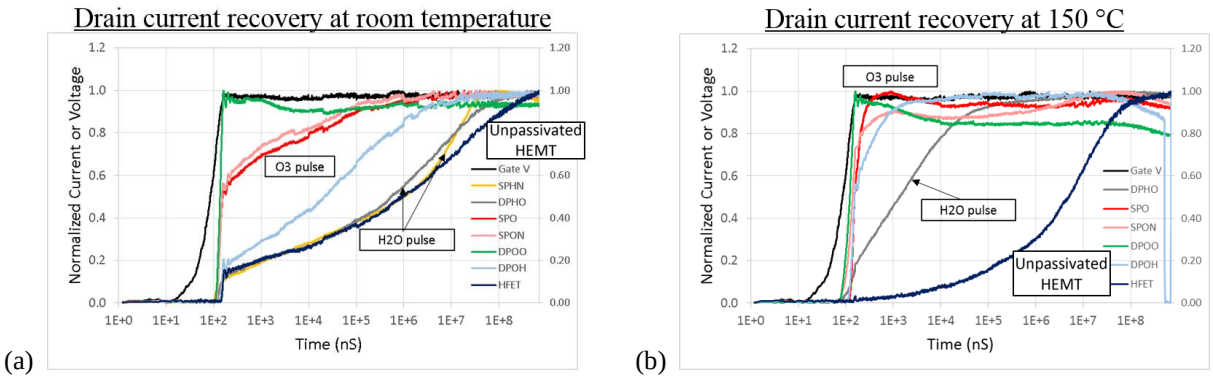


Figure 3.11: DC/RF dispersion: gate lag at (a) room temperature, and (b) elevated temperature, 150 °C.

Note the direction of current collapse as temperature is increased to 150 °C. For certain dielectrics, devices experience higher current collapse or dynamic $R_{DS(on)}$ when exposed at high temperature [25]. Such worsening is evidenced by the unpassivated HEMT in our experiment. Although counterintuitive, MOSHFETs, irrespective of O_3 or H_2O oxidant, showed better current collapse behavior at elevated temperature. This can be explained by MOSHFET traps at elevated temperature getting closer to conduction band edge and hence electrons detrapping faster. Also, note the near ideal behavior in the case of double-pulse O_3 oxidant. The drain and gate leakage components of the test were found reasonable indicating this was not a leaky device. This indicates a double-pulse O_3 further reduces interface traps.

Figure 3.12 depicts the mechanism of ALD physical chemistry. It is common to use H_2O oxidant for ALD to deposit metal oxides while at the same time, most ALD precursors are very sensitive to water [36]. H_2O or hydroxyl group (OH^-) tends to be strongly physisorbed on all surfaces of the ALD reactor. Since O_3 is a stronger oxidizer than H_2O, the surface reaction is more complete with lower impurity contents [31] and ligands terminated. With a double-pulse, the oxygen vacancies

and the hydrogen terminations left behind can be even more effectively filled with repeated exposure to oxygen molecules.

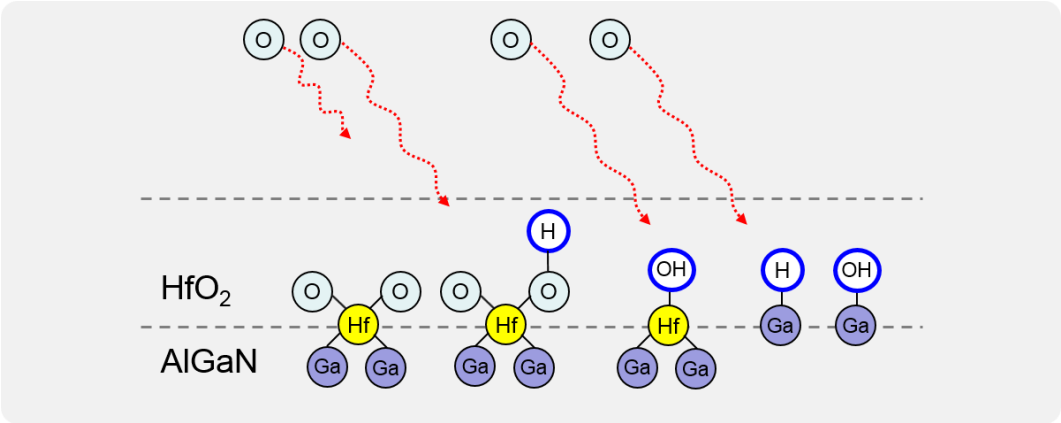


Figure 3.12: Illustration of the ALD physical chemistry and the oxygen molecules terminating hydrogen and OH^- bonds.

3.5 Summary

ALD−HfO_2/AlGaN/GaN MOSHFETs were fabricated using H_2O and O_3 as oxygen precursors, and their DC and pulsed IV characteristics were investigated. Several authors have reported such characteristics of AlGaN/GaN MOSHFETs showing improvements on dielectric and interface properties when O_3 precursor used; however, there are no reports on parametric variability with increasing temperature nor publications on reliability items such as HTRB. Our comparative analysis reveals that ozone based ALD results in improved device performance and enhances reliability compared to water based ALD. Ozone is a strongly-reactive oxidizing agent with high volatility. The use of O_3 as an oxygen precursor for ALD HfO_2 deposition reduces the formation of hydroxyl impurities (OH^-) and residual hydrogen during growth, which leads to reduced bulk and interface traps. These hydroxyl groups degrade the electrical property of the high-*k* oxide film.

An electrical data summary between the two oxidant groups is captured in Table 3.2. O_3 oxidant based devices yield lower hysteresis, V_{TH} with less negative shift, higher drain current, lower R_{on}, higher transconductance, lower gate leakage, better HTRB behavior, and better current collapse recovery compared to water oxidant based devices. Also, using ozone provides more stable Ron and V_{TH} over temperature gradient up to 200 °C. With these traits, ALD HfO_2 can be used not only in the gate region but also in the access region, thus enabling a unified dielectric solution for the GaN device.

Table 3.2: Electrical characterization – data summary

	ALD HfO_2	
	H_2O oxidant	**O_3 oxidant**
Hysteresis (V)	0.2 ~ 0.25	0.05 ~ 0.12
Threshold voltage (V)	-12.1	-4.75
Max drain current (mA/mm)	240	340
$R_{on,sp}$ ($m\Omega \cdot cm^2$) at L_{GD} = 15µm	3.8	3
Peak transconductance (mS/mm)	81.38	112.66
Gate leakage (A/cm^2)	$1.7x10^{-4}$	$5.4x10^{-6}$
HTRB V_{TH} variation (V) at 150 °C	2.5	< 0.5
Current collapse; 90% recovery (mS) at room temp	15 ~ 20	0.1

CHAPTER 4: High Temperature Operation of GaN-on-Si MOSHFETs with ALD Hafnium Oxide (HfO_2)

4.1 Introduction

As has been mentioned in chapter 1, wide bandgap (WBG) transistors offer the potential for high electron mobility transistors (HEMTs) that are suitable for high-power and high-temperature operations [10]. This is because of the low carrier generation rate by thermal activation and high breakdown fields in the WBG semiconductors [85]. Daumiller *et al*. [78] evaluated the stability of AlGaN/GaN HFETs under high-temperature stress up to 800 °C. High temperature MOSHFET studies have also been performed on SiC [80], [83], [84], and sapphire substrates [82]. However, to the best of our knowledge, there has been limited temperature investigation on GaN-on-Si MOSHFET structures, and the authors used SiO_2 [81], HfAlO [79], or SiN_x [86] for gate and surface passivation. HfO_2 is one of the popular dielectrics that has been greatly favored in the gate and passivation regions [16], [23], [37]–[39], [42]–[45], [71]–[75]. This chapter provides a systematic study of the electrical characteristics of AlGaN/GaN HFET and ALD HfO_2 MOSHFETs at elevated temperatures. In addition, further optimization of the gate dielectric thickness was attempted to provide higher input gate capacitance in order to gain more control of the channel. Lowering physical dielectric thickness (T_{ox}) is one way to increase the gate-channel capacitance that could, in turn, result in a more efficient conductivity modulation [37]; *i.e.*, higher transconductance. Static characteristics of GaN transistors on silicon substrate were investigated as a function of ambient temperature (*T*), via on-wafer probing with a heated aluminum wafer chuck, in the temperature range of 23–200 °C. The results were compared amongst MOSHFETs and reference AlGaN/GaN HFET processed on the same wafer and of identical geometry. The

high-temperature measurements were made in a nitrogen pressurized chamber to avoid possible oxidation of contact material and probes. The depletion-mode devices were characterized for output and transfer characteristics including drain current (I_{DS}), threshold voltage (V_{TH}), transconductance (g_m), hysteresis, drain leakage and gate leakage. In our experiment, four different piece parts were fabricated including an HFET and MOSHFETs with 3nm ALD HfO_2, 8nm ALD HfO_2, and 20nm ALD HfO_2. A comparative study of the current-voltage characteristics is discussed below.

4.2 Output Characteristics as a Function of L_{GD}, *T*, T_{OX}

Figure 4.1(a) and (b) show output characteristics as a function of temperature for HFET and MOSHFET, respectively. At room temperature and V_{GS} 4 V over pinch-off, HFET yielded a saturation drain current I_D of 225 mA/mm and MOSHFET yielded 330 mA/mm. At 200 °C HFET exhibited 42% and ALD HfO_2 MOSHFETs exhibited 48% of their saturation drain current evaluated at room temperature. The thermal impact on the maximum drain current I_{Dmax} can be approximated by a linear temperature dependence [85]:

$$I_{\mathrm{Dmax}}(T) = I_{\mathrm{Dmax}}(T = 300\,\mathrm{K}) \cdot (1 - \alpha \cdot T) \tag{4.1}$$

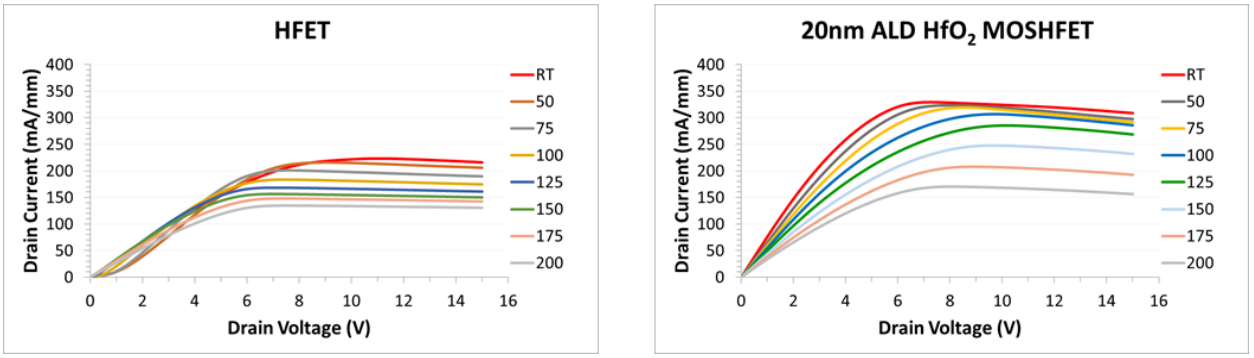
The coefficient α is typically of the order of 10^{-3} K^{-1}. Mostly the combined effect of carrier mobility and saturation velocity, which both decrease with increased temperature, is invoked to describe the temperature dependent performance of these devices [80], [82], [84]. Figure 4.2(a) and (b) show extracted specific on-resistance as a function of L_{GD} and *T* for various dielectric thicknesses (T_{ox}). Drain current, I_{DS}, decreases with increasing L_{GD} since series resistance increases in the drift region. The mobility reduction with HfO_2 MOSHFETs shows stronger temperature dependence

than that with the HFET device and this could be attributed to the additional scattering component with temperature caused by the high-k layer such as remote phonon scattering [77], [79]. The ideal specific on-resistance is given by [5]

$$R_{ON} = \frac{4BV^2}{\mu\varepsilon E_c^3} \tag{4.2}$$

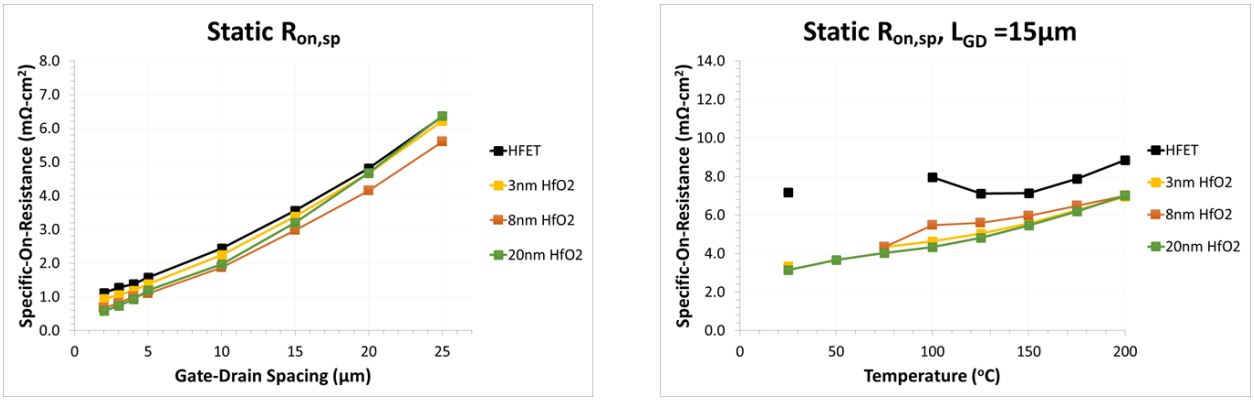
where BV is the breakdown voltage, μ is the mobility, ε is the dielectric constant, and E_c is the critical electric field for breakdown. μ, in the denominator, has a $T^{-3/2}$ dependence [78].

The values of specific on-resistance, $R_{on,sp}$, were extracted from the linear region of the I_{DS}–V_{DS} curves at V_{GS} 4V over pinch-off bias. Notice, HFET R_{on} at L_{GD} = 15 µm, at room temperature, increased from 3.6 mΩ·cm^2 in Figure 4.2(a) to 7.2 mΩ·cm^2 in Figure 4.2(b). The measurements were taken 2.5 months apart. The corresponding I_{DS} decreased ~15%, from 260 mA/mm to 225 mA/mm. This degradation is likely due to open passivation area affected by moisture and thermally grown oxide.



(a) (b)

Figure 4.1: Output characteristics of (a) HFET and (b) 20nm ALD HfO_2 MOSHFET, as a function of temperature (L_{GD} = 15 µm).



(a) (b)

Figure 4.2: Extracted static $R_{on,sp}$ of HFET and MOSHFETs plotted as a function of (a) L_{GD}, at room temperature and (b) substrate temperature at L_{GD} = 15 µm.

4.3 Transfer Characteristics as a Function of L_{GD}, *T*, T_{OX}

4.3.1 Threshold voltage (V_{TH}) variation

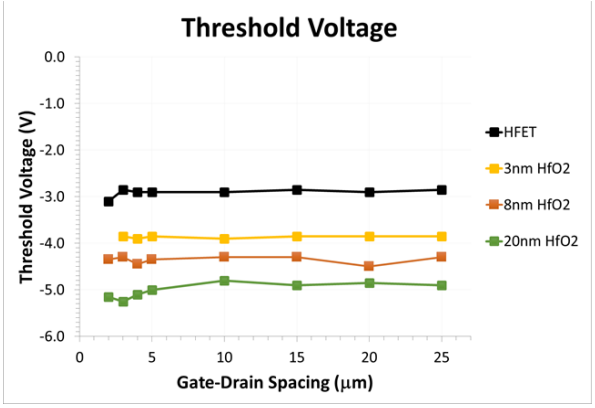
Figure 4.3(a) and (b) show threshold voltage (V_{TH}) variation as a function of L_{GD} and *T* for various T_{ox}. V_{TH}, was measured at 1mA/mm with V_{DS} = 0.1V. MOSHFETs show higher V_{TH} than HFET due to additional capacitance from the dielectric.

$$\frac{1}{C_{\mathrm{MOSHFET}}} = \frac{1}{C_{\mathrm{OX}}} + \frac{1}{C_{\mathrm{HEMT}}} \tag{4.3}$$

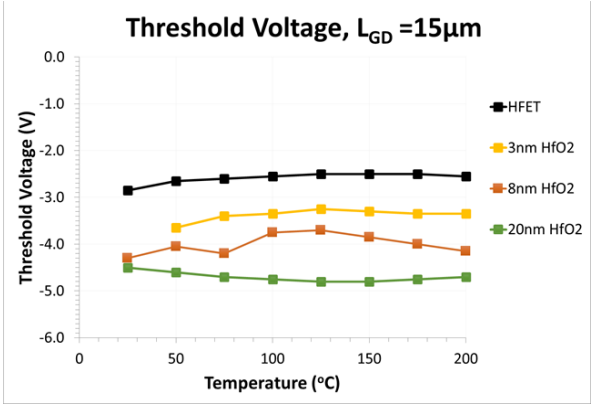
where $C_{OX} = \varepsilon_0 \varepsilon_r A/T_{OX}$, ε_0 is the vacuum permittivity, ε_r is the dielectric constant, *A* is the area of capacitor, and T_{OX} is the dielectric thickness. As T_{OX} increases $C_{MOSHFET}$ decreases.

Threshold voltage remains relatively unchanged as a function of L_{GD} since it is strictly governed by the characteristics in the drift region directly below gate. In our temperature experiment, V_{TH} variation between HFET and MOSHFETs were analogous and was approximately linear with

temperature; 0.5 to 1 mV/°C. Figure 4.4(a) and (b) show transfer characteristics of GaN HFET and 20 nm ALD HfO_2 MOSHFET at a constant L_{GD} = 15 µm and as a function of *T*. At room temperature, a good pinch-off at about –3 V and –5 V was observed for HFET and MOSHFET, respectively.

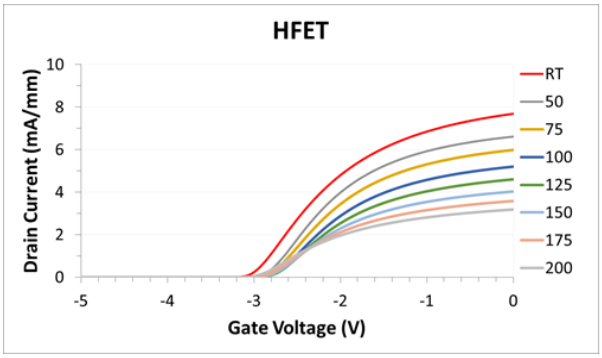


(a)

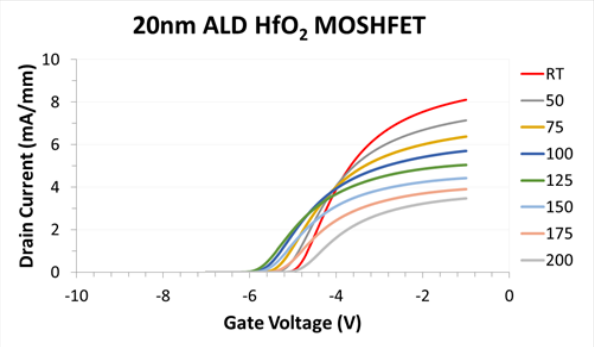


(b)

Figure 4.3: Threshold voltage (V_{TH}) of HFET and MOSHFETs plotted as a function of (a) L_{GD}, at room temperature and (b) substrate temperature at L_{GD} = 15 µm.



(a)

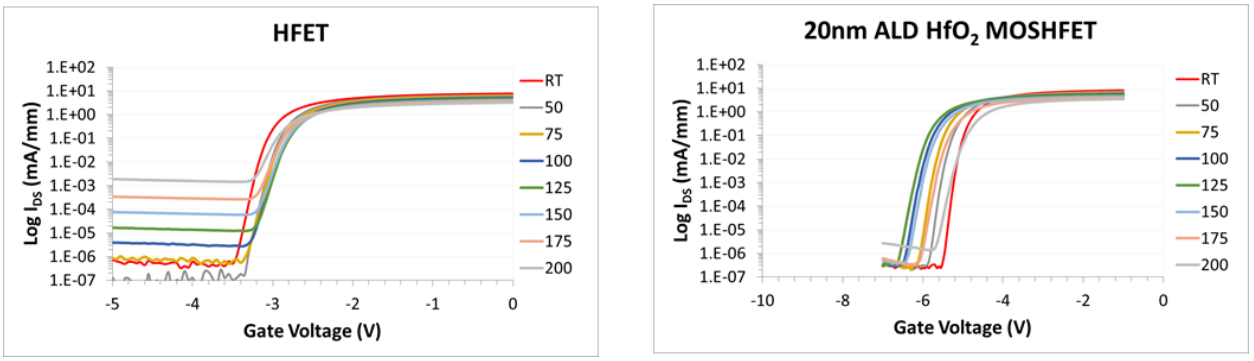


(b)

Figure 4.4: I_{DS}-V_{GS} (linear-mode) of (a) HFET and (b) 20nm ALD HfO_2 MOSHFET, as a function of temperature (L_{GD} = 15 µm).

4.3.2 Off-state leakage variation

It is generally shown that off-state leakage current increases due to the increase in tunneling current or thermionic emission current [17]. Following this principle, HFET off-state leakage increased 3 orders of magnitude going from room temperature to 200 °C, as shown in Figure 4.5(a). On the contrary, off-state leakage in MOSHFET remains practically unchanged, as shown in Figure 4.5(b). The suppression in MOSHFET off-state leakage is explained by the conduction band offset between the oxide and the AlGaN barrier layer.



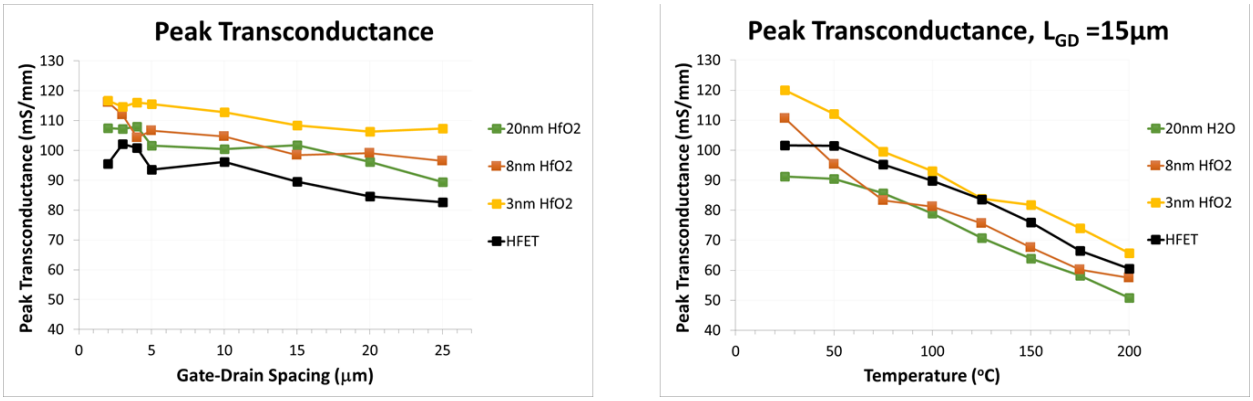
(a) (b)

Figure 4.5: Logarithmic plot of I_{DS}-V_{GS} (linear-mode) showing off-state leakage (a) HFET and (b) 20nm ALD HfO_2 MOSHFET, as a function of temperature (L_{GD} = 15 µm).

4.3.3 Peak transconductance ($g_{m,max}$) variation

Peak transconductance (g_m) is measured in the saturation mode with V_{DS} = 5V. Peak g_m decreases with increasing L_{GD} due to increase in series resistance. Peak g_m also decreases with elevated temperature as mobility of the channel electron is reduced due to phonon scattering [80], [82]–[84]. The room temperature transfer characteristics of the analyzed devices at L_{GD} = 15 µm yielded a peak transconductance, $g_{m,max}$, of 90 mS/mm and 100 mS/mm for HFET and MOSHFET

respectively, as illustrated in Figure 4.6. At 200 °C the HFET and MOSHFETs exhibited ~45% of their peak transconductance evaluated at room temperature. MOSHFETs showed similar linear sensitivity as HFET as a function of L_{GD} and temperature. As HfO_2 thickness decreases, peak g_m increases, as expected. The higher conductivity modulation is due to higher capacitance [37].



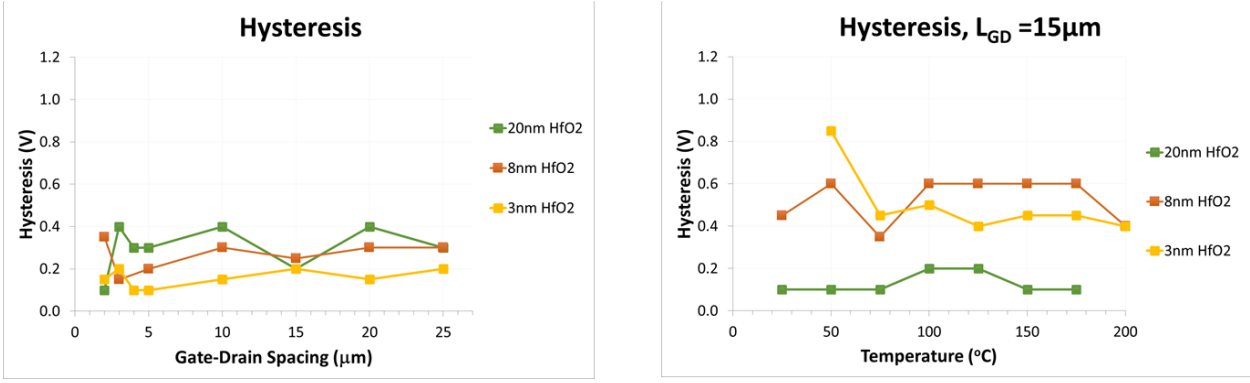
(a) (b)

Figure 4.6: Peak transconductance of HFET and MOSHFETs plotted as a function of (a) L_{GD}, at room temperature and (b) substrate temperature at L_{GD} = 15 µm.

4.4 Hysteresis as a Function of L_{GD}, *T*, T_{OX}

MOSHFET, with a dielectric layer inserted between gate metal and AlGaN barrier layer, tends to induce trap states at the dielectric/AlGaN interface as well as in the bulk. These interface states can trap electrons during measurements causing a clockwise hysteresis. An assessment of on-state gate stack reliability was performed by looking for signs of hysteresis in DC transfer characteristics, and the resulting threshold voltage instability. Figure 4.7 shows the representative measurements for ALD HfO_2 dielectrics as a function of L_{GD} and temperature. In our tests, there was no apparent L_{GD} or temperature effect on hysteresis for any of the ALD HfO_2 splits. Values at room temperature stayed low between 0.1V and 0.4V with only 0.1V to 0.2V variation at

elevated temperature. As oxide thickness increases, so does hysteresis due to increase in defect density introduced by HfO_2, as seen in Figure 4.7(a). However, Figure 4.7(b) flips the results. This is an artifact since devices with thinner dielectrics underwent stress tests prior to temperature study that could have introduced additional defects.

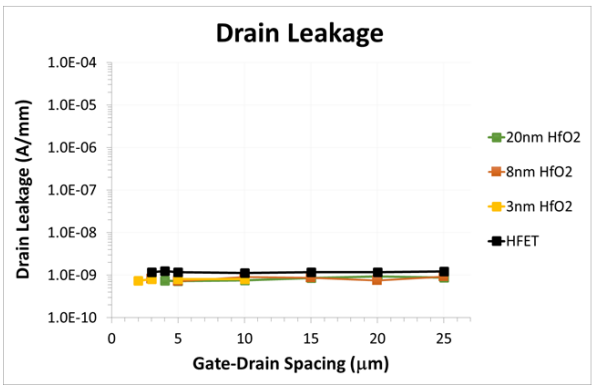


(a) (b)

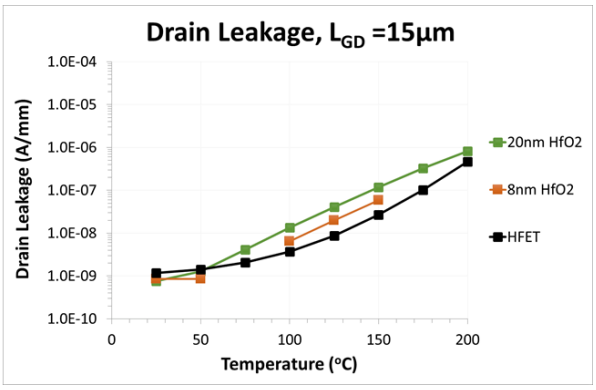
Figure 4.7: Hysteresis of HFET and MOSHFETs plotted as a function of (a) L_{GD}, at room temperature and (b) substrate temperature at L_{GD} = 15 µm.

4.5 Drain Leakage as a Function of L_{GD}, *T*, T_{OX}

Drain leakage was measured at off-state with V_{GS} 3V below pinch-off condition, while the drain voltage was swept from 0 to 100 V. Leakage stayed low and doesn't vary with L_{GD}; however, increases with increasing temperature, as clearly shown in Figure 4.8. In our temperature study, leakage spread ranged over 3 orders of magnitude for the HFET and the MOSHFETs. This high leakage current is attributed to the surface leakage caused by surface state hopping, AlGaN defects, and gate leakage through the Schottky metal by thermionic emission, which are strong function of the temperature [79].



(a)



(b)

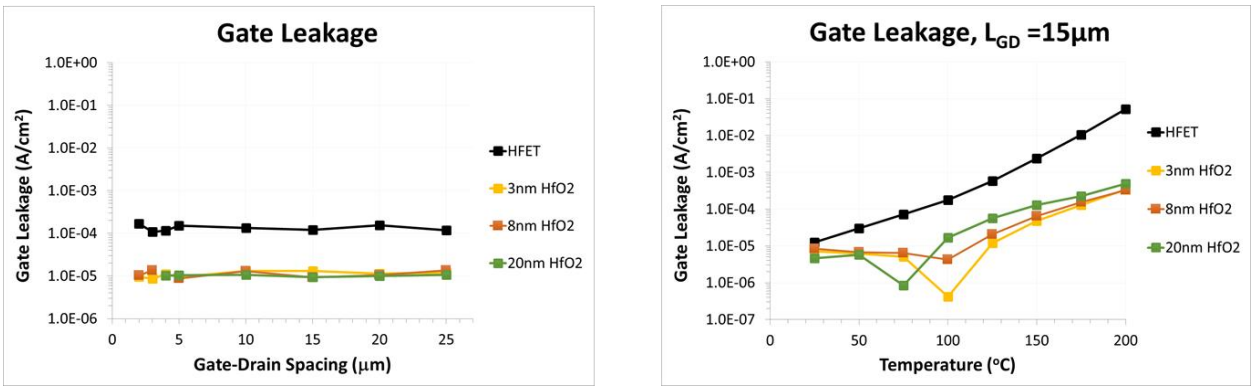
Figure 4.8: Drain leakage of HFET and MOSHFETs plotted as a function of (a) L_{GD}, at room temperature and (b) substrate temperature at L_{GD} = 15 µm.

4.6 Gate Leakage as a Function of L_{GD}, *T*, T_{OX}

Gate leakage was measured at V_{DS} = 0V and V_{GS} 5V below pinch-off condition. Leakage, I_{GS}, does not vary with L_{GD}; however, increases with increasing temperature, as shown in Figure 4.9. This is due to increase in thermionic emission current. Typically, the current in a diode is modeled by thermionic emission model [5]:

$$J = AT^2 e^{-(q\Phi_{BN}/kT)}[e^{(qV/kT)} - 1] \tag{4.4}$$

where *A* is the effective Richardson's constant, *T* is the absolute temperature, Φ_{BN} represents the effective Schottky barrier height, *k* is the Boltzmann's constant, and *V* is the applied bias. While the gate leakage current for both HFET and MOSHFETs exhibited a rapid increase with *T*, MOSHFET gate leakages remain below HFET levels. This is especially true for low to moderate electric field stress on the gate.



(a) (b)

Figure 4.9: Gate leakage of HFET and MOSHFETs plotted as a function of (a) L_{GD}, at room temperature and (b) substrate temperature at L_{GD} = 15 µm.

4.6.1 Dielectric breakdown

As the electric field across MOSHFET dielectric was increased to 3-5 MV/cm the devices with thinner dielectrics such as, 3nm and 8nm HfO_2 exhibited bi-modality. A dielectric breakdown was caused by tunneling effect and a step shift in I_{GS} measurement followed, with 6 orders of magnitude or higher gate leakage. This is illustrated in Figure 4.10. The results help postulate, while increasing gate-to-channel capacitance may be desirable to control channel, a value lower than certain physical thickness may compromise reliability of the dielectric and the transistor. The damage is permanent.

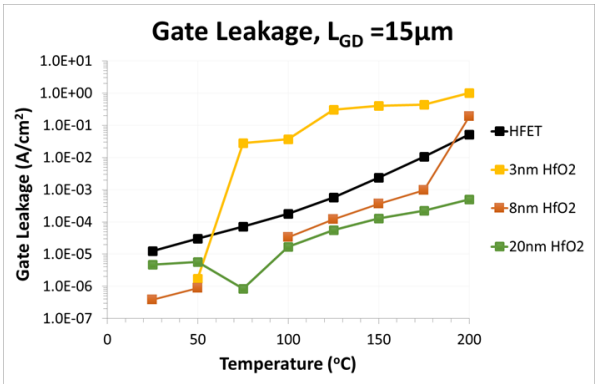


Figure 4.10: MOSHFETs with thin insulators showing breakdown with temperature stress when exposed to high electric field.

4.7 Summary

A comprehensive temperature study was conducted on AlGaN/GaN HFET and MOSHFETs with ALD HfO_2 as gate dielectric and access area passivation. Temperature was raised up to 200 °C. Static output and transfer characteristics were measured and the saturation drain current, peak transconductance, drain leakage, and gate leakage as a function of temperature were evaluated. The findings include reduction of the drain current I_{DS}, reduction of the transconductance g_m, and increase of the on-resistance R_{on} at elevated temperatures in both HFETs and MOSHFETs. At 200 °C, the HFET and MOSHFETs exhibited ~45% of their saturation drain current and peak transconductance evaluated at room temperature. This is attributed to degradation of the mobility of channel electrons due to phonon scattering. Characteristics of the MOSHFETs outperformed that of the HFET. The gate leakage current exhibited an increase with temperature but remained below the levels seen in the reference HFET. Finally, while gate leakage was suppressed with passivation, we also optimized ALD HfO_2 thickness and realized that it should be larger than 10 nm in order to avoid tunneling breakdown through the dielectric. From our experiments, the onset of this breakdown electric field was around 3-5 MV/cm with thinner dielectrics. A thicker dielectric than 10 nm, preferably in 15-20 nm range, was found effective in withstanding such electric field stress or higher. Therefore, a MOSHFET device with a 20nm ALD HfO_2 high-k dielectric was found to have a great potential for high temperature power device applications.

CHAPTER 5: Annealing Ambient Effect on GaN MOSHFETs with ALD HfO_2 Dielectric

5.1 Introduction

HfO_2 is one of the most promising dielectric candidates for AlGaN/GaN [16], [17], [23], [24], [37]–[39], [42]–[46], [71]–[75]. Chapter 2 and 3 elaborates on HfO_2 with sufficient thickness being a suitable dielectric for MOSHFET gate and access regions. In this chapter we aim to optimize the dielectric further by means of post deposition annealing (PDA). It has been reported that gate oxides annealed in forming gas ambient (FGA) can improve the electrical properties of MOSFETs [54]–[60] possibly due to passivating the interface defects; however, to the best of our knowledge, no such study has been conducted on AlGaN/GaN MOSHFET to date. Therefore, it is of great interest to perform a systematic investigation on the influence of various PDA ambient.

H_2 present in FG ambient was found effective to greatly reduce the frequency dispersion by passivating defects in the Al_2O_3 layer (border traps) in III-V MOS devices (InGaAs) [54]. FG annealed sample showed better Y_2O_3-Si interfacial quality by having a lower D_{it} than N_2 annealed samples due to passivation effect by H_2 in FG [55]. Choi *et al.* [56] reported lower interface state density and better MOSFET characteristics such as higher drive current, higher transconductance, lower subthreshold swing, and higher carrier mobility when HfO_2 annealed in FG at 600 °C. FGA was also reported effective in passivating defect states near the HfO_2-semiconductor interface [57]. A significant improvement of charge trapping was found in poly-Si/high-k HfO_2 when post PDA was investigated in FG and claimed likely due to interface state passivation [58]. A drastic reduction in leakage current has been reported on FG annealed HfO_2-on-Si due to densification of

the oxide and improved interface quality by passivating defects and dangling bonds [59, 60]. Ganapathi *et al.* [59] also reported reduced fixed charges and less frequency dispersion in the HfO_2/Si after annealing in FGA.

In this study, we deposited high-*k* HfO_2 as gate dielectric and surface area passivation using ALD technique and investigated two types of PDA ambient, nitrogen (N_2) and forming gas (95% N_2-5% H_2), and their effect on the electrical characteristics of the transistors. The DC performance, current dispersion characteristics, and reliability (*e.g.*, high temperature operation, V_{TH} variability) of the MOSHFETs were evaluated.

5.2 Experimental Procedure

MOSHFET devices were fabricated on AlGaN/GaN on Si substrate samples according to the process flow outlined in chapter 2, section 2.3.4. The ohmic contact resistance from transmission line model (TLM) measurements were deduced in the 10^{-5} $\Omega \cdot cm^2$ range and sheet resistance around 500 Ω/sq. This ensured good ohmic characteristics for the devices. A 20 nm thick HfO_2 gate dielectric was deposited by using a Cambridge Nanotech thermal ALD system. The precursors used were tetrakis(dimethylamino)hafnium (TDMAH), precursor with O_3 oxidant, at a temperature of 200 °C. HfO_2 was used as the gate dielectric as well as the passivation layer. Post deposition anneal (PDA) was performed by 60 sec RTA at 600 °C in either N_2 ambient or FG (5% H_2 in N_2). Physical thickness of the dielectrics after ALD process was measured using variable angle spectroscopic ellipsometer (VASE) on monitor Si wafers. Film thickness of HfO_2 with N_2 annealing ambient measured at 20.47 nm and that with FGA measured at 19.64 nm. The fabricated devices had transistors with gate length (L_G) of 3 μm, gate width (W_G) of 50 μm, gate-to-source separation (L_{GS}) of 2 μm. A matrix of seven MOSHFET devices are fabricated where gate to drain

separation (L_{GD}) varies from 2 μm to 25 μm. Grazing angle X-ray Diffraction (GA-XRD) was performed using Rigaku SmartLab X-ray diffractometer with parallel beam optics. Current–voltage (I–V) characteristics were measured at various temperatures (25–200 °C) using Keithley 4200−SCS. Capacitance-voltage (CV) measurements were performed by a precision inductive-capacitance-resistance (LCR) meter, HP 4284A, with an applied AC voltage of 50 mV. Current collapse was measured via pulsed I_{DS}−V_{DS} using HP 8112A, HP 8116A pulse generators, and a Tektronix TDS−420 oscilloscope.

5.3 Physical Characterization of ALD HfO_2 Film

The crystalline structure of the ALD dielectrics were analyzed by grazing angle X-ray diffraction (XRD) measurements. Figure 5.1 shows relative intensity comparison vs. angle 2-Theta of the XRD spectra for ALD HfO_2 annealed in N_2 and FG ambient, and reference from JCPDS card no. 04-005-6162. Both films showed representative monoclinic HfO_2 characteristics. Both process conditions showed peak intensities at 18°, 32° and 36° corresponding to (100), (111), and (200) phase. However, it was noticed that HfO_2 peaks were suppressed for samples annealed in N_2 and FG, at 25°, 28°, 39°, and 41° corresponding to 011, $\bar{1}11$, 021, and $\bar{2}11$. This could be attributed to the fine grain size, preferred orientation or less crystalline nature originated from the strong oxidation during the ALD reaction due to O_3 oxidant, as seen in chapter 3, section 3.3.

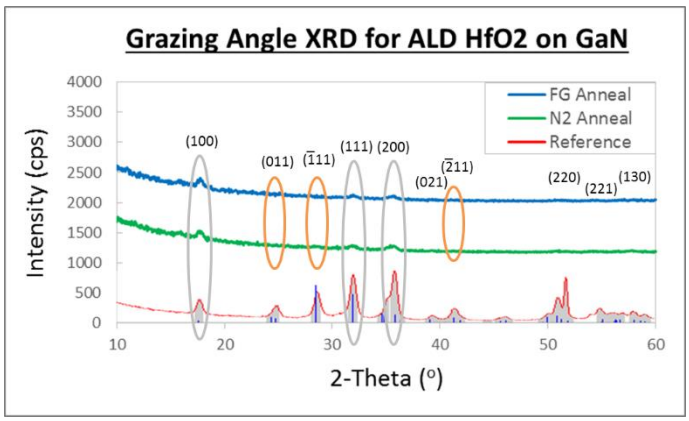


Figure 5.1: Comparison of the XRD spectra for ALD HfO_2 annealed in N_2, FG, and JCPDS reference.

5.4 Electrical Characterization of MOSHFETs

5.4.1 Capacitance-voltage (CV) characteristics

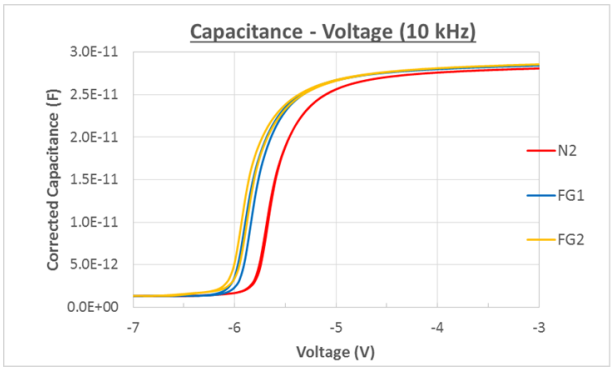
The CV characteristics were measured at 10 kHz, 100 kHz, and 1 MHz on MOS capacitors with 100 µm x 100 µm square area, for HfO_2 oxide annealed at 600 °C in N_2 and FG ambient. Figure 5.2 shows typical CV curves of the investigated samples, in which gate bias was swept bi-directionally from -7 to -3V. The frequency dispersion characteristics show hysteresis of the N_2 annealed part being lower than FGA parts at low-frequency (10 kHz). Then again, one of the FGA parts exhibited lower hysteresis than N_2 annealed part at higher frequencies (100 kHz and 1 MHz). The mixed results invalidate FG annealing related improvement. The hysteresis of a MOS capacitor is attributed to the trapping and detrapping of charges related to film defects that slowly respond to a voltage sweep. In this case, using O_3 ALD oxidant improves the interface quality such that that the effect of using different annealing ambient is indistinguishable.

Capacitance equivalent thickness (CET) of the HfO_2 layer annealed in different ambient was extracted from the accumulation level of capacitance. To correctly determine oxide capacitance,

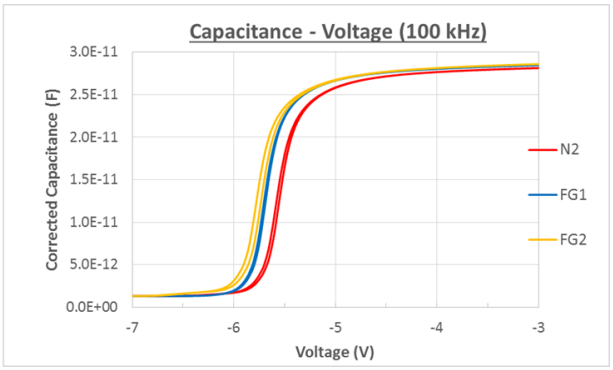
AlGaN contribution had to be first measured on an unpassivated HEMT and then taken away from the series capacitance. The following equation was used to extract CET of the investigated samples [54]:

$$C_{OX} = \frac{k\varepsilon_o A_G}{CET} \tag{5.1}$$

where C_{OX} is the maximum accumulation capacitance, ε_o is the permittivity of free space, k is the dielectric constant of HfO_2, and A_G is the area of capacitor. The calculated CET for N_2 and FG annealed samples were 19.23 and 19.03 nm, respectively.



(a)



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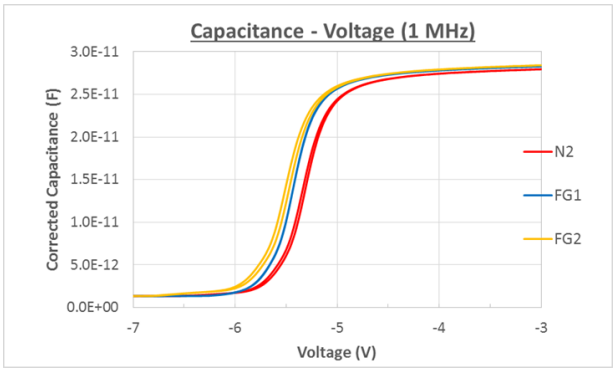
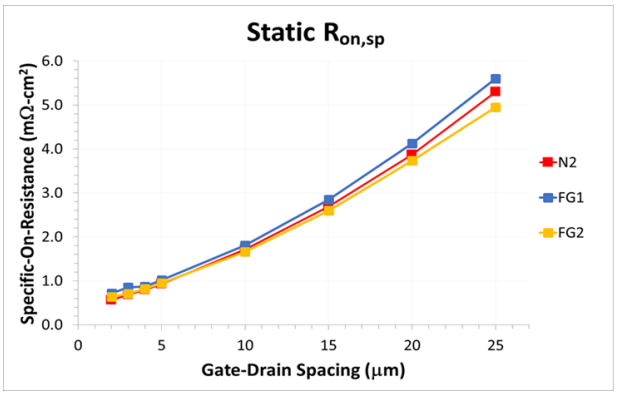


(c)

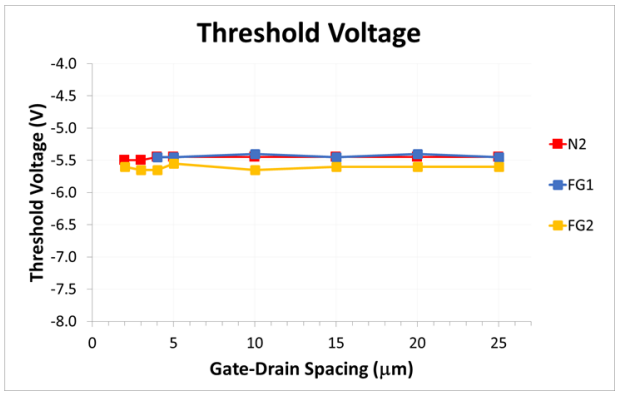
Figure 5.2: Capacitance-voltage curves of MOS capacitors for HfO_2 dielectric annealed in different ambient, measured at room temperature (a) 10 kHz, (b) 100 kHz, and (c) 1 MHz.

5.4.2 DC current-voltage (IV) characteristics

Devices with L_G x W_G = 3 x 50 μm, L_{GS} = 2 μm, and L_{GD} = 20 μm were characterized for their performance. Figure 5.3(a) thru (f) show extracted specific on-resistance, threshold voltage, peak transconductance, hysteresis, drain leakage, and gate leakage for different annealing ambients as a function of L_{GD}. The values of specific on-resistance, $R_{on,sp}$, were extracted from the linear region of the I_{DS}–V_{DS} curves at V_{GS} 4V over pinch-off bias. $R_{on,sp}$ show parabolic dependence on L_{GD}. Threshold voltage, V_{TH}, was measured at 1mA/mm with V_{DS} = 0.1V. V_{TH} remains relatively unchanged as L_{GD} increases as it is strictly governed by the characteristics in the drift region directly below gate. Peak transconductance (g_m) is measured in the saturation mode with V_{DS} = 5V, and remains relatively unchanged as L_{GD} increases. Hysteresis degrades slightly as a function of L_{GD}. Drain leakage was measured at off-state with V_{GS} 3V below pinch-off condition, while the drain voltage was swept from 0 to 100 V. Gate leakage was measured at V_{DS} = 0V and V_{GS} 5V below pinch-off condition. Both, drain and gate leakage values are low and don't vary with L_{GD}.



(a)



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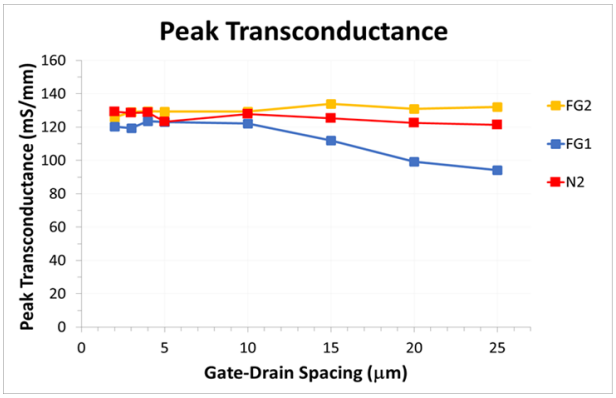

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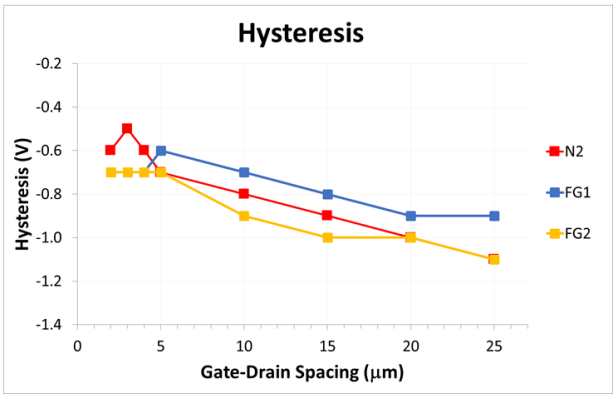

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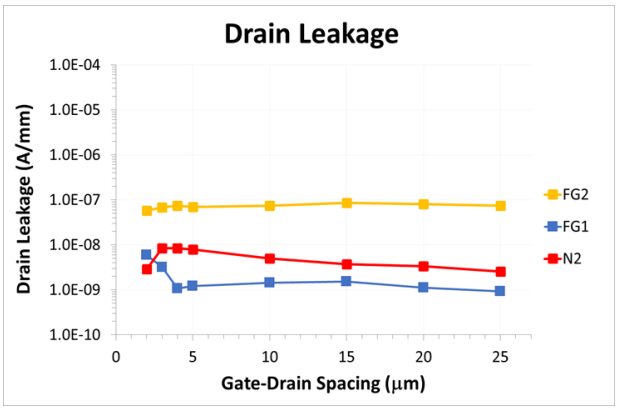

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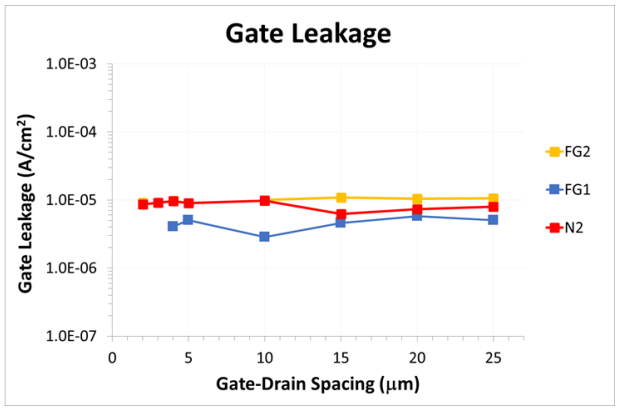


(f)

Figure 5.3: DC current-voltage characteristics of HfO_2 MOSHFETs annealed in different ambient, measured at room temperature, plotted as a function of L_{GD} (a) extracted static $R_{on,sp}$, (b) V_{TH}, (c) peak g_m, (d) hysteresis, (e) drain leakage, and (f) gate leakage.

5.4.3 Temperature dependence

We also conducted a temperature study where transistor DC characteristics were evaluated while temperature was increased from room temperature (25 °C) up to 200 °C. Figure 5.4 shows $R_{on,sp}$, threshold voltage, peak transconductance, hysteresis, drain leakage, and gate leakage variation as a function of temperature. Drain current, I_{DS}, decreases with increasing temperature due to series resistance increasing in the drift region, and reflects via increase in $R_{on,sp}$. At 200 °C, both HfO_2 MOSHFETs annealed in N_2 and FG, exhibited 2.5x of their respective specific on-resistance evaluated at room temperature. The carrier mobility reduction is attributed to phonon scattering [77], [79]. In our temperature study, MOSHFET V_{TH} variation between different annealing ambient were analogous and was insignificant with temperature increase. Peak g_m decreases with elevated temperature as mobility of the channel electron is reduced due to phonon scattering [80], [82]–[84]. At 200 °C the MOSHFETs with both N_2 anneal and FGA exhibited 46% of their peak transconductance evaluated at room temperature. The linear sensitivity as a function of temperature is in line with degradation trend evidenced in chapter 4, section 4.3.3. An assessment of on-state gate stack reliability was performed by looking for signs of hysteresis in DC transfer characteristics, and the resulting threshold voltage instability. In our study, there was no concrete temperature variance on hysteresis for any of the ALD HfO_2 anneal splits. Drain leakage increases with increasing temperature. In our temperature study, leakage spread ranged over 3 orders of magnitude for the MOSHFETs with different annealing ambient. This high leakage current is attributed to the surface leakage caused by surface state hopping, AlGaN defects, and gate leakage through the Schottky metal by the thermionic emission, which are strong function of the temperature [79]. Gate leakage also increases with increasing temperature. The temperature

dependence is attributed to classical fundamental physics and explained by excited electrons in the conduction band at elevated temperatures.

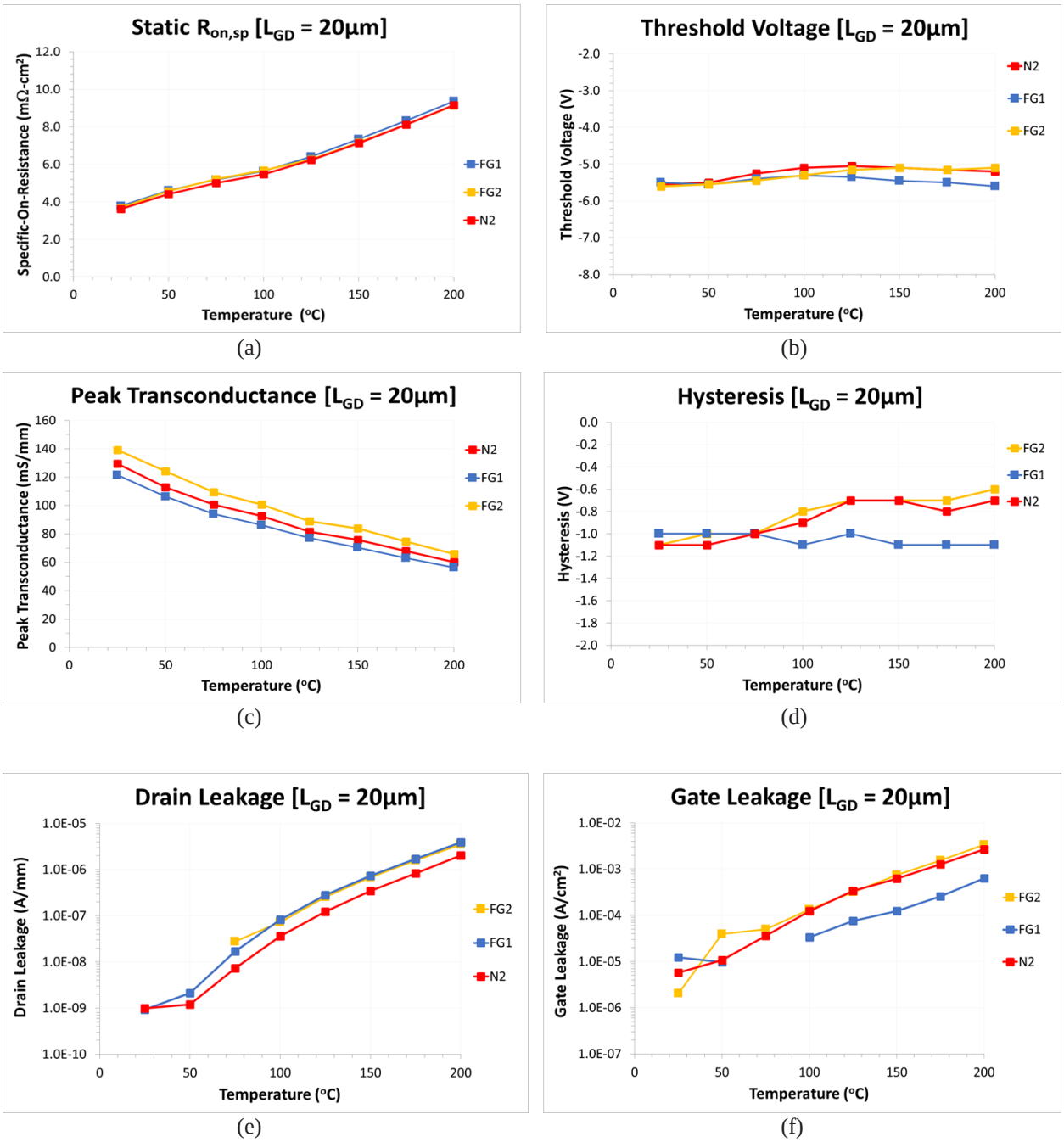
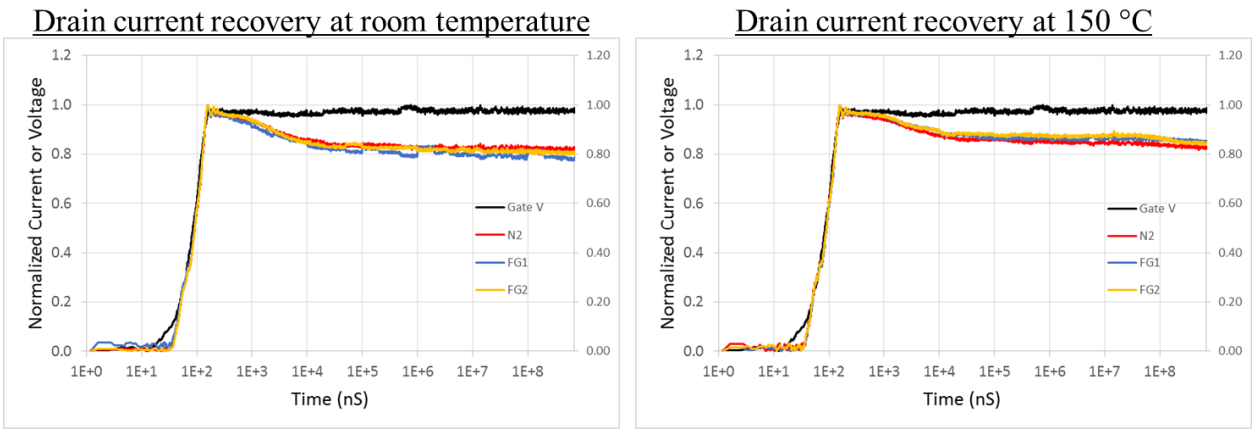


Figure 5.4: DC current-voltage characteristics of HfO_2 MOSHFETs annealed in different ambient, measured at a constant L_{GD} = 20 µm, plotted as a function of temperature (a) extracted static $R_{on,sp}$, (b) V_{TH}, (c) peak g_m, (d) hysteresis, (e) drain leakage, and (f) gate leakage.

5.4.4 Current collapse – gate lag measurement

Current collapse was measured using a custom configuration described in chapter 3, section 3.4.5. Gate lag measurement is sensitive to surface states and thus helps evaluate the passivation region of the GaN device. Figure 5.5(a) shows current collapse of the test samples at room temperature. A MOSHFET structure is effective at passivating the surface traps and thereby reducing hot-electron degradation. Devices with N_2 anneal and FGA effectively had no current collapse. The improvement is attributed to O_3 oxidant during ALD HfO_2 deposition that produces less interface trap density [32], [34]. Figure 5.5(b) shows DC/RF dispersion tests performed at an elevated temperature (150 °C) where MOSHFETs with O_3 oxidants, irrespective of PDA annealing ambient, displaying excellent current collapse recovery.



(a) (b)

Figure 5.5: DC/RF dispersion: gate lag of HfO_2 MOSHFETs annealed in different ambient, measured at (a) room temperature, and (b) elevated temperature, 150 °C.

5.4.5 High temperature reverse bias (HTRB) stress test

We carried out HTRB stress experiments on the GaN MOSHFETs with different annealing ambient with DC reverse-bias drain acceleration. The devices were electrically stressed in the off-state (gate-to-source bias, V_{GS}, 3V below V_{TH}) with drain-to-source bias V_{DS} = 150V at environmental temperature of 150 °C. In our study, the stress time was increased up to 1000 sec. This is one of the key tests to evaluate long-term reliability of power devices. Figure 5.6 shows V_{TH} stability comparison between the two annealing ambient types. In both cases, due to O_3 ALD oxidant, the reduced interface states led to more stable V_{TH} even at longer stress duration. A minimal V_{TH} drift (< 0.25V) was achieved under stress for MOSHFETs with N_2 anneal and FGA.

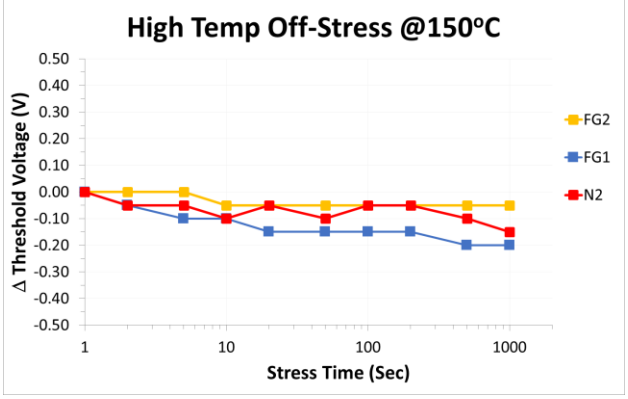


Figure 5.6: Comparison of the MOSHFET ΔV_{TH} as a function of HTRB stress time between the two annealing ambient.

5.5 Electrical Characterization of MOSHFETs with H_2O Oxidant

In this study we looked at water oxidant-based MOSHFETs which at first went through N_2 PDA for 60 sec at 600 °C. One of the devices used a single-pulse water oxidant (SPH) during the 20nm ALD HfO_2 deposition while the other device used double-pulse water oxidant (DPH). Following fabrication up to gate metal stack, the parts underwent an additional FGA cycle for 60 sec at 600

°C. A cursory electrical characterization was performed on devices before and after FG anneal. Figure 5.7 shows CV characteristics measured at 10 kHz, 100 kHz, and 1 MHz on MOS capacitors with 100 µm x 100 µm square area. Two primary observations looking at the FG annealed parts are i) the threshold voltage (V_{TH}) shifts towards positive direction, and ii) a 0.1 V hysteresis is half compared to parts that only had N_2 anneal. The lower hysteresis is an indication of cleaner interface.

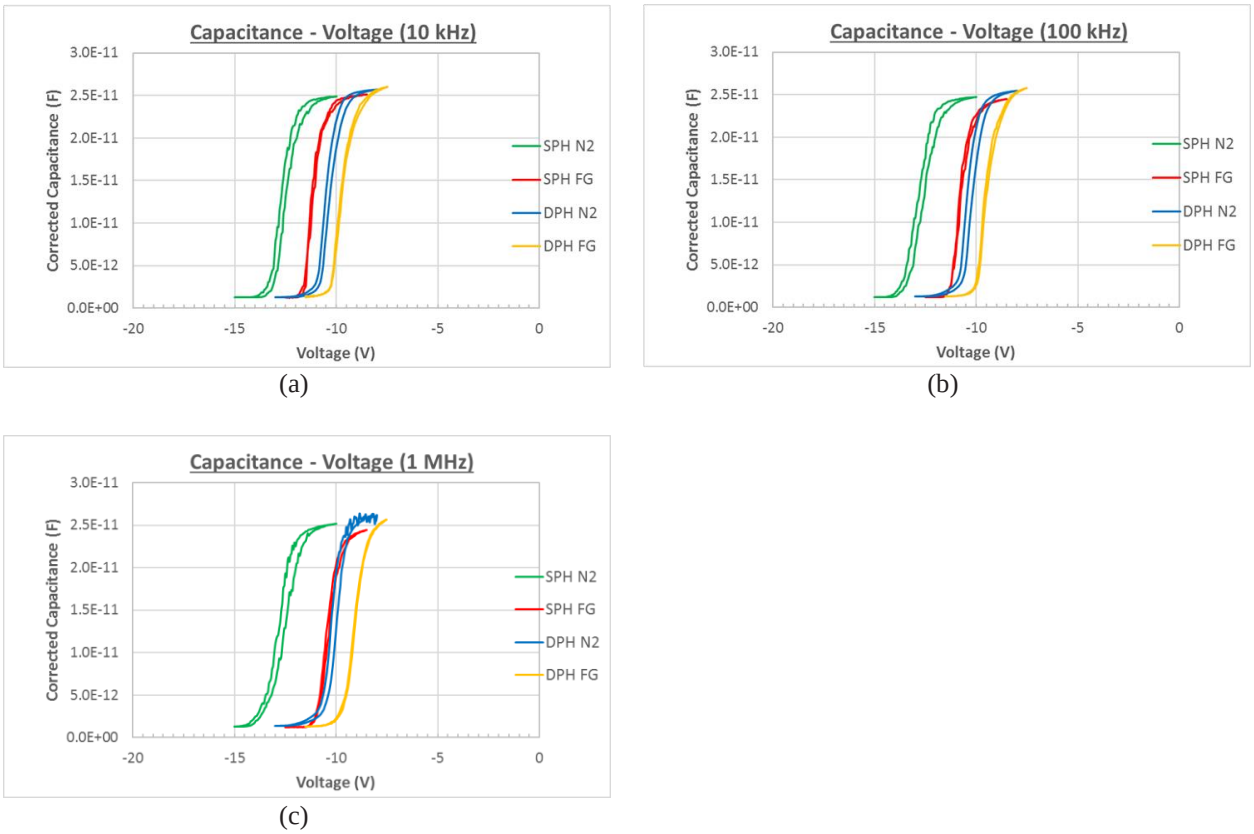


Figure 5.7: Capacitance-voltage curves for H_2O oxidant-based HfO_2 dielectric, annealed in different ambient, measured at room temperature (a) 10 kHz, (b) 100 kHz, and (c) 1 MHz.

We also carried out HTRB stress experiments on the MOSHFETs. Figure 5.8 shows V_{TH} stability comparison between the two annealing ambient. Both SPH and DPH, annealed in N_2, exhibited a

ΔV_{TH} up to 2.8 V whereas, the same devices, when underwent an additional FGA cycle, showed significant improvement in V_{TH} variation. DPH MOSHFET with FGA showed an astonishing 0.9 V ΔV_{TH}, an improvement of more than 1.8 V from the original device with N_2 anneal. A high interface trap density is the leading cause of threshold voltage instability [75]. Hence, we postulate that the FGA parts have reduced interface states.

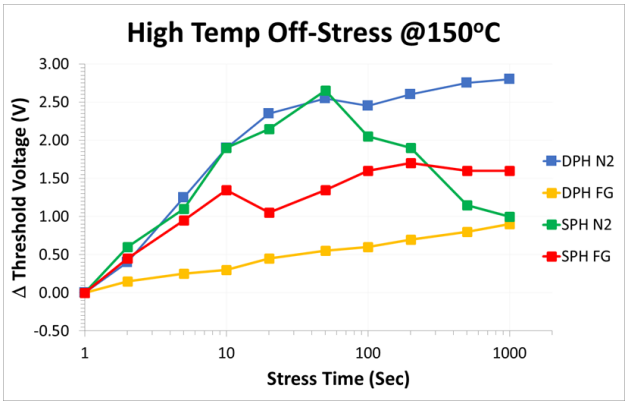


Figure 5.8: Comparison of ΔV_{TH} as a function of HTRB stress time between the two annealing ambient for H_2O oxidant-based MOSHFETs.

5.6 Summary

The objective of this chapter was to further optimize HfO_2 dielectric and achieve reduced interface trap density by means of annealing ambient. In that process, a systematic study on the effects of PDA ambient (N_2 and FG) on ALD HfO_2 deposited on AlGaN/GaN heterostructure have been presented. The physical properties of the films and electrical characteristics of the devices have been analyzed. Alongside DC CV and I-V tests, current collapse and reliability measurements were conducted with acceleration bias test at elevated temperature. O_3 oxidant-based MOSHFETs subdued the annealing ambient effect since the role of O_3 ALD oxidant alone was dominant. This is understandable having seen the significant improvement, detailed in chapter 3. Samples

annealed in N_2 and FG yielded comparable results for every category tested. While this is atypical of the published reports on other substrates, we postulate, the effect of using O_3 as ALD oxidant provides far superior bulk oxide and interface quality and therefore, trumps high temperature anneal ambient related improvements. On the contrary, although limited, experiments conducted on H_2O ALD oxidant-based devices exhibit strong indication of interface state improvement. We suggest that a deeper investigation is carried out on MOSHFETs with ALD H_2O oxidant.

CHAPTER 6: Conclusions and Future Work

6.1 Conclusions

This dissertation has focused on the performance improvement and reliability enhancement of the AlGaN/GaN MOSHFETs. GaN will be a replacement technology for Si in the power electronics sector. The rate of progress in the power density and total power available from AlGaN/GaN HEMTs has been remarkable. For the same output power, a 10-fold reduction in device size can be realized using GaN-based devices in place of conventional devices. These technological advantages result from the combination of the wide bandgap of GaN and the availability of the AlGaN/GaN heterostructure where high voltage, high current and low on-resistance can be simultaneously achieved, resulting in high power – high efficiency operation. Furthermore, the wide bandgap offers a rugged and reliable technology capable of high voltage – high temperature operation. This opens up several industrial, automotive and aircraft applications like power and high voltage rectifiers and converters. Ultimately, the compact size of GaN-based transistors will lead to lower cost products. This will increase system efficiency, reduce system costs, and expand the market applications.

In this research, we attempted two technological solutions to overcome some of the main challenges of these devices. First, by using ozone as ALD oxidant the threshold voltage drift can be significantly minimized. Also, higher output current, reduced, gate leakage, suppressed current collapse, and overall better temperature variability can be simultaneously achieved. This enables a unified dielectric solution for AlGaN/GaN MOSHFET gate and access regions which in turn, greatly simplifies the fabrication process. And second, PDA annealing after ALD high-k dielectric

deposition in N2 gas ambient, in comparison with forming gas environment. The effect of using ozone ALD during ALD HfO_2 deposition was so significant in reducing overall defects that it trumped any and all potential interface defects reduction due to PDA.

In order to harness the full potential of GaN based FETs for power switching circuits it is paramount that the fabrication process be optimized and refined to provide highly reproducible devices with a high yield. Advanced processing techniques are also critical to viably producing complex MOSHFET structures. Employing such optimization techniques and other technologies currently under development, GaN power electronics will surely become one of the leading markets for GaN devices. The conclusions of each effort are highlighted herewith.

Optimization of ALD oxidation process:

HfO_2 was selected as the choice of dielectric for AlGaN/GaN MOSHFET, gate and surface area passivation, due to high permittivity and sufficient conduction band offset to GaN. There are several reports on transistors with HfO_2 exhibiting high drain current, low on-resistance, low leakage currents, and great immunity to current collapse. Atomic layer deposition (ALD) was chosen as the preferred method of dielectric deposition since it is a well-established process that affords the growth of high quality uniform films with precise monolayer thickness.

Two types of oxidants were investigated, namely, water (H_2O) and ozone (O_3). It was found that MOSHFETs with O_3 oxidant yielded lower threshold voltage (V_{TH}) shifts, higher maximum drain current ($I_{DS,max}$) of 340 mA/mm, 20% lower on-resistance (R_{on}), higher peak transconductance at 112.66 mS/mm, lower hysteresis, and lower gate leakage ($5.4x10^{-6}$ A/cm^2) compared to water oxidant based MOSHFETs with $I_{DS,max}$ of 240 mA/mm, 81.38 mS/mm peak transconductance, and

$1.7x10^{-4}$ A/cm^2 gate leakage. DC/RF dispersion tests showed MOSHFETs with O_3 oxidant had ~200x better current collapse recovery. Temperature characterization and reliability test results, such as high temperature reverse bias (HTRB), are published for the first time on ALD-HfO_2/AlGaN/GaN MOSHFETs using TDMAH and O_3 precursor. Using an ozone oxidant provided more stability (*i.e.*, less variability in R_{on} and V_{TH}) as a function of temperature. Finally, when devices were electrically stressed in the off-state, HTRB test showed minimal V_{TH} drift (< 0.5V) in the case of O_3 oxidant vs. much larger V_{TH} drift (2.5V) in the case of H_2O oxidant.

Requirements for reliable gate and access-region operation

For AlGaN/GaN MOSHFETs, selecting dielectric materials can be challenging and often involves a compromise of the required properties such as, permittivity, conduction/valence band offsets, breakdown strength, thermal stability, and interface trap density. Therefore, it has been a standard practice to choose separate dielectrics for the gate and access regions.

In the gate region, the objective is to reduce gate leakage, maintain good gate control (ON-state reliability), minimize interface traps, and have minimal effect on threshold voltage when device undergoes stress. In the passivation region, the primary objective is to minimize current collapse. Aside from minimizing interface states, surface passivation also provides contact isolation.

The use of high-k dielectrics means high input gate capacitance which increases gate control over the channel, and results in a more efficient conductivity modulation and higher transconductance. Use of high-k dielectrics also enables a significant reduction in gate leakage by allowing a physically thicker dielectric that increases the tunneling distance, for the same gate capacitance.

Therefore, one can combat the low conduction band offset to GaN, associated with high-k dielectrics, which would increases leakage.

The challenge with high-k dielectrics have been with harboring high density of interface states. Therefore, it warrants process optimization in trying to minimize defects. In our experiments we investigated ALD chemistry of HfO_2 in terms of oxidants. The results were astounding. DC and pulsed-IV characteristics were significantly improved. Plus, HTRB, one of the key reliability parameters showed the largest improvement of all. With such performance and reliability enhancement, we concluded that high-k HfO_2 met gate and access region requirements for the GaN MOSHFET technology while simplifying fabrication process.

Temperature characterization and optimization of dielectric thickness:

The use of high-k dielectrics enables a significant reduction in gate leakage by allowing a physically thicker dielectric that increases the tunneling distance, for the same gate capacitance. At the same time, for a given high-k dielectric, the thinner the oxide the higher the input gate capacitance which in turn increases the conductivity modulation. In our temperature study of AlGaN/GaN MOSHFETs with ALD HfO_2, the saturation drain current and peak transconductance decreased by ~45% as temperature increased from room temperature (25 °C) to 200 °C. The mobility degradation is due to phonon scattering. V_{TH} and hysteresis remained relatively unchanged with respect to temperature. The drain and gate leakage increased by 3 orders of magnitude as temperature increased from room temperature (25 °C) to 200 °C. This is attributed to the surface leakage caused by surface state hopping, AlGaN defects, and gate leakage through the Schottky metal by thermionic emission, which are strong function of the temperature. Additionally, we concluded that there is an optimum thickness for HfO_2 gate dielectric below

which, tunneling breakdown can occur when exposed to high electric field and elevated temperature. From our experiments, the onset of this breakdown electric field was around 3-5 MV/cm. A thicker dielectric than 10 nm, preferably in 15-20 nm range, was found effective in withstanding such electric field stress or higher. Finally we observed that an unpassivated HFET can degrade further due to open passivation area affected by moisture and thermally grown oxide.

Role of dielectric post-deposition annealing ambient

Once we settled on ALD HfO_2 as choice of dielectric for gate and access regions of the MOSHFET, and determined optimal dielectric thickness, our goal was to further optimize the density of interface states. One approach to achieve cleaner interface is to investigate post-deposition annealing ambient. Several authors have reported improvements due to high temperature annealing using forming gas vs. N_2. We have performed physical and electrical characterization using these annealing ambient on our GaN transistors, including but not limited to, XRD crystallinity, capacitance-voltage tests, DC current-voltage tests, current collapse – gate lag measurements, reliability measurements such as, temperature sensitivity, HTRB. Our evaluations showed that the effect of O_3 oxidant in the ALD chemistry far exceeded any potential interface engineering that could be possible due to FG annealing ambient. On the contrary, the effect of annealing ambient was much more pronounced on MOSHFETs with H_2O ALD oxidant. It was evident from our limited data that FGA had potential to better passivate the devices by harboring less density interface states.

6.2 Future Work

This work encompasses AlGaN/GaN device technology. While we have had significant achievements with enhancing performance and reliability of the gate and access-region dielectric, our findings are a small fraction of the broader scope within power semiconductor materials and device development. For instance, InAlN has emerged as a promising alternative to AlGaN as a barrier layer, and is capable of delivering higher output current density and lower on-resistance owing to its strong spontaneous polarization [97], [99]. In addition, the InAlN alloy can be lattice-matched to GaN, which results in a strain-free barrier layer, and potentially offers advantages over AlGaN/GaN in terms of its reliability [97]. Ga_2O_3 has also emerged as a strong contender for future power electronics due to its excellent material properties and suitability for mass production. It has wider bandgap, higher breakdown voltage, higher power capacity, and lower loss (*i.e.*, higher efficiency) than those of traditional wide bandgap semiconductors such as silicon carbide (SiC) and gallium nitride (GaN) [131]–[133]. Another important advantage of Ga_2O_3 is that large-size single-crystal bulks can be synthesized by conventional melt-growth methods similar to those used to manufacture sapphire substrates [132]. Therefore, Ga_2O_3 power devices have the potential to surpass SiC and GaN not only in device performance but also from cost perspective.

As for high-*k* dielectrics, Al_2O_3 and HfAlO have made their marks as suitable layers offering higher performance. We believe, the methodologies and know-how, developed in this work, are applicable to the wide bandgap family employing different barrier materials and oxides.

In an attempt to further optimize dielectric properties, we investigated effect of high temperature annealing ambient on ALD HfO_2 MOSHFETs using O_3 oxidant. In our experiments, the effect of ozone dominated the characteristics, and masked utilization of annealing ambient. However, our

preliminary DC characterization on MOSHFETs using H_2O oxidant showed encouraging results indicating FG anneal reduced density of interface states. The findings warrant further investigation. Therefore, we suggest design of experiment on water oxidant-based MOSHFETs along with integrating a broader selection of ambient such as, N_2, FG, N_2O, O_2, *etc*. It has been reported that N_2O annealing significantly reduces electron trapping in the resulting oxides, and therefore enhances electrical stability of the MOSFETs [61]. Thermal nitridation of conventional oxides in a nitrogen rich ambient, most notably NH_3 and N_2O, has been shown to improve many properties of the oxide films including traps and MOSFET threshold voltage shift [62]. O_2 annealed oxides, on the other hand, have been found to demonstrate the highest electrical dielectric breakdown voltage as well as the lowest effective oxide charge, interface trap density, and total interface-trap density [55].

The device analyses performed in this work is fairly inclusive of the characterization suite. However, we recommend additional evaluations in order for a more comprehensive analysis on GaN devices. An accurate characterization of the density of interface states (D_{it}) is warranted on MOSHFETs using O_3 oxidant-based ALD HfO_2. The defects have a significant impact on device operation including shifting threshold voltage, degrading channel mobility, increasing dynamic on-resistance, and providing source of instability. D_{it} can be evaluated by using measurement methods such as, Deep Level Optical Spectroscopy (DLOS), pulsed-IV measurements in conjunction with conductance method (GV) [103], capacitance Deep Level Transient Spectroscopy (C-DLTS), current mode DLTS (I-DLTS), or transconductance dispersion measurements ($g_m(f)$) [49], and approximated using first principles calculations based on density functional theory (DFT) [2]. This would allow construction of detailed bonding models for oxide/III–V interfaces and the computation of the density of states across the band structure. We

also recommend performing fundamental breakdown voltage tests, time dependent dielectric breakdown (TDDB) measurements, and estimating lifetime on GaN devices with ozone oxidant-based ALD HfO_2.

Finally, there is a pressing need for developing normally-off, enhancement-mode, GaN transistors in order to reduce circuit complexity and provide fail-safe operation. There exist several proposed mechanisms including recessed-gate, p-GaN gate, plasma treatment, inversion-type MISHFET, flash MOSHFET, each with a unique set of trade-offs. These methods need to be rigorously investigated to engineer normally-off devices that are reliable, repeatable, and can be manufactured.

REFERENCES

[1] B. Bothwell *et al.*, "Vertical GAN - The pathway to power switching efficiency," Oct. 2015. Available: https://www.qorvo.com/resources/d/qorvo-collaboration-gan-power-switching-compound-semiconductor-20151001

[2] N. Bowers, "Yole explores the power electronics industry," Feb. 2015. Available: https://www.electronicspecifier.com/around-the-industry/yole-explores-the-power-electronics-industry

[3] P. Gammon, "Silicon and the Wide Bandgap Semiconductors, shaping the Future Power Electronic Device Market," in *Proc. 14th Int. Conf. Ultimate Integr. Silicon*, pp. 9–13, Mar. 2013.

[4] M. A. Briere, "GaN based Power Devices," *RPI CFES Conf.*, Jan. 2013. Available: http://www.rpi.edu/cfes/AnnualConference/B2%20Mike%20Briere.pdf

[5] B. J. Baliga, *Fundamentals of Power Semiconductor Devices*, New York: Springer Science, 2008, ch. 1, p. 15.

[6] F. Medjdoub, *Gallium Nitride (GaN): Physics, Devices, and Technology*, Boca Raton, FL: CRC Press, Taylor & Francis Group, 2015, ch. 1, p. 3.

[7] S. Bush, "GaN-on-Si power transistors from French lab Leti," Jul. 2015. Available: https://www.electronicsweekly.com/uncategorised/gan-on-si-power-transistors-french-lab-leti-2015-07/

[8] M. A. Khan, A. Bhattarai, J. N. Kuznia, and D. T. Olson, "High electron mobility transistor based on a GaN-$Al_xGa_{1-x}N$ heterojunction," *Appl. Phys. Lett.*, vol. 63, no. 9, pp. 1214–1215, Aug. 1993.

[9] Y. Cordier, J.-C. Moreno, N. Baron, E. Frayssinet, S. Chenot, B. Damilano, and F. Semond, "Demonstration of AlGaN/GaN High-Electron-Mobility Transistors Grown by Molecular Beam Epitaxy on Si(110)," *IEEE Electron Device Lett.*, vol. 29, no. 11, pp. 1187–1189, Nov. 2008.

[10] A. Lidow, J. Strydom, M. de Rooij, and D. Reusch, *GaN Transistors for Efficient Power Conversion*, 2nd ed. New York, NY, USA: Wiley, 2014, ch 1.

[11] U. K. Mishra, P. Parikh, and Y. Wu, "AlGaN/GaN HEMTs–an overview of device operation and applications," in *Proc. IEEE,* vol. 90, no. 6, pp. 1022–1031, Jun. 2002, DOI: 10.1109/JPROC.2002.1021567.

[12] N. Ikeda, Y. Niiyama, H. Kambayashi, Y. Sato, T. Nomura, S. Kato, and S. Yoshida, "GaN Power Transistors on Si Substrates for Switching Applications," in *Proc. IEEE,* vol. 98, no. 7, pp. 1151–1161, Jul. 2010, DOI: 10.1109/JPROC.2009.2034397.

[13] U. K. Mishra, L. Shen, T. E. Kazior, and Y. Wu, "GaN-Based RF Power Devices and Amplifiers," in *Proc. IEEE,* vol. 96, no. 2, pp. 287–305, Feb. 2008, DOI: 10.1109/JPROC.2007.911060.

[14] O. Ambacher, J. Smart, J. R. Shealy, N. G. Weimann, K. Chu, M. Murphy, W. J. Schaff, L. F. Eastman, R. Dimitrov, L. Wittmer, M. Stutzmann, W. Rieger, and J. Hilsenbeck, "Two-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in N- and Ga-face AlGaN/GaN heterostructures," *J. Appl. Phys.*, vol. 85, no. 6, pp. 3222–3233, Mar. 1999, DOI: 10.1063/1.369664.

[15] X. Hu, A. Koudymov, G. Simin, J. Yang, M. A. Khan, A. Tarakji, M. S. Shur, and R. Gaska, "Si_3N_4/AlGaN/GaN–metal–insulator–semiconductor heterostructure field–effect transistors," *Appl. Phys. Lett.*, vol. 79, pp. 2832–2834, Oct. 2001, DOI: 10.1063/1.1412591.

[16] F. Azam, B. Lee, and V. Misra, "Optimization of ALD high-k gate dielectric to improve AlGaN/GaN MOS-HFET DC characteristics and reliability," in *Proc. IEEE 5th Wksh., Wide Bandgap Power Devices and Applications (WiPDA)*, pp. 39–43, Oct. 2017, DOI: 10.1109/WiPDA.2017.8170499.

[17] B. Lee, C. Kirkpatrick, Y. Choi, X. Yang, Y. Wang, X. Yang, A. Huang, and V. Misra, "Impact of ALD Gate Dielectrics (SiO_2, HfO_2, and SiO_2/HAH) on Device Electrical Characteristics and Reliability of AlGaN/GaN MOSHFET Devices," *ECS Trans.*, vol. 41, no. 3, pp. 445–450, Oct. 2011, DOI: 10.1149/1.3633060.

[18] Y. Wang, M. Dai, M.-T. Ho, L. S. Wielunski, and Y. J. Chabal, "Infrared characterization of hafnium oxide grown by atomic layer deposition using ozone as the oxygen precursor," *Appl. Phys. Lett.*, vol. 90, no. 2, 022906, Jan. 2007, DOI: 10.1063/1.2430908.

[19] X. Liu, S. Ramanathan, A. Longdergan, A. Srivastava, E. Lee, T. E. Seidel, J. T. Barton, D. Pang, and R. G. Gordon, "ALD of Hafnium Oxide Thin Films from Tetrakis(ethylmethylamino)hafnium and Ozone," *J. Electrochem. Soc.*, vol. 152, no. 3, G213–G219, Jan. 2005, DOI: 10.1149/1.1859631.

[20] H. Tokuda, J. T. Asubar, and M. Kuzuhara, "AlGaN/GaN metal–insulator–semiconductor high-electron mobility transistors with high on/off current ratio of over 5 x 10^{10} achieved by ozone pretreatment and using ozone oxidant for Al_2O_3 gate insulator," *Jpn. J. Appl. Phys.*, 55, 120305, Nov. 2016, DOI: 10.7567/JJAP.55.120305.

[21] N. Ramanan, "Investigation of ALD Dielectrics for Improved Threshold Voltage Stability and Current Collapse Suppression in AlGaN/GaN MOS-HFETs," Ph.D. dissertation, Dept. Elect. Eng., North Carolina State University, Raleigh, NC, 2014.

[22] N. Ramanan, B. Lee, C. Kirkpatrick, R. Suri, and V. Misra, "Properties of atomic layer deposited dielectrics for AlGaN/GaN device passivation," *Semicond. Sci. Technol.*, vol. 28, no. 7, 074004, Jun. 2013, DOI: 10.1088/0268-1242/28/7/074004.

[23] C. Liu, E. F. Chor, and L. S. Tan, "Enhanced device performance of AlGaN/GaN HEMTs using HfO_2 high-*k* dielectric for surface passivation and gate oxide," *Semicond. Sci. Technol.*, vol. 22, pp. 522–527, Mar. 2007, DOI: 10.1088/0268-1242/22/5/011.

[24] P. D. Ye, B. Yang, K. K. Ng, J. Bude, G. D. Wilk, S. Halder, and J. C. M. Hwang, "GaN metal-oxide-semiconductor high-electron-mobility-transistor with atomic layer deposited Al_2O_3 as gate dielectric," *Appl. Phys. Lett.*, 86, 063501, Jan. 2005, DOI: 10.1063/1.1861122.

[25] D. Bisi, M. Meneghini, M. V. Hove, D. Marcon, S. Stoffels, T. L. Wu, S. Decoutere, G. Meneghesso, E. Zanoni, "Trapping mechanisms in GaN-based MIS-HEMTs grown on silicon substrate," *Phys. status solidi*, vol. 212, no. 5, pp. 1122–1129, Feb. 2015, DOI: 10.1002/pssa.201431744.

[26] B. M. Green, K. K. Chu, E. M. Chumbes, J. A. Smart, J. R. Shealy, and L. F. Eastman, "The effect of surface passivation on the microwave characteristics of undoped AlGaN/GaN HEMTs," *IEEE Electron Device Lett.*, vol. 21, no. 6, pp. 268–270, Jun. 2000, DOI: 10.1109/55.843146.

[27] S. Arulkumaran, T. Egawa, H. Ishikawa, T. Jimbo, and Y. Sano, "Surface passivation effects on AlGaN/GaN high-electron-mobility transistors with SiO_2, Si_3N_4 and silicon oxynitride," *Appl. Phys. Lett.*, vol. 84, no. 4, pp. 613–615, Jan. 2004, DOI: 10.1063/1.1642276.

[28] P. Kordoš, G. Heidelberger, J. Bernát, A. Fox, M. Marso, and H. Lüth, "High-power SiO_2/AlGaN/GaN metal-oxide-semiconductor heterostructure field-effect transistors," *Appl. Phys. Lett.*, vol. 87, 143501, Sep. 2005, DOI: 10.1063/1.2058206.

[29] Z. H. Liu, G. I. Ng, S. Arulkumaran, Y. K. T. Maung, and H. Zhou, "Temperature-dependent forward gate current transport in atomic-layer-deposited Al_2O_3/AlGaN/GaN metal–insulator–semiconductor high electron mobility transistor," *Appl. Phys. Lett.*, vol. 98, 163501, Apr. 2011, DOI: 10.1063/1.3573794.

[30] J. Kwon, M. Dai, M. D. Halls, and Y. J. Chabal, "Detection of a Formate Surface Intermediate in the Atomic Layer Deposition of High-κ Dielectrics Using Ozone," *Chem. Mater.*, vol. 20, pp. 3248–3250, May 2008, DOI: 10.1021/cm703667h.

[31] J. Niinistö, M. Putkonen, L. Niinistö, K. Arstila, T. Sajavaara, J. Lu, K. Kukli, M. Ritala, and M. Leskelä, "HfO_2 Films Grown by ALD Using Cyclopentadienyl-Type Precursors and H_2O or O_3 as Oxygen Source," *J. Electrochem. Soc.*, vol. 153, F39–F45, Feb. 2006, DOI: 10.1149/1.2162447.

[32] H. B. Park, M. Cho, J. Park, S. W. Lee, C. S. Hwang, J.-P. Kim, J.-H. Lee, N.-I. Lee, H.-K Kang, J.-C. Lee, and S.-J. Oh, "Comparison of HfO_2 films grown by atomic layer deposition using $HfCl_4$ and H_2O or O_3 as the oxidant," *J. Appl. Phys.*, vol. 94, pp. 3641–3647, Sep. 2003, DOI: 10.1063/1.1599980.

[33] Z. H. Liu, G. I. Ng, H. Zhou, S. Arulkumaran, and Y. K. T. Maung, "Reduced surface leakage current and trapping effects in AlGaN/GaN high electron mobility transistors on silicon with SiN/Al_2O_3 passivation," *Appl. Phys. Lett.*, vol. 98, 113506, Mar. 2011, DOI: 10.1063/1.3567927.

[34] J. B. Kim, D. R. Kwon, K. Chakrabarti, C. Lee, K. Y. Oh, and J. H. Lee, "Improvement in Al_2O_3 dielectric behavior by using ozone as an oxidant for the atomic layer deposition technique," *J. Appl. Phys.*, vol. 92, pp. 6739–6742, Dec. 2002, DOI: 10.1063/1.1515951.

[35] S. K. Kim, S. W. Lee, C. S. Hwang, Y.-S. Min, J. Y. Won, and J. Jeong, "Low Temperature (<100°C) Deposition of Aluminum Oxide Thin Films by ALD with O_3 as Oxidant," *J. Electrochem. Soc.*, vol. 153, issue 5, F69–F76. Mar. 2006, DOI: 10.1149/1.2177047.

[36] M. Dai, "In situ infrared spectroscopy study of atomic layer deposition of high-κ metal oxide and metal on passivated silicon surfaces," Ph.D. dissertation, Rutgers, The State University of New Jersey, pp. 52–53, Oct. 2008.

[37] C. Liu, E. F. Chor, and L. S. Tan, "Investigations of HfO_2/AlGaN/GaN metal-oxide-semiconductor high electron mobility transistors," *Appl. Phys. Lett.*, vol. 88, 173504, Apr. 2006, DOI: 10.1063/1.2198507.

[38] C. Liu, E. F. Chor, and L. S. Tan, "Improved DC performance of AlGaN/GaN high electron mobility transistors using hafnium oxide for surface passivation," *Thin Solid Films*, vol. 515, pp. 4369–4372, Mar. 2007. DOI: 10.1016/j.tsf.2006.07.103.

[39] V. Tokranov, S. L. Rumyantsev, M. S. Shur, R. Gaska, S. Oktyabrsky, R. Jain, and N. Pala, "HfO_2/AlGaN/GaN structures with HfO_2 deposited at ultra low pressure using an e-beam," *Phys. Stat. Sol. (RRL)*, vol. 1, no. 5, pp. 199–201, Oct. 2007, DOI: 10.1002/pssr.200701136.

[40] J. Swerts, N. Peys, L. Nyns, A. Delabie, A. Franquet, J. W. Maes, S. Van Elshocht, and S. De Gendt, "Impact of precursor chemistry and process conditions on the scalability of ALD HfO_2 gate dielectrics," *J. Electrochem. Soc.*, vol. 157, no. 1, G26–G31, Nov. 2009, DOI: 10.1149/1.3258664.

[41] M. Cho, J. Park, H. B. Park, S. W. Lee, T. J. Park, C. S. Hwang, G. H. Jang, and J. Jeong, "Comparison between atomic-layer-deposited HfO_2 films using O_3 or H_2O oxidant and $Hf[N(CH_3)_2]_4$ precursor," *Appl. Phys. Lett.*, vol. 85, no. 24, pp. 5953–5955, Dec. 2004, DOI: 10.1063/1.1829773.

[42] A. Kawano, S. Kishimoto, Y. Ohno, K. Maezawa, T. Mizutani, H. Ueno, T. Ueda, and T. Tanaka, "AlGaN/GaN MIS-HEMTs with HfO_2 gate insulator," *Phys. Stat. Sol. (C)*, vol. 7, pp. 2700–2703, Jun. 2007, DOI: 10.1002/pssc.200674769.

[43] E. Miyazaki, Y. Goda, S. Kishimoto, and T. Mizutani, "Comparative study of AlGaN/GaN metal–oxide–semiconductor heterostructure field-effect transistors with Al_2O_3 and HfO_2 gate oxide," *Solid-State Electron.*, vol. 62, pp. 152–155, Aug. 2011, DOI: 10.1016/j.sse.2011.04.017.

[44] Y. C. Chang, W. H. Chang, Y. H. Chang, J. Kwo, Y. S. Lin, S. H. Hsu, J. M. Hong, C. C. Tsai, and M. Hong, "Drain current enhancement and negligible current collapse in GaN MOSFETs with atomic-layer-deposited HfO_2 as a gate dielectric," *Microelectron. Eng.*, vol. 87, no. 11, pp. 2042–2045, Nov. 2010, DOI: 10.1016/j.mee.2010.02.013.

[45] S. Sugiura, S. Kishimoto, T. Mizutani, M. Kuroda, T. Ueda, and T. Tanaka, "Normally-off AlGaN/GaN MOSHFETs with HfO_2 gate oxide," *Phys. Stat. Sol. (C)*, vol. 5, no. 6, pp. 1923–1925, Dec. 2007, DOI: 10.1002/pssc.200778449.

[46] Y. C. Chang, H. C. Chiu, Y. J. Lee, M. L. Huang, K. Y. Lee, and M. Hong, "Structural and electrical characteristics of atomic layer deposited high κ HfO_2 on GaN," *Appl. Phys. Lett.*, vol. 90, 232904, Jun. 2007, DOI: 10.1063/1.2746057.

[47] R. Suri, "Investigation of MOS Interfaces with Atomic-Layer-Deposited High-k Gate Dielectrics on III-V Semiconductors," Ph.D. dissertation, Dept. Elect. Eng., North Carolina State University, Raleigh, NC, pp. 28–32, 2010.

[48] B. J. Baliga, "Gallium nitride devices for power electronic applications," *Semicond. Sci. Technol.*, 28, 074011, 2013.

[49] E. Zanoni, M. Meneghini, G. Meneghesso, D. Bisi, I. Rossetto, and A. Stocco, "Reliability and failure physics of GaN HEMT, MIS-HEMT and p-gate HEMTs for power switching applications: Parasitic effects and degradation due to deep level effects and time-dependent breakdown phenomena," in *Proc. IEEE Wksh., Wide Bandgap Power Devices Appl. (WiPDA)*, pp. 75–80, Nov. 2015.

[50] E. A. Jones, F. F. Wang, and D. Costinett, "Review of commercial GaN power devices and GaN-based converter design challenges," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 707–719, Sep. 2016.

[51] S. J. Pearton, J. C. Zolper, R. J. Shul, and F. Ren, "GaN: Processing, defects, and devices," *J. Appl. Phys.*, vol. 86, no. 1, pp. 1–78, Jul. 1999.

[52] G. Meneghesso *et al.*, "Gallium Nitride HEMTs: advantages, opportunities and challenges," 2014. Available: http://www.iunet.info/doc/Meneghesso.pdf

[53] Y. Ma, "EPC GaN Transistor Application Readiness: Phase Three Testing," 2011. Available: https://epc-co.com/epc/Portals/0/epc/documents/product-training/EPC_Phase_Three_Rel_Report.pdf

[54] E. J. Kim, L. Wang, P. M., Asbeck, K. C. Saraswat, and P. C. Mclntyre, "Border traps in $Al_2O_3/In_{0.53}Ga_{0.47}As$ (100) gate stacks and their passivation by hydrogen anneals", *Appl. Phys. Lett.*, vol. 96, p. 012906, 2010.

[55] H. J. Quah and K. Y. Cheong, "Effects of post-deposition annealing ambient on Y_2O_3 gate deposited on silicon by RF magnetron sputtering," *J. Alloys Compd.*, vol. 529, pp. 73–83, Jul. 2012.

[56] R. Choi, C. S. Kang, H. J. Cho, Y. H. Kim, M. S. Akbar, and J. C. Lee, "Effects of high temperature forming gas anneal on the characteristics of metal–oxide–semiconductor field-effect transistor with HfO_2 gate stack", *Appl. Phys. Lett.*, vol. 84, pp. 4839–4841, 2004.

[57] Y. Oshima, Y. Sun, D. Kuzum, T. Sugawara, K. C. Saraswat, P. Pianetta, and P. C. McIntyre, "Chemical bonding, interfaces, and defects in hafnium oxide/germanium oxynitride gate stacks on Ge(100)", *J. Electrochem. Soc.*, vol. 155, G304–G309, 2008.

[58] E. P. Gusev *et al.*, "Charge Trapping in Aggressively Scaled Metal Gate/High-*k* Stacks," *IEDM Tech. Dig.*, pp. 403–405, 2004.

[59] K. L. Ganapathi, N. Bhat, and S. Mohan, "Optimization of Oxygen flow rate for E-beam evaporated HfO_2 thin films," *Int. Conf. on Emerg. Electron.*, 2012.

[60] M. Schmidt, M. C. Lemme, H. Kurz, T. Witters, T. Schram, K. Cherkaoui, A. Negara, and P. K. Hurley, "Impact of H_2/N_2 annealing on interface defect densities in $Si(100)/SiO_2/HfO_2/TiN$ gate stacks," *Microelectron. Eng.*, vol. 80, pp. 70–73, Jun. 2005.

[61] Z. Liu, H. J. Wann, P. K. KO, C. Hu, and Y. C. Cheng, "Improvement of Charge Trapping Characteristics of N_2O-Annealed and Reoxidized N_2O-Annealed Thin Oxides," *IEEE Electron Device Lett.*, vol. 13, p. 519, 1992.

[62] Z. H. Liu, J. T. Krick, H. J. Wann, P. K. KO. C. Hu, and Y. C. Cheng, "The Effects of Furnace N_2O Annealing on MOSFETs," *IEDM Tech. Dig.*, 625, 1992.

[63] B. Lee, Y. Choi, C. Kirkpatrick, A. Huang, and V. Misra, "Performance enhancement of AlGaN/GaN metal-oxide-semiconductor heterojunction field-effect transistor (MOSHFET) with atomic layer deposition (ALD) high-k HfAlO gate dielectric layer", in *Proc. IEEE Int. Semicond. Device Res. Symp. (ISDRS)*, 2011.

[64] Z. Zhang *et al.*, "Studies on High-Voltage GaN-on-Si MIS-HEMTs Using LPCVD Si_3N_4 as Gate Dielectric and Passivation Layer," *IEEE Trans. Electron Devices*, vol. 63, no. 2, pp. 731–738, Feb. 2016.

[65] Y.C. Lin, *et al.*, "Optimization of gate insulator material for GaN MIS-HEMT," in *Proc. 2016 28th Int. Symp. Power Semicond. Devices and ICs (ISPSD)*, pp. 115–118, 2016.

[66] R. D. Long and P. C. McIntyre, "Surface Preparation and Deposited Gate Oxides for Gallium Nitride Based Metal Oxide Semiconductor Devices," *Materials*, vol. 5, no. 7, pp. 1297–1335, 2012.

[67] S. R. Bahl, "A comprehensive methodology to qualify the reliability of GaN products," 2015. Available: http://www.ti.com/lit/wp/slyy070/slyy070.pdf

[68] S. Bahl, "Application-relevant Qualification of Emerging Semiconductor Power Devices," Presented at the Applied Power Electronics Conference (APEC), 2016. Available: http://www.ti.com/lit/wp/slyy091/slyy091.pdf

[69] T. McDonald, "State of Demonstrated HV GaN Reliability and Further Requirements," presented at the Applied Power Electronics Conference (APEC), 2015. Available: https://www.infineon.com/dgdl/Infineon-Presentation_GalliumNitride_APEC2015_ReliabilityofGaNDevices-AP-v01_00-EN.pdf?fileId=5546d4624bcaebcf014c2d1d673402e1

[70] R. Strittmatter, C. Zhou, A. Lidow, and Y. Ma, "Enhancement Mode Gallium Nitride Transistor Reliability," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, pp. 1409–1413, Sep. 2015.

[71] Y. Yue, Y. Hao, J. Zhang, J. Ni, W. Mao, Q. Feng, and L. Liu, "AlGaN/GaN MOS-HEMT With HfO_2 Dielectric and Al_2O_3 Interfacial Passivation Layer Grown by Atomic Layer Deposition," *IEEE Electron Device Lett.*, vol. 29, no. 8, pp. 838–840, Aug. 2008.

[72] J. Shi, L. F. Eastman, X. Xin, and M. Pophristic, "High performance AlGaN/GaN power switch with HfO_2 insulation," *Appl. Phys. Lett.*, vol. 95, no. 4, p. 042103, Jul. 2009.

[73] J. Shi and L. F. Eastman, "Correlation Between AlGaN/GaN MISHFET Performance and HfO_2 Insulation Layer Quality," *IEEE Electron Device Lett.*, vol. 32, no. 3, pp. 312–314, Mar. 2011.

[74] X. Xin, J. Shi, L. Liu, J. Edwards, K. Swaminathan, M. Pabisz, M. Murphy, L. F. Eastman, and M. Pophristic, "Demonstration of Low-Leakage-Current Low-On-Resistance 600-V 5.5-A GaN/AlGaN HEMT," *IEEE Electron Device Lett.*, vol. 30, no. 10, pp. 1027–1029, Oct. 2009, DOI: 10.1109/LED.2009.2029130.

[75] A. Colón and J. Shi, "High-κ insulating materials for AlGaN/GaN metal insulator semiconductor heterojunction field effect transistors," *Solid-State Electron.*, vol. 99, pp. 25–30, Jun. 2014, DOI: 10.1016/j.sse.2014.05.005.

[76] Y. Hori, Z. Yatabe, and T. Hashizume, "Characterization of interface states in Al_2O_3/AlGaN/GaN structures for improved performance of high-electron-mobility transistors," *J. Appl. Phys.*, 114, 244503, 2013.

[77] W. Zhu, J. P. Han, and T. P. Ma, "Mobility measurement and degradation mechanisms of MOSFETs made with ultrathin high-κ dielectrics," *IEEE Trans. Electron Devices*, vol. 51, no. 1, pp. 98–105, Jan. 2004.

[78] I. Daumiller, C. Kirchner, M. Kamp, K. J. Ebeling, and E. Kohn, "Evaluation of the temperature stability of AlGaN/GaN heterostructure FET's," *IEEE Electron Device Lett.*, vol. 20, no. 9, pp. 448–450, 1999.

[79] B. Lee, Y. Choi, C. Kirkpatrick, A. Q. Huang, and V. Misra, "Improved high temperature device transport properties and off-state characteristics of AlGaN/GaN power device with atomic layer deposition of HfAlO high-k dielectric," *Semicond. Sci. Technol.*, vol. 28, 074016, 2013.

[80] G. Simin, A. Tarakji, X. Hu, A. Koudymov, J. Yang, M. A. Khan, M. S. Shur, and R. Gaska, "High-temperature performance of AlGaN/GaN metal–oxide–semiconductor heterostructure field-effect-transistors," *Phys. Status Solidi (a)*, vol. 188, pp. 219–222, 2001.

[81] F. Husna, M. Lachab, M. Sultana, V. Adivarahan, Q. Fareed, and A. Khan, "High-Temperature Performance of AlGaN/GaN MOSHEMT with SiO_2 Gate Insulator Fabricated on Si (111) Substrate," *IEEE Trans. Electron Device*, vol. 59, no. 9, pp. 2424–2429, 2012.

[82] D. Donoval, M. Florovic, D. Gregušová, J. Kovác, and P. Kordoš, "High temperature performance of AlGaN/GaN HFETs and MOSFETs," *Microelectron. Reliab.*, vol. 48, no. 10, pp. 1669–1672, 2008.

[83] N. Maeda, K. Tsubaki, T. Saitoh, and N. Kobayashi, "High-temperature electron transport properties in AlGaN/GaN heterostructures," *Appl. Phys. Lett.*, vol. 79, no. 11, pp. 1634–1636, 2001.

[84] S. Arulkumaran, T. Egawa, H. Ishikawa, and T. Jimbo, "High-temperature effects of AlGaN/GaN high-electron-mobility transistors on sapphire and semi-insulating SiC substrates," *Appl. Phys. Lett.*, vol. 80, no. 12, pp. 2186–2188, 2002.

[85] R. Quay, *Gallium Nitride Electronics*, ser. Mater. Sci. Berlin, Germany: Springer, 2008, ch. 7, p. 332.

[86] A. P. Tomás, M. Placidi, N. Baron, S. Chenot, Y. Cordier, J. C. Moreno, A. Constant, P. Godignon, and J. Millán, "GaN transistor characteristics at elevated temperatures," *J. Appl. Phys.*, vol. 106, no. 7, p. 074519, Oct. 2009.

[87] C. Detavernier, J. Dendooven, S. P. Sree, K. F. Ludwig, and J. A. Martens, "Tailoring nanoporous materials by atomic layer deposition," *Chem. Soc. Rev.*, vol. 40, pp. 5242–5253, 2011, DOI: 10.1039/c1cs15091j.

[88] Y. Lu, S. Yang, Q. Jiang, Z. Tang, B. Li, and K. J. Chen, "Characterization of V_T-instability in enhancement-mode Al_2O_3-AlGaN/GaN MISHEMTs," *Phys. Status Solidi (C)*, vol. 10, no. 11, pp. 1397–1400, Nov. 2013.

[89] K. Matocha, T. P. Chow, and R. J. Gutmann, "High-Voltage Normally Off GaN MOSFETs on Sapphire Substrates," *IEEE Trans. Electron Devices*, vol. 52, pp. 6–10, 2005.

[90] R. Brown *et al.*, "A Sub-Critical Barrier Thickness Normally-Off AlGaN/GaN MOS-HEMT," *IEEE Electron Device Lett.*, vol. 35, no. 9, pp. 906–908, Sep. 2014.

[91] H. Kambayashi *et al.*, "High Quality SiO_2/Al_2O_3 Gate Stack for GaN Metal–Oxide–Semiconductor Field-Effect Transistor," *Jpn. J. Appl. Phys.*, vol. 52, no. 4, pp. 04CF09-1–04CF09-6, Apr. 2013.

[92] J. Wu, W. Lu, and P. K. L. Yu, "Normally-OFF AlGaN/GaN MOS-HEMT with a Two–Step Gate Recess," in *Proc. Int. Conf. Electron Devices Solid-State Circuits*, pp. 594–596, Jun. 2015.

[93] C. Tang, G. Xie, and K. Sheng, “Enhancement-mode GaN-on-Silicon MOS-HEMT using Pure Wet Etch Technique,” in *Proc. Int. Symp. Power Semiconductor Devices IC’s*, pp. 233–236, May 2015.

[94] S. Hamady, F. Morancho, B. Beydoun *et al.*, “Scalable normally-off MIS-HEMT using Fluorine implantation below the channel,” in *Proc. 22nd Int. Symp. Power Electronics*, pp. 124–127, 2014.

[95] G. Longobardi, “GaN Power devices - Physics of GaN devices,” Jan. 2016. Available: https://youtu.be/yOS6gWUCMis

[96] Y. Niiyama, S. Ootomo, J. Li, T. Nomura, S. Kato, and T. P. Chow, “Normally off operation GaN-based MOSFETs for power electronics applications,” *Semicond. Sci. Technol.*, vol. 25, no. 12, p. 125006, 2010.

[97] K. B. Lee *et al.*, “Enhancement-mode metal–insulator–semiconductor GaN/AlInN/GaN heterostructure field-effect transistors on Si with a threshold voltage of +3.0 V and blocking voltage above 1000 V,” *Appl. Phys. Exp.*, vol. 8, p. 036502, Feb. 2015.

[98] A. Taube, M. Sochacki, J. Szmidt, E. Kaminska, and A. Piotrowska, “Modelling and Simulation of Normally-Off AlGaN/GaN MOS-HEMTs,” *INTL J. Electron. Telecommun.*, vol. 60, no. 3, pp. 253–258, Sep. 2014.

[99] S. L. Zhao *et al.*, “Enhancement-mode Al_2O_3/InAlN/AlN/GaN metal–insulator–semiconductor high-electron-mobility transistor with enhanced breakdown voltage using fluoride-based plasma treatment,” *Appl. Phys. Exp.*, vol. 7, no. 7, p. 071002, Jul. 2014.

[100] B. Lee, C. Kirkpatrick, Y.-H. Choi, X. Yang, A. Q. Huang, and V. Mishra, “Normally-Off AlGaN/GaN MOSHFET using ALD SiO2 tunnel dielectric and ALD HfO2 charge storage layer for power device application,” *Phys. Status Solidi (C)*, vol. 9, nos. 3–4, pp. 868–870, Mar. 2012.

[101] B. S. Eller, J. Yang, and R. J. Nemanich, “Electronic surface and dielectric interface states on GaN and AlGaN,” *J. Vac. Sci. Technol.*, A 31, 050807, Jun. 2013, DOI: 10.1116/1.4807904.

[102] R. Vetury, N.-Q. Zhang, S. Keller, and U. K. Mishra, “The Impact of Surface States on the DC and RF Characteristics of AlGaN/GaN HFETs,” *IEEE Trans. Electron Devices*, vol. 48, pp. 560–566, Mar. 2001.

[103] N. Ramanan, B. Lee, and V. Misra, "A Novel Methodology using Pulsed-IV for Interface or Border Traps Characterization on AlGaN/GaN MOSHFETs," in *Proc. IEEE 26th Int. Symp. Power Semiconductor Devices IC's (ISPSD)*, pp. 366–369, Jun. 2014.

[104] J. A. Mittereder, S. C. Binari, P. B. Klein, J. A. Roussos, D. S. Katzer, D. F. Storm, D. D. Koleske, A. E. Wickenden, and R. L. Henry, "Current collapse induced in AlGaN/GaN high-electron-mobility transistors by bias stress, *Appl. Phys. Lett.*, vol. 83, 1650, 2003.

[105] G. Meneghesso, F. Rampazzo, P. Kordoš, G. Verzellesi, and E. Zanoni, "Current Collapse and High-Electric-Field Reliability of Unpassivated GaN/AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 53, no. 12, pp. 2932–2941, Dec. 2006.

[106] R. C. Fitch, D. E. Walker, K. D. Chabak, J. K. Gillespie, M. Kossler, M. Trejo, A. Crespo, L. Liu, T. S. Kang, C.-F. Lo, F. Ren, D. J. Cheney, and S. J. Pearton, "Comparison of passivation layers for AlGaN/GaN high electron mobility transistors," *J. Vacuum Sci. Technol. B*, vol. 29, no. 6, p. 061204, Nov. 2011.

[107] M. Lachab, M. Sultana, H. Fatima, *et al.*, "Direct current performance and current collapse in AlGaN/GaN insulated gate high-electron mobility transistors on Si (111) substrate with very thin SiO_2 gate dielectric," *Semicond. Sci. Technol.*, vol. 27, pp. 125001-1–125001-7, Oct. 2012.

[108] J. Bernat, M. Wolter, A. Fox, M. Marso, J. Flynn, G. Brandes, and P. Kordos, "Impact of layer structure on performance of unpassivated AlGaN/GaN/SiC HEMTs," *Electron. Lett.*, vol. 40, no. 1, pp. 78–80, Jan. 2004.

[109] K. Prabhakaran, T. G. Andersson, and K. Nozawa, "Nature of native oxide on GaN surface and its reaction with al," *Appl. Phys. Lett.*, vol. 69, no. 21, pp. 3212–3214, 1996.

[110] S. W. King, J. P. Barnak, M. D. Bremser, K. M. Tracy, C. Ronning, R. F. Davis, and R. J. Nemanich, "Cleaning of AlN and GaN surfaces," *J. Appl. Phys.*, vol. 84, no. 9, pp. 5248–5260, Nov. 1998.

[111] H. Kim, V. Tilak, B. M. Green, H. Cha, J. A. Smart, J. R. Shealy, and L. F. Eastman, "Degradation Characteristics of AlGaN-GaN High Electron Mobility Transistors," in Proc. *IEEE Int. Reliability Physics Symp.*, pp. 214–218, 2001.

[112] J. Joh and J. A. del Alamo, "Mechanisms for Electrical Degradation of GaN High-Electron Mobility Transistors," *IEDM Tech. Dig.*, pp. 415–418, 2006.

[113] J. Joh and J. A. del Alamo, "Gate Current Degradation Mechanisms of GaN High Electron Mobility Transistors," *IEDM Tech. Dig.*, pp. 385–388, 2007.

[114] L. Ruguan, W. Yuansheng, Z. Chang, L. Xueyang, L. Ping, and H. Yun, "Impact of high temperature reverse bias (HTRB) stress on the Degradation of AIGaN/GaN HEMTs," *Electron Devices Solid State Circuits (EDSSC), 2014 IEEE Int. Conf.*, Jun. 2014, DOI: 10.1109/EDSSC.2014.7061108.

[115] F. Iucolano, F. Roccaforte, A. Alberti, C. Bongiorno, S. Di Franco, and V. Raineri, "Temperature dependence of the specific resistance in Ti/Al/Ni/Au contacts on n-type GaN," *J. Appl. Phys.*, vol. 100, p. 123706, 2006.

[116] J. Wuerfl, E. Bahat-Treidel, F. Brunner, E. Cho, O. Hilt, P. Ivo, A. Knauer, P. Kurpas, R. Lossy, M. Schulz, S. Singwald, M. Weyers, and R. Zhytnytska, "Reliability issues of GaN based high voltage power devices," *Microelectron. Rel.*, vol. 51, pp. 1710–1716, 2011.

[117] J. A. del Alamo and J. Joh, "GaN HEMT reliability," *Microelectron. Rel.*, vol. 49, no. 9, pp. 1200–1206, 2009.

[118] J. Joh, "Degradation Mechanisms of GaN High Electron Mobility Transistors," Master of Science thesis, Dept. Elect. Eng., Massachusetts Institute of Technology, Cambridge, MA, pp. 15–20, 2007.

[119] P. Ivo *et al.*, "Influence of GaN cap on robustness of AlGaN/GaN HEMTs," *IEEE Int. Reliab. Phys. Symp.*, pp. 71–75, Montreal, QC, Canada, Apr. 2009.

[120] S. Arulkumaran *et al.*, "Studies on the Influences of i-GaN, n-GaN, p-GaN and InGaN Cap Layers in AlGaN/GaN High-Electron-Mobility Transistors Oxidation and the origin of the two-dimensional electron gas in AlGaN/GaN heterostructures," *Jpn. J. Appl. Phys.*, vol. 44, pp. 2953, 2005.

[121] C. J. Kirkpatrick, "Gate Stack Design for Threshold Voltage Control of Gallium Nitride Power Transistors," Ph.D. dissertation, Dept. Elect. Eng., North Carolina State University, Raleigh, NC, pp. 49–51, 2013.

[122] S. Mills, "Ultra-low Power Room TemperatureMetal Oxide Gas Sensors: A Study in Sensitivity, Selectivity and Reliability," Ph.D. dissertation, Dept. Elect. Eng., North Carolina State University, Raleigh, NC, p. 28, 2017.

[123] B. Sarkar, “Atomic Layer Deposition (ALD) Enabled Techniques for Novel Memory Applications,” Ph.D. dissertation, Dept. Elect. Eng., North Carolina State University, Raleigh, NC, pp. 26–27, 2015.

[124] N. Kaminski, O. Hilt, "SiC and GaN devices – wide bandgap is not all the same," *IET Circuits, Devices and Syst.*, vol.8, no.3, pp. 227–236, 2014.

[125] E. Zanoni, “GaN HEMT reliability research,” 2017. Available: https://www.dei.unipd.it/en/system/files/reliability%20study%20publishable%20final.pdf

[126] D. Cheney, E. Douglas, L. Liu, C.-F. Lo, B. Gila, F. Ren, and S. Pearton, “Degradation Mechanisms for GaN and GaAs High Speed Transistors,” *Materials*, vol. 5, no. 12, pp. 2498–2520, 2012.

[127] H. Kim, V. Tilak, B. M. Green, J. A. Smart, W. J. Schaff, J. R. Shealy, and L. F. Eastman, "Reliability evaluation of high power AlGaN/GaN HEMTs on SiC substrate," *phys. stat. sol. (a)*, vol. 188, pp. 203-206, 2001.

[128] S. Ruvimov *et al.*, “Microstructure of Ti/Al and Ti/Al/Ni/Au ohmic contacts for n-GaN,” *Appl. Phys. Lett.*, vol. 69, no. 11, pp. 1556–1558, Sep. 1996.

[129] J. K. Kim, H. W. Jang, and J.-L. Lee, “Mechanism for ohmic contact formation of Ti on *n*-type GaN investigated using synchrotron radiation photoemission spectroscopy,” *J. Appl. Phys.*, vol. 91, no. 11, pp. 9214–9217, 2002.

[130] C. Lu, H. Chen, X. Lv, X. Xie, and S. N. Mohammad, “Temperature and doping-dependent resistivity of Ti/AlPd/Au multilayer ohmic contact to n-GaN,” *J. Appl. Phys.*, vol. 91, pp. 9218–9224, 2002.

[131] M. Higashiwaki, K. Sasaki, T. Kamimura, M. H. Wong, D. Krishnamurthy, A. Kuramata, T. Masui, and S. Yamakoshi, “Depletion-mode Ga_2O_3 metal-oxide-semiconductor field-effect transistors on β-Ga_2O_3 (010) substrates and temperature dependence of their device characteristics,” *Appl. Phys. Lett.*, vol. 103, no. 12, p. 123511, Sep. 2013.

[132] K. Irmscher, Z. Galazka, M. Pietsch, R. Uecher, and R. Fornari, “Electrical properties of β−Ga_2O_3 single crystals grown by the Czochralski method”, *J. Appl. Phys.*, vol. 110, pp. 063720, 2011.

[133] K. Sasaki, A. Kuramata, T. Masui, E. G. Villora, K. Shimamura, and S. Yamakoshi, “Device-Quality β-Ga_2O_3 Epitaxial Films Fabricated by Ozone Molecular Beam Epitaxy,” *Appl. Phys. Exp.*, vol. 5, p. 035502, Feb. 2012.