ABSTRACT

KANALE, AJIT. Dynamic Characterization and Failure Analysis of the 1200V, 10A Silicon Carbide JBSFET (Under the direction of Dr. B. Jayant Baliga and Dr. Subhashish Bhattacharya).

The power electronics and the power semiconductor devices industries are intimately intertwined in their efforts to increase the efficiency of power conversion. Advances in one field inform and drive the efforts in another in this quest.

Over the past few decades, silicon carbide has risen to prominence as the choice material for fabricating power devices, due to its superior breakdown electric field, low on-resistance, low switching losses and high temperature range of operation. Recent research has expanded this effort to create monolithic devices which can replace modular switches made of discrete components. In addition to simplifying the packaging, this also improves the performance of the switch while providing enhanced robustness to extreme current and voltage stresses.

The focus of this work is to characterize the 1200V silicon carbide JBSFET – a monolithic integration of the conventional planar MOSFET and a JBS diode. JBSFETs fabricated under PowerAmerica were packaged in TO-3 and TO-247 packages. These devices were subject to static and dynamic characterization along with a conventional silicon carbide planar MOSFET to enable a comparative study of the two structures. While the static characterization involved on-resistance, threshold and blocking voltage measurement along with third quadrant operation, the dynamic characterization was conducted using two separate tests – switching losses using a double pulse tester, and short circuit characterization tests using a separate short circuit test setup. It has been shown that the JBSFET is a superior switch and a robust device compared to the conventional MOSFET.

This thesis introduces the JBSFET and provides a brief history of power electronics building up to the JBSFET in Chapter 1. The static characterization is detailed in Chapter 2. The switching tests are described in Chapter 3. Short circuit tests are discussed in Chapter 4. Each chapter includes a discussion of the device physics governing the observed performance. The thesis concludes with an overview the JBSFET as a superior switch and the future possibilities for power electronics.

Dynamic Characterization and Failure Analysis of the 1200V, 10A Silicon Carbide JBSFET

by
Ajit R Kanale

A thesis submitted to the Graduate Faculty of
North Carolina State University
in partial fulfillment of the
requirements for the degree of
Master of Science

Electrical Engineering

Raleigh, North Carolina
2019

APPROVED BY:

Dr. B . Jayant Baliga Co-Chair of Advisory Committee	Dr. Subhashish Bhattacharya Co-Chair of Advisory Committee

Dr. Douglas C. Hopkins

DEDICATION

To my parents, Meenakshi and Raghavendra

BIOGRAPHY

Ajit Kanale was born in Bangalore, India. He graduated with a Bachelors' Degree in Avionics from the Indian Institute of Space Science and Technology, Thiruvananthapuram, India. In 2012, He was posted as a Satellite Engineer in the Indian Space Research Organization's satellite mission control facility at Bangalore where he managed remote sensing and scientific satellite missions.

In 2016, Ajit moved to Raleigh, NC to pursue graduate studies at the North Carolina State University. His research is in the domain of power electronics and power devices under the joint guidance of Prof. Subhashish Bhattacharya and Prof. Jayant Baliga. As part of his MS research, he proved the robustness of the JBSFET as compared to the planar MOSFET using dynamic characterization tests. His doctoral research explores the application of the BiDFET in AC-AC conversion applications.

ACKNOWLEDGEMENTS

I would like to thank my research advisors, Dr. Subhashish Bhattacharya and Dr. Jayant Baliga for their constant guidance throughout my graduate studies. Their queries, comments and suggestions during discussions on experimental results helped me shape my tests more efficiently. Their inputs help me evolve my writing skills and coached my expression of ideas. I would like to thank Dr. Douglas Hopkins for accepting to be on this committee and for his precise and detailed guidance on pursuing this research. He has also been very helpful in allowing us the use of PREES lab resources to package our devices.

Special thanks to Kijeong Han for his mentorship throughout my research. His guidance and discussions helped me improve my knowledge of device fabrication and testing and also improved my own approach to research in general. I must thank Bahji Ballard and Adam Morgan for their unquestioning support whenever I approached them with a fresh set of devices to be packaged. I would also like to thank Vishnu Mahadeva Iyer, Anup Anurag, Utkarsh Raheja, Sanket Parashar and Ashish Kumar for helping me out with the dynamic testing of the power devices. Their valuable inputs helped me understand, setup and conduct the dynamic characterization tests.

All this would not have been possible without the steady and unfailing support and encouragement of my parents, who have been my bedrock and inspiration in life.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF PUBLICATIONS

This work has produced technical publications in conferences. The full list of these publications is given below.

Accepted for publication in conference proceedings

1. **Ajit Kanale**, B. Jayant Baliga, Kijeong Han, Subhashish Bhattacharya, "***Experimental Study of High-Temperature Switching Performance of 1.2kV SiC JBSFET in Comparison with 1.2kV SiC MOSFET***", in the 12th European Conference on Silicon Carbide and Related Materials, Birmingham, UK, 2018
2. **Ajit Kanale**, Kijeong Han, B. Jayant Baliga, Subhashish Bhattacharya, "***Superior short circuit performance of 1.2kV SiC JBSFETs compared to 1.2kV SiC MOSFETs***", 12th in the 12th European Conference on Silicon Carbide and Related Materials, Birmingham, UK, 2018
3. Kijeong Han, **Ajit Kanale**, B. Jayant Baliga, Bahji Ballard, Adam Morgan, Douglas C. Hopkins, "***New Short Circuit Failure Mechanism for 1.2kV 4H-SiC MOSFETs and JBSFETs***", in the 6th IEEE Workshop on Wide Bandgap Power Devices and Applications, Atlanta, GA, 2018

Accepted for presentation in conference

4. Adam J. Morgan, **Ajit Kanale**, Kijeong Han, Jayant Baliga, Douglas C. Hopkins, "***New Dynamic Power MOSFET Model to Determine Maximum Device Operating Frequency***", in the IEEE Applied Power Electronics Conference and Exposition, 2019

CHAPTER 1

INTRODUCTION

1.1. A Brief history of Power Device Technology

Semiconductor power devices have been a fundamental component of power electronics systems for the past 50 years[1, 2, 3]. Since the 1950s, with the invention of the point-contact transistor by Shockley, Bardeen and Brattain[4], followed by the subsequent development of the junction transistor[5], there have been a variety of semiconductor devices being created for high-power applications[1, 6-9]. Figure 1.1. illustrates the various domains employing power devices mapped as per the system power rating and operating frequency.

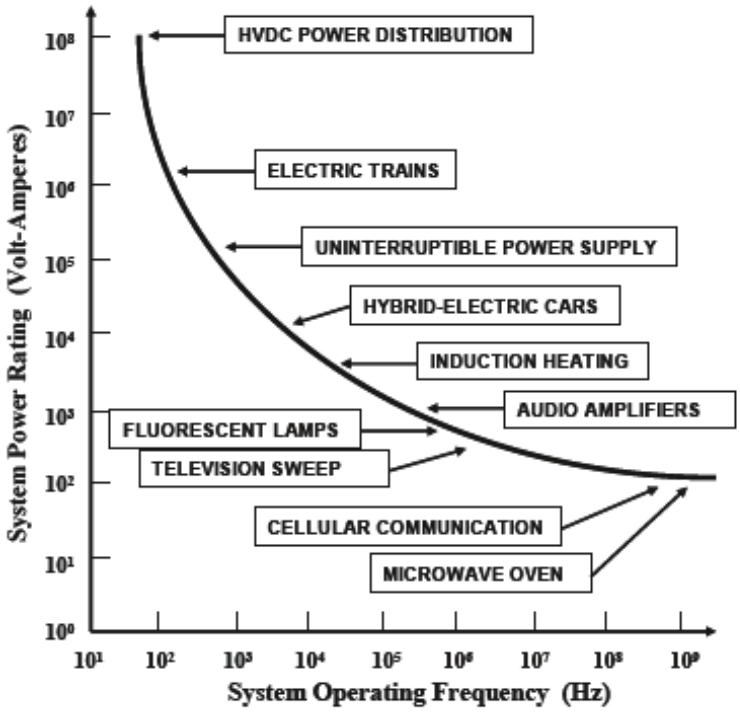


Image Reference: B. J. Baliga, "***Fundamentals of Power Semiconductor Devices***", pp.2, Springer, NY, 2008

Figure 1.1. Power device rated power and operating frequencies for different applications.

Silicon has been the material of choice for the development of power devices owing to its natural abundance, economy and adaptability of fabrication processes and favorable electrochemical properties.

The junction transistor invented at Bell Labs, was eventually developed and commercialized in the 1970s as Darlington power bipolar junction transistors (BJTs) after considerable process enhancements[10]. Power BJTs rely on a current supply to the base to control their operation. Furthermore, these devices also have poor current gain[10]. These shortcomings in the BJT led to research in voltage control of devices to simplify the drive circuitry and improve power gain. The most popular method to do this was through a metal-oxide-semiconductor (MOS) gate structure, which employed voltage signals coupled with a capacitive gate terminal to modulate a channel between two power terminals. This, subsequently led to the introduction of power MOSFETs in the 1970s. Parallel efforts to combine the high current conduction capability of bipolar devices along with the voltage control of MOS devices led to the development of MOS-gated thyristors[11], and subsequently, the IGBTs[12] in 1980s, revolutionizing the field of power conversion. Figure 1.2. displays a history of innovations in power semiconductor device technology.

Towards the turn of the new millennium, research and industrial innovations[13-15] have successfully scaled power devices over a large range of operating voltages. Figure 1.3. displays different power devices based on their operating voltage, current and frequency levels. While standalone IGBTs are shown in the graph above, multiple IGBTs have been encapsulated in modules to achieve current conduction levels closer to 4kA.

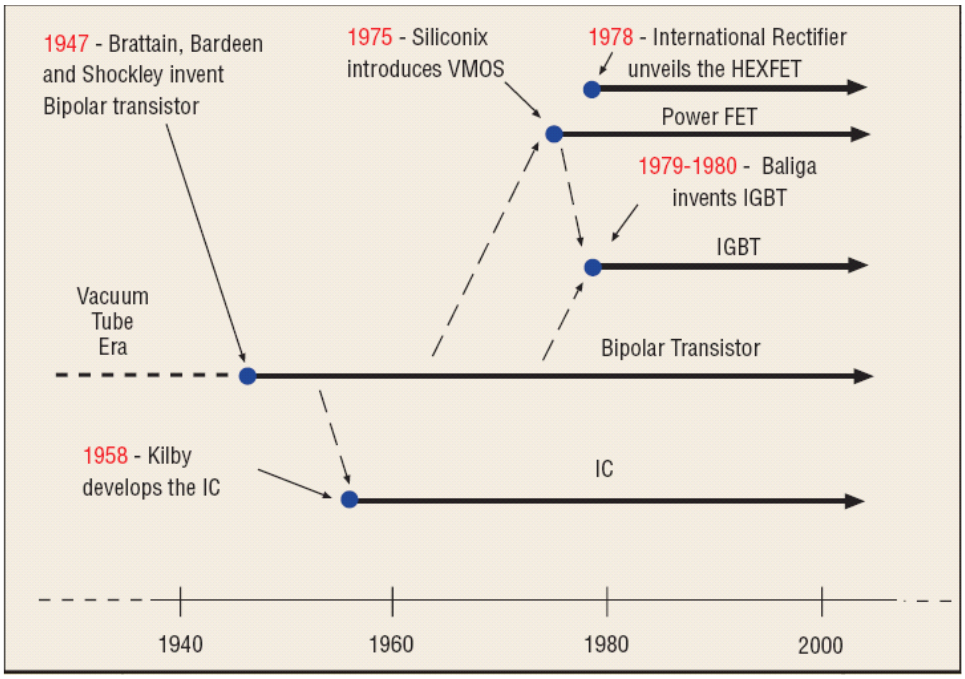
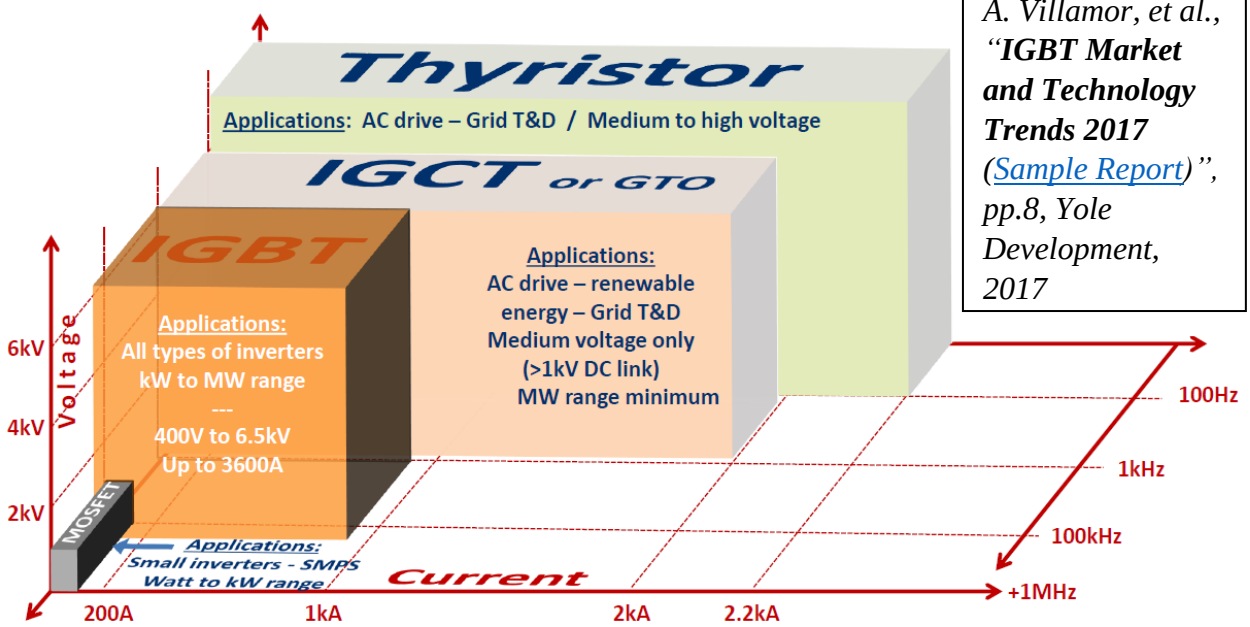


Image Reference: *S. Grossman, "**Advances in Discrete Semiconductors March On**", Power Electronics Technology, pp. 52-56, 2005*

Figure 1.2. A timeline of power semiconductor technology.



*A. Villamor, et al., "**IGBT Market and Technology Trends 2017** (Sample Report)", pp.8, Yole Development, 2017*

Figure 1.3. Silicon Power Devices arranged as per range of operation.

1.2. Wide bandgap materials and their significance in the future of Power Devices

A 1982 research article[16] showed that materials with wide bandgap would be suitable for creation of power devices. The basis for this theory is the relation of semiconductor device on-resistance with its material properties. Power devices are created with a low-doped drift region

which is designed to block reverse voltage. The resistance of an ideal, one-dimensional drift region, ignoring any effects due to edge terminations and assuming a parallel-plane electric field in reverse blocking, can be expressed[10] as

$$R_{On,Sp,Ideal} = \frac{4BV^2}{\varepsilon_S \mu_n E_C^3} \tag{1-1}$$

where BV is the breakdown voltage, ε_S is the electric permittivity of the semiconductor, μ_n is the electron mobility in the drift region and E_C is the critical electric field of breakdown. The denominator in (1-1) is called Baliga's Figure of Merit for power devices (BFoM).

$$BFoM = \varepsilon_S \mu_n E_C^3 \tag{1-2}$$

A BFoM analysis of different power semiconductor materials based on previously reported[17, 18] data illustrates that wide bandgap semiconductors can be used to produce power devices with significantly lower on-resistance.

Table 1.1. Comparison of materials based on Baliga's Figure of Merit estimates their suitability for use in designing power semiconductor devices.

Property	**Si**	**GaAs**	**GaP**	**4H-SiC**	**GaN**	**Diamond**
Bandgap (eV)	1.12	1.27	2.26	3.26	3.45	5.45
Rel. Dielectric Constant, ε_S	11.7	13.1	11.1	10.1	9	5.5
e^- Mobility μ_n ($cm^2V^{-1}s^{-1}$)	1500	8500	110	1000	1250	2200
Critical Electric Field E_C (V/cm)	3×10^5	4×10^5	7×10^5	2.2×10^6	2×10^6	1×10^7
BFoM	**4.19×10^7**	**6.31×10^8**	**3.71×10^7**	**9.52×10^9**	**7.97×10^9**	**1.07×10^{12}**
Rel. BFOM (compared to Si)	1	15.04	0.88	226.96	189.93	25535.51

Development of power devices over half a century years has pushed silicon technology to the limits of its physical performance[19-22]. Developing very high voltage devices using Silicon would require thick drift regions, resulting in higher on-resistance, thus causing conduction losses.

Silicon carbide, due to its higher electric field of breakdown, facilitates the development of power devices with a higher voltage rating and almost 1000x reduction in on-resistance compared to silicon devices of similar dimensions. This is quantified using analytical expressions relating the critical electric field of Si and SiC to the doping concentration of the drift region[10]. These relations can be used in (1-1) to obtain Si and SiC expressions for $R_{On,Sp,Ideal}$ in terms of breakdown voltage.

$$R_{On,Sp,Ideal}(Si) = 5.93 * 10^{-9} BV^{2.5} \tag{1-3}$$

$$R_{On,Sp,Ideal}(SiC) = 2.97 * 10^{-12} BV^{2.5} \tag{1-4}$$

These equations are plotted in Figure 1.4. Both equations and figure clearly show the 1000x improvement in $R_{On,Sp,Ideal}$ for SiC power devices.

There has been considerable research in the domain of SiC power devices over the past three decades[23], leading to the development of different classes of SiC devices[24-27]. Furthermore, advancements in process technology have helped to reduce the fabrication costs of silicon carbide devices[28]. Presently, several industrial entities are actively commercializing SiC devices with different power ratings[29-35]. Research interest in the development of SiC devices is growing in the form of wide-band gap semiconductor research programs and international conferences dedicated to the development of wide bandgap power electronics.

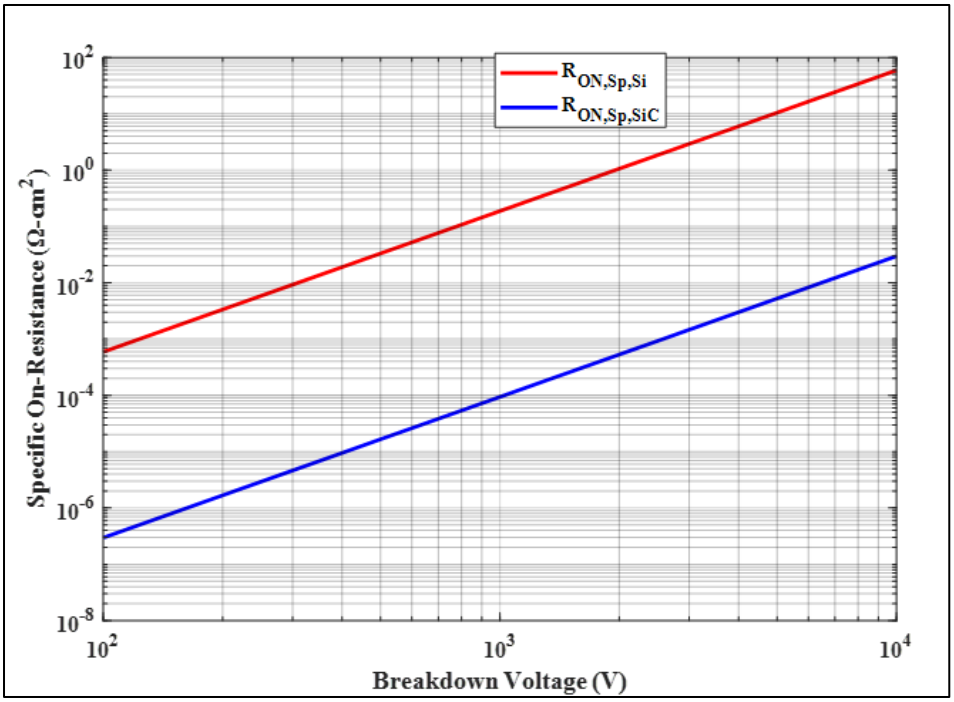


Figure 1.4. Specific R_{ON} vs Breakdown Voltage tradeoff for the ideal 1-D drift region.

1.3. The importance of Monolithic Integration

The main source of power loss in transistor circuits is the switching loss incurred due to turn-off and turn-on of the semiconductor switch. With the widespread growth of wide bandgap semiconductor power devices with rapid switching transients, there has been a considerable reduction in switching losses. As industry adopts increasingly efficient devices, the power loss due to the switch becomes comparable to that caused by parasitics within the circuit. Typical sources of parasitics are packaging and interconnections between modules and discrete devices[36]. While modules provide a simple solution to mitigating parasitics, wiring internal to the module itself contributes to stray inductances. The most optimal solution to this problem is to realize monolithically integrated devices which not only combine multiple semiconductor devices, but also eliminate the packaging bulk and stray inductances arising from connections.

While monolithic integration has transformed the low-voltage systems such as processors, memories and handheld devices, it is yet to make inroads into power device technology. However,

there have been some attempts to achieve monolithic integration of Si and SiC devices for different applications[37-38]. The JBSFET, discussed in some detail in this work, is an example of monolithic integration of the JBS diode and power MOSFET structures[39].

1.4. Structures analyzed in this Thesis – the SiC MOSFET and SiC JBSFET

1.4.1 The SiC Power MOSFET

A metal-oxide-semiconductor field-effect transistor (MOSFET) is a three terminal device which employs a voltage signal coupled with a capacitive gate to control a channel of charge carriers between two power terminals. Figure 1.5. shows the typical structure of a SiC power MOSFET.

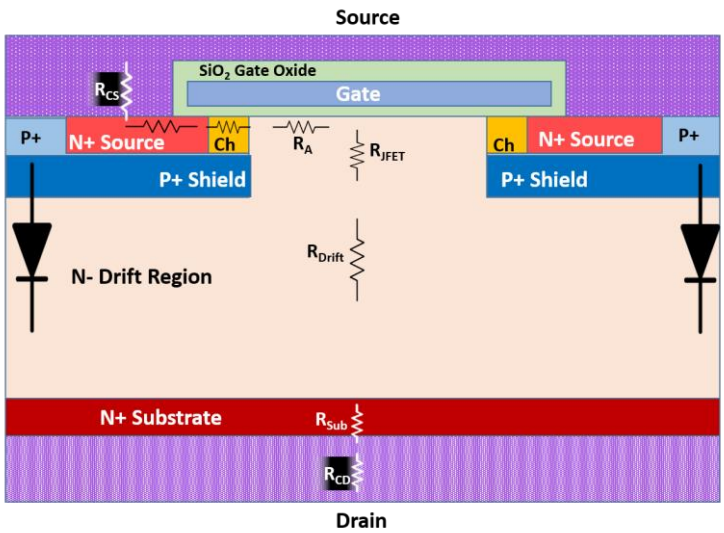


Figure 1.5. The SiC Power MOSFET Structure.

Power MOSFETs are designed with a low-doped, epitaxially grown drift region. Application of a positive bias across the drain-source contacts creates a reverse bias across the N-drift/P-base junction and a forward bias across the N-source/P-base junction. The drift region is doped such that the reverse bias depletion region is predominantly contained within itself. Devices with larger blocking voltage rating are designed with thicker drift regions. Under these conditions, the device can be turned on by the application of a positive gate voltage, which creates an inversion

channel in the P-base region under the gate oxide. Electrons are injected from the source through this channel into the drift region, hence realizing current flow through the MOSFET[10].

Silicon carbide planar MOSFET structures are equipped with a highly-doped P+ shielding region at the bottom of the P-base to prevent reach-through breakdown at high-electric fields[40].

MOSFET on-resistance is a combination of several components[10] along the path of electron flow in the device. These components are marked in Fig 5. While the major contributor for MOSFET on-resistance in Si devices is the drift region resistance, the corresponding component for SiC devices is the channel resistance[22]. This is due to the relatively low mobility of electrons in SiC. There is great interest in process optimization for SiC devices in order to improve the electron mobility in the material.

1.4.1.1. Threshold Voltage

The minimum gate bias required to create an inversion channel in the power MOSFET is called its threshold voltage, V_{TH}. Current flow begins when the gate bias exceeds the device threshold voltage. V_{TH} is a function of the choice of gate material and the P-base doping, along with interface charges at the oxide semiconductor interface[10].

1.4.1.2. Third Quadrant Operation

The power MOSFET has a body diode, in the form of a P-N junction, as highlighted in Fig 5. Under the application of a negative bias across the drain-source contacts, this body diode can be made to conduct current. This can be beneficial in sustaining reverse conduction in power converter circuits. The physics of this process is similar to that of P-i-N rectifiers.

1.4.1.3. MOSFET parasitics

Semiconductor junctions are created due to differently doped regions in a substrate. Hence, every semiconductor junction can be associated with an equivalent capacitance[41]. In the power

MOSFET, the presence of a capacitive MOS gate adds another capacitor. These equivalent capacitors are shown in Figure 1.6. These capacitances are evaluated using standard characterization tests[42]. Figure 1.7. shows a typical plot of parasitic capacitances across a range of drain-source bias voltages.

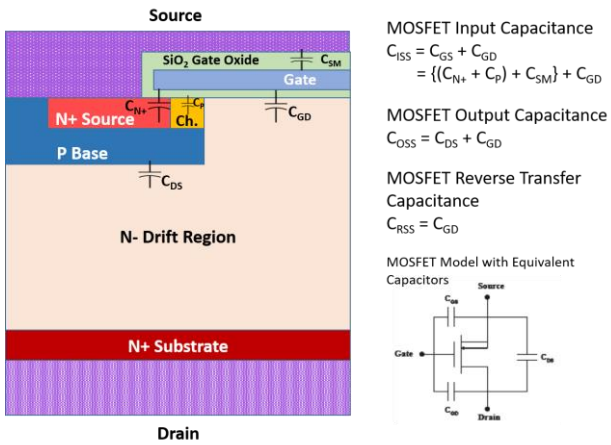


Figure 1.6. SiC MOSFET parasitic capacitances with expressions for equivalent capacitors.

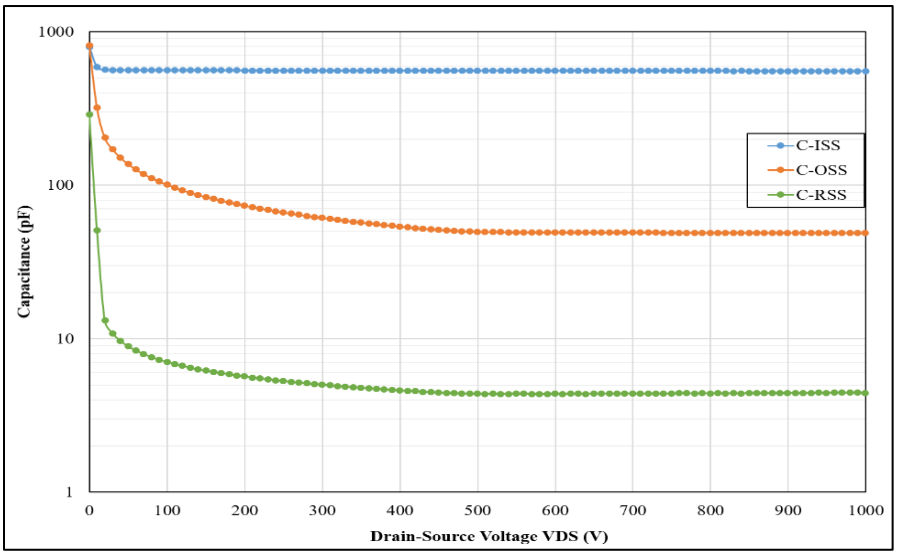


Figure 1.7. MOSFET parasitic Capacitances as a function of V_{DS}.

MOSFET parasitic capacitances vary with the drain source voltage applied across the device. This influences switching behavior in the form of delays during turn-on and turn-off

transitions. The influence of parasitic device capacitances is clearly explained through the example of a clamped inductive load switching circuit[10]. Assuming a set DC bus voltage, the inductor load current freewheels through the clamper diode. When a gate pulse signal is given to the MOSFET, it turns on and the load current commutates from the diode to the MOSFET. At the negative edge of the gate pulse, the MOSFET turns off and the current commutates back to the diode. Figure 1.8. illustrates the turn-on transients of a power MOSFET along with the associated processes involved.

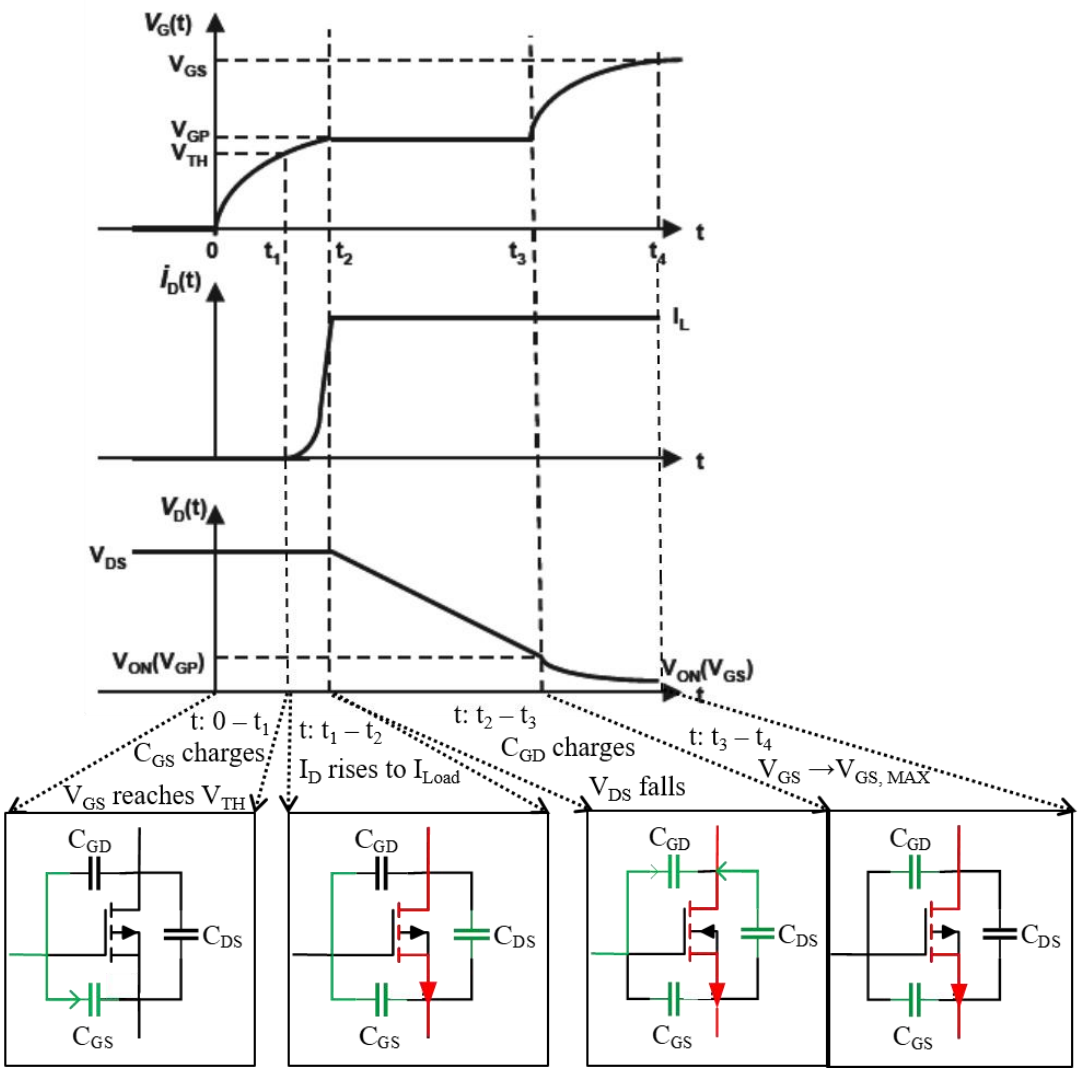


Figure 1.8. Power MOSFET Turn-on transient.

Figure 1.9. shows the turn-off transients for the power MOSFET along with its associated processes. It can be seen that ideally, the turn-on and turn-off processes are symmetrical to each other. The gate-drain capacitance, which is charged or discharged during the plateau region of either transient, is also called the Miller capacitance. The parasitic capacitances of a power MOSFET are the limiting factor determining its maximum operating frequency.

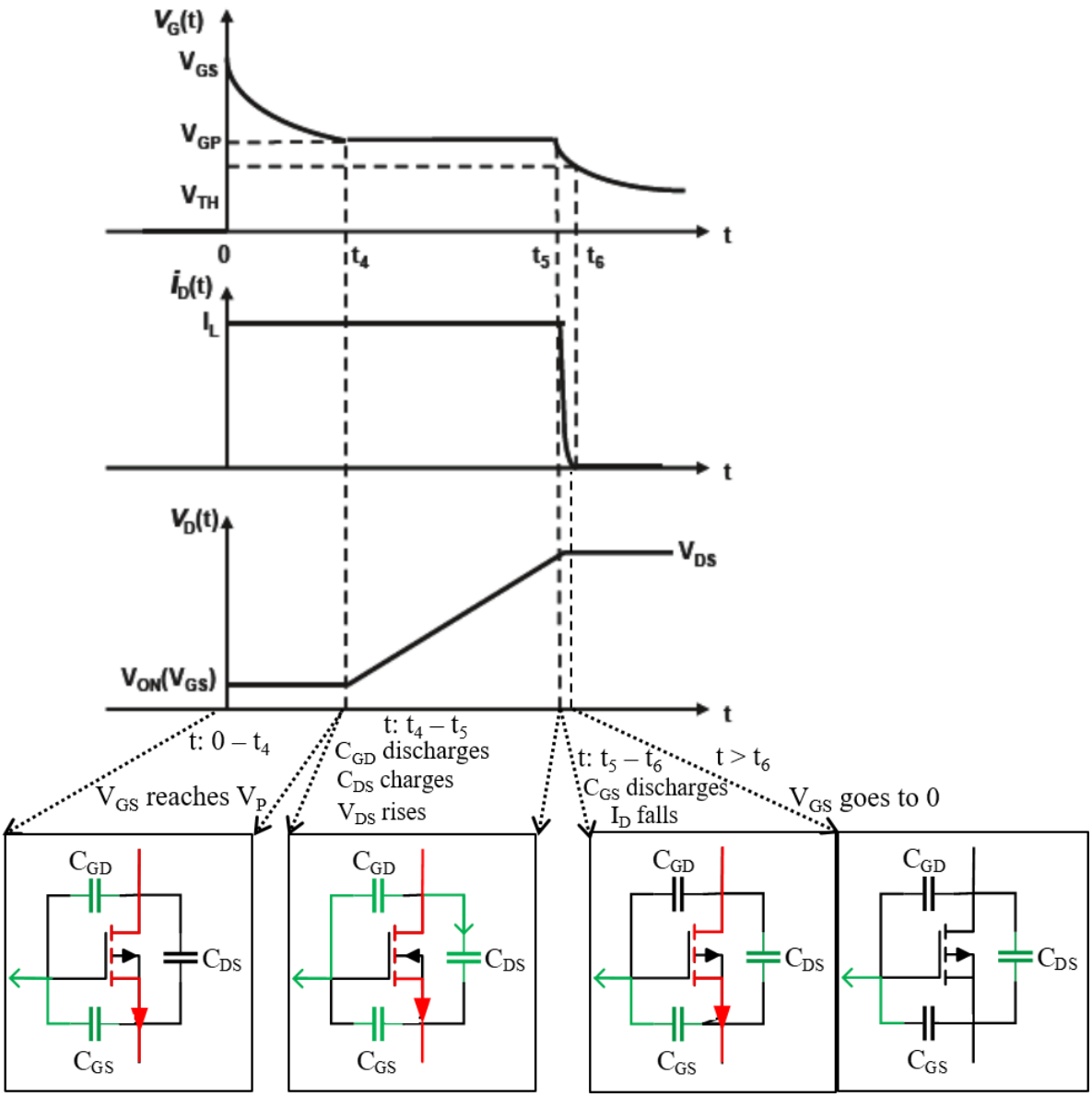


Figure 1.9. Power MOSFET Turn-Off Transient.

1.4.2 The SiC JBSFET

The SiC JBSFET is a monolithic integration of the JBS diode structure into a power MOSFET. SiC JBS rectifiers are typically used in antiparallel connection to SiC MOSFETs in power converter systems. This is done to eliminate the switching loss occurring due to third quadrant operation of the MOSFET[43]. The MOSFET body diode, being a p-n junction device, causes large losses due to reverse recovery current. Figure 1.10. shows the structure of a JBSFET. The JBSFET is functionally similar to a MOSFET except for its third quadrant behaviour, which is similar to the JBS rectifier.

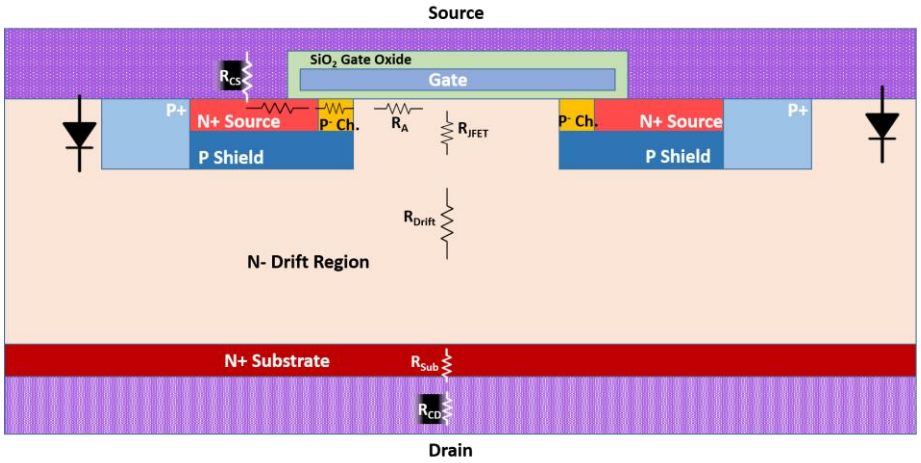


Figure 1.10. The SiC JBSFET Full Cell View.

The SiC MOSFET and SiC JBSFET structures are compared in some detail in the subsequent chapters, with explanations of the underlying physics.

1.5. Device Design, Fabrication and Testing

The devices discussed in this thesis are 1.2kV SiC FETs designed under the PowerAmerica Institute at the North Carolina State University[44]. Both devices are fabricated using the PRESiCE[28] process. These designs will be henceforth referred to as the PA (SiC) MOSFET and PA (SiC) JBSFET. Figure 1.11. and Figure 1.12. show the structure of the PA devices with relevant dimensions included.

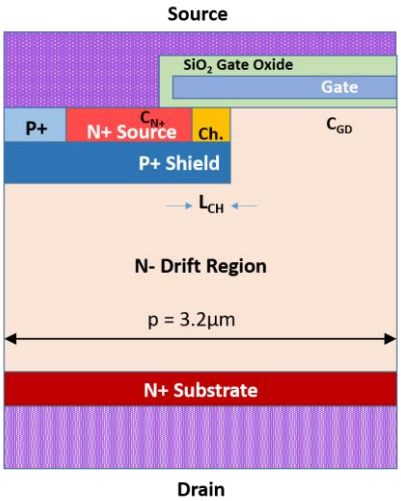


Figure 1.11. SiC MOSFET Structure with dimensions.

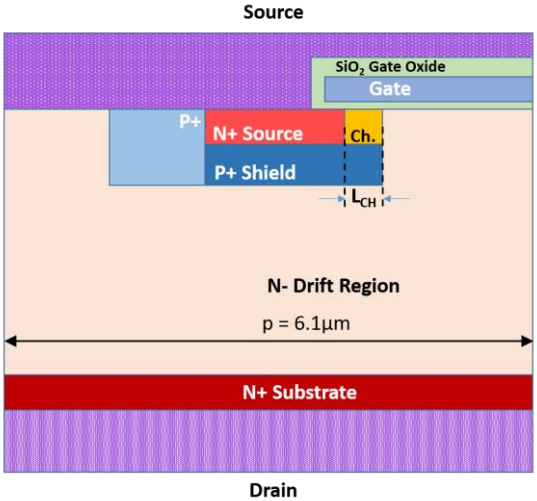


Figure 1.12. SiC JBSFET Structure with dimensions.

The devices are both built on a 360µm SiC substrate with a 10µm thick epitaxially grown drift layer. The doping of the drift layer is set to $8x10^{15}$ cm^{-3}. The P-base and N+-source structures are created by ion-implantation, with a doping of $5x10^{16}$ cm^{-3} and $1\text{-}2x10^{19}$ cm^{-3}, respectively. The devices were fabricated at the 6-inch SiC foundry at X-FAB, Lubbock, TX. Both devices were created with a 0.5µm channel length and the same chip active area of $0.045cm^2$. The MOSFET had a half-cell pitch of 3.2µm, while the JBSFET had a half-cell pitch of 6.1µm. The devices had similar hybrid-JTE[45] edge termination.

Figure 1.13. TO-3 package used for the PowerAmerica devices.

Figure 1.14. Encapsulated TO-3 case after packaging.

The SiC wafer was diced and subsequently, the devices were packaged in TO-3 cases at the NCSU PREES Lab[46].

Figure 1.13. and Figure 1.14. show the TO-3 packaging before and after the encapsulation process. Figure 1.13. also shows the wire-bonding used to attach the device to the package. The packaged devices were subjected to static and dynamic characterization. Eventually, they were characterized for their SC energy. The next three chapters explain the results of the characterization tests.

1.6. References

1. B. K. Bose, "***Evaluation of modern power semiconductor devices and future trend of converters***", Industry Applications Society Annual Meeting, IEEE, 1989
2. B. K. Bose, "***Power Electronics – A technology review***", Proceedings of the IEEE, vol. 80, no, 8, pp. 1303-1334, 1992
3. M. S. Adler, "***The Evolution of Power Device Technology***", IEEE Transactions on Electron Devices, Vol ED-31 (11), pp.1570-1591, 1984
4. J. Bardeen and W.H. Brattain, "***The transistor, A semi-conductor triode***", Physical Review Letters, vol 74, no. 2, pp. 230-231, 1948
5. U.S. Patent 2569347, issued Sept. 25, 1951
6. B. J. Baliga, "***Switching Lots of Watts at high speeds: State-of-the-art development yields solid-state devices capable of handling over 10 million watts***", in IEEE Spectrum, vol 19, no. 12, pp. 42-48, 1981
7. B. J. Baliga, "***Revolutionary Innovations in Power Discrete Devices***", International Electron Devices Meeting, pp. 102-105, IEEE, 1986
8. B. J. Baliga, *"**An Overview of Smart Power Technology**"*, IEEE Transaction on Electron Devices, Vol. 38, no. 7, pp. 1568-1575, 1991
9. B. J. Baliga, *"**Trends in Power Semiconductor Devices**"*, IEEE Transactions on Electron Devices, Vol. 43, no. 10, pp. 1717-1731, 1996
10. B. J. Baliga, "**Fundamentals of Power Semiconductor Devices**", Springer, NY, 2008, pp. 507-508
11. B. J. Baliga, "***Enhancement and depletion mode vertical-channel MOS-gated thyristors***", Electronics Letters, vol. 15, no. 20. pp. 645-647, 1979
12. B. J. Baliga, M. S. Adler, R. P. Love, P. V. Gray, N. D. Zommer, "***The insulated Gate transistor: A new three-terminal MOS-controlled bipolar power device***", IEEE Transactions on Electron Devices, vol. ED-31, no. 6, pp. 821-828, 1984
13. B. J. Baliga, "***MOS Devices for Power Electronic Applications***", 28th European Solid-State Device Research Conference, pp. 81-87, 1998
14. B. J. Baliga, "***The future of power semiconductor device technology***", in Proceedings of the IEEE, vol. 89, no. 6, pp. 822-832, 2001
15. B. K. Bose, "***Power Electronics and Motor Drives – Recent Progress and Perspective***", IEEE Transactions on Industrial Electronics, vol. 56, no. 2, pp. 581 – 588, 2009
16. B. J. Baliga, "***Semiconductors for high-voltage, vertical channel field-effect transistors***", Journal of Applied Physics, vol. 53, no. 3, pp. 1759-1764, 1982

17. K. Shenai, R. S. Scott, B. J. Baliga, "***Optimum Semiconductors for high-power electronics***", IEEE Transactions on Electron Devices, vol. 36, no. 9, pp. 1811-1823, 1989

18. L. Tolbert, B. Ozpineci, S. K. Islam, M. S. Chinthavali, "***Wide bandgap semiconductors for utility applications***", pp. 1-5, 2003

19. R. G. Rodrigues, D. E. Piccone, W. H. Tobin, L. W. Willinger, J. A. Barrow, T. A. Hansen, J. Zhao, L. Cao, "***Operation of power semiconductors at their thermal limit***", Conference Record of the IEEE Industry Applications Conference, Thirty-third IAS Annual Meeting, vol. 2, pp. 942-953, 1998

20. J. L. Hudgins, G. S. Simin, E. Santi, M. A. Khan, "***An Assessment of wide bandgap semiconductors for power devices***", IEEE Transactions on Power Electronics, vol. 18, no. 3, pp. 907-914, 2003

21. K. Shenai, P. G. Neudeck, M. Dudley, R. F. Davis, "***High-power switching in semiconductors – What is beyond Silicon Thyristor?***", IEEE EnergyTech, pp. 1-6, 2011

22. B. J. Baliga, "**Gallium Nitride and Silicon Carbide Power Devices**", World Scientific, New Jersey, 2017

23. B. J. Baliga, "***Silicon Carbide Power Devices: A 35-year journey from conception to commercialization***", 76th Device Research Conference, pp. 1-2, 2018

24. D. Garrido-Diez, I. Baraia, "***Review of wide bandgap materials and their impact in new power devices***", IEEE International Workshop of Electronics, Control, Measurement, Signals and their Application to Mechatronics, pp. 1-6, 2017

25. H. A. Mantooth, M. D. Glover, P. Shepherd, "***Wide bandgap technologies and their implications on miniaturizing power electronic systems***", IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 2, no. 3, pp. 374-385, 2014

26. X. She, A. Q. Huang, O. Lucia, B. Ozpineci, "***Review of Silicon Carbide power devices and their applications***", IEEE Transactions on Industrial Electronics, vol. 64, no. 10, pp. 8193-8205, 2017

27. A. Stefanskyi, L. Starzak, A. Napieralski, "***Silicon Carbide power electronics for electric vehicles***", Conference record of the tenth International Conference on Ecological Vehicles and Renewable Energies, pp. 1-9, 2015

28. B. J. Baliga, W. Sung, K. Han, J. L. Harmon, A. Tucker, S. Syed, "***PRESiCE: Process Engineering for manufacturing SiC Electronic devices***", Proceedings of the 2017 International Conference on Silicon Carbide and Related Materials, Materials Science Forum, vol. 924, pp. 523-526, 2017

29. Wolfspeed SiC product portfolio, https://www.wolfspeed.com/power/products

30. Littelfuse SiC product portfolio, https://www.littelfuse.com/products/power-semiconductors/silicon-carbide.aspx

31. Infineon SiC technologies, https://www.infineon.com/cms/en/product/power/wide-band-gap-semiconductors-sic-gan/silicon-carbide-sic/

32. ST Silicon Carbide MOSFETs, https://www.st.com/content/st_com/en/products/power-transistors/wide-bandgap-transistors.html

33. Rohm SiC device portfolio, https://www.rohm.com/sic

34. United SiC product portfolio, https://unitedsic.com/products/

35. GeneSiC Semiconductor SiC transistors, http://www.genesicsemi.com/sic-transistors/

36. C. D. Brown, B. Sarlioglu, "***Reducing Switching Losses in BLDC motor drives by reducing body diode conduction of MOSFETs***", IEEE Transactions on Industry Applications, vol. 51, no. 2, pp. 1864-1871, 2015

37. M. Uchida, N. Horikawa, K. Tanaka, K. Takahashi, T. Kiyosawa, M. Hayashi, M. Niwayama, O. Kusumoto, K. Adachi, C. Kudou, M. Kitabake, "***Novel SiC Power MOSFET with integrated unipolar internal inverse MOS-channel diode***", 2011 International Electron Devices Meeting, pp. 26.6.1-26.6.4, 2011

38. R. Radhakrishnan, J. H. Zhao, "***Monolithic Integration of a 4H-Silicon Carbide Vertical JFET and a JBS Diode***", IEEE Electron Device Letters, vol. 32, no. 6, pp. 785-787, 2011

39. W. Sung, B. J. Baliga, "***On Developing One-chip integration of 1.2kV SiC MOSFET and JBS Diode (JBSFET)***", IEEE Transactions on Industrial Electronics, vol. 64, no. 10, pp. 8206-8212, 2017

40. B. J. Baliga, "***Silicon Carbide Semiconductor Devices having Buried Silicon Carbide Conduction Barrier Layers Therein***", U.S. Patent 5,543.637, Issued August 6, 1996

41. S. M. Sze, K. K. Ng, "**Physics of Semiconductor Devices**", 3rd Ed., Wiley Interscience, New Jersey, 2007

42. "**Measurement of Small Values of Transistor Capacitance**", JEDEC Standard JEDC398, July 1972

43. S. Bontemps, A. Basler, P. Doumerge, "***Evaluation of the need for SiC SBD in parallel with SiC MOSFETs in a module phase leg configuration***", Proceedings of PCIM Europe, pp. 1074-1080, 2015

44. Power America Institute, https://poweramericainstitute.org/about-poweramerica/

45. W. Sung, B. J. Baliga, "***A Near Ideal Edge Termination Technique for 4500V 4H-SiC devices: The hybrid Junction Termination Extension***", IEEE Electron Device Letters, vol. 37, No. 12, pp. 1609-1612, 2016

46. Packaging Research in Electronics Energy Systems, http://prees.org/

CHAPTER 2

THE SIC MOSFET VS SIC JBSFET - STATIC ELECTRICAL CHARACTERISTICS

Static characterization tests are the standard means to extract datasheet parameters and voltage ratings for electronic devices. For power MOSFETs, these comprise of forward and reverse I-V curves, threshold voltage and leakage current studies[1,2]. Device capacitances are also measured as part of the basic characterization exercise. Each of these tests is conducted with the aim of extracting or observing a particular parameter. This chapter explains the testing methodology and the tests itself. The chapter concludes with a comparison of the static parameters of the SiC MOSFET and JBSFET.

2.1. Test Methodology

Static characterization is conducted using the Keysight B1505 Curve Tracer. This test setup has modules equipped with fixtures supporting devices of TO-247 or TO-3 packages. An I-V tester module is used to conduct forward and reverse characterization, threshold voltage measurements, third quadrant operation studies, and breakdown voltage and leakage current evaluation. A separate fixture is used to measure device parasitic capacitances. The curve tracer has configurable settings for either module to conduct the different tests mentioned above. Each of these tests will be described in this chapter in the subsequent sections. Figure 2.1. shows the curve tracer with the modules for I-V and capacitance test.

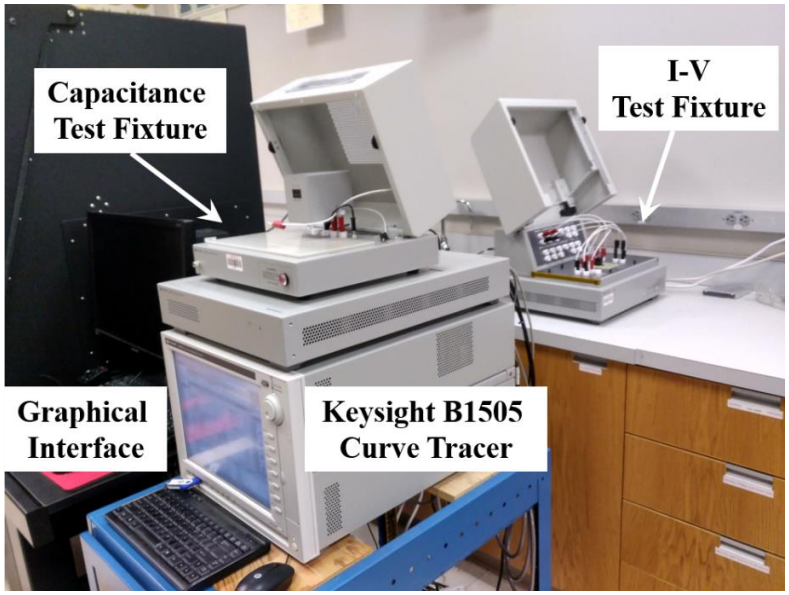


Figure 2.1. Keysight Curve Tracer B1505 with attached modules for I-V and Capacitance Tests.

2.2. Forward Characterization

In this study, forward characterization is used to evaluate the on-resistance of a power device. For a power MOSFET, this test is conducted by turning the device on at different levels of gate bias. Ideally, forward characterization is done to observe the MOSFET transition from active mode to saturation mode at different gate bias voltages. However, automated testers typically set a limit to the maximum power being consumed by the device, and to minimize device heating. As a result, automated testers may not be able to show device saturation at all gate voltages during forward characterization.

The JEDEC standard circuit for a forward I-V characterization is shown in Figure 2.2.

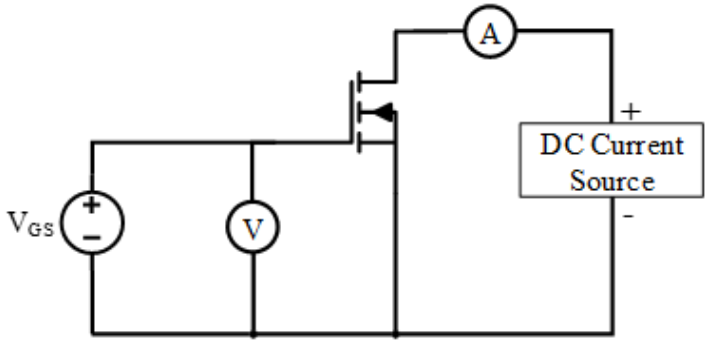


Figure 2.2. Forward I-V characterization test Circuit.

Figure 2.3. shows the I-V curves for a CREE 2nd Generation MOSFET C2M0160120D[3] measured using the curve tracer.

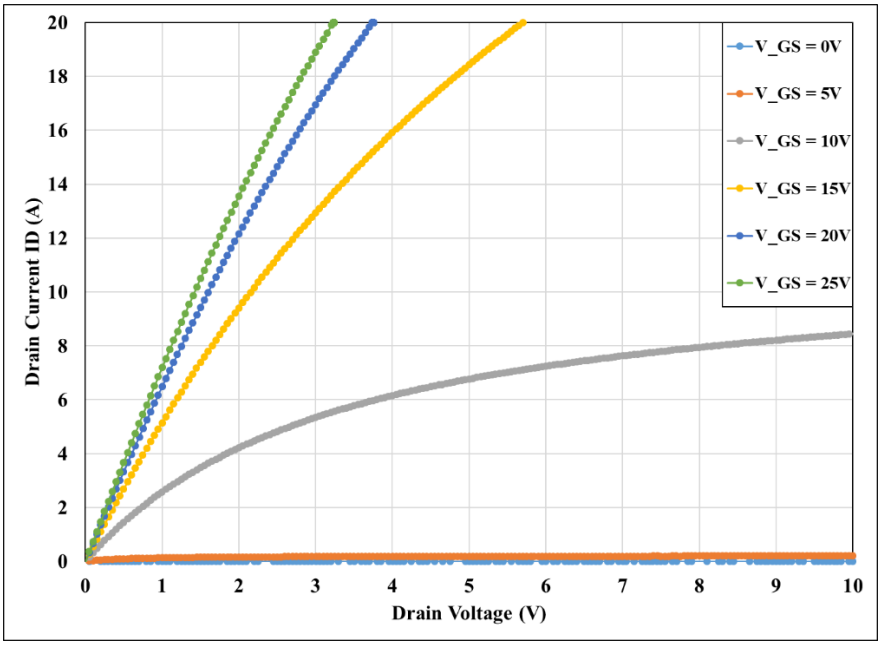


Figure 2.3. Forward Characteristics of a CREE C2M0160120D MOSFET.

The on-resistance of power MOSFETs can be extracted from the forward characteristics by evaluating as the ratio of the drain bias to the forward current at the chosen gate bias and current level.

$$R_{On} = \frac{R_{On,Sp}}{A_{Act}} = \left.\frac{V_{DS}}{I_D}\right|_{V_{GS},I_{ON}} \tag{2-1}$$

In (2-1), A_{Act} is the active area on the transistor chip, $R_{On,Sp}$ is the specific on-resistance of the device, V_{DS} is the drain bias supplied to the device (assuming the source is grounded), and I_D is the drain current, also called the forward current of the device.

For purposes of forward characterization, the PA devices were given gate bias voltages of 0, 5, 10, 15, 20 and 25 volt. The drain bias was increased from 0 to 10V for each gate bias. The test would truncate either when the device voltage reached 10V or when its forward current

reached the curve tracer limit of 20A. The forward I-V curves for the PA MOSFET are shown in Figure 2.4.

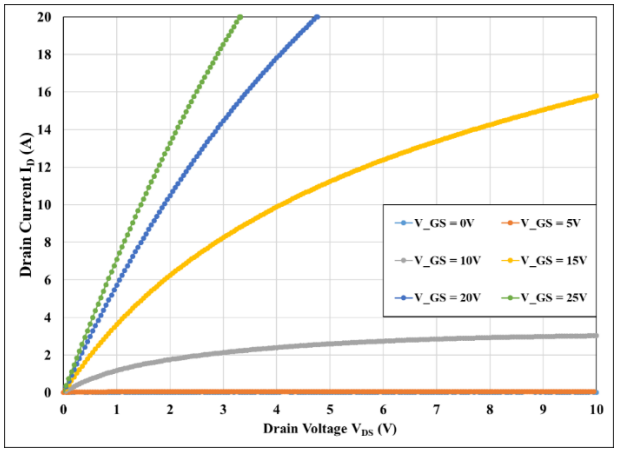


Figure 2.4. Forward I-V Curves for the PA SiC MOSFET.

The forward I-V curves for the PA JBSFET are shown in Figure 2.5. It appears that the JBSFET has a smaller drain saturation current for a given gate bias, when compared to the PA MOSFET.

On-resistance can be measured at any desired value of gate bias and drain current[3,4,5]. To keep the assessment as close as possible to industrial metric, the on-resistance of the PA devices was extracted at a gate bias of 20 V for a forward current of 10A, similar to some commercial device datasheets.

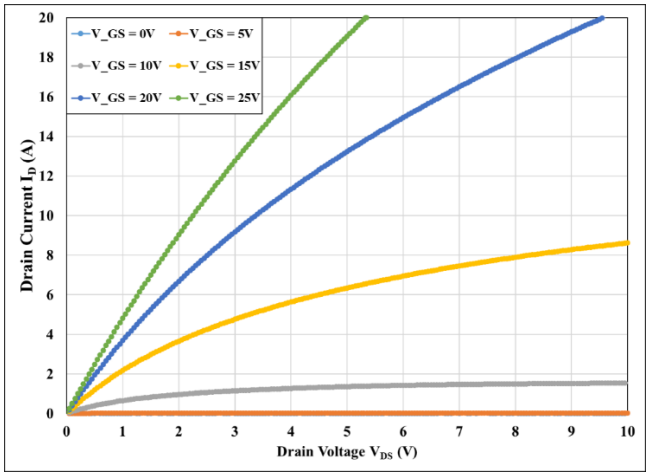


Figure 2.5. Forward I-V Curves for the PA SiC JBSFET.

Table 2.1. shows the on-resistance for the PA SiC MOSFET and JBSFET devices. It follows that the PA JBSFET has a higher on resistance than the PA MOSFET device.

Table 2.1. On-resistance of PowerAmerica SiC Devices.

Device	Conditions	R_{On} (mΩ)	Active Area (cm^2)	$R_{On,Sp}$ (mΩ-cm^2)
PA SiC MOSFET	V_{DS} = 20V, I_D = 10A	189.1	0.045	8.5
PA SiC JBSFET	V_{DS} = 20V, I_D = 10A	337.5	0.045	15.2

Discussion

SiC transistor on-resistance can be expressed as[6]

$$R_{On} = R_{CH} + R_A + R_{JFET} + R_D + R_{subs} \tag{2-2}$$

where R_{CH} is the channel resistance, R_A is the accumulation resistance, R_{JFET} is the resistance due to the JFET region, R_D is the drift region, and R_{subs} is the substrate resistance.

Based on analytical model described in [6], it can be said that the channel resistance is the most prominent contributor to on-resistance. This is due to the poorer channel mobility in SiC compared to Si. Channel resistance can be expressed as

$$R_{CH} = \frac{L_{CH}p}{\mu_{inv}C_{OX}(V_G - V_T)} \tag{2-3}$$

where L_{CH} is the channel length, p is the half-cell pitch, μ_{inv} is the inversion mobility in SiC, C_{OX} is the gate oxide capacitance, V_G is the gate bias and V_T is the threshold voltage.

It is seen that the device on-resistance is proportional to cell pitch. From the design of the PA devices described in Chapter 1, the JBSFET, due to its larger cell pitch, can be expected to have a larger on-resistance.

Table 2.2. Verification of R_{ON} proportionality to cell pitch.

Device	R_{ON} (mΩ)	Half-Cell Pitch, p (μm)	**Ratio (R_{ON}/p)**
PA MOSFET	189.1	3.2	**59**
PA JBSFET	337.5	6.1	**55.33**
Ratio (MOSFET/JBSFET)	**0.56**	**0.52**	

The PA devices follow the expected proportionality of on-resistance and cell pitch.

2.3. Threshold Voltage

Threshold voltage is defined as the minimum gate bias required to initiate forward current flow in a MOSFET. Looking into device physics, it is the minimum voltage required to create a channel of majority carriers in the base region of the MOSFET. To characterize power MOSFET threshold voltage, the device is maintained at a small, fixed drain bias, while the gate bias is steadily ramped until the forward current exceeds a pre-set value.

For this study, the threshold voltage is measured at a drain bias of 0.1V, and is defined as the gate bias for a forward current of 1 mA.

The same test can be used to measure transconductance, G_M, of the power MOSFET. Transconductance is defined as the derivative of the forward current with respect to the gate bias.

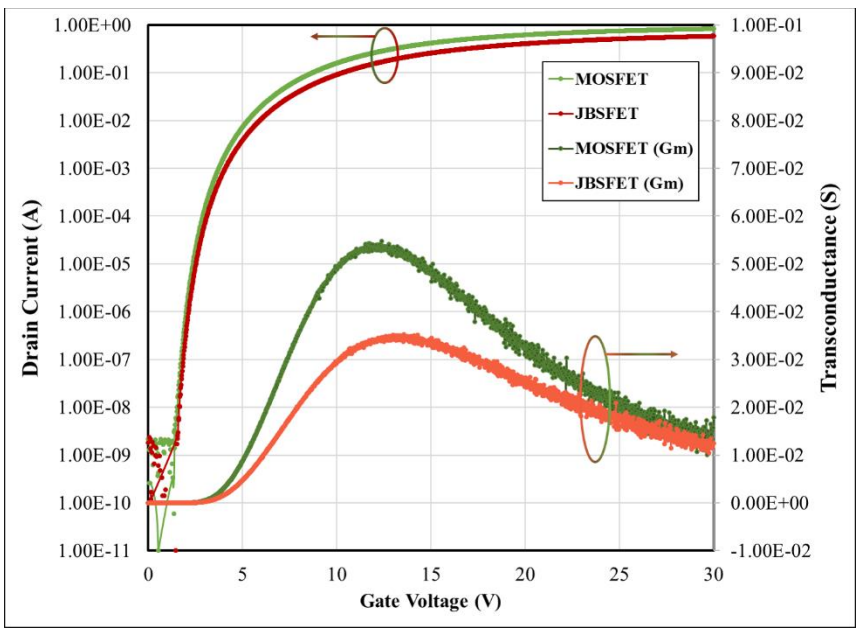


Figure 2.6. Threshold voltage and transconductance curves for the PowerAmerica devices.

Table 2.3. compares the threshold voltages and the transconductance of the SiC MOSFET and JBSFET. It is seen that the PA MOSFET and JBSFET have similar threshold voltages. The transconductance of the devices was measured at a threshold voltage of 3.9V, a point intermediate

to both the MOSFET and JBSFET. The JBSFET is seen to have a smaller transconductance compared to the MOSFET.

Table 2.3. Threshold Voltages for PowerAmerica SiC devices.

Device	Condition	V_{TH} (V)	$G_{M, Max}$ (mS)	1/Cell Pitch, p^{-1} (μm)
(a) SiC MOSFET	I_D = 1mA	3.74	54.8	0.62
(b) SiC JBSFET	I_D = 1mA	4.08	34.8	0.33
Ratio (a)/(b)			1.57	1.91

Discussion

The threshold voltage of the SiC power MOSFET is expressed as[6]

$$V_{TH} = \frac{\sqrt{4\varepsilon_S kTN_A \ln {N_A}/{n_i}}}{C_{OX}} + \frac{2kT}{q}\ln\frac{N_A}{n_i} + \frac{Q_F}{C_{OX}} \tag{2-4}$$

where N_A is the P-base doping, k is the Boltzmann's constant, T, the ambient temperature and Q_F is the interface charge. From the formula, it appears that the only variation between the PA MOSFET and JBSFET would be the fixed interface charges. These are not quantified in a straightforward manner. Hence, it can be expected that the PA devices must have threshold voltages close to each other. The data from Table 2.3. matches this prediction.

The transconductance of a MOSFET varies proportionally to the drain bias and inversely to the cell pitch for low drain bias voltages. For a device active area A and a cell pitch p, the transconductance can be formulated as[7]

$$g_M = \frac{dI_D}{dV_G} = \frac{A_{Act}\mu_{ni}C_{OX}}{pL_{CH}}V_D$$

It is seen that the transconductance of the PA MOSFET has a higher value than that of the PA JBSFET, which follows the trend predicted by the inverse ratio of their cell pitch.

2.4. Reverse Conduction, or Third Quadrant Operation

Power MOSFETs have an integral body diode in their structure, as shown in Figure 1.5. The presence of this diode allows flow of current in the reverse direction. This is particularly

beneficial in inverter applications. The body diode is a P-i-N rectifier. Hence, using reverse conduction through the body diode leads to space charge storage in the drift region, causing reverse recovery currents. These exhibit themselves as a current overshoot during switching, and result in increased switching power loss. This phenomenon is studied in detail in Chapter 3.

For characterization purposes, the MOSFET is subject to reverse voltage without a gate bias. This creates a reverse current flow through the body diode.

The JBSFET, by definition, has an integrated JBS diode in its structure. This causes a reverse current to spread out below the P-base corner[8]. This, in turn, raises the potential at the cathode and thus, indirectly reducing the potential across the P-N diode. The MOSFET P-N body diode does not turn-on as long as the bias across it is less than the built-in potential of the P-N junction.

Figure 2.7. shows a comparative plot of the reverse current flow in the PA MOSFET and PA JBSFET devices.

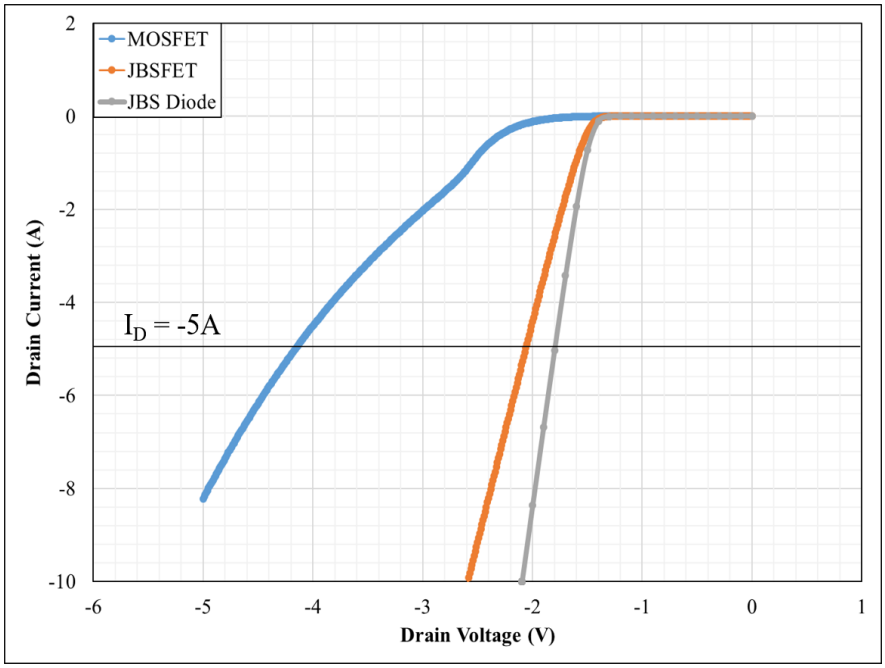


Figure 2.7. 3rd Quadrant Operation of PowerAmerica Devices.

Discussion

From the explanation given above, it follows that the JBSFET third quadrant operation must be similar to an inverted forward I-V curve of a JBS diode. This difference is clearly seen in Figure 2.7., which corroborates the theory. A similar observation is made in [9]. The device used to obtain the reference JBS diode curve in Figure 2.7. was taken from the same wafer as the PA MOSFET and JBSFET. This device was designed similar to the integrated JBS diode in the JBSFET . The P^+-well and cell-width of this JBS diode were twice as wide as the P^+-well and cell width of the integrated JBS diode.

2.5. Breakdown Voltage

Breakdown voltage is the blocking potential at the onset of impact-ionization-induced avalanche current. This is the absolute maximum voltage that the device can block in the forward direction. The blocking voltage is a function of drift region doping and edge termination design. A well-designed edge termination is one with a higher critical electric field of breakdown compared to the active area within the cell.

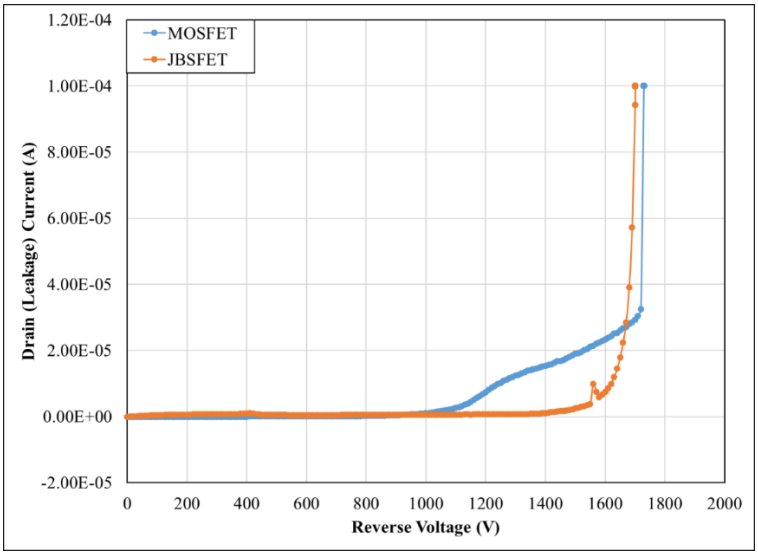


Figure 2.8. Breakdown Voltage Test of PowerAmerica Devices.

For characterizing power MOSFET breakdown voltage, the device is subjected to an increasing drain-source voltage, while keeping the gate potential at zero. The test is conducted until the leakage current exceeds a preset limit. For this work, the leakage current limit to measure breakdown voltage is set at 100µA. Figure 2.8. shows the breakdown voltage curve for the PA SiC MOSFET and PA SiC JBSFET.

The only difference between the devices is the presence of an embedded JBS Diode in the JBSFET. Hence, their breakdown voltage tests must be identical. The result seen in Figure 2.8 meets this expectation – the MOSFET has a BV_{DSS} of 1730V, and the JBSFET, 1700V. Furthermore, it shows that the Schottky Contact, which is typically prone to leakage under extreme stress and reverse bias[6], does not deteriorate the MOSFET structure when monolithically integrated into it.

2.6. Capacitance Measurements

Parasitic capacitances in a power MOSFET were discussed in Chapter 1. The characterizing circuits used to measure power device capacitance are shown below. For the purposes of this study, power device capacitances were measured using the capacitance measurement fixture of the Keysight curve tracer. Figure 2.9, Figure 2.10 and Figure 2.11 display the circuit used to evaluate the device capacitances for the SiC MOSFET and JBSFET.

Capacitance tests are conducted by passing a small amplitude, high frequency AC signal across the gate-source of the device, while sweeping the drain bias. To simplify measurement of the intended capacitance, a large capacitor (~10µF) is placed parallel to the excluded capacitance. The large capacitor creates an AC short and thus eliminates the undesired capacitance from the measurement. Measurement is always made by connecting probes across the gate-source or gate-drain of the device.

To elucidate, when measuring C_{ISS}, a 10µF capacitor is placed parallel to C_{DS}. This creates an AC short and thus removes C_{DS} from the measurement, leaving only C_{GD} and C_{GS} in parallel to be measured..

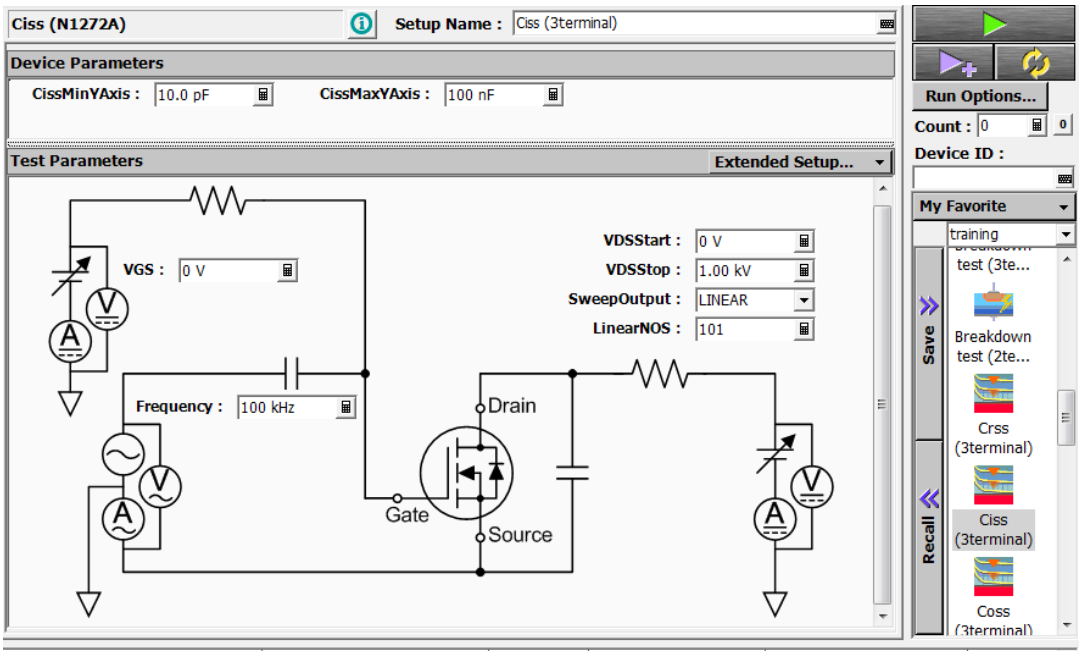


Figure 2.9. CISS test circuit on the Keysight B1505 Curve Tracer.

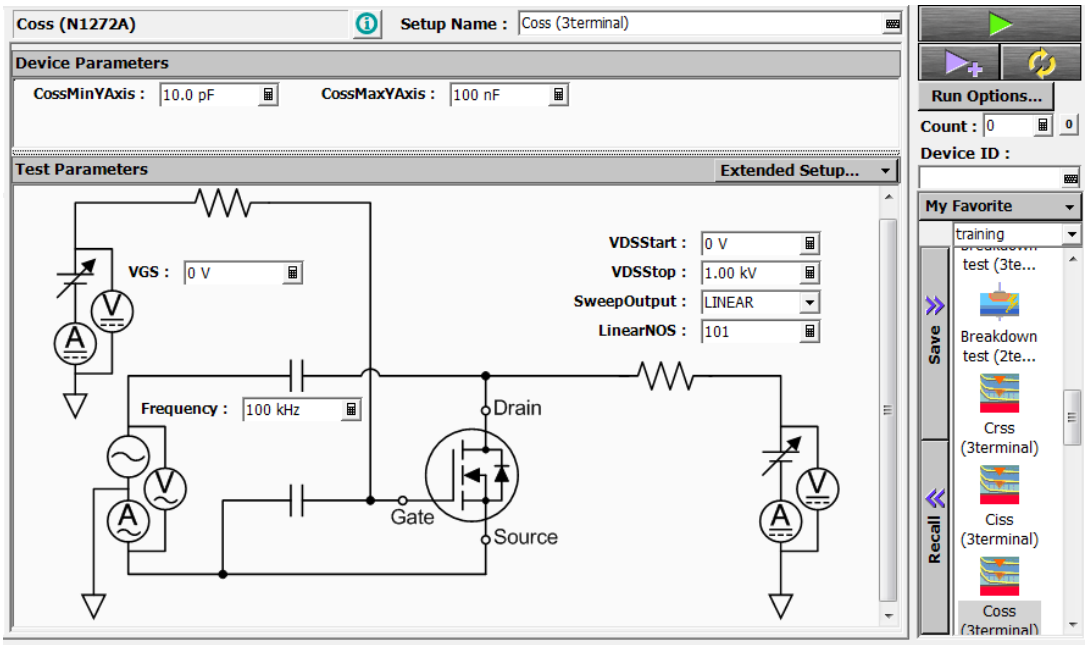


Figure 2.10. COSS test Circuit on the Keysight B1505 Curve Tracer.

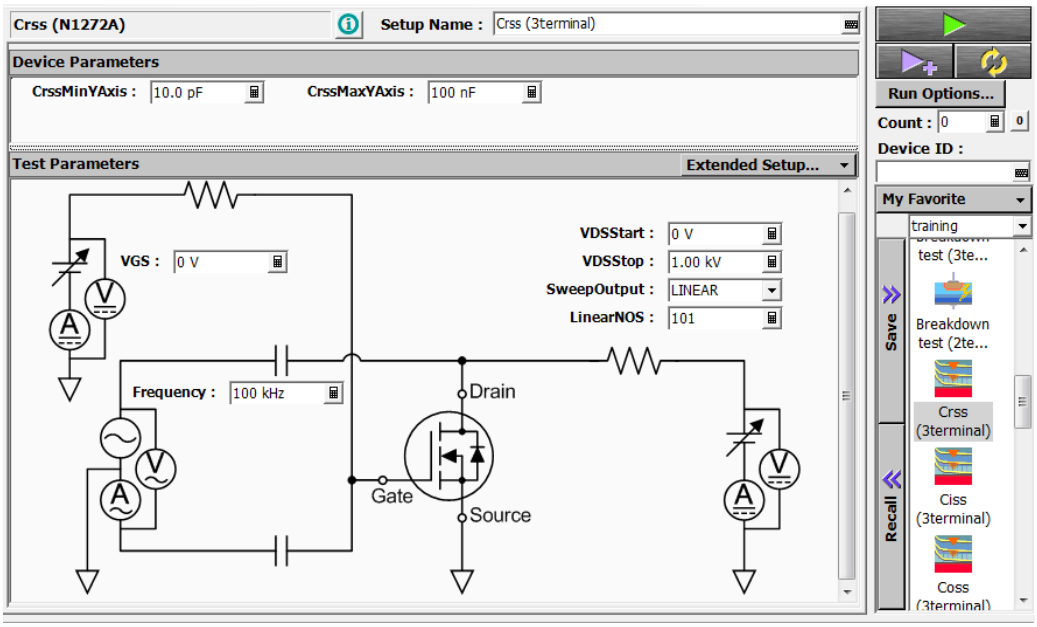


Figure 2.11. CRSS test Circuit on the Keysight B1505 Curve Tracer.

Figure 2.12. shows the comparative waveforms of parasitic device capacitances for the PA MOSFET and PA JBSFET.

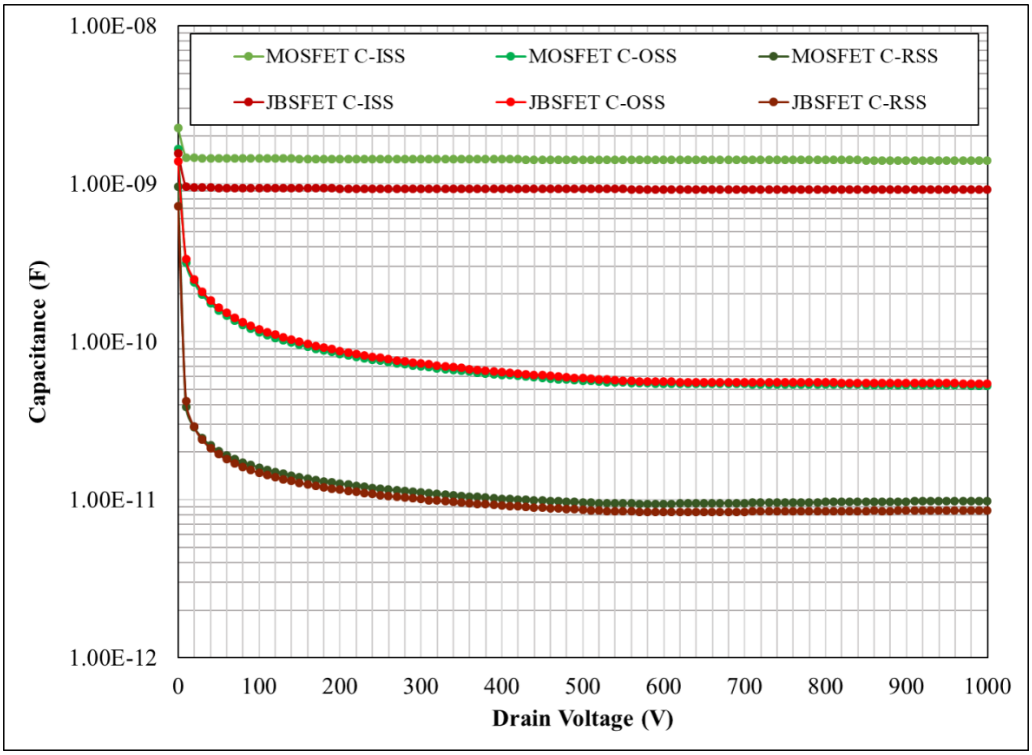


Figure 2.12. Device Capacitances for PowerAmerica Devices.

Table 2.4. lists the parasitic capacitances of the PA MOSFET and PA JBSFET structures.

Table 2.4. Capacitance Test Data for PowerAmerica devices.

Device	Conditions	C_{ISS} (pF)	C_{OSS} (pF)	C_{RSS} (pF)
SiC MOSFET	V_{DS} = 1000V	1402	52.7	9.84
SiC JBSFET	V_{DS} = 1000V	914	54.3	8.58

2.7. Summary

The basic device characteristics were discussed with a view of providing a datasheet-level comparison for the SiC MOSFET and JBSFET structures. SiC power MOSFET on-resistance was found to be a strong function of cell pitch. Hence, the device with the larger cell pitch exhibits a larger on-resistance. The threshold voltage is a function of P-base doping and interface charges in the oxide-semiconductor edge. Hence, similar devices can be expected to have similar threshold voltages – only varying due to interface charge distributions. However, the transconductance of power MOSFETs varies inversely with their cell pitch. Hence, the MOSFET shows a greater transconductance compared to the JBSFET. The MOSFET exhibits a third quadrant behavior similar to that of a reverse P-N diode, whereas the JBSFET resembles a reversed JBS diode, which can be attributed to its monolithically integrated JBS diode. There is no significant difference in the breakdown voltage behaviour of the two devices, which follows expectations, since the two devices have similar edge terminations and drift region doping profiles.

2.8. References

1. V. Barkhordarian, "***Power MOSFET Basics***", Power Conversion and Intelligent Motion – English Edition 22, no. 6, 1996

2. "***Power MOSFET Electrical Characteristics***", Application Note #AN20180726, Toshiba Electronic Devices & Storage Corporation Asia, 2018

3. Datasheet, C2M0160120D, CREE Wolfspeed 2nd Gen. SiC MOSFET, https://www.wolfspeed.com/media/downloads/169/C2M0160120D.pdf

4. "***Power MOSFETs***", JEDEC Standard JESD24, July 1985

5. Datasheet, SCT2160KE, Rohm 2nd Gen. Planar SiC MOSFET, https://www.rohm.com/datasheet/SCT2160KE/sct2160ke-e

6. B. J. Baliga, "***Gallium Nitride and Silicon Carbide Power Devices***", Wiley Interscience, New Jersey, 2017

7. B. J. Baliga, "***Fundamentals of Power Semiconductor Devices***" Springer, NY, 2008

8. K. Kawahara, S. Hino, K. Sadamatsu, Y. Nakao, Y. Yamashiro, Y. Yamamoto, T. Iwamatsu, S. Nakata, S. Tomohisa, S. Yamakawa, "***6.5kV Schottky-Barrier-Diode-Embedded SiC-MOSFET for Compact full-Unipolar Module***", Proceedings of the 29th International Symposium on Power Semiconductor Devices and ICs, pp. 41-44, 2017

9. W. Sung, B. J. Baliga, "***Monolithically Integrated 4H-SiC MOSFET and JBS Diode (JBSFET) using a single Ohmic/Schottky Process Scheme***", IEEE Electron Device Letters, vol. 37, no. 12, pp. 1605-1608, 2016

CHAPTER 3

THE SIC MOSFET VS SIC JBSFET – SWITCHING LOSS STUDIES

One of the major motivations for the development of the SiC JBSFET is its application in inverters, motor drives and photovoltaic systems[1]. In these applications, the DC-to-AC conversion process involves the power switches to conduct current in both directions. It has been shown that a standalone MOSFET is prone to energy loss due to reverse conduction through its P-N body diode. A popular solution to alleviate the loss has been to connect a JBS diode antiparallel to the power MOSFET[2,3]. A JBS diode, by virtue of its unipolar nature of current conduction, does not undergo reverse recovery. This reduces the overall power loss in the converter.

While the addition of a JBS diode reduces the power loss, the packaging bulk increases. The inclusion of the diode also introduces parasitic inductances in the circuit. Hence, a monolithically integrated combination of the JBS diode and MOSFET can be expected to enhance the performance of the system. This chapter explores the dynamic behaviour of the SiC MOSFET and JBSFET by evaluating the switching behaviour of the devices under different test conditions.

3.1. Testing Methodology

Switching tests are conducted by using a clamped inductive load switching circuit, also commonly known as the double pulse test (DPT) circuit. Figure 3.1. shows the schematic of the DPT setup.

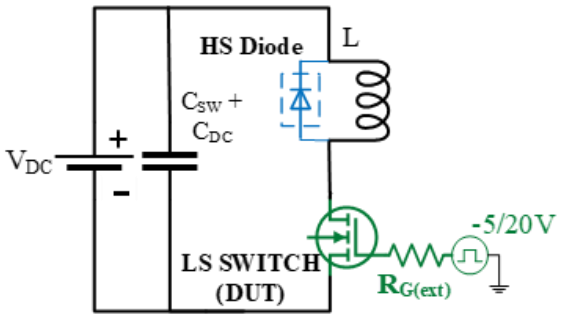


Figure 3.1. Schematic for the Clamped Inductive Load Switching Test.

The power device being evaluated for switching losses is interchangeably called the low-side (LS) switch or device under test (DUT). Similarly, any device connected parallel to the load inductor is called the high-side (HS) device. In the above circuit, the DUT is given two gate pulse signals in succession. The first pulse builds up current in the inductor and enables the evaluation of DUT turn-off behaviour at the set current. During this turn-off, the current built up in the inductor commutates to the freewheeling diode connected across it. The second pulse begins with the DUT turn-on, when the freewheeling current commutates back from diode to the DUT. Hence, the negative edge of the first gate pulse and the positive edge of the second gate pulse are used to compute switching losses.

Standard switching characterizations evaluate the switching performance of a device at room temperature for different gate resistances. However, to comprehensively evaluate the effectiveness of the monolithic integration in the JBSFET, switching tests were conducted in two studies – Switching loss with varying 1. gate resistances; 2. different device combinations, and, junction temperatures. Both these studies will be discussed in detail in this chapter.

3.2. Design of the Circuit

The DPT aims to evaluate DUT switching at a set current. Thus, for a given inductor, the first gate pulse must be wide enough to allow the build up of the set current.

$$t_{pulse} = L\frac{I_D}{V_{DS}} \tag{3-1}$$

In a practical test setup, the high voltage supply is typically not capable of sourcing large currents. Hence, a capacitor bank must be used in parallel with the DC voltage supply to provide the switching current. To compute the size of the switching capacitor bank, the energy to be built up in the inductor can be matched to the energy of the switching capacitor bank.

$$C_{SW} = L\frac{{I_D}^2}{{V_{DC}}^2} \tag{3-2}$$

The DPT circuit, being made of a power loop, has a parasitic resistance which can cause I^2R loss. R, being a parasitic element, may be numerically very small, but when coupled with large currents, it can cause a noticeable change in the power loss graph. As a result, the DC bus voltage in the circuit drops with every successive pulse. To countermand this phenomenon, an additional capacitor is required with the sole purpose of maintaining the DC bus voltage. The energy supplied by this capacitor must exceed any possible I^2R loss due to parasitic resistances in the circuit.

$$C_{DC} \geq \frac{{I_D}^2 R_{parasitic}}{V_{DC}\Delta V_{DC}} \tag{3-3}$$

As seen by the above derivation, it is advisable to select an overrated DC bus capacitor to ensure a stable DC voltage and negligible ΔV_{DC}.

The switching losses of the SiC MOSFET and JBSFET were extracted using a CREE Evaluation Kit 8020-CRD-8FF1217P-1. This multi-purpose circuit board was set up in the DPT configuration with a 350µH inductor. The circuit board has an inbuilt capacitor bank of 25µF. The board is equipped with a gate drive channel which can be configured to supply different gate voltages. The set voltage and current for the DPT was set, respectively, at 800V and 10A. A Tektronix arbitrary function generator AFG3024 was used to provide two gate pulses of -5/20V (low/high level voltages) of 4.3µs width. Figure 3.2. shows the DPT setup used for the studies in this thesis.

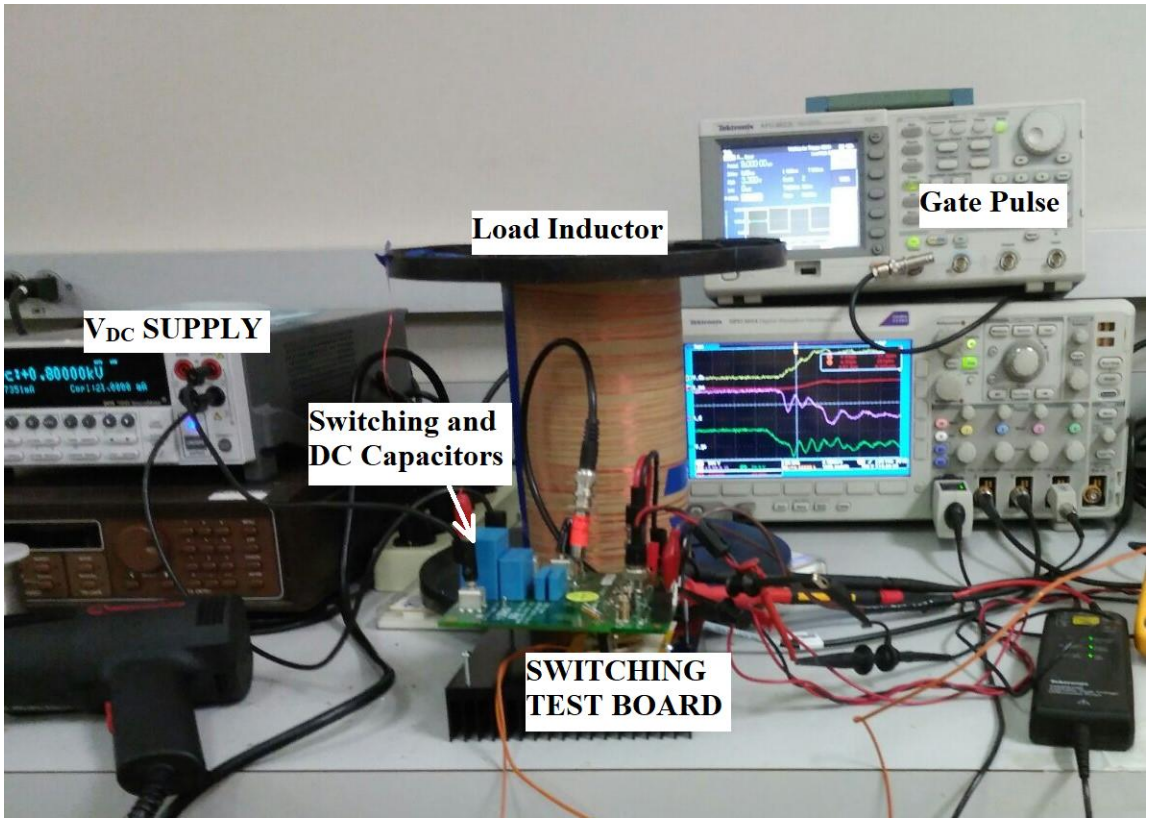


Figure 3.2. Clamped Inductive Load Switching Test Setup.

3.3. Study 1 – Switching Loss vs Gate Resistance

The DUT is connected to the gate drive circuitry through a gate resistance. This resistance, coupled with the DUT input capacitance, influences the gate voltage transient of the device. Hence, evaluating switching losses with different external gate resistances enables close observation of switching behaviour – especially to understand the gate voltage evolution during the switching process.

This study is conducted at room temperature. The different gate resistances used are 2.5Ω, 5 Ω, 10 Ω, 15 Ω and 20 Ω. Figure 3.3. shows a typical switching waveform. This graph was taken for the switching test of the PA SiC MOSFET with a 2.5 Ω external gate resistance.

Switching loss is computed by integrating the product of the drain voltage and drain current from the start of current rise until the end of voltage drop. This is typically seen as a positive 'hill'

in the power graph. This method is used to calculate the energy loss during turn-off and turn-on transients for both the SiC MOSFET and JBSFET, as shown in Figure 3.4. and Figure 3.5. This exercise is repeated for different values of gate resistance to observe the trend followed by the devices. Table 3.1 shows the switching losses for the PowerAmerica devices for different gate resistances, while the same information if plotted in Figure 3.6.

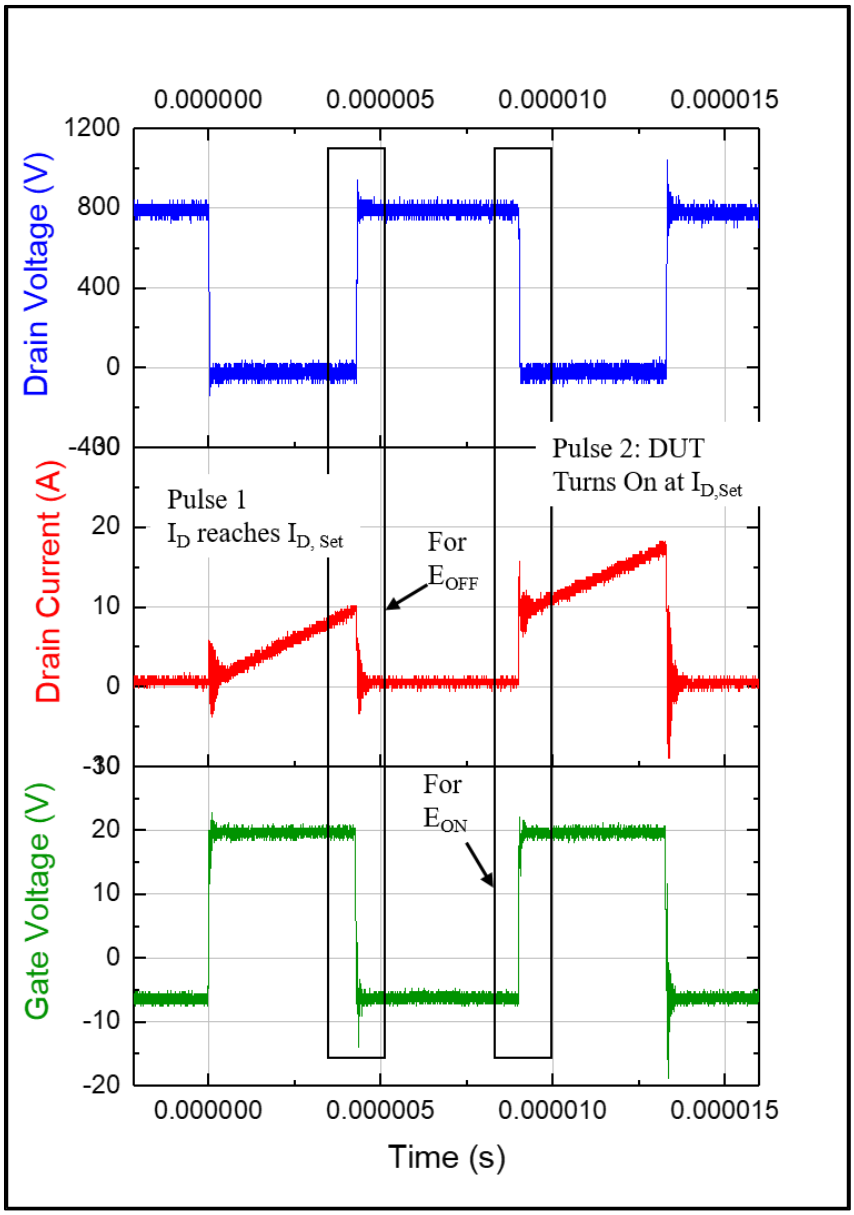


Figure 3.3. Switching waveform for the PA SiC MOSFET ($R_{G,Ext}$ = 2.5 ohm).

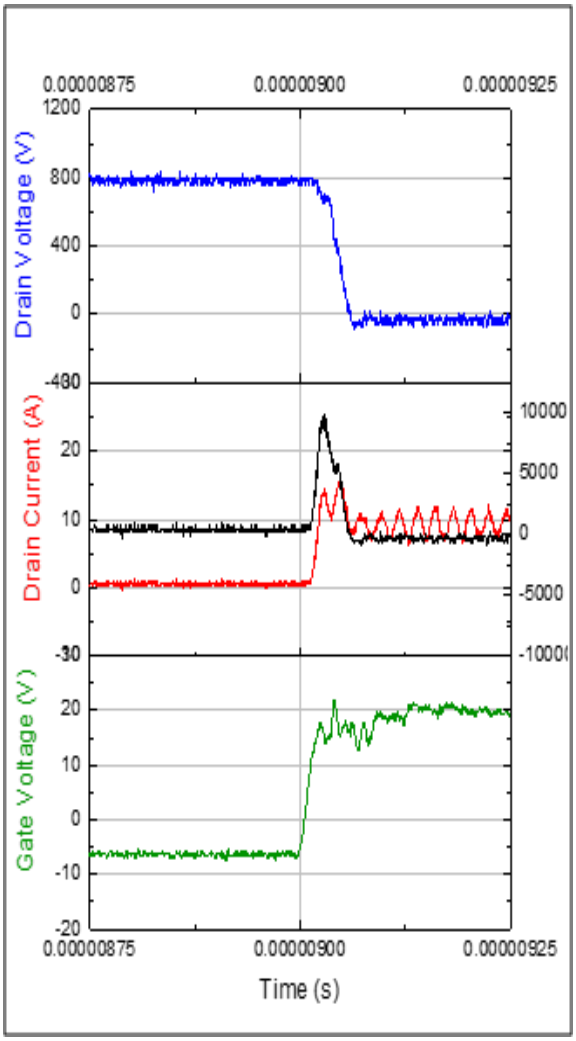


Figure 3.4. PA SiC MOSFET turn-on switching waveform with Power Computation.

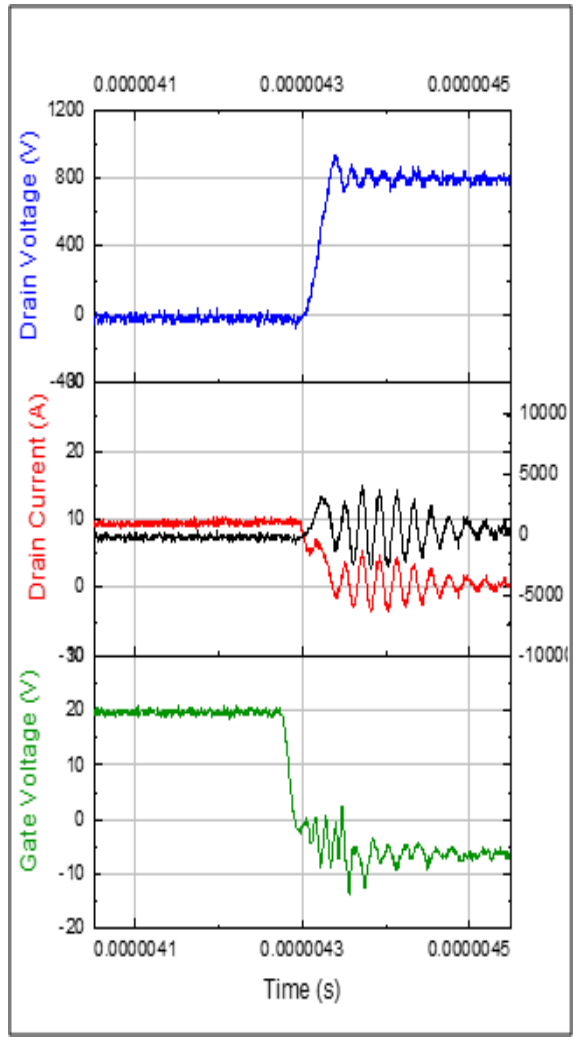


Figure 3.5. PA SiC MOSFET turn-off switching waveform with Power Computation.

Table 3.1. Switching Losses for different Gate resistances.

Transient	Condition	Property	SiC MOSFET	SiC JBSFET	% Difference
Turn-on transient	$R_G = 2.5\Omega$	t_{ON} (ns)	58.3	64.3	
		E_{ON} (μJ)	212	260	22.6
	$R_G = 5\Omega$	t_{ON} (ns)	65.1	77.3	
		E_{ON} (μJ)	257	318	23.7
	$R_G = 10\Omega$	t_{ON} (ns)	77.5	96	
		E_{ON} (μJ)	319	379	18.8
	$R_G = 15\Omega$	t_{ON} (ns)	91	103.6	
		E_{ON} (μJ)	368	436	18.4
	$R_G = 20\Omega$	t_{ON} (ns)	99.3	119.5	
		E_{ON} (μJ)	416	482	15.9

Table 3.1 (continued). Switching Losses for different Gate Resistances.

Turn-off transient	$R_G = 2.5\Omega$	t_{OFF} (ns)	39.6	36.2	
		E_{OFF} (µJ)	71.7	79	10.2
	$R_G = 5\Omega$	t_{OFF} (ns)	41.1	35.3	
		E_{OFF} (µJ)	70	79	12.86
	$R_G = 10\Omega$	t_{OFF} (ns)	39.4	35.9	
		E_{OFF} (µJ)	70	80	14.28
	$R_G = 15\Omega$	t_{OFF} (ns)	39.6	35.4	
		E_{OFF} (µJ)	73.7	80.4	9.1
	$R_G = 20\Omega$	t_{OFF} (ns)	38.4	36.1	
		E_{OFF} (µJ)	71.7	80.6	12.4

It is seen that the JBSFET has a marginally higher turn-on loss compared to the MOSFET. It is also clear that the JBSFET transients are slower than the corresponding transients for the MOSFET. This can be attributed to the lower transconductance of the JBSFET, which, inherently produces a smaller amount of current for a given gate and drain bias. This conjecture requires further data and study to be confirmed.

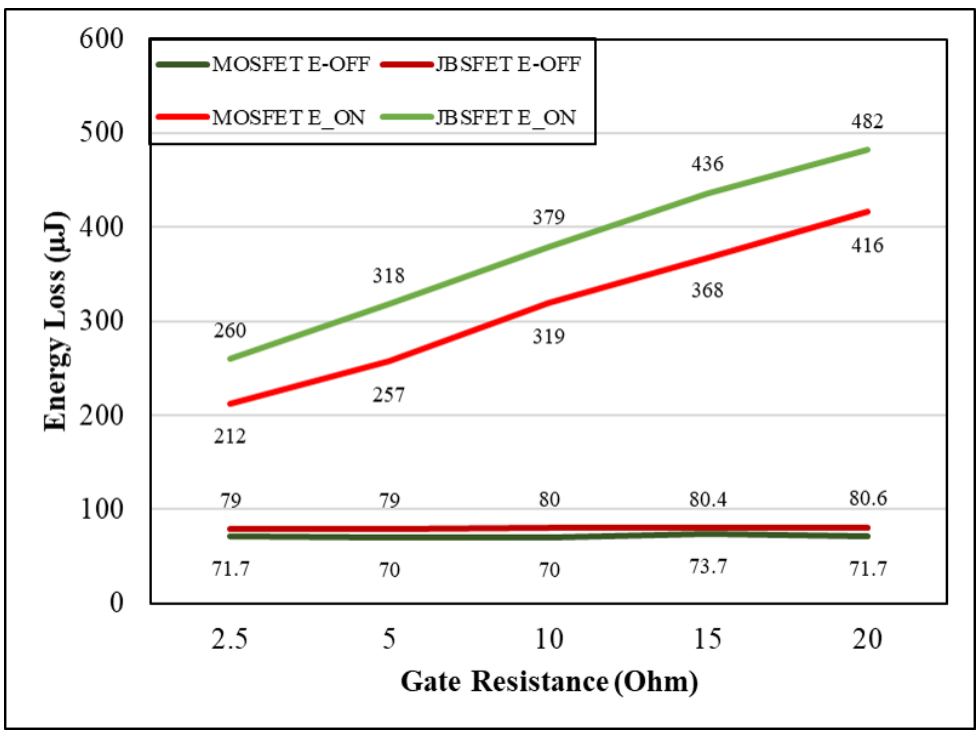


Figure 3.6. Switching Loss comparison for the PowerAmerica MOSFET and JBSFET.

3.4. Study 2 - Switching Loss with Temperature variations

From a standalone comparison, the JBSFET has a higher switching loss compared to the SiC MOSFET. However, in practical applications, when devices are employed in inverters and bridge converters, the MOSFET is commonly placed with an antiparallel-connected Schottky diode[2,3]. Furthermore, given that the JBSFET is a monolithic integration of a JBS diode and a power MOSFET, it is more relevant to compare the switching performance of the JBSFET with a MOSFET-antiparallel-JBS diode combination. To further simplify nomenclature, the freewheeling device connected across the load inductor will be called the high-side (HS) device, while the DUT will be called low-side (LS) device.

In practical applications, the continuous operation and the presence of high-power circuit components leads to internal and external heating in a power device. Hence, as an additional variable, the above study with different combination was done under different junction temperatures. The different combinations tested are –

Case 1: (HS) PA MOSFET/ (LS) PA MOSFET;

Case 2: (HS) PA MOSFET+Antiparallel JBS Diode/ (LS) PA MOSFET

Case 3: (HS) PA JBSFET/ (LS) PA JBSFET

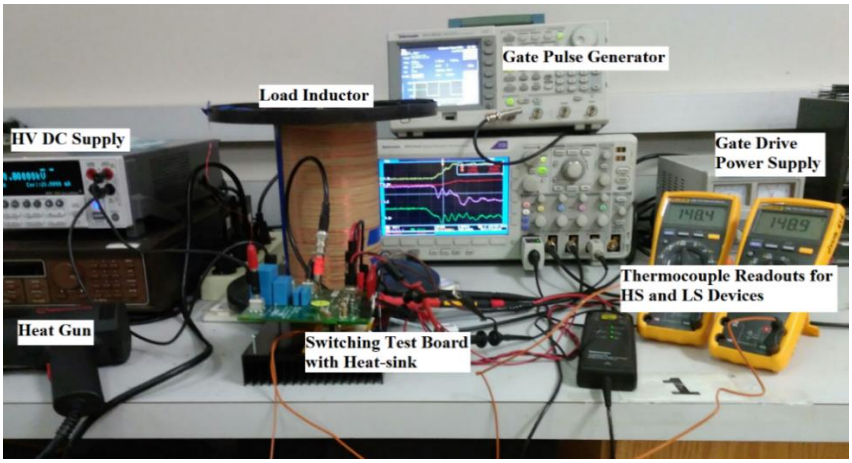


Figure 3.7. High-temperature Switching test setup.

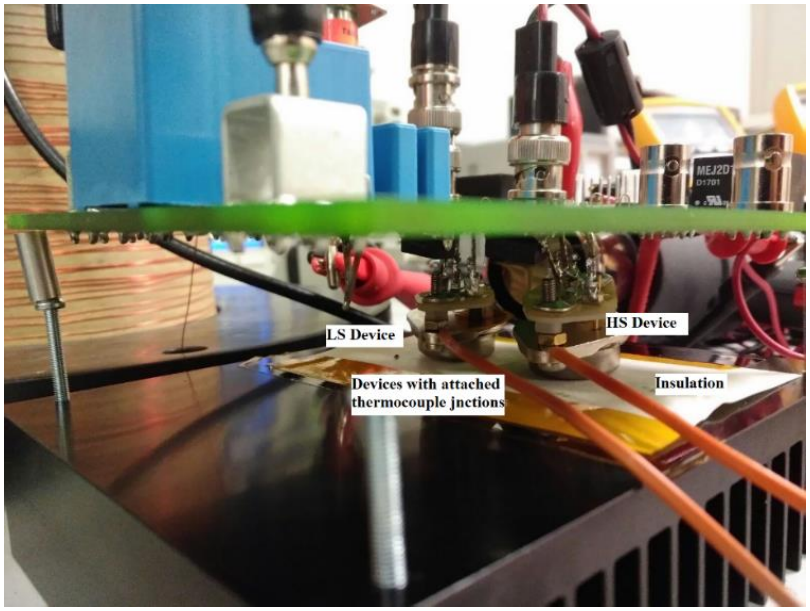


Figure 3.8. A zoomed in view of the Switching Test Setup.

The devices were heated externally using a heat gun to bring them up to the targeted case temperature, subsequent to which the gate pulses were applied. For this study, 0/25V gate pulses were applied at the DUT gate. The gate resistance was maintained at 2.5Ω. The switching energy was extracted from the waveforms in the manner described in the previous section. The turn-on and turn-off losses along with peak turn-on currents for each case across different temperatures are listed in Table 3.2., Table 3.3. CASE 2 Switching Loss at different case temperatures (Rg = 2.5 Ohm).

and

Table **3.*4***., respectively. Table 3.5. compares the extreme temperature cases across the different combinations to observe the overall performance of devices. Figure 3.9. and Figure 3.10. show this information graphically. It must also be noted that the JBSFET switching loss at 25^0C reduces with increase in Gate bias voltage.

Table 3.2. CASE 1 Switching Loss across different case temperatures (Rg = 2.5 Ohm).

Case 1	HS: SiC MOSFET			LS: SiC MOSFET	
	Turn-on			Turn-off	
	(1)	(2)	(3)	(4)	(5)
T_{CASE} (^{0}C)	E_{ON} (µJ)	t_{ON} (ns)	$I_{D, Pk}$ (A)	E_{OFF} (µJ)	t_{OFF} (ns)
25	206	52.27	16.80	90.60	48.53

Table 3.2 (Continued)**.** CASE 1 Switching Loss across different case temperatures (R_G=2.5Ω).

50	228	52.80	18.40	90.90	43.73
75	248	52.80	18.40	93.10	45.33
100	272	54.27	18.40	93.40	42.40
125	291	59.20	19.20	92.50	48.53
150	297	58.13	20.80	94.10	45.33

Table 3.3. CASE 2 Switching Loss at different case temperatures (Rg = 2.5 Ohm).

Case 2	HS: SiC MOSFET+ Antiparallel JBS Diode			LS: SiC MOSFET	
	Turn-on			Turn-off	
	(1)	(2)	(3)	(4)	(5)
TCASE (0C)	EON (µJ)	tON (ns)	ID, Pk (A)	EOFF (µJ)	tOFF (ns)
25	210	50.13	18.00	93.70	45.87
50	230	54.53	18.00	96.60	45.73
75	249	56.00	18.00	93.70	46.40
100	276	54.67	18.00	93.10	45.87
125	293	56.00	18.80	94.30	45.07
150	302	54.40	21.40	92.70	45.07

Table 3.4. CASE 3 Switching Loss at different temperatures.

Case 3	HS: SiC JBSFET			LS: SiC JBSFET	
	Turn-on			Turn-off	
	(1)	(2)	(3)	(4)	(5)
T_{CASE} (^{0}C)	E_{ON} (µJ)	t_{ON} (ns)	$I_{D, Pk}$ (A)	E_{OFF} (µJ)	t_{OFF} (ns)
25	197	51.73	16.00	92.20	43.20
50	203	54.93	16.00	95.30	42.13
75	203	54.40	16.00	92.20	44.80
100	210	53.33	17.00	95.00	44.27
125	212	54.40	17.00	90.00	44.80
150	206	51.73	18.00	92.20	44.80

Table 3.5. Switching Losses for different device combinations at case temperatures 25^0- 150^0C.

Case No.	Device Combinations (High-side/Low-side)	$I_{D, On}$ [A]		$\Delta I_{D,On}$(%) (b) vs. (a)	E-ON [µJ]		ΔE_{ON} (%) (d) vs. (c)
		(a) 25^0C	(b) 150^0C		(c) 25^0C	(d) 150^0C	
1	MOSFET/MOSFET	16.8	20.8	23.81	206	297	44.17
2	MOSFET-Diode/MOSFET	16.4	21.4	30.49	210	302	43.81
3	JBSFET/JBSFET	16	18	12.5	197	206	4.57
% Change (Case 3 vs. Case 2)		-2.5	-18.9		-6.6	-46.6	

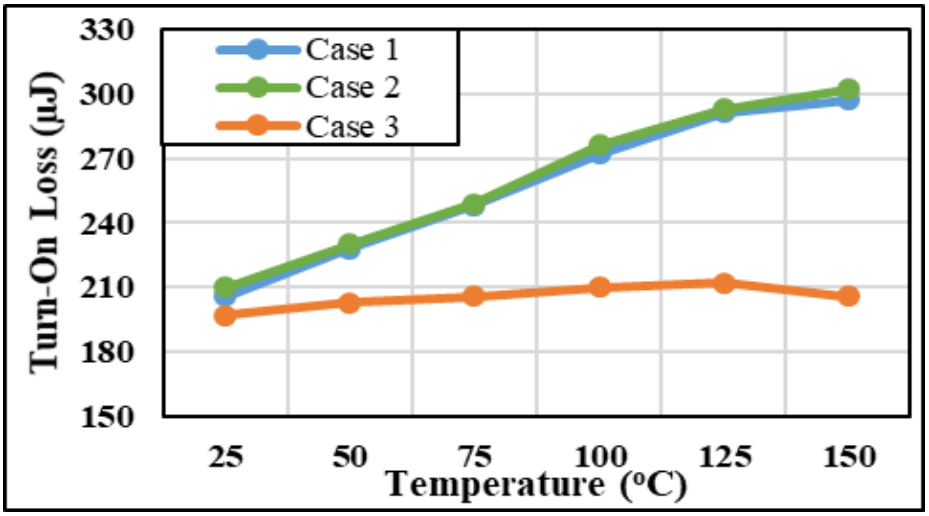


Figure 3.9. Turn-on Loss vs Case Temperature for different device combinations (Rg= 2.5 Ω).

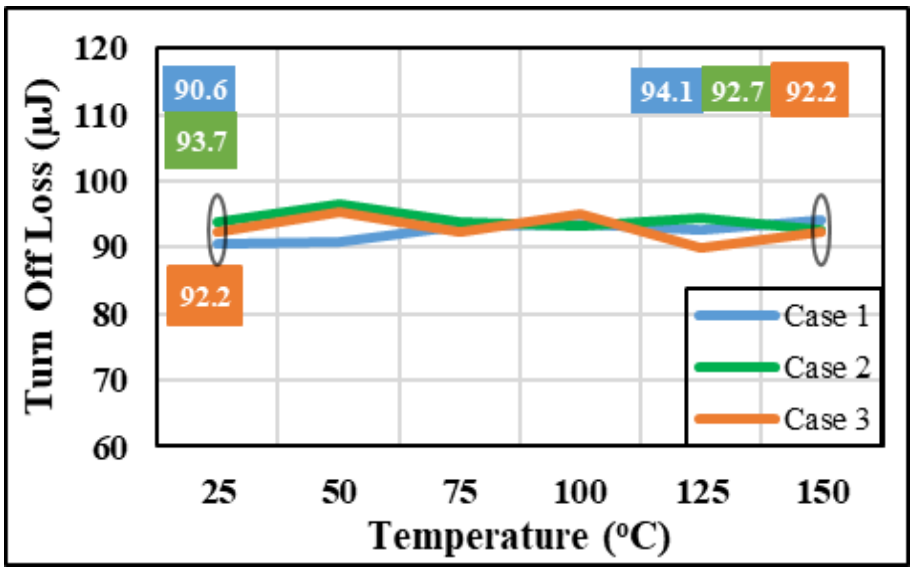


Figure 3.10. Turn-off Loss vs Case Temperature for different device combinations (R_G = 2.5Ω).

Discussion

Switching losses are primarily governed by charge storage elements in the switching loop. When using a MOSFET in the high side and low side, the reverse recovery charge due to the P-N body diode in the HS device causes energy loss during current commutation as the LS device turns on. When using an antiparallel JBS diode, the reverse recovery is avoided.

However, with rising temperatures, the on-state voltage of the P-N diode falls, while that of the JBS diode rises. Figure 3.11. shows the forward I-V curve of a JBS diode and the third quadrant curves of a MOSFET body diode taken at different temperatures.

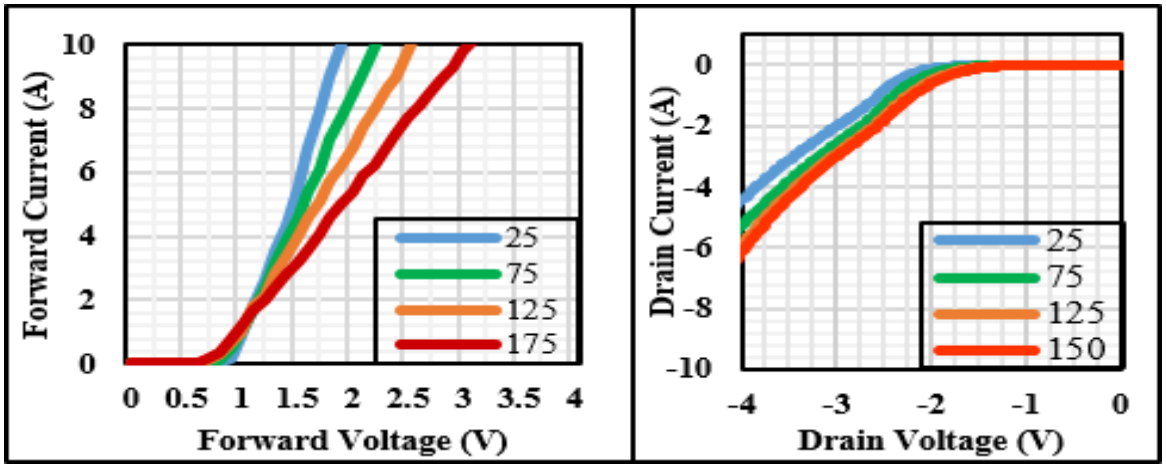


Figure 3.11. Forward voltage of a JBS Diode (left) and the third quadrant conduction graphs of a SiC MOSFET (right) measured at different temperatures.

With increasing junction temperatures, the on-state voltage of the JBS Diode becomes high enough to turn the MOSFET's P-N body diode on. And the JBS diode eventually becomes ineffective in preventing energy loss during turn-on.

In the JBSFET, however, this phenomenon is not possible, since the monolithic integration suppresses the P-N body diode from turning on. Hence, Case 3 with the HS and LS JBSFETs has minimal increase in energy loss with increasing temperature.

This is also corroborated by the trend seen in peak overshoot current during turn-on. While the peak overshoot current in Cases 1 and 2 rises by 23-30% as T_{CASE} rises from 25 ^{0}C to 150^{0}C, Case 3 exhibits only 12.5% increase in peak overshoot current[4].

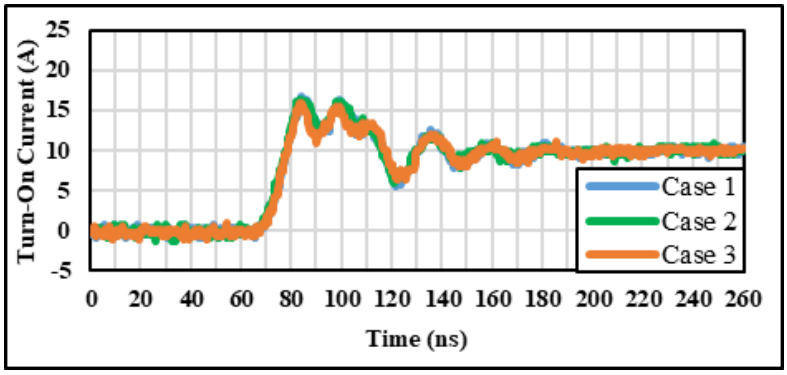


Figure 3.12. Turn-on Current Waveform at T_{CASE} = 25^0C.

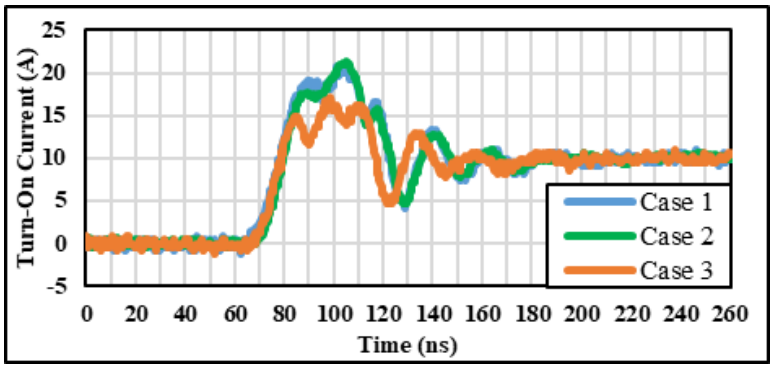


Figure 3.13. Turn-On Current Waveforms at T_{CASE} = 150^0C.

Hence, the JBSFET is proven to be a better switch when considering the full range of system operating temperatures.

3.5. Summary

Power device switching is affected by its parasitic capacitance and body-diode structures. To minimize power loss, SiC MOSFETs are typically used along with antiparallel JBS diodes. It is seen that the JBSFET has a higher switching loss compared to the MOSFET for a gate drive of -5/20V, across different gate resistances. However, the switching loss reduces when gate drive is increased to 0/25V.

To understand the effectiveness of the monolithic integration in JBSFETs, the switching tests were conducted for three combinations of high-side and low-side devices: MOSFET/MOSFET, MOSFET+antiparallel JBS Diode/MOSFET, and JBSFET/JBSFET. It

appears that the MOSFET body diode turns on at elevated temperatures due to a simultaneous rise of JBS diode on-voltage and fall in the on-voltage of the of MOSFET's body-diode. However, this is not seen in case 3 as the JBSFET successfully suppress the activation of the P-N body diode.

3.6. References

1. K. Shenai, B. J. Baliga, "**Monolithically Integrated Power MOSFET and Schottky Diode with Improved Reverse Recovery Characteristics**", IEEE Transactions on Electron Devices, vol. 37, no. 4, pp. 1167-1169, 1990

2. D. Martin, P. Killeen, W. A. Curbow, B. Sparkman, L. E. Kegley, T, Mcnutt, "**Comparing the switching performance of SiC MOSFET intrinsic body diode to additional SiC Schottky diodes in SiC power modules**", Proceedings of the 4th IEEE Wide Bandgap Power Devices and Applications, pp. 242-246, 2016

3. D. Martin, W. A. Curbow, B. Sparkman, L. E. Kegley, T, Mcnutt, "**Switching performance comparison of 1200V and 1700V SiC optimized half-bridge power modules with SiC antiparallel Schottky diodes versus MOSFET intrinsic body diodes**", Proceedings of the 2017 Applied Power Electronics Conference and Exposition, pp. 2297-2304, 2017

4. A. Kanale, B. J. Baliga, K. Han, S. Bhattacharya, "**Experimental Study of High-Temperature Switching Performance of 1.2kV SiC JBSFET in Comparison with 1.2kV SiC MOSFET**", accepted for publication in Proceedings of the European Conference on Silicon Carbide and Related Materials, pp. 1-4, 2018

CHAPTER 4

SIC MOSFET VS JBSFET – SHORT CIRCUIT CHARACTERIZATION

Short circuit characterization of power devices is essential to evaluate their ruggedness to fault conditions resulting in a short circuit[1]. The short circuit withstand capability (t_{SC}) of a power device is defined as the time duration it can operate in saturated current with high drain bias voltage before onset of failure. Presently, research on gate drivers has helped develop systems with fast response which can detect and prevent short circuit events[2,3]. In general, a short circuit capability of 10µs is considered a benchmark by industry standards. This chapter discusses the short circuit behavior of the SiC MOSFET and JBSFET structures.

There have been attempts to improve short circuit capability of SiC power MOSFETs, but they have a tradeoff with the on-resistance of the device[4].

4.1. Testing Methodology

Short circuit characterization of the power MOSFET is performed by turning the device on under direct application of a high drain bias. This results in a large current flow through the device. The gate pulse width is gradually increased to see the maximum energy the device can take before failure.

The short circuit test circuit is a simple connection of device across the high voltage DC supply, with a capacitor bank in parallel, to provide the short circuit current. Its schematic is shown in Figure 4.1. Figure 4.2. is an image of the actual test setup used for the short circuit testing. Short circuit failures can be explosive in nature, hence it is essential that the setup is enclosed in a Plexiglas box to prevent any damage or injury.

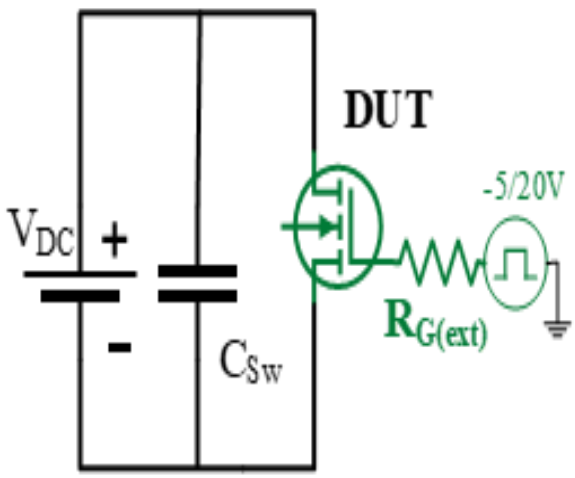


Figure 4.1. Short Circuit Test Schematic.

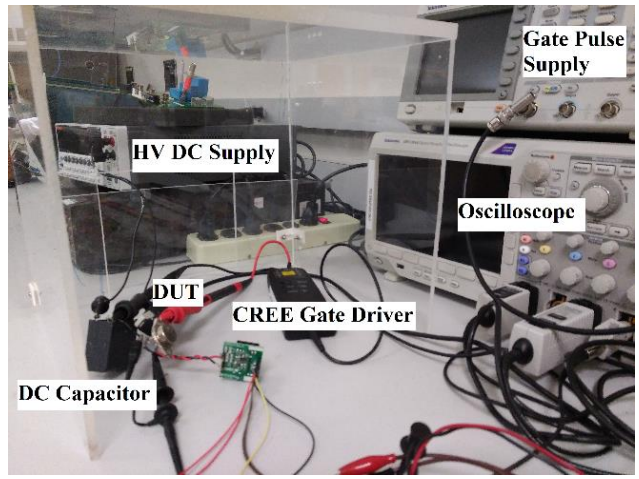


Figure 4.2. Short Circuit Test Setup.

4.2. Device Physics

The short circuit test is functionally similar to the forward I-V characterization. Hence, the short circuit current can be expressed using the following equation.

$$I_{D,Sat} = \frac{\mu_{ni} C_{OX} Z}{2L_{CH}} (V_{GS} - V_{TH})^2 \quad (4\text{-}1)$$

In (4-1), μ_{ni}, is the inversion layer mobility of electrons in SiC, Z is the channel density, which is also computed as the ratio of the device active area to its cell pitch and $I_{D,Sat}$ is the saturation current in the device. As the gate pulse is prolonged, the large amount of current flowing through the device causes a temperature rise. This might be impacting mobility through different contributing factors, which are discussed in some detail in [5].

The reduction in mobility with increasing temperature is also seen as a reduction in short circuit current. When the supplied energy increases beyond a critical limit, the device undergoes destructive failure.

4.3. Short Circuit Measurements

The PA SiC MOSFET and PA SiC JBSFET were subjected to short circuit tests with a drain bias of 800V and under gate biases of -5/15V and -5/20V. Figure 4.3. and Figure 4.4. show

the short circuit test waveform for the PA SiC MOSFET and the PA SiC JBSFET for gate biases of -5/15V, and -5/20V, respectively.

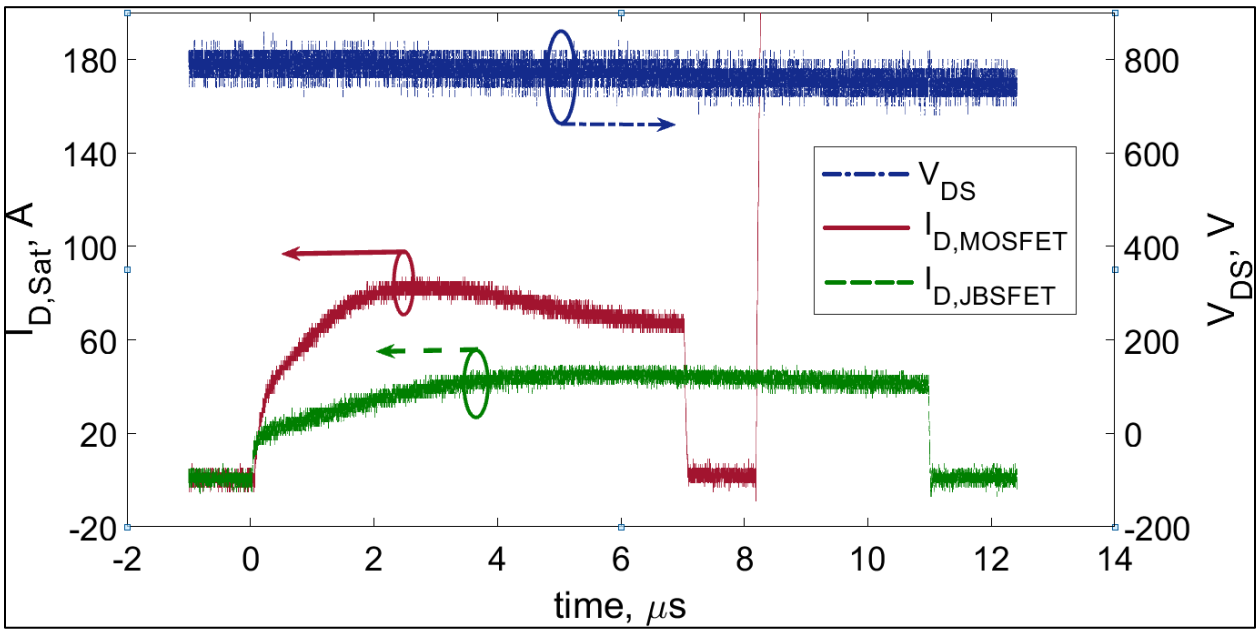


Figure 4.3. Short circuit waveform of the PA MOSFET and PA JBSFET for a Gate Bias of -5V/15V.

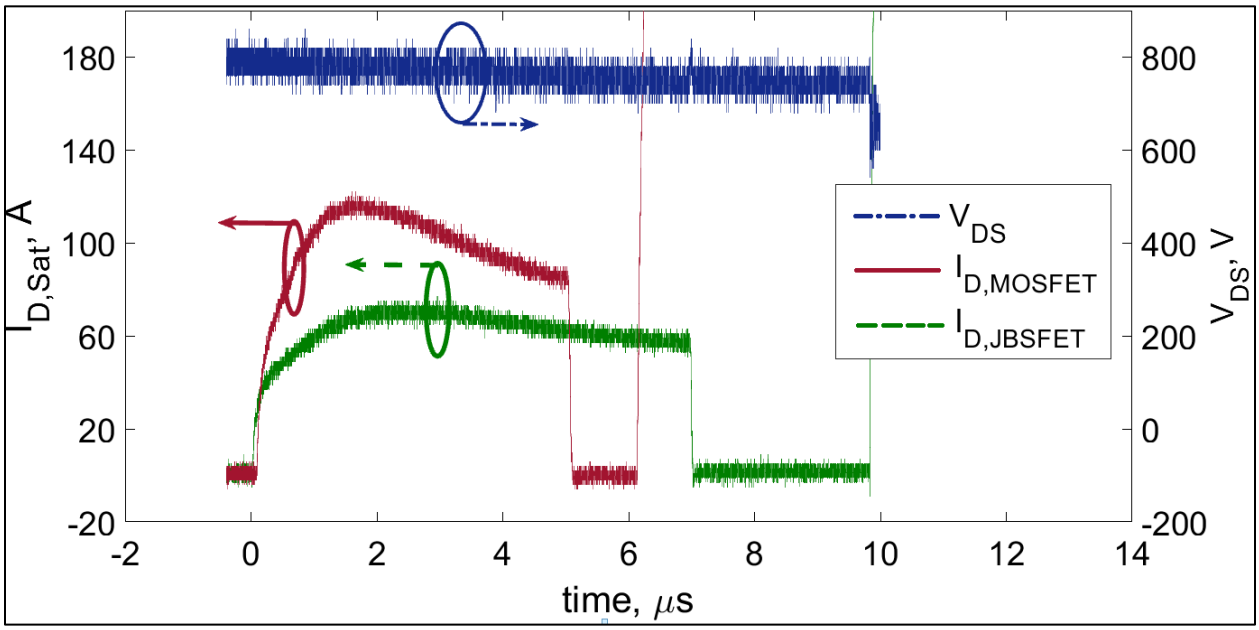


Figure 4.4. Short circuit waveform of the PA MOSFET and PA JBSFET for a Gate Bias of -5/20V.

It is seen that the PA MOSFET fails at 7μs for a gate bias of 15V and at 5μs for a gate bias of 20V. It is also clear that lower drain saturation currents allow longer short circuit withstand capability. A similar trend is exhibited by the PA JBSFET, which passes the 10μs benchmark for a gate bias of -5/15V and fails at 7μs for a gate bias of -5/20V. The peak short circuit current for the PA JBSFET is found to be lesser than that of the PA MOSFET for either gate bias.

Hence, it can be concluded that the JBSFET has a better short circuit capability compared to the SiC MOSFET.

4.4. Discussion

The short circuit capability of power devices has been studied in some detail over the years[6-9]. The most common short circuit failure mechanism for SiC devices reported in literature include the activation of the parasitic N-P-N bipolar transistor within the MOSFET structure[10, 11] and a failure of the gate oxide[12]. The N-P-N parasitic BJT is believed to turn on due to an increase in the leakage current, which, in turn, is caused by the injection of traps at the oxide-semiconductor interface into the P-base. The gate oxide failure is said to be a hysteretic effect of repetitive short circuit on the thin gate oxide layer.

Both failure mechanisms are rooted in the high junction temperature seen by the device during short circuit operation. The most logical way to circumvent this situation is to create devices with a larger cell pitch[13]. The larger area increases the on-resistance and thus, suppressing the peak short circuit current. This suppression reduces the temperature rise and thus, would allow device operation in short circuit mode for a longer period of time. This is directly seen in the results reported above, since the PA JBSFET, which is larger in cell pitch, compared to the PA MOSFET has a better short circuit capability.

Other methods to increase short circuit ruggedness have attempted to introduce embedded source resistance regions in the device[14], which, too, causes an increase in device on-resistance, subsequently leading to improved short circuit capability.

The pattern of failure suggests the existence of a critical energy that may be unique to silicon carbide devices or the design of power MOSFETs. The failure mechanism observed in the PA devices do not hint at either known mechanism, i.e, there is no current tail towards the end of the short circuit pulse, nor is there any sign of gate degradation seen in the gate pulse. However, the devices are shorted and cannot sustain a voltage after failure. This hints at the possibility of the source metal melting through the top region[15] and penetrating the drift region, thereby destroying the device.

4.5. An Additional Application of the Short Circuit Test

It was observed that the peak current seen during a short circuit pulse (see Figure 4.4), could be an approximation of the saturation current at that drain bias. Table 4.1. shows the measured peak current values at V_{DS} = 800V for different gate biases. The channel width Z is calculated as the ratio of the active area to the cell pitch. Both devices have an identical active area of 0.045cm^2. Hence, the MOSFET, with its cell pitch of 3.1µm, has a channel width of 140.6 cm, while the JBSFET, with its cell pitch of 6.1µm, has a channel width of 73.8 cm. It is seen that at either gate bias, the ratio of the peak short circuit currents matches the ratio of their channel widths. From (4-1), it can be concluded that the peak short circuit current at any drain bias can be used as a measure for the saturation current of the device at that drain bias.

With this new knowledge, it is possible to extend forward I-V curves to any voltage and get the corresponding saturation current. To obtain the same, the MOSFET can be subject to non-destructive short circuit tests (with $t_{Gate\text{-}Pulse}$ < 1µs). In this way, the forward I-V of a device, which

was mentioned to have been constrained by the power capabilities of automated testers, can be obtained with little extra effort. Figure 4.5. is a plot of extended I-V characteristics for the PA MOSFET and JBSFET for gate biases of 15V and 20V.

Table 4.1. Experimentally measured $I_{D,Sat}$ at V_{DS} = 800V.

Sl No.	Device	Measured $I_{D,Sat}$ (A)		Channel Width (cm)
		V_{GS} = 15 V	V_{GS} = 20V	
1	MOSFET	85	130	140.6
2	JBSFET	45	75	73.8
Ratio		1.9	1.7	1.9

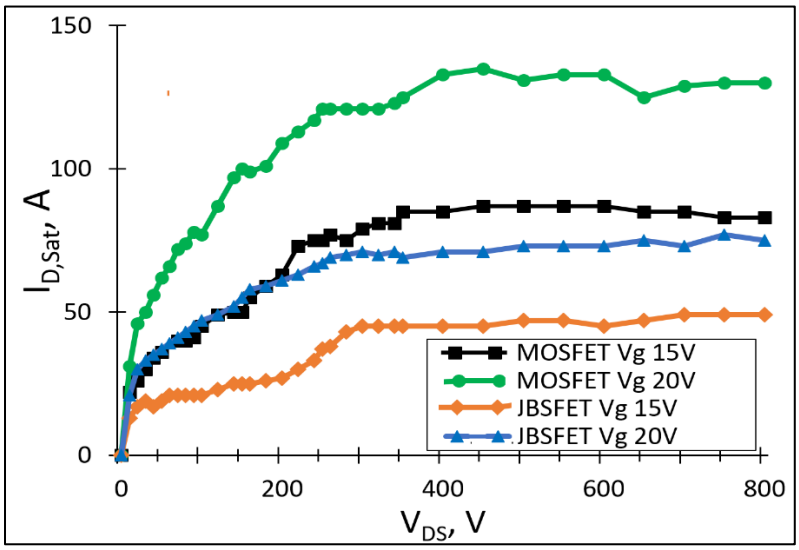


Figure 4.5. High Voltage I-V Curves extracted from short-pulse, non-destructive SC tests.

4.6. A new Figure of Merit to evaluate Short Circuit Robustness

The tradeoff between short circuit withstand capability and device on-resistance has been mentioned before[13]. The JBSFET, too, achieves a similar tradeoff to gain enhanced short circuit ruggedness. In practical applications, as showed in Chapter 3, SiC MOSFETs are used along with antiparallel JBS diodes. Short circuit robustness metrics, however, do not include the JBS diode when describing tradeoffs between short circuit withstand time against chip area and on-resistance. Since the JBSFET is a combination of two devices, it needs to be compared with the MOSFET-

antiparallel diode for a fair evaluation. This requires a new figure-of-merit. It is proposed[15] that an equivalent specific on-resistance be used to evaluate t_{SC} vs R_{ON} tradeoff for the power MOSFET + antiparallel JBS diode combination. The equivalent specific on-resistance would be defined as

$$R_{ON,Sp,Eq} = R_{ON,MOSFET} * (A_{Act,MOSFET} + A_{Chip,JBS\ Diode}) \tag{4-3}$$

where A_{ACT} is the active area of the device and A_{Chip} is the chip area of the device. For the PA devices, the MOSFET was coupled with a CREE JBS Diode[17] for the purposes of this analysis.

Table 4.2. $R_{On,Sp,Eq}$ for comparing the JBSFET with MOSFET+ Antiparallel diode combination.

Device	Active Area (cm^2	R_{ON} (mΩ)	Gate Bias (V)	t_{SC} (µs)	$R_{On,Sp,Eq}$ (mΩ-cm^2)
MOSFET	0.045	153	V_{GS} = 15V	7	6.9
			V_{GS} = 20V	5	
JBSFET	0.045	200	V_{GS} = 15V	>10	9
			V_{GS} = 20V	7	
MOSFET+ antiparallel Diode	0.045+0.0285 = 0.0735	153	V_{GS} = 15V	7	11.2
			V_{GS} = 20V	5	

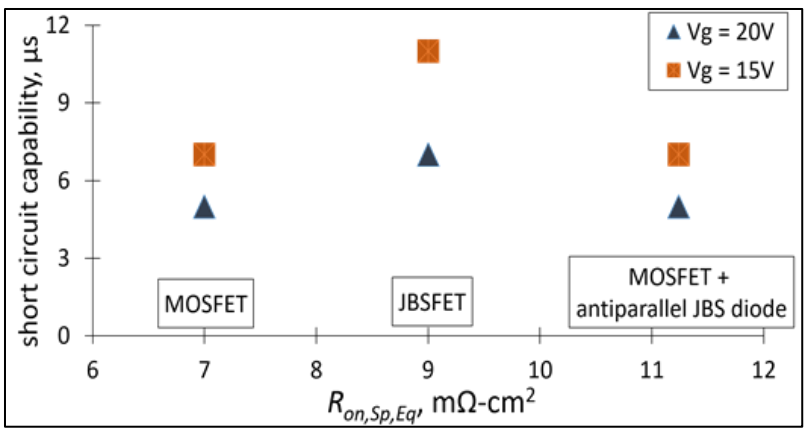


Figure 4.6. Using $R_{On,Sp,Eq}$ to compare JBSFET and MOSFET +JBS Diode combinations

Table 4.2. lists the parameters discussed above. Figure 4.6. displays a graphical representation to show the need for equivalent on-resistance as a new metric to provide a fair comparison for the JBSFET's short circuit robustness. The process of monolithic integration in the JBSFET allows economy of chip area and on-resistance while providing enhanced short-circuit

ruggedness, when compared to the MOSFET + antiparallel diode combination which only increases the effective chip area with no variations in the short-circuit performance.

4.7. Summary

The short circuit capability of power devices was introduced and the short circuit performance of the PA MOSFET and JBSFET was reported. It was shown that the JBSFET is a superior switch from a short circuit ruggedness standpoint. This was followed by a discussion of known SiC MOSFET Short-circuit failure mechanisms. The short circuit test was modified to develop a method for measurement of high-voltage forward I-V data for power devices. It is believed that this method can be used to obtain forward I-V curves up to any voltage, as long as the short-circuit pulse itself is kept small enough to leave the device undamaged.

A new figure of merit was defined to enable a fair comparison between the JBSFET and MOSFET-antiparallel JBS diode combinations to evaluate t_{SC} vs R_{ON} tradeoff.

4.8. References

1. P. Godignon, V. Soler, M. Cabello, J. Montserrat, J. Rebollo, L. Knoll, E. Bianda, A. Mihaila, "New Trends in High voltage MOSFET based on wide bandgap materials", Proceedings of the 2017 International Semiconductor Conference, pp. 3-10, 2017

2. S. Hazra, K. Vechalapu, S. Madhusoodhanan, S. Bhattacharya, K. Hatua, "Gate Driver Design Considerations for Silicon Carbide MOSFETs Including Series Connected Devices" Proceedings of the 2017 IEEE Energy Conversion Congress and Exposition, pp. 1-5, 2017

3. A. Tripathi, K. Mainali, S. Madhusoodhanan, A. Yadav, K. Vechalapu, S. Bhattacharya, "A MV Intelligent Gate Driver for 15kV SiC IGBT and 10kV SiC MOSFET", Proceedings of the 2016 Applied Power Electronics Conference and Exposition, pp. 2076-2082, 2016

4. X. Huang, L. Fursin, A. Bhalla, W. Simon, J. C. Dries, "Design and Fabrication of 3.3kV SiC MOSFETs for Industrial Applications", Proceedings of the 29th International Symposium of Power Semiconductor Devices and ICs, pp 255-258, 2017

5. T. Kimoto, J. A. Cooper, "Fundamentals of Silicon Carbide Technology", pp. 329-339, Wiley Singapore, 2014

6. M.Trivedi, K. Shenai, "Failure Mechanisms of IGBTs under short-circuit and clamped inductive switching stress", IEEE Transactions on Power Electronics, vol. 14, no. 1, pp. 108-116, 1999

7. X. Huang, G. Wang, Y. Li, A. Q. Huang, B. J. Baliga, "Short-Circuit Capability of 1200V SiC MOSFET and JFET for fault protection", Proceedings of the 28th IEEE Applied Power Electronics Conference and Exposition, pp. 197-200, 2013

8. D. P. Sadik, J. Colmenares, D. Peftitsis, G. Tolstoy, J. Rabkowski, H. Nee, "Analysis of Short-Circuit conditions for Silicon Carbide Power Transistors and Suggestions for Protection", Proceedings of the 16th European Conference on Power Electronics and Applications, pp. 1-10, 2014

9. J. An, M. Namai, H. Yano, N. Iwamuro, Y. Kobayashi, S. Harada, "Methodology for enhanced short-circuit capability of SiC MOSFETs", Proceedings of the 30th International Symposium on Power Semiconductor Devices and ICs, pp. 391-394, 2018

10. G. Romano, A. Fayyaz, M. Riccio, L. Maresca, G. Breglio, A. Castellazzi, A. Irace, "A Comprehensive Study of Short-Circuit Ruggedness of SiC Power MOSFETs", IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 4, no. 3, pp. 978, 2016

11. R. Singh, B. Gummel, S. Sundaresan, "Short Circuit Robustness of 1200V SiC Switches", in 2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications, pp. 1-4, 2015

12. R. Green, D. P. Urciuoli, A. J. Lelis, "Short-Circuit Robustness Testing of SiC MOSFETs", Proceedings of the European Conference on Silicon Carbide and Related Materials, pp. 525-528, 2017

13. Y. Nakao, S. Watanabe, N. Miura, M. Imaizumi, T. Oomori, “Investigation into Short-Circuit Ruggedness of 1.2kV 4H-SiC MOSFETs”, Proceedings of the International Conference on Silicon Carbide and Related Materials, pp. 1123-1126, 2008

14. H. Hatta, T. Tominaga, S. Hino, N, Miura, S. Tomohisa, S. Yamakawa. “Suppression of short-circuit current with embedded source resistance in SiC-MOSFET”, in International Conference on Silicon Carbide and Related Materials, pp. 727-730, 2017

15. K. Han, A. Kanale, B. J. Baliga, B. Ballard, A. Morgan, D. C. Hopkins, “New Short Circuit Failure Mechanism for 1.2kV 4H-SiC MOSFETs and JBSFETs”, accepted for publication in the Proceedings of the 6th IEEE Workshop on Wide bandgap Power Devices and Applications, pp. 1-4, 2018

16. A. Kanale, K. Han, B. J. Baliga, S. Bhattacharya, “Superior Short circuit Robustness of 1.2kV SiC JBSFETs when compared to 1.2kV SiC MOSFETs”, accepted for publication in the Proceedings of the 2018 European Conference on Silicon Carbide and Related Materials, pp. 1-4, 2018

17. CREE SiC JBS Diode C4D015120A, https://www.wolfspeed.com/c4d05120a

CHAPTER 5

CONCLUSIONS AND FUTURE WORK

As power semiconductor device technology, in tandem with developments in power electronics, accelerate known engineering systems towards greater efficiency and higher operating frequencies, technologies will continue to shrink and become increasingly compact. The recent interest in monolithic integration of power devices like the JBSFET is a shining example of such compaction at work. To propagate such technology further, it is necessary to navigate the tradeoffs on switching loss and on-resistance, while maintaining a rugged device capable of operating in adverse environments.

In this work, the JBSFET was characterized alongside a planar MOSFET of similar design and investigated for efficiency in switching and short circuit test conditions. It was seen that the JBSFET is an effective switching transistor over a large temperature range, due to its ability to suppress the parasitic P-N body diode completely. The larger cell pitch indirectly strengthens the JBSFET against short circuit faults. Hence the JBSFET is a more efficient and rugged switch compared to the SiC MOSFET.

However, the JBSFET needs to be investigated for avalanche ruggedness, as that is a very important fault condition in power converter systems. Subsequent to its ruggedness testing, the JBSFET must be employed as a switch in power converters to ascertain the true impact of the monolithic integration. Newer technologies such as the BiDFET[1] promise a major leap in the quest to consolidate and simplify power electronics systems.

As systems grow more compact and complex with each day, silicon carbide technology must find ways to eliminate process-induced obstacles and venture into the very high blocking voltage ranges. It is an interesting future for wide bandgap power devices, as power electronics

technology has developed mechanisms to detect fault conditions and protect solid state switches from catastrophic failure. Industrial efforts to commercialize SiC power devices have also produced a lot of innovative advances in power device technology. As all spheres – industry, academia and government converge on wide bandgap devices as the means to create a greener, cleaner future, there is no doubt that the next stage of the wide bandgap semiconductor revolution is around the corner.

5.1. References

1. B. J. Baliga, K. Han, “Monolithic SiC Bi-directional field effect transistor (BiDFET): concept and electrical characteristics”, in the 50th Government Microcircuit Applications and Critical Technology Conference, 2018