ABSTRACT

HAN, KIJEONG. Design, Analysis, and Optimization of 1.2 kV 4H-SiC Planar-Gate Power MOSFETs for Improved High Frequency Switching. (Under the direction of Dr. B. Jayant Baliga).

This research focuses on the analysis, design, fabrication, and testing of high frequency 1.2 kV 4H-SiC Planar-Gate Power MOSFETs. To achieve the high switching capability, the MOSFET’s reverse transfer capacitance ($C_{gd}$) and gate-to-drain charge ($Q_{gd}$), resulting from the gate-to-drain overlap above the JFET region, must be minimized because they are the dominant components limiting the switching speed. Therefore, achieving low values for the High-Frequency Figures-of-Merit (HF-FOMs), defined as $[\text{Ron} \times C_{gd}]$ and $[\text{Ron} \times Q_{gd}]$, is a main goal for this research. Gate oxide thickness ($t_{OX}$) of 50 nm and channel length ($L_{CH}$) of 0.5 $\mu$m were fixed for all the 1.2 kV 4H-SiC Planar-Gate Power MOSFET structures throughout this thesis.

An extensive study of structure optimizations for conventional 1.2 kV 4H-SiC Planar-Gate Power MOSFETs to reduce on-resistance and improve the switching capability has been carried out first with analytical models and numerical simulations.

In order to improve the HF-FOM, a 1.2 kV 4H-SiC Split-Gate MOSFET (SG-MOSFET) structure was experimentally verified for the first time. Compared with the conventional Planar-Gate MOSFET, the SG-MOSFET has 2.4× smaller HF-FOM $[\text{Ron} \times Q_{gd}]$ due to the reduced gate-to-drain charge.

To further improve the device electrical characteristics, a novel 1.2 kV 4H-SiC Buffered-Gate MOSFET (BG-MOSFET) structure has been experimentally demonstrated to have superior HF-FOMs for the first time. The split-gate electrode is buffered from the drain by extending the P+ shielding region beyond its edge. From the measured data on devices fabricated in a 6-inch foundry, X-FAB, the BG-MOSFET is demonstrated to have 4.0× and 2.6× smaller HF-FOM
[Ron×Qgd], and 3.6× and 2.1× smaller HF-FOM [Ron×Cgd], when compared to the conventional Planar-Gate MOSFET and Split-Gate MOSFET, respectively.

Most SiC planar-gate power MOSFETs have been reported with the linear cell topology. To understand the electrical performance with various channel and JFET densities in the MOSFET structures, different cell topologies have been studied. A 1.2 kV rated 4H-SiC MOSFET with octagonal-cell topology has been experimentally demonstrated for the first time. From the measured electrical characteristics, the MOSFET with the octagonal-cell topology is demonstrated to have 1.4× superior HF-FOM [Ron×Qgd], and 2.1× superior HF-FOM [Ron×Cgd] compared with the conventional linear-cell MOSFET. Moreover, the Split-Gate (SG) concept is combined with the octagonal cell topology for the first time (SG-OCTFET) to achieve a further improvement in Cgd, Qgd, and HF-FOMs. A detailed comparison of the measured electrical characteristics for the 1.2 kV 4H-SiC power MOSFETs with linear, square, hexagonal, octagonal, and Split-Gate octagonal cell topologies fabricated at X-Fab using the same design rules and process flow as the conventional linear-cell MOSFETs will be provided.
Design, Analysis, and Optimization of 1.2 kV 4H-SiC Planar-Gate Power MOSFETs for Improved High Frequency Switching.

by
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DEDICATION

To my wife, Hyunjung Lee,
BIOGRAPHY

Kijeong Han received the B.S. and M.S. degrees in electrical engineering at Korea Aerospace University, Goyang, South Korea in 2012, and Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea in 2014, respectively. He started working in 2015 toward the Ph.D. degree in wide bandgap high voltage and high power devices in the department of Electrical and Computer Engineering at North Carolina State University. He has worked for the U.S. Department of Energy (DOE) funded PowerAmerica project to design novel 4H-SiC power MOSFETs. In the project, he contributed to establishing the PRocess Engineered for manufacturing Silicone Carbide (SiC) Electronic-devices (PRESiCE™) at a foundry company, X-Fab, Texas. In addition, he has performed device designs for the Solar Energy Technologies Office (SETO) project supported by the U.S. DOE to achieve PV inverter systems using bi-directional FETs (BiDFETs). His research interests include the design, fabrication, characterization, and analysis of high power devices. He has authored and coauthored over 20 technical journal and conference papers. He received the Early Doctoral Research Achievement Award from College of Engineering at NCSU in 2019.
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CHAPTER 1.

Introduction

1. Background & Motivation

For high power applications, 4H-SiC is an attractive wide bandgap semiconductor having high critical electric field (~2 MV/cm), which makes SiC power devices have a thin drift layer with high doping concentration to support high breakdown voltage [1][2]. Especially, 4H-SiC power MOSFETs have come into the spotlight due to the fast switching speed and low specific on-resistance. In the past decade, there has been tremendous progress in the electrical performances of 4H-SiC power MOSFETs resulting in their commercialization [3]. It is widely known that the SiC MOSFET switches faster than its counterpart, i.e. Si IGBT, due to its inherent unipolar property in current conduction. Maximum allowable frequency of the devices can be an indicator to study the performance differences. The maximum frequency is calculated based on on-resistance (or forward voltage drop for the IGBTs), switching energy loss, and thermal resistance [4];

\[
P_{loss} = V \times I \times \delta + f_{max} \times E_{sw} = (T_{j,max} - T_c)/R_{\theta,jc}\quad \text{(1.1)}
\]

\[
f_{max} = \frac{(T_{j,max} - T_c)/R_{\theta,jc} - (V \times I \times \delta)}{E_{sw}}\quad \text{(1.2)}
\]

where \(P_{loss}\) is maximum power loss, \(V\) is voltage, \(I\) is current, \(\delta\) is duty cycle, \(f_{max}\) is the maximum frequency, \(E_{sw}\) is the switching energy loss, \(T_{j,max}\) is the maximum junction temperature, \(T_c\) is ambient temperature, and \(R_{\theta,jc}\) is the thermal resistance. Figure 1.1(a) shows the thermal resistance...
in the package for the Wolfspeed’s SiC MOSFETs [5] and Infineon’s Si IGBTs [6] as a function of chip size. The thermal resistance of Si IGBTs in the commercial package is about twice that of SiC MOSFETs for the same chip size. The analytically calculated maximum frequency for the 1.2 kV SiC MOSFETs and Si IGBTs with available electrical characteristics [5][6] is shown in Figure 1.1(b) [4]. The results indicate the SiC MOSFETs overall allows higher maximum operating frequency for the same current rating conditions compared with the Si IGBTs. However, the maximum frequency capability of the SiC MOSFETs is rapidly reduced when the current rating is increased, and it becomes no longer superior to that of the Si IGBTs, especially for the higher operating current ratings (Figure 1.1(b)). This behavior is more noticeable if the Si IGBTs have as low thermal resistance as the SiC MOSFETs with advanced packaging technology (see the dashed line in Figure 1.1(b)).

In order to improve the maximum frequency capability of the SiC MOSFETs even for the higher current ratings, the switching energy loss should be minimized as observed from (1.2). This is particularly important for the high frequency applications because the switching energy loss becomes dominant in total energy consumption.

Figure 1.1. (a) Thermal resistance used in the package of 1.2 kV SiC MOSFETs [5] and Silicon IGBTs [6] as a function of chip size, (b) Calculated maximum frequency of 1.2 kV SiC MOSFETs and IGBTs with available electrical characteristics from the datasheets, using duty cycle of 0.5 [4].
2. Switching Characteristics

It is known that reverse transfer capacitance (C<sub>gd</sub>) and gate-to-drain charge (Q<sub>gd</sub>), resulting from the gate-to-drain overlap above the JFET region, are the dominant components limiting the switching capability [7][8]. Figure 1.2(a) shows a clamped inductive load switching circuit configuration using a free-wheeling diode (high side) and 4H-SiC MOSFET (low side) [2]. The C<sub>gd</sub> of the MOSFET is marked in the figure. Turn-on switching waveforms for gate voltage (V<sub>g</sub>), drain current (I<sub>d</sub>), and drain voltage (V<sub>d</sub>) of the switching circuit are shown in Figure 1.2(b). When the gate voltage becomes bigger than threshold voltage (V<sub>th</sub>), the drain current begins increasing. When the current reaches to load current, it remains constant and the drain voltage decreases toward ~0 V. Meanwhile, the gate plateau voltage is observed due to the C<sub>gd</sub> charging as marked in Figure 1.2(b), and the dominant switching energy loss occurs during the plateau. This plateau time, thus, is directly related to the C<sub>gd</sub> values. The Q<sub>gd</sub> can be obtained from the C<sub>gd</sub> as below [2];

\[
Q_{gd} = \int C_{gd}(V_d) \, dV_d
\]  

(1.3)

Figure 1.2. (a) Clamped inductive load switching circuit configuration with a free-wheeling diode (high side) and 4H-SiC MOSFET (low side), (b) Turn-on switching waveforms for gate voltage (V<sub>g</sub>), drain current (I<sub>d</sub>), and drain voltage (V<sub>d</sub>) of the switching circuit [2].
Here, \( V_d \) is the drain voltage. Therefore, in order to reduce the energy loss in high frequency applications, the MOSFET’s \( C_{gd} \) and \( Q_{gd} \) must be minimized because the switching energy loss mainly originates from their charging (turn-on plateau) and discharging (turn-off plateau) during each switching cycle [7]. High Frequency Figures-of-Merit (HF-FOMs), defined as \( R_{on} \times C_{gd} \) and \( R_{on} \times Q_{gd} \), are common high frequency performance indicators [2]. It is important to achieve low values for the HF-FOMs.

In addition, a gate driver design without false trigger can be achieved with smaller \( C_{gd} \) and devices with larger FOM \( [C_{iss}/C_{gd}] \) ratio are desirable to prevent shoot-through current during high frequency operation [2].

There have been several research reports to reduce the \( C_{gd} \) and \( Q_{gd} \) so that the improved HF-FOMs could be achieved. Cree, Inc. (Wolfspeed) has proposed and demonstrated 4H-SiC central implant MOSFET (CIMOSFET) structures to improve the \( C_{gd} \), \( Q_{gd} \), and HF-FOMs in 2015 [9]. This approach requires an additional mask step for p-type ion implantation in the middle of the JFET region to reduce the gate-to-drain overlap area. Si split-gate and terraced-gate structures have demonstrated to have the better \( C_{gd} \), \( Q_{gd} \), and HF-FOMs [7][10][11]. Numerical simulation studies of a 4H-SiC split-gate MOSFET structure have been presented without any experimental results in ISPSD 2016 [12].

3. PRESiCE™

The Process engineered for manufacturing Silicone Carbide (SiC) electronic-devices (PRESiCE™) has been set up, established, and successfully qualified at a commercial foundry company, X-Fab, by running multiple wafer lots on a PowerAmerica project funded by Office of Energy Efficiency and Renewable Energy (EERE), U.S. Department of Energy [13]. The
PowerAmerica sponsored the development of PRESiCE™ in 2015 for fabricating wide bandgap power devices such as MOSFETs, JBSFETs, and JBS rectifiers to encourage participation of more companies in manufacturing devices and to drive the device manufacturing cost down by increasing the wafer volume at the foundry in the United States.

Figure 1.3(a) shows the fabricated power devices on a 4H-SiC 6-inch wafer using the PRESiCE™, and the fabricated devices were measured with the semi-automatic Signatone probe station and Keysight B1505A curve tracer as shown in Figure 1.3(b). Wafer maps and statistical distributions were created using macro programs out of the measured data from the multiple devices.

![Figure 1.3](image1.png)

(a) Fabricated power devices on a 4H-SiC 6-inch wafer, (b) Semi-automatic Signatone probe station and Keysight B1505A curve tracer.

![Figure 1.4](image2.png)

Figure 1.4. Wafer map and statistical distribution of the on-resistance of power MOSFETs manufactured using PRESiCE™ technology [13].
fabricated wafer lots. The NCSU PRESiCETM process has been qualified by comparing those wafer maps and statistical distributions to each other.

A wafer map of the on-resistance of a typical power MOSFET with the statistical distribution and a wafer map of the threshold voltage of a typical power MOSFET with the statistical distribution is shown in Figure 1.4 and Figure 1.5, respectively. The figures demonstrate that the standard deviations of the device parameters are very small allowing the manufacturing of power MOSFETs with high yield.

All the designed and optimized 1.2 kV rated 4H-SiC planar gate power MOSFETs for my entire Ph.D work were fabricated at X-Fab using the qualified PRESiCETM process.

4. Outline of Dissertation

In this dissertation, novel device structure designs, fabrications, and characterizations of 1.2 kV 4H-SiC planar-gate power MOSFETs for the improved HF-FOMs are extensively discussed. Gate oxide thickness (tOX) of 50 nm and channel length (LCH) of 0.5 µm were fixed for
all the 1.2 kV 4H-SiC Planar-Gate Power MOSFETs throughout this dissertation. The dissertation consists of total 6 chapters.

Chapter 1 provides the research background and motivation with regard to the 1.2 kV 4H-SiC planar-gate MOSFETs with the improved HF-FOMs.

Chapter 2 presents the optimization of JFET region parameters for the 1.2 kV 4H-SiC linear cell planar-gate MOSFET to achieve the reduced $C_{gd}$, $Q_{gd}$, and HF-FOMs. The MOSFETs with various designs in the JFET region were fabricated on 6-inch wafers. Investigations on on-resistance, $C_{gd}$, $Q_{gd}$, and leakage currents in the forward blocking mode conclude that the optimized JFET region allows improved HF-FOMs.

Chapter 3 discusses the 1.2 kV-rated 4H-SiC linear cell Split Gate MOSFET (SG-MOSFET) structure. It has been demonstrated to have superior HF-FOMs with experimental validation for the first time. Excellent electrical characteristics (specific on-resistance, threshold voltage, breakdown voltage, $C_{gd}$, and $Q_{gd}$) were measured from devices fabricated on a 6-inch SiC wafer. Compared to the conventional MOSFET, the SG-MOSFET has $2.4\times$ smaller HF-FOM $[R_{on}\times Q_{gd}]$ due to the reduced $Q_{gd}$.

Chapter 4 describes a novel 1.2 kV-rated 4H-SiC linear cell Buffered-Gate MOSFET (BG-MOSFET) structure. The structure has been intensively studied and experimentally demonstrated to have superior HF-FOMs for the first time. From the measured data on devices fabricated in a 6-inch foundry, the BG-MOSFET is demonstrated to have $4.0\times$ and $2.6\times$ smaller HF-FOM $[R_{on}\times Q_{gd}]$, and $3.6\times$ and $2.1\times$ smaller HF-FOM $[R_{on}\times C_{gd}]$, when compared to the conventional MOSFET and SG-MOSFET, respectively.

Chapter 5 presents detailed comparisons of the electrical characteristics for the 1.2 kV rated 4H-SiC planar-gate MOSFETs with linear, square, hexagonal, octagonal, and Split-Gate octagonal
cell topologies fabricated using the same design rules and process flow in a 6-inch foundry for the first time. TCAD numerical simulations have been conducted to analyze the structures. It has been observed that the square and hexagonal cell topologies with the same structural dimensions show similar electrical performance. When compared with the standard linear cell topology: (a) the hexagonal cell topology has 1.15× better on-resistance and 1.12× worse HF-FOM \([R_{on} \times Q_{gd}]\); (b) the octagonal cell topology has 1.5× worse on-resistance and 1.4× better HF-FOM \([R_{on} \times Q_{gd}]\); (c) the Split-Gate octagonal cell topology has 1.5× worse on-resistance and 2.3× better HF-FOM \([R_{on} \times Q_{gd}]\). In addition, the octagonal cell topologies have a much superior \([C_{iss}/C_{gd}]\) FOM to prevent shoot-through during high frequency switching.

Chapter 6 summarizes the major accomplishment of this work and discusses future works.
REFERENCES


CHAPTER 2.

Optimization of 1.2 kV 4H-SiC Linear Cell Planar-Gate MOSFETs

1. Background & Motivation

1.1. Major Issues of 4H-SiC MOSFETs

Due to the superior material properties, low on-resistance, and fast switching speed with unipolar current conduction, 4H-SiC MOSFETs have been spotlighted and commercialized [1][2][3]. Although the 4H-SiC MOSFETs have shown tremendous progresses in the electrical performances in the past decade, there are still two major performance limiting factors that should be carefully considered for the structure optimization study [1][2].

High gate oxide electric field is the first performance limiting factor in the 4H-SiC MOSFETs. Figure 2.1 shows the half-cell cross-sectional view of the 4H-SiC planar-gate power MOSFETs [2]. During the forward blocking mode, the highest electric field is observed at the corner of the P+ shielding region in the 4H-SiC and at the center of the gate oxide (“A” in Figure 2.1). SiO₂ has been used for the gate oxide in the 4H-SiC MOSFETs because it can be formed easily with a thermal oxidation process, similar to Si [1][2][4]. Relative dielectric constant for the SiO₂ is 3.9, while that for the 4H-SiC is 9.7 [1]. From the Gauss’s law, the relationship of the electric field between the SiO₂ and 4H-SiC can be found as below;

\[
\varepsilon_{ox} \cdot \varepsilon_{ox} = \varepsilon_{4H-SiC} \cdot \varepsilon_{4H-SiC}
\]

\[
\varepsilon_{ox} = 2.5 \cdot \varepsilon_{4H-SiC}
\]
These equations indicate that the electric field of the SiO$_2$ becomes 2.5 times bigger than that of the 4H-SiC at the interface. Although the critical electric field for the SiO$_2$ is about 10 MV/cm, it is important to keep the electric field less than 4 MV/cm because of reliability issues [4]. Therefore, the gate oxide electric field should be dealt with carefully when the MOSFET structure is designed.

The second major issue in the 4H-SiC MOSFET is the poor channel mobility. The high interface trap density, D$_{it}$ is observed at the interface between the 4H-SiC and thermally grown gate oxide (“B” in Figure 2.1) due to the C-atom dangling bonds [4]. In recent years, significant advances have been made with regards to the gate oxide process on the 4H-SiC. Most notably, high temperature post oxidation annealing process (POA) using nitric oxide (NO) or nitrogen dioxide (NO$_2$) helps to reduce the D$_{it}$, which improves the channel mobility. The nitrided oxide technique, therefore, has been used for the gate oxidation process by most SiC MOSFET developers [5]. Nevertheless, the improved channel mobility is much smaller than the bulk mobility. In addition, there is a trade-off between the channel mobility and threshold voltage [6]. Therefore, it is still the major performance limiting factor in the 4H-SiC MOSFETs.

Figure 2.1. Half-cell cross-sectional view of the 4H-SiC MOSFET structure [2].
1.2. Inversion vs. Accumulation Channels

Due to the wide energy bandgap property of 4H-SiC, two different channel modes can be designed: inversion mode channel (Inv) and accumulation mode channel (Acc) designs. Detailed information on the design of the channels to achieve a reasonable threshold voltage and field effect mobility will be discussed in the following sections. The Inv-channel MOSFET (InvFET) and Acc-channel MOSFET (AccFET) cross-sectional views are shown in Figure 2.2(a) and (b), respectively [1][2]. For the Acc-channel, constant n-type doping near the top surface needs to be designed to assure accumulation mode operation. The n-type Acc-channel is completely depleted by the built-in potential of the junction with the P+ shielding region underneath the n-type channel (Figure 2.2(b)), creating a potential barrier for electrons at zero gate bias in the blocking mode [1][2][7]. Current transport in the channel occurs with positive gate bias induced accumulation layers to create an enhancement mode device.

![INVERSION-MODE MOSFET](#)

![ACCUMULATION-MODE MOSFET](#)

Figure 2.2. Cross-sectional views [2] of the (a) Inversion-mode channel MOSFET (InvFET), (b) Accumulation-mode channel MOSFET (AccFET).

Field effect channel mobilities of 4H-SiC AccFETs and InvFETs at high temperatures are shown in Figure 2.3(a) [6]. The channel mobilities were measured from lateral MOSFET structures at high temperatures up to 200°C. It indicates that the channel mobility for the Acc-channel structures is over 20 cm²/Vs at room temperature, which is about 2 times higher than that of the
Inv-channel structures. In addition, both Acc- and Inv-channel mobilities increase as temperature rises as shown in Figure 2.3(a). The increase in absolute value of the channel mobility is about the same for both structures. The higher channel mobility for the AccFETs improves the channel resistance, leading to the reduced total specific on-resistance when compared to the InvFETs [6].

It should be noted that there is a trade-off between the channel mobility and threshold voltage. A clear correlation between the channel mobility and threshold voltage has been found for both AccFETs and InvFETs as shown in Figure 2.3(b) [6]. This result indicates that the AccFETs can have larger channel mobility at an acceptable threshold voltage with the carefully designed channel structure.

Figure 2.3. (a) Field effect channel mobilities of SiC AccFETs and InvFETs at high temperatures, (b) Trade-off between channel mobility and threshold voltages [6].

Figure 2.4 shows the electrostatic potential simulation results near the gate oxide interface along with X dimension for (a) Acc and (b) Inv MOSFETs with the channel length of 0.3 μm at V_d=1200 V and V_g=0 V. The channel barriers are shown in the figure. The results indicate that Acc-channel MOSFETs have smaller channel barriers than Inv-channel devices, resulting in inevitable larger leakage current inherently [1]. Although the AccFETs have a little bit higher leakage current than InvFETs due to the smaller channel barrier, that is still well below the standard
industry leakage current of 100 µA. These behaviors will be discussed in detail with experimental results in the next chapter.

2. Structure Optimization

Asmita Saha and James A. Cooper have published a research paper regarding the 1 kV-rated 4H-SiC power MOSFET structure optimization in 2007 as shown in Figure 2.5 [8]. The study
mainly focused on reducing the on-resistance ($R_{on}$) with optimization of the JFET region, current spreading layer (CSL), and source contact area using a figure-of-merit, defined as $[BV^2/R_{on,sp}]$, where $R_{on,sp}$ is $R_{on}$ multiplied by a device active area. However, other important electrical characteristics such as capacitance and gate charge are not discussed in the paper. For the improved high speed and high frequency capability in the SiC MOSFETs, it is necessary to reduce the reverse transfer capacitance ($C_{gd}$) and gate-to-drain charge ($Q_{gd}$) as well as the $R_{on}$ by conducting the structural optimization as mentioned in the previous chapter.

2.1. JFET Region Optimization

In this chapter, the optimization of the JFET region for the conventional planar MOSFET will be mainly focused with emphasis on HF-FOMs, $[R_{on} \times C_{gd}]$ and $[R_{on} \times Q_{gd}]$, because the JFET region optimization has a direct impact on $C_{gd}$ and $Q_{gd}$ as well as $R_{on}$ as shown in (2.3), (2.4), and (2.5) below [1][2];

\[
C_{gd} = W_{JFET} \cdot Z_{Cell} \cdot \left( \frac{C_{OX} C_{S,M}}{C_{OX} + C_{S,M}} \right) \tag{2.3}
\]

\[
Q_{gd} = \int C_{gd}(V_d) \, dV_d \tag{2.4}
\]

\[
R_{JFET} \propto \frac{\rho_{JFET}}{W_{JFET} - W_{dep.}} \left( \text{where, } W_{dep.} = \sqrt{\frac{2\varepsilon_S V_{bi}}{qN_{JFET}}} \right) \tag{2.5}
\]

where $W_{JFET}$ is the JFET width (shown in Figure 2.6), $Z_{Cell}$ is the unit cell length orthogonal to the cross section. $C_{OX}$ and $C_{S,M}$ are the gate oxide capacitance and semiconductor capacitance, respectively. $\rho_{JFET}$ is the JFET region resistivity, $W_{dep.}$ is the depletion width (shown in Figure 2.6),
\( \varepsilon_S \) is the SiC dielectric constant, \( V_{bi} \) is the built-in potential, and \( N_{JFET} \) is the JFET region doping concentration. As shown in (2.3) and (2.4), the \( C_{gd} \) is proportional to the \( W_{JFET} \) and the \( Q_{gd} \) is directly related to the \( W_{JFET} \) because the \( Q_{gd} \) is obtained by the integral of the \( C_{gd} \) with respect to \( V_d \) (Drain voltage). Therefore, the reduced \( C_{gd} \) and \( Q_{gd} \) can be achieved with the narrower JFET width. In addition to the \( C_{gd} \) and \( Q_{gd} \), the narrow \( W_{JFET} \) helps to reduce the gate oxide electric field by a screening effect of the \( P^+ \) shielding region [1].

However, the narrow \( W_{JFET} \) increases the \( R_{on} \). The \( R_{on} \) consists of source and drain contact resistance (\( R_C \)), \( N^+ \) source resistance (\( R_S \)), channel resistance (\( R_{CH} \)), JFET resistance (\( R_{JFET} \)), drift resistance (\( R_{DR} \)), and substrate resistance (\( R_{SUB} \)) as shown in Figure 2.6 [2]. The \( R_{JFET} \) is inversely proportional to the \( W_{JFET} \) (2.5), so the narrow \( W_{JFET} \) has a bad effect on the electron flow in the JFET region, which causes the increase of the \( R_{on} \). By increasing the doping concentration in the JFET region (\( N_{JFET} \)), the \( R_{on} \) can be maintained low at the narrower JFET width due to the reduced \( \rho_{JFET} \) and \( W_{dep} \) as shown in (2.5).

Therefore, the JFET optimization should be carried out in accordance with the balance between the JFET width and JFET doping concentration to achieve the optimized \( C_{gd} \), \( Q_{gd} \), gate oxide electric field less than 4 MV/cm, and \( R_{on} \).
2.2. Analysis with Analytical Models

In this section, the $R_{on,sp}$ of the conventional linear cell SiC MOSFET structures with various $W_{JFET}$ is analyzed using the analytical models which are available in [1][2]. Among the numerous series resistance components mentioned earlier, the only $R_{ch,sp}$, $R_{drift,sp}$, and $R_{JFET,sp}$ will be considered because they are the major contribution sources to the $R_{on}$ [9].

![Cross-sectional view of the 1.2 kV-rated 4H-SiC MOSFET](image)

Figure 2.7. Cross sectional view of the 1.2 kV-rated 4H-SiC conventional Acc-or Inv-channel MOSFETs with pertinent structural information. The $P^+$ contact is in the orthogonal direction to the cross-section to reduce the cell pitch ($W_{Cell}$). For the analytical calculations, the channel mobility ($\mu_{ch,FE}$) of 21 cm$^2$/V·s for the Acc-channel or 13 cm$^2$/V·s for the Inv-channel structure measured at room temperature is used as discussed in the previous section (Figure 2.3(a)). The analytical models for the $R_{ch,sp}$, $R_{drift,sp}$, and $R_{JFET,sp}$ are as below [1][2];

\[
R_{ch,sp} = \frac{L_{CH} \cdot W_{Halfcell}}{\mu_{CH,FE} \cdot C_{OX} (V_g - V_{th})} \quad [\Omega \cdot \text{cm}^2] \tag{2.6}
\]
\[ R_{\text{drift,sp}} = \rho_{\text{Drift}} \cdot W_{\text{Halfcell}} \cdot \ln \left( \frac{W_{\text{Halfcell}}}{W_{\text{JFET}} - W_{\text{dep}}} \right) + \rho_{\text{Drift}} (t - (W_{\text{Halfcell}} - W_{\text{JFET}} - W_{\text{dep}})) \quad [\Omega \cdot \text{cm}^2] \quad (2.7) \]

\[ R_{\text{JFET,sp}} = \frac{\rho_{\text{JFET}} \cdot t_{p^+} \cdot W_{\text{Cell}}}{W_{\text{JFET}} - W_{\text{dep}}} \quad [\Omega \cdot \text{cm}^2] \quad (2.8) \]

where \( C_{\text{OX}} \) is the oxide capacitance, \( V_g \) is the applied gate voltage, \( V_{\text{th}} \) is the threshold voltage, \( \rho_{\text{JFET}} \) is the resistivity of the JFET region, \( t_{p^+} \) is the junction depth of the P\(^+\) shielding region, \( W_{\text{dep}} \) is the depletion width in the JFET region, \( \rho_{\text{Drift}} \) is the resistivity of the drift region, and \( t \) is the drift region thickness.

The analytically calculated \( R_{\text{on,sp}} \) with \( R_{\text{ch,sp}}, \ R_{\text{drift,sp}}, \) and \( R_{\text{JFET,sp}} \) for the conventional Acc-channel MOSFETs having the various \( W_{\text{JFET}} \) is plotted in Figure 2.8. The analytical calculations for the structures without \( (N_{\text{JFET}} = 8 \times 10^{15} \text{ cm}^{-3}) \) and with the enhanced JFET doping concentration \( (N_{\text{JFET}} = 3 \times 10^{16} \text{ cm}^{-3}) \) are shown in Figure 2.8(a) and (b), respectively. As expected, the \( R_{\text{on,sp}} \) is increased when the \( W_{\text{JFET}} \) is reduced because the \( R_{\text{JFET,sp}} \) and \( R_{\text{drift,sp}} \) are increased. The increase of

Figure 2.8. Analytically calculated \( R_{\text{on,sp}} \) with \( R_{\text{ch,sp}}, \ R_{\text{drift,sp}}, \) and \( R_{\text{JFET,sp}} \) for the conventional MOSFETs having various \( W_{\text{JFET}} \) and \( N_{\text{JFET}} \) of (a) \( 8 \times 10^{15} \text{ cm}^{-3} \) and (b) \( 3 \times 10^{16} \text{ cm}^{-3} \).
the \( R_{\text{drift,sp}} \) with the narrower \( W_{\text{JFET}} \) is resulted from current spreading for the current conduction below the \( P^+ \) shielding region \([1][2]\). The increased \( R_{\text{JFET,sp}} \) and \( R_{\text{drift,sp}} \) with narrower \( W_{\text{JFET}} \) can be mitigated by the enhanced JFET doping of \( 3\times10^{16} \ \text{cm}^{-3} \) as shown in Figure 2.8(b). Thereby, the total \( R_{\text{on,sp}} \) for the MOSFETs with narrow \( W_{\text{JFET}} \) can be kept low.

The measured \( \mu_{\text{CH,FE}} \) from the lateral Acc and Inv mode MOSFET structures with \( L_{\text{CH}} \) of 200 \( \mu\text{m} \) \([6]\) is compared with the analytically calculated drift region mobility (\( \mu_{\text{Drift}} \)) up to 150°C in Figure 2.9 \([9]\). The \( \mu_{\text{Drift}} \) was calculated using \([4]\);

\[
\mu_{\text{Drift}} = \frac{1020}{1 + (N_{\text{Drift}}/1.8\times10^{17})^{0.6}} \left( \frac{T}{300} \right)^{-2.7} \text{cm}^2/\text{V} \cdot \text{s}
\]  

(2.9)

where \( N_{\text{Drift}} \) is the drift region doping concentration and \( T \) is the junction temperature. The \( \mu_{\text{Drift}} \) decreases rapidly, while the measured \( \mu_{\text{CH,FE}} \) for both of the Acc and Inv structures increases, with increasing temperature as shown in Figure 2.9.
Figure 2.10 compares the calculated $R_{ch}$, $R_{JFET}$, and $R_{drift}$ components using analytical models for Acc and Inv MOSFETs with various JFET widths at (a) 25°C and (b) 150°C. The contribution of $R_{JFET}$ and $R_{drift}$ to $R_{on}$ becomes larger than $R_{ch}$ at narrower JFET width. The impact is greater in the Acc structures [9].

Figure 2.10 compares the calculated $R_{ch}$, $R_{JFET}$, and $R_{drift}$ resistances for Inv and Acc MOSFETs with various $W_{JFET}$ and enhanced $N_{JFET}$ ($3 \times 10^{16}$ cm$^{-3}$) at (a) 25°C and (b) 150°C [9]. The $R_{JFET}$ and $R_{drift}$ increase with temperatures due to a reduction in bulk mobility, while the $R_{ch}$ decreases due to an increase in channel mobility (Figure 2.9). Consequently, the contribution of $R_{JFET}$ and $R_{drift}$ to $R_{on}$ becomes larger from 25°C to 150°C for both of the Acc and Inv MOSFETs as shown in Figure 2.10(a) and (b), leading to an increase of $R_{on}$ at 150°C.

Analytically calculated increase in the ratio $[R_{on}(150°C)/R_{on}(25°C)]$ for Acc and Inv MOSFETs with various JFET widths is shown in Figure 2.11 [9]. The ratio becomes greater with narrower JFET width for both of the MOSFETs because of the bigger $R_{JFET}$ and $R_{drift}$ portions as shown in Figure 2.11. In addition, the increase in the ratio is smaller in the Inv structures than in the Acc structures overall due to more balanced $R_{JFET}$, $R_{drift}$, and $R_{ch}$ with increasing temperature. These analytical calculations will be compared with the actual experimental data in the following section.
2.3. TCAD Numerical Simulations

TCAD numerical simulations were performed for the 1.2 kV-rated SiC conventional planar power MOSFETs. All the structures have the Acc-channel and same structural parameters except for the WJFET and N_JFET as described in Figure 2.7.

The Breakdown Voltage (BV) simulations were conducted as a function of the N_JFET and W_JFET with the oxide field limitation of 4 MV/cm as shown in Figure 2.12(a). The BV of 1700 V was observed for the devices with the W_JFET of 0.6 µm regardless of the N_JFET. However, when the W_JFET becomes large, the BV with the higher N_JFET gets reduced because of the oxide field limitation. Therefore, the N_JFET less than 4×10^16 cm^-3 is required to achieve the high enough BV for the structures with wide W_JFET.

The oxide electric field should be carefully examined to determine the W_JFET because the electric field at the gate oxide increases with enhanced JFET doping as already discussed in Figure 2.12(a). The oxide electric field simulations for the structures with the enhanced JFET doping of 3×10^16 cm^-3 were performed at V_d of 1600 V as shown in Figure 2.12(b). In order to keep the oxide...
electric field less than 4 MV/cm, the $W_{JFET}$ should be kept less than 1 µm.

Figure 2.13 compares the $R_{on,sp}$ (Figure 2.13(a)), $Q_{gd,sp}$, $C_{gd,sp}$, and HF-FOMs (Figure 2.13(b)) obtained from the simulations. The simulated $R_{on,sp}$ does not include any substrate and contact resistance. As shown in Figure 2.13(a), $R_{on,sp}$ is maintained low at the narrower $W_{JFET}$ by increasing the doping concentration in the JFET region as discussed in the previous section. The
minimum $R_{on,sp}$ is found at $W_{JFET}=0.9 \, \mu m$ with the enhanced $N_{JFET}$ of $3 \times 10^{16} \, cm^{-3}$ and $W_{JFET}=1.1 \, \mu m$ without the enhanced JFET doping, respectively.

Figure 2.13(b) shows that the narrow JFET width reduces significantly the $C_{gd,sp}$ and $Q_{gd,sp}$ as expected. Although the best HF-FOMs are observed at $W_{JFET}=0.3 \, \mu m$ as shown in Figure 2.13(b), the $R_{on,sp}$ increases substantially when $W_{JFET}$ is decreased to 0.3 \, \mu m. An optimum $W_{JFET}$ is, therefore, determined to be 0.7 \, \mu m in order to keep the gate oxide electric field below 4 MV/cm for reliability and to obtain a low $R_{on,sp}$ with taking into account the lateral straggle of the P+ shielding region during the ion implantation process, simultaneously.

3. Fabrication of 1.2 kV 4H-SiC Planar-Gate MOSFETs

3.1. Structure Information

Based up on the TCAD numerical simulation in the previous section, the optimum $W_{JFET}$ and $N_{JFET}$ for the 1.2 kV 4H-SiC planar-gate MOSFET structures are 0.7 \, \mu m and $3 \times 10^{16} \, cm^{-3}$. For comparison of the electrical characteristics, the MOSFET structures with $W_{JFET}$ of 0.7, 1.1, 1.5 \, \mu m, and with and without the enhanced $N_{JFET}$ are designed for the actual fabrication [10]. Table 2.1 summarizes the structure design variations [10]. The number in the device name represents the designed JFET width and “J” next to the device name indicates that the structures have the enhanced JFET doping concentration of $3 \times 10^{16} \, cm^{-3}$. The cell pitch ($W_{Cell}$) is changed with the different $W_{JFET}$ as shown in Table 2.1.

The 1.2 kV MOSFETs can have the accumulation mode (Acc) or inversion mode (Inv) channels. As shown in Figure 2.14, the n-type Acc-channel and p-type Inv-channel are carefully designed using the TCAD numerical simulations [6][10]. The Acc-channel is designed to assure the completely depleted N-base layer by the P+ shielding region underneath so that current
transport in the channel occurs with positive gate bias induced the accumulation layers [1][2][7].

The doping profile near the SiC surface was optimized by the numerical simulations in order to accomplish reasonable threshold voltage with high channel mobility [6]. The enhanced \( N_{JFET} \) profile is also shown in the figure. The designed junction depth of the P+ shielding region is about 0.65 \( \mu m \).

<table>
<thead>
<tr>
<th>Device name</th>
<th>( N_{JFET} ) [cm(^{-3})]</th>
<th>( W_{JFET} ) [( \mu m )]</th>
<th>( W_{cell} ) [( \mu m )]</th>
</tr>
</thead>
<tbody>
<tr>
<td>MOSFET_0.7</td>
<td>( 8 \times 10^{15} ) (No enhanced doping)</td>
<td>0.7</td>
<td>2.8</td>
</tr>
<tr>
<td>MOSFET_1.1</td>
<td>( 3 \times 10^{16} )</td>
<td>1.1</td>
<td>3.2</td>
</tr>
<tr>
<td>MOSFET_1.5</td>
<td>( 3 \times 10^{16} )</td>
<td>1.5</td>
<td>3.6</td>
</tr>
</tbody>
</table>

Table 2.1. Design variations of JFET widths and doping concentrations [10].

Figure 2.14. Designed implant profiles for Acc- and Inv-channel, and enhanced JFET. Series implants of Aluminum and Nitrogen were used, respectively [6][10].
3.2. Hybrid-JTE Edge Termination

A hybrid-junction termination extension (Hybrid-JTE) was designed to provide high reliable breakdown voltages over a wide range of JTE doses [11]. The Hybrid-JTE edge termination consists of two main parts: (i) the ring-assisted JTE (RA-JTE) and (ii) the multiple floating field ring JTE (MFZ-JTE) as shown in Figure 2.15. The RA-JTE is used to relieve the electric field at the main P+ junction so that high breakdown voltage can be sustained at low JTE doses. The MFZ-JTE structure placed next to the RA-JTE plays a role of the high electric field mitigation at high JTE doses to maintain high breakdown voltage. For the RA-JTE, 4 µm-wide P+ rings are placed in the 60 µm-wide single zone JTE (SZ-JTE) structure [10]. The spaces among the P+ rings have the relationship of \( S_n = S_1 + (n-1) \). For the MFZ-JTE, a gradual charge distribution is achieved by controlling the width of the discrete implanted regions as shown in Figure 2.15. The width of each discrete charge zone (\( W_n \)) has the relationship of \( W_n = W_1 / \alpha^{(n-1)} \). There are 12-zone in the 60 µm wide MFZ-JTE that is optimized at \( \alpha = 1.05 \) [10]. The P+ rings for the RA-JTE are formed during the P+ contact implant process simultaneously. The discrete charge zones for the MFZ-JTE and SZ-JTE are formed by a series of Al implant process. Therefore, only one extra mask step is required for the JTE implant to make the Hybrid-JTE edge termination [10][11].

The TCAD numerical breakdown voltage simulations with the Hybrid-JTE as a function

![Figure 2.15. Cross-sectional view of the Hybrid-JTE edge termination. The termination consists of RA-JTE and MFZ-JTE to achieve reliable breakdown voltage [10].](image-url)
of JTE dose are shown in Figure 2.16 [10]. For comparison, the simulations for the conventional SZ-JTE edge termination design were also conducted. It is found that the high breakdown voltage over 1600 V was achieved for the JTE doses from $1 \times 10^{13}$ to $3 \times 10^{13}$ cm$^{-2}$ with the Hybrid-JTE design, while the breakdown voltage with the SZ-JTE edge termination shows over 1600 V only at $1.4 \times 10^{13}$ cm$^{-2}$ as shown in Figure 2.16.

### 3.3. Layout Description

Figure 2.17 shows a layout designed for the Power America (PA) project - Budget Period 2 (BP2). Various devices such as PiN diodes, Ni & Ti JBS diodes, 1.2 kV conventional planar-gate power MOSFETs, and 1.2 kV planar-gate power JBSFETs [12][13] were designed by Dr. Woongje Sung [14] and one 1.2 kV Split-Gate (SG) power MOSFET [15] was designed by me for the PA BP2 1st lot. The SG-MOSFET will be discussed in Chapter 3. Among 5×5 different structures, total 11 conventional planar-gate power MOSFETs with different structural parameters were included as shown in Figure 2.17. Specifically, “MOS8”, “MOS9”, and “MOS11” designs are compared to each other in this chapter for the JFET region optimization research. They have
the exactly same structural parameters except for the JFET width. The $W_{\text{JFET}}$ for “MOS8”, “MOS9”, and “MOS11” is 1.5, 1.1, and 0.7 µm, respectively.

### 3.4. Process Flow

All the devices were fabricated at a 6-inch foundry, X-Fab, using the NCSU PRESiCE™ process [16] as discussed in the previous chapter. I supervised the wafer fabrication at X-Fab because Dr. Woongje Sung left NCSU.
4H-SiC Si-face (0001) 6-inch wafers with n-type epitaxial layer (doping $8 \times 10^{15}$ cm$^{-3}$, thickness 10 μm, and 4° tilted toward <1120>) were used as the starting material. The fabrication process flow is briefly described in Figure 2.18:

![Fabrication process flow for the Acc 1.2 kV 4H-SiC conventional planar-gate MOSFETs.](image)

The zero alignment mark was etched (Mask 1). The enhanced JFET (Mask 2), Acc- (or Inv-) channel and $P^+$ shielding (Mask 3), $P^+$ JTE for the edge termination regions (Mask 4), $P^+$ contact (Mask 5), and $N^+$ source (Mask 6) were formed by a series of implants of N and Al. A 10-min implant activation anneal was conducted at 1650°C with a carbon cap after all the ion implantation steps. A 50 nm thick gate oxide was grown by dry oxidation at 1175°C, followed by NO interface annealing. A 500 nm N-type poly-Si gate was deposited and patterned (Mask 7), followed by oxide interlayer dielectric deposition. NiSi ohmic contact process was conducted with an RTA on the both front and backsides (Mask 8). The oxide interlayer dielectric on the poly-Si was etched for
the gate contact (Mask 9). Al-based metal was deposited and patterned for the source and gate pads (Mask 10). Passivation layers (Nitride and Polyimide) were stacked and patterned on the front side (Mask 11). A solderable metal stack was lastly deposited on the backside. A total 11-mask set was used for the fabrication if the enhanced JFET implantation was included. The active area for all the devices is 0.045 cm². The same hybrid JTE edge termination design [11] was used for the 1.2 kV conventional planar-gate power MOSFETs.

4. Experimental Results and Discussions

4.1. Experimental Results

All the devices shown in Table 2.1 were successfully fabricated at the 6-inch foundry, X-Fab. All experimental measurements were done by me because Dr. Woongje Sung left NCSU. Figure 2.19 shows a SEM image for the cross sectional view of the fabricated 1.2 kV Acc-channel planar-gate MOSFET structure with W_{JFET} of 0.7 μm. The shining P⁺ shielding regions are clearly

![Image](image-url)

**Figure 2.19.** SEM cross-sectional image for the fabricated 1.2 kV SiC Acc-channel planar-gate power MOSFET with W_{JFET} of 0.7 μm.
Figure 2.20. Typical output characteristics for Acc MOSFET_J_0.7 and MOSFET_1.1 measured at $V_g$ from 0 to 25 V with 5 V steps at room temperature [10].

Figure 2.21. Wafermaps of $R_{on,sp}$ for Acc MOSFET_J_0.7 [10] and MOSFET_1.1 extracted at $V_g$ of 20 V and $I_d$ of 10 A from 60 devices each.
observed due to the reflection of electron beam against the implanted Al elements [17]. It is found that the MOSFET structure was very well defined through the fabrication process described in the previous section.

All the fabricated devices were measured using the semi-automatic Signatone Probestation and Keysight B1505A Curve Tracer with the provided standard measurement methods. Wafermaps and statistical distributions were created with the measured data using macro programs.

Figure 2.20 shows typical output characteristics of fabricated Acc MOSFET_J_0.7 ($N_{JFET}=3\times10^{16}$ cm$^{-3}$ and $W_{JFET}=0.7$ µm) and Acc MOSFET_1.1 (without enhanced JFET doping and $W_{JFET}=1.1$ µm) measured at $V_g$ from 0 to 25 V with 5 V step [10]. As expected from the TCAD numerical simulations shown in the section 2.3, the MOSFET_J_0.7 shows the better on-resistance compared with the MOSFET_1.1 structure due to the enhanced JFET doping. The wafermaps for the specific-on-resistance ($R_{on,sp}$) of the Acc MOSFET_J_0.7 and MOSFET_1.1 from all 60 dies

![Graph of typical transfer characteristics](image)

Figure 2.22. Typical transfer characteristics for Acc MOSFET_J_0.7 and MOSFET_1.1 measured at $V_d$ of 0.1 V at room temperature.
were extracted at $V_g=20\ \text{V}$ and $I_d=10\ \text{A}$ as shown in Figure 2.21. The MOSFET_J_0.7 and MOSFET_1.1 have the excellent statistical distribution with average $R_{on,sp}$ of 6.35 and 6.63 m$\Omega$-$\text{cm}^2$ and standard deviation of 0.20 and 0.18, respectively. It is noteworthy that 1.7 m$\Omega$-$\text{cm}^2$ parasitic resistance ($R_{\text{sub}}$: 0.7 and $R_{\text{probing}}$: 1 m$\Omega$-$\text{cm}^2$) is included in the results. The $R_{on}$ for the other fabricated Acc MOSFET structures are summarized in Table 2.2.

The typical transfer characteristics of the fabricated Acc MOSFET_J_0.7 and MOSFET_1.1 measured at room temperature are shown in Figure 2.22. The threshold voltages ($V_{th}$) are extracted at $V_d=0.1\ \text{V}$ and $I_d=1\ \text{mA}$ as marked with the red dot line in the figure. They have the same $V_{th}$ within the experimental error. Figure 2.23 shows the wafermaps for $V_{th}$ of the Acc MOSFET_J_0.7 and MOSFET_1.1 measured from all 60 dies. They have the excellent
Figure 2.24. Typical reverse transfer capacitance ($C_{gd}$) for Acc MOSFET_J_0.7 and MOSFET_1.1 measured at room temperature.

Figure 2.25. Wafermaps of $C_{gd}$ for Acc MOSFET_J_0.7 \[^{10}\] and MOSFET_1.1 extracted at $V_d$ of 1000 V from 60 devices each.
statistical distribution with average $V_{th}$ of 2.00 and 1.89 V and standard deviation of 0.10 and 0.16, respectively. The $V_{th}$ values for the other fabricated Acc devices are summarized in Table 2.2.

The measured reverse transfer capacitance ($C_{gd}$) of the fabricated Acc MOSFET J_0.7 and MOSFET_1.1 can be compared in Figure 2.24. The $C_{gd}$ at $V_d=1000$ V for the Acc MOSFET J_0.7 is smaller than that for the Acc MOSFET_1.1 because the $C_{gd}$ is proportional to the JFET width as discussed earlier in (2.3). Therefore, the measured $C_{gd}$ data is consistent with the analytical models. Figure 2.25 shows the wafermaps for the $C_{gd}$ of the Acc MOSFET J_0.7 and MOSFET_1.1 extracted at $V_d=1000$ V from all 60 dies. The average $C_{gd}$ is 4.95 and 8.28 pF with the standard deviation of 0.27 and 0.21 for the Acc MOSFET J_0.7 and MOSFET_1.1, respectively. The $C_{gd}$ values for the other fabricated Acc devices are summarized in Table 2.2.

![Figure 2.26](image.png)

Figure 2.26. Typical measured gate-to-drain charge ($Q_{gd}$) for Acc MOSFET J_0.7 and MOSFET_1.1 at $V_d$ of 800 V and $I_d$ of 10 A at room temperature.

The typical gate charge waveforms measured at $V_d=800$ V and $I_d=10$ A are shown in Figure 2.26 for the Acc MOSFET J_0.7 and MOSFET_1.1. The extracted $Q_{gd}$ values at a plateau (marked in the figure) are 15.8 nC for the MOSFET J_0.7 and 18.5 nC for the MOSFET_1.1, respectively. The $Q_{gd}$ for the Acc MOSFET J_0.7 is also smaller compared with the Acc MOSFET_1.1 due to
the narrower $W_{\text{JFET}}$ as discussed in (2.4). The $Q_{\text{gd}}$ values for the other fabricated Acc devices are summarized in Table 2.2.

It is particularly important to investigate the blocking capability of the 1.2 kV SiC planar-gate power MOSFETs with the enhanced JFET doping concentration. Figure 2.27 compares the

![Figure 2.27. Comparison of blocking capability. MOSFETs with narrower JFET widths (MOSFET_J_0.7) show lower leakage currents [10].](image)

10^{-5} \quad 10^{-4}

Figure 2.27. Comparison of blocking capability. MOSFETs with narrower JFET widths (MOSFET_J_0.7) show lower leakage currents [10].

the narrower $W_{\text{JFET}}$ as discussed in (2.4). The $Q_{\text{gd}}$ values for the other fabricated Acc devices are summarized in Table 2.2.

It is particularly important to investigate the blocking capability of the 1.2 kV SiC planar-gate power MOSFETs with the enhanced JFET doping concentration. Figure 2.27 compares the

![Figure 2.28. Cumulative distribution of leakage current measured from total 60 dies on a 6-inch wafer at $V_d=1000$ V, $V_g=0$ V at room and high temperature (175°C) [10].](image)

Figure 2.28. Cumulative distribution of leakage current measured from total 60 dies on a 6-inch wafer at $V_d=1000$ V, $V_g=0$ V at room and high temperature (175°C) [10].

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blocking characteristics of 5 randomly chosen Acc MOSFET_J_0.7 and MOSFET_1.1 among 60 dies each on a 6-inch wafer [10]. As shown, it is confirmed that the enhanced JFET doping does not degrade the breakdown voltage at I_d of 100 μA. Furthermore, it is observed that the MOSFET structure with the narrower JFET width that was accomplished by the enhanced JFET doping (MOSFET_J_0.7) actually reduces the leakage currents. In order to examine the results more carefully, the leakage currents were measured for both MOSFET_J_0.7 and MOSFET_1.1 from total 60 dies each at V_d of 1000 V and room and high temperature (175°C) as shown in Figure 2.28 [10]. The MOSFET_1.1 shows overall the higher leakage current compared to the MOSFET_J_0.7, but its magnitude is still much smaller than the allowable typical maximum leakage current of 100 μA in datasheets. The observed higher leakage current for the MOSFET_1.1 is due to the higher electric field in the JFET region with wider JFET width as discussed earlier. This tendency is kept at both room and high temperature (175°C) as shown in Figure 2.28.

In order to compare the electrical performance between the Acc- and Inv-channel MOSFETs with the enhanced N_{JFET}, the output characteristics for the fabricated Acc and Inv

![Figure 2.29. Normalized R_{on} from measured output characteristics of the fabricated Acc and Inv-channel SiC MOSFETs with different JFET widths (0.7, 1.1, 1.5 μm) [9].]
MOSFETs with various JFET widths were measured at higher temperatures up to 150°C [9]. As expected, the Acc MOSFETs show lower $R_{on}$ due to the higher channel mobility as explained in the previous section. When it comes to the increase in the ratio $[R_{on}(150^\circ C)/R_{on}(25^\circ C)]$, however, the Inv devices have smaller increase as shown in Figure 2.29 [9]. It shows the measured normalized $R_{on}$ ($V_g=20$ V, $I_d=10$ A) as a function of temperature for the fabricated Acc and Inv MOSFETs with various $W_{JFET}$ (0.7, 1.1, 1.5 $\mu$m) values. The results demonstrate that the smallest increase in the ratio $[R_{on}(150^\circ C)/R_{on}(25^\circ C)]$ can be achieved with the Inv MOSFET with largest $W_{JFET}$ (1.5 $\mu$m) as expected from Figure 2.10 and 2.11. The measured $R_{on}$ and the calculated ratio $[R_{on}(150^\circ C)/R_{on}(25^\circ C)]$ for all the fabricated Acc and Inv devices are summarized in Table 2.3.

4.2. Discussions

All the experimental results for the fabricated 1.2 kV 4H-SiC Acc-channel planar-gate MOSFET structures with the $W_{JFET}$ of 0.7, 1.1, 1.5 $\mu$m, and with and without the $N_{JFET}$ of $3\times10^{16}$ cm$^{-3}$ are summarized in Table 2.2.

It is demonstrated that all the fabricated Acc devices have the same threshold voltage ($V_{th}$) of about 2 V within the experimental error, and the $V_{th}$ is in the acceptable range for enhancement mode operation.

All the structures show the excellent breakdown voltages over 1600 V at $I_d$ of 100 $\mu$A regardless of the enhanced $N_{JFET}$.

As expected from the analytical models and TCAD numerical simulations, the MOSFET structure with the narrow JFET width showed the very high on-resistance when it did not receive the enhanced $N_{JFET}$ (MOSFET_0.7). The increased JFET doping (MOSFET_J_0.7) ensures the on-resistance is kept as low as other structures (MOSFET_J_1.1 and MOSFET_J_1.5). It should
be noted that there is substantial parasitic resistance \( R_{\text{sub}} \approx 16 \, \text{m} \Omega \) + \( R_{\text{probing}} \approx 22 \, \text{m} \Omega \) included in the results.

It can be observed that the MOSFETs with the same \( W_{\text{JFET}} \) have the same \( C_{gd} \) and \( Q_{gd} \) values within the experimental error regardless of the enhanced \( N_{\text{JFET}} \) since the JFET width directly determines them as discussed in the previous section.

As the JFET width has a direct impact on the \( C_{gd} \) and \( Q_{gd} \), it is concluded that the enhanced JFET doping allows the small \( C_{gd} \) and \( Q_{gd} \) as well as the low on-resistance, resulting in an improved HF-FOMs as shown in Table 2.2. Therefore, it has been experimentally demonstrated that about 1.7× and 1.2× reduction in the HF-FOM \( R_{\text{on}} \times C_{gd} \) and HF-FOM \( R_{\text{on}} \times Q_{gd} \) could be achieved in the Acc MOSFET_\text{J}_0.7 by the JFET region optimization compared with the Acc MOSFET_1.1.

### Table 2.2. Experimental results for 1.2 kV Acc MOSFET structures with and without the enhanced \( N_{\text{JFET}} \).

<table>
<thead>
<tr>
<th></th>
<th>( W_{\text{cell}} ) [( \mu \text{m} )]</th>
<th>( V_{\text{th}} ) ((I_d=1, \text{mA})) [V]</th>
<th>( B\text{V} ) ((I_d=100, \text{mA})) [V]</th>
<th>( R_{\text{on}} ) ((I_d=10, \text{A})) [m( \Omega )]</th>
<th>( C_{gd} ) ((V_d=1, \text{kV})) [pF]</th>
<th>( Q_{gd} ) [nC]</th>
<th>HF-FOM ( (R_{\text{on}} \times C_{gd}) ) [ns]</th>
<th>HF-FOM ( (R_{\text{on}} \times Q_{gd}) ) [m( \Omega \cdot \text{nC} )]</th>
</tr>
</thead>
<tbody>
<tr>
<td>MOSFET_0.7</td>
<td>5.6</td>
<td>1.89</td>
<td>1654</td>
<td>581</td>
<td>4.66</td>
<td>15.1</td>
<td>2706</td>
<td>8769</td>
</tr>
<tr>
<td>MOSFET_1.1</td>
<td>6.4</td>
<td>1.81</td>
<td>1655</td>
<td>147</td>
<td>8.28</td>
<td>18.5</td>
<td>1220</td>
<td>2725</td>
</tr>
<tr>
<td>MOSFET_1.5</td>
<td>7.2</td>
<td>1.94</td>
<td>1652</td>
<td>146</td>
<td>11.3</td>
<td>20.5</td>
<td>1652</td>
<td>2997</td>
</tr>
<tr>
<td>MOSFET_\text{J} 0.7</td>
<td>5.6</td>
<td>2.00</td>
<td>1635</td>
<td>141</td>
<td>4.95</td>
<td>15.8</td>
<td>699 (1.7x)</td>
<td>2229 (1.2x)</td>
</tr>
<tr>
<td>MOSFET_\text{J} 1.1</td>
<td>6.4</td>
<td>2.04</td>
<td>1645</td>
<td>138</td>
<td>8.39</td>
<td>18.3</td>
<td>1158</td>
<td>2521</td>
</tr>
<tr>
<td>MOSFET_\text{J} 1.5</td>
<td>7.2</td>
<td>2.20</td>
<td>1647</td>
<td>143</td>
<td>11.3</td>
<td>20.4</td>
<td>1616</td>
<td>2920</td>
</tr>
<tr>
<td>Cree (C2M0160120D)</td>
<td>-</td>
<td>2.6</td>
<td>&gt;1200</td>
<td>160.0</td>
<td>4.0</td>
<td>14.0</td>
<td>640</td>
<td>2240</td>
</tr>
</tbody>
</table>

*\( R_{\text{on}} \) @ \( V_g=20 \, \text{V}, \, I_d=10 \, \text{A} \); includes \( R_{\text{sub}} \approx 16 \, \text{m} \Omega \) + \( R_{\text{probing}} \approx 22 \, \text{m} \Omega \)
All the experimental results measured at higher temperatures up to 150°C for the fabricated 1.2 kV 4H-SiC Acc- and Inv-channel planar-gate MOSFETs with the enhanced NJFET and various WJFET (0.7, 1.1, 1.5 µm) are summarized in Table 2.3.

In addition, all the electrical characteristics of the fabricated MOSFETs are compared with those of the typical commercial MOSFET (C2M0160120D [17]) in Table 2.2 and Table 2.3 [9].

The Acc-channel MOSFETs have lower Ron than the Inv-channel MOSFETs due to the higher channel mobility as discussed earlier.

It is found that the fabricated MOSFET structures with the same WJFET have the similar Cgd and Qgd values regardless of the channel types due to the identical JFET and drift region parameters.

Table 2.3. Experimental results for 1.2 kV Acc and Inv MOSFET structures with the enhanced N\textsubscript{JFET} [9].

<table>
<thead>
<tr>
<th>Wcell [µm]</th>
<th>Ron [mΩ]</th>
<th>Cgd [pF]</th>
<th>Qgd [nC]</th>
<th>FOM (Ron×Cgd) [mΩ⋅pF]</th>
<th>FOM (Ron×Qgd) [mΩ⋅nC]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Acc-0.7</td>
<td>5.6</td>
<td>141</td>
<td>204</td>
<td>1.45</td>
<td>4.95</td>
</tr>
<tr>
<td>Acc-1.1</td>
<td>6.4</td>
<td>138</td>
<td>177</td>
<td>1.28</td>
<td>8.39</td>
</tr>
<tr>
<td>Acc-1.5</td>
<td>7.2</td>
<td>143</td>
<td>179</td>
<td>1.25</td>
<td>11.3</td>
</tr>
<tr>
<td>Inv-0.7</td>
<td>5.6</td>
<td>166</td>
<td>223</td>
<td>1.34</td>
<td>5.25</td>
</tr>
<tr>
<td>Inv-1.1</td>
<td>6.4</td>
<td>163</td>
<td>189</td>
<td>1.16</td>
<td>8.64</td>
</tr>
<tr>
<td>Inv-1.5</td>
<td>7.2</td>
<td>172</td>
<td>182</td>
<td>1.06</td>
<td>11.7</td>
</tr>
<tr>
<td>C2M0160120D</td>
<td>-</td>
<td>160</td>
<td>290</td>
<td>1.83</td>
<td>4.0</td>
</tr>
</tbody>
</table>

*Ron @ Vg=20 V, Id=10 A; includes R\textsubscript{sub} (~16 mΩ) + R\textsubscript{probing} (~22 mΩ)
It has been reported that the \(C_{gd}\) and \(Q_{gd}\) values are unchanged with temperature [19][20]. Consequently, the measured \(C_{gd}\) and \(Q_{gd}\) values at room temperature can be used for the calculations of the HF-FOM \([R_{on} \times C_{gd}]\) and HF-FOM \([R_{on} \times Q_{gd}]\) at 150\(^\circ\)C. Thus, the calculated HF-FOMs for the Acc and Inv MOSFETs show exactly the same trend as \(R_{on}\) with temperature.

Although the Acc MOSFETs show a bigger increase in the HF-FOMs at higher temperature, its absolute values are still better than those of the Inv MOSFETs. The smallest ratio \([R_{on}(150\,^\circ\text{C})]/R_{on}(25\,^\circ\text{C})]\) is observed for the Inv MOSFET with the WJFET of 1.5 \(\mu\)m. Consequently, its HF-FOM \([R_{on} \times Q_{gd}]\) at 150\(^\circ\)C is 1.07\(\times\) better although its 25\(^\circ\)C HF-FOM \([R_{on} \times Q_{gd}]\) is worse than for the commercial device. The best HF-FOM \([R_{on} \times Q_{gd}]\) at 150\(^\circ\)C is observed for the Acc MOSFET with the WJFET of 0.7 \(\mu\)m. Although its 25\(^\circ\)C HF-FOM \([R_{on} \times Q_{gd}]\) is the same as the commercial device, its HF-FOM \([R_{on} \times Q_{gd}]\) at 150\(^\circ\)C is 1.26\(\times\) better.

5. Conclusions

The JFET region parameters for 1.2 kV rated SiC MOSFETs were optimized in order to improve the HF-FOMs. The enhanced NJFET allows the narrower WJFET and thus smaller \(C_{gd}\) and \(Q_{gd}\) without an increase in the on-resistance. The structures with the narrower WJFET and enhanced NJFET are also beneficial for reducing the leakage current in the blocking mode. It is therefore experimentally demonstrated that the enhanced NJFET is essential to improve the HF-FOMs and blocking behaviors of the 1.2 kV 4H-SiC MOSFETs.

The theoretical understanding and experimental demonstration of how to achieve a low ratio \([R_{on}(150\,^\circ\text{C})]/R_{on}(25\,^\circ\text{C})]\) for the 1.2 kV SiC planar MOSFETs have also been discussed. The electrical characteristics were measured from the fabricated 1.2 kV SiC Acc- and Inv-channel devices with the enhanced NJFET and compared with those for the commercially available
MOSFET. It was found that the Inv MOSFET with $W_{JFET}$ of 1.5 $\mu$m has the smallest ratio $[R_{on}(150^\circ C)/R_{on}(25^\circ C)]$ of 1.06 due to the balance of $R_{jfet}$, $R_{drift}$, and $R_{ch}$ with increasing temperature as expected from the analytical model. Both of the fabricated Acc and Inv MOSFETs show the smaller ratio $[R_{on}(150^\circ C)/R_{on}(25^\circ C)]$ compared with the commercially available MOSFET. The Acc MOSFET with the $W_{JFET}$ of 0.7 $\mu$m has better $[R_{on} \times C_{gd}]$ by 1.15$\times$ and $[R_{on} \times Q_{gd}]$ by 1.26$\times$ at 150$^\circ$C compared with the commercial MOSFET.
REFERENCES


CHAPTER 3.

Demonstration of 1.2 kV 4H-SiC Linear Cell Split-Gate MOSFETs (SG-MOSFET) with Superior Electrical Characteristics

1. Background & Motivation

There have been several approaches to improve the reverse transfer capacitance ($C_{gd}$), gate-to-drain charge ($Q_{gd}$), and high frequency figures-of-merit (HF-FOMs) for high speed switching capability with low energy consumption.

One of the approaches is the split gate poly-si structure, which can effectively reduce the $C_{gd}$ and $Q_{gd}$ because of the reduced gate-to-drain overlap. The silicon Split-Gate MOSFET (SG-MOSFET) structure has been previously proposed and demonstrated to reduce the $C_{gd}$ and improve the HF-FOM as shown in Figure 3.1(a) [1][2].

Another similar structure, Terraced-Gate (TG-MOSFET) MOSFET, has also been demonstrated to improve the electrical characteristics with the terraced gate structure reducing the gate-to-drain capacitance in the Si device as shown in Figure 3.2(b) [3].

Numerical simulation studies of a 4H-SiC SG-MOSFET structure have been recently presented in ISPSD 2016 [4]. However, their proposed structure contains a Schottky contact plus shallow P-layer in the JFET region which adds considerable fabrication complexity. The paper does not have any experimental validation for their analysis.

In the SG-MOSFETs, the high gate oxide electric field is concentrated at the edge of the split poly-Si gate. It is particularly important for SiC MOSFETs because of the gate oxide reliability [5][6][7] as mentioned in Chapter 2. Therefore, the gate oxide electric field study should
be associated carefully when it comes to the structure optimization for the 4H-SiC SG- and TG-MOSFETs.

In this chapter, the structure optimization with TCAD numerical simulations and experimental demonstration of the improved HF-FOMs for 1.2 kV 4H-SiC SG-MOSFETs will be discussed in detail.

2. Structure Optimization using TCAD Numerical Simulations

In this section, the 1.2 kV 4H-SiC SG-MOSFETs and TG-MOSFETs are analyzed using TCAD numerical simulations so that one of the structures is selected for fabrication based on the simulated electrical characteristics.

2.1. SiC Split-Gate vs. Terraced-Gate MOSFETs

Figure 3.2 shows a cross-sectional view of the conventional MOSFET, SG-MOSFET, and TG-MOSFET with the detailed structural parameters used in the TCAD numerical simulations [8].
In the simulations, the enhanced JFET doping concentration was not included as shown in Figure 3.2. All the structures have the accumulation mode channel (Acc-channel) [9]. The simulations were performed with various poly-Si gate overhang (X) into the JFET region (poly-Si gate length from the edge of channel) [8]. Therefore, when the X width is 0.9 µm, which is same as the JFET width, the structure becomes the conventional MOSFET. The electric field distribution at $V_d$ of 1200 V and $V_g$ of 0 V, shown in Figure 3.3 and 3.4(a), indicates that electric field is mainly concentrated at the edge of the poly-Si gate in the both SG and TG-MOSFETs. It was observed that the oxide electric field is suppressed by the P+ Shielding layer when X becomes small (Figure 3.3).

Figure 3.3. Simulation results of electric field distribution at $V_d$ of 1200 V for SG-MOSFET (left) and TG-MOSFET (right) with X of 0.5 µm [8].
3.4(a) left), and by proximity of the split poly-Si gates when X becomes large (Figure 3.4(a) right).

The maximum gate oxide electric field values were extracted from the simulations at $V_d$ of 1200 V and $V_g$ of 0 V and shown in Figure 3.4(b) as a function of X width. The maximum oxide electric field was 3 MV/cm at X of 0.5 µm for both the SG- and TG-MOSFETs.

Figure 3.5 compares the $Q_{gd,sp}$ and HF-FOM ($R_{on} \times Q_{gd}$) for the SG- and TG-MOSFET structures as a function of X length. X of 0.9 µm corresponds to the conventional MOSFET [8]. Both structures show the decreased $Q_{gd,sp}$ and HF-FOM ($R_{on} \times Q_{gd}$) when the X length becomes
small due to the reduction of the gate-to-drain overlap. In addition, the SG-MOSFET shows the more improved electrical characteristics with the smaller X length compared with the TG-MOSFET. Therefore, from the simulation results, the SG-MOSFET is found to be much superior to the TG-MOSFET as well as the conventional MOSFET in terms of the improved electrical performance.

2.2. Structure Optimization

In the previous section, the SG-MOSFET was shown to have superior performance over the TG-MOSFET. Therefore, the SG-MOSFET is optimized with the TCAD numerical simulations for the actual fabrication in this section [10][11].

Figure 3.6 shows cross-sectional views of the conventional MOSFET and the SG-MOSFET devices with structural parameters. The numerical simulations were conducted for the structures with the same enhanced JFET doping of \(3 \times 10^{16} \text{ cm}^{-3}\) to reduce the on-resistance. Figure 3.7 provides the simulated specific on-resistance \(R_{\text{on,sp}}\) as a function of JFET width \(W_{\text{JFET}}\) for

![Figure 3.6. Cross-sectional view of the 1.2 kV SiC conventional MOSFET (left) and SG-MOSFET (center) structures. Structural parameters are given.](image-url)
the conventional Acc- and Inv-channel MOSFETs at room temperature and 150°C [11]. The simulation results shown in the figure indicate an optimum JFET width ($W_{JFET}$) of 0.9 \( \mu \text{m} \) to achieve the lowest $R_{on,sp}$ at both temperatures for both Acc- and Inv-channel structures. However, for the better $C_{gd,sp}$, $Q_{gd,sp}$, and HF-FOMs, the optimum JFET width for the fabricated conventional device was chosen at $W_{JFET}=0.7 \, \mu \text{m}$ in the Chapter 2 [12].

The simulations of the SG-MOSFETs with fixed $W_{JFET}$ of 0.9 \( \mu \text{m} \) were performed for the smallest $R_{on,sp}$. The maximum oxide electric field, $R_{on,sp}$, $Q_{gd,sp}$, $C_{gd,sp}$, HF-FOM ($R_{on} \times C_{gd}$), and HF-FOM ($R_{on} \times Q_{gd}$) were obtained from the SG-MOSFETs with the accumulation-channel (Acc) as a function of the poly-Si gate overhang ($X$) into the JFET region as shown in Figure 3.8 [10].

In the SG-MOSFETs, the largest electric field is concentrated at the edge of the poly-Si gate as discussed in the previous section. It is important to keep the maximum electric field in the gate oxide well below 4 MV/cm for reliable operation [5]. The numerical simulations show a maximum value for the electric field in the gate oxide at $X=0.5 \, \mu \text{m}$ (Figure 3.8(b)). As already discussed in Figure 3.4, the oxide field is suppressed by their proximity or the P$^+$ shielding region when the space between the split poly-Si gates is small (i.e. $X>0.5 \, \mu \text{m}$) or large (i.e. $X<0.5 \, \mu \text{m}$),
respectively. From the numerical simulations, it can be concluded that the X width must be less than 0.3 µm to keep the oxide electric field well below 4 MV/cm.

As shown in Figure 3.8(a), the $Q_{gd,sp}$ and $C_{gd,sp}$ in the SG-MOSFETs are significantly improved with decrease in X values. Although the best HF-FOMs are observed at X=0.1 µm as shown in Figure 3.8(b), the $R_{on,sp}$ increases considerably when X is decreased to 0.1 µm because of an increase in the accumulation layer resistance (Figure 3.8(a)). Taking process alignment tolerances into account, large variations in the $R_{on,sp}$ are anticipated when X is less than 0.2 µm.

From the numerical simulations, an optimum X value is therefore determined to be 0.3 µm in order to keep the gate oxide electric field well below 4 MV/cm for reliability and to obtain the low $R_{on,sp}$ simultaneously. For this case, about 2× smaller HF-FOMs are projected compared with the conventional MOSFET.

Figure 3.9 shows the simulated $R_{on,sp}$, $C_{gd,sp}$, and HF-FOM ($R_{on}\times Q_{gd}$) as a function of temperature for both Acc- and Inv-channel SG-MOSFETs with optimum $W_{JFET}=0.9$ µm and X=0.3 µm [11]. Both structures have the same $C_{gd,sp}$ values regardless of temperature variations.
consistent with previous measurements on 1.2 kV SiC power MOSFETs [13].

It is observed that the $R_{on,sp}$ increases with temperatures for both structures with almost the same slope. The calculated HF-FOMs follow the same trends as the $R_{on,sp}$ with temperatures as shown in Figure 3.9. The simulations predict that the Acc-channel SG-MOSFET will have 1.1× smaller HF-FOM compared to Inv-channel SG-MOSFET. In addition, the HF-FOMs are projected to increase from room temperature to 150°C by 1.4× for both structures.

3. Fabrication of 1.2 kV 4H-SiC SG-MOSFETs

In this section, the fabrication of the 1.2 kV 4H-SiC SG-MOSFETs will be discussed. The devices are fabricated using the exactly same process as the one for the 1.2 kV conventional MOSFET structures discussed in Chapter 2.

3.1. Layout Description

Figure 3.10 shows layouts for the Power America (PA) project - Budget Period 2 (BP2): (a) 1st lot layout (shown in Chapter 2), and (b) 2nd lot layout for the 1.2 kV Split-Gate power
MOSFET structures. One Split-Gate power MOSFET structure in the BP2 1st lot layout and the entire BP2 2nd lot layout were designed by me. Total 6 Split-Gate power MOSFET structures with slightly different structural parameters were designed within the two layouts as shown in Figure 3.10. Among them, “SGMOS0” design is the optimized SG-MOSFET structure for the JFET width of 0.9 µm and X width of 0.3 µm as discussed in the previous section.

3.2. Process Flow

All the structures were fabricated at a 6-inch foundry, X-Fab, using the NCSU PRESiCE™ process [14]. The exactly same number of masks and same process as the 1.2 kV conventional MOSFETs are used. The SG-MOSFET structures were fabricated on a 6-inch, N⁺ 4H-SiC wafer with a 10 µm thick and 8×10¹⁵ cm⁻³ doped n-type epi-layer using a total of 11-masks. The fabrication process flow is briefly described in Figure 3.11:
The zero alignment mark was etched (Mask 1). The enhanced N⁻ JFET (Mask 2), Acc- or Inv-channel and P⁺ shielding (Mask 3), P JTE for the JTE rings of the edge termination regions (Mask 4), P⁺ contact orthogonal to the cross-section (Mask 5), and N⁺ source (Mask 6) were formed by a series of implants of N and Al. A 10-min implant activation anneal was conducted at 1650°C with a carbon cap after all the ion implantation steps. The 50 nm thick gate oxide was formed by dry oxidation at 1175°C, followed by an NO annealing. N-type poly-Si gate (500 nm) was deposited and patterned to define the X width (Mask 7). Oxide interlayer dielectric deposition was performed, followed by Ni ohmic contact process with an RTA on the both front and back sides (Mask 8). The oxide interlayer dielectric on the poly-Si was etched for the gate contact (Mask 9). Al-based metal stacks were used to form the source and gate pads (Mask 10). Nitride and Polyimide passivation layers were deposited on the front side and patterned (Mask 11). Lastly, a solderable metal stack was deposited on the back side. The active area for all the devices is 0.045
cm$^2$. The same hybrid JTE edge termination design [15] was used for the 1.2 kV Split-Gate power MOSFETs.

4. Experimental Results and Discussions

4.1. Experimental Results

All the SG-MOSFETs were successfully fabricated at the 6-inch foundry, X-Fab. Figure 3.11 shows the SEM image for the fabricated Inv-channel SG-MOSFET with $W_{JFET}$ of 0.9 $\mu$m and $X$ of 0.3 $\mu$m [11]. The very well defined Split-Gate structure through the fabrication is clearly observed in Figure 3.12.

All the fabricated devices were measured using the semi-automatic Signatone Probestation and Keysight B1505A Curve Tracer with the standard measurement methods. Figure 3.13 shows

![Split Gate Poly-Si](image)

Figure 3.12. SEM cross-sectional image for the fabricated 1.2 kV SiC Inv-channel Split-Gate power MOSFET with $W_{JFET}$ of 0.7 $\mu$m [11].
Figure 3.13. Typical output characteristics for Acc conventional MOSFET and SG-MOSFET measured at $V_g$ from 0 to 25 V with 5 V steps at room temperature [10].

typical measured output characteristics of the fabricated Acc-channel conventional MOSFET and SG-MOSFET demonstrating enhancement-mode operation [10]. The measured on-resistance at $V_g=20$ V and $I_d=10$ A is 141 and 140 m$\Omega$ with for the conventional MOSFETs and the SG-MOSFETs, respectively. This demonstrates that the process alignment tolerance is sufficient to manufacture SG-MOSFETs with $X = 0.3$ $\mu$m in a foundry environment. The measured specific on-resistance of 6.3 m$\Omega$-cm$^2$ is 3 times larger than the ideal on-resistance obtained by adding the epi layer and substrate resistance because of additional contributions from channel (25%), JFET (12%), and drift spreading (38%) resistances extracted from the simulations. Both devices have the same measured on-resistance despite different $W_{JFET}$ and cell pitch as expected from the simulation results in Figure 3.7.

The typical measured transfer characteristics of the fabricated Acc conventional MOSFET and SG-MOSFET at room temperature are shown in Figure 3.14. It shows the identical transconductance ($g_m$) between the conventional MOSFET and SG-MOSFET. The threshold voltages
(V_{th}) are extracted at V_d=0.1 V and I_d=1 mA as marked with the red dot line in the figure. They have the same V_{th} of about 2.00 V within the experimental error.

Figure 3.15 compares the blocking characteristics of the Acc conventional MOSFET and SG-MOSFET [10]. Both structures show very similar leakage and breakdown voltage. This

Figure 3.15. Comparison of blocking capability for Acc conventional MOSFET and SG-MOSFET [10].
demonstrates that the electric field on the gate oxide for the SG-MOSFET is sufficiently low. The breakdown voltages extracted at I_d of 100 µA for the MOSFET and SG-MOSFET are 1634 and 1626 V, respectively.

The measured reverse transfer capacitance (C_{gd}) of the Acc SG-MOSFET can be compared with that for the Acc conventional MOSFET in Figure 3.16 [10]. The C_{gd} for the SG-MOSFET at V_d=1000 V is 3.7 pF compared with 4.9 pF for the conventional MOSFET. More significantly, the C_{gd} for the SG-MOSFET at V_d=0 V is 118 pF which is about 6 times smaller compared with 715 pF for the conventional MOSFET as shown in the zoomed-in view inset in Figure 3.16. The significant reduction of C_{gd} at small V_d values can be explained by the geometric factor. The C_{gd} is proportional to (X-W_0)/(W_{cell}/2), where W_0 is JFET depletion width and W_{cell}/2 is the half cell pitch [6][7]. The calculated values for the conventional MOSFET and SG-MOSFET are 0.178 and 0.033 using W_0 of 0.2 µm, which agrees with the 6 times smaller C_{gd} at low V_d for the SG-MOSFET. This large reduction reduces the gate-drain charge significantly.

Figure 3.16. Typical reverse transfer capacitance (C_{gd}) for Acc conventional MOSFET and SG-MOSFET measured at room temperature [10].
The measured gate charge waveforms at \( V_d = 800 \) V and \( I_d = 10 \) A for the Acc conventional MOSFET and the Acc SG-MOSFET are provided in Figure 3.17 [10]. The \( Q_{gd} \) obtained from the gate voltage plateaus (marked in Figure 3.17) is 15.8 and 6.7 nC for the conventional MOSFET and the SG-MOSFET, respectively. The observed reduction by a factor of \( 2.4 \times \) provides experimental confirmation of the improved switching performance of the 4H-SiC SG-MOSFET structure for the first time.

The Inv-channel SG-MOSFET with \( W_{JFET} = 0.9 \) \( \mu \)m and \( X = 0.3 \) \( \mu \)m is also fabricated simultaneously for the electrical performance comparison at higher temperatures.

The output characteristics measured at room and 150°C for the fabricated Acc- and Inv-channel SG-MOSFETs can be compared in Figure 3.18 and 3.19, respectively [11]. The measured on-resistances \( (R_{on}) \) at \( V_g = 20 \) V and \( I_d = 10 \) A for the Acc- and Inv-channel SG-MOSFETs were 140 and 163 m\( \Omega \) at room temperature, and 188 and 217 m\( \Omega \) at 150°C, respectively. The observed increase \( R_{on} \) is much smaller than that reported for commercial devices as discussed later. The
The difference between the Acc- and Inv-channel SG-MOSFETs in the on-resistances is mainly due to the different channel mobilities as discussed before [16].

The observed behavior of the increased on-resistance with increasing temperature has already been discussed with the measured field effect channel mobilities ($\mu_{\text{CH,FE}}$) and the
analytically calculated bulk mobilities for both Acc- and Inv-channel structures at higher temperatures as shown in Figure 2.9 in Chapter 2. The $\mu_{CH,FE}$ were found to slightly increase with the same slope as temperature rises to 150°C for both Acc- and Inv-channel devices. An increase in channel mobility with increasing temperature has been previously reported for SiC devices due to trapping of carriers at interface states [17].

The normalized $R_{on}$ values measured as a function of temperature at $V_g=20$ V and $I_d=10$ A for the fabricated Acc- and Inv-channel SG-MOSFETs can be compared with those for a typical commercial MOSFET (Wolfspeed C2M0160120D product [18]) in Figure 3.20 [11]. The resistance of our fabricated Acc- and Inv-channel SG-MOSFETs increase by only $1.3\times$ from room temperature to 150°C compared with $1.8\times$ increase for the typical commercial device. This behavior is observed for our devices because the channel resistance decreases with increasing temperature due to both a reduction in the threshold voltage (see Figure 3.22 discussion) and an increase in channel mobility. This effect compensates for the increase in bulk resistance with
increasing temperature. The observed behavior retains the ability to parallel our devices with good current sharing while less derating of their current is required at elevated temperatures.

The typical transfer characteristics of the Acc- and Inv-channel SG-MOSFETs measured at temperatures up to 150°C are shown in Figure 3.21 [11]. The threshold voltages extracted at $V_d=0.1$ V and $I_d=1$ mA are 2.34 and 3.44 V at room temperature, and 1.38 and 2.26 V at 150°C for the Acc- and Inv-channel SG-MOSFETs, respectively as shown in Figure 3.22 [11]. The threshold voltages over 2.5 V at 150°C is desirable for the power devices to avoid any false trigger.

In order to understand the $V_{th}$ variation with temperature, the $V_{th}$ was calculated using standard models given by [7] and [17] for the inversion-mode device:

$$V_{th} = \Phi_{MS} + 2\phi_B + \frac{1}{C_{OX}} \left( \sqrt{4\varepsilon_s qN_A \phi_B + q \int_{E_i}^{E_F} \phi_i D_n(E) dE - qN_{Eff}} \right)$$  \hspace{1cm} (3.1)
and the accumulation-mode device [7]:

$$V_{th} = \Phi_{MS} + \frac{\varepsilon_s V_{bi} t_{OX}}{\varepsilon_{OX} W_N} - \frac{q N_D t_{OX}}{2 C_{OX}} + \frac{1}{C_{OX}} \int_{E_S}^{E_F + \Phi_B} D_{it}(E) dE - q N_{Eff}$$  \quad (3.2)

where $\Phi_{MS}$ is work function between the gate poly-Si and semiconductor fermi level energy, $\phi_B$ is the bulk potential, $C_{OX}$ is the oxide capacitance, $\varepsilon_S$ and $\varepsilon_{OX}$ are the semiconductor and oxide dielectric constant, and $N_A$ and $N_D$ are the channel doping concentration for the Inv- and Acc-structures, respectively. $D_{it}$ is the interface-state density, $t_{OX}$ is the gate oxide thickness, $V_{bi}$ is the built-in potential, and $N_{Eff}$ is the effective oxide charge density. As shown in the equations above, the higher threshold voltages can be achieved with higher $N_A$ in Inv MOSFETs and lower $N_D$ in Acc MOSFETs, respectively. To apply these models, the $D_{it}$ was extracted using the High-Low

![Figure 3.22. Threshold voltages ($V_{th}$) were experimentally extracted, and analytically calculated for fabricated Acc- and Inv-channel SG-MOSFETs at temperatures up to 150°C [11].](image-url)
method [19] from C-V measurements on fabricated MOS structures on the same wafer as shown in Figure 3.23 and 3.24 [11]. Two threshold voltage cases (without $D_{it}$ and with $D_{it}$) were calculated and compared to the measured data to check the impact of the interface traps as shown in Figure 3.22 [11]. The $N_{Eff}$ of $1.5 \times 10^{12}$ cm$^{-2}$ was assumed for all cases so that the modeled threshold

![Figure 3.23. Measured C-V curves at low (1 kHz) and high (100 kHz) frequencies for fabricated Acc- and Inv-channel MOS structures [11].](image1)

![Figure 3.24. Extracted $D_{it}$ for fabricated Acc- and Inv-channel MOS structures using the High-Low method [19]. Both structures show similar $D_{it}$ [11].](image2)
voltages with $D_n$ are matched with the measured values at room temperature. A good agreement of the temperature dependence of the threshold voltage is observed only by including the measured $D_n$. These results demonstrate that a high $D_n$ is an important factor determining the rate of decrease in the $V_{th}$ with temperature for our devices.

The typical measured room temperature blocking characteristics of the Acc- and Inv-channel SG-MOSFETs are shown in Figure 3.25 [11]. Both structures have excellent breakdown voltage due to the same Hybrid-JTE edge termination design [15]. The breakdown voltages extracted at $I_d$ of 100 $\mu$A for the Acc- and Inv-channel SG-MOSFETs are 1626 V and 1635 V, respectively. The Acc-channel structure shows about one-order higher leakage current compared to the Inv-channel structure, but its magnitude is still much smaller than the allowable typical maximum leakage current of 100 $\mu$A in datasheets. These results imply that the oxide electric field for both SG-MOSFETs is sufficiently low to achieve acceptable leakage current and high breakdown voltage at room temperature.
Figure 3.26. Measured leakage currents at $V_d$ of 1000 V for fabricated Acc- and Inv-channel SG-MOSFETs at elevated temperatures [11].

The leakage currents measured at $V_d$ of 1000 V for both devices as a function of temperature can be compared in Figure 3.26 [11]. The Acc-channel SG-MOSFET shows steady increase of the leakage currents from $\sim$10 nA to $\sim$2 $\mu$A from 25°C to 150°C. However, the Acc-channel SG-MOSFET exhibits sufficiently low leakage current at 150°C when compared to the

Figure 3.27. Reverse transfer capacitance ($C_{gd}$) of fabricated Acc- and Inv-channel SG-MOSFETs measured at elevated temperatures [11].
The typical maximum leakage current of 100 µA in datasheets. The observed higher leakage current for the Acc-channel SG-MOSFET is due to the smaller potential barrier for electrons in the N-base region as already discussed in Chapter 2. In contrast, the leakage current (~2-3 nA) for the Inv-channel SG-MOSFET remains nearly constant with increasing temperature.

The measured reverse transfer capacitance ($C_{gd}$) of the Acc- and Inv-channel SG-MOSFETs at higher temperatures up to 150°C can be compared in Figure 3.27 [11]. It can be observed that the two SG-MOSFETs have the same $C_{gd}$ values due to the identical JFET and drift region parameters. In addition, the $C_{gd}$ remains independent of the temperature as expected by the simulation results in Figure 3.9 and reported for commercial devices [13]. The $C_{gd}$ measured at $V_d=1000$ V is 3.7 and 3.8 pF for the Acc- and Inv-channel SG-MOSFETs, respectively, which is equal within experimental error.

The gate charge waveforms measured at $V_d=800$ V and $I_d=10$ A and room temperature are shown in Figure 3.28 for the fabricated Acc- and Inv-channel SG-MOSFETs [11]. Although the Inv-channel structure shows a plateau at a higher gate voltage than the Acc-channel device due to

![Figure 3.28](image_url)

**Figure 3.28.** Measured gate charge of Acc- and Inv-channel SG-MOSFETs at $V_d=800$ V and $I_d=10$ A. Both structures have the similar $Q_{gd}$ values despite the plateau at higher gate voltage for the Inv device [11].
its larger threshold voltage, the extracted $Q_{gd}$ values are the same for the Acc- (6.7 nC) and Invchannel (6.6 nC) SG-MOSFETs within experimental error.

### 4.2. Discussions

All the electrical characteristics of the fabricated Acc- and Inv-channel SG-MOSFETs are compared with those of the fabricated Acc-channel conventional MOSFET and typical commercial MOSFET (C2M0160120D [18]) in Table 3.1 [10][11]. The specific values such as $R_{on,sp}$, $C_{gd,sp}$, and $Q_{gd,sp}$ for all our fabricated structures are provided using the active area of 0.045 cm$^2$. It should be noted that about 1.7 mΩ·cm$^2$ parasitic resistance ($R_{sub}$: 0.7 and $R_{probing}$: 1 mΩ·cm$^2$) is included for all the $R_{on,sp}$ results.

It has been found that the $C_{gd}$ values are independent of the various temperatures (shown in Figure 3.26), and it has been reported that the $Q_{gd}$ values are also unchanged with the various temperatures [20]. Consequently, the measured $C_{gd}$ and $Q_{gd}$ values at room temperature can be used for the calculations of the HF-FOM [$R_{on} \times Q_{gd}$] and HF-FOM [$R_{on} \times C_{gd}$] at 150°C.

The Acc-channel SG-MOSFET has lower $R_{on,sp}$ than the Inv-channel SG-MOSFET due to the higher accumulation channel mobility as discussed earlier. This results in about 1.2× smaller HF-FOM [$R_{on} \times Q_{gd}$] and HF-FOM [$R_{on} \times C_{gd}$] at both room temperature and 150°C for the Acc-channel SG-MOSFET when compared with the Inv-channel SG-MOSFET. The HF-FOMs at 150°C are 1.3× larger than at room temperature due to an increase in their $R_{on,sp}$.

The calculated HF-FOM [$R_{on} \times Q_{gd}$] and HF-FOM [$R_{on} \times C_{gd}$] at 25°C and 150°C of the Acc SG-MOSFET are found to be 2.4× and 1.3×, and 2.6× and 1.4× lower than those of the Acc conventional MOSFET with the reduced $C_{gd}$ and $Q_{gd}$ due to the split gate structures.
In addition, the HF-FOM \( [R_{on} \times Q_{gd}] \) and HF-FOM \( [R_{on} \times C_{gd}] \) at 25°C for the Acc-channel SG-MOSFET are found to be a factor of 2.4\( \times \) and 1.2\( \times \) smaller than the typical commercial conventional MOSFET. Both Acc- and Inv-channel SG-MOSFETs have even superior performance at the elevated temperatures (150°C). The calculated HF-FOM \( [R_{on} \times Q_{gd}] \) and HF-FOM \( [R_{on} \times C_{gd}] \) for the Acc-channel SG-MOSFET are found to be a factor of 3.2\( \times \) and 1.7\( \times \) smaller at 150°C compared with the commercial conventional MOSFET. This improvement in performance is due to the smaller increase in \( R_{on} \) as a function of temperature for the Acc-channel SG-MOSFET.

### 5. Conclusions

The 1.2 kV 4H-SiC accumulation and inversion mode channel SG-MOSFETs have been successfully fabricated and compared with respect to electrical characteristics such as on-
resistance, threshold voltage, breakdown voltage, leakage current, reverse transfer capacitance, and gate-to-drain charge at temperatures up to 150°C.

The Acc-channel SG-MOSFET has lower threshold voltage and higher leakage current than the Inv-channel SG-MOSFET mainly due to the inherently lower channel barrier potential of the accumulation mode channel. The threshold voltage of the Acc-channel SG-MOSFET is observed to remain in a reasonable range for enhancement mode operation at room temperature. But, the threshold voltages over 2.5 V at 150°C is desirable for the reliable operation, which can be achieved with higher $N_A$ in Inv- and lower $N_D$ in Acc-MOSFETs, respectively. The lower on-resistance of the Acc-channel SG-MOSFET, due to its larger channel mobility, provides about $1.2\times$ smaller HF-FOMs at both room temperature and 150°C compared to the Inv-channel SG-MOSFET.

The Acc SG-MOSFET has experimentally demonstrated to have significantly superior HF-FOMs due to reduced reverse transfer capacitance and gate-to-drain charge with the same specific on-resistance compared with those for the Acc-channel conventional MOSFET. It was conclusively shown that the Acc SG-MOSFET has an improvement in HF-FOM [$R_{on}\times Q_{gd}$] by $2.4\times$ and HF-FOM [$R_{on}\times C_{gd}$] by $1.3\times$ at room temperature.

In addition, the Acc-channel SG-MOSFET shows better performance compared to the typical commercial MOSFET. Its HF-FOM [$R_{on}\times Q_{gd}$] and HF-FOM [$R_{on}\times C_{gd}$] are smaller by a factor of $2.4\times$ and $1.2\times$ at 25°C, and by a factor of $3.2\times$ and $1.7\times$ at 150°C.

In conclusion, the numerical simulations and experimental results demonstrate the SG-MOSFETs have reduced rate of increase in the on-resistance with temperature when compared with typical commercial power MOSFETs. Combining this attribute with the low reverse transfer capacitance and gate-to-drain charge of the split-gate structure produces superior HF-FOMs at
elevated temperatures. This demonstrates that the 4H-SiC SG-MOSFETs have excellent characteristics for high frequency applications not only at room temperature but also at elevated temperatures.

For further improvement of the 4H-SiC SG-MOSFETs, a self-aligned process to define the “X” width precisely without a mask should be developed to eliminate any possible misalignment during the fabrication. Thereby, more stable electrical characteristics can be achieved.
REFERENCES


CHAPTER 4.

Development of Novel 1.2 kV 4H-SiC Linear Cell Buffered-Gate MOSFETs (BG-MOSFET) for Extremely Low HF-FOMs

1. Background & Motivation

Cree, Inc. (Wolfspeed) has recently proposed central implant MOSFET (CIMOSFET) structures to improve the $C_{gd}$, $Q_{gd}$, and HF-FOMs [1]. This approach requires an additional implant mask step for an extra p-type region in the center of the JFET region to improve the electrical characteristics by reducing the gate-to-drain overlap area as shown in Figure 4.1(a) [1]. In addition, the high gate oxide reliability can be expected in the CIMOSFET structure because the high gate oxide electric field which is concentrated at the center of the gate oxide can be mitigated due to the extra p-region placed in the middle of the JFET region. The simulation results of the gate oxide electric field at $V_d$ of 960 V are shown in Figure 4.1(b) [1]. It shows the mitigated gate oxide electric field.
field in the CIMOSFET compared with the SiC commercial conventional MOSFET (C2M0080120D [2]).

In the previous chapter, the 4H-SiC Split-Gate power MOSFET structures were discussed to improve the $C_{gd}$, $Q_{gd}$, and HF-FOMs [3][4][5]. The structure optimization was conducted with TCAD numerical simulations not only to improve the HF-FOMs, but also to alleviate the high gate oxide electric field concentrated at the edge of the split poly-Si gate.

For more improved HF-FOMs with even further reduced gate oxide electric field, an innovative 4H-SiC Buffered-Gate MOSFET structure was proposed by Dr. B. Jayant Baliga [6] and has been experimentally demonstrated [7][8]. The split-gate poly-Si electrode is buffered from the drain by extending the $P^+$ shielding region beyond its edge in the BG-MOSFET eliminating the largest electric field concentrated at the edge of the poly-Si gate. An additional $N^+$ JFET region is required in the BG-MOSFET structure to prevent complete depletion above the $P^+$ shielding region beyond the gate edge. In the BG-MOSFET structure, an increase in $R_{on,sp}$ is traded off against reduced switching losses to achieve significantly improved HF-FOMs for high frequency applications. It is commonplace to trade-off higher on-state voltage drop to achieve reduced switching losses in the bipolar power devices like IGBTs [10]. A similar approach was taken for SiC power MOSFETs.

In this chapter, the novel 4H-SiC Buffered-Gate MOSFETs are analyzed, optimized, and characterized in detail.

2. Structure Optimization using TCAD Numerical Simulations

As briefly introduced in the background section, the 4H-SiC Buffered-Gate (BG) MOSFET structure has the extended $P^+$ shielding region beyond the split-gate electrodes as shown in Figure
4.2 [8]. The extended P\(^+\) shielding region buffers the high gate oxide electric field concentrated at the edge of the split gate structures as discussed in Chapter 3, so more reliable gate oxide can be expected. In addition, the P\(^+\) shielding region reduces the gate-to-drain overlap, which effectively decreases the reverse transfer capacitance (\(C_{gd}\)) and gate-to-drain charge (\(Q_{gd}\)), so significantly improved HF-FOMs can be expected.

In order to achieve the buffered gate structure with the extended P\(^+\) shielding region, the additional N\(^+\) JFET region is necessary to avoid very high on-resistance because of the completely depleted area above the P\(^+\) shielding region beyond the split gate edge as shown in Figure 4.2.

In this section, the 1.2 kV 4H-SiC Buffered-Gate MOSFETs are analyzed and optimized for the N\(^+\) JFET region, and \(X_1\) and \(X_2\) widths using TCAD numerical simulations so that the structure has the improved \(C_{gd}\), \(Q_{gd}\), and HF-FOMs with low enough gate oxide electric field.

### 2.1. N\(^+\) JFET Doping Concentration

Figure 4.2 shows cross-sectional views of the accumulation-channel (Acc) C-MOSFET, SG-MOSFET, and accumulation- (Acc) or inversion-channel (Inv) BG-MOSFET structures [8].
The N⁺ JFET region must be included in the BG-MOSFET to prevent a potential barrier for electrons above the P⁺ shielding region as already discussed above. Therefore, the N⁺ JFET region doping concentration and thickness must be carefully chosen to allow current flow without degrading the breakdown voltage. The N⁺ JFET region doping concentration was carefully studied by 2-D TCAD numerical simulations in order to optimize the device operation.

For the simulations, the BG-MOSFET structures shown in Figure 4.2 have the same channel length of 0.5 \( \mu \text{m} \), and the optimum JFET doping (\( N_{\text{JFET}} \)) and width (\( W_{\text{JFET}} \)) of \( 3 \times 10^{16} \text{ cm}^{-3} \) and 0.7 \( \mu \text{m} \), respectively, as previously shown and discussed in Chapter 2.

Figure 4.3 shows the simulation results of specific on-resistance (\( R_{\text{on,sp}} \)) and maximum gate oxide electric field at \( V_{\text{d}}=1600 \text{ V} \) as a function of N⁺ JFET doping concentration for the Acc- and Inv-channel BG-MOSFETs [8]. An N⁺ JFET region thickness of 0.2 \( \mu \text{m} \), poly-Si gate overhang into the JFET region (\( X_1 \)) of 0.4 \( \mu \text{m} \), and P⁺ shielding region width beyond the poly-Si gate edge (\( X_2 \)) of 0.1 \( \mu \text{m} \) were used in the simulations. The highest oxide electric field is found at the edge of the split poly-Si gate as already discussed in the SG-MOSFET structures in Chapter 3. As expected,
it is observed that the poly-Si gate edge is buffered by the P+ shielding region in the BG-MOSFETs with low N+ JFET doping concentration from the oxide electric field simulation results. However, the simulation results show that the BG-MOSFETs have very high Ron,sp with the low N+ JFET doping concentration. Forward conduction simulations were conducted at V_g of 20 V and I_d of 10 A with various N+ JFET doping concentration to check the high Ron,sp values as shown in Figure 4.4. It shows the current density in the cross-section of Inv-channel BG-MOSFET structures with N+ JFET doping of (a) 1×10^{17}, (b) 2×10^{17}, and (c) 4×10^{17} cm^{-3}, respectively. The white lines indicate the depletion region boundary. The simulation results explain that the high Ron,sp is resulted from the narrow current pathway because of the depletion above the extended P+ shielding region with not enough N+ JFET doping concentration as shown in Figure 4.4. The Ron,sp is decreased with the increase of the N+ JFET doping concentration, but it becomes steady with higher N+ JFET doping concentration (> 4×10^{17} cm^{-3}) as shown in Figure 4.3. It also shows that the extracted oxide electric field from the simulations exceeds 4 MV/cm with the higher N+ JFET doping concentration without any benefits in Ron,sp. This indicates an optimum N+ JFET doping concentration of 3×10^{17} cm^{-3} for
both Acc- and Inv-channel BG-MOSFETs. The N+ JFET doping concentration of $1.5 \times 10^{17} \text{ cm}^{-3}$ is also selected for electrical performance comparison.

### 2.2. Structure Optimization

From the previous section, the N+ JFET region doping concentration and thickness were chosen to allow current flow without degrading the breakdown voltage using TCAD numerical simulations. It was found that 0.2 $\mu$m thick N+ JFET regions with doping concentrations of $3.0 \times 10^{17} \text{ cm}^{-3}$ was satisfactory. The N+ JFET doping of $1.5 \times 10^{17} \text{ cm}^{-3}$ was also selected for the electrical performance comparison.

For the optimization of the $X_1$ and $X_2$ widths, the TCAD numerical simulations were performed for the Acc-channel BG-MOSFET structures (shown in Figure 4.2). The simulated Acc BG-MOSFET structures have the same channel length of 0.5 $\mu$m, enhanced JFET doping of $3 \times 10^{16} \text{ cm}^{-3}$, JFET width ($W_{\text{JFET}}$) of 0.7 $\mu$m, and the N+ JFET doping of $1.5 \times 10^{17} \text{ cm}^{-3}$ or $3 \times 10^{17} \text{ cm}^{-3}$.

Figure 4.5 compares the simulation results of $Q_{\text{gd,sp}}$, $C_{\text{gd,sp}}$, $R_{\text{on,sp}}$, maximum oxide electric field (at $V_d=1200 \text{ V}$ and $V_g=0 \text{ V}$), HF-FOM [$R_{\text{on}} \times Q_{\text{gd}}$], and HF-FOM [$R_{\text{on}} \times C_{\text{gd}}$] for the Acc BG-MOSFETs as a function of $X_1$ widths [7][8]. The $W_{\text{N+JFET}}$ was fixed to 0.7 $\mu$m for the simulations. The solid lines and dashed lines indicate the Acc BG-MOSFET structures with higher ($3 \times 10^{17} \text{ cm}^{-3}$) and lower ($1.5 \times 10^{17} \text{ cm}^{-3}$) N+ JFET doping concentration, respectively.

The oxide electric field (see Figure 4.5(b) and Figure 4.6(b)) is well below 3 MV/cm in the BG-MOSFET structures demonstrating that the split poly-Si gate edges are buffered by the P+ shielding regions as previously discussed.

Significantly reduced $Q_{\text{gd,sp}}$, $C_{\text{gd,sp}}$, and gate oxide electric field with gradually increased $R_{\text{on,sp}}$ are observed in Figure 4.5(a) and (b) when $X_1$ decreases from 0.7 to 0.1 $\mu$m. Consequently,
the HF-FOMs are significantly reduced with decrease of $X_1$ as shown in Figure 4.5(b). Almost same $Q_{gd,sp}$ and $C_{gd,sp}$ are observed for the BG-MOSFETs with the same $X_1$ width regardless of the N$^+$ JFET doping concentration due to the same $W_{JFET}$ and $N_{JFET}$, but the increase of $R_{on,sp}$ for the smaller $X_1$ widths is larger for the case of the lower N$^+$ JFET doping concentration as shown in Figure 4.5(a). Figure 4.5(a) and Figure 4.5(b) indicate the $X_1$ width smaller than 0.5 $\mu$m is necessary due to the rapid increases in the $Q_{gd,sp}$, gate oxide electric field, and HF-FOM $[R_{on} \times Q_{gd}]$ for the larger $X_1$ values. In addition, the BG-MOSFETs with the higher N$^+$ JFET doping concentration show the better HF-FOMs because of the lower $R_{on,sp}$. Based up on the simulation results and process alignment tolerances, the optimum $X_1$ value of 0.4 $\mu$m was chosen for the BG-MOSFETs. For the fair comparison, the $X_1$ width of 0.4 $\mu$m was also selected for the SG-MOSFET.

Figure 4.6 shows the obtained $Q_{gd,sp}$, $C_{gd,sp}$, $R_{on,sp}$, maximum oxide electric field (at $V_d=1200$ V and $V_g=0$ V), and HF-FOMs as a function of the P$^+$ shielding region width ($X_2$) beyond the poly-Si gate [7][8]. Based up on the previous simulation results, the $X_1$ was fixed at 0.4 $\mu$m for the simulations.
When the $X_2$ width is -0.4 $\mu$m which is same as the $X_1$ width, the structure becomes the regular Split-Gate MOSFET because there is no extended P$^+$ shielding region as marked in Figure 4.6. In addition, for the BG-MOSFET structures, the $X_2$ width should be bigger than 0 $\mu$m so that the split-gate is buffered from high drain voltage (marked in Figure 4.6).

Significantly reduced $Q_{gd,sp}$ and $C_{gd,sp}$ with increased $R_{on,sp}$ are observed when $X_2$ increases to 0.5 $\mu$m due to enhanced screening of the gate by the P$^+$ shielding region as shown in Figure 4.6(a). No different $Q_{gd,sp}$ and $C_{gd,sp}$ are found between the BG-MOSFETs with the higher and lower N$^+$ JFET doping concentration at the same $X_2$ width. However, the increase of $R_{on,sp}$ is much larger for the case of the lower N$^+$ JFET doping concentration due to the larger depletion as discussed in Figure 4.4.

Figure 4.6(b) demonstrates that the oxide electric field is well below 3 MV/cm for the BG-MOSFET structures with higher and lower N$^+$ JFET doping concentration because of the buffered gate oxide by the extended P$^+$ shielding region as discussed so far. The HF-FOMs are greatly reduced with the increase of $X_2$ as shown in Figure 4.6(b) in spite of the increase in $R_{on,sp}$. The best
HF-FOMs occur with $X_2$ of 0.5 $\mu$m. However, the improvement of the HF-FOMs is not significant compared to the structure with $X_2$ of 0.3 $\mu$m, and the $R_{on,sp}$ increases significantly for $X_2$ of 0.5 $\mu$m which is not desirable. Consequently, the optimum $X_2$ was determined to be 0.3 $\mu$m. Numerical simulations of the Acc BG-MOSFET with the higher $N^+ JFET$ doping concentration at the $X_1$ of 0.4 $\mu$m and $X_2$ of 0.3 $\mu$m demonstrate that about $3 \times$ reduced HF-FOMs can be expected compared with the Acc SG-MOSFET.

Table 4.1 summarizes the structural parameters for the conventional (C), Split-Gate (SG), and Buffered-Gate (BG) MOSFETs for fabrication based up on the TCAD numerical simulations. Detailed comparison of the electrical characteristics for those structures will be discussed in the following section.
3. Fabrication of 1.2 kV 4H-SiC BG-MOSFETs

In this section, the fabrication of the 1.2 kV 4H-SiC BG-MOSFETs will be discussed. The devices are fabricated with total 12 masks including the additional N⁺ JFET implant using the NCSU PRESiCE™ process [11].

3.1. Layout Description

Figure 4.7 shows a layout designed by me for the Power America (PA) project - Budget

Figure 4.7. PowerAmerica (PA) Budget Period 2 (BP2) 2nd lot layouts for the 1.2 kV Buffered-Gate power MOSFET structures.
Period 2 (BP2) 2nd lot for the 1.2 kV Buffered-Gate power MOSFET structures. Total 12 Buffered-Gate power MOSFET structures with slightly different structural parameters were designed as shown in Figure 4.7. The “BGMOS 9” design is the optimized BG-MOSFET structure with the $X_1$ of 0.4 $\mu$m, $X_2$ of 0.3 $\mu$m, and the JFET width of 0.7 $\mu$m as discussed in the previous section.

3.2. Process Flow

All the structures were fabricated at 6-inch foundry, X-FAB, TX, using our PRESiCE™ process with the same design rules for features and alignment tolerances as the conventional MOSFET fabrication process [11].

The Acc- and Inv-channel BG-MOSFETs were fabricated on a 6-inch, N$^+$ 4H-SiC wafer with an n-type epi-layer (Thickness: 10 $\mu$m, Doping: $8\times10^{15}$ cm$^{-3}$). A total 12-mask including the addition N$^+$ JFET implant mask is used for the process. Acc conventional (C) MOSFET and Acc Split-Gate (SG) MOSFET with $X_1$ of 0.4 $\mu$m were also fabricated at the same time for comparison.

The basic fabrication steps to create the BG-MOSFET are shown in Figure 4.8 [8]: The zero alignment mark was etched (Mask 1). The enhanced N$^-$ JFET (Mask 2), Acc- or Inv-channel and P$^+$ shielding (Mask 3), P JTE for the JTE rings of the edge termination regions (Mask 4), P$^+$ contact orthogonal to the cross-section (Mask 5), and N$^+$ source (Mask 6) were formed by a series of implants of N and Al. The N$^+$ JFET region was formed by additional implantation step so that the channel length of 0.5 $\mu$m and the $W_{N^+\text{JFET}}$ (shown in Figure 4.2) of 0.7 $\mu$m are defined (Mask 7), followed by an implant activation anneal at 1650°C for 10-min with a carbon cap. Dry oxidation at 1175 °C was used to form the 50 nm thick gate oxide, followed by a post oxidation anneal in nitric oxide (NO) ambient and N-type poly-Si gate deposition. The poly-Si gate and gate oxide were patterned to define the $X_1$ and $X_2$ widths for the buffered gates (Mask 8). Thick oxide interlayer
The active area for all the devices is 0.045 cm². The same hybrid JTE edge termination design [12] was used for the 1.2 kV Buffered-Gate power MOSFETs.

4. Experimental Results and Discussions

4.1. Experimental Results
All the BG-MOSFETs were successfully fabricated at the 6-inch foundry, X-Fab. Figure 4.9 shows the SEM image for the fabricated Acc-channel BG-MOSFET with $X_1$ of 0.4 $\mu$m and $X_2$ of 0.3 $\mu$m [8]. It is clearly observed that the extended P$^+$ shielding regions were very well defined by the additional N$^+$ JFET implant and the split poly-Si gates are buffered by the regions as shown in Figure 4.9.

All the fabricated devices were measured using the Keysight B1505A Curve Tracer with the standard measurement methods.

Figure 4.10 shows the measured output characteristics of the fabricated Acc and Inv BG-MOSFETs, demonstrating that the N$^+$ JFET regions are not completely depleted by the P$^+$ shielding region [7][8]. The I-V characteristics were measured at gate biases of 0 to 25 V with 5 V steps. As expected from the simulations, the structure with the higher N$^+$ JFET doping (BG-MOS_H) has lower on-resistance. The measured on-resistances at $V_g=25$ V and $I_d=1$ A are 181,
186, and 238 mΩ for the Inv BG-MOS_H, Acc BG-MOS_H, and Acc BG-MOS_L, respectively. Although the Acc structure has higher channel mobility [13], the Inv BG-MOSFET shows lower $R_{on}$. This is due to smaller N+ JFET region resistance determined by the higher N+ JFET doping concentration above the JFET region. Figure 4.11 shows the N+ JFET implantation profiles for the Acc BG-MOS_H and Inv BG-MOS_H [8]. The region “a” (above the P+ shielding region) in the

Figure 4.10. Typical measured output characteristics of fabricated 1.2 kV rated Acc and Inv BG-MOSFETs with high or low N+ JFET doping measured at $V_g$ from 0 to 25 V with 5 V steps [7][8].

Figure 4.11. (a) Cross-section view of the BG-MOSFET, (b) N+ JFET implant profiles along with “a” and “b” marked in (a). Higher N+ JFET doping is required to compensate the P-base in Inv BG-MOSFET, resulting in the reduced BV [8].
Figure 4.11(a) requires the proper amount of the Nitrogen dose through the additional implant to form the N⁺ JFET region as already discussed in the fabrication process (Figure 4.8). For the Acc-channel BG-MOSFET case, the N⁺ JFET doping profile of about $3 \times 10^{17}$ cm⁻³ is enough to form the N⁺ JFET region because of the low doped N-base. Therefore, there is no difference in the doping concentration profiles between “a” (above the P⁺ shielding region) and “b” (above the JFET region) as shown in Figure 4.11(b). However, much higher N⁺ JFET doping profile is required to overcome and invert the P-base region to the N⁺ JFET region in the Inv BG-MOSFET. The N⁺ JFET doping concentration of $3 \times 10^{17}$ cm⁻³ above the P⁺ shielding region (“a”) could be obtained with very high doping concentration of $1 \times 10^{18}$ cm⁻³ above the JFET region (“b”) as shown in Figure 4.11(b). The higher N⁺ JFET doping concentration for the Inv BG-MOS_H reduces the N⁺ JFET region resistance as discussed above.

The measured blocking characteristics for all the BG-MOSFETs with the same Hybrid-JTE edge termination [12] are shown in Figure 4.12 [8]. The Acc BG-MOS_H and Acc BG-MOS_L show the excellent breakdown voltages of 1617 and 1623 V at I_d of 100 µA, respectively.

![Figure 4.12](image).

Figure 4.12. Typical room temperature blocking characteristics ($V_{gs} = 0$ V) of fabricated SiC Acc- and Inv-channel BG-MOSFETs with high or low N⁺ JFET doping. BV is defined at I_d = 100 µA.
In contrast, the breakdown voltage for the Inv BG-MOSFET is significantly reduced because the high N⁺ JFET doping concentration (shown in Figure 4.11) leads to earlier avalanche breakdown at the edge of the P⁺ shielding region due to much higher electric field.

Figure 4.13 compares the transfer characteristics at room temperature for the fabricated MOSFETs measured at $V_d=0.1$ V. The threshold voltages ($V_{th}$) extracted at $I_d=1$ mA for Acc C-MOSFET, Acc SG-MOSFET, Inv BG-MOS_H, Acc BG-MOS_H, and Acc BG-MOS_L are 2.00, 1.80, 2.98, 2.04, and 1.72 V, respectively. The $V_{th}$ for all the Acc-channel structures are about 2 V, which is about 1 V lower than that for the Inv BG-MOS_H.

Figure 4.14 shows the measured $C_{gd}$ up to 1000 V for all the Acc-channel structures [7][8]. The $C_{gd}$ for the Inv BG-MOS_H was measured up to only 500 V because of the reduced breakdown voltage. The $C_{gd}$ extracted at $V_d=1000$ V are 5.43, 3.07, 1.04, and 0.96 pF for the Acc C-MOSFET, SG-MOSFET, BG-MOS_H, and BG-MOS_L, respectively. The $C_{gd}$ for the Inv BG-MOS_H shows 2.60 pF at $V_d=500$ V. The higher $C_{gd}$ value in the Inv BG-MOFSET compared with the Acc BG-MOSFETs is due to the higher N⁺ JFET doping concentration.
Figure 4.14. Typical measured reverse transfer capacitance of fabricated SiC C-, SG-, and BG-MOSFETs. The Acc BG-MOS_H and _L have much smaller $C_{gd}$ [7][8].

Figure 4.15 compares the measured gate charge at $V_d=800$ V and $I_d=10$ A of the fabricated Acc MOSFETs [7]. The Inv BG-MOS_H could not be measured because of the lower BV of 520 V as shown in Figure 4.12. A much smaller plateau ($Q_{gd}$) can be observed in the Acc BG-MOSFET

Figure 4.15. Measured gate charge at $V_d=800$ V and $I_d=10$ A of fabricated SiC Acc C-, SG-, and BG-MOSFETs with high or low N$^+$ JFET doping. Much smaller plateau ($Q_{gd}$) is observed in the Acc BG-MOS_H and _L [7].
structures when compared with the other devices. The $Q_{\text{gd}}$ values extracted from the gate voltage plateaus are 15.6, 9.7, 2.7, and 2.5 nC for the Acc C-MOSFET, SG-MOSFET, BG-MOS_H, and BG-MOS_L, respectively.

The $C_{\text{gd}}$ and $Q_{\text{gd}}$ are almost equal for the two $N^+$ JFET doping concentrations in the Acc BG-MOSFETs, which is consistent with the simulation results (Figure 4.5(a) and 4.6(a)). It is therefore experimentally demonstrated for the first time that the BG-MOSFET structures are superior to the C-MOSFET and SG-MOSFET in terms of the reduced $C_{\text{gd}}$ by $5.2 \times$ and $3 \times$, and $Q_{\text{gd}}$ by $5.8 \times$ and $3.6 \times$, respectively.

4.2. Discussions

All the experimental results for all the fabricated devices are summarized in Table 4.2. They are also compared with typical commercial MOSFET (C2M0160120D [14]) in the table.

The measured breakdown voltages for the Acc BG-MOSFETs are close to the C- and SG-MOSFETs, which are sufficient for 1.2 kV-rated devices. The $V_{\text{th}}$, measured at $V_d=0.1$ V and $I_d=1$ mA, for all the Acc-channel devices are about 2 V within the experimental error and they are about 1 V smaller than that for the Inv-channel BG-MOSFET. The BG-MOSFETs show the significantly improved $C_{\text{gd,sp}}$ and $Q_{\text{gd,sp}}$ due to the structural advantages regardless of the $N^+$ JFET doping concentration. It is experimentally demonstrated that the Acc BG-MOSFETs have reduced $C_{\text{gd,sp}}$ by $5.2 \times$ and $3 \times$, and $Q_{\text{gd,sp}}$ by $5.8 \times$ and $3.6 \times$ when compared with the Acc C- and SG-MOSFETs. The Inv BG-MOSFET has a lower $R_{\text{on,sp}}$ due to the higher $N^+$ JFET doping concentration as discussed above, but this results in lower breakdown voltage with much higher electric field and higher $C_{\text{gd,sp}}$. 
It is experimentally confirmed that the higher $N^+$ JFET doping concentration in the Acc BG-MOS structure (Acc BG-MOS_H) produces a smaller on-resistance, resulting in better HF-FOMs by $1.2 \times$ compared to the lower $N^+$ JFET doping case (Acc BG-MOS_L). The Acc BG-MOS_H has the improved HF-FOM $[R_{on} \times C_{gd}]$ by $3.6 \times$ and $2.1 \times$, and HF-FOM $[R_{on} \times Q_{gd}]$ by $4.0 \times$ and $2.6 \times$ compared with the C-MOSFET and SG-MOSFET, respectively.

In addition, the HF-FOM $[R_{on} \times C_{gd}]$ and HF-FOM $[R_{on} \times Q_{gd}]$ for the Acc BG-MOS_H and BG-MOS_L are found to be a factor of $3.3 \times$ and $2.1 \times$, and $4.2 \times$ and $3.5 \times$ smaller than the typical commercial conventional MOSFET, respectively due to the significantly reduced $C_{gd}$ and $Q_{gd}$ with the structural property.

<table>
<thead>
<tr>
<th></th>
<th>$W_{cell}$ [µm]</th>
<th>$BV$ [V]</th>
<th>$V_{th}$ [V]</th>
<th>$C_{gd,sp}$ ($V_d=1kV$) [pF/cm$^2$]</th>
<th>$Q_{gd,sp}$ [nC/cm$^2$]</th>
<th>$*R_{on,sp}$ [mΩ-cm$^2$]</th>
<th>HF-FOM ($R_{on} \times C_{gd}$) [mΩ⋅pF]</th>
<th>HF-FOM ($R_{on} \times Q_{gd}$) [mΩ⋅nC]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Acc MOSFET</td>
<td>5.6</td>
<td>1689</td>
<td>2.00</td>
<td>110</td>
<td>351</td>
<td>5.78</td>
<td>636</td>
<td>2029</td>
</tr>
<tr>
<td>Acc SG-MOS</td>
<td>5.6</td>
<td>1688</td>
<td>1.80</td>
<td>68</td>
<td>216</td>
<td>5.96</td>
<td>406</td>
<td>1287</td>
</tr>
<tr>
<td>Inv BG-MOS_H</td>
<td>7.0</td>
<td>520</td>
<td>2.98</td>
<td>57.8**</td>
<td>-</td>
<td>8.14</td>
<td>407**</td>
<td>-</td>
</tr>
<tr>
<td>Acc BG-MOS_H</td>
<td>7.0</td>
<td>1617</td>
<td>2.04</td>
<td>23</td>
<td>60</td>
<td>8.39</td>
<td>194 (better: $3.3 \times / 2.1 \times$)</td>
<td>503 (better: $4.0 \times / 2.6 \times$)</td>
</tr>
<tr>
<td>Acc BG-MOS_L</td>
<td>7.0</td>
<td>1623</td>
<td>1.72</td>
<td>21</td>
<td>56</td>
<td>10.73</td>
<td>229 (better: $2.8 \times / 1.8 \times$)</td>
<td>596 (better: $3.4 \times / 2.2 \times$)</td>
</tr>
<tr>
<td>Cree (C2M0160120D)</td>
<td>-</td>
<td>-</td>
<td>2.60</td>
<td>(C$_{gd}$) 4.0</td>
<td>(Q$_{gd}$) 14.0</td>
<td>(R$_{on}$) 150</td>
<td>600 (worse: $0.4 \times / 0.3 \times$)</td>
<td>2100 (worse: $0.3 \times / 0.4 \times$)</td>
</tr>
</tbody>
</table>

* $R_{on,sp} @ V_g=25$ V, $I_d=1$ A; includes $R_{p+oon}$ (~1 mΩ-cm$^2$) + $R_{sub}$ (~0.07 mΩ-cm$^2$)

** $C_{gd,sp} @ V_d=500$ V (for INV BG-MOS_H)

### Table 4.2. Experimental results for 1.2 kV Acc- and Inv-channel BG-MOSFETs.
The measured $R_{on,sp}$ reported in Table 4.2 includes the contribution of about 1.7 mΩ-cm$^2$ from the 350 µm thick, 0.02 Ω-cm substrate (0.7 mΩ-cm$^2$) and the parasitic probe-testing (1 mΩ-cm$^2$) resistance. $R_{on,sp}$ and HF-FOMs will be reduced by 20-30% without these parasitic components.

5. Conclusions

Novel 1.2 kV-rated 4H-SiC BG-MOSFET structures have been proposed and successfully fabricated on 150 mm wafers in a foundry for the first time. Both Acc and Inv BG-MOSFET structures have been experimentally demonstrated to have superior $C_{gd}$, $Q_{gd}$, and HF-FOMs characteristics.

The Inv BG-MOSFET shows a little bit lower on-resistance due to the inevitable higher $N^+$ JFET doping concentration above the JFET region, leading to the lower $N^+$ JFET region resistance. However, the higher doping concentration results in the poor breakdown voltage as well as the higher $C_{gd}$, which makes the Inv BG-MOSFET unsuitable for the 1.2 kV device.

In addition, the Acc BG-MOSFETs with two different $N^+$ JFET implant concentrations were compared in the electrical performance. Although their $R_{on}$ is larger than that for the conventional MOSFET, the structures are demonstrated to have significantly improved $C_{gd}$, $Q_{gd}$, and HF-FOMs. The higher doping case produces lower on-resistance with similar $C_{gd}$ and $Q_{gd}$ as expected from the TCAD numerical simulation results.

From the measured electrical characteristics, it has been experimentally confirmed that the BG-MOSFET has improved HF-FOM [$R_{on} \times C_{gd}$] by a factor of 3.6× and 2.1×, and HF-FOM [$R_{on} \times Q_{gd}$] by a factor of 4.0× and 2.6× compared with the C-MOSFET and SG-MOSFET, respectively due to the significantly reduced $C_{gd}$ and $Q_{gd}$. In addition, the Acc BG-MOS_H shows
the improved HF-FOM $[R_{on} \times C_{gd}]$ by 3.1× and HF-FOM $[R_{on} \times Q_{gd}]$ by 4.2× compared with the commercially available conventional planar-gate power MOSFET.

The proposed novel structure can be also applied to vertical power MOSFETs fabricated from other materials to achieve improved HF-FOMs for the high frequency applications.
REFERENCES


[8] K. Han, B. J. Baliga, and W. Sung, “Accumulation channel vs. Inversion channel 1.2 kV rated 4H-SiC Buffered-Gate (BG) MOSFETs: Analysis and Experimental Results,” in Proc.


CHAPTER 5.

Analysis for Various Cell Topologies of 1.2 kV 4H-SiC Planar-Gate MOSFETs and JBSFETs

1. Background & Motivation

In the previous chapters, several 4H-SiC MOSFET structures have been introduced, discussed, and demonstrated to have the improved $C_{gd}$, $Q_{gd}$ and HF-FOMs. As previously discussed, the smaller HF-FOM $[R_{on} \times C_{gd}]$ and HF-FOM $[R_{on} \times Q_{gd}]$ reduce total power loss in high frequency applications. They are independent of device area allowing comparison of device designs and technologies. In addition to the HF-FOMs, a figure-of-merit (FOM), defined as $[C_{iss}/C_{gd}]$ is also important to achieve a gate driver design without false trigger [1]. Therefore, devices with larger FOM $[C_{iss}/C_{gd}]$ ratio with smaller $C_{gd}$ are desirable to prevent shoot-through current during high frequency operation [1][3].

All the MOSFET structures discussed in the previous chapters were designed with the conventional linear cell topology (or a stripe cell topology). The electrical characteristics of Si MOSFETs with various cell topologies have been studied due to different channel and JFET densities [2][3].

In this chapter, the electrical performance of 4H-SiC planar-gate power MOSFETs with various cell topologies will be compared. In 2018, Prof. Baliga proposed a novel octagonal cell topology [4]. The novel octagonal cell topology will be introduced and analyzed to improve the $C_{gd}$, $Q_{gd}$, and HF-FOMs as well as the FOM $[C_{iss}/C_{gd}]$ for the high frequency applications. In addition, 4H-SiC planar-gate power JBSFETs, where JBS diode is monolithically integrated into the MOSFET for more energy efficient operation [5][6], with the various cells will be studied.
1.1. Cell Topologies

Figure 5.1 shows the various cell topologies for the planar-gate power MOSFETs [3][7]. Various cell topologies were proposed and demonstrated for Si power MOSFETs to reduce on-resistance due to the different channel and JFET densities as well as the unit cell area [2][3]. In addition, the impact of the cell topologies on the breakdown voltage is particularly important because each cell topology has different aspect of the electric field distribution at the junctions [9].

Silicon power MOSFETs with various cell topologies (linear, square, hexagonal, and atomic lattice layouts (ALL) for the poly-Si gate electrode) have been previously reported to improve their electrical performance [3][10][11][12]. Experimental results on the 4H-SiC planar-gate power MOSFETs with linear [13], square [9], and hexagonal [14] cell topologies have been reported. In addition, numerical simulation results of a trade-off between increased on-resistance and reduced switching losses for SiC MOSFETs with the ALL design have been reported without experimental data [15]. However, an accurate comparison between the various cell topologies cannot be made based up on the previous works because the devices were made by several groups with different design rules and process flows.

Meanwhile, the octagonal cell topology shown in Figure 5.1(b) has been proposed [4], which is preferable to the ALL layout from the fabrication view point. The proposed octagonal cell topology contains octagonal poly-Si gate regions with straight edges that can be defined more precisely than the circular shapes in the ALL layout making this design preferable for manufacturing products [4]. The octagonal shape allows connecting them using bars in orthogonal directions with the same width as the edges of the octagon. The JFET and channel regions located inside the octagonal poly-Si regions are shown in the figure [4].
The channel current in square, hexagonal, and octagonal MOSFETs flows along 4 to 8 different directions on the Si-face. This has negligible influence on the channel current distribution because there is little difference in the channel mobility on [11\_2] and [11\_0] directions on the Si-face (0001) wafer [15].

In this chapter, a detailed comparison of the measured electrical characteristics for the 1.2 kV 4H-SiC power MOSFETs with linear, square, hexagonal, and octagonal cell topologies using the same design rules and process flow is provided [7][8].

### 1.2. Monolithically Integrated JBS Diode and MOSFET (JBSFET)

The JBSFET, a monolithically integrated 4H-SiC MOSFET and JBS diode, was created to eliminate body-diode conduction [5][6]. The MOSFET and JBS diode share not only the forward conducting layers, but also the edge termination. Therefore, this approach saves the SiC wafer area, reduces the number of packages in half, and eliminates the parasitic inductance between separately packaged devices. Thereby, more energy efficient operation can be expected in typical...
converter topologies, where the MOSFETs are generally employed with an antiparallel JBS diode to prevent body diode conduction [17]. Figure 5.2(a) shows the JBSFET device symbol, describing the monolithic integration of JBS diode in the 4H-SiC MOSFET structure, and Figure 5.2(b) shows the cross-sectional view of the JBSFET, where the Schottky contact area is integrated in the MOSFET unit cell structure [6].

Experimental results for the 4H-SiC JBSFETs have been previously published with the conventional linear cell topology [5][18][19] and the hexagonal cell topology [20]. Once again, the accurate comparison between the cell topologies cannot be made based up on the previous works because of the different design rules and process flows.

A detailed comparison of 1.2 kV rated 4H-SiC JBSFETs with Linear, Hexagonal (Hex), and Octagonal (Oct) cell topologies is provided in this chapter [21]. The three different JBSFET cell topologies were simultaneously fabricated at a 6-inch foundry, X-Fab, using the same process with identical edge termination. Two Oct JBSFET structures with different JBS diode density are included for comparison, so the 3rd quadrant on-state voltage drop ($V_F$) of the JBS diode for each cell topology in the JBSFETs will be compared to each other.
Figure 5.3. (a) MOSFET cell cross-section for all the cell topologies. Cell topologies for fabricated 1.2 kV 4H-SiC MOSFETs with detailed information: (b) Linear, (c) Square, (d) Hexagonal, (e) Octagonal, (f) Split-Gate Octagonal. All the structures have the same channel length of 0.5 µm [8][22].
2. Structure Optimization using TCAD Numerical Simulations

The cross section for all the MOSFETs is shown in Figure 5.3(a) with pertinent structural information, and the top-views for the linear, square, hexagonal, octagonal, and Split-Gate octagonal cell topologies are shown in Figure 5.3(b), (c), (d), (e), (f) with delineation of the polysilicon gate region, base region, N+ source region, JFET region, and contact boundaries [8][22]. The P+ contact region is located orthogonal to the cross section in the linear cell structure to reduce its cell pitch.

2.1. Square & Hexagonal Cell Optimization

Two-dimensional TCAD numerical simulations were performed to optimize the W_{JFET} by rotating the cell structure on the edge “A” in Figure 5.3(a) to approximate the square and hexagonal cell structures [8].

Figure 5.4 shows the simulation results for Q_{gd,sp}, C_{gd,sp}, R_{on,sp}, HF-FOM (R_{on} \times Q_{gd}), HF-FOM (R_{on} \times C_{gd}), and maximum gate oxide electric field (at V_d = 1200 V, V_g = 0 V) as a function of W_{JFET} for the Acc square and hexagonal cell topologies [8]. It can be seen that the R_{on,sp} is almost constant with decreasing W_{JFET} until it is made smaller than 0.7 \mu m. The JFET resistance contribution begins to dominate at this width. The Q_{gd,sp} and C_{gd,sp} reduce with decreasing W_{JFET} (Figure 5.4(a)) as expected due to the smaller JFET area. Consequently, the HF-FOMs are observed (Figure 5.4(b)) to decrease significantly with reduction in W_{JFET}. It is necessary to ensure an oxide electric field below 3 MV/cm in the blocking mode for SiC power MOSFETs to ensure reliable operation [9][23]. The oxide electric field decreases with reduction in W_{JFET} (Figure 5.4(b)) due to the P+ shielding region, with values less than 3 MV/cm at and below 0.9 \mu m. Taking fabrication process tolerances into account, the optimum W_{JFET} was determined to be 0.7 \mu m for the square and hexagonal cell topologies.
2.2. Octagonal Cell Optimization

Figure 5.3(e) shows the top-view of the octagonal cell topology. The P+ shielding region, with N+ source region on top, is placed under the bars. The length of the bar determines the contact area for the N+ source and P+ contact regions and unit cell area in the octagonal cell MOSFETs. If the bar is too short, the contact area becomes too small for fabrication. If the bar is too long, the unit cell area becomes large increasing the specific on-resistance.

Two-dimensional TCAD numerical simulations were performed to optimize the W_JFET by rotating the cell structure on the edge “B” in Figure 5.3(a) to approximate the Acc octagonal cell structure [8]. This approach does not take the poly-Si bars into account, which reduces the specific on-resistance and increases the specific capacitance and gate charge. The JFET region width (W_JFET) in the octagonal cell topology was optimized to minimize its HF-FOMs.

Figure 5.5 shows the simulation results for Q_{gd,sp}, C_{gd,sp}, R_{on,sp}, HF-FOM (R_{on}×Q_{gd}), HF-FOM (R_{on}×C_{gd}), and maximum oxide electric field (at V_d=1200 V, V_g=0 V) as a function of W_JFET [8].
The $Q_{gd,sp}$ and $C_{gd,sp}$ are observed to reduce significantly (Figure 5.5(a)) with decreasing $W_{JFET}$ as expected from the smaller JFET area. The $R_{on,sp}$ is observed to rapidly increase when $W_{JFET}$ becomes smaller than $1.1\ \mu m$ (Figure 5.5(a)) due to an increase in the JFET and drift resistances.

The HF-FOMs are observed to exhibit a minimum value at an optimum $W_{JFET}$ of $1.1\ \mu m$ (Fig. 2(b)). At this value, the gate oxide electric field is suppressed to 2.6 MV/cm. The maximum oxide electric field at the same bias condition for the linear cell MOSFETs with $W_{JFET}$ of 0.7 and 1.1 $\mu m$ is 2.4 and 4 MV/cm, respectively.

The width “$a$” (Figure 5.3(a) and (e)) must be made sufficiently large to allow for contact to the N$^+$ source and P$^+$ contact regions in the octagonal cell design. The width “$b$” can be optimized in the octagonal cell layout to improve performance. The baseline octagonal design has an optimum $W_{JFET}$=1.1 $\mu m$ with $a$=$b$=1.1 $\mu m$. The more compact octagonal cell design has an optimum $W_{JFET}$=1.1 $\mu m$ with $a/2$=$b$=0.55 $\mu m$ (compact octagonal cell) [7][8].
2.3. Split-Gate Octagonal Cell Optimization

A significant improvement in the HF-FOMs for the linear cell, 1.2 kV 4H-SiC planar-gate MOSFET structure has been demonstrated by using the Split-Gate (SG) topology due to reduction in the gate-to-drain overlap area [24][25]. The Split-Gate (SG) structure concept was combined with the octagonal cell topology for the first time to achieve a further improvement in $C_{gd}$, $Q_{gd}$, and HF-FOMs [22].

Figure 5.3(f) shows the top-view of the Split-Gate octagonal cell topology (SG-OCTFET). The SG-OCTFET structure was also optimized using 2-D TCAD numerical simulations by rotating the cell structure as indicated in Figure 5.3(f). Simulations of the Acc SG-OCTFETs were performed with the fixed $W_{JFET}$ of 1.5 $\mu$m and length of $a=1.1$ $\mu$m as shown in Figure 5.6 [22]. The $R_{on,sp}$ (at $V_g=20$ V and $I_d=10$ A) does not change significantly with decreasing “X” width until it becomes less than 0.2 $\mu$m, as shown in Figure 5.6(a). This indicates that the accumulation layer under the gate electrode in the JFET region has minimal impact on the $R_{on,sp}$. As expected, the $C_{gd,sp}$ (at $V_d=1$ kV) and $Q_{gd,sp}$ for the SG-OCTFETs are significantly reduced with decrease of the “X” width as shown in Figure 5.6(a) due to the smaller overlap area between the gate electrode and JFET region. Consequently, the best (lowest) HF-FOM [$R_{on} \times Q_{gd}$] and HF-FOM [$R_{on} \times C_{gd}$] occur at the “X” width of 0.1 $\mu$m as shown in Figure 5.6(b). However, a rapid increase of $R_{on,sp}$ is observed when the “X” width is reduced from 0.2 to 0.1 $\mu$m.

The maximum gate oxide electric field is concentrated at the edge of the poly-Si gate electrode in the split gate structures. The “X” width must be optimized to keep the maximum electric field in the gate oxide below 4 MV/cm for acceptable oxide reliability. As previously discussed in Chapter 3 for the case of linear-cell SG-MOSFETs [24], the numerical simulation results for the octagonal cell SG-MOSFETs show a peak in the oxide electric as the “X” width is
The oxide electric field at the edge of poly-Si gate electrode is suppressed by the proximity of the P+ shielding region for small values of “X” (<0.7 µm), while it is reduced by the proximity of the split poly-Si gates for large values for “X” (>0.9 µm). A maximum value of 4.4 MV/cm for the electric field is observed at X=0.7 to 0.9 µm in Figure 5.6(b). It can be concluded that the “X” width must be smaller than 0.3 µm to keep the oxide electric field below 4 MV/cm while achieving good HF-FOMs. From the simulation results and process alignment tolerances, an optimum value for the “X” width is determined to be 0.3 µm. For this case, 2.6× improved HF-FOM [R_{on}×Q_{gd}] is achieved compared with the octagonal cell with W_{JFET} of 1.5 µm (O_J1.5).

2.4. Electric Field Distribution at Schottky Contact in Various Cell JBSFETs

Figure 5.7(a), (b), (c) shows the linear, hexagonal (Hex), and octagonal (Oct) cell topologies for the accumulation channel (Acc) JBSFETs, respectively, with detailed structural and regional information. The cross section for all the devices along line A-A’ is shown in Figure 5.7(d) [21]. As discussed above, in the Oct cell topology, the JFET and channel regions are varied. The oxide electric field at the edge of poly-Si gate electrode is suppressed by the proximity of the P+ shielding region for small values of “X” (<0.7 µm), while it is reduced by the proximity of the split poly-Si gates for large values for “X” (>0.9 µm). A maximum value of 4.4 MV/cm for the electric field is observed at X=0.7 to 0.9 µm in Figure 5.6(b). It can be concluded that the “X” width must be smaller than 0.3 µm to keep the oxide electric field below 4 MV/cm while achieving good HF-FOMs. From the simulation results and process alignment tolerances, an optimum value for the “X” width is determined to be 0.3 µm. For this case, 2.6× improved HF-FOM [R_{on}×Q_{gd}] is achieved compared with the octagonal cell with W_{JFET} of 1.5 µm (O_J1.5).
surrounded by the P⁺ shielding regions inside the octagonal-shaped poly-Si regions. The poly-Si bars with the same width as the edges of the octagon are used to connect the octagonal poly-Si gate regions just like the octagonal cell MOSFETs. The length of the bar “2a” determines the N⁺, P⁺ Ohmic contact, and JBS Schottky contact areas as well as the unit cell area in the Oct cell topology.

All the fabricated structures have the same JFET width ($W_{\text{JFET}}$) of 1.5 μm and channel length of 0.5 μm. Two bar lengths (a=1.6 μm for the Oct JBSFET design and a=2.8 μm for the Oct_D JBSFET design) were chosen for comparing the electrical performance. The Oct_D design...
has higher JBS diode density to reduce the third quadrant on-state voltage drop. The JBS diode density is defined as (JBS diode area)/(unit cell area).

A low surface electric field at the Schottky contact is achieved in the JBS diode to reduce the leakage current under the high reverse bias [3]. TCAD numerical simulations were performed to examine the electric field at the Schottky contact in the integrated JBS diodes at high reverse bias (V=1.2 kV). The JBS diodes in the Hex and Oct JBSFETs was modelled as a cylindrical structure by rotating the cross-section on the right-hand-side as indicated in Figure 5.8(a) [21]. The

Figure 5.8. (a) TCAD simulation structure for linear and cylindrical (rotated at the right edge) JBS diodes that are monolithically integrated in JBSFETs. (b) Simulation results of electric field distribution at 1.2 kV for linear cell (left) and cylindrical cell JBS diodes (right). (c) Extracted electric field values at 1.2 kV along with the lines marked in red in (b) [21].
simulation for the Linear structure was performed without cell rotation. It can be observed from Figure 5.8(b) that a much smaller electric field is generated at the corner of the P-N junction in the Oct and Hex cells compared with the Linear cell. More importantly, it can be seen in Figure 5.8(c) that a greater reduction of the electric field at the Schottky contact is observed in JBS diodes formed in the Hex and Oct JBSFETs compared with the conventional linear cell topology. This suppresses the large increase in leakage current with increasing reverse bias voltage observed in SiC Schottky diodes [3].

3. Fabrication of 4H-SiC MOSFETs and JBSFETs with Various Cell Topologies

In this section, the fabrication process of the 1.2 kV 4H-SiC MOSFETs and JBSFETs with various cell topologies will be discussed. The devices were fabricated with total 11 masks using the NCSU PRESiCE™ process [26].

Table 5.1 and Table 5.2 summarize the detailed structural parameters for all the fabricated various cell MOSFETs and JBSFETs, respectively.

3.1. Layout Description

Figure 5.9 shows a layout designed by me for the Power America (PA) project - Budget Period 3 (BP3) 1st lot for the 1.2 kV 4H-SiC planar-gate power MOSFET and JBSFET structures with various cell topologies. Total 3 linear, 2 square, 3 hexagonal, and 8 octagonal cell MOSFETs, and 1 linear, 1 hexagonal, and 3 octagonal cell JBSFETs were designed as shown in Figure 5.9. Each structure has slightly different structural dimensions for the detailed comparison of the electrical characteristics.
Table 5.1. Fabricated 1.2 kV 4H-SiC various cell MOSFETs with structural parameters.

<table>
<thead>
<tr>
<th>Cell type</th>
<th>Linear</th>
<th>Square</th>
<th>Hexagonal</th>
<th>Octagonal</th>
</tr>
</thead>
<tbody>
<tr>
<td>*W_{A-B} [µm]</td>
<td>2.8</td>
<td>4.2</td>
<td>4.2</td>
<td>3.8</td>
</tr>
<tr>
<td>a [µm]</td>
<td>1.1</td>
<td>1.6</td>
<td>1.1</td>
<td></td>
</tr>
<tr>
<td>b [µm]</td>
<td>NA</td>
<td></td>
<td></td>
<td>1.1</td>
</tr>
<tr>
<td>L_{CH} [µm]</td>
<td></td>
<td></td>
<td></td>
<td>0.5</td>
</tr>
<tr>
<td>X [µm]</td>
<td>NA</td>
<td></td>
<td></td>
<td>0.3</td>
</tr>
<tr>
<td>W_{JFET} [µm]</td>
<td>0.7</td>
<td>1.1</td>
<td>1.1</td>
<td>0.7</td>
</tr>
<tr>
<td>N_{JFET} [cm^{-3}]</td>
<td>3x10^{16}</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>T_{drift} [µm]</td>
<td>10</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>N_{drift} [cm^{-3}]</td>
<td>8x10^{15}</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*W_{A-B} for Lin_0.7

Table 5.2. Fabricated 1.2 kV 4H-SiC various cell JBSFETs with structural parameters.

<table>
<thead>
<tr>
<th>Cell type</th>
<th>Linear JBSFET</th>
<th>Hex JBSFET</th>
<th>Oct JBSFET</th>
<th>Oct_D JBSFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>W_{A-A} [µm]</td>
<td>6.1</td>
<td>6.6</td>
<td>5.9</td>
<td>7.6</td>
</tr>
<tr>
<td>W_{Sh} [µm]</td>
<td>1.0</td>
<td>1.5</td>
<td>1.1</td>
<td>2.8</td>
</tr>
<tr>
<td>a [µm]</td>
<td>NA</td>
<td></td>
<td>1.6</td>
<td>2.8</td>
</tr>
<tr>
<td>L_{CH} [µm]</td>
<td></td>
<td></td>
<td>0.5</td>
<td></td>
</tr>
<tr>
<td>W_{JFET} [µm]</td>
<td></td>
<td></td>
<td>1.5</td>
<td></td>
</tr>
<tr>
<td>N_{JFET} [cm^{-3}]</td>
<td>3x10^{16}</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>T_{drift} [µm]</td>
<td></td>
<td></td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>N_{drift} [cm^{-3}]</td>
<td>8x10^{15}</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
3.2. Process Flow

All the structures were successfully fabricated simultaneously at 6-inch foundry, X-FAB, TX, using the NCSU PRESiCE™ process with the same design rules for features and alignment tolerances as the conventional MOSFET fabrication process [26].

Total 11 mask layers were designed for the different cell topologies. All the accumulation- and inversion-channel structures have the same active areas of 0.045 cm$^2$ and same hybrid-JTE
edge termination designs [27]. 4H-SiC Si-face (0001) 6-inch wafers (4° tilted toward <1120>) with n-type epitaxial layer ($8 \times 10^{15}$ cm$^{-3}$ doped and 10 µm thick) on N$^+$ substrates were used as the starting material. The conventional MOSFET process flow has already been shown in Chapter 2, so the fabrication process in this section will be focused on the JBSFET structures.

The basic fabrication steps to create the JBSFET are shown in Figure 5.10: The zero alignment mark was etched (Mask 1). The enhanced N$^-$ JFET (Mask 2), P$^+$ shielding (Mask 3), P JTE for the JTE rings of the edge termination regions (Mask 4), P$^+$ contact (Mask 5), and N$^+$ source (Mask 6) were formed by a series of high temperature implantations of N and Al, followed by an implant activation annealing process at 1650°C for 10-min with a carbon cap. A 55 nm thick gate oxide was grown by dry oxidation at 1175 °C, followed by NO interface annealing. An n-type silicided poly-Si gate was then deposited and patterned (Mask 7). An oxide interlayer dielectric
(ILD) was deposited and patterned (Mask 8), followed by a nickel silicide (NiSi) process with an RTA (900 °C) on the both front and backsides. The Ohmic and Schottky contacts were simultaneously formed with this process [5]. The oxide interlayer dielectric on the poly-Si was etched for the gate contact (Mask 9). A 4 µm thick Al layer was deposited and patterned to serve as the source and gate pads (Mask 10). Nitride and polyimide passivation layers were stacked and patterned on the front side to open the source and gate contact areas (Mask 11). A solderable metal stack was lastly deposited on the backside.

4. Experimental Results and Discussions

4.1. Experimental Results for MOSFETs with Various Cell Topologies

The electrical characterization was performed through the static measurement for the fabricated MOSFETs with various cell topologies. At first, the octagonal cell MOSFETs with various W JFET are compared with the optimum linear cell MOSFET with W JFET of 0.7 µm to analyze and demonstrate the new octagonal cell topologies in detail. After that, the various cell topologies such as linear, square, hexagonal, and octagonal cells will be compared to each other.

Figure 5.11 shows typical measured output characteristics at V g=20 V of the fabricated octagonal cell MOSFETs with different W JFET (O_J0.9 to O_J1.5) and the compact design (O_J1.1_C) [7]. The octagonal cells with wider W JFET have lower R on as expected from the simulations (Figure 5.5(a)). The compact design has lower R on for the same W JFET of 1.1 µm as expected. The lower resistance characteristics of the linear cell design with W JFET=0.7 µm is included for comparison.

Figure 5.12 compares the measured C gd up to 1000 V for the fabricated devices [7]. The C gd for the Oct MOSFETs (measured at V d=1000 V) reduces from 2.8±0.5 to 2.3±0.5 to 1.6±0.5 to
1.0±0.5 pF when \( W_{\text{JFET}} \) is reduced from 1.5 to 1.3 to 1.1 to 0.9 \( \mu \)m as expected. In comparison, the \( C_{\text{gd}} \) for the linear cell is 4.79 pF. The \( C_{\text{gd}} \) for the compact design (O_J1.1_C) is 2.2±0.5 pF.
The measured gate charge (at $V_d=800$ V and $I_d=10$ A) for the fabricated devices as shown in Figure 5.13 [7]. It can be observed that the linear cell design has the largest $Q_{gd}$. The $Q_{gd}$ for the Oct MOSFETs becomes smaller with decreasing $W_{JFET}$ as expected. The significant reduced $C_{gd}$

![Figure 5.13](image)

Figure 5.13. Measured gate charge of fabricated linear cell and octagonal cells with different $W_{JFET}$ at $V_d=800$ V and $I_d=10$ A. The plateaus ($Q_{gd}$) get gradually smaller with narrower $W_{JFET}$ in Oct MOSFETs [7].

The measured gate charge (at $V_d=800$ V and $I_d=10$ A) for the fabricated devices as shown in Figure 5.13 [7]. It can be observed that the linear cell design has the largest $Q_{gd}$. The $Q_{gd}$ for the Oct MOSFETs becomes smaller with decreasing $W_{JFET}$ as expected. The significant reduced $C_{gd}$

![Figure 5.14](image)

Figure 5.14. Typical measured output characteristics at $V_g=20$V of fabricated (a) Acc-channel and (b) Inv-channel 1.2 kV MOSFETs with various cell topologies [8].
and $Q_{gd}$ values for the Oct MOSFETs are due to the reduced JFET area compared with the linear-cell design. All the measured data for the octagonal cell topologies is recorded in Table 5.3.

Figure 5.14 shows typical measured output characteristics at $V_g=20$ V of the fabricated Acc and Inv MOSFETs with various cell topologies [8]. The Lin_J#, Sqr_J#, Hex_J#, O_J#, and O_J#_C represent the linear, square, hexagonal, octagonal, and compact octagonal cell topologies, respectively. The numbers next to the cell topologies in the legends indicate the JFET widths in the MOSFETs. The Acc MOSFETs have a lower on-resistance ($R_{on}$) compared with the Inv devices for each cell topology with the same $W_{JFET}$ due to the larger channel mobility [28] as shown in Figure 5.14(a) and (b). Compared with the linear cell, the $R_{on}$ for the Hex_J0.7 is 10% lower, the Sqr_J1.1 is equal, and the O_J1.1_C is 50% larger due to the difference in channel and JFET densities provided in Table 5.4 in the next section (Discussion). The O_J1.1_C has smaller $R_{on}$ compared with the O_J1.1 due to the larger channel density.

The measured transfer characteristics at $V_d=0.1$ V for the fabricated Acc and Inv MOSFETs are shown in Figure 5.15 [8]. As expected, all the cell designs with accumulation- and
inversion-channel have the same threshold voltage \( (V_{\text{th}}) \) of \( 2.06 \pm 0.1 \) and \( 4.18 \pm 0.02 \) V, respectively.

Figure 5.16(a) and (b) show typical measured blocking characteristics of the Acc and Inv MOSFETs with identical edge termination, respectively [8]. The breakdown voltage (BV) was extracted at \( I_d=100 \) μA. An excellent BV over 1600 V is achieved for the linear and octagonal cell designs. In contrast, the BV for the square (Sqr_J1.1) and hexagonal (Hex_J1.1) designs is reduced by \( 200 \sim 300 \) V compared with the linear cell. This is due to localized high electric field concentration at the corners of the square and hexagonal cells [9]. This problem is mitigated in the hexagonal cell design by reducing the JFET width (Hex_J0.7 design) as shown in Figure 5.15(a) and (b).

A larger leakage current \( (10^{-7} \) A) is observed for the Acc octagonal cell designs than \( (10^{-8} \) A) for the linear (Lin_J0.7) and hexagonal (Hex_J0.7) cells in Figure 5.15(b) for drain voltages up to 1400 V [8]. In order to understand this behavior, TCAD simulations were conducted at \( V_d=1.2 \) kV and \( V_g=0 \) V to compare the channel potential barriers for the Acc and Inv MOSFETs near the
gate oxide interface as shown in Figure 5.17 [8]. A smaller potential barrier is observed for the Acc devices compared with the Inv devices (shown in Figure 5.17(a)). Figure 5.17(b) shows the extracted barrier heights for the Acc and Inv MOSFETs with various channel lengths. It can be observed that the barriers get smaller with decreasing channel length. The simulation results demonstrate that the barrier height for both cases is sufficiently large for a channel length of 0.5 µm resulting in the low leakage current for the linear (Lin_J0.7) and hexagonal (Hex_J0.7) cell designs (Figure 5.16(a)). The masking process was optimized for the linear cell topology. Consequently, the size of the P⁺ shielding and N⁺ source regions were not accurately defined for the very small octagonal shapes during the masking process. MOSFETs with the octagonal cell designs may have smaller (<0.5 µm) local channel length leading to the higher leakage current in the Acc octagonal cell designs (Figure 5.16(a)). Although the leakage current for the Acc octagonal cell is one order of magnitude larger than for the Inv octagonal cell, its absolute value (0.1 µA) is well below the typical device specification of 100 µA in data sheets.
The measured $C_{gd}$ (=Crss) for the various cell topologies can be compared in Figure 5.18 for the Acc and Inv devices [8]. The fluctuation in the $C_{gd}$ data at high drain voltages is due to the small values near the measurement limits (0.5 pF) of the equipment. The data for each cell design for the Inv devices was found to be identical to that for the Acc devices due to the same JFET region parameters as shown in Figure 5.18(a) and (b). The $C_{gd}$ is proportional to the JFET area [3]. The $C_{gd}$ for the square and hexagonal topologies is larger than for the linear cell while that for the octagonal cell is much smaller due to the difference in JFET density. The $C_{gd}$ extracted at $V_d=1$ kV for the Acc Lin_J0.7, Sqr_J1.1, Hex_J1.1, Hex_J0.7, O_J1.1, and O_J1.1_C is 4.8±0.5, 17.6, 17.4, 12.9, 1.6±0.5, and 2.2±0.5 pF, respectively. The $C_{gd,sp}$ values at $V_d=0$ V and 1000 V are summarized in Table 5.4 in the next section (Discussion) for all the fabricated devices.

The measured $C_{iss}$ (=Cgs+Cgd) for the various cell topologies are shown in Figure 5.19 for the Acc and Inv devices [8]. At high drain voltages, the $C_{iss}$ becomes equal to $C_{gs}$ because of negligible $C_{gd}$ values. The $C_{gs}$ is determined by the overlap between the gate and the P-base/N+ source regions [3]. The octagonal cell has larger poly-Si gate overlap area while the square and
hexagonal cells have smaller poly-Si gate overlap areas compared with the linear cell. The measured $C_{iss}$ values are consistent with these differences in the gate overlap area. However, the contribution from $C_{gd}$ becomes significant at low drain voltages. Consequently, the $C_{iss}$ for the Sqr_J1.1 and Hex_J1.1 with their large JFET densities becomes greater than that for the linear and

![Graph](a)

![Graph](b)

Figure 5.19. Measured input capacitance ($C_{iss}$) of fabricated (a) Acc and (b) Inv MOSFETs. The Sqr and Hex MOSFETs with $W_{JFET}$ of 1.1 $\mu$m show the smallest $C_{iss}$ values at $V_d=1 \text{kV}$, but the highest values at low $V_d$ [8].

hexagonal cells have smaller poly-Si gate overlap areas compared with the linear cell. The measured $C_{iss}$ values are consistent with these differences in the gate overlap area. However, the contribution from $C_{gd}$ becomes significant at low drain voltages. Consequently, the $C_{iss}$ for the Sqr_J1.1 and Hex_J1.1 with their large JFET densities becomes greater than that for the linear and

![Graph](a)

![Graph](b)

Figure 5.20. Typical measured output capacitance ($C_{oss}$) of fabricated Acc and Inv MOSFETs with various cell topologies. All the structures have similar $C_{oss}$ regardless of the channel types and cell topologies [8].
octagonal cells as shown in Figure 5.19(a) and (b) for the fabricated Acc and Inv devices, respectively. The extracted $C_{iss,sp}$ values at $V_d=1000$ V are provided in Table 5.4 in the next section (Discussion) for all the fabricated devices.

Figure 5.20 compares the measured $C_{oss}$ (= $C_{ds}$+$C_{gd}$) for the various cell topologies [8]. All the cell topologies have the same value of 49.5±0.5 pF at $V_d=1000$ V within measurement error. However, the $C_{oss}$ at $V_d=0$ V shows slightly different values for different cell topologies: Lin J0.7 = 1.47, Sqr J1.1&Hex J1.1 = 1.83, Hex J0.7 = 1.66, O J1.1 = 0.97, O J1.1 C = 1.10 nF. These differences are due to similar $C_{ds}$ values for all the cells but different $C_{gd}$ values (Figure 5.18) due to changes in JFET density for each cell topology.

The measured gate-to-drain charge (at $V_d=800$ V and $I_d=10$ A) for the fabricated Acc- and Inv-channel MOSFETs with the various cell topologies is shown in Figure 5.21 [8]. It can be observed that the Acc square cell (Sqr J1.1) and hexagonal cell (Hex J1.1) have much larger $Q_{gd}$ (30.0±3 nC) than the Acc linear cell while the Acc octagonal cell (O J1.1) has the smallest $Q_{gd}$ (5.3±0.2 nC) due to its significantly smaller JFET area as shown in Figure 5.21(a). Very similar

![Figure 5.21](image-url)

Figure 5.21. Measured gate charge at $V_d=800$ V and $I_d=10$ A of fabricated (a) Acc and (b) Inv MOSFETs. A large gate plateau ($Q_{gsd}$) is observed in the Sqr and Hex designs. Much smaller gate plateau ($Q_{gsd}$) is observed in the Oct designs [8].
results were observed for the Inv devices for each cell topology (shown in Figure 5.21(b)). However, the plateau voltage for the Inv devices was larger due to its larger threshold voltage and lower transconductance ($g_m$) [3]. The extracted values for $Q_{gd,sp}$ are provided in Table 5.4 in the next section (Discussion) for all the cell topologies.

4.2. Experimental Results for Split-Gate Octagonal MOSFETs (SG-OCTFET)

The successfully fabricated Acc SG-OCTFET (O_J1.5_SG) based on the optimization is compared with other octagonal cell topologies (O_J1.5, O_J1.1, O_J1.1_C) in this section.

Figure 5.22 shows typical measured output characteristics at $V_g=20$ V for the fabricated devices [22]. It is observed that the O_J1.5, O_J1.1_C, and O_J1.5_SG have the same $R_{on}$ values at $I_d=10$ A.

Figure 5.23 compares typical measured blocking characteristics of the fabricated MOSFETs with the same Hybrid-JTE edge termination. An excellent breakdown voltage (BV)
over 1600 V extracted at $I_d=100 \mu A$ is achieved for the SG-OCTFET. Similar overall leakage current is observed compared with other devices as shown in the figure.

Figure 5.24 shows the measured $C_{gd}$ up to 1 kV for all the devices [22]. The noise in the $C_{gd}$ data at high drain voltages is caused by the measurement limit of 0.5 pF for the experimental setup.

Figure 5.24. Measured reverse transfer capacitance ($C_{gd}$) of fabricated octagonal cell topologies and SG-OCTFET (O_J1.5_SG) [22].
The $C_{gd}$ extracted at $V_d=1$ kV for the O_J1.5, O_J1.1, O_J1.1_C, O_J1.5_SG devices is $2.8\pm0.5$, $1.6\pm0.5$, $2.2\pm0.5$, $1.2\pm0.5$ pF, respectively. The smallest $C_{gd}$ is observed with the SG-OCTFET.

The measured gate charge (at $V_d=800$ V and $I_d=10$ A) for the fabricated devices is shown in Figure 5.25 [22]. It can be observed that the new split-gate octagonal cell design (O_J1.5_SG) has the smallest $Q_{gd}$ as expected.

All the measured experimental results are summarized in Table 5.3 and 5.4 in the next section (Discussion) for comparison of the devices.

### 4.3. Experimental Results for JBSFETs with Various Cell Topologies

Typical measured output characteristics of the fabricated JBSFETs with various cell topologies are shown in Figure 5.26 [21]. The on-resistance measured at $V_g$ of 20 V for the Hex cell is $1.28\times$ lower than that for the Linear cell case while those for the Oct and Oct_D cells are $1.25\times$ and $2.46\times$ larger than the Linear cell case. This correlates with their smaller channel and
It can be seen from the transfer characteristics in Figure 5.27 that all the Acc JBSFETs have the same threshold voltages of 2.32±0.04 V measured at \( V_d \) of 0.1 V and \( I_d \) of 1 mA [21].

**Figure 5.26.** Typical measured output characteristics at \( V_g=20 \) V of fabricated 1.2 kV Acc JBSFETs with various cell topologies. Active area is 0.045 cm\(^2\) [21].

**Figure 5.27.** Measured transfer characteristics for fabricated Acc JBSFETs with various cell topologies. \( V_{th} \) was extracted at \( I_d=1 \) mA [21].
The measured blocking characteristics of the JBSFETs with identical edge termination are shown in Figure 5.28 [21]. The breakdown voltage (BV) was extracted at \( I_d = 100 \mu A \). The measured BV for the Hex cell design is only 1350 V which may be too low for a 1200 V rated device. Its BV is much lower than for the linear cell due to localized high electric field concentration at the hexagonal shaped corners [9]. The highest BV of 1620 V is observed for the Oct designs due to a reduced electric field in its JFET region. A larger leakage current up to drain voltage of ~1200 V is observed in Figure 5.28 for the Acc Oct cell designs than those for the Linear and Hex cells. As discussed in the previous section with Figure 5.16, the channel potential barrier is sufficiently large for a channel length of 0.5 \( \mu m \) resulting in the low leakage current for the Linear and Hex cell topologies. It is conjectured that the P+ shielding and N+ source regions were not accurately patterned for the Oct cell topologies during the masking process because the photolithography process was optimized for the Linear cell topology. The Oct and Oct_D JBSFETs may have smaller (<0.5 \( \mu m \)) local channel length. It has been demonstrated by numerical
simulations that the channel potential barrier gets reduced with smaller channel length as shown in Figure 5.16. This leads to the higher leakage current observed in the Oct cell designs. Nevertheless, the leakage current for the Oct cell topologies (<0.1 µA) is well below the typical leakage current limit of 100 µA in data sheets.

Figure 5.29. Measured 3\textsuperscript{rd} quadrant characteristics of fabricated Acc JBSFETs with various cell topologies [21].

Figure 5.30. Typical measured reverse transfer capacitance of fabricated JBSFETs with various cell topologies. The Hex cell has higher $C_{rss}$ values while the Oct cell has lower $C_{rss}$ values than the Linear design [21].
The measured third quadrant characteristics for the different JBSFETs are shown in Figure 5.29 [21]. The JBS diodes in the Hex and Oct cell structures have higher on-state voltage drops than the Linear cell case. This is because their JBS diode area density of 0.05 is $3 \times$ smaller than for the Linear cell. The JBS diode on-state voltage drop in the Oct cell topology can be made equal to that of the Linear cell topology by increasing its area density to 0.167 as shown by the Oct_D cell design.

The measured $C_{gd}$ (= $C_{rss}$) for all the devices are shown in Figure 5.30 [21]. The $C_{gd}$ for the Hex cell is larger than that for the Linear cell, while that for the Oct cell is much smaller. This is due to the $C_{gd}$ values being proportional to the JFET area density [3] which is provided in Table 5.5 in the next section (Discussion). The JFET density is defined as (JFET area)/(unit cell area). The $C_{gd}$ values extracted at $V_d=1$ kV for the Linear, Hex, Oct, and Oct_D are 6.39, 14.11, 2.10, and 1.35 pF, respectively.

The measured $C_{iss}$ for all the devices are shown in Figure 5.31 [21]. The $C_{iss}$ consists of $C_{gs}$ plus $C_{gd}$. The $C_{gs}$ is determined by the overlap area between the gate and the N-base/N$^+$ source.
regions [21]. At high drain voltages, the $C_{iss}$ becomes equal to $C_{gs}$ because of negligible $C_{gd}$ values. However, at low drain voltages, the contribution of the $C_{gd}$ becomes significant. The Oct cells have larger $C_{iss}$ values at $V_d$ of 1000 V because of the poly-Si bars add to the gate-source overlap area. However, the Hex cell has the greater $C_{iss}$ at $V_d$ of 0 V as shown in the inset graph in Figure 5.26 due to its larger $C_{gd}$ compared with the Linear and Oct cells.

It can be observed in Figure 5.32 that all the cell topologies have the same $C_{oss} (=C_{ds}+C_{gd})$ of 48.45±0.6 pF at high voltages within measurement accuracy [21]. These results indicate that all the cells have similar $C_{ds}$ and relatively negligible $C_{gd}$ values at $V_d$ of 1000 V.

![Figure 5.32. Typical measured output capacitance ($C_{oss}$) of fabricated JBSFETs with various cell topologies. All the structures have similar $C_{oss}$ values regardless of the cell topologies [21].](image)

The measured gate charge at $V_d$=800 V and $I_d$=10 A for the various JBSFET cell topologies can be compared in Figure 5.33 [21]. Much smaller gate charge ($Q_{gd}$) is observed for the Oct cell JBSFETs compared with the Hex and Linear cell structures due to their significantly smaller JFET area density. The extracted values for $Q_{gd,sp}$ are provided in Table 5.5 in the next section (Discussion) for all the cell topologies. The $Q_{gd,sp}$ values for the Linear, Hex, Oct, and Oct_D are 356, 578, 147, and 84 nC/cm², respectively.
All the experimental results for the 1.2 kV 4H-SiC Acc conventional linear cell, Acc linear cell Split Gate MOSFET (SG-MOSFET) in Chapter 3, and octagonal cell MOSFETs (including SG-OCTFET) with various $W_{JFET}$ (0.9 to 1.5 $\mu$m) are summarized in Table 5.3 [7][22]. The channel and JFET (“X”-portion) densities are calculated as $\text{[channel perimeter]/[unit cell area]}$ and $\text{[JFET(“X”-portion) area]/[unit cell area]}$, respectively. All the designs had breakdown voltages (measured at $I_d=100 \mu$A) above 1600 V which is much larger than the 1.2 kV device rating. The threshold voltages ($V_{th}$), measured at $V_d=0.1$ V and $I_d=1$ mA, are about 2 V for all cases.

The measured $R_{on,sp}$ value for $W_{JFET}=1.1 \mu$m in the octagonal MOSFET is close to that obtained using the simulations (shown in Figure 5.5(a)) and larger than the $R_{on,sp}$ for the linear cell designs. The measured HF-FOMs for the octagonal cell MOSFETs with a $W_{JFET}$ of 1.1 $\mu$m are observed consistent with the simulations as shown in Figure 5.5(b). The optimum octagonal design

![Figure 5.33. Measured gate charge at $V_d=800$ V and $I_d=10$ A of fabricated JBSFETs. A large gate plateau ($Q_{gd}$) is observed in the Hex design. Much smaller gate plateau ($Q_{gd}$) is observed in the Oct design [21].](image)
with $W_{JFET}=1.1 \ \mu m$ (O_J1.1) has better HF-FOM $[R_{on} \times C_{gd}]$ by $1.7 \times$ and HF-FOM $[R_{on} \times Q_{gd}]$ by $1.2 \times$ compared with the linear-cell MOSFET. The compact octagonal design (O_J1.1) has even better HF-FOM $[R_{on} \times C_{gd}]$ by $2.1 \times$ and HF-FOM $[R_{on} \times Q_{gd}]$ by $1.4 \times$ compared with the linear-cell design. In addition, the SG-OCTFET has much superior HF-FOM $[R_{on} \times C_{gd}]$ by $1.8 \times$ and HF-FOM $[R_{on} \times Q_{gd}]$ by $1.6 \times$ compared with the optimized compact octagonal cell (O_J1.1). The SG-

Table 5.3. Experimental results for 1.2 kV 4H-SiC Acc octagonal cell MOSFETs compared with conventional linear MOSFET [7][22].

<table>
<thead>
<tr>
<th>Acc-channel</th>
<th>Lin_J0.7</th>
<th>*Lin_J0.9_SG</th>
<th>O_J1.5</th>
<th>O_J1.3</th>
<th>O_J1.1</th>
<th>O_J0.9</th>
<th>O_J1.1</th>
<th>O_J1.5_SG</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>W_{A-B} [\mu m]</strong></td>
<td>2.8</td>
<td>3.0</td>
<td>5.1</td>
<td>4.8</td>
<td>4.5</td>
<td>4.2</td>
<td>3.8</td>
<td>5.1</td>
</tr>
<tr>
<td>CH. density [\mu m²]</td>
<td>0.36</td>
<td>0.33</td>
<td>0.26</td>
<td>0.26</td>
<td>0.26</td>
<td>0.26</td>
<td>0.38</td>
<td>0.26</td>
</tr>
<tr>
<td>JFET (X) density</td>
<td>0.25</td>
<td>0.10</td>
<td>0.14</td>
<td>0.12</td>
<td>0.1</td>
<td>0.08</td>
<td>0.14</td>
<td>0.05</td>
</tr>
<tr>
<td>BV [V]</td>
<td>1628</td>
<td>1629</td>
<td>1607</td>
<td>1630</td>
<td>1605</td>
<td>1639</td>
<td>1605</td>
<td>1625</td>
</tr>
<tr>
<td>$V_{th}$ [V]</td>
<td>1.96</td>
<td>2.08</td>
<td>2.12</td>
<td>2.06</td>
<td>2.02</td>
<td>2.04</td>
<td>2.12</td>
<td>2.02</td>
</tr>
<tr>
<td>***$R_{on,sp}$ [mΩ·cm²]</td>
<td>5.61</td>
<td>5.30</td>
<td>8.38</td>
<td>9.72</td>
<td>12.8</td>
<td>25.5</td>
<td>8.47</td>
<td>8.51</td>
</tr>
<tr>
<td>$C_{gd,sp}$ ($V_d=1kV$) [pF/cm²]</td>
<td>106</td>
<td>82</td>
<td>62</td>
<td>51</td>
<td>35</td>
<td>22</td>
<td>48</td>
<td>27</td>
</tr>
<tr>
<td>$Q_{gd,sp}$ [nC/cm²]</td>
<td>311</td>
<td>149</td>
<td>233</td>
<td>160</td>
<td>113</td>
<td>67</td>
<td>144</td>
<td>88</td>
</tr>
<tr>
<td>HF-FOM ($R_{on} \times C_{gd}$) [mΩ·pF]</td>
<td>595</td>
<td>435</td>
<td>520</td>
<td>496</td>
<td>449</td>
<td>561</td>
<td>407</td>
<td>230</td>
</tr>
<tr>
<td>HF-FOM ($R_{on} \times Q_{gd}$) [mΩ·nC]</td>
<td>1745</td>
<td>790</td>
<td>1953</td>
<td>1555</td>
<td>1449</td>
<td>1710</td>
<td>1220</td>
<td>749</td>
</tr>
</tbody>
</table>

*Optimized linear cell Split-Gate (SG) MOSFET in Ch. 3 **W_{A-B} for Lin_0.7 and Lin_J0.9_SG ***$R_{on,sp}$ @ $V_g=20V$, $I_d=10A$; includes $R_{sub,sp}$ (~0.7 mΩ·cm²)
OCTFET shows even 1.9× and 1.1× better HF-FOM \([R_{on} \times C_{gd}]\) and HF-FOM \([R_{on} \times Q_{gd}]\) compared with the linear SG-MOSFET, respectively, due to the smaller “X” density.

All the experimental results on the various cell topologies are summarized in Table 5.4 together with structural information [8][22]. The optimum octagonal (O_J1.1), compact octagonal (O_J1.1_C), and Split-Gate octagonal (O_J1.1_SG) cells are also included in the table.

The breakdown voltage of devices with the square and hexagonal cell topologies with JFET widths of 1.1 µm (i.e. Sqr_J1.1 and Hex_J1.1) was found to be reduced by 200-300 V as discussed in the previous section. The breakdown voltage of all other cell designs exceeded 1600 V. All of the Acc MOSFET cell topologies have 1.3~2.0× smaller (superior) HF-FOM \([R_{on} \times Q_{gd}]\) compared to the Inv counterparts due to the lower on-resistance arising from the higher channel mobility.

The Acc square and hexagonal cell topologies (Sqr_J1.1 & Hex_J1.1) have similar \(R_{on,sp}\) to the Acc linear cell topology (Lin_J0.7). However, they have: (a) worse FOM \([C_{iss}/C_{gd}]\) by a factor of 4.4×, (b) worse HF-FOM \([R_{on} \times C_{gd}]\) by a factor of 3.6×, and (c) worse HF-FOM \([R_{on} \times Q_{gd}]\) by a factor of 2.1×. These differences are due to the 1.82× larger JFET density with the wide JFET width (1.1 µm) in the square and hexagonal cell topology. Similar results are observed for the Inv devices.

The Acc hexagonal cell topology with the optimized JFET width (Hex_J0.7) has 1.2× smaller \(R_{on,sp}\) compared with the linear cell topology (Lin_J0.7) due to the higher JFET density. However, it has: (a) worse FOM \([C_{iss}/C_{gd}]\) by a factor of 3.0×, (b) worse HF-FOM \([R_{on} \times C_{gd}]\) by a factor of 2.3×, and (c) worse HF-FOM \([R_{on} \times Q_{gd}]\) by a factor of 1.1×. These differences arise from the 1.34× larger JFET density in the hexagonal cell topology. Similar results are found for the Inv devices.
Table 5.4. Experimental results for 1.2 kV 4H-SiC MOSFETs with various cell topologies [8][22].

<table>
<thead>
<tr>
<th>CH. type</th>
<th>Lin_J0.7</th>
<th>Sqr_J1.1</th>
<th>Hex_J1.1</th>
<th>Hex_J0.7</th>
<th>O_J1.1</th>
<th>O_J1.1_C</th>
<th>O_J1.5_SG</th>
</tr>
</thead>
<tbody>
<tr>
<td>Acc</td>
<td>2.8</td>
<td>4.2</td>
<td>4.2</td>
<td>3.8</td>
<td>4.5</td>
<td>3.8</td>
<td>5.1</td>
</tr>
<tr>
<td>Inv</td>
<td>0.295</td>
<td>0.295</td>
<td>0.360</td>
<td>0.259</td>
<td>0.377</td>
<td>0.256</td>
<td></td>
</tr>
<tr>
<td>CH. den. [µm]</td>
<td>0.357</td>
<td>0.357</td>
<td>0.357</td>
<td>0.360</td>
<td>0.259</td>
<td>0.377</td>
<td>0.256</td>
</tr>
<tr>
<td>JFET(X) density</td>
<td>0.250</td>
<td>0.455</td>
<td>0.455</td>
<td>0.334</td>
<td>0.098</td>
<td>0.143</td>
<td>0.052</td>
</tr>
<tr>
<td>BV [V]</td>
<td>1628</td>
<td>1726</td>
<td>1338</td>
<td>1467</td>
<td>1605</td>
<td>1661</td>
<td>1605</td>
</tr>
<tr>
<td>Vth [V]</td>
<td>1.96</td>
<td>4.16</td>
<td>2.16</td>
<td>4.18</td>
<td>2.14</td>
<td>4.16</td>
<td>2.02</td>
</tr>
<tr>
<td>**R_{on,sp} [mΩ⋅cm²]</td>
<td>5.61</td>
<td>9.60</td>
<td>5.53</td>
<td>9.79</td>
<td>5.50</td>
<td>9.71</td>
<td>4.87</td>
</tr>
<tr>
<td>C_{iss,sp} (V_d=1 kV) [nF/cm²]</td>
<td>28.2</td>
<td>31.3</td>
<td>23.8</td>
<td>26.7</td>
<td>22.9</td>
<td>25.6</td>
<td>25.6</td>
</tr>
<tr>
<td>C_{oss,sp} (V_d=1 kV) [pF/cm²]</td>
<td>1062</td>
<td>1107</td>
<td>1058</td>
<td>1093</td>
<td>1049</td>
<td>1089</td>
<td>1096</td>
</tr>
<tr>
<td>C_{gd,sp} (V_d=0 V) [nF/cm²]</td>
<td>17.8</td>
<td>13.2</td>
<td>28.9</td>
<td>27.1</td>
<td>29.6</td>
<td>26.5</td>
<td>23.5</td>
</tr>
<tr>
<td>C_{gd,sp} (V_d=1 kV) [pF/cm²]</td>
<td>106</td>
<td>97</td>
<td>392</td>
<td>392</td>
<td>386</td>
<td>389</td>
<td>286</td>
</tr>
<tr>
<td>Q_{gd,sp} [nC/cm²]</td>
<td>311</td>
<td>311</td>
<td>667</td>
<td>733</td>
<td>644</td>
<td>733</td>
<td>400</td>
</tr>
<tr>
<td>FOM (C_{iss}/C_{gd})</td>
<td>266</td>
<td>323</td>
<td>61</td>
<td>68</td>
<td>59</td>
<td>66</td>
<td>90</td>
</tr>
<tr>
<td>HF-FOM (R_{on,sp}C_{gd}) [mΩ⋅pF]</td>
<td>595</td>
<td>931</td>
<td>2168</td>
<td>3838</td>
<td>2123</td>
<td>3777</td>
<td>1393</td>
</tr>
<tr>
<td>HF-FOM (R_{on,sp}Q_{gd}) [mΩ⋅nC]</td>
<td>1745</td>
<td>2986</td>
<td>3689</td>
<td>7176</td>
<td>3542</td>
<td>7117</td>
<td>1948</td>
</tr>
</tbody>
</table>

*W_{A-B} for Lin_0.7  **R_{on,sp} @ V_{g}=20V, I_d=10A; includes R_{sub} (~0.7 mΩ⋅cm²)
The octagonal cell topology has much smaller $C_{gd,sp}$ and $Q_{gd,sp}$, but larger $R_{on,sp}$ due to its smaller channel and JFET densities. The Acc compact octagonal cell topology (O_J1.1_C) has $1.5\times$ larger $R_{on,sp}$ compared with the conventional linear MOSFETs (Lin_J0.7). However, it has: (a) superior FOM [$C_{iss}/C_{gd}$] by a factor of $2.9\times$, (b) superior HF-FOM [$R_{on}\times C_{gd}$] by a factor of $1.5\times$, and (c) superior HF-FOM [$R_{on}\times Q_{gd}$] by a factor of $1.4\times$ in spite of the larger $R_{on,sp}$. These differences are due to the $1.75\times$ smaller JFET density in the compact octagonal cell design. Similar results are observed for the Inv devices. In addition, the Acc Split-Gate octagonal cell design (SG-OCTFET, O_J1.5_SG) has (a) much superior FOM [$C_{iss}/C_{gd}$] by a factor of $4.6\times$, (b) HF-FOM [$R_{on}\times C_{gd}$] by a factor of $2.6\times$, and (c) HF-FOM [$R_{on}\times Q_{gd}$] by a factor of $2.3\times$ compared with the conventional linear MOSFETs due to the reduced gate-to-drain overlap with the split gate structures.

The experimental results for the fabricated 1.2 kV 4H-SiC JBSFETs are summarized in Table 5.5 with structural information [21]. The channel (CH.), JFET, and JBS diode densities for all the cell topologies were calculated as (channel perimeter)/(unit cell area), (JFET area)/(unit cell area), and (JBS diode area)/(unit cell area), respectively. The Hex cell has the lowest $R_{on,sp}$ due to the biggest channel density, but its BV of 1350 V may be insufficient for a 1200 V rated device.

The Oct cell has excellent HF-FOM [$R_{on}\times Q_{gd}$] by $1.9\times$ and $2.5\times$, and FOM [$C_{iss}/C_{gd}$] by $5.1\times$ and $10.1\times$ with superior $C_{gd,sp}$ and $Q_{gd,sp}$ compared with Linear and Hex JBSFETs, respectively. However, larger 3rd quadrant on-state voltage drop is observed for this design than the Linear cell case because of the $3\times$ smaller JBS diode area density.

The Oct_D cell has $2.5\times$ higher $R_{on,sp}$ due to the low channel density, but it has much superior $C_{gd,sp}$ ($4.7\times$) and $Q_{gd,sp}$ ($4.2\times$) than Linear cell JBSFET. As a consequence, the Oct_D JBSFET has superior HF-FOM [$R_{on}\times Q_{gd}$] by $1.7\times$ and $2.2\times$ compared with Linear and Hex
Table 5.5. Experimental results for 1.2 kV 4H-SiC JBSFETs with various cell topologies [21].

<table>
<thead>
<tr>
<th>Acc-channel</th>
<th>Linear JBSFET</th>
<th>Hex JBSFET</th>
<th>Oct JBSFET</th>
<th>Oct_D JBSFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>$W_{AA}$ [µm]</td>
<td>6.1</td>
<td>6.6</td>
<td>5.9</td>
<td>7.6</td>
</tr>
<tr>
<td>$W_{Sh}$ [µm]</td>
<td>1.0</td>
<td>1.5</td>
<td>1.1</td>
<td>2.8</td>
</tr>
<tr>
<td>CH. density [µm$^{-1}$]</td>
<td>0.164</td>
<td>0.211</td>
<td>0.193</td>
<td>0.116</td>
</tr>
<tr>
<td>JFET density</td>
<td>0.246</td>
<td>0.403</td>
<td>0.109</td>
<td>0.065</td>
</tr>
<tr>
<td>JBS diode density</td>
<td>0.164</td>
<td>0.052</td>
<td>0.054</td>
<td>0.167</td>
</tr>
<tr>
<td>$BV$ [V]</td>
<td>1556</td>
<td>1351</td>
<td>1625</td>
<td>1618</td>
</tr>
<tr>
<td>$V_{th}$ [V]</td>
<td>2.34</td>
<td>2.28</td>
<td>2.26</td>
<td>2.36</td>
</tr>
<tr>
<td>3rd $V_F$ (@ 5A) [V]</td>
<td>1.89</td>
<td>2.34</td>
<td>2.41</td>
<td>1.91</td>
</tr>
<tr>
<td>$^*R_{on,sp}$ [mΩ-cm$^2$]</td>
<td>8.83</td>
<td>6.90</td>
<td>11.00</td>
<td>21.71</td>
</tr>
<tr>
<td>$C_{iss,sp}$ [nF/cm$^2$]</td>
<td>17.7</td>
<td>19.7</td>
<td>30.0</td>
<td>26.4</td>
</tr>
<tr>
<td>$C_{oss,sp}$ [nF/cm$^2$]</td>
<td>1.08</td>
<td>1.06</td>
<td>1.07</td>
<td>1.09</td>
</tr>
<tr>
<td>$C_{gd,sp}$ [pF/cm$^2$]</td>
<td>142</td>
<td>314</td>
<td>47</td>
<td>30</td>
</tr>
<tr>
<td>$Q_{gd,sp}$ [nC/cm$^2$]</td>
<td>356</td>
<td>578</td>
<td>147</td>
<td>84</td>
</tr>
<tr>
<td>FOM ($C_{iss} / C_{gd}$) [mΩ⋅pF]</td>
<td>125</td>
<td>63</td>
<td>638</td>
<td>880</td>
</tr>
<tr>
<td>HF-FOM ($R_{on} \times C_{gd}$) [mΩ⋅pF]</td>
<td>1254</td>
<td>2167</td>
<td>517</td>
<td>651</td>
</tr>
<tr>
<td>HF-FOM ($R_{on} \times Q_{gd}$) [mΩ⋅nC]</td>
<td>3143</td>
<td>3988</td>
<td>1617</td>
<td>1824</td>
</tr>
</tbody>
</table>

*$R_{on,sp}$ @ $V_g$=20V, $I_d$=10A; includes $R_{sub}$ (~0.7 mΩ-cm$^2$)

JBSFETs, respectively. In addition, its FOM [$C_{iss}/C_{gd}$] is $7.0 \times$ and $14.0 \times$ better than the Linear and Hex JBSFETs, respectively.
5. Conclusions

The 1.2 kV rated 4H-SiC accumulation-channel (Acc) and inversion-channel (Inv) MOSFETs were successfully fabricated in a 6-inch foundry, X-fab with various cell topologies using the same design rules and process flow. The octagonal cell MOSFET has been proposed and demonstrated to have much smaller $C_{gd}$ and $Q_{gd}$ compared with the linear cell topology for the first time. The larger $R_{on,sp}$ with smaller channel and JFET densities is traded off against reduced $C_{gd}$ and $Q_{gd}$ to achieve significantly improved HF-FOMs. TCAD numerical simulations indicated an optimum octagonal design with JFET width of 1.1 $\mu$m for achieving minimum HF-FOMs. The measured values for all the device parameters were consistent with the simulations.

It has been experimentally demonstrated that the compact octagonal design improves the HF-FOM [$R_{on} \times C_{gd}$] by a factor of 2.1× and HF-FOM [$R_{on} \times Q_{gd}$] by a factor of 1.4× compared with the conventional linear-cell MOSFET, with identical process flow. In addition, the octagonal cell topology has a much superior FOM [$C_{iss}/C_{gd}$] to prevent shoot-through during high frequency switching.

Electrical characteristics of 1.2 kV rated 4H-SiC split-gate octagonal cell power MOSFETs have been experimentally quantified for the first time allowing comparison with other technologies. The datasheet for the latest 600 V COOLMOS product (IPL60R365P7) has $R_{on}=310$ m$\Omega$ and $Q_{gd}=4$ nC leading to HF-FOM [$R_{on} \times Q_{gd}$] =1240. The datasheet for a state-of-the-art 1.2 kV SiC power MOSFET product (CREE C2M0160120D) with linear cell topology has $R_{on}=160$ m$\Omega$ and $Q_{gd}=14$ nC leading to HF-FOM [$R_{on} \times Q_{gd}$]=2240, which is not competitive with the 600 V Si COOLMOS product. This work demonstrates for the first time that a HF-FOM [$R_{on} \times Q_{gd}$] 1.66-times better than the 600 V COOLMOS product can be achieved in a 1.2 kV SiC power MOSFET by using the SG-OCTFET topology, which opens new application opportunities for 1.2 kV SiC power MOSFETs.
The novel 1.2 kV 4H-SiC octagonal cell JBSFET was also successfully fabricated with the linear and hexagonal cell topologies for the first time using the same process flow at the X-fab. The on-state voltage drop for the integrated JBS diode in the octagonal cell JBSFET was found to be equal to that of the JBS diode in the linear cell design when its area density was made the same. It is experimentally demonstrated that the octagonal cell JBSFETs show superior HF-FOMs and FOM \( \frac{C_{iss}}{C_{gd}} \) compared with other cell topologies just like the octagonal MOSFETs.

In conclusion, the best HF-FOMs were measured for the octagonal cell topology making it the best choice for high frequency applications where switching losses dominate over on-state power loss, and the smallest \( R_{on,sp} \) was observed for the hexagonal cell topology making it the best choice for low frequency applications where on-state power loss is more important than switching losses.
REFERENCES


CHAPTER 6.

Summary and Future Work

1. Major Accomplishment

1.2 kV-rated 4H-SiC Planar-Gate Power MOSFETs have been extensively researched to improve the high speed switching capability by reduction of the MOSFET’s reverse transfer capacitance (C_{gd}) and gate-to-drain charge (Q_{gd}) because they are the dominant components limiting the switching speed. The main aim, therefore, is to achieve low values for the High-Frequency Figures-of-Merit (HF-FOMs - [R_{on} \times C_{gd}], [R_{on} \times Q_{gd}]).

An extensive study of the JFET region parameter optimizations for conventional 1.2 kV 4H-SiC Planar-Gate Power MOSFETs has been carried out with analytical models and TCAD numerical simulations to reduce R_{on}, C_{gd}, and Q_{gd}. The MOSFETs with various JFET region parameters were fabricated on 6-inch wafers and characterized. It has been experimentally confirmed that the enhanced JFET doping concentration is essential to achieve the smaller C_{gd} and Q_{gd} without an increase in the R_{on}, and improve the blocking characteristics of the 1.2 kV 4H-SiC MOSFETs.

A 1.2 kV 4H-SiC Split-Gate MOSFET (SG-MOSFET) structure has been researched to improve the electrical characteristics and successfully fabricated using the exactly same fabrication process as the conventional MOSFET process. It has been experimentally verified that the SG-MOSFET has 2.4× smaller HF-FOM [R_{on} \times Q_{gd}] compared with the optimized conventional Planar-Gate MOSFET for the first time. Moreover, the SG-MOSFETs have reduced rate of increase in R_{on} with temperature when compared with typical commercial power MOSFETs, leading to the superior HF-FOMs at elevated temperatures. Therefore, the 4H-SiC SG-MOSFETs have excellent
characteristics for high frequency applications not only at room temperature but also at elevated temperatures.

For further improvement of the HF-FOMs, a novel 1.2 kV 4H-SiC Buffered-Gate MOSFET (BG-MOSFET) structure has been discussed and fabricated. It has been experimentally demonstrated to have superior HF-FOMs with successfully fabricated devices on 6-inch wafers for the first time. The BG-MOSFET is demonstrated to have $4.0\times$ and $2.6\times$ smaller HF-FOM $[R_{on}\times Q_{gd}]$, and $3.6\times$ and $2.1\times$ smaller HF-FOM $[R_{on}\times C_{gd}]$, when compared to the conventional Planar-Gate MOSFET and Split-Gate MOSFET, respectively, due to the structural advantages. In addition, it shows the improved HF-FOM $[R_{on}\times C_{gd}]$ by $3.1\times$ and HF-FOM $[R_{on}\times Q_{gd}]$ by $4.2\times$ compared with the typical commercial power MOSFET.

The 1.2 kV rated Planar-Gate power MOSFETs with various cell topologies have been extensively researched to improve the electrical characteristics with different channel and JFET densities:

A 1.2 kV rated 4H-SiC MOSFET with octagonal-cell topology has been fabricated and experimentally demonstrated to achieve the improved HF-FOMs due to the reduced JFET densities for the first time. The octagonal cell topology has octagonal gate regions with straight edges that can be defined more precisely making this design preferable from the fabrication point of view.

A detailed comparison of the 1.2 kV 4H-SiC power MOSFETs with linear, square, hexagonal, and octagonal cell topologies successfully fabricated on 6-inch wafers using the same design rules and process flow as the conventional linear-cell MOSFETs has been discussed. It has been experimentally demonstrated that (a) the hexagonal cell topology has $1.15\times$ better $R_{on}$, but $1.12\times$ worse HF-FOM $[R_{on}\times Q_{gd}]$; (b) the octagonal cell topology has $1.5\times$ worse $R_{on}$, but $1.4\times$ better HF-FOM $[R_{on}\times Q_{gd}]$ when compared with the standard linear cell topology.
A 1.2 kV rated 4H-SiC Split-Gate octagonal MOSFET (SG-OCTFET) has been fabricated and experimentally demonstrated to have the improved electrical characteristics for the first time. The SG-OCTFETs have the Split-Gate (SG) concept combined with the octagonal cell topology so that the further improvement in $C_{gd}$, $Q_{gd}$, and HF-FOMs is achieved. The Split-Gate octagonal cell topology has 1.5× worse on-resistance and 2.3× better HF-FOM [$R_{on}\times Q_{gd}$] compared with the conventional linear cell MOSFET.

All the octagonal cell topologies show a much superior [$C_{iss}/C_{gd}$] FOM compared to the other cell topologies, so more reliable operations are expected by preventing the shoot-through during high frequency switching.

2. Future Work

Although the superior HF-FOMs were achieved with the novel structures, the specific-on-resistance ($R_{on,sp}$) of ~5.5 mΩ⋅cm² is larger than the state-of-the-art value (2.7 mΩ⋅cm²) according to the published ISPSD 2014 conference paper by Cree Wolfspeed. Therefore, the achievement of the reduced $R_{on,sp}$ is the main goal of future work.

The substrate resistance can be reduced by thinning the substrate thickness. Currently, all the devices have the same substrate thickness of 350 µm with the substrate resistivity of 0.02 Ω⋅cm, leading to the specific substrate resistance ($R_{sub,sp}$) of 0.7 mΩ⋅cm². If the substrate thickness is reduced to 100 µm, the $R_{sub,sp}$ would be 0.2 mΩ⋅cm², which is about 70% reduction. The substrate thinning technique is therefore simple, but a very effective way to reduce the on-resistance.

As discussed in the previous chapters, the contribution of the channel resistance to the total on-resistance is very big. For the smaller total on-resistance, it is necessary to achieve the reduced channel resistance, and it can be reduced by making the channel shorter. In the NCSU PRESiCE™
process, the base regions (channel) of all the fabricated Planar-Gate power MOSFETs are defined by the separately aligned P+ shielding and N+ source regions. A self-aligned process, which is a technique that the P+ shielding and N+ source regions are aligned to each other without a mask, is used to form the base regions for the shorter channel lengths to eliminate the possible misalignment during the fabrication process. Therefore, the self-aligned process should be developed in order to improve and stabilize the electrical performance. It should be noted that the Short-Circuit (SC) ruggedness performance of the device with the shorter channel lengths will be traded-off with the reduced on-resistance because of higher saturation current.

In addition, the smaller channel resistance can be achieved with the reduced gate oxide thickness because the channel resistance is inversely proportional to the gate oxide capacitance ($C_{ox}$) which is increased with the reduced gate oxide thickness. In this case, the careful gate oxide reliability study is required to confirm that the MOSFETs with the thin gate oxide have the improved electrical characteristics without any possible performance degradation.

Lastly, a current spreading layer (CSL) below the P+ shielding region is also helpful to reduce the $R_{on,sp}$. This layer can be formed with the deeper n-type implant when the enhanced JFET region is formed, so no additional mask is required. However, it increases the electric field at the junction between the P+ shielding region and CSL with high drain bias at the forward blocking mode. Therefore, the optimization of the layer should be conducted carefully for the better $R_{on,sp}$ without any degradation of the blocking characteristics.
Comprehensive Physics of Third Quadrant Characteristics for Accumulation- and Inversion-Channel 1.2 kV 4H-SiC MOSFETs

Detailed physics of the third quadrant electrical characteristics of 1.2 kV rated 4H-SiC accumulation (Acc) and inversion (Inv) channel MOSFETs, based up on experimentally measured data and TCAD numerical simulations, are described in this section [1]. The power MOSFETs with various channel lengths (0.3, 0.5, 0.8, 1.1 µm) used in this study were fabricated in a 6-inch commercial foundry. Numerical simulations verified that there are two current paths in the 3rd quadrant: (i) through the base region and (ii) through the p-n body diode.

It is demonstrated that the Acc MOSFETs have a smaller 3rd quadrant knee voltage ($V_{knee}$) of -1.2 V compared with -1.9 V for the Inv MOSFETs (at $V_g=0$ V and room temperature). Numerical simulations show that this difference is due to a smaller potential barrier for electron transport from the drain to the source in the base region for accumulation channel devices than inversion channel devices. Acc devices are shown to have lower voltage drop in the 3rd quadrant.

1. Introduction

In applications, the SiC MOSFETs are generally employed with an anti-parallel JBS diode for fast switching and inactivation of the internal p-n body diode [2]. It has been found that the internal bipolar p-n body diode of the SiC MOSFETs undergoes performance degradation with generation of stacking faults (SFs) originating from basal plane dislocation (BPDs) in epi-layers [3][4]. In order not to activate the p-n body diode, monolithically integrated MOSFET and JBS diode (JBSFET) structures have been proposed and demonstrated by many groups [5][6][7].
Nevertheless, the possibility of use of the p-n body diode in the applications is of great interest because of cost and size benefits [8]. Previous studies of the internal body diode and third quadrant characteristics of 4H-SiC power MOSFETs have focused on the current flow paths [9][10]. Detailed physics of electron transport was not discussed and only inversion-channel devices were analyzed in the previous reports. The previous report [10] concluded that third quadrant current flow occurs exclusively across the p-n body diode when V_g=0 V. This is inconsistent with our measured data.

This section provides a comprehensive discussion of the physics of current transport in the 3rd quadrant highlighting the difference between accumulation-channel (Acc) and inversion-channel (Inv) MOSFETs for the first time. The 1.2 kV rated 4H-SiC Acc and Inv MOSFETs were fabricated with 4 different channel lengths in a 6 inch commercial foundry. An improved understanding of current transport in the 3rd quadrant has been developed based up on measured data and TCAD numerical simulations.

2. Device Structure and Fabrication Technology

A cross-sectional schematic view of the fabricated 1.2 kV Acc and Inv 4H-SiC MOSFETs is shown in Figure A.1 with detailed structural information. P-base and N-base regions are used for the Inv and Acc devices, respectively. The implant profiles for the Acc and Inv devices with the P⁺ shielding region were previously published [11]. MOSFETs with 4 different channel lengths (L_CH) were fabricated simultaneously at a 6-inch foundry, X-Fab, using the PRESiCETM 11-mask NCSU fabrication process [12]. The active area for all the devices was 0.045 cm². A Si-face (0001) 4H-SiC 6-inch wafer with a 10 μm thick and 8×10¹⁵ cm⁻³ doped n-type epitaxial layer grown on an N⁺ substrate was used as the starting material.
3. Experimental Results and Analysis

Typical measured 3rd quadrant I-V characteristics at $V_g=0$ V and room temperature for the fabricated Acc- and Inv-channel MOSFETs with $L_{CH}=0.5$ µm are shown in Figure A.2. It can be observed that the Acc and Inv devices have a different knee voltage ($V_{knee}$) of about -1.2 and -1.9 V at $V_g=0$ V, respectively, which is well below the typical built-in potential of a SiC p-n diode ($\approx 2.6$ V) [13]. An inflexion point $V_{INFL}$ in the I-V characteristics for both Acc and Inv MOSFETs is observed at around -2.8 V.

Two-dimensional TCAD numerical simulations were conducted to elucidate the physics for the 3rd quadrant characteristics using the parameters shown in Figure A.1. A P$^+$ ohmic contact is located orthogonal to the cross-section in the actual devices. An additional P$^+$ contact terminal was added on the side of the P$^+$ shielding region in the simulations to represent the actual fabricated device cell structure.
Current flow in the 3rd quadrant with $V_g = 0$ V can occur either via the p-n body diode or base region under the gate. The transport of electrons from the drain to the source via the base region is governed by the potential barrier. The potential barriers for electrons (shown in Figure A.3) near the gate oxide interface, marked as a yellow dashed line in Figure A.1, were obtained by numerical simulations at $V_g = V_d = 0$ V for the Acc and Inv MOSFETs with $L_{CH} = 0.5$ µm. It can be seen that the potential barriers for the electron transport from the drain to the source for the Acc
and Inv devices are 1.2 and 1.9 V, respectively. These values match the experimentally observed $V_{knee}$ which was extracted at $I_d=-50$ mA in Figure A.2 for the two cases providing conclusive evidence that the current flow in the 3rd quadrant is determined by the observed potential barrier.

The distribution of the total current density for the Acc and Inv MOSFETs with $L_{CH}=0.5 \mu m$ was obtained from the simulations. Figure A.4 shows the cross-sectional images of the current distribution at $V_g=0$ V for various values of $V_d$: a. 0 V; b. -1.2 V; c. -1.9 V; d. -2.8 V; and e. -5.0 V as marked in Figure A.2. The results in Figure A.4b. and c. on the left clearly show that the current begins conducting through the base at $V_d=-1.2$ V for the Acc case; while the results in Figure A.4b. and c. on the right clearly show that the current begins conducting through the base at $V_d=-1.9$ V for the Inv case. It is also observed that the current flows through the p-n body diode for both the devices at $V_d=-2.8$ V as shown in Figure A.4d. and e. for both cases.

These simulation results demonstrate that there are two current conduction paths: (i) electron current ($I_e$) through the base, and (ii) hole current ($I_h$) through the p-n body diode. The electron current flow occurs when they overcome the barrier in the base. The required $V_d$ to overcome the barrier is the $V_{knee}$.
The experimental data in Figure A.2 shows a negative inflexion in current (lower than expected) at $V_d=-2.8$ V, where the total current increases at a reduced rate with increasing drain bias. Numerical simulations were performed to understand this phenomenon. Two different simulation variables were tried to reproduce the observed inflexion: (i) various electron ($\tau_e$) and hole ($\tau_h$) lifetimes, and (ii) traps in the P$^+$ shielding region. It has been reported that an acceptor-type trap located at ($E_C-0.27$ eV) and a donor-type trap located at ($E_V+0.42$ eV) are distributed in the P$^+$ shielding region by the Al implantation with the trap concentrations dependent on the implanted Al concentration [14][15]. Both acceptor and donor traps with concentration of $10^{19}$ cm$^{-3}$ were included in the simulations. The trap density can be larger than the P$^+$ shielding region doping concentration because they are created by multiple defects generated by each implanted Al atom due to the high implant energy.

Figure A.5(a) shows the total current, $I_e$, and $I_h$ obtained from the simulated 3$^{rd}$ quadrant I-V characteristics for the Acc MOSFET with $L_{CH}=0.5$ $\mu$m with and without the traps in the P$^+$ shielding region using various $\tau_e$ and $\tau_h$. The current $I_e$ flows from source contact into N$^+$ source region, and the current $I_h$ flows from P$^+$ contact into the P$^+$ region. When the simulation is performed without the traps and with $\tau_e=\tau_h>10$ ns, the total current increases at a faster rate with increasing drain bias when the p-n body diode turns-on. This is the expected behavior because of the additional hole current $I_h$ through the p-n body diode. However, this behavior does not agree with the experimental results in Figure A.2.

It is observed that the $I_e$ has slightly negative inflexion at point $\circ$ for the case of very low lifetime ($\tau_e=\tau_h=10$ ns) when no traps are included. However, such poor lifetime is unrealistic according to previous literature [16]. A negative inflexion in $I_e$ is also observed at point $\circ$ when the traps are included in the P$^+$ shielding region. In this case, the various lifetime did not have any
significant effects on the results. It is found that the MOSFETs without the traps have slightly larger negative $V_{\text{INFL}}$ (-3.0 V, point ①) than with the traps (-2.8 V, point ②) from the zoomed-in $I_h$ result as shown in Figure A.5(b).

Figure A.5(c) shows the simulation results for the electron current density at $V_d$ of -5 V without (left) and with the traps (right). It can be observed in Figure A.5(c) left that the electrons traverse the $P^+$ shielding region and flow into the $N^+$ source region when the body diode is turned on without the traps. In comparison, the electrons only flow through the base region if there are the traps in the $P^+$ shielding region as shown in Figure A.5(c) on the right. From these results, it is
hypothesized that there are traps distributed in the P+ shielding region due to residual ion implant damage, leading to the negative inflexion in electron current.

As previously mentioned, the contact to the P+ shielding region is located orthogonal to the cross-section to reduce the cell pitch and on-resistance. This approach increases the P+ resistance \( R_{P+} = R_C + R_{Int} \) that affects the \( I_h \) through the body diode.

Figure A.6(a) shows the schematic view of the P+ contact, where the \( R_{Int} \) and \( R_C \) are calculated by \( \rho_{P+} \cdot \frac{L_{short}}{(L_{N+} \cdot T_{P+})} \) and \( \rho_{C} \cdot \frac{1}{\text{Area}_{P+}} \), respectively [17]. From these equations, the calculated total \( R_{P+} \) is about 1.6 \( \Omega \) with measured contact resistivity (\( \rho_{C} \)) of \( 3.6 \times 10^{-3} \, \Omega\cdot\text{cm}^2 \). Figure A.6(b) compares the 3rd quadrant simulation results for the Acc MOSFETs (\( L_{CH}=0.5 \, \mu\text{m} \)) with two different \( R_{P+} \) values added to the P+ contact terminal. It can be seen that the total current has a positive inflexion caused by high \( I_h \) for the case of a small \( R_{P+} \) (0.16 \( \Omega \)). In contrast, a negative inflexion can be observed at about -2.8 V with negligible \( I_h \) when a high \( R_{P+} \) (1.6 \( \Omega \)) is used. Consequently, a high resistance in the P+ shielding region can also lead to the observed negative inflexion in 3rd quadrant current.
Figure A.7 shows the measured 3rd quadrant I-V characteristics for (a) Acc and (b) Inv MOSFETs with various L\textsubscript{CH} at room temperature (solid) and 150°C (dashed) [1].

Figure A.7 shows the measured 3rd quadrant I-V characteristics for (a) Acc and (b) Inv MOSFETs with various L\textsubscript{CH} (0.3, 0.5, 0.8, 1.1 µm) at room temperature (solid) and 150°C (dashed). The V\textsubscript{knee} is reduced and currents are increased for all the cases at higher temperature, which is consistent with previous measurements [18]. Figure A.8 shows the simulation results for (a) Acc and (b) Inv MOSFETs with various L\textsubscript{CH} at room temperature. The results show that the electron current I\textsubscript{e} through the base is dominant.

Figure A.8. Simulation results for (a) Acc and (b) Inv MOSFETs with various L\textsubscript{CH} at room temperature [1].
Figure A.9 shows the measured 3rd quadrant characteristics for the (a) Acc and (b) Inv MOSFETs (LCH=0.5 µm) at Vg from -4 to 4 V at room temperature. It is observed that the V_knee is increased with increasing negative Vg and decreased with increasing positive Vg for both structures. In addition, the inflexion point, V_{INFL}, changes with Vg as indicated by the solid green lines.

In order to understand the observed behavior, 3rd quadrant simulations were conducted for the Acc MOSFETs (LCH=0.5 µm) using Vg from -4 to 4 V. Changes in V_{knee} and V_{INFL} are observed with different Vg values as shown in Figure A.10(a). In order to understand this behavior, the potential barrier at the oxide interface (yellow dashed line in Figure A.1) was extracted, as shown in Figure A.10(b), at Vd=0 V with Vg varied from -4 to 4 V. The potential barrier for electron injection from the drain to the source are given in the figure for each value of Vg. The potential in the JFET region remains close to zero at positive Vg due to formation of an accumulation layer. Positive gate bias reduces the potential barrier, producing a current path for electron through the base region. Larger negative gate bias produces an increase in the potential barrier for transport of
electrons from the source to the drain in the 1st quadrant. However, the JFET potential also becomes increasingly negative due to the formation of a depletion region under the gate. Consequently, it is observed that the potential barrier for transport of electrons from the drain to the source remains the same (1.2±0.2 V) with increasing negative gate bias. This barrier voltage is not equal to the $V_{\text{knee}}$ observed in Figure A.10(a).

To understand the increase in $V_{\text{knee}}$ with increasing negative $V_g$, the potential barrier was studied for case (b) with $V_g=-2$ V at various $V_d$ (i. 0; ii. -1.2; iii. -2.1; iv. -3; v. -5 V corresponding to operating points in Figure A.10(a), respectively). The plots in Figure A.10(c) show a reduction...
in the potential barrier with increasing negative $V_d$ values. The barrier becomes zero at operating point iii. $V_d=-2.1$ V. Current flow by electron transport from drain to source can therefore begin to occur with a $V_{knee}$ of -2.1 V as observed in Figure A.10(a). This confirms that the $V_{knee}$ is directly related to the potential barrier in the base region, which is determined by the gate voltage.

The cross-sections of the distribution of the electrostatic potential are shown in Figure A.11 at $V_d=-3$ V for various $V_g$ ((a) -4; (b) -2; (c) 0; (d) 2; (e) 4 V). It can be observed that the potential of the N-drift region below the P$^+$ shielding region varies with $V_g$. The potential here is close to -3 V at $V_g= -4$ V (Figure A.11(a)), and it is just -1.5 V at $V_g= 4$ V (Figure A.11(e)). Consequently, the hole current $I_h$ can flow through the p-n body diode due to sufficient forward bias of the junction at $V_g= -4$ V, but not at $V_g= 4$ V. The $V_{INFL}$ can be observed by monitoring the current flowing through the contact to the P$^+$ shielding region. This hole current is shown in Figure A.10(a).

Figure A.11. Cross-sections of simulated electrostatic potential for Acc MOSFETs ($L_{CH}=0.5$ µm) at $V_d=-3$ V and $V_g= (a) -4$ V, (b) -2 V, (c) 0 V, (d) 2 V, (e) 4 V [1].
as an inset. It can be seen that turn-on voltage for the body diode shifts from -2.8 V at \( V_g = 0 \) V to
-2.4 V at \( V_g = -4 \) V because the shunting resistance is eliminated. On the other hand, the body diode
turn-on voltage shifts from -2.8 V at \( V_g = 0 \) V to -3.1 V at \( V_g = 4 \) V because the shunting resistance
is reduced.

4. Discussion and Conclusions

The 3rd quadrant I-V characteristics measured at room temperature for all the devices are
summarized in Table A.1. As discussed earlier, the \( V_{knee} \) is the voltage required for electron
transport from the drain to the source, which varies with \( V_g \) due to changes in barrier potential.
The same value for \( V_{knee} \) is observed for structures with different channel length for each value of
\( V_g \). This is because the same potential barrier height is produced across the width of the base region
(equal to the channel length). Although the barrier extends over a greater distance with increasing
channel length, this does not impact the energy required for electrons to be transported from the
drain to the source in the 3rd quadrant.

It can be observed in Table A.1 that the \( V_{INFL} \) changes with not only changes in \( V_g \) but also
with changes in channel length \( L_{CH} \). The inflexion point voltage \( V_{INFL} \) is determined by the p-n
body diode operating with a resistive shunt path via the base region under the gate. The shunt
resistance becomes smaller with increasing positive gate bias. This suppresses injection from the
p-n diode pushing the \( V_{INFL} \) to larger values. The shunting resistance is smaller for smaller channel
lengths (or base widths). This produces an increase in the measured \( V_{INFL} \) with reduction of
channel length.

The physics of the 3rd quadrant characteristics 1.2 kV rated 4H-SiC accumulation-channel
(Acc) and inversion-channel (Inv) MOSFETs with various channel lengths (0.3, 0.5, 0.8, 1.1 \( \mu \)m)
have been discussed in detail using measured data and TCAD numerical simulations.

It is hypothesized that there are traps in the P⁺ shielding region introduced by the Al implants. Similar 3rd quadrant I-V characteristics to the measured data was reproduced using traps in the simulations. From the simulations, it was verified that there are two current paths through the base region and p-n body diode. The hole current is almost negligible with high P⁺ shielding region resistance.

| Table A.1. Summary of experimental results for the 3rd quadrant I-V characteristics of MOSFETs. |
|---------------------------------------------------------------|---------------------------------------------------------------|
| **Temp. 25°C** | **Type** | **Acc L<sub>CH</sub> [µm]** | **Inv L<sub>CH</sub> [µm]** |
| **V<sub>g</sub> [V]** | | 0.3 | 0.5 | 0.8 | 1.1 | 0.3 | 0.5 | 0.8 | 1.1 |
| -4 | -2.6 | -2.6 | -2.6 | -2.6 | -2.6 | -2.6 | -2.6 | -2.6 | -2.6 |
| -2 | -1.8 | -1.8 | -1.8 | -1.8 | -2.0 | -2.0 | -2.0 | -2.0 | -2.0 |
| 0 | -1.1 | -1.2 | -1.3 | -1.3 | -1.7 | -1.9 | -1.9 | -1.9 | -1.9 |
| 2 | -0.2 | -0.2 | -0.2 | -0.2 | -0.5 | -0.5 | -0.5 | -0.5 | -0.5 |
| 4 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **V<sub>knee</sub> [V]** | | 0 | 2 | 4 | 0 | 2 | 4 | 0 | 2 | 4 |
| -4 | -2.6 | -2.6 | -2.6 | -2.6 | -2.6 | -2.6 | -2.6 | -2.6 | -2.6 | -2.6 |
| -2 | -2.6 | -2.6 | -2.6 | -2.6 | -2.6 | -2.6 | -2.6 | -2.6 | -2.6 | -2.6 |
| 0 | -2.9 | -2.8 | -2.7 | -2.6 | -2.8 | -2.7 | -2.7 | -2.6 | -2.6 | -2.6 |
| 2 | -3.4 | -3.1 | -3.0 | -2.8 | -3.1 | -2.9 | -2.8 | -2.7 | -2.7 | -2.7 |
| 4 | -3.8 | -3.5 | -3.1 | -3.0 | -3.4 | -3.2 | -3.0 | -2.9 | -2.9 | -2.9 |
| **V<sub>INFL</sub> [V]** | | 0 | 2 | 4 | 0 | 2 | 4 | 0 | 2 | 4 |
| -4 | -4.6 | -5.1 | -5.6 | -5.9 | -5.0 | -5.2 | -5.5 | -5.6 | -5.6 | -5.6 |
| -2 | -3.7 | -4.3 | -4.8 | -5.3 | -4.4 | -4.8 | -5.2 | -5.4 | -5.4 | -5.4 |
| 0 | -2.8 | -3.3 | -3.8 | -4.4 | -3.5 | -4.1 | -4.6 | -4.9 | -4.9 | -4.9 |
| 2 | -2.5 | -2.7 | -2.9 | -3.4 | -2.8 | -3.2 | -3.8 | -4.3 | -4.3 | -4.3 |
| 4 | -2.0 | -2.3 | -2.5 | -2.7 | -2.5 | -2.7 | -3.0 | -3.4 | -3.4 | -3.4 |
From the numerical simulations, it was shown that Acc MOSFETs have lower knee voltages ($V_{\text{knee}}$) than Inv MOSFETs in the 3rd quadrant due to smaller potential barrier in the base region for electron transport from the drain to the source. Both the Acc and Inv MOSFETs have similar p-n body diode turn-on voltages ($V_{\text{INFL}}$). The $V_{\text{INFL}}$ changes with $V_g$ and $L_{CH}$ due to the change in shunting path resistance.

From the measured voltage drop, $V_F$ at $I=5$ A given in Table A.1, it is demonstrated for the first time that devices with shorter channel length have smaller 3rd quadrant diode voltage drop. In addition, it is demonstrated that Acc devices have smaller voltage drop than Inv devices making them superior in the 3rd quadrant, as well as in the 1st quadrant due to superior channel mobility.
REFERENCES


