ABSTRACT

CHATTERJI, ARINDAM. Design of a High Efficiency Silicon Carbide Converter for More Electric Aircrafts. (Under the direction of Dr. Srdjan Lukic).

Rapid developments in the field of Wide Band Gap (WBG) power electronics have paved the way for widespread transportation electrification. More recently, this trend has been extended to the aerospace industry, in a bid to make aircrafts lighter, less fuel consuming and thereby more cost efficient. High power density and efficiency power converters are at the forefront of this effort, enabling More Electric Aircrafts (MEA). The design of such a high efficiency SiC based T-type converter for MEA applications is presented in this thesis. The design is 97.78% efficient with a power density of 8.23 kW/L using commercially available devices.

A comprehensive loss model is developed for the T-type converter in an attempt to optimally size the cooling mechanism, which tends to be the bottleneck towards higher power density designs. An amalgam of simulation, analytical and approximation methods are utilized to realize an accurate loss model from an asymmetric source. This model illustrates the superiority of the T-type converter for certain operating conditions suitable to the application. It is shown that the T-type converter is the most efficient option as compared to the 2-level Voltage Source Inverter and 3-level Neutral Point Converter (NPC).

Electronic systems designed for altitude operation exhibit differing dynamics than those at sea level. Therefore, design standards relevant to the application are reviewed and followed to ensure high altitude functionality for the electrical as well as thermal operation of the system. Board level creepage and clearance as well as system level cooling considerations are made for continuous operation in low density air.

Furthermore, the converter is laid out onto a Printed Circuit Board (PCB) wherein design decisions are made to pick the lowest volume consuming options. The PCB layout is further

analyzed in ANSYS Q3D to determine parasitic inductances, which are then used to size necessary decoupling capacitors. This approach ensures reliability by minimizing the risk of damaging voltage spikes to the devices.

A 3-D model of the system is built and analyzed.The system allows easy vertical integration of the gate driver and control circuitry, making it a modular system. The converter presents itself as a strong fit for the requirements of the MEA application. The work done in this thesis helps provide a strong foundation for a multi-physics approach for an MEA converter which can be built upon and validated in experiment.

Design of a High Efficiency Silicon Carbide Converter for More Electric Aircrafts

by
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BIOGRAPHY

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INTRODUCTION

Recent decades have shown a growing interest in realizing electric counterparts to traditional transportation mechanisms [11] in a bid to reduce carbon emissions, thus enabling a more habitable planet. This trend can be witnessed in increased production and sales of hybrid as well as fully electric vehicles (EVs) in industry, coupled with considerable research in these topics in the research realm. The movement has also reached new heights entering the aerospace industry, with all electric and more electric aircrafts (MEA) gradually entering industry as shown in Figure 1.1 adapted from [10] and also expanding quickly in research labs. Several benefits arise from this, primarily those related to reducing fuel consumption by reducing weight on board and improving electrical distribution by creating more efficient and reliable systems [1] . While all electric aircrafts are limited primarily

by the relatively low energy density and high cost of available battery technologies, [22] their MEA counterparts are becoming adopted by industry leaders Boeing and Airbus. This indicates a clear paradigm shift in the aviation industry and highlights the importance of key enabling technologies for the same.

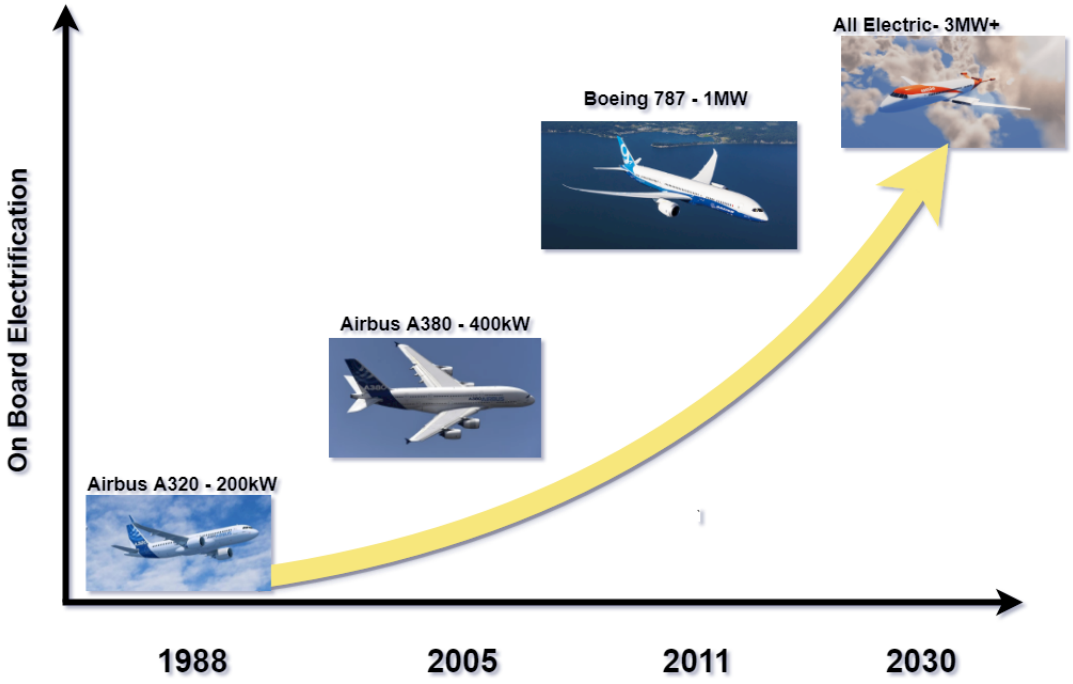


Figure 1.1: Aerospace Industry Trend

The key idea of an MEA is to replace or supplement conventionally hydraulic, pneumatic and mechanical loads by their electrical analogues, thereby reducing weight on board. Aside from more energy dense batteries, power electronics converters (PEC) and integrated starter generators (ISG) form the core of the MEA electric distribution network. The ISG is a key component in the generation of electric power on board as well as a compact solution to assist in the starting of the jet engines. They're used extensively across several power levels

depending on the size of the aircraft as well as the electric distribution system implemented. The PEC is responsible for providing bidirectional power, both to the ISG in starter mode, as well as the different loads on board in generator mode.

In both of these enabling technologies, high power density and high reliability are of utmost importance. While these are often conflicting goals, the focus of the design process must be to reach an optimized solution trading off between the two. On the converter side, the wide adoption of silicon carbide (SiC) devices over silicon (Si) has paved the way for high power density designs. The wide band gap characteristic of SiC enables higher junction temperature operation of 175 °C in practical conditions and close to 400 °C in experimental research environments[22]. They have also found use in high ambient temperature environments upto 500 [12] making them suitable for harsh environments. Additionally, SiC devices have a significantly smaller die area relative to Si devices, reducing the smaller parasitic capacitances between terminals. This characteristic enables the realization of higher switching frequencies [19] and in turn low volume and weight output filters for converter systems. Overall, the use of SiC devices in an MEA application aligns perfectly with the goal of high power density, both in terms of volume as well as weight.

An important aspect of the converter system that dominates the volume, and therefore power density, is the cooling mechanism. The power output capability of a converter is directly related to the temperature which it's junction can sustain. The junction temperature must be managed at a level that prevents device failure due to thermal runaway. Since SiC devices' power handling capabilities are high due to the previously mentioned ability to reach high junction temperatures, and cooling capability of a heatsink is directly related to volume, smaller cooling mechanisms can be used to restrict the junction temperature to a predetermined level.

To further realize the goal of high power density, it is important to ensure that the converter losses are as low as possible, to minimize the source of heat dissipation. While an

MEA system has several converters, the bidirectional PEC is one that must be focussed on as it directly interfaces with the ISG. There are several options in the 2-level as well as multi-level converter domains, discussed in [25], [5], [27] and with the conventional 2 level voltage source inverter (VSI), 3-level diode clamped neutral point converter (NPC) and 3-level T-type converter being the most widely used. While 3-level converters usually add initial cost and/or complexity to the system relative to 2-level solutions, their outstanding efficiencies along with low total harmonic distortion (THD) make them increasingly attractive alternatives. [27] Compares the three topologies in general low voltage motor drive applications and finds that the 3 level topologies have superior efficiency. The T-type converter is found to be the most efficient at medium switching frequencies. The additional benefit of reduced chip area as compared to 2-level topologies at high switching frequencies was also noted. As a further step, it was shown that due to reduced harmonic losses in the 3-level converters, the test machine was better off in terms of considerably lower heating and degradation

[5] Compares the three mentioned topologies specifically in the ISG application with different combinations of single and multiple converter-machine systems. It concludes that 3-level converters outperform with regards to efficiency, THD at all power levels considered. The T-type converter is found to be the least lossy at the lower power levels for the single machine-single converter combination.[20] Compares a 2-level and a T-type converter for a 100kVA ISG application using Si and SiC modules, including MOSFETs as well as IGBTs. The T-type converter is SiC found to be the most efficient across all switching frequencies.

Thus, the T-type converter is clearly a strong choice for implementation in the ISG application, worthy of deeper investigation. In particular, it is advantageous to explore a high power density design using the highest performing commercially available devices. The literature thus far has either employed custom built SiC modules, or a combination of SiC and Si technologies in implementing the T-type. This thesis delves deep into the design

Table 1.1: Target Metrics

Power Output	35 kW
Switching frequency	40 kHz
Nominal Voltage	540 VDC
Efficiency	>98%
Power Density	>15kW/L
Cooling	Forced Air at 50 °C Ambient
Design Standard	IEC 60664-1 at 30000 ft

of an all-SiC T-type converter for aerospace ISG applications using discrete devices with target metrics as shown in the table below.

The organization of this thesis is as follows. Section 2 describes in detail specifics of the application, including aircraft electrical distribution systems, the characteristics of an ISG as well as the desired characteristics of the PEC. Section 3 describes the T-type working mechanism, including switching patterns and modulation scheme. It shows a simulation model and also compares efficiencies against the NPC and VSI. Section 4 outlines an in depth thermal analysis of the system using PLECS and MATLAB. Section 5 describes the considerations made to ensure a high power density design while adhering to IEC 60664-1 at 30000 ft standards. Section 6 addresses the PCB layout of the design. This includes DC link, sensing circuitry, as well as parasitic inductance minimization. Section 7 showcases a CAD model of the system, expected system performance and future work.

CHAPTER

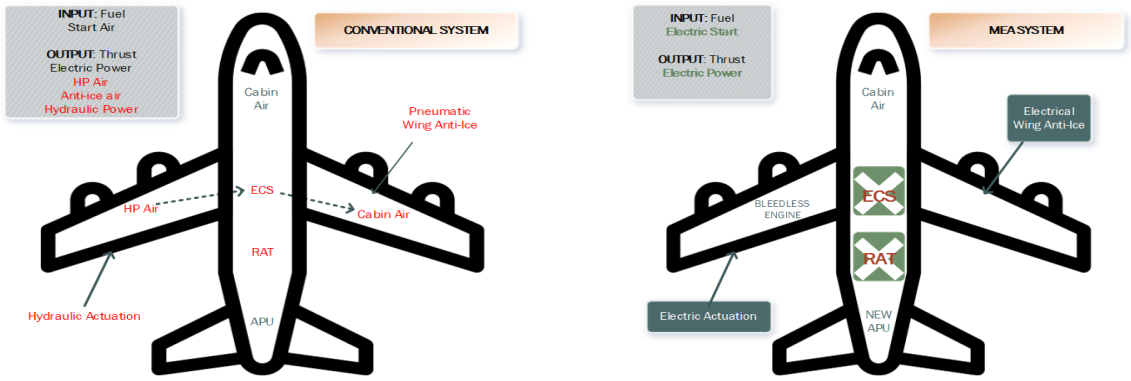
2

APPLICATION OVERVIEW AND TECHNOLOGY REQUIREMENTS

This chapter contains a detailed review of the MEA architecture as well as different aircraft distribution systems used in industry. This description enables a deeper understanding of the MEA system and thereby derives the necessary characteristics of the ISG as well as the PEC.

2.1 Conventional vs MEA Load Distribution

Conventional aircrafts use their gas turbine engines to power their sub-systems by using different methods, including electrical pneumatic, hydraulic and mechanical power transfer as indicated in Figure 2.1a adapted from [13]. The electrical systems provide power for loads such as avionics, lighting and entertainment systems. The pneumatic system powers loads such as the cabin pressurization system, air conditioning and anti-ice systems. The mechanical system and hydraulic systems are primarily used for pumping and flight control and auxiliary systems. A large amount of power in the mega-watt range is required by all these loads. However, with the development of lighter and more efficient electrical systems, some of these loads and power conversion systems can be replaced or even eliminated. As shown in Figure 2.1b in particular, the heavy pneumatic environmental control system (ECS) and Ram Air Turbine (RAT) can be eliminated and the anti-ice as well as flight control can be electrically realized.



(a) Conventional Aircraft System (b) MEA Aircraft System

Figure 2.1: Conventional vs MEA Load Systems

In effect, increasing the electrical power capability on board would allow for massive weight reduction overall on board. Doing so also enables more efficient engine designs where loads do not need to be powered by the bleed air system through the jet engine. These measures also improve the reliability of the system by reducing maintenance needs and costs. Since electrical systems are typically easier to diagnose and reconfigure, the life of the aircraft is better monitored and estimated. Ultimately, the fuel consumption of the aircraft is reduced, reducing emissions as well as operation costs overall.

2.2 Conventional Electrical Architectures on Board

In order to appreciate MEA electrical distribution systems, it is first necessary to introduce the conventional counterparts. Conventional electrical distribution standards are primarily as follows [30]:

- 28 VDC - Generally supplying low power loads or avionics on large aircrafts or entire distribution on small aircrafts
- 115 VAC at 400 Hz - Large loads on civilian aircrafts
- 270 VDC - Primarily military aircrafts and certain large loads on civilian aircrafts

The AC distribution system is presently most widely used. The following section describes the different generation systems employed by various industry leaders.

2.2.1 Constant Speed Constant Frequency System

In conventional AC systems, the most widespread implementation is the constant speed drive (CSD) as shown in Figure 2.2 wherein a mechanical gearbox is implemented between the shaft of the jet engine and the generator. The Boeing 701 to 777, Airbus A320 are some examples that use this [16]. The CSD converts the variable speed on the input due to the varying speed of the turbine into a constant speed to drive the AC generator. While this solution is safe and effective, the addition of the mechanical gearbox adds a complicated, expensive and most detrimentally, heavy stage to the distribution network.

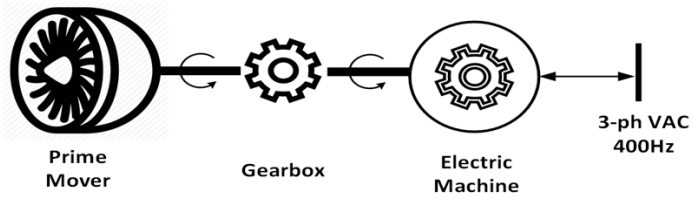


Figure 2.2: Constant Speed Drive System

2.2.2 Variable Speed Constant Frequency System

Due to a lack of reliable and power dense power electronics and machines in the past, the CSD prevailed. However technological advancements in power electronics and micro-processor technologies introduced the Variable Speed Constant Frequency (VSCF) and Variable Speed Variable Frequency (VSVF) systems. In a VSCF system the generator may be connected directly to the jet engine shaft [21]. The frequency variation from the variable speed of the jet engine is overcome by adding a DC link to between the generator and frequency sensitive AC loads, followed by a back-to-back rectifier-inverter as shown in

2.3. The PEC block ensures that the frequency sensitive loads are operating at the rated frequency [8]. This approach has been implemented on the Boeing 777, MD90 [15] for the backup generators.

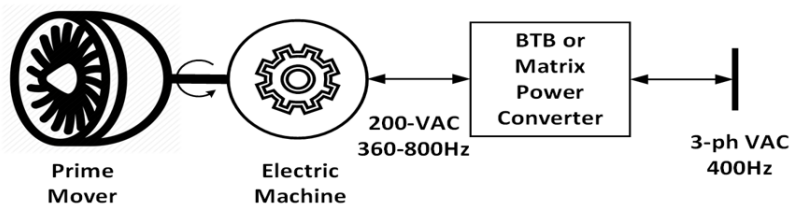


Figure 2.3: VSCF System with DC Link

The alternative method of implementation is where the DC link and inverter-rectifier converter is replaced with a direct AC/AC cycloconverter or matrix converter [21]. This solution is primarily employed on military applications such as the F18.

2.3 MEA Electrical Architectures

With the conversion of loads and sources from non-electrical to the electrical domain, an increased electric power output capability is required on board. This section addresses solutions presently implemented in industry.

2.3.1 Variable Speed Variable Frequency System

The most advanced MEA adapted aircrafts in operation today are the high capacity Boeing 787 and Airbus A380 [21]. These systems do not use any means of constant frequency correction, but instead directly use the variable frequency generated by the jet engine-generator

connection. These variable speed variable frequency systems (VSVF) are used to power frequency insensitive loads such as the wing ice protection, galley ovens, cargo heaters [33]. For frequency dependent loads, auto transformer units (ATUs) or power electronic converters are used at the point of load (POL). As shown in the simple image in 2.4, the shaft is directly connected to the generator, outputting 360-800 Hz of fundamental frequency varying due to the varying shaft speed. While this solution is attractive and will likely gain traction in the future, the major challenges in adoption are the complex cooling system and mechanical design of the variable frequency generators (VFGs).

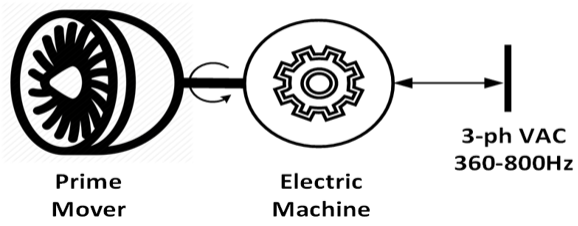


Figure 2.4: VSVF System

2.3.2 High Voltage DC

High Voltage DC (HVDC) is a solution mostly restricted to the military applications such as the F-18 and JSF-16 [21] in industry. As shown in Figure 2.5 this system employs a DC distribution network and uses a bidirectional power converter to invert or rectify voltage depending on the direction of power transfer. HVDC is an extremely promising technology due to the tremendous benefit of weight reduction due to reduced cabling as well as high reliability and efficiency. Battery energy density limits currently act as the bottleneck for widespread commercial implementation. However, it can be implemented in modular

forms on larger aircrafts to power appropriate loads. Additionally, having an HVDC bus on board allows the seamless implementation of the ISG where-in the battery serves as the source for starting mode, and gets recharged in generating mode. For MEA of the future, this technology is quickly growing and will likely be implemented broadly within the next decade.

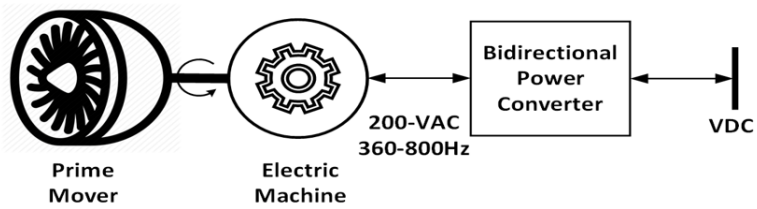


Figure 2.5: HVDC System

2.3.3 Example MEA Architecture

Figure 2.6 shows an example of a realizable MEA distribution network for future applications, combining the benefits of both technologies currently implemented. A mixed combination of DC and AC power distribution networks can be achieved by using a primary HVDC bus regulated by the main bidirectional power converter interfacing with the electric machine. Additional DC/AC and DC/DC converters can then be used tailor made to support the nature of the loads. These secondary converters can be placed within the aircraft as desired and could enable optimized weight distribution as well as high efficiency operation. The modular nature of this architecture ensures high reliability and flexibility.

The shaded box in the image represent the key elements of the architecture, namely the ISG and PEC, both of which must be further developed to make widespread adaptation possible.

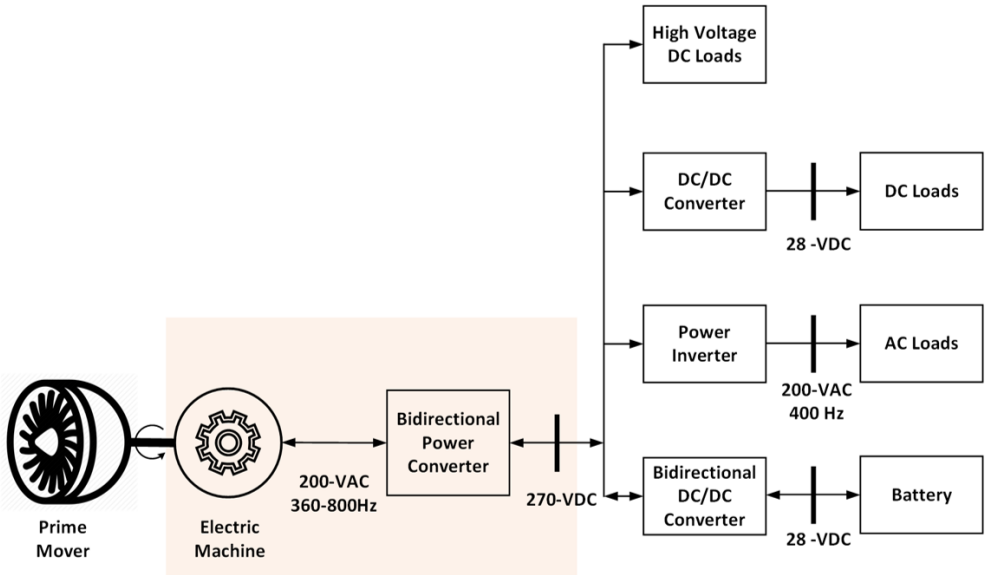


Figure 2.6: MEA Example Architecture

2.3.4 Integrated Starter Generator

The ISG's characteristic torque-speed curve is as shown in Figure 2.7. The two portions of the curve can be described as follows:

1. Starter Mode

   In starter mode the ISG acts as a motor, delivering mechanical power to the jet engine. The electrical flow of power is sourced from the DC system on board through the bidirectional power converter, with the ISG acting as the load for the converter. ω_{base} represents the base speed of the machine acting as a motor. The motor runs in constant torque mode until this speed is reached, causing the attached jet engine turbine to start rotating from standstill. Upon reaching ω_{base}, fuel is ignited within the jet engine to enhance the speed of rotation. The motor continues to deliver a reduced torque at higher speeds. Once a self sustaining speed is reached, at ω_{start}, the machine is disconnected and starting mode is realized. The peak torque requirement of the ISG can be derived from the starter mode. [6]

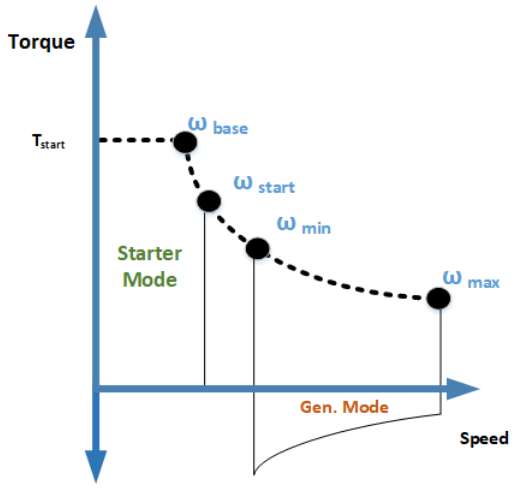


Figure 2.7: ISG Torque - Speed Curve

2. Generator Mode

   Once the starter mode operation is complete in Figure 2.7, torque provided by the ISG continues to reduce with increasing speed. Once speed ω_{min} is reached, the ISG enters generator mode and provides AC electrical power to the power converter. The speed continues to increase due to the increase in speed of the jet engine turbine, and torque decrease until ω_{max} is reached, which is the maximum deliverable speed by the machine. ω_{max} is used to size the machine and is derived from the speeds of the aircraft jet engine.

The machine must thus have high speed as well as high torque capabilities, which are conflicting goals. Moreover, the design process requires an intensive multi-physics perspective, including electrical, magnetic and thermal considerations. [23] serves as a good reference, comparing potential machine topologies holistically and listing the pros and cons of each. Currently, the Wound Field Synchronous Machine (WFSM) is the most popular choice due to inherent safety and reliability. Trends migrate favorably towards Permanent Magnet Machines (PMMs) due to their inherent high power density and efficiency, albeit the need for additional protection measures.

The ratings of the machine dictate the ratings of the bidirectional power converter. Maximum power is needed in the generating mode and thus the converter is sized appropriately. Additionally, the converter must have the following key attributes:

- High Power Density & Efficiency
- Low Total Harmonic Distortion (THD)
- Low Electromagnetic Interference (EMI)

The detailed design of a converter exhibiting these characteristics will be presented here on.

CHAPTER

3

CONVERTER TOPOLOGY

Having established the required characteristics of the PEC, a detailed topology selection procedure is presented. The target specifications determined from the machine for the converter are:

Table 3.1: Target Metrics

Power Output	35 kW
Nominal Bus Voltage	540 VDC
Efficiency	>98%
Power Density	>15kW/L
Cooling	Forced Air at 50 °C Ambient
Design Standard	IEC 60664-1 at 30000 ft

3.1 Topologies Explored

Comprehensive literature review as well as simulations for the specifications are undertaken to pick the most suitable topology for this application. 2-level Voltage Source Inverter (VSI) as shown in Figure 3.1, 3-level Neutral Point Clamped (NPC) as shown in Figure 3.2 and 3-level T-type (TTC) as shown in Figure 3.3 are compared. The most fundamental difference between the 2-level and 3-level converters is the number of voltage levels seen in the AC output waveform. The converters otherwise have varying loss profiles, control schemes and device rating requirements. Existing literature is used to summarize those differences and study how they affect this application, followed by verification in simulation.

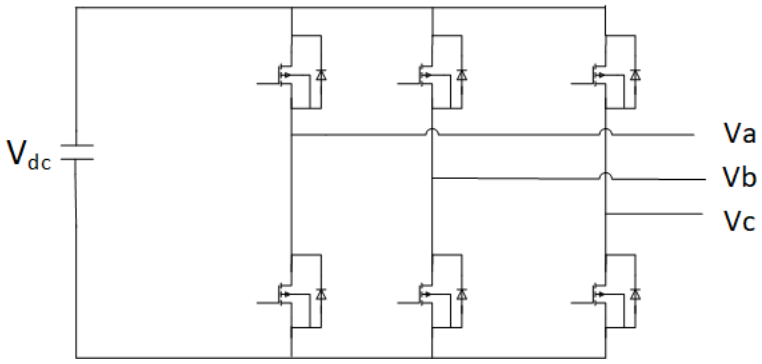


Figure 3.1: 2-Level Voltage Source Inverter

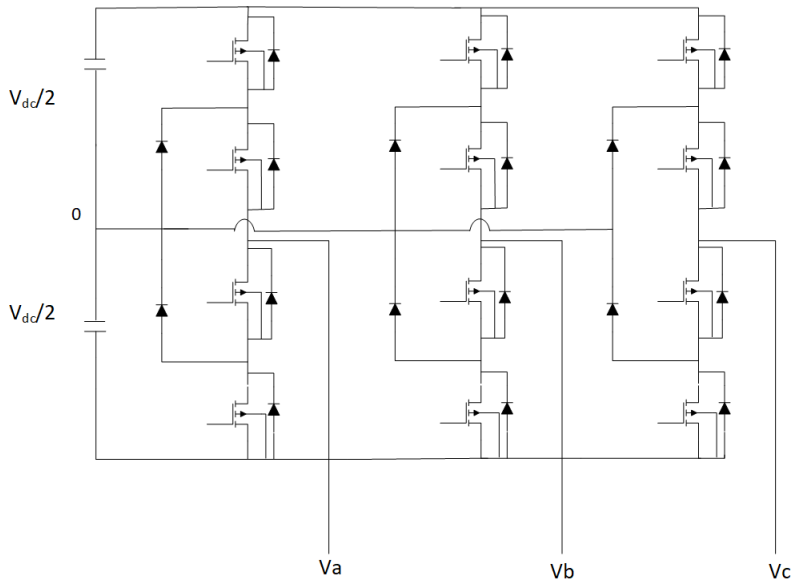


Figure 3.2: 3-level Neutral Point Clamped

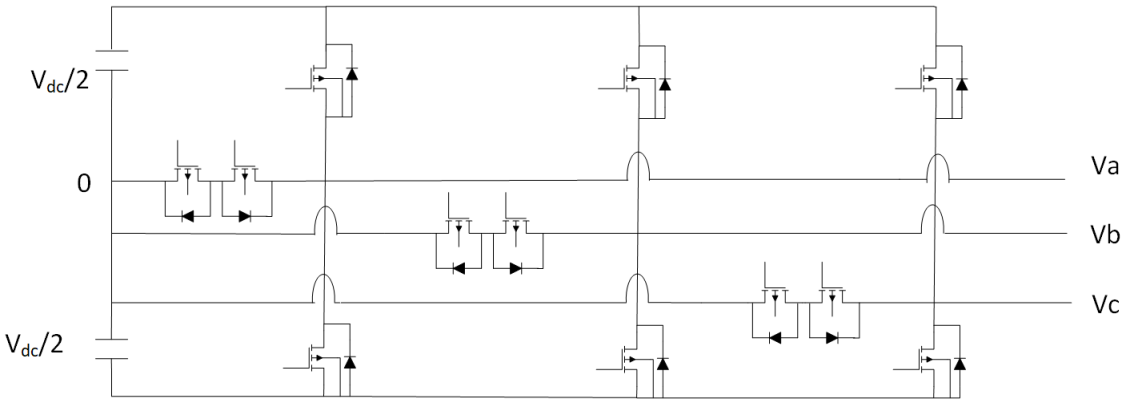


Figure 3.3: 3-level T-type

3.1.1 Holistic Comparison

[28] Compares the efficiencies of the VSI, NPC and TTC for a 10 kW system using Si IGBTs over varying switching frequencies. The results are as shown in Figure 3.4. The NPC and TTC have flatter efficiency curves with increasing frequencies whereas the VSI efficiency drops quickly for the same. High switching frequencies are desired for smaller overall system volume, therefore this trait in the VSI is undesired. Additionally, due to the increased number of levels in the 3-l topologies, an added advantage is lower THD resulting in cleaner output waveforms.

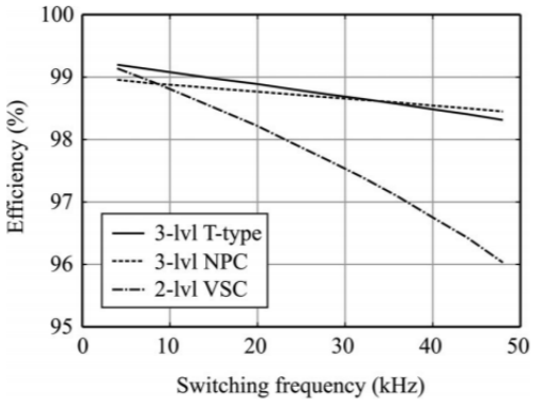


Figure 3.4: Converter Efficiency vs Switching Frequency [28]

The overall loss comparison is based on two primary factors:

1. Conduction loss $\propto$ Number of devices in conduction path
2. Switching loss $\propto$ Blocking voltage of devices

The high switching losses are due to the higher blocking voltage of the switches in the VSI, wherein all switches must block the full DC link voltage. Additionally, the commutation voltage during switching for the devices are also the full DC link whereas for the NPC the

switching commutation voltage is only half that for all devices, and for the TTC half for the midpoint connected devices.

Conversely, the conduction losses of the VSI are generally lower than that of the NPC due to lesser number of devices in the conduction path, whereas they are comparable to the TTC as shown in [27].

Comparing the NPC and TTC, the efficiency curves are very similar and crossover at the 35 kHz mark, indicating that the TTC exhibits higher switching losses than the NPC. The switching frequency is of importance in order to extract optimal efficiency. The TTC shows most potential, but must be further evaluated for the application.

3.1.2 Application Specific Comparison

[5] Provides a study of various converter and machine combinations at varying power levels for an ISG application, ranging from single machine-converter to multiple machine - converter combinations in simulation. In the combination of interest - Single Machine Single-Converter (SC-SM) as shown on Figure 3.5, with varying power levels, the TTC is shown to have maximum efficiency as well as minimum THD. Various additional factors need to be stated as well to contextualize these results. Firstly, the devices used here are SiC modules for the 2L and Si IGBT modules for the 3L topologies. Additionally, different switching frequencies are used for the SiC and Si modules. The control algorithm employed by the authors claim to adjust for these mismatches for a fair comparison. The result encourages a deeper look into the TTC.

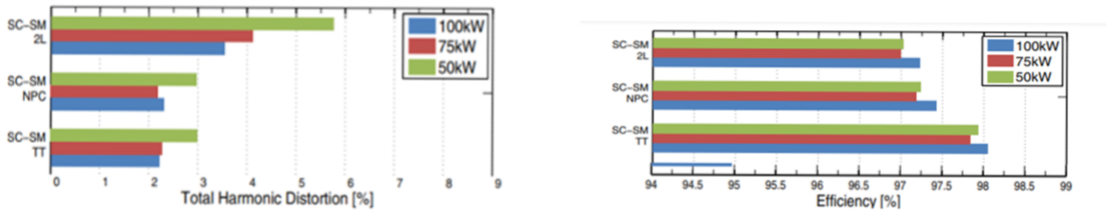


Figure 3.5: Single Converter - Single Machine Comparison[5]

In [6] shows the build of an optimized ISG system and tests losses in hardware. For a 45kW system, it compares VSI and NPC IGBT module based converters across all ISG operation modes, as described in section 2. As shown in Figure 3.6 the NPC has higher efficiency across all operating conditions.

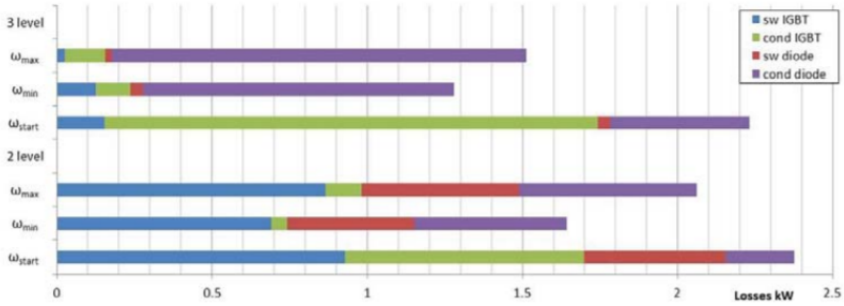


Figure 3.6: Converter Efficiency over ISG Operating Conditions [6]

The literature review presents a strong case for 3-l converters over 2-l VSI and leans towards the TTC being the most efficient given the optimal switching frequency. It combines the benefits of the low conduction loss of the VSI and the low switching loss of the NPC. Its operation will be further presented in detail in the coming subsection. Lastly, while

the literature review provides deep insight, it is inconclusive without simulating the three converters once the necessary devices are selected. The results of this simulation will be presented and discussed.

3.2 T-type Converter

The TTC topology is as shown in 3.3 is an advanced 3-level topology typically used in medium voltage applications [17]. The converter is simplified to a single phase in order to describe the operating principle as shown in 3.7. High side devices T1/D1 and low side devices T4/D4 block the full DC-link voltage. The neutral point connected bidirectional switches T2/D2, T3/D3 block half the DC-link voltage [28]. Due to this property the bidirectional switches exhibit low switching losses and acceptable conduction losses even though they are series connected. The neutral point switches can be connected in common-drain/collector or common-source/emitter configuration depending on the switch technology being used.

In most works presented in the past, [3], [2] Si IGBTs are used for the bidirectional switch as they tend to offer extremely low conduction losses while trading off switching losses. .Since the blocking voltage of the switches is low, the typically high switching losses from cheaper IGBTs as compared to SiC devices is noted as a tradeoff between efficiency and cost.SiC devices are used for the high and low side switches since the benefit in reduced switching losses is significant. [14] further replaces T2/T3 with high performing MOSFETs and D2/D3 with SiC diodes and notes the increased efficiency. In order to completely leverage the TTC, all devices can be replaced with their SiC counterparts to maximize efficiency, while pushing higher power output, in critical applications.

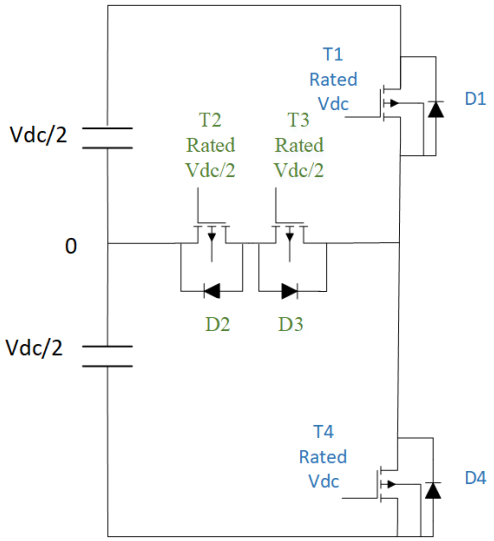


Figure 3.7: Single Phase TTC

3.2.1 Switching States

The most simple switching scheme for the TTC would be to close T1 for positive voltage level, T2 and T3 for 0, and T4 for negative voltage level in both current directions [28]. However this requires a current polarity dependent switching scheme. Instead, a minor modification wherein T2 and T3 are additionally closed, for the positive and negative voltage levels respectively, the current commutation becomes polarity independent as shown in table 3.2. Using this approach, the modulation scheme for the TTC is identical to the NPC, as derived in detail in [24].

Table 3.2: Current Independent Switching States of TTC

State	Output Voltage	T1	T2	T3	T4
Positive	Vdc/2	ON	ON	OFF	OFF
0	0	OFF	ON	ON	OFF
Negative	-Vdc/2	OFF	OFF	ON	ON

3.2.2 Current Commutation

A detailed example of the current commutation for positive to 0 and 0 to positive is described to further illustrate the polarity independent commutation scheme. The current commutation for the positive voltage to 0 voltage level assuming a positive output current is as shown in Figure 3.8 from left to right. The system starts with T1 and T2 in on states connecting the output to the Vdc/2 potential with positive output current. When switching to the 0 potential level, T1 is turned off. After a necessary dead time interval to prevent shoot through, T3 is turned on. During the dead time the current is forced to commutate through T2 and anti-parallel diode D3. And finally, T3 is turned on after the dead time interval to commutate current.

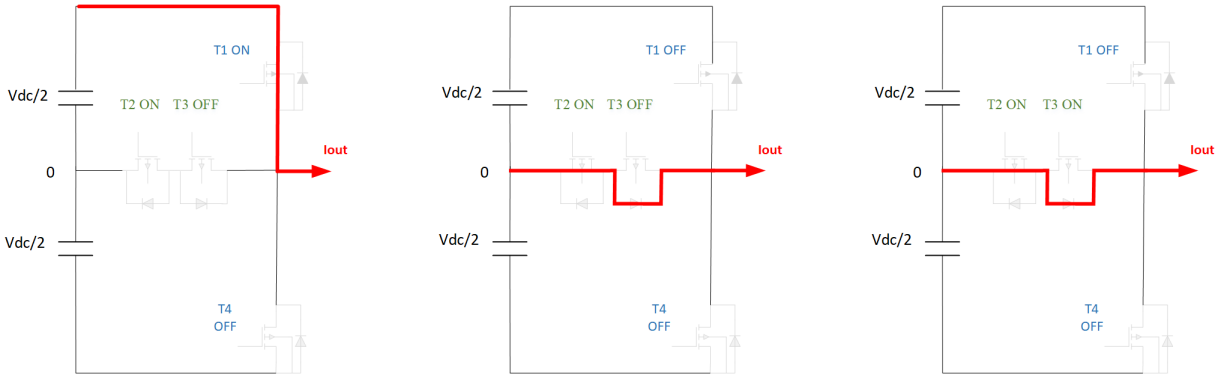


Figure 3.8: Positive to 0 Voltage (Current > 0)

Similarly, the scenario for negative current is illustrated in Figure 3.9. Focusing on the switching states of all devices, it can be seen that they are identical to the positive current scenario. Starting with T1 in the on state, the body diode conducts momentarily in the on-off transition. The current then commutates to the neutral point through T3 once it is turned on after a dead time, thus showing the natural commutation of current from the

positive to 0 potential.

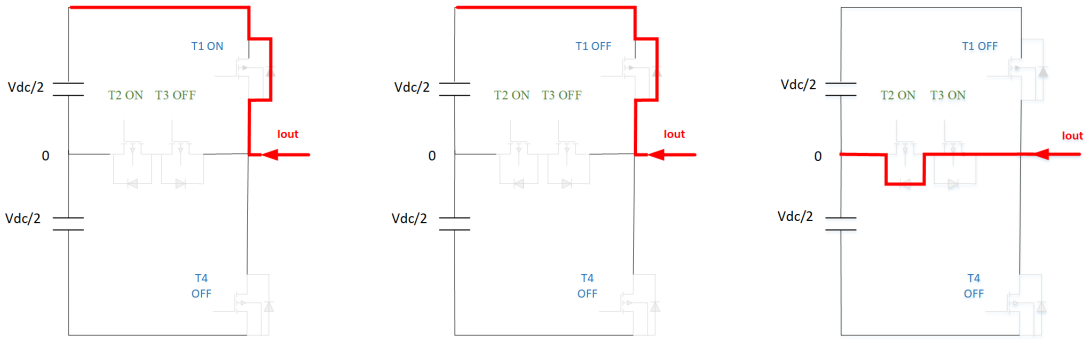


Figure 3.9: Positive to 0 Voltage (Current < 0)

Furthermore, the commutation for the 0 to positive potential switching are illustrated. As shown in Figure 3.10, current initially is flowing through T2 and T3 being on. T3 is then switched off and T1 switched on after a turn on delay to complete the transition.

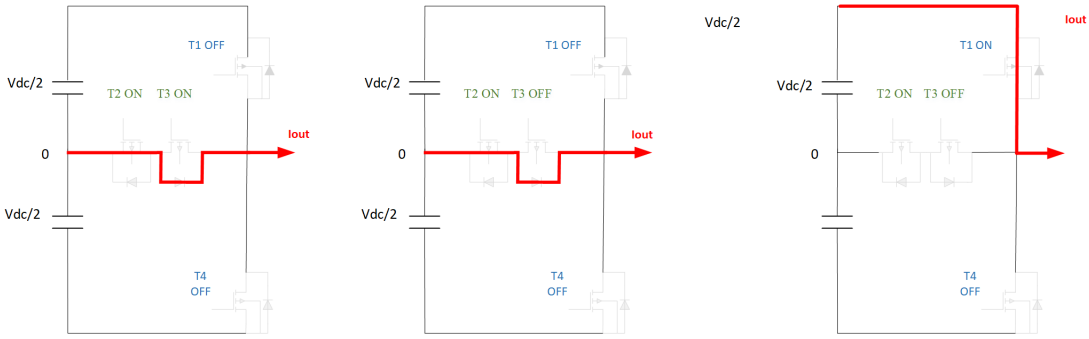


Figure 3.10: 0 to Positive Voltage (Current > 0)

Similarly, as shown in Figure 3.11, the same switching pattern is utilized for negative current operation. T3 is switched off and T1 is turned on after a delay time. The body diode T1 conducts current momentarily. Both cases have the same switching pattern.

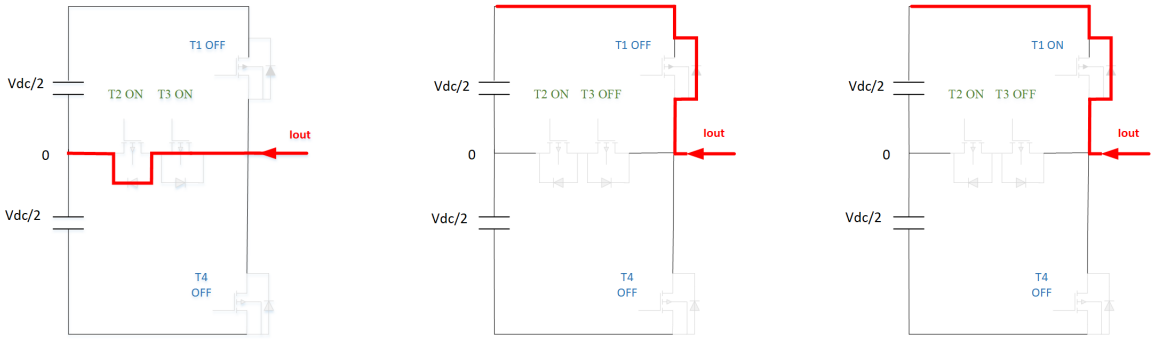


Figure 3.11: 0 to Positive Voltage (Current < 0)

Due to symmetry of the circuit, the same procedure applies for commutation from negative to 0 and 0 to negative. In this case T4 performs the same function as T1, enabling connection of the load to the negative node. In both positive and negative current conditions, the switching pattern remains the same.

Thus the operation principle of the TTC is realized. Table 3.3 shows all combinations of allowable and destructive states. The destructive states all result in shorting of either positive, negative or 0 potential nodes. As long as adjacent switches such as T1/T3, T2/T4 are not switched on at the same time, and the high and low side switches are not shorted, the converter functions. Additionally, no more than two switches should ever be switched on under any conditions.

Table 3.3: All Permutations of Switching States

T1	0	1	0	0	0	1	0	1	0	1	0	1	1	1
T2	0	0	1	0	0	1	0	0	1	0	1	0	1	1
T3	0	0	0	1	0	0	1	1	0	0	1	1	0	1
T4	0	0	0	0	1	0	1	0	1	1	1	1	1	0
State	Allowed							Destructive						

3.2.3 Modulation

A dual carrier sine pulse width modulation (SPWM) is developed and implemented to implement the commutation states desired. The triangle carrier frequency is set as the switching frequency desired for the converter, whereas the sine wave frequency is set as the fundamental output wave frequency desired. An important consideration is the modulation index m_a, which determines the amplitude of the output wave.It is a ratio of amplitudes, defined as:

$$m_a = \frac{A_{sine}}{A_{carrier}} \tag{3.1}$$

It is set at 0.8 in this application as a practical value. Figure 3.12 illustrates the modulating and carrier waves over a fundamental period of the output voltage.

The positive carrier controls devices T1 and T3, controlling the positive output switching

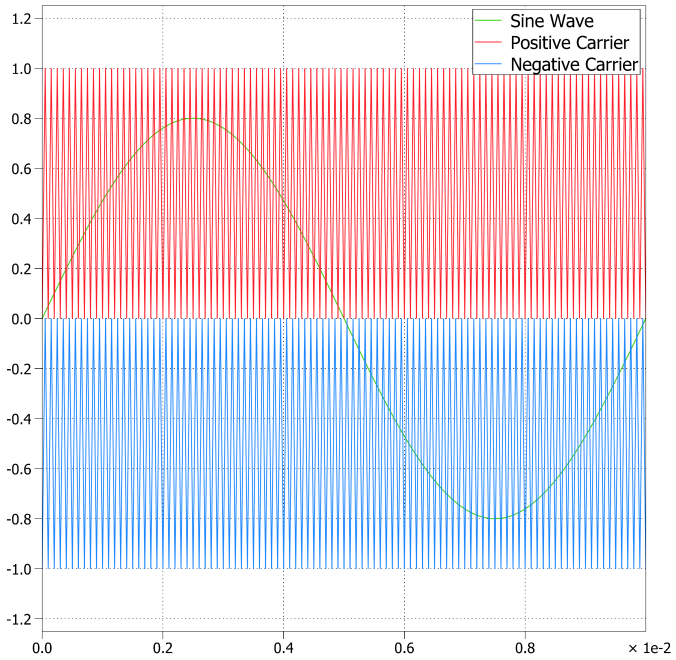


Figure 3.12: Modulation Over a Fundamental Cycle)

cycle whereas the negative carrier does so for devices T2 and T4, controlling the negative half cycle. T1 is turned on for instances when the sinusoidal wave has an amplitude greater than that of the positive carrier. Conversely, T4 is turned on for instances when the sinusoidal wave has an amplitude greater than that of the negative carrier. T2 and T3 are have switching states complementary to those of T4 and T1 respectively. This modulating pattern enables the operation required as highlighted in the previous section, while avoiding any destructive states.

Figure 3.13 shows the switching states for all switches within a single phase. It is of interest to note the patterns, as they dictate the loss profile of the converter, explored deeply in subsequent sections.

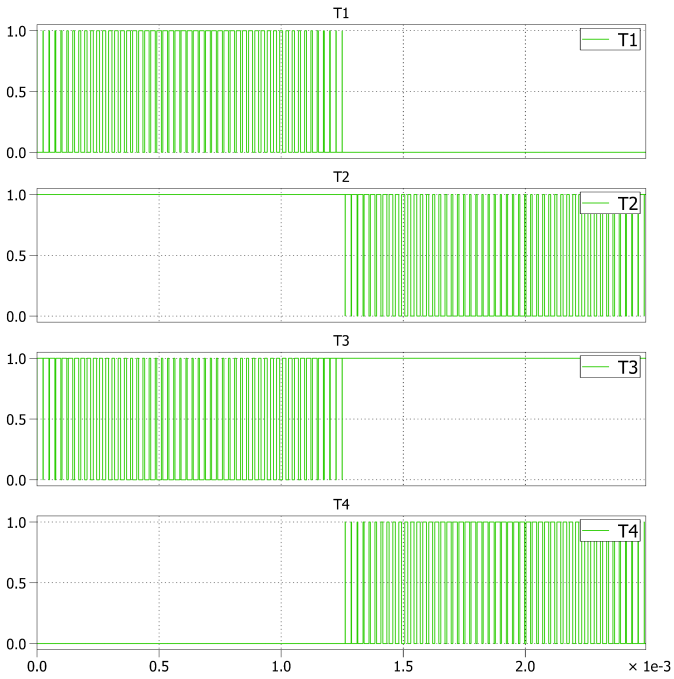


Figure 3.13: Switch states over a Fundamental Cycle

3.2.4 Simulation Model

A 3 phase, 35kW system is simulated using ideal components in PLECS as shown in Figure 3.14. The phase voltage is as shown in Figure 3.15a and line-line voltage and phase current are as shown in Figure 3.15b. The rms values for the output phase voltage and phase current are found using the scope tool. Power output is calculated using phase voltage and current rms values in 3.2:

$$P_{out} = 3 * I_{phaserms} * V_{phaserms} \tag{3.2}$$

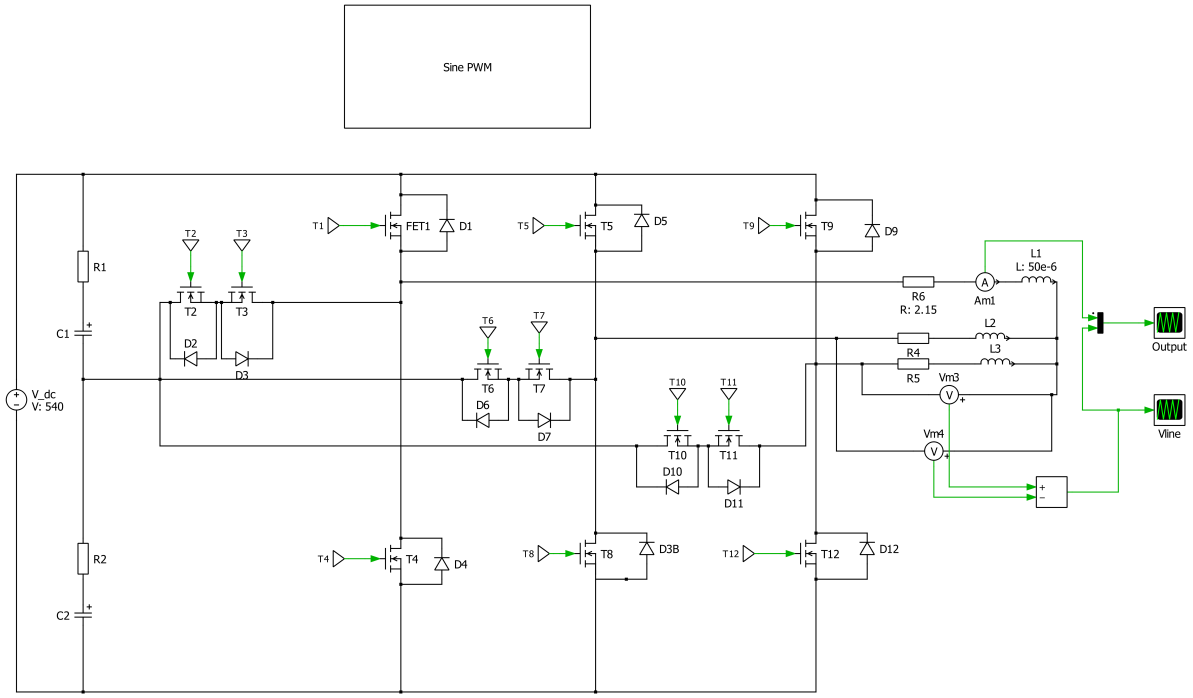
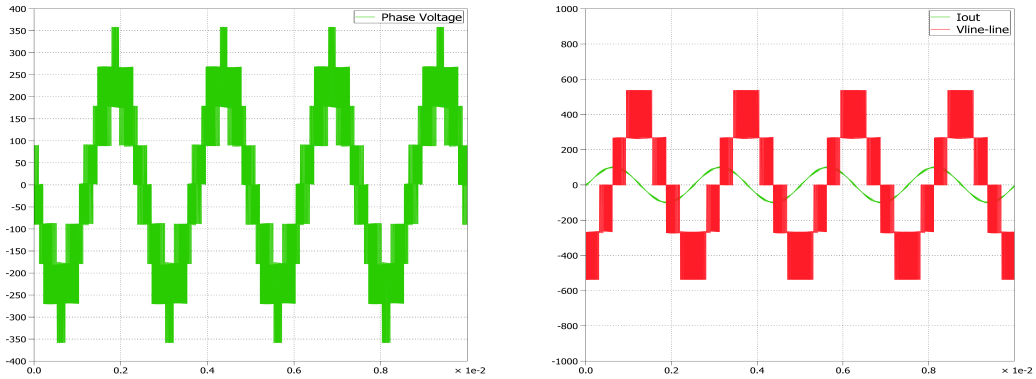


Figure 3.14: PLECS Schematic



(a) Output Phase Voltage (b) Output Line Voltage and Phase Current

Figure 3.15: Converter Output Waveforms

3.3 Device Selection

This section presents the device selection for an all SiC 3 phase TTC. The most efficient devices are sought after. These devices will then be implemented with their loss models to compare against the NPC and VSI as an accurate method of estimating the best performing converter.

Most works referenced thus far either use discrete devices at power levels of under 10 kW with IGBT-SiC hybrid solutions or custom built power modules for the TTC [20], [28], [2]. Due to the timeline of this work, custom built power modules was not an option, and therefore commercially available discrete devices are picked for a 35kW application. The TTC has mixed voltage levels as described earlier. For this application, the bus voltage is fixed at 540 VDC, adhering to aerospace standards. T1 and T4 must be rated for at least this value, whereas T2,T3 for half this value. The simulation model developed aids in finding accurate current and voltage values seen by the devices. They are rated incorporating a safety margin of 1.5. Desired ratings for all devices summarized in table 3.4. Devices T1 and T4 will be referred to as half-bridge devices and T2,T3 as neutral point devices hereon for simplicity.

Table 3.4: Desired Device Ratings

Device	Desired Characteristics with 1.5x safety
T1, T4	Vds > 810 V, Id > 90 A
T2, T4	Vds > 405 V, Id > 90A
D1, D2	Vblock > 405 V, IF > 90A

Beyond the minimum voltage and current ratings, the most important datasheet parameters for the devices are:

1. $R_{ds,on}$: The on-state resistance of the SiC devices determines the conduction losses by

I^2_{rms} * $R_{ds,on}$. The device with the lowest $R_{ds,on}$ would exhibit lowest conduction losses and must be used.

2. E_{on}, E_{off} : The on and off switching energies are directly proportional to switching losses, and the lowest energy consuming devices must be picked. This parameter is usually test dependent and cannot be accurately estimated until experimental verification. In the case of the TTC this is especially apparent, since T1 and T4, while blocking VDC, only between levels 0 to Vdc/2 and Vdc/2 to Vdc, thereby halving the effective commutation voltage, and thus the on and off energies.

3. V_F : Similar to the $R_{ds,on}$ of the SiC FET, SiC diodes exhibit conduction losses in the form I_{rms} * V_F, i.e the forward drop voltage. Since SiC diodes have no reverse recovery current [7], this is the only loss component.

3.3.1 Half-Bridge Devices

Table 3.5 shows the devices considered. Beyond the minimum ratings specified in Table 3.4, the junction temperature Tj is constrained to over 175 °C to ensure high temperature operation. From the metrics listed, it is clear that the Wolfspeed C3M0016120K is the best performing device due to its lowest $R_{ds,on}$ and second lowest switching energies. It also has the added benefit of the TO-247-4 package, coming with a Kelvin source pin that aids gate driver design.

Table 3.5: Half-Bridge Devices

Manufacturer	Part	Vds(V)	Ids(A)	Tj (C)	Rds max (mΩ)	Etotal (mJ)	Package
Wolfspeed	C3M0021120D	1200	100	175	28.8	4.7	TO247-3
Wolfspeed	C3M0016120D	1200	115	175	22.3	7.5	TO247-3
Wolfspeed	C3M0016120K	1200	115	175	22.3	1.9	TO247-4
Microchip	MSC025SMA120B	1200	103	175	28	2.22	TO247-3
ON Semi	NVHL020N120SC1	1200	118	175	27	2.22	TO247-3

3.3.2 Neutral-Point Devices

A similar comparison is done for the neutral point devices, and the C3M0015065K device is found to be best performing, both in terms of lowest $R_{ds,on}$ as well as switching energies. It also has the added advantage of being the same package as the Half-Bridge devices, thereby ensuring symmetry in the layout phase.

Since there are no trade-off parameters in the diode, the SiC diode with the lowest forward drop voltage within the ratings specified is chosen . The Infineon IDWD40G120C5 with a forward drop of 1.7 V is chosen. It is also beneficial to address that an external diode is chosen for the neutral point bidirectional switch since these diodes commutate the full load current. Had the SiC body diodes of the C3M0015065K been used for this, their forward drop voltage of 4.7 V would result in much more heat and losses in the package, ultimately leading to low efficiency and reliability.

Table 3.6: Neutral-Point Devices

Manufacturer	Part	Vds(V)	Ids(A)	Tj (C)	Rds max (mΩ)	Etotal (mJ)	Package
Wolfspeed	C3M0015065K	650	120	175	20	0.5	TO247-4
Wolfspeed	C3M0016120D	1200	115	175	22.3	7.5	TO247-3
Wolfspeed	C3M0016120K	1200	115	175	22.3	1.9	TO247-4
STM	SCTH100N65G2	650	95	175	32	0.98	H2-PAK-7
ROHM	SCT3017ALHRC11	650	118	175	22.1	0.55	TO247-3

3.4 Converter Loss Comparisons

Having gone through a comprehensive review and device selection process, the TTC, NPC and VSI converters can finally be compared in this section on a level playing field. The devices chosen for the TTC would also be the most efficient for the VSI and NPC, therefore no additional device selection is required. The VSI would simply use the Half Bridge devices

for all of its 6 devices, whereas the NPC would use the neutral point devices for its switches and diodes. Additionally, all 3 converters use the SPWM switching scheme. PLECS is used to determine switching and conduction losses for the systems using the device properties built into the switch models. The switching frequency is restricted to under 45 kHz, in compliance with aerospace EMI standards.

3.4.1 TTC vs NPC

35kW systems are simulated for both 3-L converters with varying switching frequency. The results are shown in Figure 3.16. It is clear that the TTC is the superior performing converter until 45kHz, where the switching losses start to dominate and the NPC turns out to be about 0.1 % more efficient. This comparison proves that superiority of the TTC in this application, as it is the more efficient option for the switching frequencies typically used on air crafts. While previous works [28] established 35 kHz as the efficiency crossover point with IGBT technology, all SiC TTC pushes this boundary higher. The varying junction temperature on the x-axis is intentionally simulated to show behavior at higher power levels where the junction temperature would be higher. Additionally, the PLECS model uses the corresponding on state resistances to determine a more accurate operating point. From this plot, 40 kHz is chosen to be the nominal operating frequency of the system and can now be compared against the VSI.

3.4.2 2-L vs 3-L

All 3 converters are simulated within nominal conditions of 35kW switching at 40 kHz. Figure 3.17 shows the results, confirming the superiority of the TTC at this operating point. Lastly, the loss component breakdown is presented in 3.18 exhibiting the nature of the TTC wherein the topology inherently combines the low conduction losses from the VSI and

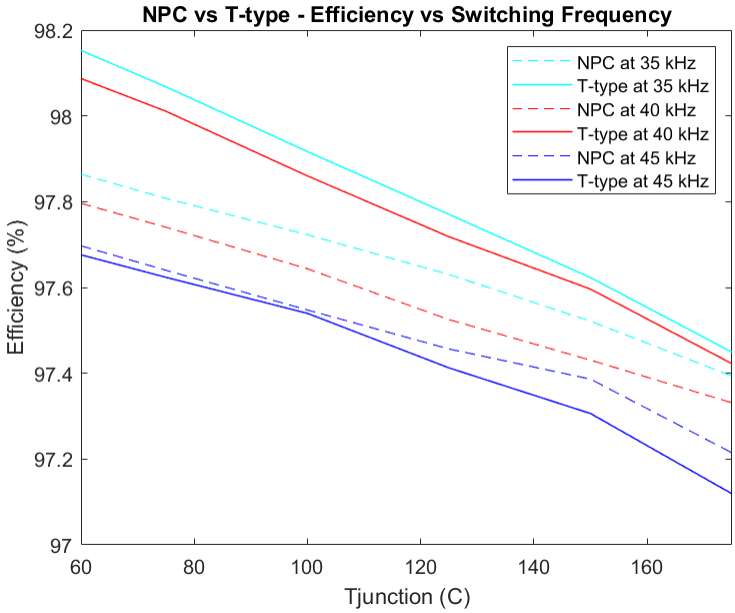


Figure 3.16: NPC vs TTC

low switching losses of the NPC to form a formidable solution for low-medium switching frequency applications.

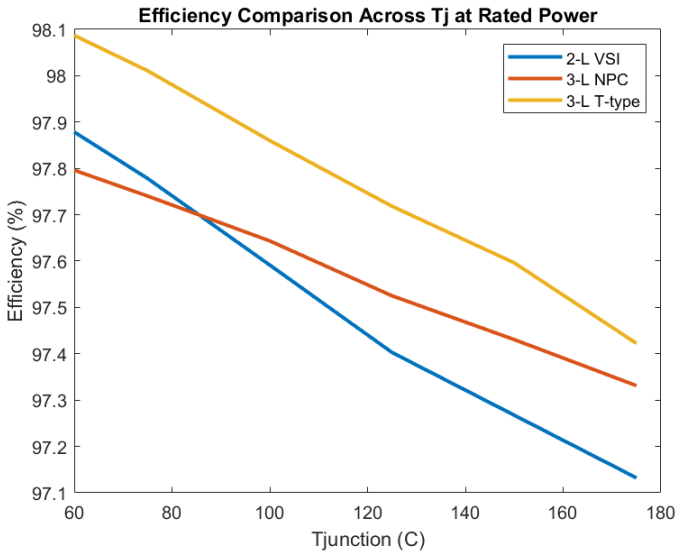


Figure 3.17: NPC vs TTC vs VSI

Figure 3.18: Loss Components Comparison

CHAPTER

4

THERMAL MODEL

A detailed analysis of the thermal behavior of the T-Type Converter is presented in this chapter. For a high power density design, it is of utmost importance to optimize the cooling mechanism of the system, as it takes up the most volume. Additionally, devices must be cooled efficiently to avoid the possibility of catastrophic thermal runaway where the devices would fail due to exceeded maximum junction temperature ratings. PLECS and MATLAB are used in conjunction to procure and analyze loss data in order to estimate the cooling requirements of the system. The governing equation for this analysis is the relationship between thermal resistance R_{th} , P_{loss} and the difference in temperatures between the surfaces Δ T. They are related as shown in equation 4.1. Specifications of the system demand forced air cooling. This chapter lays out the approach undertaken towards an optimal

solution.

$$P_{loss} = \frac{\Delta T}{R_{th}} \tag{4.1}$$

4.1 Heat Dissipation Model

Before estimating the losses it is important to model the flow of heat in the system. This is shown in Figure 4.1. The source of the heat is the junction of the die, due to the conduction and switching losses when operating. The flow of this heat is through the following network:

1. $Rth_{j\text{-}c}$: The thermal resistance between the junction and case due to the packaging technology used

2. Rth_{TIM}: The characteristic resistance of the thermal interface material securing onto the electrical insulating material

3. Rth_{AlN}: Aluminum Nitride is the electrically insulating material of choice due to its low characteristic resistance. It ensures that the heatsink and the device do not interface electrically

4. $Rth_{H\text{-}A}$: The last resistance to consider is that between the heatsink and ambient temperature determined by the physical geometry of the heatsink and cooling approach undertaken

Figure 4.2 shows an equivalent electrical analogy. In this case, the loss is modeled as as constant current source, flowing through a series of resistances to a constant voltage source representing the ambient temperature. In order to find the appropriate heatsink solution, the $Rth_{H\text{-}A}$ must be calculated with the knowledge of all other variables. All other

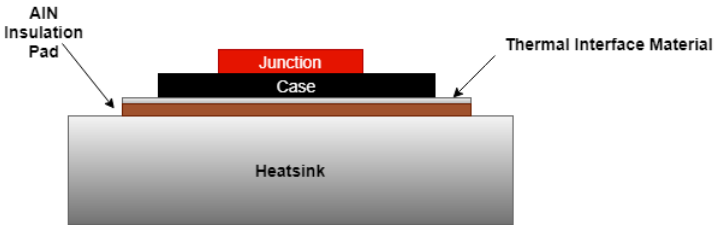


Figure 4.1: Thermal Stackup

thermal resistance values are data sheet parameters that can be estimated. The losses are found in the method laid out in the following section.

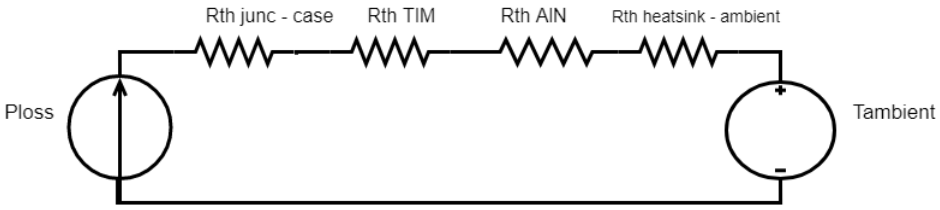


Figure 4.2: Thermal Equivalent Circuit

4.2 PLECS - MATLAB Iterative Loss Estimation

4.2.1 PLECS Initial Loss Data

PLECS offers a useful thermal toolbox that serves as a bridge between the electrical and thermal dynamics of the converter. As shown in Figure 4.3 the purple box represents an isothermal surface, covering all enclosed devices at the same temperature. The probes on the top right corner extract losses for the devices necessary, averaged over a switching cycle for conduction losses, and using impulse averages at switching frequency for switching losses.

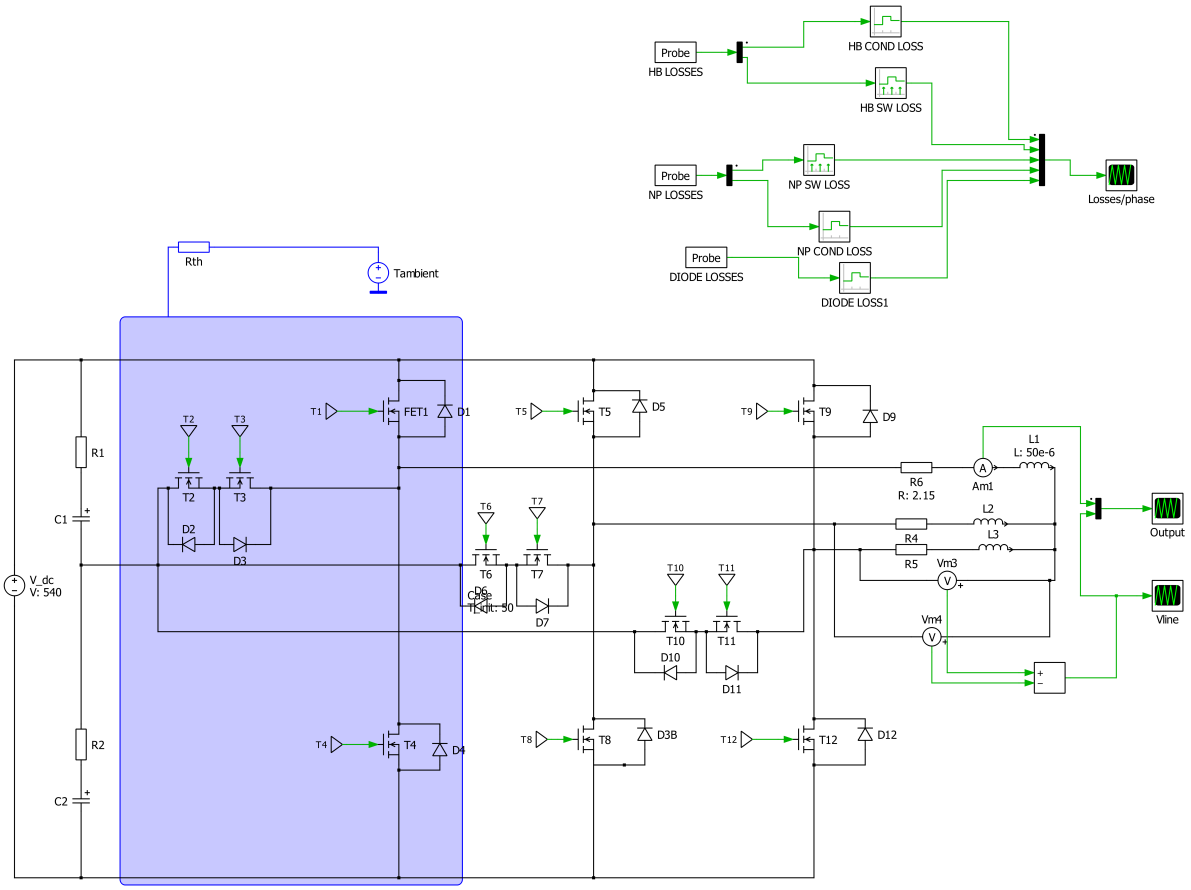
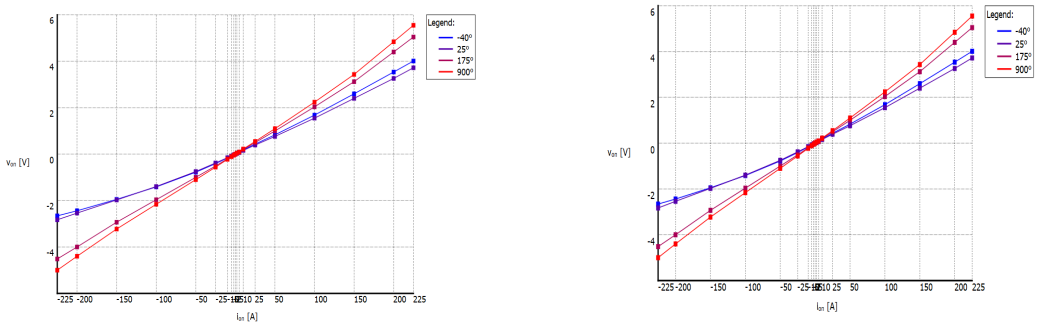


Figure 4.3: Thermal Analysis Setup

As a first step, it is important to estimate the loss profile of each device across different junction temperatures. This is done by using a look-up table approach wherein the device loss characteristics such as $R_{ds,on}$ and E_{on} and E_{off} are imported into the device electrical model. $R_{ds,on}$ is highly junction temperature dependent and therefore effects losses dramatically across different temperatures as shown in Figure 4.4 for both types of switches. The diode also exhibits a similar characteristic as shown in 4.5.



(a) HB Conduction Loss

(b) Neutral Point Conduction Loss

Figure 4.4: Conduction Loss Temperature Dependence - Switches

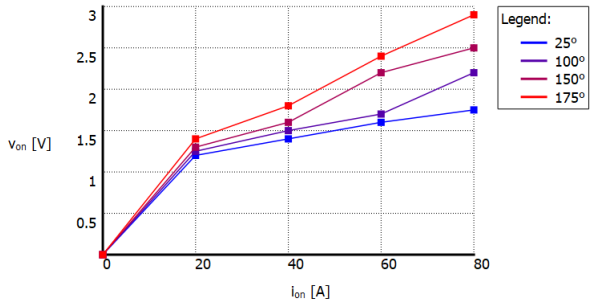
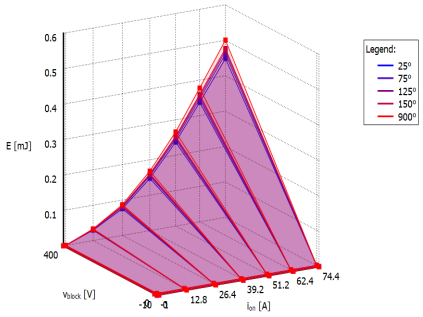
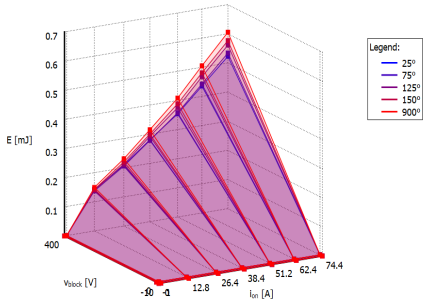


Figure 4.5: Diode Conduction Loss Table

Switching Losses on the other hand do not have as strong a dependency on the junction temperature, as shown in the small variation in the switching energies with temperature in Figures 4.6 and 4.7.

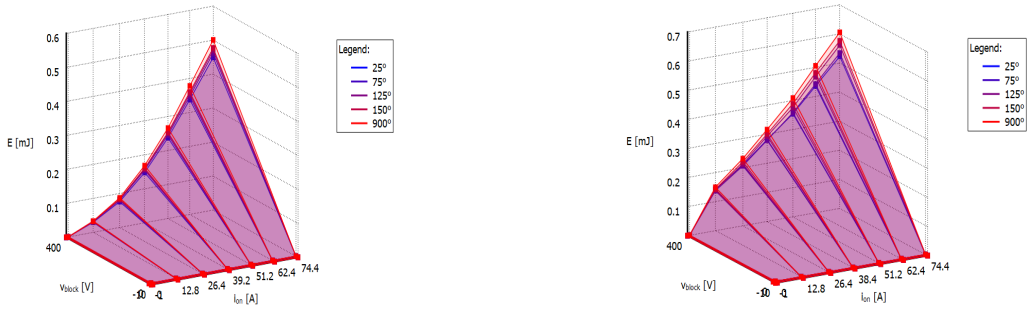


(a) HB Switch Off Energy



(b) HB Switch On Energy

Figure 4.6: Half Bridge Switches Switching Energies



(a) Neutral Switch Off Energy

(b) Neutral Switch On Energy

Figure 4.7: Neutral Point Switches Switching Energies

The converter is simulated with changing junction temperature to understand the effects. This is done by setting the ambient temperature and junction temperature to be the same in the PLECS model, with an negligible thermal resistance between them. Additionally, the thermal capacitance of the isothermal heatsink surface is set to a large value to ensure that the temperature is kept constant. The data points for each device from 60 °C to 175 °C is collected in this fashion while also varying output power.

4.2.2 MATLAB Data Curve-fitting

The conduction and switching loss data from PLECS is imported into MATLAB to form 3-D loss surfaces for each device. A polynomial curve-fitting approximation is used for the same. The results of the curve fit are shown in Figures 4.8, 4.9 and 4.10. A few key observations are made:

1. The system has an asymmetrical loss distribution, dominated by the half-bridge losses

2. An estimation must be made for the amount of heat being extracted per phase into

the heatsink

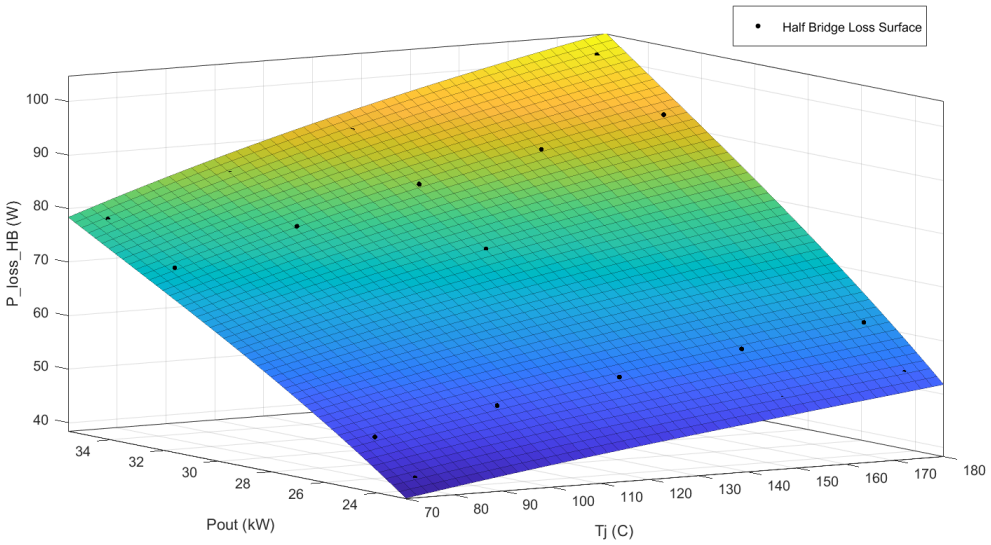


Figure 4.8: Half Bridge Devices Loss Surface

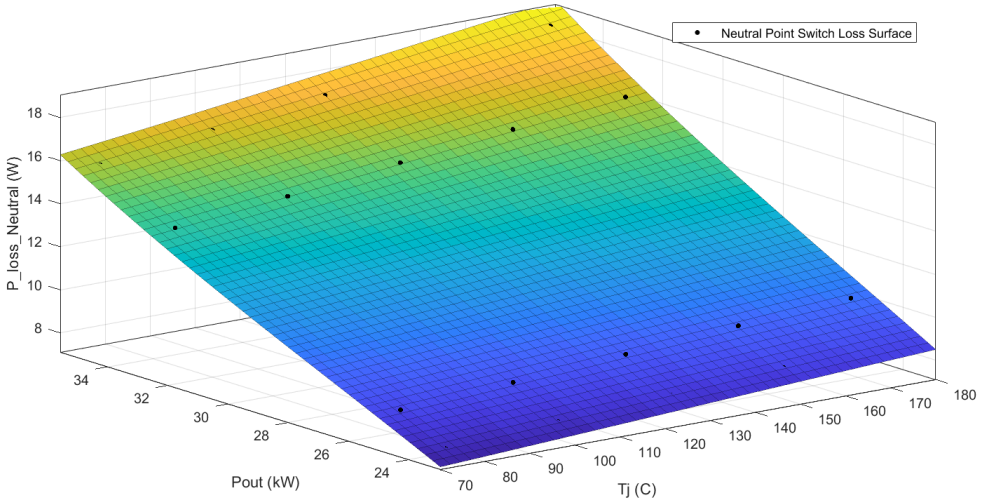


Figure 4.9: Neutral Point Switches Loss Surface

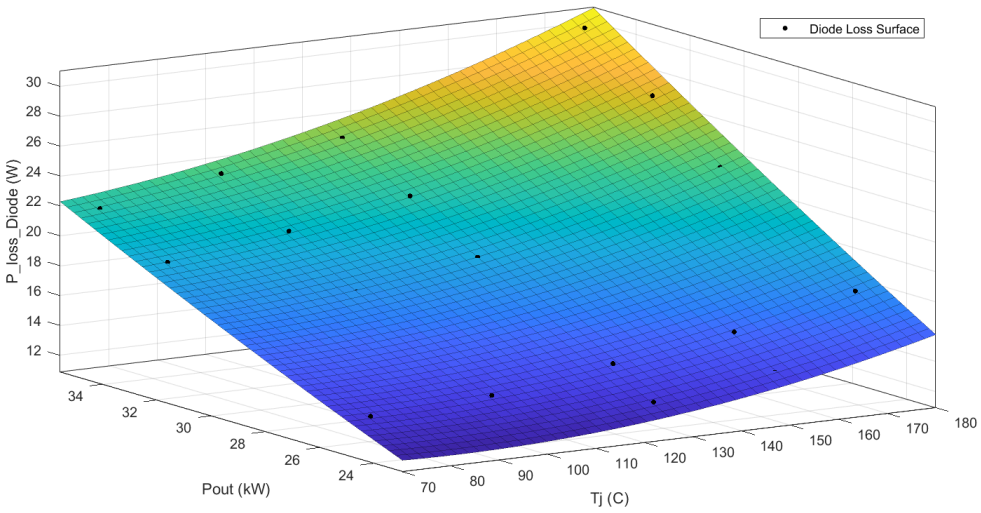


Figure 4.10: Diode Loss Surface

An additional consideration also needs to be made while assessing the heat extraction: the junction to case thermal resistance of each device. These are asymmetrical as well as shown in Table 4.1 and need to be factored in since they would add to the unequal heat source contributions.

Table 4.1: Junction to Case Resistance Mismatch

Device	$Rth_{j\text{-}c}$ (C/W)
Half Bridge	0.27
Neutral Point	0.35
Diode	0.4

4.2.3 MATLAB Iterative Approximation

In order to utilize the data extracted to from as an accurate a model as possible in simulation for the rated 35 kW power level, the following simple recursion method is developed:

1. Initial junction temperature of device guessed
2. Losses found from loss surface data
3. Temperature rise in heatsink calculated per phase
4. Actual junction temperature reverse calculated

Once the initial guess and reverse calculated numbers match, the heatsink temperature is known. With a constant ambient temperature, the required $Rth_{H\text{-}A}$ is known. This model serves to factor in the mismatch in heat sources as well as $Rth_{J\text{-}C}$ for each device and does this by using a permutations of the single heat flow equation 4.1. While it uses approximations in the curve-fitting process, it enables a good starting point to be verified in simulation.

For the 35kW system, the results are as shown in table 4.2. Note that the losses here are per device and are scaled appropriately per phase.

Table 4.2: Recursive Approximation Result

$T_{ambient}(°C)$	50
$T_{j,HalfBridge}(°C)$	127
Conduction Loss (W)	45.08
Switching Loss (W)	46.14
$T_{jNeutral}(°C)$	106
Conduction Loss (W)	14.5
Switching Loss (W)	2.4
$T_{jDiode}(°C)$	109
Conduction Loss (W)	24.4
Rth Heatsink/phase (°C /W)	0.168

4.2.4 PLECS Verification

Finally, the entire system model is simulated in PLECS including previously ignored thermal resistances. The $Rth_{j\text{-}c}$ values are incorporated within the device models as Cauer models extracted from datasheets for a more accurate representation as shown in Figures 4.11 , 4.12, 4.13.

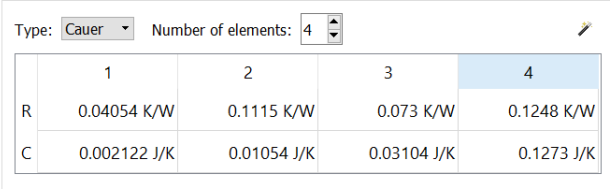


Figure 4.11: Half Bridge Cauer Model

Type: Cauer Number of elements: 4

	1	2	3	4
R	0.04054 K/W	0.1115 K/W	0.073 K/W	0.1248 K/W
C	0.002122 J/K	0.01054 J/K	0.03104 J/K	0.1273 J/K

Figure 4.12: Neutral Point Switch Cauer Model

Type: Cauer Number of elements: 4

	1	2	3	4
R	0.0348 K/W	0.127 K/W	0.0767 K/W	0.15 K/W
C	0.0053 J/K	0.0149 J/K	0.0466 J/K	0.193 J/K

Figure 4.13: Diode Cauer Model

Additionally, the Rth_{TIM}, Rth_{AlN} and $Rth_{H\text{-}A}$ are lumped into a series resistance. The combined Rth of TIM and AlN is estimated as 0.047 °C /W. The junction temperatures are measured on PLECS and plotted in Figure 4.14. This image shows that the iterative approximation overestimates the junction temperatures for the devices, however provides a methodical starting point. The heatsink Rth can now be iterated to find the appropriate number for a set restricted maximum junction temperature.

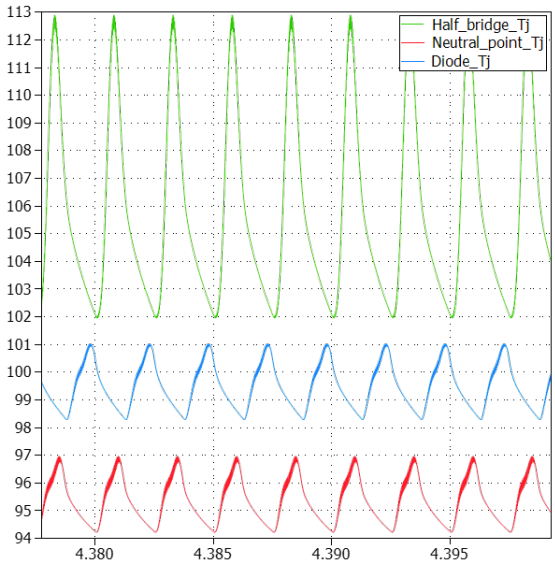


Figure 4.14: MATLAB Estimation Simulation

In this application, that limit is set to about 70% of maximum junction temperature of 120 °C. After a few iterations, an $Rth_{H\text{-}A}$ of 0.2 is found to provide the desired performance as shown in Figure 4.15.

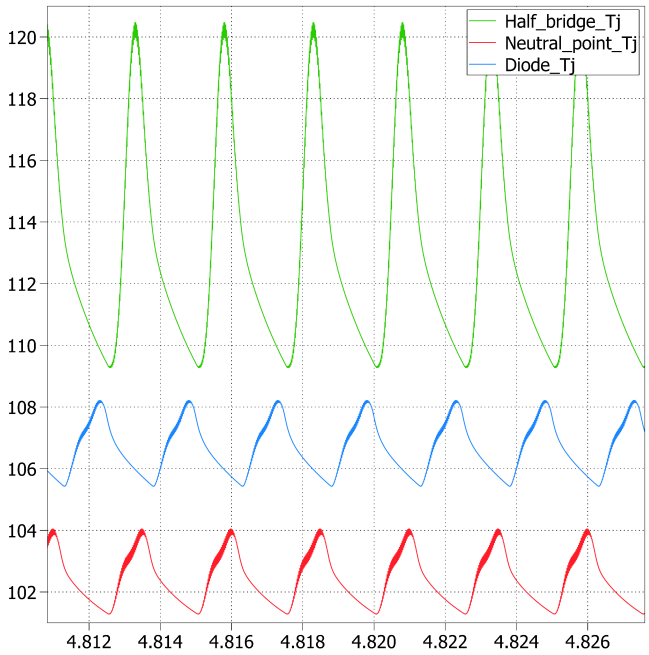


Figure 4.15: Junction Temperatures at 0.2 Rth_{H-A}

4.3 System Efficiency Estimation

At this juncture, heatsinks available commercially can be evaluated to find the appropriate cooling solution. Additionally, the final efficiency estimate for the converter's nominal operating point along with the cooling mechanism can be found. The loss profile is as shown in Figure 4.16. The efficiency estimate derived from this thermal model is summarized in Table 4.3.

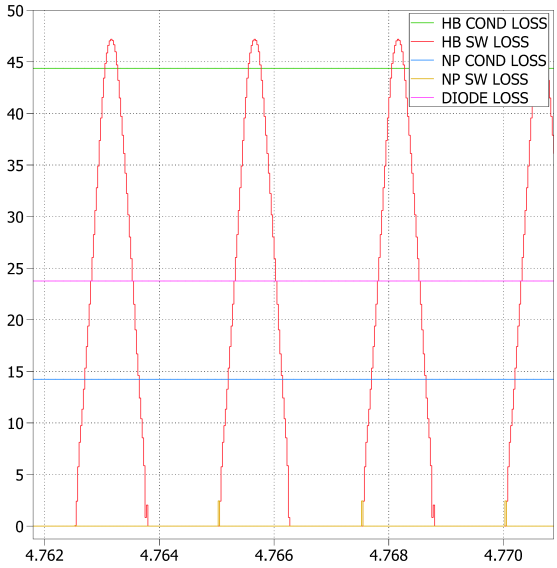


Figure 4.16: Final System Losses

Table 4.3: Final Efficiency Estimate

Half Bridge Losses (W)	91.56
Neutral Point Losses (W)	16.6
Diode Losses (W)	23.75
Total Losses (W)	791.5
Efficiency	97.78 %

CHAPTER

5

HIGH ALTITUDE DESIGN

The targeted application in this work requires special attention to the standards for electronic systems at high altitude as well as other applicable standards. Specifically, four considerations are focused on and the drive design decisions namely:

1. Capacitor sizing to adhere to the MIL-STD-704 standard
2. Board level clearance required by IEC 60664-1 standard at 30,000 feet
3. Board level clearance required by IEC 60664-1 standard at 30,000 feet
4. Fan sizing for equivalent operation at 30,000 feet

5.1 Capacitor Sizing

The DC link capacitor must be appropriately sized depending on the rated power and maximum allowable voltage ripple. As shown in [20], the capacitance value for a TTC is calculated as:

$$C_{dc} > \frac{\frac{8 \times P_{out}}{3 \times m_a \times VDC \times \cos\phi} \sqrt{\frac{m_a}{2} \times \left(\frac{\sqrt{3}}{2\pi} + (\frac{2\sqrt{3}}{\pi} - \frac{9 \times m_a}{8}) \cos\phi^2 \right)}}{\Delta VDC \times f_s} \tag{5.1}$$

The MIL-STD-704 enforces an absolute maximum ripple voltage of 2.2%. Using the system ratings in equation 5.1, the minimum capacitance requirement is 600 μF. This number is significantly large and will play into increasing the volume of the overall system.

5.2 Creepage and Clearance

The IEC 60664-1 standard defines the necessary standards for board level creepage and clearance necessary at high altitudes. These standards are derived from Paschen's law that states that the dielectric properties of air change with altitude [9]. Essentially, air is not as good an insulator at high altitude resulting in a lower breakdown voltage. This phenomenon is illustrated in 5.1, showing how the curve shifts with increasing voltage [9]. The creepage and clearance of the power supply has to take this into account.

[31] Provides a guide to calculating the necessary clearance and creepage required at a specified height above sea level. The definitions of importance are:

1. Rated operational voltage (Ue): A rated operational voltage of an equipment is a value of voltage which, combined with a rated operational current, determines the application of the equipment

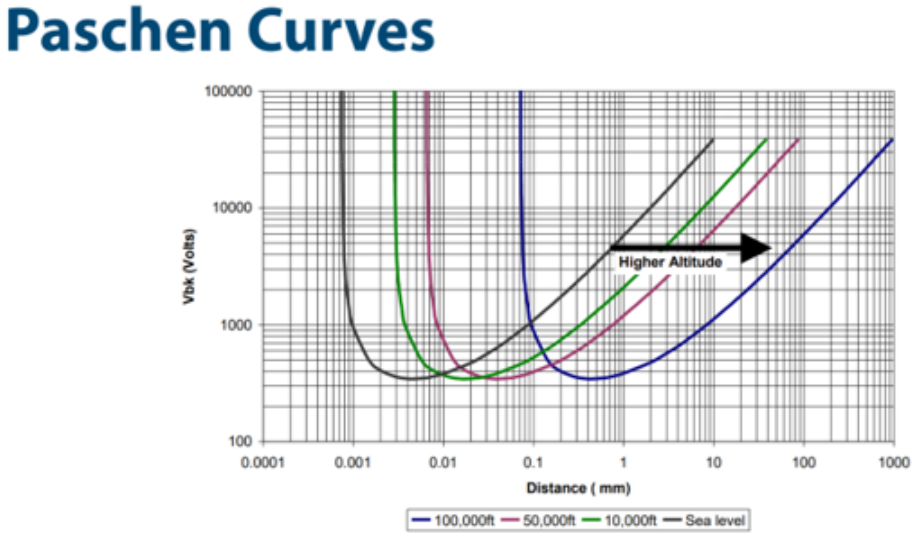


Figure 5.1: Paschen's Curves

2. Rated insulation voltage (Ui): The rated insulation voltage of an equipment is the value of voltage to which dielectric tests and creepage distances are referred

3. Rated impulse withstand voltage (Uimp): The peak value of an impulse voltage of prescribed form and polarity which the equipment is capable of withstanding without failure under specified conditions of test and to which the values of the clearances are referred

4. Rated operational current (Ie): A rated operational current of an equipment is stated by the manufacturer and takes into account the rated operational voltage, the rated frequency and the utilization category

5. Overvoltage category: conventional number based on limiting (or controlling) the values of prospective transient overvoltages occurring in a circuit

Ui at height H is scaled as shown in equation 5.2 where m is a constant 0.5 and H is the

height in metres :

$$K_a = e^{\left(m\frac{H}{150}\right)} \quad (5.2)$$

The scaled voltage is used to determine creepage from a table factoring in pollution degree and material group. The relevant table is shown in Figure 5.2. The maximum impulse voltage Uimp is used to determine clearance using the table shown in Figure 5.3 both found is [31].

Minimum creepage distances

Rated insulation voltage of equipment or working voltage a.c. r.m.s. or d.c. [b,c,d]	Minimum creepage distances for equipment subject to long term stress													
	Printed wiring material													
	Pollution degree													
	1	2	1	2			3				4			
	Material groups													
	All	All except IIIb	All	I	II	III	I	II	IIIa	IIIb	I	II	IIIa	IIIb
V	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm
10	0,025	0,04	0,08	0,4	0,4	0,4	1	1	1		1,6	1,6	1,6	
12,5	0,025	0,04	0,09	0,42	0,42	0,42	1,05	1,05	1,05		1,6	1,6	1,6	
16	0,025	0,04	0,1	0,45	0,45	0,45	1,1	1,1	1,1		1,6	1,6	1,6	
20	0,025	0,04	0,11	0,48	0,48	0,48	1,2	1,2	1,2		1,6	1,6	1,6	
25	0,025	0,04	0,125	0,5	0,5	0,5	1,25	1,25	1,25		1,7	1,7	1,7	
32	0,025	0,04	0,14	0,53	0,53	0,53	1,3	1,3	1,3		1,8	1,8	1,8	
40	0,025	0,04	0,16	0,56	0,8	1,1	1,4	1,6	1,8		1,9	2,4	3	
50	0,025	0,04	0,18	0,6	0,85	1,2	1,5	1,7	1,9		2	2,5	3,2	
63	0,04	0,063	0,2	0,63	0,9	1,25	1,6	1,8	2		2,1	2,6	3,4	
80	0,063	0,1	0,22	0,67	0,95	1,3	1,7	1,9	2,1		2,2	2,8	3,6	
100	0,1	0,16	0,25	0,71	1	1,4	1,8	2	2,2		2,4	3	3,8	
125	0,16	0,25	0,28	0,75	1,05	1,5	1,9	2,1	2,4		2,5	3,2	4	
160	0,25	0,4	0,32	0,8	1,1	1,6	2	2,2	2,5		3,2	4	5	
200	0,4	0,63	0,42	1	1,4	2	2,5	2,8	3,2		4	5	6,3	
250	0,56	1	0,56	1,25	1,8	2,5	3,2	3,6	4		5	6,3	8	
320	0,75	1,6	0,75	1,6	2,2	3,2	4	4,5	5		6,3	8	10	
400	1	2	1	2	2,8	4	5	5,6	6,3		8	10	12,5	
500	1,3	2,5	1,3	2,5	3,6	5	6,3	7,1	8		10	12,5	16	
630	1,8	3,2	1,8	3,2	4,5	6,3	8	9	10		12,5	16	20	a
800	2,4	4	2,4	4	5,6	8	10	11	12,5		16	20	25	
1000	**3,2**	**5**	**3,2**	**5**	**7,1**	**10**	**12,5**	**14**	**16**		**20**	**25**	**32**	
1250			4,2	6,3	9	12,5	16	18	20		25	32	40	
1600			5,6	8	11	16	20	22	25		32	40	50	
2000			7,5	10	14	20	25	28	32		40	50	63	
2500			10	12,5	18	25	32	36	40		50	63	80	
3200			12,5	16	22	32	40	45	50	a	63	80	100	
4000			16	20	28	40	50	56	63		80	100	125	
5000			20	25	36	50	63	71	80		100	125	160	
6300			25	32	45	63	80	90	100		125	160	200	
8000			32	40	56	80	100	110	125		160	200	250	
10000			40	50	71	100	125	140	160		200	250	320	

Figure 5.2: Creepage Standard Table

At 30,000 feet for the ratings of this system, creepage required is 14mm whereas clearance is 4mm. The high creepage requirement further challenges the high power density goal, as it generally increases the volume of the system.

Minimum clearances in air

Altitude m	for U_{imp}= 4kV	for U_{imp}= 6kV	for U_{imp}= 8kV	for U_{imp}= 12kV
2000	3,0 mm	5,5 mm	8,0 mm	14,0 mm
3000	3,4 mm	6,3 mm	9,1 mm	16,0 mm
4000	3,9 mm	7,1 mm	10,3 mm	18,1 mm
5000	4,4 mm	8,1 mm	11,8 mm	20,7 mm
6000	5,1 mm	9,4 mm	13,6 mm	23,8 mm
7000	5,9 mm	10,7 mm	15,6 mm	27,3 mm
8000	6,8 mm	12,4 mm	18,0 mm	31,5 mm
9000	7,9 mm	14,4 mm	21,0 mm	36,7 mm
10000	9,1 mm	16,6 mm	24,2 mm	42,3 mm
15000	20,0 mm	36,7 mm	53,4 mm	93,4 mm
20000	43,5 mm	79,8 mm	116,0 mm	203,0 mm

Figure 5.3: Clearance Standard Table

5.3 Cooling Fans Calibration

The density of air at high altitude is less than that at sea level [32]. This reduces its convective capability and overall heat transfer capacity. This drastically affects force air cooled systems' ability to extract heat from the system due to a reduced amount of airflow as well as a reduction in the static pressure of the air that is flowing. To counteract this, more powerful fans must be used at high altitudes. The key attributes of the fans are:

1. Cubic Feet per Minute (CFM): CFM defines a fan's airflow ability over a given volume. In the case of this system, the airflow goes through the fins of the heatsink. The required value at sea level is calculated in equation 5.3 where Q refers to the amount of heat being extracted from the system in kW and Δ T refers to the difference in air temperature at either end of the heatsink.

$$CFM_{sealevel} = \frac{1760 \times Q}{\Delta T} \tag{5.3}$$

This equation is modified at high altitude as shown in 5.5 with an added term r that

refers to the density of air at the specified altitude. Figure 5.4 specifies this density [26].

$$CFM_{altitude} = \frac{2074 \times Q}{r \times \Delta T} \tag{5.4}$$

Using this equation, the required CFM at 30,000 ft is calculated as 27.2.

Table 1: Air Density Change with Altitude		
Altitude (ft)	Density (lb/ft^3)	Density (kg/m^3)
Sea Level	.075	1.19
5000	.066	1.06
10000	.056	.904
15000	.048	.771
20000	.041	.652
25000	.034	.549
30000	.029	.458
35000	.024	.379

Figure 5.4: Air density vs Altitude

2. Static Pressure: The static pressure ρ provided by the fan's forced air flow is also diminished at high altitude due to reduced air density. The compensated required pressure is calculated using the fan law [26]

$$\frac{\rho_{sealevel}}{\rho_{altitude}} = \left(\frac{CFM_{sealevel}}{CFM_{altitude}}\right)^2 \tag{5.5}$$

Using this equation, the required static pressure at 30,000 ft is calculated as 198 Pa.

Table 5.1 summarizes the extra considerations for high altitude design.

Table 5.1: High Altitude Design Considerations Summary

Metric	Requirement
Capacitance	> 600 uF
Creepage	14 mm
Clearance	4 mm
CFM	27.2
Static Pressure	198 Pa

CHAPTER

6

SYSTEM CONSTRUCTION

This chapter lists all the necessary components required to build the converter. The most power dense solution is picked for every component. Additionally, the layout is optimized to minimize parasitic inductances, and verified through simulation in ANSYS Q3D.

6.1 DC Link Capacitors

Film capacitors chosen for this application due to their characteristic high ripple capacity as well as high reliability [4]. Additionally, they typically have low ESR, resulting in low losses and self heating. A 2x safety margin is considered in creating the DC link, selecting the smallest volume capacitors with adequate ripple current capability as shown in [18].

The WIMA DCP4G064009JD4KSSD shown in is found to have the highest capacitance per volume. Three of them are used in parallel per split bus. It's key characteristics are shown in Table 6.1

Table 6.1: Capacitor Characteristics

Metric	Measure
Capacitance	400 uF
VDC Rating	400 V
Ripple Current Rating	41 A
ESR	1 m Ω
Dimensions	57 mm x 45 mm x 65 mm

Figure 6.1: DC Link Capacitor

6.2 Sensing Circuitry

DC link voltage and output phase current are to be sensed for closed loop control implementation purposes. There are several methods for sensing both of these signals and the smallest volume consuming are chosen.

6.2.1 DC Link Voltage Sensing

This process does not have high bandwidth requirements since the instantaneous DC voltage is not of interest for controlling. Thus, an isolated amplifier is used for this purpose. The DC link voltage is connected to the amplifier through a resistor divider network to scale it down to the allowable input voltage of the amplifier. The Texas Instruments AMC 1301 shown in Figure 6.2 is chosen for this application due to its simplistic but high performing design, as well as the many application notes associated with using it for this application. The output of the amplifier is connected to a high precision gain boosting amplifier OPA 320 for ADC scaling.

Figure 6.2: DC Link Sensing Amplifier

6.2.2 Output Current Sensing

The output current sensing is typically a high bandwidth requiring process. A relatively new technology is used for this purpose, hall-effect integrated circuits from Allegro as shown in Figure 6.3. These isolated sensors have high bidirectional current sensing capabilities as well as suitable mV/A sensitivity for direct interfacing with the controller. Additionally, the built in isolation removes the need for high volume isolated power supplies, making these ICs suitable for high power density applications. The ACS 772 is used in this case with a bidirectional 150A sensing capability as well as built in high dv/dt shielding.

Figure 6.3: Phase Current Sensing IC

6.3 Heatsink

Heatsinks are chosen following the analysis from Chapter 4. Two orientations, one per phase and one per converter are explored. Fischer Elektronik is found to have the highest performing cooling aggregates and the following options are found to be most optimal on the thermal resistance - volume trade off.

1. One per phase: LAM 5 shown in Figure 6.4. This selection utilizes 3 heatsinks per

converter, one per phase. Figure 6.5 shows the thermal resistance properties with varying fans and lengths. For an Rth of 0.2 the 150 mm, 24 VDC fan option is selected. The total volume per converter using this option is 1.125L

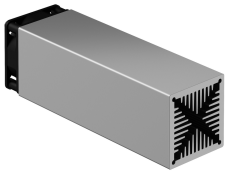


Figure 6.4: LAM 5

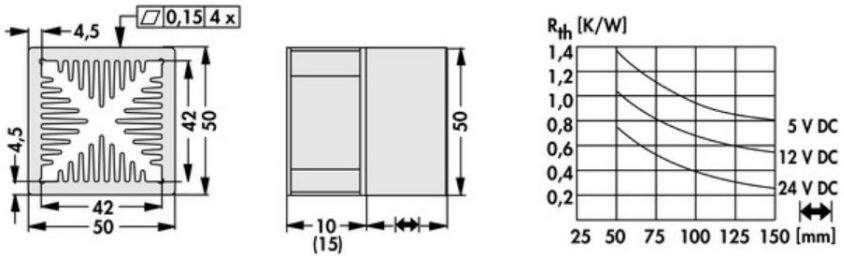


Figure 6.5: LAM 5 Characteristics

2. One per converter: LA 30 shown in Figure 6.6. This selection utilizes one heatsink per converter. Figure 6.5 shows the thermal resistance properties with varying fans and lengths. The thermal resistance must be one-third that of a 3 heatsink solution. For an Rth of 0.06 the 150 mm, 24 VDC fan option is selected. The total volume per converter using this option is 1.9L.

While the LAM5 option is smaller in volume, it requires spacing between phases for

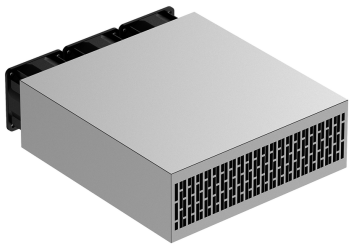


Figure 6.6: LA 30

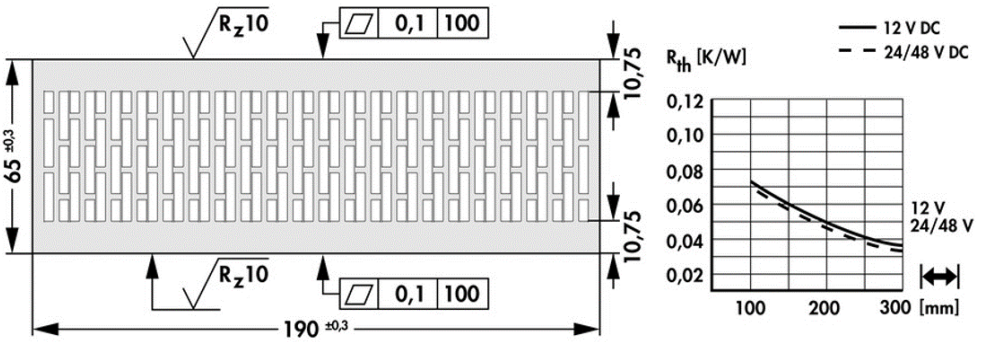


Figure 6.7: LA 30 Characteristics

mounting, whereas the LA 30 is a single piece. Layouts of the power stage considering both heatsinks are shown in the following sectionto determine the smaller volume overall.

6.3.1 Fans

As indicated in Chapter 5, the fans the cooling aggregates come with will not be adequate for a high altitude application. Therefore, fans with the scaled CFM and Static Pressure values are found while maintaining the length and height dimensions of the original fans for ease of swap. The LA 30 requires a CFM> 137 and static pressure > 198 Pa to perform at the same level in high altitude. The Sanyo 9GV0812G1011 fulfills these requirements with a

CFM of 137 and pressure of 490 Pa. It is 60mm x 60mm x 38mm in volume, 6mm wider than the original fan. Similarly, the Delta PFB0512EHF fulfills the requirements of the LAM 5 as shown in Chapter 5. The fan has a CFM of 31.6, pressure of 261.8 Pa. Its volume is 50mm x 50mm x 32 mm, more than twice the width of the original option.

6.4 Layout

The most pivotal step in the layout is the device orientation. With 6 devices per phase, there are several possible combinations of the layout. The design focus is to keep the current commutation loops as small as possible in order to minimize parasitic inductances, while maintaining symmetry as much as possible. Parasitic inductances in high switching frequency applications cause overshoots on the device drain-source voltages. If unchecked, these overshoots may cause device failure. This design process is explained in the subsections following.

6.4.1 Commutation Loop

The topic of commutation loops is revisited with a focus on the parasitic inductances within the loop. Stray inductance is directly proportional to the length of the connection. As shown in Figure 6.8 four primary stray inductances are of interest:

1. LDC+, LDC- : These are the stray inductances due to long high voltage connections to the DC bus and are typically the most significant within the system.

2. LT2: Inductance due to the connection between T2 and bus neutral.

3. LT3: Inductance due to the connection between T3 and phase output.

In a 4-Layer PCB one layer is dedicated to the bus neutral potential, thereby minimizing LT2 by extremely short connections to the layer using vias. LT3 on the other hand, requires careful positioning to minimize the length of connection to the output node.

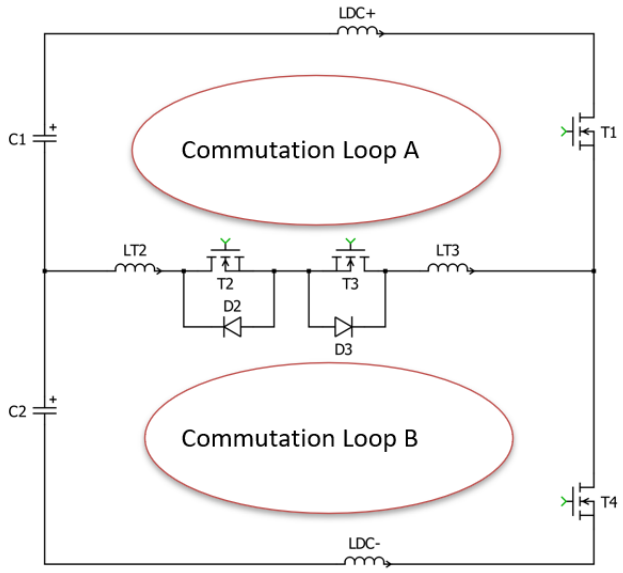


Figure 6.8: Commutation Loops

6.4.2 Device Orientation

After several permutations, 6.9 shows the optimal placement of devices. DC+ and DC- connections refer to connections to the positive and negative nodes of the DC bus respectively, split bus neutral refers to the connection to the DC link midpoint, and output is the phase output node. This layout minimizes LT3 by close connection to the output node. Additionally, a dual row design is utilized to minimize space between actively switching devices. Had a single row design been implemented, the diodes would either increase the

distance between switching nodes or been far enough from the neutral point switches wherein the additional parasitic inductances would arise between the diode and neutral point switch nodes.

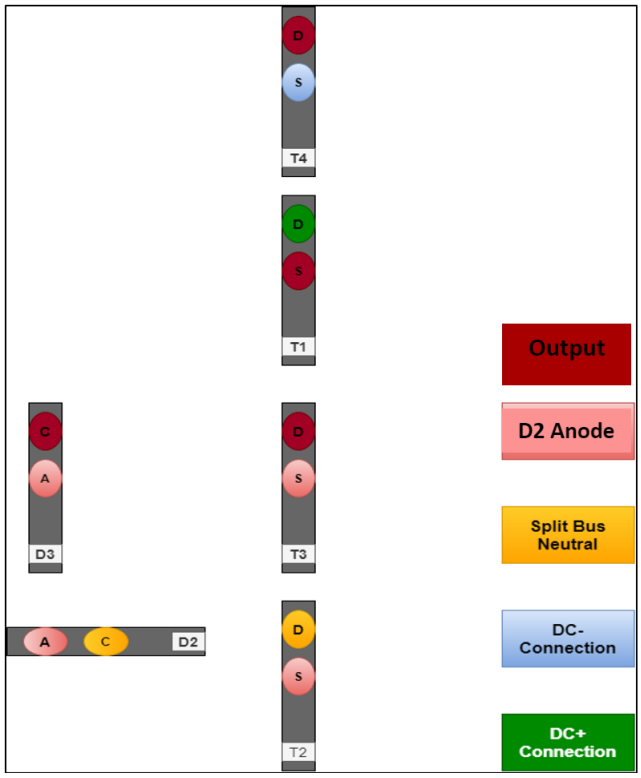


Figure 6.9: Optimal Device Orientation

6.4.3 Power Stage Layout

A 4 layer PCB is utilized with the following layer stack:

1. TOP: Signal layer with DC+ and output nodes routed
2. GND: Split bus neutral node layer

3. PWR: Power planes for sensors

4. BOT: Signal layer with DC - node routed

A creepage of 14mm is maintained between high voltage lines and a clearance of 4mm is maintained at all points.

The devices are placed and heatsinks attached to the bottom layer of the PCB. The device orientation is used for both single and 3 heatsink designs.In the 3 heatsink design, the switches are placed along the side of the heatsink and D2,D3 are bent to attach to the bottom of the heatsink. In the single heatsink, all devices are bent D2, D3 are attached the same way and all 4 switches are bent to the right, away from the diodes.

The 3 heatsink layout is as shown in Figure 6.10 and the single heatsink is as shown in Figure 6.11 with key nodes marked. The red layer is the TOP whereas the blue is BOT. The layouts are nearly identical with the exception of the mechanical layer, representing the heatsinks, in striped pink along the devices.

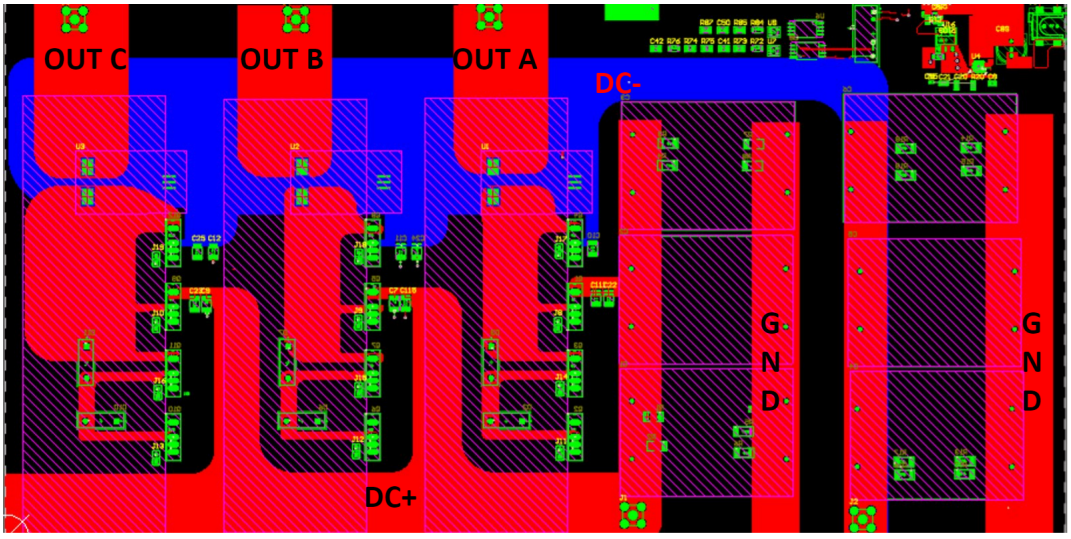


Figure 6.10: 3 heatsink layout

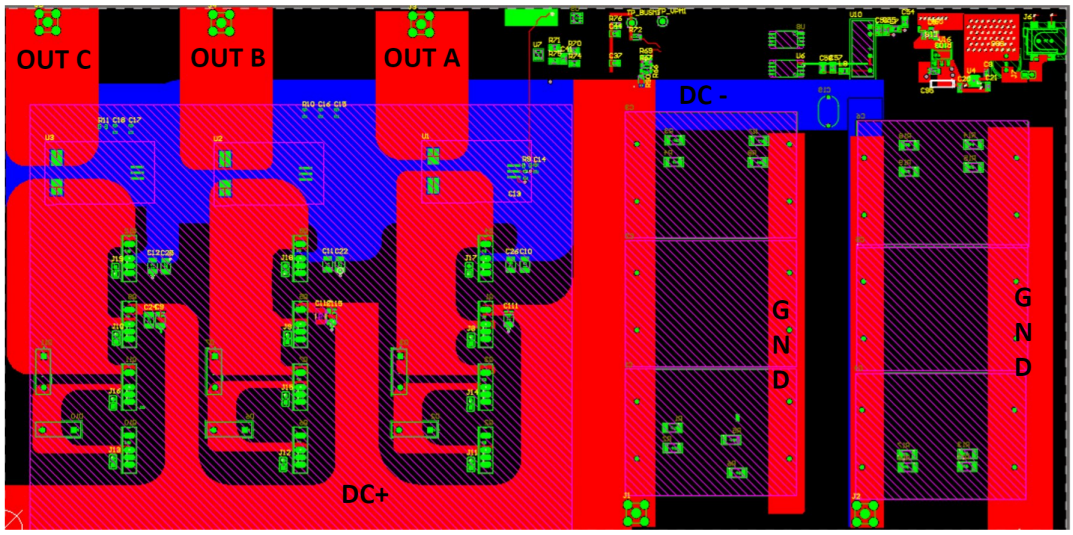


Figure 6.11: 1 heatsink layout

The layout confirms that the 3 heatsink design narrowly occupies less length due to the vertical/bent combination. It therefore would exhibit greater power density and is chosen as the final design. It also has the benefits of easier construction and debugging since only the passive devices are inaccessible once attached. Having only 2 devices bent also minimizes the number of mounting holes required through the PCB to attach the diodes to the heatsink, aiding in maintaining clearances.

6.4.4 Parasitic Extraction

The 3 heatsink layout is imported into ANSYS Q3D to estimate the parasitic inductances in the commutation loop. The estimation for LDC+ and LDC- aids in the design process of decoupling capacitors to minimize this inductance. The importing process includes defining the necessary layers and material properties. The TOP, GND and BOT layers are imported since they are the only ones part of the commutation loop. Images of the imported circuit are as shown in Figures 6.12 and 6.13.

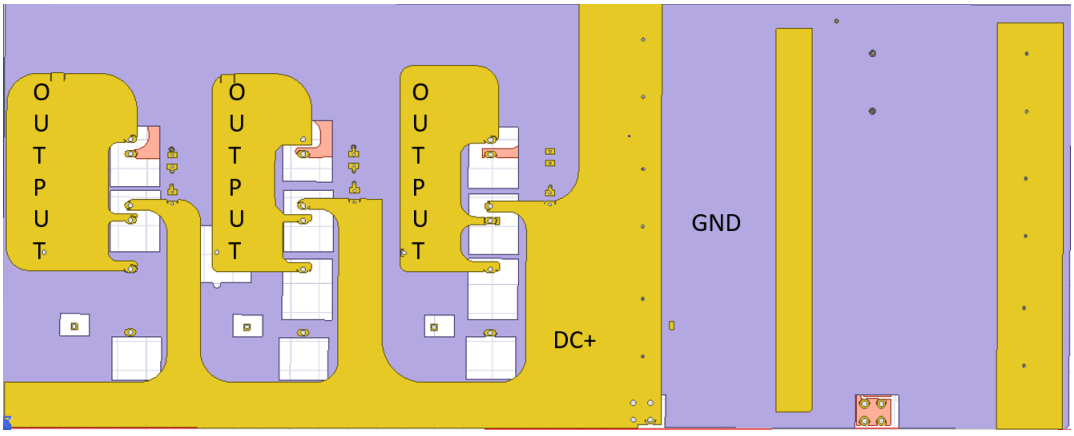


Figure 6.12: Top Layer Q3D Extraction

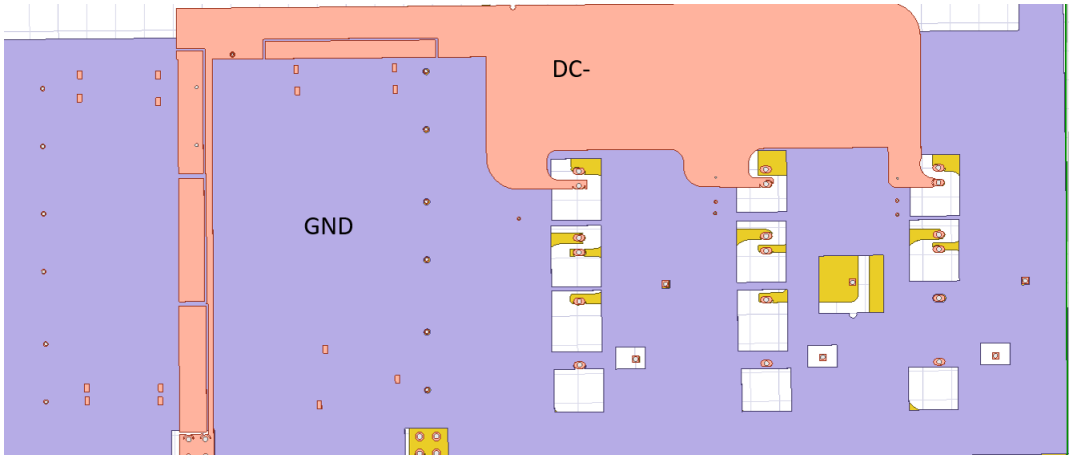


Figure 6.13: Bottom Layer Q3D Extraction

The commutation paths are identified as sources and sinks and matrix series connections are created to complete the return current path. The results of this extraction are as shown in Table 6.2. As expected, LDC+ and increase with every phase due to the longer current path from the DC link. These inductances would result in high overshoot due to the extremely small dt at high switching frequencies, and must be reduced via decoupling capacitors.

Table 6.2: Parasitic Inductance Extraction

Current Path	**Phase A**	**Phase B**	**Phase C**
LDC+	16.89 nH	33.49 nH	61.8 nH
LDC-	18.89 nH	24.8 nH	34.8 nH
LT3	0.4nH	0.5nH	0.27nH
LT2	0.1 nH	0.1 nH	0.1 nH

6.4.5 Decoupling Capacitors

Decoupling capacitors must be placed close to the device terminals to minimize the commutation loop. This is depicted in Figure 6.14, emphasizing the smaller commutation loop. $L_{decoup1}$ and $L_{decoup2}$ are estimated to be much lower than LDC+ and LDC-.

The method outlined in [29] estimates the value of the decoupling capacitor as shown in 6.1. A maximum multiplier of 2 VDC is used to estimate the surge voltage.

$$C_{decoup} > \frac{L_{trace} \times I_{main}^2}{V d s_{surge}^2 - V_{DC}^2} \tag{6.1}$$

Using the worst case L_{trace} of Phase C, a solution 2.5 nF is found. A 40x multiplier is implemented of 0.1 uF is implemented in the design. Low ESL Ceralink capacitors are used. The implementation on board is shown in 6.15. As many capacitors as feasible are placed in

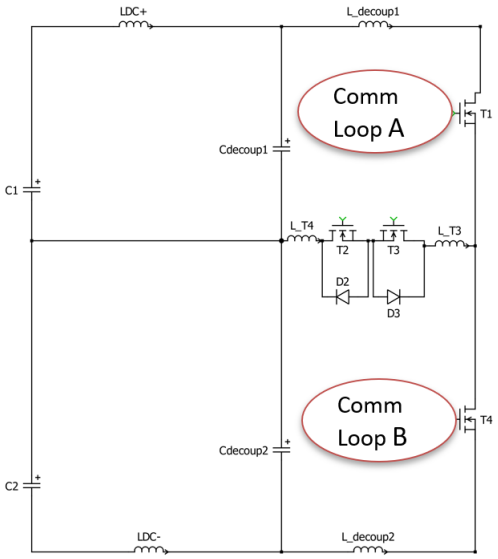


Figure 6.14: Decoupling Capacitor Placement

parallel to minimize the ESL. The circle indicates the revised commutation loop for positive and negative voltage commutation whereas the white boxes represent the location of the capacitors.

Table 6.3: Parasitic Inductance Extraction with Decoupling Capacitors

Current Path	Phase A	Phase B	Phase C
Comm Loop A	3.48 nH	3.6 nH	3.41 nH
Comm Loop B	5.5 nH	5.36 nH	5.4 nH

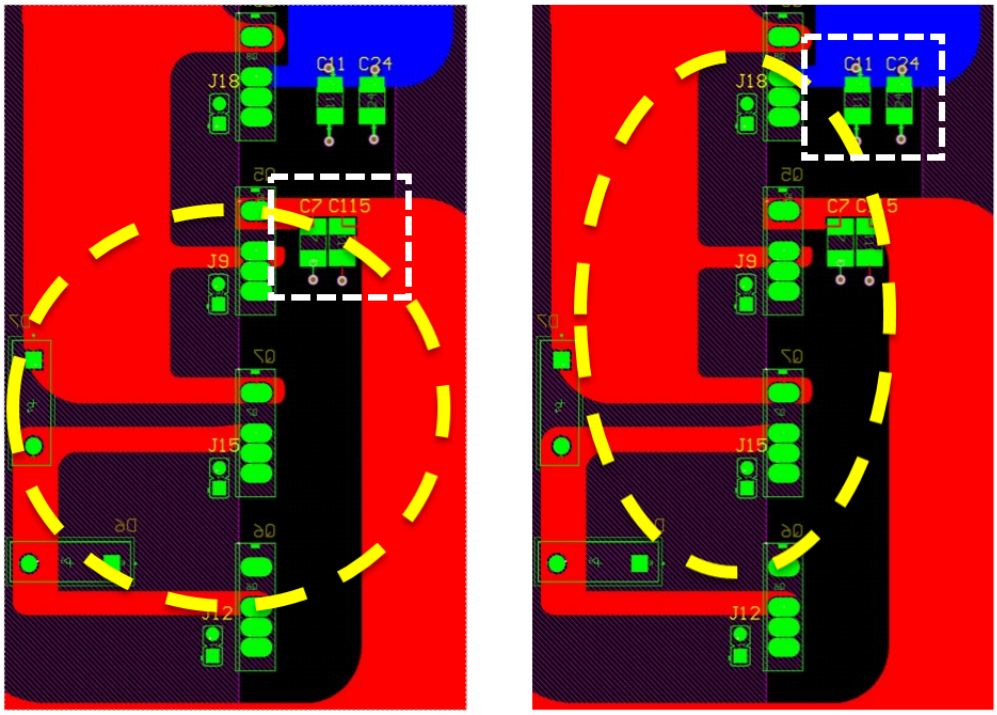


Figure 6.15: Decoupling Capacitor Placement on Board

Lastly, the revised commutation loop is simulated in Q3D. The results are as shown in Table 6.3, indicating significantly lower parasitic inductances.

The analysis presented outlines an analytical and simulation hybrid approach in determining the size of the decoupling capacitors. These values would likely need to be re-tuned in experimental verification to find the optimal solution.

CHAPTER

7

RESULTS & CONCLUSION

The final chapter of this work will showcase a CAD model of the system and discuss the expected system performance versus the initial targets.

7.1 CAD Model

A SolidWorks model of the complete system is shown in 7.1. The top side of the board is open for vertical integration of the gate driver and control circuitry and maximize power density.

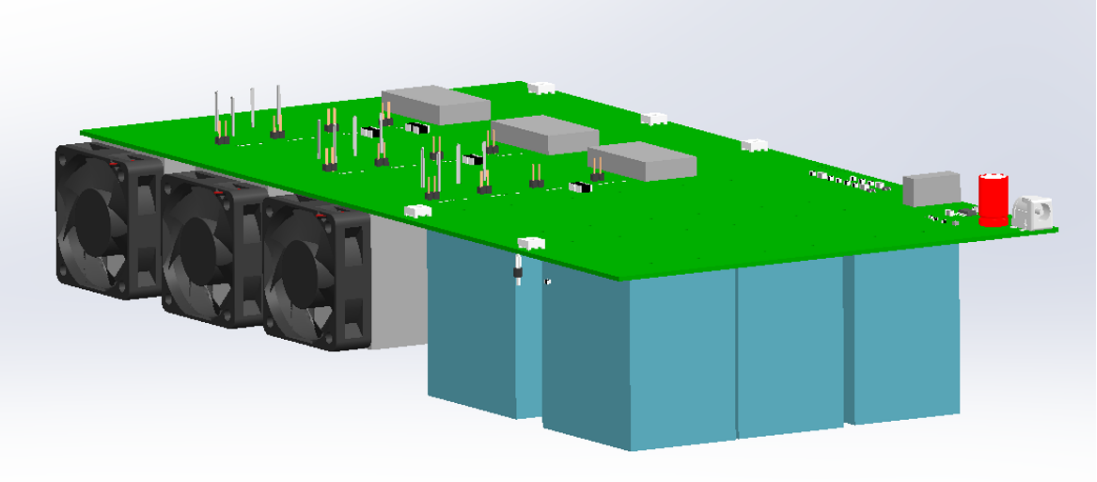


Figure 7.1: Final System

7.2 Expected Performance

The volume of the CAD model is estimated as 4.25L equating to a power density of 8.24 kW/L for a 35 kW system. As shown in the thermal model, the estimate efficiency is 97.78%. All high altitude design standards are met. Table 7.1 compares these metrics to the targets.

Table 7.1: Expected Performance

Target	Design Achieved
15kW/L	8.26 kW/L
>98%	97.78 %

7.3 Discussion

7.3.1 Efficiency

The design all but achieves the efficiency target and may even do so in the experimental setup. The following notes are made in this regard:

1. The reason for this is the likely overestimated switching losses in the simulation model, assuming the switching energies for rated voltage whereas the half bridge switches commutate only at half that value. Switching losses are likely to be lower in that case.

2. Efficiency can be further improved with a more advanced modulation scheme such as the Space Vector Modulation scheme regarded as a more efficient option.

7.3.2 Power Density

1. The added MIL-STD standard dramatically increases the required capacitance in the system and may not be required. The current design is extremely conservative with the standard, as it doubles the minimum capacitance value calculated. For instance, if a less conservative approach of 1.3x required value is used, the power density is increased by 4kW/L. This would likely be a useful design iteration once verified in an experimental setting.

2. Forced Air Cooling is limited by the availability of high performing heatsinks and the large volume associated with them. A more advanced liquid cooling approach could dramtically increase the power density as well.

7.4 Conclusion

A detailed design procedure of a 97.78% efficient, 35 kW, all SiC T-Type Converter was presented in this work. A review of the electrification architectures of current and future more electric aircrafts was shown. Additionally, a level playing field comparison between popular 2-level and 3-level carried out, and the benefits of the T-type converter for the application were made clear.

An in-depth loss model of the T-type converter was developed using a PLECS-MATLAB based iterative process to determine the cooling mechanism required in the system, and verified in simulation. Furthermore, common high altitude design standards were taken into consideration while realizing the physical converter in the thermo-electrical domain.

Additional high power density components were chosen and the converter laid out. ANSYS Q3D was used to ensure low parasitic inductances in the system and a simulation - analytical model shown to determine the size of decoupling capacitors. The benefit of adding them was then presented as well. Finally, an 8.26 kW/L design was shown in CAD and a discussion on further improving the design was conveyed.

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