ABSTRACT

KHACHARIYA, DOLAR. A Path Towards GaN-based Vertical Superjunction Devices. (Under the direction of Dr. Spyridon Pavlidis.)

GaN devices offer exciting competition to incumbent technologies for high-power electronic devices. The wide bandgap of GaN enables it to achieve higher breakdown voltages and reduced on-resistance compared to traditional Si in unipolar devices, as predicted by the classical Baliga figure of merit (BFOM). Further performance gains can be obtained by using the superjunction (SJ). While this has been demonstrated experimentally in both Si and SiC technology, there are no experimental demonstrations of GaN-based vertical SJ devices in the literature. This stems from one major limitation: selective area doping. In response, this dissertation investigates two approaches for selective area doping to obtain vertical SJ devices in GaN technology: lateral polar junctions and ion implantation.

In the lateral polar junction approach, selective area doping is achieved using polarity control during the epi-growth of GaN. N-polar GaN readily incorporates oxygen, a shallow donor, making it the choice for the n-type column. Thus, while Mg present during GaN growth renders Ga-polar domains p-type, the N-polar domains remain n-type. Since N-polar GaN pillars will carry current, it is necessary to understand how doping and barrier heights influence performance. However, there are presently few reports that experimentally investigate the electronic properties of N-polar GaN relevant to SJ design. Therefore, the thesis presents the design, fabrication, and analysis of Schottky, p-n, and camel diodes formed on bulk N-polar GaN to assess the ability of GaN SJ devices to be formed with LPJs.

The study of Schottky diodes with N-polar GaN revealed three major insights: (1) the barrier height on a pristine surface is 0.4 eV, which is low and increases leakage current under reverse bias, (2) the heightened chemical sensitivity of N-polar GaN compared to Ga-polar

GaN complicates processing and reduces thermal stability and (3) oxygen incorporation can be controlled to achieve n-type doping in the 10^{17} cm^{-3} range, which is necessary for kV-class SJ drift regions. Two different solutions are presented to increase the barrier height. Firstly, a 5 nm thin SiN interlayer is introduced between the metal and n-type layer, which increased the barrier to 0.8 eV, reduced the leakage to 4 orders, and increased temperature operation to 400 °C. The second is a camel diode where a thin and fully ionized p^+ layer was grown on the n-type layer, and its thickness and doping determine the barrier height. However, p-type doping in N-polar GaN is a nascent technology so p-n diodes were studied first to investigate Mg incorporation and the role of background oxygen level. Following this study, N-polar GaN camel diodes are demonstrated with a threshold voltage of ∼1 V, or 0.6 V larger than in Schottky diodes. Using all this knowledge, an LPJ structure is grown with a camel junction. The extracted threshold voltage was 1.15 V, and the net doping level was $\sim 10^{17}$ cm^{-3}. Material and electrical analysis confirm charge balance between Ga- and N-polar domains, which is the first demonstration in GaN technology and serves as a path towards obtaining vertical GaN SJs.

Selective area p-type doping can also be realized using Mg ion implantation. To date, reliable implantation activation was a bottleneck to achieve practical p-type doping in GaN. A new annealing technique using ultra-high pressure has achieved the most efficient electrical activation to date. GaN-on-GaN p-n diodes are manufactured with this approach. A breakdown voltage of 1 kV breakdown voltage with a maximum field in the device 3.36 MV/cm is achieved, which are the highest reported values in the literature so far.

Thus, this thesis aims to explore these two selective area doping control techniques for GaN and make them viable for future high-performance GaN SJ developments.

A Path Towards GaN-based Vertical Superjunction Devices

by
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DEDICATION

To my parents and my fiancée Jainul Patel

BIOGRAPHY

Dolar Khachariya was born in Jetpur, Gujarat, India. He earned his Bachelor of Technology in Electronics and Communications from U. V. Patel College of Engineering in 2011 and Master of Technology in Microelectronics from IIT Bombay in 2015. He joined North Carolina State University in August 2017 and started pursuing his PhD in May 2018. During his time as a graduate student, he developed expertise in the design, simulation, fabrication, and characterization of III-nitride devices.

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Chapter 1

Introduction

Power electronics are an essential part of many modern-day electronic systems, including but not limited to renewable/non-renewable energy generation-storage-transmission, power grids, industrial motor drives, electric cars and trains, home appliances, and day-to-day electronics as shown in Fig. 1.1. At the center of any power electronic system are power switches whose primary function is to efficiently convert power. Since a considerable amount of the power losses occurs at these power switches, their evolution has played a vital role in achieving compact and energy-efficient power systems.

In the early 1900s, power devices used for power conversion were mainly mercury arc rectifiers (Peter Cooper Hewit, 1902), triodes (Lee De Forest, 1906), controlled grid high vacuum tube rectifiers (Lee De Forest, 1906), metal tank rectifiers (Errol Shand, 1925), and ignitrons (Joseph Slepian, 1930s) [1]. The first electronic revolution started with the invention of the silicon transistor at Bell Laboratories in 1948. Soon after, power electronic systems emerged with silicon bipolar devices, such as bipolar power transistors and thyristors. However, with growing demand and increasing power ratings, power systems became bulky and costly. In the 1970s, the development of metal-oxide-semiconductor (MOS) technology offered a solution for low power with high-frequency applications. However, for high-power applications, bipolar devices were still indispensable. The second electronic revolution happened after the invention of the insulated gate bipolar transistor (IGBT) by Baliga at General Electric in the 1980s, which revolutionized the power device market [2, 3]. These IGBTs became ubiquitous in most power electronic systems and improved efficiency while providing the

economic benefits of reduced energy consumption. This reduction in energy consumption has been found to eliminate the emission of over 100 trillion pounds of carbon dioxide, mitigating its impact on global warming [4]. Since then, many other advanced rectifiers and transistors were realized [5–7]. Nonetheless, the search for novel devices and semiconductor materials to enhance the performance of power electronics continues today, with the hope of yielding further economic gains and reducing the impact on our environment.

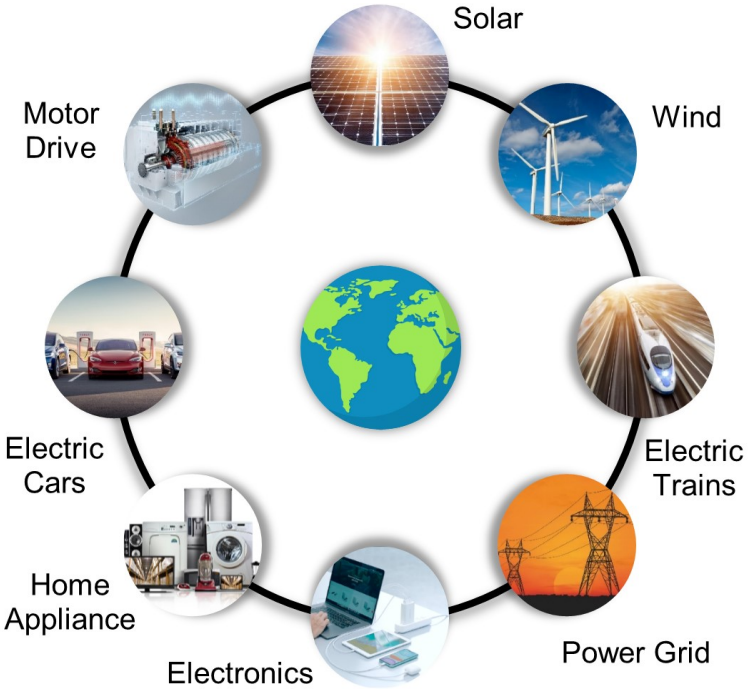

Figure 1.1: Application space of power semiconductor devices.

1.1 Introduction to Superjunction Power Devices

1.1.1 Conventional Unipolar Power Devices

The primary purpose of a power device is to block the applied voltage in the OFF state while having the lowest resistance in the ON state. However, there is a tradeoff between the breakdown voltage (BV) of the device and its specific on-resistance (R_{ON}). The relationship between BV and R_{ON} for unipolar power devices, such as Schottky diodes and metal-oxide-semiconductor field-effect transistors (MOSFETs), is derived here. The schematic cross-section of a typical n-type drift region in a conventional unipolar power device and the electric field across the drift region at the onset of breakdown is shown in Fig. 1.2. The on-resistance of this n-type drift region can be derived as:

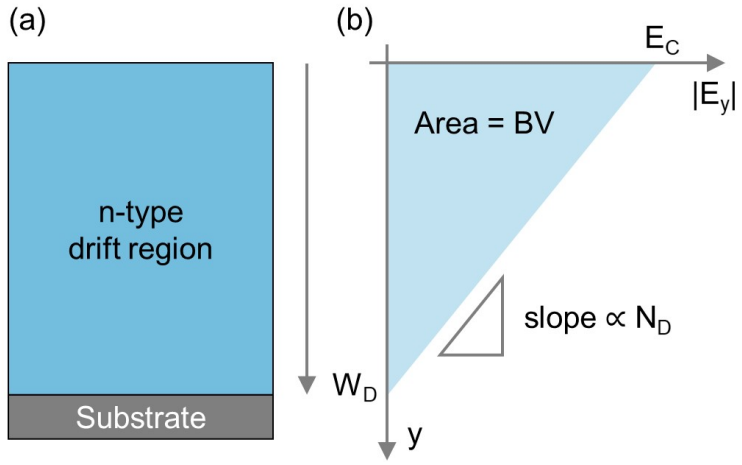

Figure 1.2: (a) The cross-sectional view of a typical n-type drift region in a conventional unipolar power device. (b) The electric field distribution along the drift region at the onset of breakdown. Here, E_C is the critical electric field of the material, while N_D and W_D are the doping and thickness of the n-type drift region, respectively.

$$R_{ON} = \frac{W_D}{q\mu_n N_D} \tag{1.1}$$

where, q is the charge, μ_{n} is the electron mobility in the drift region, $\mathrm{W_D}$ is the thickness of the drift region, and $\mathrm{N_D}$ is the doping density in the drift region. The relationships between the electric field, doping, and drift region thickness are given as follows:

$$W_D = \sqrt{\frac{2\varepsilon_S BV}{qN_D}} \tag{1.2}$$

and,

$$E_C = \sqrt{\frac{2qN_D BV}{\varepsilon_S}} \tag{1.3}$$

where, ε_S is the dielectric permittivity, and $\mathrm{E_C}$ is the critical electric field of the semiconductor material. Using Eqs. 1.1, 1.2, and 1.3, the relationship between the on-resistance and the breakdown voltage can be obtained as:

$$R_{ON} = \frac{4BV^2}{\varepsilon_S \mu_n E_C^3} \tag{1.4}$$

The denominator of Eq. 1.4 is known as the Baliga Figure of Merit (BFOM) for unipolar power devices:

$$BFOM = \varepsilon_S \mu_n E_C^3 \tag{1.5}$$

The BFOM offers a method to quantitatively evaluate the impact of a semiconductor's material properties on a unipolar power device's performance [8]. The relationship between the breakdown voltage and critical electrical field for unipolar devices (for non-punch-through case) can also be written as:

$$R_{ON} = \frac{4BV^2}{\varepsilon_S \mu_n E_C^3} \tag{1.6}$$

Using all the equations from Eq. 1.1 to Eq. 1.6, the relationship between R_{ON} and BV, derived from one-dimensional (1D) electric field analysis, is:

$$R_{ON} \propto BV^{2.5} \tag{1.7}$$

which is the theoretical limit for any conventional unipolar device with a 1D electric field. Thus, the higher the BV capability of the device, the higher the R_{ON} because the device would have a thicker drift region with lower doping.

As mentioned earlier, since the second half of the 20th century, Si has been heavily used in power devices due to its natural abundance and economic viability. However, wide bandgap materials such as SiC and GaN [9, 10], as well as ultra-wide bandgap materials such as Ga_2O_3, diamond, and AlN [11], have recently gained much attention due to their larger bandgaps, higher breakdown field strengths, and higher electron saturation velocities compared to Si. The BFOM of GaN has been found to be approximately 4000 times higher than Si and 6 times higher than SiC [12]. This higher BFOM for GaN makes it possible to realize devices that have a smaller on-resistance (R_{ON}), are smaller in area, and possess the capability to work at a higher frequency for a similar breakdown capability compared to Si. Figure 1.3 compares on-resistance versus the breakdown voltage for Si, SiC, and GaN unipolar devices such as Schottky diodes and MOSFETs. The graph is generated using the relationship between R_{ON} and BV reported by Baliga in [10]. Also, the dependence of mobility on doping concentrations is accounted for in the calculation. From Fig. 1.3, it is evident that GaN-based unipolar devices would have lower on-resistance than Si- and SiC-based devices. In practice, Si-based power device technology has already reached its 1D unipolar

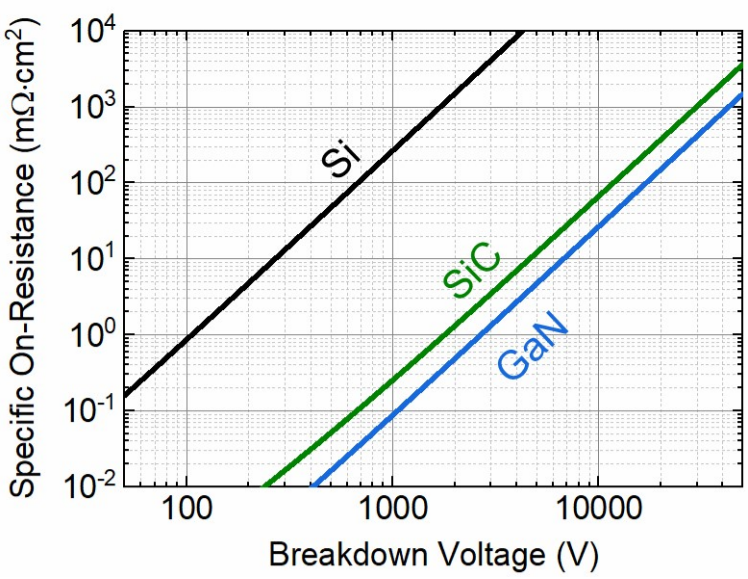

Figure 1.3: (a) Theoretical limit of specific on-resistance (R_{ON}) versus breakdown voltage comparison for conventional Si, SiC, and GaN unipolar devices.

theoretical limit, while SiC-based power devices are approaching their theoretical limit [13,14]. In comparison, GaN-based power devices are showing consistent progress towards, but still far from, their 1D theoretical limit [15–17].

1.1.2 History and Concept of Superjunction Devices

The aforementioned theoretical limit [see Eq. 1.7] for unipolar devices was considered unbreakable for about 30 years until the demonstration of Si-based RESURF (Reduced SURface Field) devices [18]. In this RESURF device, the surface electric field was reduced by creating a two-dimensional (2D) profile for the electric field, which increased the BV capability of the device. Subsequent theoretical and experimental reports on this new device concept were published in which the device was alternatively referred to as a superjunction (SJ) [19], CoolMOS [20], MDmesh [21], and charge-coupled or charge-balanced device. Compared to conventional power devices, the main difference is that the drift region of this new device is

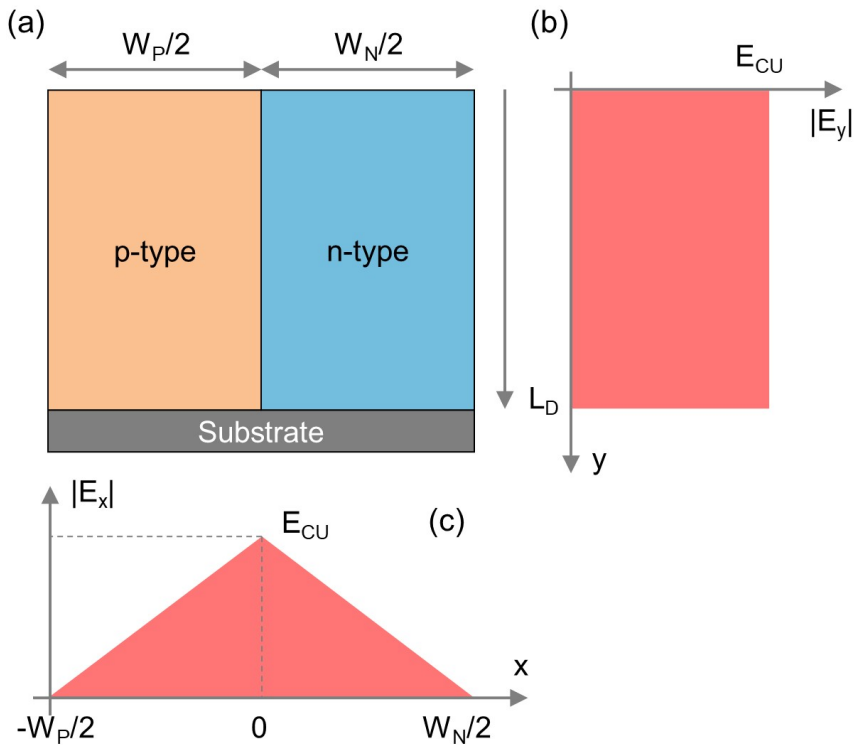

Figure 1.4: (a) The cross-sectional view of a typical unit cell of a superjunction power device. The electric field distribution along the (b) y-direction obtained at x=-$W_P/2$=$W_N/2$ and (c) x-direction obtained at the middle of the drift region, y=$L_D/2$, at the onset of breakdown. Here, E_{CU} is the uniform critical electric field, W_N and W_P are the widths of the p- and n-type column of the drift region, respectively.

realized using either horizontally aligned or vertically stacked alternating p-type and n-type doped columns/pillars, which helps to create a 2D electric field by balancing the charges inside the drift region.

The schematic cross-section of the drift region in the SJ structure made of p- and n-type columns is shown in Fig. 1.4(a). The lateral depletion region forms between the p- and n-type columns when a reverse bias is applied to the structure, which creates an electric field in the x-direction, as shown in Fig. 1.4(c). By increasing the reverse bias voltage, the depletion in the lateral direction increases and, with it, the electric field. To achieve better charge coupling, both columns should be totally depleted before the applied reverse bias reaches

the breakdown voltage. Thus, when the reverse bias reaches the breakdown voltage, the electric field in the y-direction of the structure would be uniform, defined as the uniform critical electric field (E_{CU}) in p- and n-type columns, as shown in Fig. 1.4(b). Therefore, by comparing Figs. 1.3(b) and 1.4(b), SJ devices can have a larger breakdown capability for similar-sized drift regions than conventional power devices. In addition, because of the decoupling of drift region thickness and doping in each column, SJ devices can provide a smaller on-resistance as the doping can be controlled via the width of p- and n-type columns. Thus, a vertical superjunction structure could break the conventional unipolar theoretical limit. Further details on the theoretical modeling and simulations of the SJ devices and their comparison to conventional unipolar devices are presented in Chapter 2.

1.1.3 Development of Superjunctions in Si and SiC

The fabrication process flow for SJ devices is not trivial as it requires horizontally or vertically aligned p- and n-type columns. The two main techniques to achieve a SJ are multiepitaxy with ion-implantation and trench etching with side-wall regrowth [22, 23]. In the multiepitaxy technique, subsequent masked implantation and epi-growth are performed to achieve desired thickness and doping in p- and n-type columns. In contrast, deep trenches are formed in trench technology, and then regrowth is done to fill those trenches. The fabrication process flow for multiepitaxy and trench techniques is shown in Figs. 1.5(a) and 1.5(b), respectively. The key advantage of the multiepitaxy technique is that the doping levels of p- and n-type columns can be controlled in each epitaxy layer. This doping control would also provide the benefits of achieving the desired doping in edge termination layers. The advantage of the trench technique is that the interface between both the columns would be smooth compared to multiepitaxy devices, where the chain of spheres would be created due to the diffusion of the implanted species. The cross-sectional SEM images of 600 V rated Si-based SJ MOSFETs

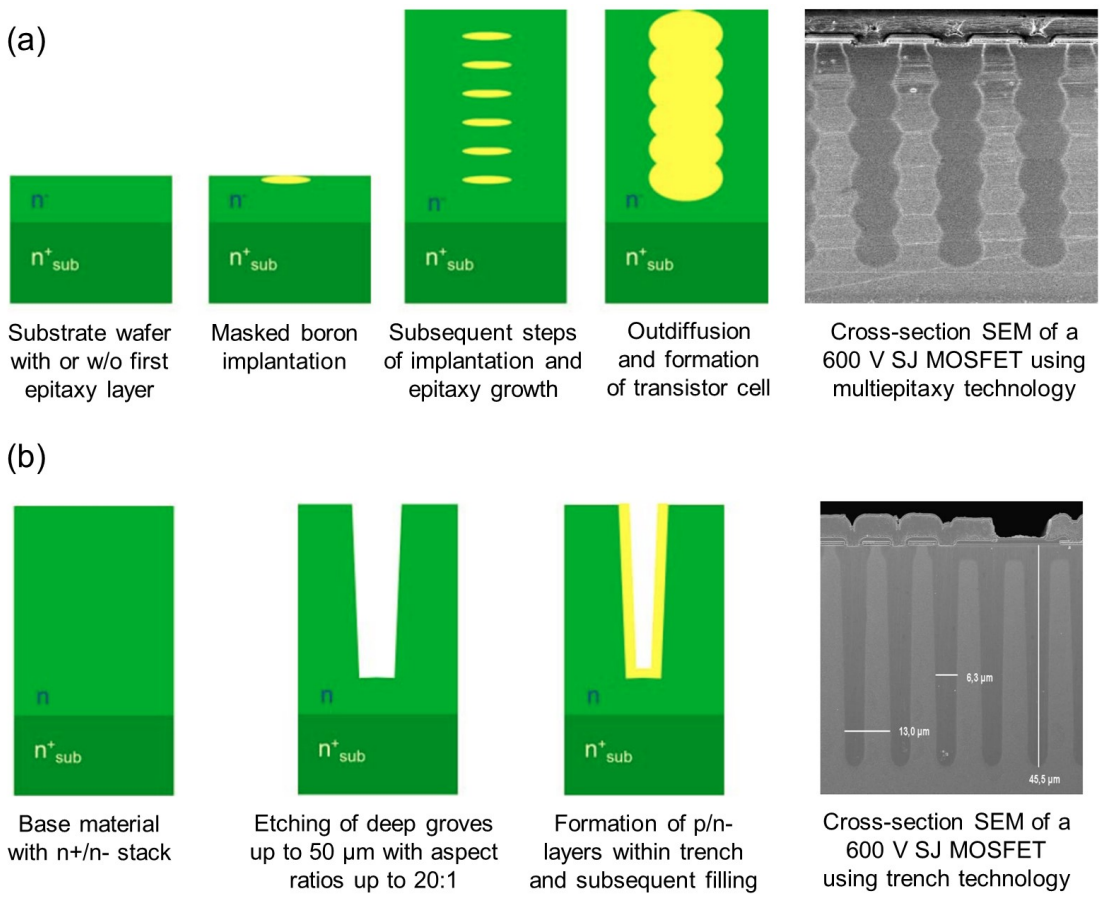

Figure 1.5: The fabrication process flow of superjunctions using (a) multiepitaxy with ion-implantations and (b) trench etching with regrowth on side-wall. The cross-section SEM images are also shown for both techniques. Figure from [22].

fabricated using both techniques are also shown in Fig. 1.5.

To date, many Si-based SJ devices for commercial products can be found in the marketplace, and numerous publications in the literature are available [22, 24, 25]. The comparison of R_{ON} vs. BV for different SJ devices using both fabrication techniques mentioned above against the Si unipolar limit is shown in Fig. 1.6. The graph shows that the SJ devices indeed cross the theoretical limit of conventional unipolar devices. In recent years, experimental work on SiC-based SJ devices is also reported in the literature [26–29]. In both materials, SJ devices have outperformed their conventional counterparts, thus increasing competition among technologies.

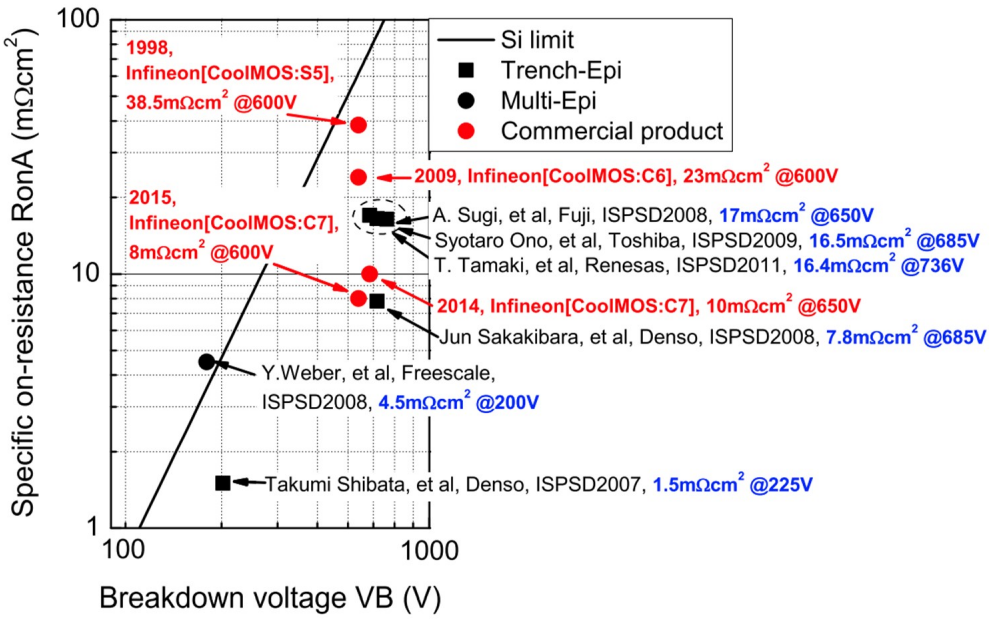

Figure 1.6: Specific on-resistance (R_{ON}) versus breakdown voltage comparison for different superjunction devices fabricated using multiepitaxy and trench technology and compared against conventional Si unipolar devices limit. Figure from [22].

1.2 GaN-based Superjunction Devices and Challenges

As shown in Fig. 1.3, conventional GaN-based power devices offer low on-resistance for a given breakdown voltage application compared to Si and SiC conventional devices. Similarly, developments of superjunctions in GaN technology would potentially achieve superior performance over their conventional devices as well as Si- and SiC-based SJ devices. However, a vertical GaN SJ device capable of competing with Si and SiC SJ devices has yet to be reported since selective area doping control using ion implantation and etch/regrowth remains challenging. Instead of relying on these fabrication techniques to obtain selective area doping, the polar nature of GaN presents a unique opportunity to create superjunctions differently.

Currently, several experimental demonstrations of lateral GaN-based Polarization superjunction (PSJ) devices have been reported in the literature [30–32]. A polarization superjunction concept relies on the charge compensation of positive and negative polarization

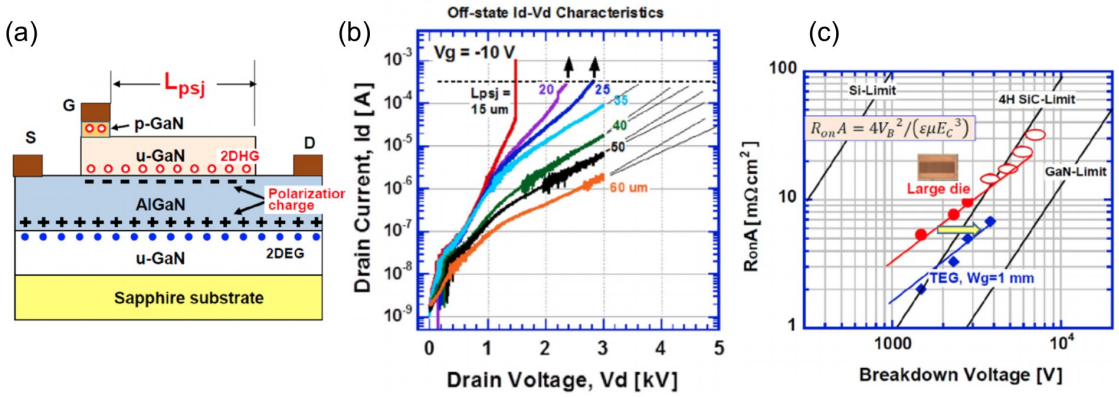

Figure 1.7: (a) Schematic cross-section of lateral GaN Polarization superjunction (PSJ) FET. (b) The off-state characteristics of PSJ-FET with various PSJ lengths (LPSJ). (c) Specific on-resistance (R_{ON}) vs. breakdown voltage of fabricated PSJ-FETs on sapphire. Figure from [30].

charges at heterointerfaces of a GaN/AlGaN/GaN heterostructure [33]. The schematic cross-section of such type of structure is shown in Fig. 1.7(a). In this heterostructure, all the layers remain free of impurity doping. For FET applications, in forward bias, current flow happens through a two-dimensional electron gas (2DEG), whereas in reverse bias, the charge balance is achieved via the positive and negative polarization charges. In 2017, Kawai *et al.* reported the performance of large area die PSJ-FETs with different lengths of the PSJ region (LPSJ) [30]. The off-state characteristics of PSJ-FETs with various LPSJ are shown in Fig. 1.7(b). The setup used to measure breakdown characteristics in their work was limited to 3 kV. Thus, the breakdown voltage had to be predicted carefully for larger LPSJ devices, as seen in Fig. 1.7(b). The on-resistance (R_{ON}) versus breakdown voltage is shown in Fig. 1.7(c). In the graph, the red circles are large area devices with different LPSJ, the empty red ellipses are the extrapolated values from Fig. 1.7(b), and the blue circles are the small test structure devices. Although the breakdown voltage increases linearly with the distance LPSJ, the current performance of the devices does not exceed the GaN unipolar 1D limit. In 2017, Unni and Narayanan reported the simulation analysis of the same PSJ concept for vertical GaN technologies [34]. However, they did not provide detailed fabrication mechanisms to achieve

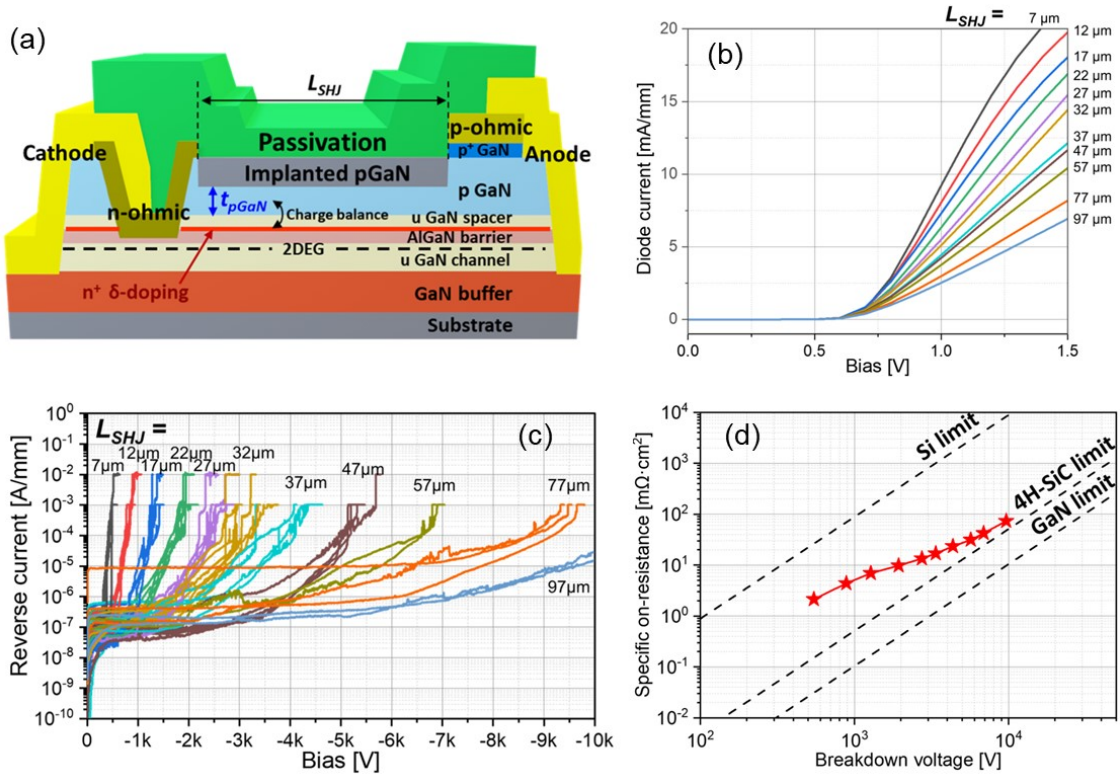

Figure 1.8: (a) Schematic cross-section of lateral GaN super-heterojunction Schottky barrier diode (SHJ-SBD). (b) The forward and (c) reverse bias I-V characteristics of SHJ-SBD with various LSHJ spacings. (d) Specific on-resistance (R_{ON}) vs. breakdown voltage of fabricated SHJ-SBD. Figure from [35].

these vertically aligned alternating GaN and AlGaN columns on a substrate.

Han *et al.* recently reported lateral GaN-based super-heterojunction (SHJ) Schottky barrier diodes (SBD) with breakdown capability over 10 kV [35]. The schematic cross-section of SHJ-SBD is shown in Fig. 1.8(a). Compared to PSJ devices, the charge balance in SHJ devices is obtained between n-type delta doping at the upper GaN/AlGaN interface and negative charge from ionized p-type dopants in p-GaN on top. The forward and reverse current-voltage characteristics of SHJ-SBD with the different anode to cathode spacing (LSHJ) are shown in Figs. 1.8(b) and 1.8(c), respectively. These graphs show that with increasing LSHJ, on-resistance increases, and so does the breakdown voltage. Figure 1.8(d) benchmarks

the R_{ON} vs. BV for all spacings. Again, with LSHJ spacing, BV increases linearly; however, the performance of the SHJ devices is still below GaN unipolar 1D limit.

It should be noted that the GaN-based experimental superjunction devices are lateral devices and not vertical. To achieve vertical GaN SJs, there are several research barriers to address concerning selective area doping. As mentioned before, SJ devices basically require alternating p- and n-type doping regions with zero net charges. Two approaches are considered in this thesis to address this challenge: polarity control and ion implantation.

The first approach to realize the lateral p/n doped regions is by polarity control, which is unique to III-nitrides. The inherent polar doping selectivity of GaN can be used to achieve the doping scheme for a lateral GaN p/n junction. Oxygen, which unintentionally incorporates into N-polar GaN at levels $>10^{19}$ cm^{-3}, acts as the n-type dopant, whereas Ga-polar GaN does not readily incorporate oxygen. Accordingly, lateral polarity junctions (LPJs) with alternating domains of O-doped N-polar and Mg-doped Ga-polar GaN can be fabricated to realize lateral p/n junctions. In addition to this lateral patterning, the proper doping profiles must be attained in the N- and Ga-polar domains for SJ operation. To achieve a breakdown voltage greater than 1 kV, the n-type doping in the drift region's N-polar domain (and p-type doping in the Ga-polar domain) must be reduced to 10^{17} cm^{-3} for typical micron-wide domains. By implementing the chemical potential control (CPC) framework [36, 37], MOCVD process conditions could be designed in order to decrease the oxygen concentration by increasing the growth supersaturation. This would lead to a reduction in oxygen from $>10^{19}$ cm^{-3} to low 10^{17} cm^{-3}. As this method makes it possible to grow both p- and n-type domains together in a single growth run, thick drift regions can be realized without any issues related to regrowth requirements or lithographic misalignments errors for regrowth. The introduction and detailed discussion on polarity control is presented in Section 1.3.

The second approach is ion implantation, which is one of the basic tools for semiconductor

device fabrication, and as such, any mature semiconductor system should be capable of being processed in this form. Currently, GaN does not possess a robust ion implantation toolbox that allows for reliable implantation control and activation. Nonetheless, recent advances in the realization of p-type GaN via Mg ion implantation and high-temperature and ultra-high-pressure post-implantation annealing techniques have opened a path to achieve SJ devices in GaN. The introduction of p-type doping via Mg ion implantation and novel annealing techniques are presented in Section 1.4.

1.3 GaN-based Lateral Polar Junctions

GaN is a polar material, and it can be grown in two different polar orientations, gallium-polar and nitrogen-polar. The partial unit cell of the wurtzite GaN crystal structure with Ga- and N-polar orientation is shown in Fig. 1.9. Ga-polar GaN is defined in the $+c$ direction (0001),

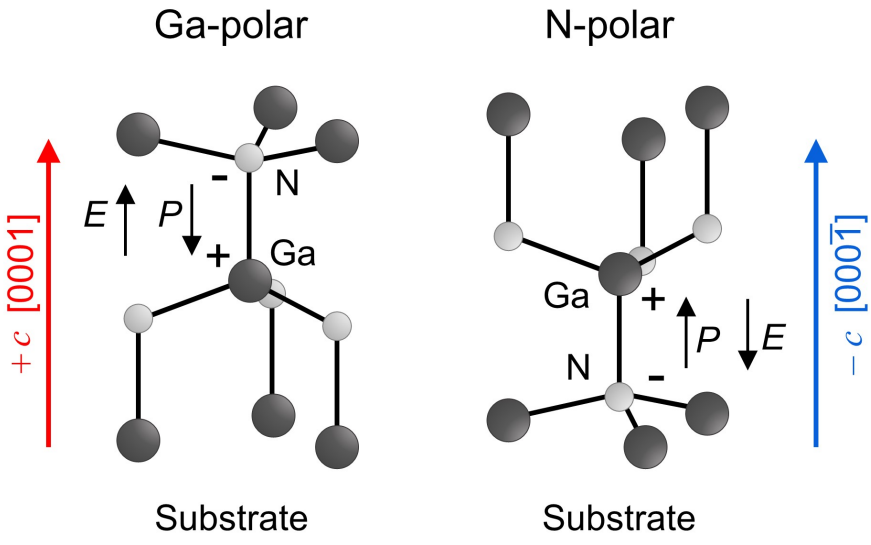

Figure 1.9: Schematic of the wurtzite GaN crystal structure with Ga-polar ($+c$ axis) and N-polar ($-c$ axis) orientations. Here, P denotes spontaneous polarization charge, and E denotes electric field.

whereas N-polar GaN is in the $-c$ direction $(000\bar{1})$ of the lattice, as indicated by arrows in Fig. 1.9. These two polarities along the c-axis should not be confused with the surface termination as each polar orientation may be terminated with either one of the species [38]. Due to the non-centrosymmetric (i.e., lack of inversion symmetry) arrangement of the hexagonal unit cell, a charge dipole is created between Ga and N atoms, which induces an electric field along the c-direction of the crystal. Figure 1.9 shows the direction of the electric field and spontaneous polarization charge for both polarities. It should be noted that the directions of the electric field and polarization charge are opposite in N-polar GaN than in Ga-polar GaN.

1.3.1 Historical Perspective on Polarity Control

Since the beginning, due to the lack of GaN substrate availability, both Ga- and N- polar GaN films have been grown heteroepitaxially on c-plane sapphire or SiC substrates by different growth techniques such as metalorganic chemical vapor deposition (MOCVD), hydride vapor phase epitaxy (HVPE), pulsed laser deposition (PLD), and molecular beam epitaxy (MBE) [39–47]. There are few reports on controlling the polarity of GaN by using Si-face or C-face of SiC substrates [41, 43, 44]. In contrast, the polarity control was found to be complicated when films were grown on the sapphire substrate due to its non-polar nature. The polarity of the GaN surface during the growth determines not only the impurity and defect incorporation but also the surface morphology of the films, which impacts the device performance [45–55]. Typically, Ga-polar GaN films were characterized by a very smooth "mirror-like" surface morphology, whereas N-polar GaN films were rough with a high density of hexagonal facetted hillocks. Early on, it was commonly believed that MOCVD growth resulted in $+c$ polarity (Ga-polar) films due to the N-rich conditions and high substrate temperatures, whereas MBE growth resulted in $-c$ polarity (N-polar) films [46, 47]. However, many researchers have obtained different polarity films using both growth techniques [47].

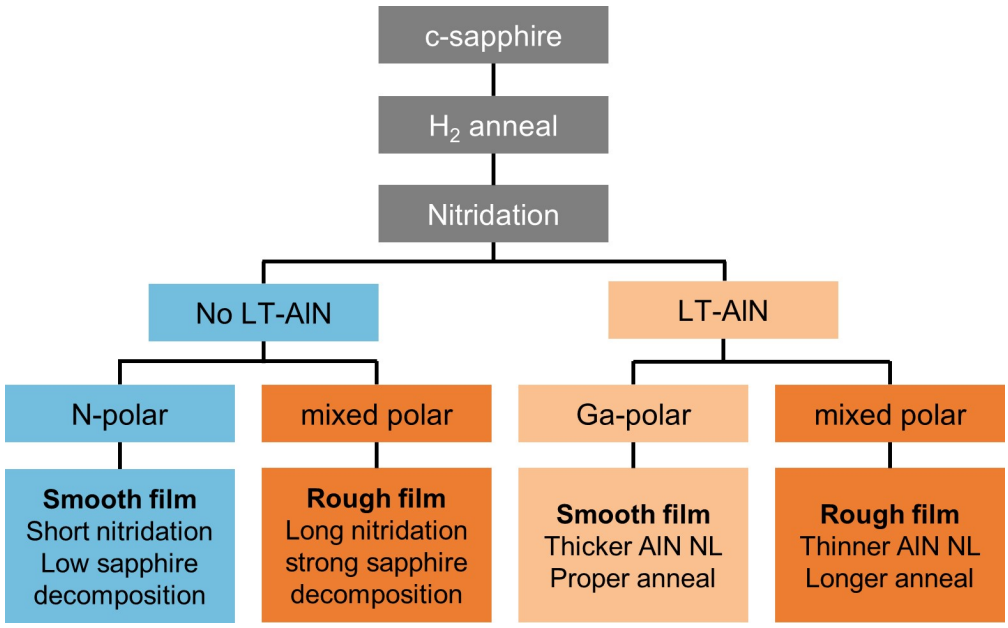

Figure 1.10: The flow chart of the polarity scheme for Ga-polar and N-polar GaN films grown on a *c*-plane sapphire substrate using MOCVD. The figure is adapted from [58].

Stutzmann *et al.* reported that both Ga- and N-polar GaN could be grown using MBE if the film is grown on low temperature (LT) AlN buffer layer and directly on sapphire substrate, respectively [46]. They found that the thickness of the LT-AlN buffer layer also affects the polarity of the grown film. In the case of MOCVD growth, it was also understood that the substrate pre-treatments prior to GaN film growth, such as H_2 anneal and/or nitridation and LT III-nitride buffer layer thickness, have a huge deciding factor on resulting the film polarity and crystalline quality [40, 42, 47, 48, 56, 57]. The detailed flow chart of the GaN polarity control mechanism is shown in Fig. 1.10. The graph is adapted from [58]. The graph depicts the importance of nitridation step and shows how smooth Ga- and N-polar GaN films can be obtained on *c*-plane sapphire substrate.

All these findings on the polarity control scheme provided a pathway to control the GaN film polarity locally on a single substrate, leading to developments of lateral polar junctions (LPJ). In LPJ, Ga- and N-polar GaN domains are grown side-by-side in a single growth

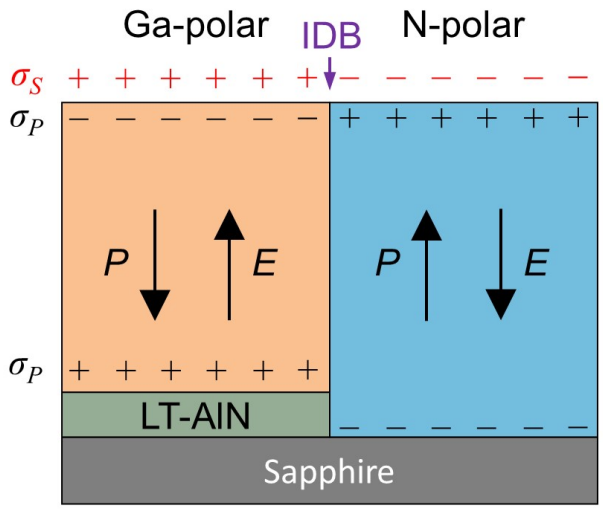

Figure 1.11: Schematic of the GaN lateral polar junction (LPJ) comprising Ga- and N-polar domains. Both domains are separated by an inversion domain boundary (IDB). Here, P is the polarization charge, and E is the electric field. The signs of the resulting net polarization charge (σ_P) and the counter polarization charge (σ_S) on the surface for both domains are also shown.

using a patterned LT-AlN buffer layer on the sapphire substrate. The schematic of GaN LPJ comprising Ga- and N-polar domains is shown in Fig. 1.11. As shown here, in LPJ, Ga-polar GaN is grown on an LT-AlN buffer layer, whereas N-polar GaN is grown on the sapphire substrate after exposure of N precursor at high temperatures (i.e., nitridation) [38, 46, 50, 51, 59–61]. It should also be noted that both Ga- and N-polar domains are separated by an inversion domain boundary (IDB), as shown in Fig. 1.11. The IDB can be very sharp or made up of mix-polar material with a relatively rough surface, and its width could vary up to several nm. In the case of rough, wider, and mix-polar IDB, it could have an adverse effect from a device application standpoint as it could create a charge-imbalance between SJ pillars. So, a sharper IDB is required between the two domains to achieve better device performance. To obtain LPJs, first, the LT-AlN buffer layer is grown, then the sample is patterned using lithography followed by LT-AlN buffer layer removal from open areas via dry etching or wet chemical etching to expose the sapphire substrate. This patterned sample is then loaded into

the MOCVD reactor to grow GaN LPJs. Several other methods to obtain GaN LPJs on a sapphire substrate are also reported in the literature using different buffer layers instead of the LT-AlN layer, such as Al and carbon layer [62–64]. Recently, Hite *et al.* have reported ∼100 μm thick GaN LPJ growth using HVPE on single-crystal GaN substrates using an MOCVD-grown template, which was a major technical breakthrough [65, 66].

Polarity control not only allows to grow Ga- and N-polar domains on the same substrate but also offers selectivity in doping of the structures. Usually, MOCVD-grown N-polar GaN films are n-type due to high unintentional oxygen incorporation ($>10^{19}$ cm^{-3}) that acts as a shallow donor for N-polar GaN [45, 67, 68]. In contrast, Ga-polar GaN films remain undoped (carrier concentration $<10^{16}$ cm^{-3}) if dopants are not introduced during the growth. Therefore, during the LPJ growth, if no dopants are introduced, the Ga-polar domains would remain undoped, whereas the N-polar domains would be n-type. This unique doping selectivity advantage in GaN LPJ enables various novel LPJ-based devices, as has been reported in the literature for electronic and optoelectronic applications. A few of them are summarized in the subsequent section.

1.3.2 Summary of the Devices Realized using LPJs

Aleksov *et al.* reported current-voltage (I-V) characteristics of n/n lateral polarity junctions in 2006 [50]. The schematic structure and the optical image of the GaN LPJ consisting of Ga- and N-polar domains are shown in Figs. 1.12(a) and 1.12(b). In this work, during the growth of LPJs, Si dopants are introduced to dope Ga-polar domains n-type. In comparison, N-polar GaN domains remained n-type due to unintentional oxygen incorporation during the growth. Hall measurements indicated that the doping and mobility in the N-polar GaN domain are around 3×10^{19} cm^{-3} and 100 cm^2/Vs, respectively and in the Ga-polar domains are around 6×10^{19} cm^{-3} and 140 cm^2/Vs, respectively. The I-V characteristic between Ga-

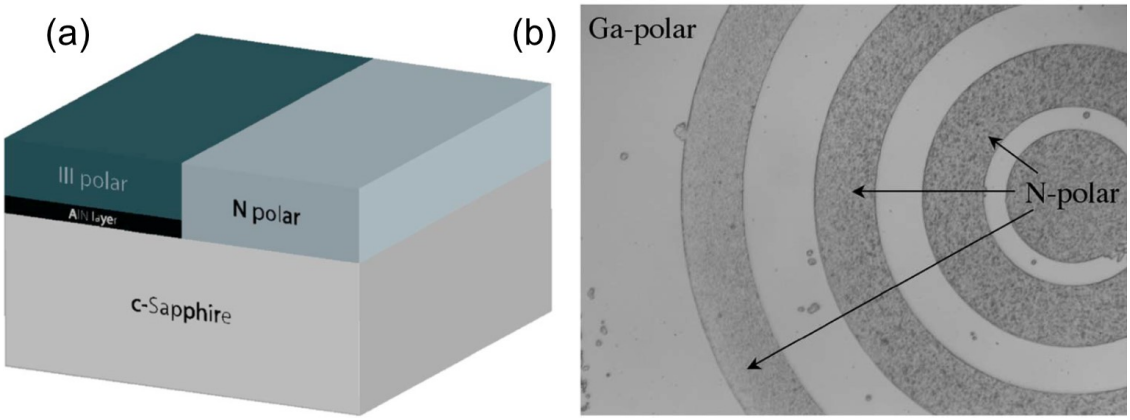

Figure 1.12: (a) Schematic structure of the fabricated lateral n/n junction. (b) Optical microscope image of the GaN LPJ surface consisting of Ga-polar and N-polar domains. Figure from [50].

and N-polar domains is found to be linear, which suggests that there is no energy barrier for the carriers across the IDB of the LPJ. The results in their work led them to conclude that the LPJs can be treated as GaN/GaN homojunction with the electronic properties that are only determined by the bulk properties of the material, such as doping and defect concentrations instead of influence from IDB [50].

Soon after, Collazo *et al.* reported lateral p/n junctions by taking advantage of the polar selective doping in LPJs [51]. Figure 1.13(a) shows the schematic of their fabricated lateral p/n structure on a sapphire substrate. The total thickness of Ga- and N-polar GaN domains are 2.2 μm. During the growth, LPJ is grown to a thickness of 1.5 μm without any intentional doping, followed by 0.7 μm thick with Mg doping. As mentioned earlier, during the LPJ growth, N-polar GaN domains always incorporate unintentional oxygen, making it n-type. In contrast, Ga-polar domains remain undoped to moderately doped (with the oxygen: 10^{16} cm^{-3} to 10^{17} cm^{-3}) depending upon the growth conditions of LPJ. Thus, utilizing the advantage of doping selectivity in LPJ, Collazo *et al.* introduced a controlled amount of magnesium during the LPJ growth, which made Ga-polar domain p-type. In contrast, the N-polar domain also incorporated magnesium, but it still remained as n-type

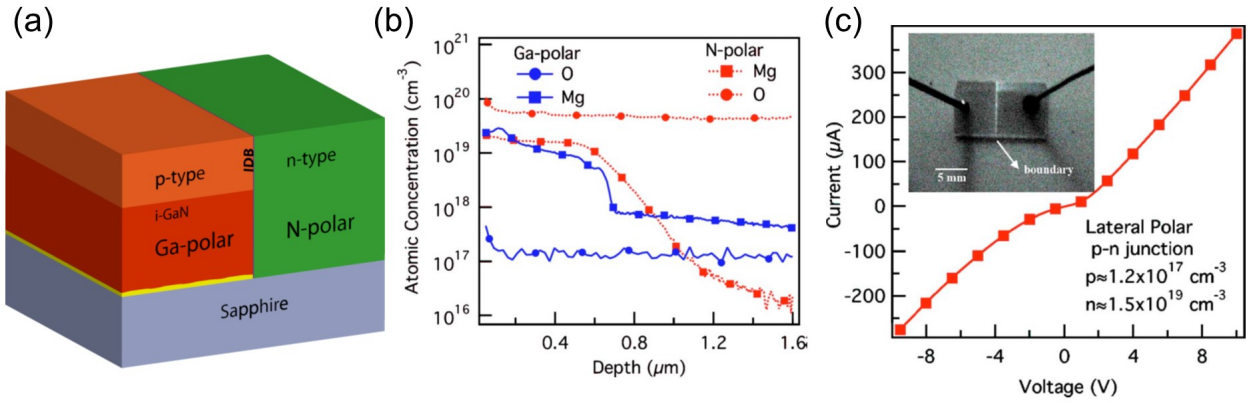

Figure 1.13: (a) Schematic structure of the fabricated lateral p/n junction. The total thickness of Ga- and N-polar domains are 2.2 μm. In the Ga-polar domain, i-GaN is 1.5 μm thick, and the p-type layer is 0.7 μm thick. (b) Secondary ion mass spectroscopy depth profile of oxygen and magnesium on N- and Ga-polar domains for the first 1.6 μm of the total structure. (c) Current-voltage characteristics of the lateral p/n diode. The inset image shows the fabricated device under forward bias operation, demonstrating electroluminescence at the boundary between two domains. Figure from [51].

due to higher background oxygen than magnesium [51]. This is reflected in the secondary ion mass spectroscopy (SIMS) performed on both Ga- and N-polar domains, as shown in Fig. 1.13(b). In Ga- and N-polar domains, oxygen is around 1.7×10^{17} cm^{-3} and 6×10^{19} cm^{-3}, respectively. In comparison, both domains have Mg around 1.7×10^{19} cm^{-3}, which suggests that the net doping in Ga-polar is p-type and N-polar GaN is n-type. For further validation, the hall measurements are reported on both polarity domains. Ga-polar domain showed p-type doping with hole carrier concentrations around 1.1×10^{17} cm^{-3} and mobility around 12 cm^2/Vs. N-polar domain showed n-type doping with electron carrier concentrations around 1.7×10^{19} cm^{-3} and mobility around 99 cm^2/Vs. The I-V characteristics [see Fig. 1.13(c)] of the fabricated lateral p/n diode show rectifying behavior with rectification ratio around 1.5 at ±5 V. The inset image shows electroluminescence under the forward bias operation of the diode. The I-V behavior showed rectification although significant reverse bias leakage is observed which could be due to very high doping in both domains. Also, the LPJ was made

on ∼1 cm^2 substrate with half of the area Ga-polar and other half N-polar GaN, meaning there are only two domains on the whole sample. Thus, it could be possible that higher leakage current could be due to the leakage current paths through the outer sidewalls of the Ga- and N-polar domains in parallel to the actual p/n junction barrier. Indeed, they mentioned that the fabricated structure was not intended to be an optimized device, but a construction to demonstrate possibility of lateral p/n junction based on polar selectivity.

To tackle the challenges in their previous work [51], such as lower rectification ratio and higher reverse leakage current, Collazo *et al.* fabricated a p/n junction using an LPJ approach with 250 μm diameter sized N-polar domains surrounded by Ga-polar domains, as shown in Fig. 1.14(a). This way, the junction boundary would be vertical, which isolates p- and n-type regions. The current flow would be perpendicular to dislocations in the material, so there would be no additional leakage path than from the junction itself. The LPJ growth thickness and the doping levels are identical to their previous work, as shown in Fig. 1.13. The I-V characteristics of the lateral p/n diode in linear and semilog scale are shown in

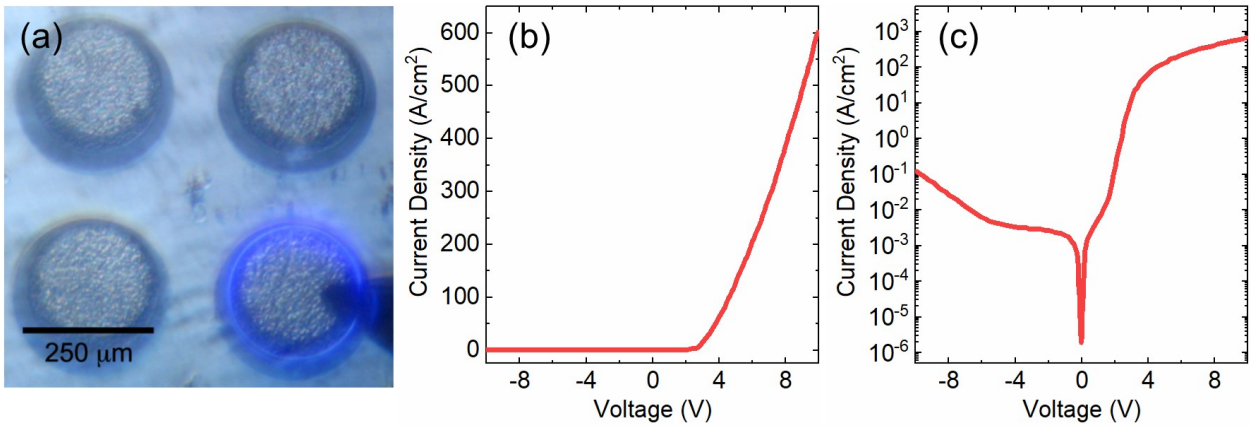

Figure 1.14: (a) Optical micrograph of a lateral p/n diode demonstrating electroluminescence. Current-voltage characteristics of a lateral p/n diode in (b) linear and (b) semilog scale. (Courtesy R. Collazo)

Figs. 1.14(b) and 1.14(c). The current density is calculated by taking the circumference of the diode (785 μm) and the thickness of the p-type region (0.7 μm), corresponding to a diode area of 550 μm^2. From linear I-V, in Fig. 1.14(b), it is seen that the diode turns on at $\sim$3 V and has a current density in the order of a few hundred A/cm^2 in forward bias, which corresponds to differential resistance in the order of m$\Omega\cdot$cm^2. The semilog scale I-V, shown in Fig. 1.14(c), shows the diode has a lower reverse bias leakage with a rectification ratio $\sim$4 orders of magnitude at $\pm$10 V.

In summary, Collazo *et al.* fabricated lateral p/n junctions using a polarity control approach on a sapphire substrate. Indeed, Ga-polar and N-polar GaN domains showed p-type and n-type conductivity, respectively. This successful demonstration of selective p-type and n-type doping in LPJs is the major stepping stone towards realizing a vertical GaN superjunction with controlled doping and charge balance.

Many other exciting devices utilizing LPJ structures are also reported in the literature by taking advantage of selective doping capabilities across the polar domains. Collazo *et al.* reported a depletion-mode metal-semiconductor field-effect transistor (MESFET) with n-type N-polar domains as source & drain and a Ga-polar channel on polarity-patterned wafers [60]. Other electronic device structures such as Schottky diodes [69] and photodiodes [70] are also reported. Recently, Guo *et al.* reported a review on the polarity control and applications of III-nitride LPJs in different devices [71].

1.3.3 Realization of Vertical GaN Superjunction using LPJs

As mentioned in Section 1.2, two main techniques to obtain SJ structures are trench etching/regrowth and ion implantation. They have already been demonstrated to be effective in both Si and SiC technologies. Despite several ongoing efforts to develop similar methods for selective area doping in GaN, these approaches have not been successfully applied to GaN to

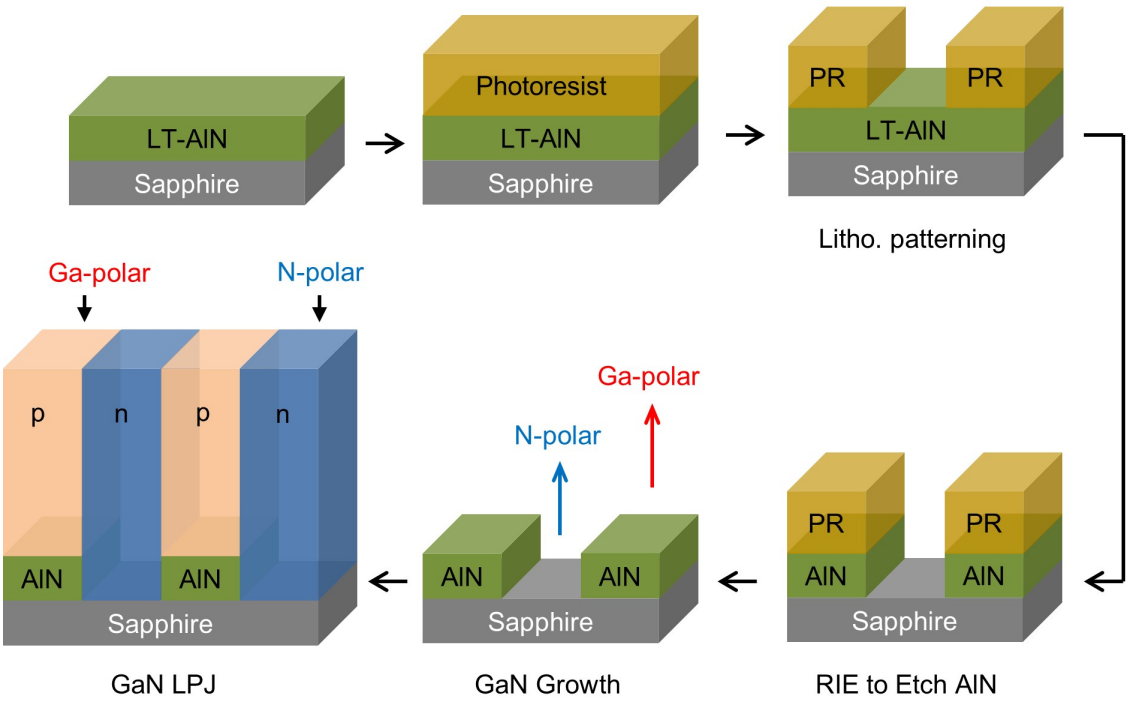

Figure 1.15: Process flow for fabricating GaN SJ structure using later polar junction (LPJ) approach.

realize vertical SJ devices. Therefore, instead of these conventional methods, a novel lateral polar junction approach could be employed to realize vertical GaN SJ devices. As mentioned above in this section, this approach is only available in III-Nitride technology due to the possible polarity control. It provides a promising path towards selective area doping of thick and narrow p/n columns necessary in high-performance vertical GaN SJ devices. The process flow for fabricating GaN SJ structure using LPJ is shown in Fig. 1.15.

Again, the phenomenon that allows for the superjunction is the asymmetry in defect incorporation, as mentioned previously in this section. Specifically, preferential incorporation of shallow donor oxygen occurs in N-polar GaN, making it n-type while Ga-polar GaN remains undoped. In contrast, Mg incorporates similarly into GaN for both polarities. Hence, if Mg is introduced at concentrations below O concentration in N-polar GaN, the Ga-polar domains would become p-type, while the N-polar domains will remain n-type. The process flow shown

in Fig. 1.15 is for the GaN LPJ growth on a sapphire substrate. The primary focus of this thesis is to realize charge balanced (i.e., equal dose in p- and n-type domains) GaN LPJs and demonstrate that epitaxial growth is performed on the sapphire substrates.

As mentioned previously, recently Hite *et al.* have demonstrated two critical technological breakthroughs relevant for the GaN LPJs: (1) thick GaN lateral polar structures exceeding 100 μm by growing them using HVPE on an MOCVD grown template and (2) the possibility of a vertical inversion through a thin oxide interlayer [65, 66, 72]. The first breakthrough helps support the possibility of growing these LPJs to the desired thickness by MOCVD, i.e., there is no fundamental limit to the thickness that could be achieved in the GaN SJ. The second breakthrough suggests the possibility of using native substrates (HVPE GaN templates or ammonothermal single crystals) to realize fully vertical GaN-on-GaN SJ devices.

1.4 Background on p-type doping in GaN via Mg ion-implantation

As mentioned earlier in Section 1.2, ion implantation could be another toolbox to achieve p- and n-type columns for GaN SJ similar to what has been done in Si and SiC technology. N-type regions would be formed during epitaxy, while p-type doping would be achieved via selective-area Mg ion implantation. Several post-annealing techniques have been used to activate the implanted Mg in GaN. This section presents a review on Mg ion implantation and post-activation annealing techniques to obtain selective area p-type doping in GaN.

After ion implantation, the lattice disorder/damage due to the ion bombardments must be repaired, and the impurity atoms must be electrically activated, meaning they must migrate to proper lattice positions. To achieve that, post-implantation anneal is required, which is typically done at higher temperatures. It is an essential step as device performance relies

on the efficiency of post-implantation anneal. A general rule of thumb is that the annealing temperature should be 2/3 of the melting point of the material. In that case, for GaN, the required post-implantation annealing temperature would be ∼1650 °C (based on the melting point of GaN ∼2500 °C [73]) to remove lattice damage. However, GaN decomposes when annealed above 1000 °C due to the loss of nitrogen from the GaN surface [74]. Thus, it is difficult to activate the implanted Mg ions and remove lattice damage in GaN. To address this challenge, several different techniques, such as the use of a capping layer and different annealing instruments, have been reported in the literature.

Different pulsed annealing techniques such as multicycle rapid thermal annealing (MRTA) [75,76], and gyrotron microwave annealing [77] have been reported to perform post-implantation activation annealing. In those techniques, the Mg activation annealing was done at different annealing temperatures ranging from 1000 °C to 1370 °C using a cap layer with N_2 overpressure of 3 MPa (∼30 bar). These techniques have also studied the effect of different cap layers in Mg activation anneal [78]. To demonstrate the capability of selective area doping, junction barrier Schottky (JBS) diodes with 600 V blocking capability have been realized using Mg implantation coupled with MRTA post-implantation anneal technique [79, 80]. Even though these techniques might have avoided GaN surface decomposition, the Mg activation ratios are only ∼0.5 to 8% [75–77]. In addition, removal of the cap layer would also possibly damage the GaN surface, which can affect the ohmic contact formation for p-type GaN. In comparison, electrical activation ratios for B implantation in Si and SiC are reported to be 100% and 95%, respectively [81, 82].

Recently, ultra-high-pressure annealing (UHPA) has also been considered [84–87]. It is performed under high pressure (∼1 GPa or 10^4 bar) with N_2 overpressure, which protects the GaN surface from decomposition. The phase diagram of GaN is shown in Fig. 1.16. The grey shaded area, shown in the graph, is the region where GaN decomposes. To avoid GaN decom-

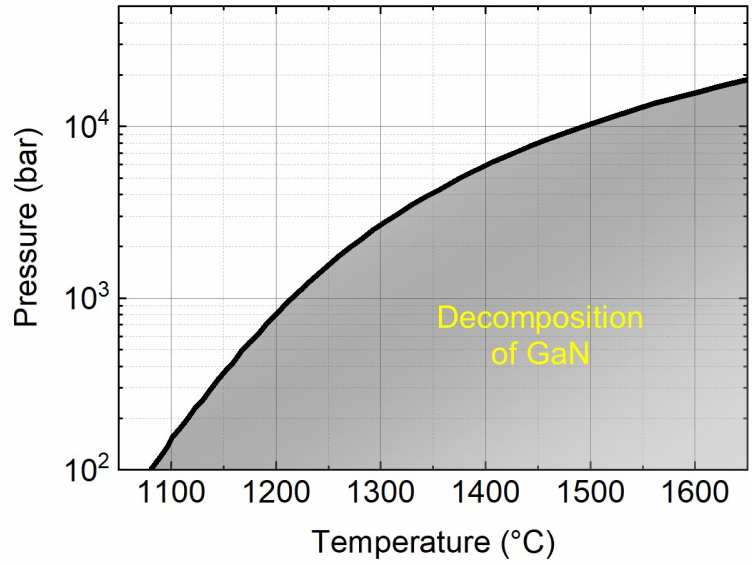

Figure 1.16: The experimental pressure-temperature (p-T) equilibrium curve for the GaN. Adapted from [83].

position at any temperature, the pressure must be higher than the black line shown in Fig. 1.16. These studies have reported Mg activation at different annealing temperatures ranging from 1200 °C to 1500 °C for different periods. It was shown that almost ∼100% activation of the implanted Mg ions was achieved at 1300 °C to 1400 °C using this UHPA technique [84, 87]. The p-type conductivity with high free carrier concentration and mobility comparable to epi-doped p-type GaN was confirmed via hall measurements. Moreover, this technique was used to achieve better edge terminations for epi-doped p-n diodes [88, 89]. However, there are no reports on JBS or p-n diodes using this UHPA technique. In this thesis, GaN p-n diodes are reported to demonstrate that Mg ion implantation and proper activation anneal via UHPA can be used to realize p-type doping in GaN. The successful demonstration of p-type doping via ion implantation would serve as a path to realize the GaN SJ devices in the future.

1.5 Objectives and Scope of the Thesis

The superjunction concept revolutionized the power device market by offering a pathway to reduced losses. In Si and SiC technologies, SJ devices have been experimentally shown to cross their 1D unipolar limit, but this achievement remains elusive for GaN. Thus, it is essential to show similar performance improvement in GaN SJ devices by crossing its 1D theoretical limit. Moreover, there is a need to demonstrate an approach for vertical GaN SJ devices that can compete with Si and SiC, particularly at high voltages.

Therefore, the objective of the thesis is to demonstrate selective area doping control for the realization of GaN-based vertical superjunction diodes using two distinct methods: a novel lateral polar junction approach and ion implantation.

In order to realize GaN SJ devices using lateral polar junctions, the path is divided into several building blocks as follows:

1. A simple theoretical model is developed to obtain material parameters such as p/n columns width and doping and drift layer thickness requirements to achieve kV-class GaN SJ devices.

2. The unintentional oxygen concentration (n-type doping) in N-polar GaN usually results in the order of 10^{19} cm^{-3}. Constant feedback to the material grower was required to achieve required doping control from the perspective of SJ devices. Thus, a study of N-polar GaN material properties is required to estimate the doping levels via Schottky contacts. The properties of N-polar Schottky diodes need to be evaluated, as N-polar GaN would control the flow of current from the perspective of the GaN SJ diode.

3. The N-polar GaN surface is highly reactive to the standard chemicals used in day-to-day device fabrication processes. Additionally, a lower Schottky barrier height for N-polar GaN is reported in comparison to Ga-polar GaN. Thus, the ultra-thin SiN interlayer is

proposed to passivate the surface polarization charge, introduce a chemical barrier, and increase the Schottky barrier height of the diode.

4. Another alternative to increase the barrier height while keeping unipolar device properties is to form a camel diode. The camel diode requires a thin layer of p-type doping. The thickness and doping of this p-type layer would tune the barrier height between the Schottky barrier and the p-n diode barrier. In N-polar GaN, achieving p-type doping is crucial because p-type dopants are usually compensated by background unintentional n-type (oxygen) dopants. Thus, demonstration of p-type conductivity is first required in N-polar GaN. To this end, first, a study of the N-polar GaN p-n diode is required. This would help to realize a camel diode in N-polar GaN.

5. In the end, the study of lateral polar junction-based SJ structure to estimate the doping levels in both Ga-polar (p-type) and N-polar (n-type) via electrical and material characterization techniques.

From the ion implantation perspective, the development of the high-pressure and high-temperature post-implantation anneal technique has provided a path to realize the control of p-type doping in GaN via Mg ion implantation. The validation of p-type doping in GaN is validated by fabricating kV-class p-n diodes with p-type doping using Mg ion implantation followed by high-pressure and high-temperature post-activation anneal. This would enable to realize selective area p- and n-type doping in GaN.

1.6 Thesis Outline

The thesis aims to develop insight into each building block mentioned previously to realize a path to obtaining GaN-based vertical superjunction devices. The thesis is organized in the following manner:

Chapter 2 reports a simple theoretical model developed for GaN SJ devices and compares it with conventional unipolar devices. A 1750 V breakdown voltage GaN SJ is designed using the developed analytical equations and simulated using Silvaco to verify the developed model. The blocking current-voltage and capacitance-voltage characteristics are reported and analyzed. The impact of charge imbalance on the GaN SJ device performance is also evaluated.

Chapter 3 reveals the electrical and material properties of N-polar GaN Schottky diodes, such as barrier height and doping levels. An investigation of how different chemicals, such as solvents, bases, and acids, used in regular device fabrication processes affect the electrical properties of N-polar GaN Schottky diodes is presented.

Chapter 4, initially, introduces the history of the developed SiN technology on GaN material. Then, the material properties of SiN and the barrier heights at metal/SiN and SiN/N-polar GaN are investigated using a 7 nm LPCVD-grown SiN interlayer. Later, introducing a 5 nm SiN interlayer shows that the barrier height can be increased, reverse bias leakage can be reduced, and reliable operation at elevated temperatures can be obtained.

Chapter 5 discloses the p-type doping capability in N-polar GaN material confirmed via Hall measurements. The N-polar GaN p-n diodes are fabricated and characterized to investigate the incorporation of Mg and oxygen. The electrical properties of N-polar p-n diodes are also compared to Ga-polar GaN diodes. Then, theoretical design equations for GaN camel diodes are devised and validated with TCAD simulations. Based on the design rules, two different N-polar GaN camel diodes are fabricated, and their electrical characteristics are

presented.

Chapter 6 demonstrates the first-ever charge-balanced GaN lateral polar junctions for GaN-based vertical SJ applications. The material characteristics of the grown LPJ are obtained via secondary electron microscopy (SEM), integrated differential phase contrast (iDPC) imaging in scanning transmission electron microscopy (STEM), secondary ion mass spectroscopy (SIMS), and atom probe tomography (APT). The electrical properties of the fabricated LPJ diode are investigated via current-voltage and capacitance-voltage characteristics. Both material and electrical characteristics confirm that the doping levels in Ga- and N-polar GaN domains are equal.

Chapter 7 presents GaN-on-GaN p-n diodes using p-type doping obtained via Mg ion implantation. These p-n diodes demonstrate 1 kV blocking characteristics as a result of successful Mg post-implantation activation anneal via high-pressure and high-temperature techniques. Silvaco-based TCAD simulations are reported to estimate the breakdown field strength of the fabricated p-n diodes.

Chapter 8 summarizes the achievements and contributions of this work and outlines avenues of potential future research.

Chapter 2

Design Space for Vertical GaN Superjunction

2.1 Background and Significance

The optimum performance of a SJ device depends on a variety of device parameters such as p/n column width, thickness, and doping, all of which can be calculated before device fabrication. Many efforts have already been made to develop analytical models for Si [19, 90], and SiC [91] SJ devices. Similar efforts are ongoing to develop a model for GaN-based SJ devices. Z. Li *et al.* [92] have reported simulation results for 5-20 kV GaN-based SJ devices. B. Song *et al.* [93] have combined two models from [90] and [91] to develop an analytical model for GaN Lateral Polarization-doped superjunction devices. However, those models are based on complicated infinite series to solve the electric field, which requires substantial computation and time. In comparison, a simplified and more intuitive approach to derive equations for modeling various parameters for Si-based SJ devices has been shown by Baliga [6]. In this thesis, the same framework is applied to GaN in order to guide the design of GaN SJ devices and provide a reference for experimental results. TCAD simulations are also performed using Silvaco ATLAS to evaluate the accuracy of the developed models. Some of the discussion and data presented in this chapter are from our publication [94].

2.2 Development of Theoretical Model for GaN SJ

Figure 2.1(a) shows the schematic cross-section of a typical SJ drift region formed with alternating p/n columns. For comparison, a cross-section of the drift region in conventional power devices is shown in Fig. 2.2(a). The unit cell cross-section of the SJ device with a half-width of p and n columns is shown in Fig. 2.1(b). The lateral depletion region forms between the p and n columns when a reverse bias is applied to the structure, which creates an electric field in the x-direction, as shown in Fig. 2.1(c). By increasing the reverse bias voltage, the depletion in the lateral direction increases and the electric field with it. To achieve better charge coupling, both columns should be totally depleted before the applied reverse bias reaches the breakdown voltage. Thus, when the reverse bias reaches the breakdown voltage, the electric field in the y-direction of the structure will be uniform, defined as the uniform critical electric field (E_{CU}) in p and n columns, as shown in Fig. 2.1(d). It is seen that a two-dimensional (2D) electric field is formed with the help of p/n columns in the SJ structure. On the other hand, for conventional devices, the electric field in the drift region increases with the reverse bias voltage. At the onset of breakdown, the maximum electric field in the device reaches to its material critical electric field (E_C). The electric field, for this case, in the drift region is triangular and one-dimensional (1D), as shown in Fig. 2.2(b). Thus, from Figs. 2.1(d) and 2.2(b), it is evident that SJ devices can have a larger breakdown voltage capability for a similarly sized drift region in conventional devices. In addition, creating a charge balance and controlling the doping laterally between p/n columns makes it possible to dope the SJ columns higher than conventional drift regions, which reduces the on-resistance. This section provides a detailed description of the theoretical model developed for GaN SJ devices. Using the developed model, device parameters such as p/n column width, doping, and thickness can be predicted for a given breakdown voltage application.

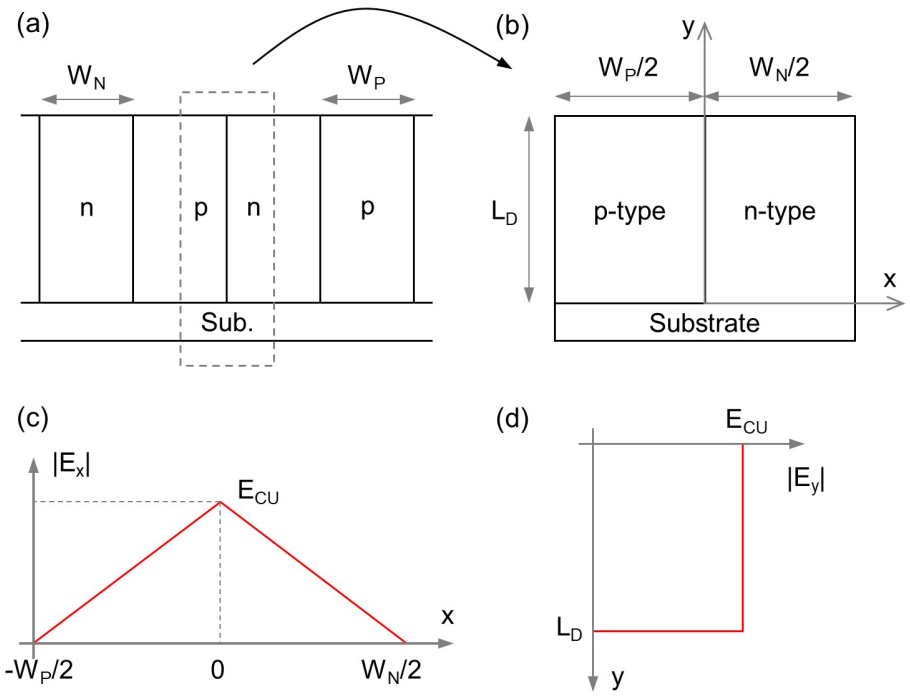

Figure 2.1: Cross-sectional view of (a) SJ device structure and (b) unit cell of the SJ structure represented in figure (a) with a dotted rectangle. The electric field distribution (c) in the x-direction obtained at the middle of the drift region ($y = L_D/2$) and (d) in the y-direction obtained at the middle of the p/n column ($x=W_N/2=-W_P/2$) at the breakdown. The figure is not drawn to scale.

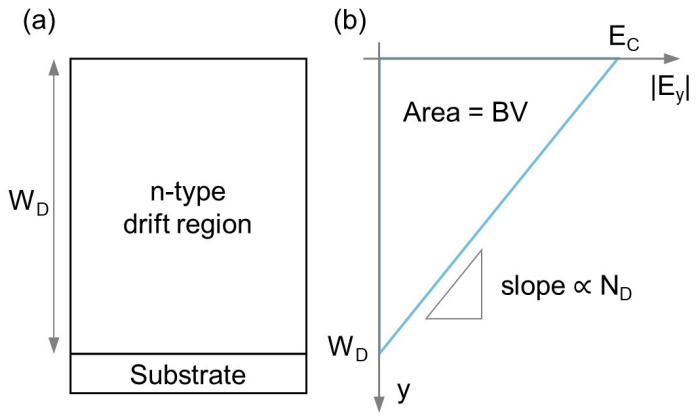

Figure 2.2: (a) Cross-sectional view of the drift region in conventional power devices. (b) The electric field distribution along the drift region at the onset of breakdown.

As the electric field increases, free carriers are accelerated, creating more free carriers through impact events with the lattice atoms in the depletion region of the drift layer. The number of free carriers increases exponentially with increasing reverse bias, and avalanche breakdown occurs when carrier multiplication reaches infinity, i.e., the impact ionization integral reaches unity [4]. The ionization integral (II) is given by:

$$II = \int_0^W \alpha_p \exp\left[\int_0^y (\alpha_n - \alpha_p)\, dy'\right] dy = 1 \tag{2.1}$$

where, W is the width of the breakdown path, α_n and α_p are the impact ionization coefficients of electrons and holes, respectively. These impact ionization coefficients can be defined as the number of electron-hole pairs created by the single electron or hole traveling 1 cm through the depletion region in the direction of an electric field. These coefficients are a function of the electric field shown as [95]:

$$\alpha_n = a_n \exp\left(-\frac{b_n}{E}\right) \quad \text{and} \quad \alpha_p = a_p \exp\left(-\frac{b_p}{E}\right) \tag{2.2}$$

where, a_n, b_n, a_p, and b_p are material-dependent parameters, and E is the electric field.

Several efforts have been taken to develop impact ionization coefficients for GaN based on theoretical and experimental work [96–101]. In this thesis, the ionization coefficients used are based on the report from Ozbek-Baliga [97]. In their work, the coefficients were obtained using the pulse electron beam technique, which localizes the measurements to avoid defects detected in the material using electron beam induced current (EBIC) scans [102]. Thus, the parameters that were reported are for ideal GaN material. From this, an assessment of GaN's true potential as a material in power devices can be made.

For simplicity, the effective value (α_{eff}) for the electron (α_n) and hole (α_p) coefficients is of used in Eq. 2.1 for the avalanche breakdown conditions. Thus, by substituting $\alpha_n = \alpha_p = \alpha_{eff}$, the ionization integral, Eq. 2.1, becomes:

$$\int_0^W \alpha_{eff}\, dy = 1 \tag{2.3}$$

For more straightforward device design calculations, Fulop reported a simple form of α_{eff} from empirical results instead of Chynoweth's form of α shown in Eq. 2.2 [95, 103]. It is given as:

$$\alpha_{eff} = C \cdot E^g \tag{2.4}$$

where, C and g are constants and can be obtained by fitting the electron and hole impact ionization coefficients. In this form, Ozbek and Baliga reported a power law for GaN by fitting the measured electron and hole impact ionization coefficients [97, 102]. As mentioned above, these electron and hole impact ionization coefficients were measured experimentally. The Ozbek-Baliga power-law fit for GaN is given as:

$$\alpha_{eff} = 1.5 \times 10^{-42} \cdot E^7 \quad [\mathrm{cm}^{-1}] \tag{2.5}$$

where E is in V/cm. By replacing the value of α_{eff} in Eq. 2.3 and solving it for the drift region thickness ($\mathrm{L_D}$), the relation between uniform electric field ($\mathrm{E_{CU}}$) and $\mathrm{L_D}$ for GaN SJ device was obtained:

$$E_{CU} = 9.44 \times 10^5 \cdot L_D^{-1/7} \quad [\mathrm{V/cm}] \tag{2.6}$$

where, L_D is in cm. As the breakdown voltage is just the product of uniform electric field and the drift region thickness of the SJ, as seen in Fig. 2.1(d), the relation between the breakdown voltage and drift region thickness of the GaN SJ device is obtained:

$$BV = E_{CU} \cdot L_D = 9.44 \times 10^5 \cdot L_D^{6/7} \quad [\text{V}] \tag{2.7}$$

where, E_{CU} is in V/cm and L_D is in cm. Hence, the thickness of the vertical p/n columns of GaN SJ for the required breakdown voltage can be calculated using:

$$L_D = 1.07 \times 10^{-7} \cdot BV^{7/6} \quad [\text{cm}] \tag{2.8}$$

The optimum dose for the charge-balanced SJ device can be found by considering the peak value of the electric field in Fig. 2.1(c), which is E_{CU}. It is expressed as:

$$Q_{optimum} = qN_D\frac{W_N}{2} = \varepsilon_S E_{CU} = qN_A\frac{W_P}{2} \tag{2.9}$$

where, $Q_{optimum}$ is the required dose to create a charge balance within the p/n columns, ε_S (=$10.4\varepsilon_0$) is the permittivity of GaN, W_N and W_P are the width of the n and p columns, respectively; N_D and N_A are the doping concentrations of the n and p columns, respectively. Using Eqs. 2.7 and 2.9, the relationship between the dose and breakdown for GaN SJ can be obtained as:

$$N_D \cdot W_N = N_A \cdot W_P = 1.08 \times 10^{14} \cdot BV^{-1/6} \quad [\text{cm}^{-2}] \tag{2.10}$$

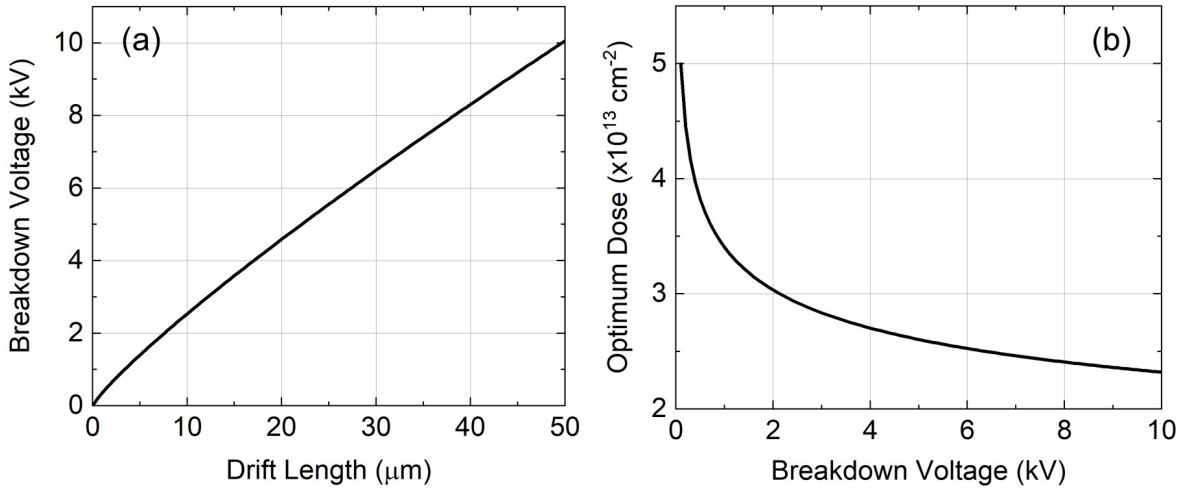

Figure 2.3: (a) Breakdown voltage versus required drift region thickness, (b) required optimum dose versus breakdown voltage for GaN-based SJ devices up to 10 kV.

Using Eqs. 2.8 and 2.10, we can find GaN SJ device parameters for a given breakdown voltage or vice versa. Figs. 2.3(a) and 2.3(b) show the drift region thickness and the optimum dose for a breakdown voltage range till 10 kV. Using the optimum dose graph shown in Fig. 2.3(b), the required doping can be calculated by choosing achievable column widths for a given breakdown voltage. For comparison, the design parameters for conventional GaN power devices can be written in similar ways and are given as [10]:

$$W_D = 1.7 \times 10^{-7} \cdot BV^{7/6} \quad [\text{cm}] \tag{2.11}$$

and,

$$N_D \cdot W_D = 6.77 \times 10^{13} \cdot BV^{-1/6} \quad [\text{cm}^{-2}] \tag{2.12}$$

where W_D is the homogeneous drift region thickness for parallel plane breakdown case. Thus, from Eqs. 2.8, 2.10, 2.11, and 2.12, it is clear that SJ devices can have a smaller drift region

thickness and higher doping compared to the conventional devices for a given breakdown voltage. It should be noted that the drift region thickness increases as per the breakdown voltage requirement increases, based on Eqs. 2.11 and 2.12 for the conventional devices. This would lead to a reduction in doping and a corresponding increase in on-resistance. In comparison, for SJ devices, the doping can still be controlled via the p- and n-type column widths. This would allow increasing doping for the drift region of SJ, reducing the on-resistance for a similar breakdown voltage capability device compared to conventional devices.

As SJ devices can have larger drift region doping, a lower on-resistance can be obtained compared to equivalent conventional devices. The ideal specific on-resistance for the SJ structure, shown in Fig. 2.1(b), considering unipolar current flow, i.e., only through n column, can be given as [6]:

$$R_{on,sp-ideal} = \frac{L_D}{q\mu_n N_D} \cdot \frac{W_N + W_P}{W_N} \tag{2.13}$$

Now, L_D and N_D (=N_A) can be replaced in terms of the BV to obtain a relation between on-resistance and breakdown voltage as follows:

$$L_D = \frac{BV}{E_{CU}} \tag{2.14}$$

and,

$$N_D = \frac{2 \cdot \varepsilon_S \cdot E_{CU}}{q \cdot W_N} \tag{2.15}$$

Using Eqs. 2.13, 2.14, 2.15, and assuming $W_N = W_P$, the ideal specific on-resistance can be written as:

$$R_{on,sp-ideal} = \frac{BV \cdot W_N}{\varepsilon_S \cdot \mu_n \cdot E_{CU}^2} \tag{2.16}$$

Now, using Eqs. 2.7 and 2.8, the uniform electric field, in the form of breakdown voltage, can be represented as follows:

$$E_{CU} = 9.35 \times 10^6 \cdot BV^{-1/6} \quad [\mathrm{V/cm}] \tag{2.17}$$

Thus, the ideal specific on-resistance for GaN SJ devices can be given as:

$$R_{on,sp-ideal}(SJ) = \frac{1.444 \times 10^{-14} \cdot BV^{4/3} \cdot W_N}{\varepsilon_S \cdot \mu_n} \quad [\Omega \cdot \mathrm{cm}^2] \tag{2.18}$$

A similar relationship of on-resistance with respect to breakdown voltage for the conventional GaN power devices with the 1D electric field has been derived and shown as:

$$R_{on,sp-ideal}(1D) = \frac{2.457 \times 10^{-21} \cdot BV^{5/2}}{\varepsilon_S \cdot \mu_n} \quad [\Omega \cdot \mathrm{cm}^2] \tag{2.19}$$

From these on-resistance equations, in the case of SJ devices, the on-resistance is proportional to breakdown voltage with a power of 4/3 for SJ. In contrast, for conventional devices, it is a power of 5/2. Thus, it is clearly seen that the SJ devices break the 1D theoretical limit of conventional unipolar devices and offer very small on-resistance. Additionally, the on-resistance for SJ devices also depends on the width of the p/n column as seen in Eq. 2.18; thus, smaller column widths further reduce the on-resistance of the SJ devices. Using Eqs. 2.18 and 2.19, the comparison of on-resistance versus breakdown voltage characteristics for GaN conventional (1D limit) and SJ devices with different column widths (for $W_N = W_P$) are

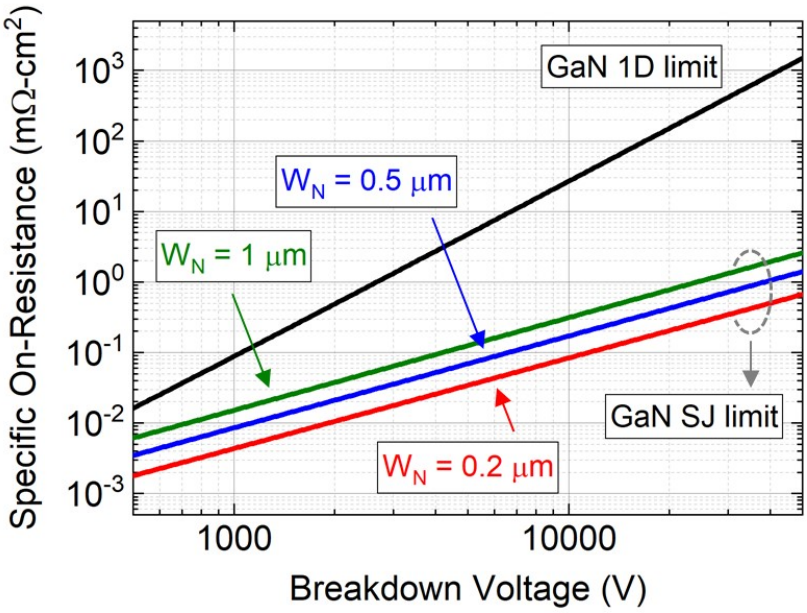

Figure 2.4: Theoretical limit of the ideal specific on-resistance versus breakdown voltage comparison for GaN SJ devices. The on-resistance for three different column widths of SJ devices are compared with the conventional 1D devices.

shown in Fig. 2.4. It should be noted that the specific on-resistance reported here is only from the drift region portion of the device and does not include the parasitic resistances such as resistance of substrate and resistances of anode and cathode metal contacts. The graph shows on-resistances for 0.2 μm, 0.5 μm, and 1 μm column widths GaN SJ devices. The cell pitch size ($W_{cell} = W_N + W_P$) of these SJ devices would be 0.4 μm, 1 μm, and 2 μm. The pitch size of 1 μm and 2 μm can be easily achieved via stepper lithography. Whereas for 0.4 μm pitch size devices, laser interference lithography can be used to achieve large area patterns on substrates [104–107]. In this work, 2 μm pitch size is implemented using stepper lithography to realize GaN SJ devices. A comparison of the ideal theoretical R_{ON} vs. BV between 1D and SJ devices for Si, SiC, and GaN is shown in Fig. 2.5. In the graph, the cell pitch of the SJ devices is chosen to be 2 μm. For comparison, the experimental results of Si and SiC SJ-MOSFET are shown in the graph with the respective cell pitch size of the

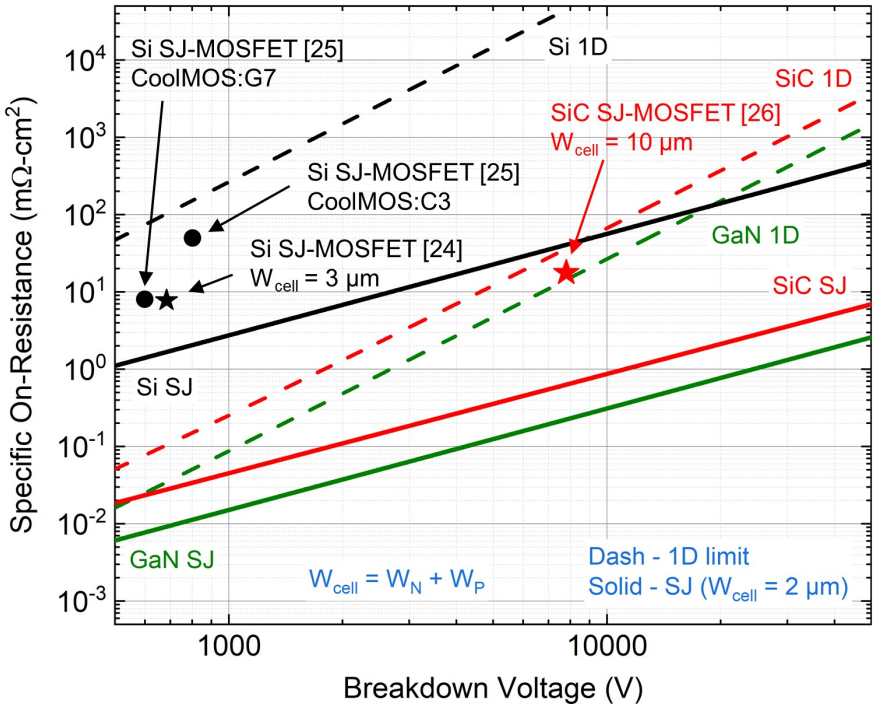

Figure 2.5: Comparison of the ideal specific on-resistance versus breakdown voltage between 1D limit and SJ limit for Si, SiC, and GaN technologies. The W_{cell} for the SJ devices is 2 μm.

p/n columns. In addition, few commercially available Si SJ-MOSFETs (CoolMOS) are also reported in Fig. 2.5. It is worth noting that these Si and SiC experimental devices show lower R_{ON} than their 1D limit. Thus, SJ devices can outperform their conventional unipolar devices. As per the graph, it can be observed that the GaN SJ devices would have lower R_{ON} than SiC-based SJ devices. Additionally, as the fabrication of SiC-based SJ devices rely on either implantation or etch/regrowth techniques, achieving a smaller cell pitch would be crucial due to lithographic limitations, especially in the case of multiepitaxy when thicker drift regions are required for high BV devices. In comparison, for the GaN-based SJ devices using the LPJ approach, the buffer layer needs to be patterned only once at the beginning of the growth to obtain p/n columns in a single growth run. After patterning the buffer layer, thick p/n columns can be grown in a single growth run without requiring multiepitaxy and alignments of multiple lithographies. Thus, a relatively smaller cell pitch can be realized in

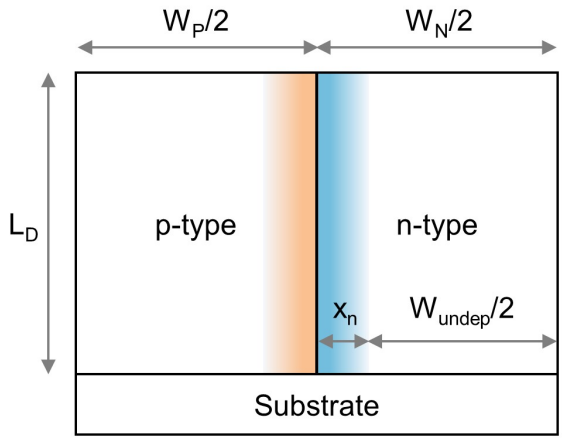

Figure 2.6: The schematic cross-section of the unit cell SJ device structure, including depletion region across the lateral p-n junction columns due to the built-in potential. Here, W_{undep} is the undepleted region in an n-type column, and x_n is the depleted region. The development of the depletion region reduces the available area for the current in an n-type column.

GaN SJ devices compared to SiC SJ devices, which would allow a larger doping level to be used, in turn leading to a further reduction in R_{ON}.

As mentioned previously, the above derived specific on-resistance equation (Eq. 2.18) is for the ideal SJ device structures. In real devices, the available area for the current would be lower due to the presence of the depletion layer created by lateral p-n diode built-in potential. The schematic cross-section of the SJ structure, including depletion regions in p/n columns, is shown in Fig. 2.6. Thus, the actual specific on-resistance for the SJ devices would be the modified version of Eq. 2.13, and can be written as:

$$R_{on,sp-ideal} = \frac{L_D}{q\mu_n N_D} \cdot \frac{W_N + W_P}{W_{undep}} \tag{2.20}$$

where, W_{undep} is the undepleted portion of the n column width from where the electrons would flow during the on-state, which is written as:

$$W_{undep} = W_N - 2x_n \tag{2.21}$$

where, x_n is the depletion region width in the n column, and it can be given as:

$$x_n = \left(\frac{2 \cdot \varepsilon_S \cdot (V_{bi} - V_F) \cdot N_A}{q \cdot N_D \cdot (N_A + N_D)} \right)^2 \tag{2.22}$$

where, V_{bi} is the built-in potential between n and p columns and V_F is the applied forward bias. Thus, the presence of the depletion region would slightly increase the on-resistance value from its ideal theoretical value in SJ devices. Recently, Zhou *et al.* also reported theoretical calculations on the performance limitations due to the depletion regions in the SJ made with impurity-doped columns. However, they suggested use of a natural polarization superjunction structure in GaN could avoid this issue as no dopants are needed [108].

2.3 TCAD Simulations of GaN Superjunction

TCAD simulations are performed using Silvaco ATLAS to evaluate the accuracy of the developed model for GaN SJ. A 1750 V breakdown voltage GaN SJ diode for a 1.2 kV rating application is designed and simulated to validate the designed equations in the previous section. The following subsections provide insight into the blocking characteristics and capacitance-voltage characteristics of the 1750 V GaN SJ.

2.3.1 Blocking Characteristics of 1750 V GaN SJ

The required parameters to simulate the SJ structures are the thickness of the drift region (L_D), and widths (W_P, W_N), and doping concentrations (N_A, N_D) of the p/n columns, all of which can be calculated using the above-designed model. According to Eq. 2.8, the required drift region thickness (L_D) to achieve 1750 V breakdown is 6.5 μm. Similarly, using Eq. 2.10, the required dose ($N_D \cdot W_N = N_A \cdot W_P$) in the p/n column is $\sim 3 \times 10^{13}$ cm^{-2}. Choosing W_N =

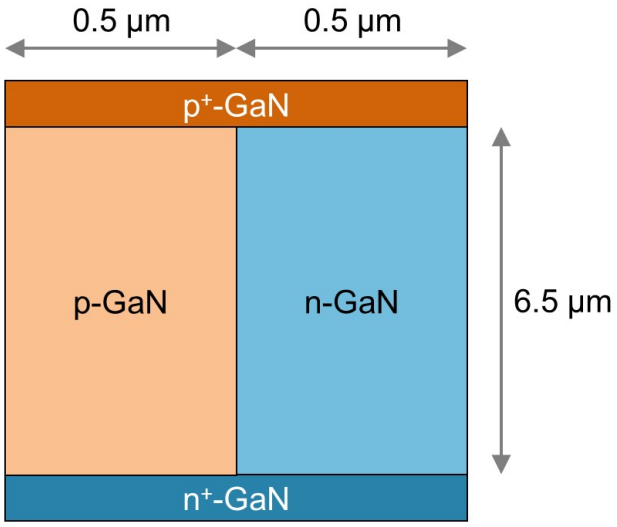

Figure 2.7: The schematic cross-section of the simulated GaN SJ device structure for 1750 V breakdown voltage capability. The required drift region thickness (L_D) is 6.5 μm. The half widths of p- and n-type columns ($W_N/2 = W_P/2$) are 0.5 μm each. The doping concentration ($N_A = N_D$) in each column is $\sim 3\times10^{17}$ cm^{-3}.

$W_P = 1$ μm, as it is easily manufacturable with the i-line stepper lithography, the required p/n column doping ($N_A = N_D$) is calculated from dose, and it is $\sim 3\times10^{17}$ cm^{-3}. The cross-section of the simulated structure for the 1750 V breakdown GaN SJ device is shown in Fig. 2.7. It should be noted that the structure has an additional p$^+$-GaN layer on top in comparison to the structure shown in Fig. 2.1(b). This is only used to facilitate the modeling of the reverse blocking performance of the SJ diode. The actual realization of the GaN SJ diode for the purpose of this thesis would be unipolar in nature.

Table 2.1: Impact ionization model parameters for GaN from [97].

a_n (cm^{-1})	1.5×10^5
b_n (V/cm)	1.41×10^7
a_p (cm^{-1})	6.4×10^5
b_p (V/cm)	1.46×10^7

As reported in Section 2.2, the simplest form of impact ionization coefficient is used to derive the GaN SJ device design parameters with the help of the Ozbek-Baliga power law [97, 102]. This power-law was extracted using the measured impact ionization coefficients for electrons and holes in the form of Eq. 2.2. Therefore, the electron and hole impact ionization coefficients used for the GaN SJ device simulations are taken from their work, and the values are reported in Table 2.1.

The corresponding Silvaco-based TCAD simulation results show a breakdown voltage of 1730 V, which is in good agreement with the developed model. The reverse blocking current-voltage (I-V) characteristics of the GaN SJ diode are shown in Fig. 2.8(a). As mentioned in the previous section, the avalanche breakdown occurs when the ionization integral reaches 1, meaning the total number of electron-hole pairs generated within the depletion region approaches infinity. The simulated ionization integral for the GaN SJ device as a function of applied bias is reported in Fig. 2.8(b). The graph shows that the ionization integral reaches 1

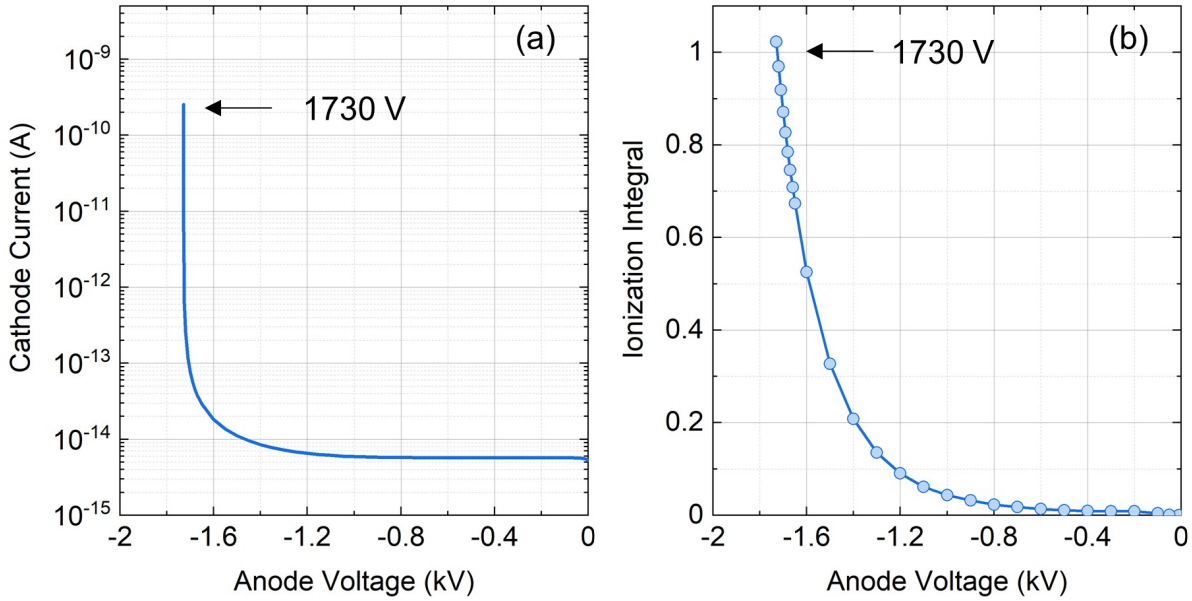

Figure 2.8: Simulated (a) blocking I-V characteristics and (b) ionization integral of the 1750 V designed GaN SJ device. The extracted breakdown voltage is 1730 V.

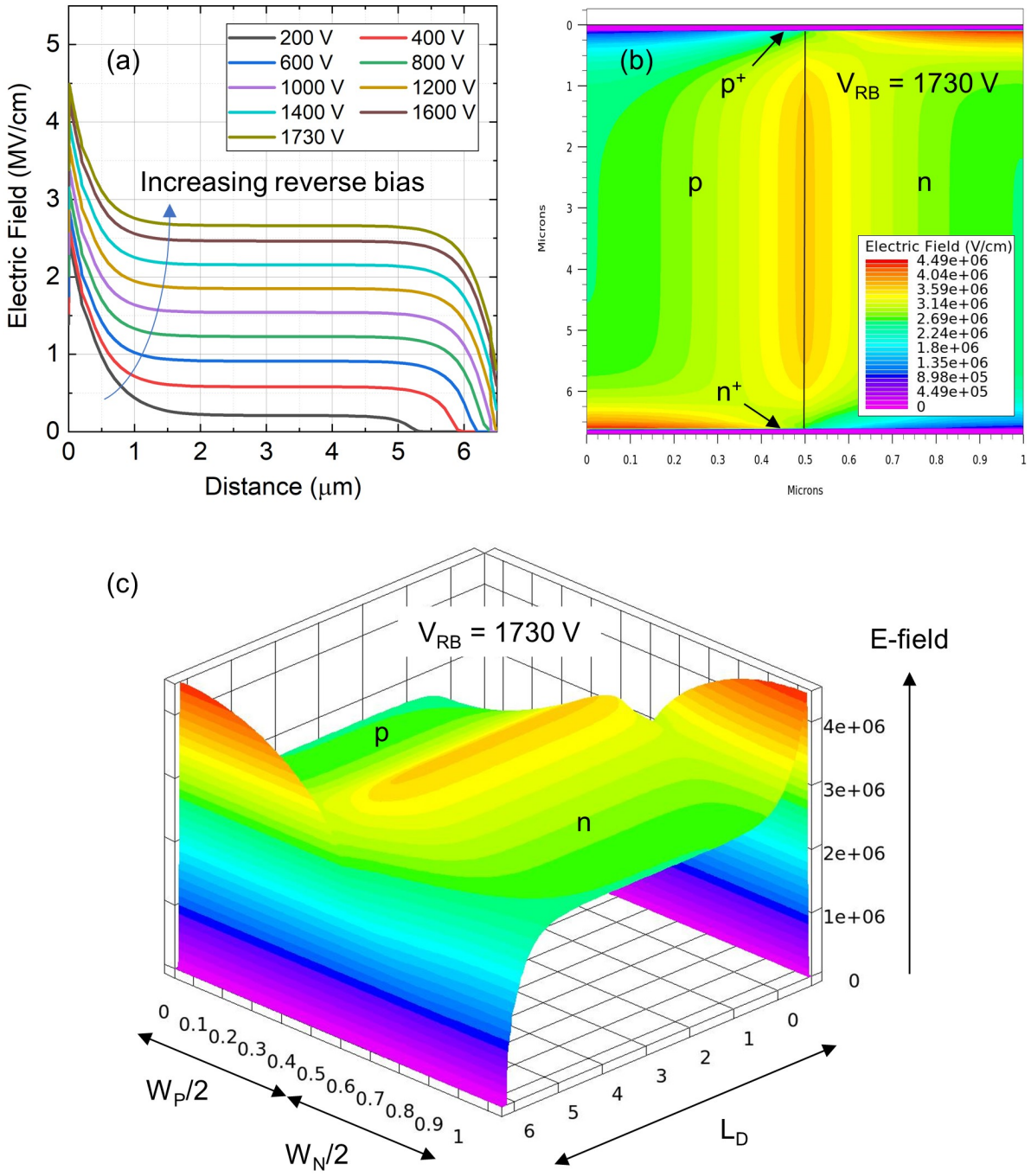

Figure 2.9: (a) Evolution of the electric field profile in the vertical direction across drift region at x = $W_N/2$ as a function of reverse bias. (b) Two-dimensional (c) three-dimensional electric field distribution in the device at reverse bias 1730 V.

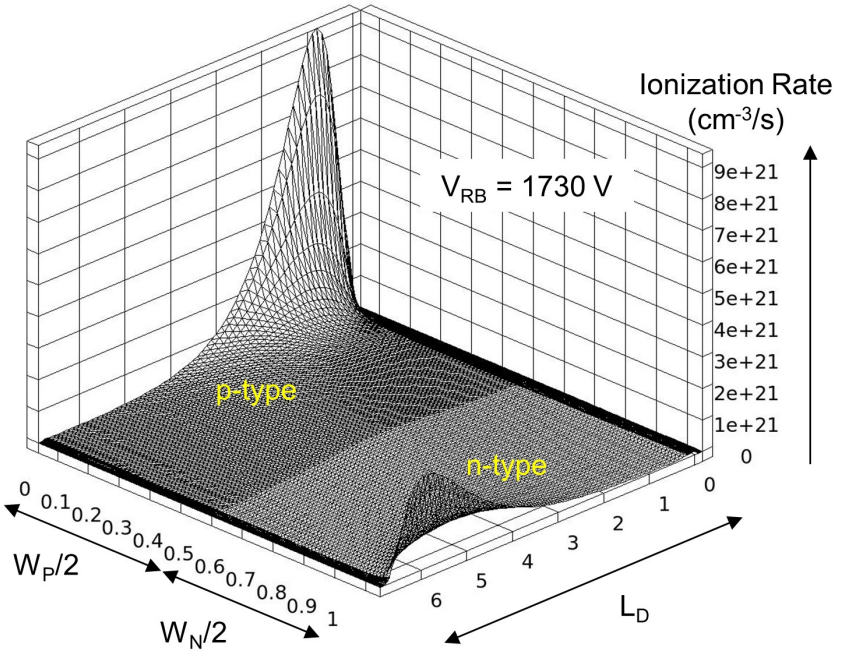

Figure 2.10: Three-dimensional impact ionization rate at the onset of breakdown (1730 V).

at 1730 V, confirming that the breakdown at that bias is due to the avalanche multiplication.

The electric field profile along the vertical direction across the drift region at x = $W_N/2$ is shown in Fig. 2.9(a) as a function of the reverse bias voltages. It is seen that, at higher reverse biases, the electric field is very uniform with a slightly higher e-field near the lateral p/n junction, at the bottom of p-type, and the top of the n-type column. Two-dimensional and three-dimensional electric field contours at the onset of breakdown, at 1730 V, are shown in Figs. 2.9(b) and 2.9(c), respectively. A three-dimensional view of the generation of free carriers by impact ionization is shown in Fig. 2.10 at the onset of breakdown. The graph suggests that impact ionization, i.e., breakdown, occurs at $W_N/2$ and $W_P/2$, instead of at the top p^+-n or bottom p-n^+ interfaces [see Fig. 2.7].

In comparison, a conventional GaN device with the same drift region doping (3×10^{17} cm^{-3}) is simulated using Silvaco too. The breakdown voltage of that conventional GaN diode is

found to be around 220 V. Thus, SJ devices clearly offer a performance advantage over their conventional unipolar counterparts. These results demonstrate that the first-order device design parameters for a GaN SJ diode can be calculated using the model designed in this thesis. It should be noted that these models are not valid in the presence of the charge imbalance (i.e., when $N_D \cdot W_N \neq N_A \cdot W_P$). The insight on the SJ performance degradation due to the charge imbalance is given in Section 2.4.

2.3.2 Capacitance-Voltage Characteristics of 1750 V GaN SJ

The capacitance-voltage (C-V) characteristic of the same 1750 V SJ diode simulated above is analyzed. The C-V characteristic in reverse bias from 0 V to -1730 V is shown in Fig. 2.11. As the reverse bias increases, the depletion region is formed due to the modulation of charges

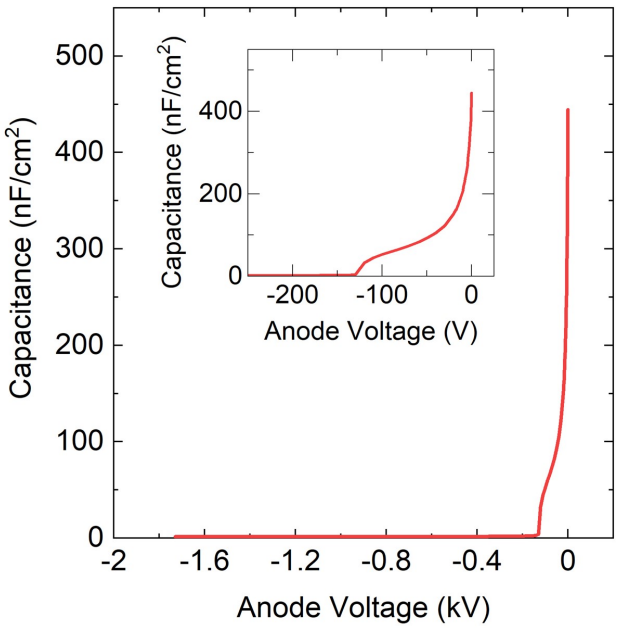

Figure 2.11: The capacitance-voltage characteristics of 1750 V GaN SJ diode. The inset graph shows the same C-V curve for 0 V to -250 V.

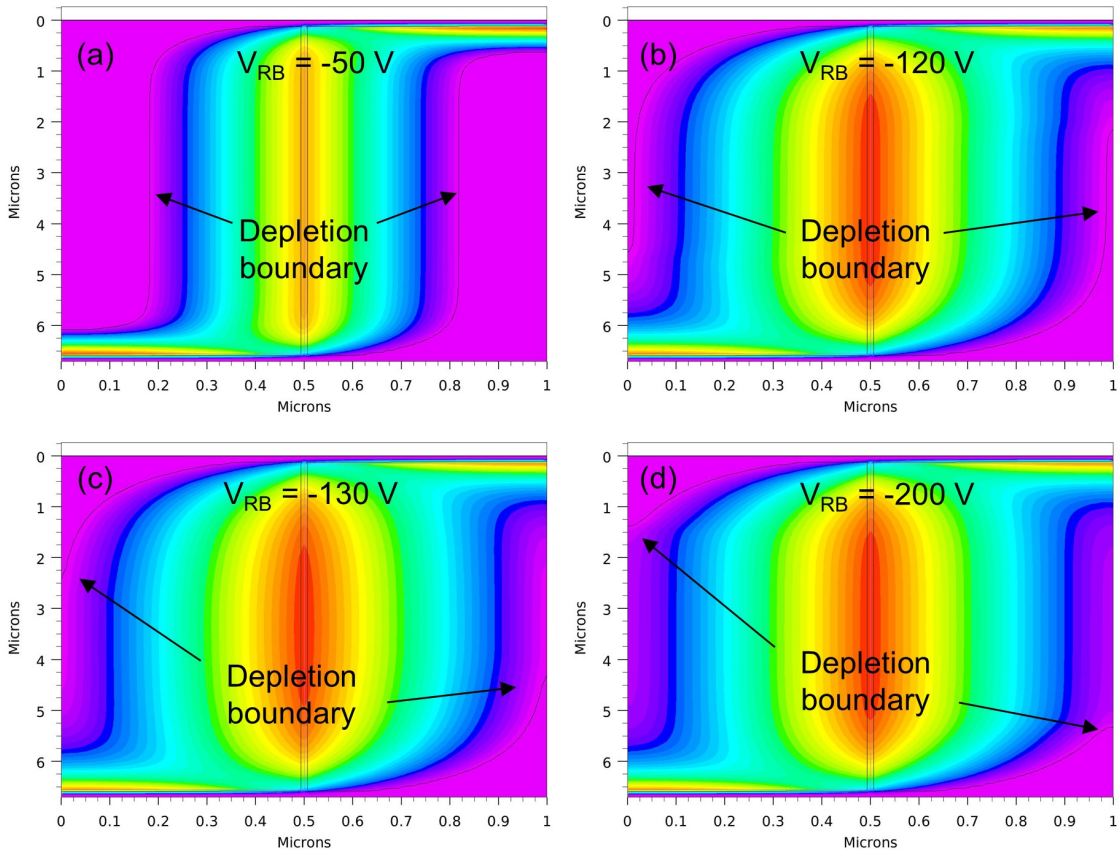

Figure 2.12: The 2D electric field contours of 1750 V GaN SJ structure including depletion edge boundary at reverse bias (a) -50 V, (b) -120 V, (c) -130 V, and (d) -200 V.

at three different junctions in the SJ, namely at the top p^+-n junction, lateral p-n junction, and bottom p-n^+ junction. The depletion region increases with increasing reverse bias that, in turn, reduces the capacitance. The capacitance drops sharply when going from 0 V to -200 V and becomes almost constant after that. The inset of Fig. 2.11 shows the C-V graph in reverse bias from 0 V to -250 V. It is clearly seen that the transition in capacitance happens between -120 V to -130 V. To investigate further, the development of depletion regions at different reverse bias voltages are simulated and reported here. The 2D electric field contours at the reverse bias voltages -50 V, -120 V, -130 V, and -200 V are shown in Figs. 2.12(a) to 2.12(d). In those graphs, the depletion region boundary is presented as a black line, which

can be seen at the end of the electric field contour. It can be observed that initially, the depletion region grows at all three junctions, and is thus responsible for the sharp roll-off in the capacitance up to -100 V [see Fig. 2.11]. From -120 V to -130 V, only a small increase in the depletion region is observed, as seen in Figs. 2.12(b) and 2.12(c). This explains the change in slope in this voltage range. After -130 V, the depletion region barely increases. This means that no charges are modulated, and no change in the capacitance is observed as a function of reverse bias until breakdown. This is the exact reason why the electric field in SJ devices is uniform in the vertical direction [see Fig. 2.9(a)]. A similar abrupt reduction in capacitance is also reported for simulated C-V analysis in Si-based SJ diode [109]. As a result of the abrupt reduction of capacitance at lower reverse biases, the turn-off energy loss of the SJ diode would be very small compared to a conventional diode. However, this would create an abrupt rise in anode voltage during the turn-off transient, which would result in a large dV/dt transient. This large dV/dt could be an issue in power electronic circuits [6].

2.4 Effects of Charge Imbalance on SJ Performance

As mentioned earlier, a drift region of the superjunction structure is made of p- and n-type columns, which should have equal dose (or, in other words, be charge-balanced) to achieve maximum possible breakdown voltage from the designed SJ structure. However, achieving perfectly charge-balanced structures is difficult in actual device fabrication due to a variety of technological challenges, such as p-doping activation. Thus, an investigation is required to analyze the impact of charge imbalance on the breakdown voltage of the SJ device.

The charge imbalance (CI) is typically represented in percentage, and it would be created because of the difference in doping of p/n columns ($N_D \neq N_A$) or variations in the width of p/n columns ($W_N \neq W_P$). In this work, the charge imbalance is investigated via variations of doping

levels in p/n columns. As seen in the previous section, the optimal doping concentrations for both p- and n-type columns can be extracted using Eq. 2.10 for a given breakdown voltage application. For the charge imbalance, two cases can be considered: first, the variations in p column doping when doping in n column would be the optimally designed doping, and second, the variations in n column doping when doping in p column would be the optimally designed doping. Charge imbalance percentage in both cases can be defined as:

$$\text{CI (p-column)} = \frac{N_A - N_D}{N_D} \times 100\% \tag{2.23}$$

and,

$$\text{CI (n-column)} = \frac{N_D - N_A}{N_A} \times 100\% \tag{2.24}$$

Based on the above equations, we can see that the charge imbalance can be negative or positive depending on whether the doping is lower or higher than optimal doping in another column.

The impact of charge imbalance on breakdown voltage for the above designed 1750 V GaN SJ device structure is analyzed using Silvaco TCAD simulations. As reported earlier, the required optimal doping in p/n columns for 1750 V GaN SJ structure is 3×10^{17} cm^{-3} when the p/n column widths are 1 μm each. Two cases are considered for the charge imbalance in the 1750 V SJ device. In the first case, negative charge imbalance is created in SJ by keeping optimal design doping in the n column and reducing doping in the p column. In the second case, positive charge imbalance is created in SJ by keeping the optimal doping in the p column and increasing doping in the n column. For both cases, the other device parameters of the 1750 V SJ device are kept the same as they are, such as L_D is 6.5 μm and W_N and W_P

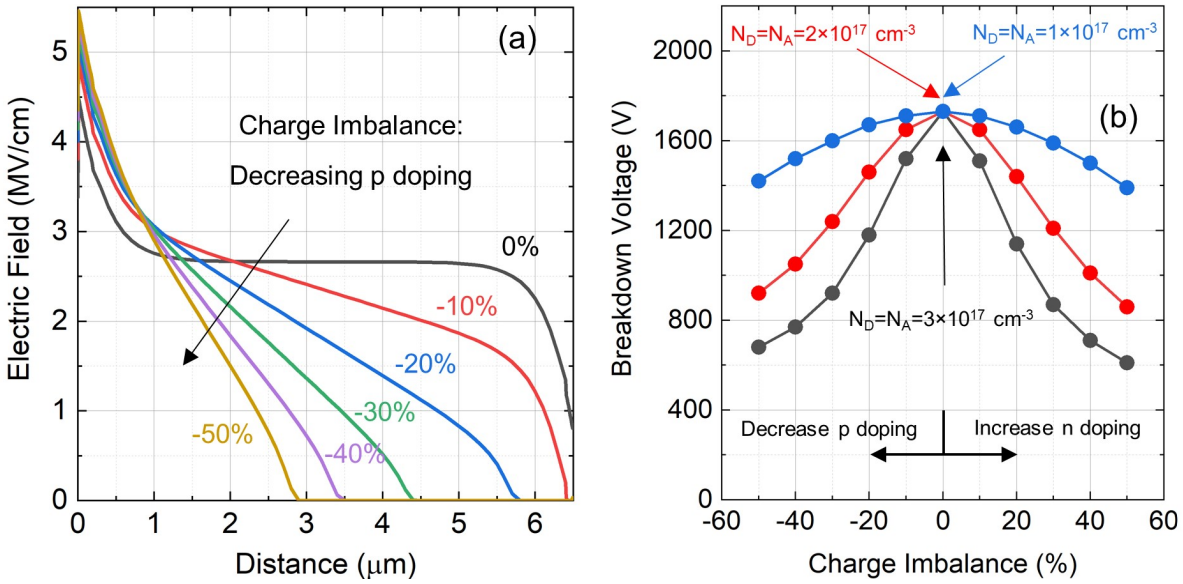

Figure 2.13: (a) The electric field distribution along the y-direction (at the onset of breakdown voltage) at x= $W_N/2$ in charge-imbalanced 1750 V GaN SJ diode structure with various charge imbalance percentages. The charge imbalance is created by reducing doping in the p column. (b) The breakdown voltage versus charge imbalance as a function of doping imbalance between the p and n columns. For both figures, the dimensions of SJ structures are L_D = 6.5 μm and W_N = W_P = 1 μm.

are 1 μm each. For the first case, doping in a p-type column is reduced from 3×10^{17} cm^{-3} to vary charge imbalance from 0% (charge-balanced) to -50% in step of -10%. For the second case, doping in an n-type column is increased from 3×10^{17} cm^{-3} to vary charge imbalance from 0% (charge-balanced) to 50% in step of +10%.

Figure 2.13(a) shows the electric field along the y-direction of the drift region at x=$W_N/2$ at the onset of breakdown for various charge imbalance percentages. The graph shows that the electric field changes from uniform to triangular distribution as the charge imbalance percentage increases. Thus, the breakdown voltage of the device would reduce as a function of charge imbalance. This can be seen in Fig. 2.13(b). The breakdown voltages for both positive and negative charge imbalances are simulated and shown in Fig. 2.13(b). As mentioned earlier, negative charge imbalance is created by reducing the p-type doping, while positive charge

imbalance is created by increasing the n-type doping. Here, the breakdown voltage for a charge-balanced case (0%) is the center point of the x-axis in the graph. The black circles with a line represent the case when the optimal doping for a charge-balanced case ($N_A = N_D$) is 3×10^{17} cm^{-3}. It can be observed that the breakdown voltage degrades sharply from 1730 V to lower voltages with a positive or negative charge imbalance. In comparison, two other cases are studied when optimal doping concentration in the balanced case is reduced to 2×10^{17} cm^{-3} (red circles with line) and 1×10^{17} cm^{-3} (blue circles with line). As shown in Fig. 2.13(b), the breakdown voltage at the charge balance point for both these cases is still 1730 V. Thus, the reduction in optimal doping does not degrade the SJ performance only if the charge is balanced in both columns. Nonetheless, even if the optimal doping is reduced, the breakdown voltage still degrades with the increase in charge imbalance. Interestingly, the reduction in the breakdown voltage with the charge imbalance is lower as we reduce the optimal doping, as seen in Fig. 2.13(b). Thus, the impact of charge imbalance could be lowered by reducing the optimal doping. A similar trend was reported by Napoli *et al.* for Si SJ devices [110].

However, reducing the optimal doping would increase the on-resistance of the SJ. Additionally, as the p/n column widths are constant even though doping levels are reduced, the depletion width would increase if the optimal doping levels would be reduced. This would lower the available area for the current flow and thus again increases the on-resistance. Nonetheless, the doping level in the case of conventional GaN unipolar devices to obtain 1730 V breakdown would be in the range of 1×10^{16} cm^{-3}. Thus, the on-resistance in SJ device, using $N_A = N_D = 1\times10^{17}$ cm^{-3}, would still be lower than in conventional GaN unipolar power device.

2.5 Conclusion

In summary, a first-order analytical model to obtain design parameters for GaN SJ devices is realized using the impact ionization coefficients for GaN reported in the literature. This model is validated using the TCAD simulations of a 1750 V GaN SJ diode. It is confirmed that not only does the analytical model provide an accurate estimate of the drift layer requirements, but that the GaN SJ will indeed outperform a conventional GaN unipolar device with equivalent drift region doping thickness. C-V analysis shows the growth of depletion regions at three different junctions as a function of bias in the SJ structure. Due to the faster depletion at the lateral p-n junction, the abrupt reduction of capacitance is observed at very low reverse bias voltages than the designed breakdown voltage for SJ. This confirms that both columns are fully depleted before the bias reaches to breakdown voltage. Understanding the growth of depletion regions in SJ structure is utilized to analyze doping levels in the experimental LPJ diode reported in Chapter 6. The impact of charge imbalance on the SJ device performance is also evaluated using simulations. It is observed that the SJ breakdown performance deteriorates significantly in the presence of charge imbalance when the device is designed using the optimal device design parameters from developed analytical equations. Instead, a slight reduction in the doping levels than optimal doping levels for both the columns has a lower effect in the presence of charge imbalance.

Chapter 3

Study of N-polar GaN Material Properties via Schottky Contacts

N-polar GaN films obtained via MOCVD are typically n-type due to high unintentional oxygen incorporation ($>10^{19}$ cm^{-3}) that acts as a shallow donor [45, 67, 68]. Therefore, it becomes the natural choice for the n-type pillar of the GaN LPJ-based SJ device. There remain, however, many open questions regarding the electrical properties of devices made with N-polar GaN, and the processing approaches that must be adopted in response to its heightened chemical sensitivity. Moreover, it is crucial to avoid the formation of hillocks and pits on the surface of the N-polar GaN films as they lead to higher inversion domains [52, 55, 111], meaning Ga-polar regions within N-polar columns, which may alter the doping levels of the film. Thus, the primary focus of this chapter is to investigate the electrical properties of the N-polar GaN from an SJ device perspective and provide feedback to the material grower to meet the doping requirements, especially in N-polar GaN in the order of $\sim 10^{17}$ cm^{-3} for the SJ device fabrication. Additionally, it is also observed that the N-polar GaN surface readily reacts with the base and acid chemicals, which are typically used in regular semiconductor device fabrication processes [112–115]. However, these previously published reports did not provide a detailed explanation of how these chemicals affect the behavior of Schottky contacts. Therefore, an investigation of how these chemicals change the electrical properties of the N-polar GaN Schottky contacts is provided in this chapter. Most of the results are from our publication [116].

3.1 Introduction

The surface properties of any semiconductor strongly impact the behavior of metal - semiconductor contacts. Therefore, to realize high-performance GaN devices, a systematic study of how processing steps impact the semiconductor surface and accompanying metal-semiconductor interfaces is essential. Hacke *et al.* reported on the first GaN Schottky diodes with a barrier height of 0.844 eV and 0.94 eV for Au on n-GaN using current-voltage (I-V) and capacitance-voltage (C-V) measurement techniques, respectively [117]. Since then, several research groups have studied Schottky contacts to n-type doped GaN by using different metals. Amongst them, the most commonly studied metals on n-type doped GaN for Schottky contacts are Pt and Ni, whose I-V barrier heights range from 0.83 to 1.13 eV [118–121] and 0.66 to 1.13 eV [122–125], respectively. It is worth noting that there is a significant spread in the reported barrier height values for a given metal choice, as well as a dependence on the measurement techniques used (e.g., I-V vs. C-V). The reason for the barrier height inhomogeneities is usually attributed to high surface state densities, low/high barrier surface defects, metal-induced gap states (MIGS), surface morphology, tunneling current components, and the presence of the native oxides at the metal/semiconductor interface [126]. These types of inhomogeneities in GaN Schottky diodes are frequently reported in the literature [120, 121, 123, 124].

In addition, GaN Schottky contacts are influenced by surface polarization charges. Studies have shown that the polar axis may influence the barrier height and the band bending at the surface of GaN [119, 127–129]. According to Reddy *et al.* [130], who studied the surfaces of Ga-polar and N-polar GaN using X-ray Photoelectron Spectroscopy (XPS), the barrier height decreases from Ga-polar to non-polar to N-polar. Similarly, Rizzi and Luth [131] reported a theoretical prediction of the difference in Schottky barrier height between Ga- and N-polar GaN, in which a polarization charge (Q_{pol}/e) of 1.8×10^{13} cm^{-2} in N-polar GaN surface reduced the barrier height of N-polar GaN by 0.33 eV. In further studies, where

Schottky diodes were made, it was also found that the barrier height of N-polar GaN was lower than that of Ga-polar GaN [119, 132–135].

Non-idealities at the metal/semiconductor interface may arise from the reaction of the GaN surface to the chemicals used in device fabrication processes. Therefore, to achieve near-ideal device performance, it is crucial to identify which chemicals maintain a pristine surface prior to Schottky metal contact deposition. Numerous chemical treatments have been studied to clean the Ga-polar GaN surface [125, 136, 137]. Reddy *et al.* [125], for example, employed an acid treatment to remove adventitious carbon before depositing Ni-based Schottky contacts. In doing so, they reported defect-free forward and reverse bias characteristics up to an annealing temperature of 600 °C. However, due to the different growth kinetics and chemical properties of N-polar GaN [138], the chemical treatments used to clean Ga-polar GaN may not be directly translatable. In this context, Rajan *et al.* [112] and Wong *et al.* [113] reported that the chemicals required in conventional Ga-polar GaN fabrication and cleaning processes, such as bases and acids, readily react with the N-polar GaN surface. However, they did not provide electrical data to describe how these chemicals specifically impact performance. The highly reactive nature of the N-polar GaN surface is also expected to increase the thickness of the native oxide [114, 130], which should be removed before any metal contacts or passivation dielectrics are deposited. This makes it difficult to compare the results from studies involving N-polar GaN where acid or base cleaning strategies were either not used or not explicitly disclosed [119, 132, 133]. On the other hand, English *et al.* [114] and Wei *et al.* [115] each reported that the N-polar GaN surface morphology was affected by choice of acid or base treatments, but neither correlated the effects to the behavior of Schottky contacts nor did they consider the effect of common solvents used in processing. Later Downey *et al.* [134] studied N-polar GaN Schottky diode barrier heights for different metals after cleaning the surface using O_2 plasma followed by 30 s 10:1 buffered HF. However, they did not provide

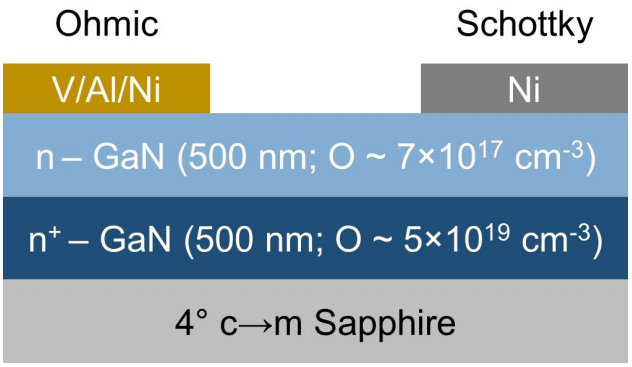

Figure 3.1: A schematic of an MOCVD grown Ni/N-polar GaN Schottky diode.

AFM or XPS scans of the surface in order to link electrical behavior to physical or chemical changes to the N-polar GaN surface as a consequence of HF treatment. In comparison, Kim *et al.* [139] reported a comparison of Schottky barrier heights between Ga-polar and N-polar GaN after cleaning the surface in HCl for 1 min. They found a similar barrier height for N-polar compared to Ga-polar GaN, which they attributed to the creation of surface states in N-polar GaN following acid exposure. Therefore, the chemical sensitivity of N-polar GaN raises the question of whether the same chemical treatment strategies that provide near-ideal Ga-polar Schottky diode behavior can be adopted by their N-polar counterparts [125, 140].

The following sections present a systematic analysis of how the electrical behavior of Ni-based Schottky contacts made to N-polar GaN is influenced by solvent, base, and acidic chemical treatments. Electrical testing is complemented by morphological and compositional characterization of the surface in order to shed light on the complicated impact chemical treatments have on N-polar GaN. Finally, a model that accounts for the variation in barrier height due to GaN surface polarity and field-enhanced barrier lowering.

3.2 Experimental Details

N-polar GaN layers were grown on a sapphire substrate 4° misoriented towards the m-plane using a vertical, cold-wall, radio frequency (RF) heated, low-pressure metalorganic chemical vapor deposition (MOCVD) system. A 500 nm thick n^+-doped layer was followed by a 500 nm thick n-type layer, as shown in Fig. 3.1. Both n^+- and n-type GaN layers were unintentionally oxygen doped [51, 141], resulting in carrier concentrations of approximately 5×10^{19} cm^{-3} and 7×10^{17} cm^{-3}, respectively. Immediately after the growth, the wafer was diced into small samples, and each sample underwent different chemical treatments, as summarized in Table 3.1. Sample A was not subjected to any chemical treatments and, therefore, served as a control sample. Samples B and C were dipped into solvent-based chemicals: Sample B was submerged in isopropyl alcohol (IPA), commonly used to remove organic residue, while Sample C was dipped into an electron-beam resist developer (MIBK:IPA = 1:3) and subsequently rinsed with IPA. The effect of exposure to a base (pH = 13) was investigated with Sample D, which was dipped into 3% Tetra-methyl ammonium hydroxide (TMAH)-based photoresist developer (CD-26) and then rinsed with deionized (DI) water for 30 sec. The

Table 3.1: Chemical treatments on different samples prior to the Schottky metal deposition.

Sample	**Chemical Treatment**
A	As-grown
B	1 min IPA
C	1 min MIBK:IPA (1:3) + 15 sec IPA rinse
D	1 min TMAH (3%) + 30 sec DI rinse
E	1 min RT HCl:H_2O (1:1) + 30 sec DI rinse
F	1 min Hot HCl:H_2O (1:1) + 30 sec DI rinse

last set of samples was subjected to acid treatment (pH < 1), specifically room temperature (RT) HCl:H_2O (1:1) for Sample E and hot (75 °C) HCl:H_2O (1:1) for sample F. HCl is chosen because it is a chemical widely used to clean the GaN surface prior to the metal deposition [125, 140, 142]. Both of these samples were rinsed with DI water. All of the samples were blow-dried with N_2.

Immediately after the chemical treatments, the first batch of the samples was loaded into an UHV e-beam evaporation chamber (base pressure: $\sim 10^{-9}$ Torr). 250 nm of nickel was deposited through a thin shadow mask to define Schottky contacts. Shadow masking was employed to avoid further exposure to chemicals that might alter the surface and confound the device's dependence on the above-listed chemical treatments. After the Schottky contact, a large area ohmic contact was employed with V/Al/Ni (30/100/200 nm) [143, 144] using the same e-beam evaporation system.

AFM and SEM were performed on these samples to investigate the changes in the surface morphology due to these chemical treatments. The second batch of chemically treated samples was loaded into an UHV (base pressure: $\sim 10^{-10}$ Torr) system to perform XPS utilizing an X-ray source with a Mg ($h\nu = 1253.6$ eV) anode. For each sample, the molar fraction (atomic %) of Ga, N, and O on the surface were measured, and the surface stoichiometry was determined from the areas under Ga $2p_{3/2}$, N 1s, and O 1s core-level peaks normalized using appropriate atomic sensitivity factors [145]. The surface sensitivity of XPS makes it possible to distinguish down to half a monolayer of oxygen. It should be noted that the total time it took to remove the samples from the MOCVD reactor, apply the chemical treatments and finally load them into an UHV chamber for either metal deposition or XPS was limited to 20 minutes.

Electrical measurements, namely room-temperature I-V, C-V, and temperature-dependent I-V (or I-V-T), were performed in a vacuum probe station (base pressure: $\sim 10^{-7}$ Torr) using a

Keithley 4200 semiconductor parameter analyzer. I-V measurements were conducted on diodes with a diameter of 70 μm. In contrast, the C-V characteristics for all six different samples were performed on 300 μm diameter diodes at room temperature. The C-V measurements were done at 1 MHz using the parallel RC (resistor and capacitor) circuit for all the diodes. The net doping concentration of the n-type region is calculated using the following equation:

$$N_D = -\frac{2}{q\varepsilon_S} \frac{1}{d\left(\frac{A^2}{C^2}\right)/dV} \tag{3.1}$$

where, A is the area of the diode, ε_S ($= 10.4\varepsilon_0$) is the permittivity of GaN, N_D is the donor concentration inside the n-type GaN. The net doping concentration in the n-GaN layer is found to be around 7.5×10^{17} cm^{-3} $\pm$ 0.5×10^{17} cm^{-3} for all samples using Eq. 3.1. The C-V barrier height is extracted for all the samples by extrapolating the $1/C^2$ vs. V graph in forward-bias where $1/C^2$ reaches to zero. It should be noted that the intercept voltage is considered to be equivalent to the C-V barrier height as the additional terms in the C-V barrier height equation [146] stays within 0.04 eV for the doping level observed in our N-polar GaN diodes. Therefore, the interpretation would not impact the C-V barrier height value in this work.

To further verify the change in Schottky barrier height with different chemical treatments, the forward bias I-V measurements are performed in vacuum (base pressure: $\sim10^{-7}$ Torr) as a function of temperature up to 200 °C. To ensure accurate I-V-T barrier height extraction, the temperature was measured on the N-polar GaN surface by a thermocouple, which was calibrated to metal melting points. The barrier heights for each chemically treated diode were extracted using the following equation:

$$\ln\left(\frac{I_0}{AT^2}\right) = \ln\left(A^{**}\right) - \frac{q\phi}{kT} \tag{3.2}$$

where, I_0 is the extrapolated saturation current, A is the area of a diode, T is the temperature, A^{**} is the effective Richardson's constant, and ϕ ($=\phi_{B,IV}$) is the I-V barrier height. Reported spreads in barrier height extracted with this method are based on measurements of five diodes. The I-V-T measurements and Richardson plots [$\ln(I_0/AT^2)$ vs. $1/kT$] are reported for all different chemically-treated samples in the Results Section, where the slope of the graph is proportional to the I-V barrier height.

3.3 Experimental Results

3.3.1 As-grown N-polar GaN

Figure 3.2(a) presents the 5×5 μm^2 AFM image of the as-grown N-polar GaN surface. It is seen that the surface roughness of the as-grown N-polar GaN is smooth and exhibits step flow with related step bunching. The smooth surface morphology was further verified using SEM, as shown in Fig. 3.2(b). From XPS [Fig. 3.2(c)], it was determined that the ratio of Ga to N is 1.28, which is as expected for the GaN surface [147]. It is also seen that the molar

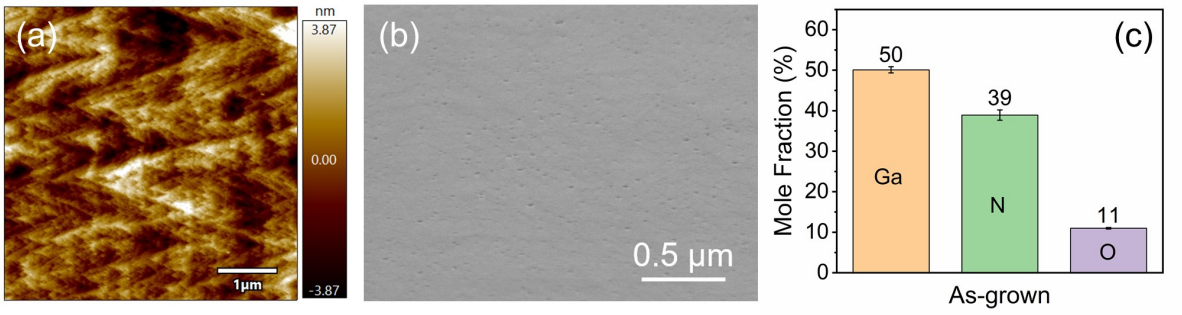

Figure 3.2: (a) AFM and (b) tilted-view SEM images of the as-grown sample indicate a smooth N-polar GaN surface prior to chemical treatments. (c) The mole fraction (in %) obtained via XPS of Ga, N, and O for the as-grown sample reveals the presence of an oxide monolayer.

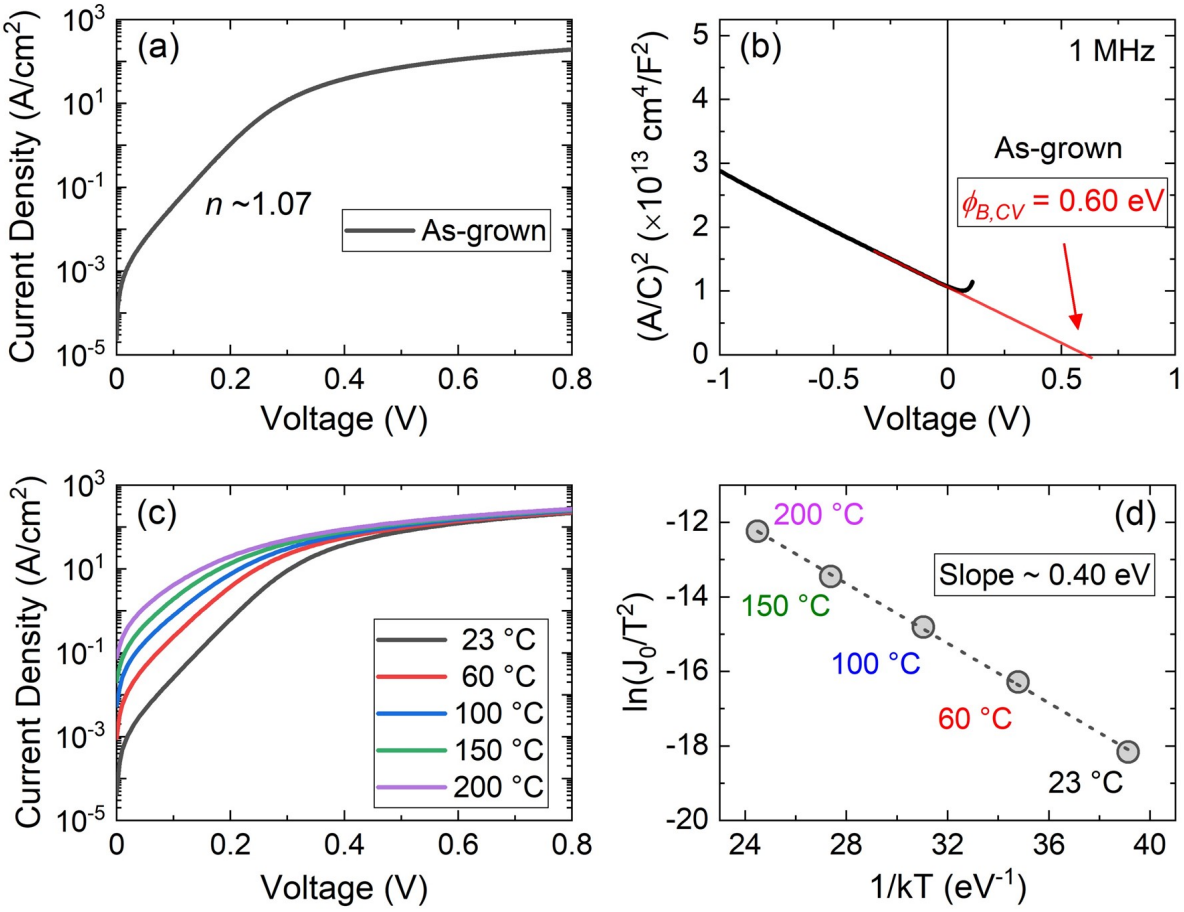

Figure 3.3: Room temperature (a) forward bias current-voltage (I-V), (b) capacitance-voltage (C-V), (c) temperature-dependent I-V characteristics, and (d) Richardson plot for as grown Ni/N polar GaN Schottky diodes.

fraction of O 1s peak is around 11%, which is slightly higher than what is typically observed in Ga-polar GaN and corresponds to 0.5-1 monolayer of native oxide [130].

Figure 3.3(a) shows the room temperature forward bias I-V of as-grown N-polar GaN surface Schottky diode. The ideality factor (n), extracted from I-V measurements of several devices, is ~1.07 to ~1.1 and represents near-ideal behavior. From the C-V behavior in Fig. 3.3(b), a barrier height of 0.60 eV is extracted, which is similar to the C-V barrier height value reported by Fang *et al.* [132]. The temperature-dependence of the forward I-V

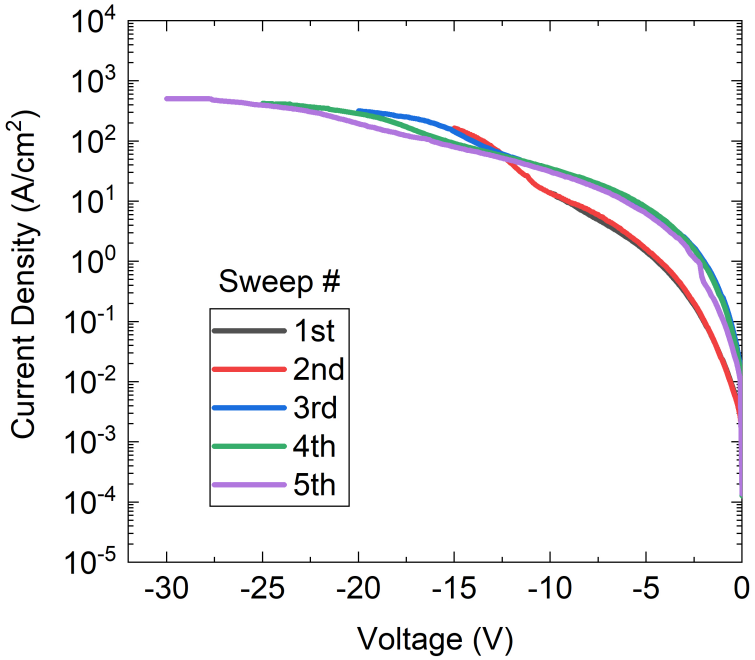

Figure 3.4: Multiple reverse bias I-V sweeps on the as-grown N-polar GaN surface Schottky diode measured at room temperature.

characteristics (Figs. 3.3(c), 3.3(d)) reveals that the barrier height is 0.40 eV with a spread of ±0.03 eV, which is similar to the I-V-T barrier height value reported by Osvald *et al.* [133]. A proposed explanation for the difference in barrier heights extracted via I-V and C-V is presented in next Section 3.4.

Figure 3.4 shows multiple reverse bias IV sweeps up to -30 V. Due to the low Schottky barrier (0.4 eV) and higher doping levels (7×10^{17} cm^{-3}) compared to the standard high-power diodes, the leakage current levels in these diodes are very high. As a result, the current level reaches compliance at a very early reverse bias voltage of -30 V, although the device does not break down.

3.3.2 Solvent-treated Schottky Diodes

AFM and SEM images of the solvent-treated samples (Figs. 3.5(a)- 3.5(d)) showed similar step flow or step bunching to the as-grown samples. Additionally, Figs. 3.5(e) and 3.5(f) depict XPS of these samples where the O 1s peak percentages are comparable to the as-grown peak percentage, indicating that the oxygen oxidation state did not change with the solvent-based chemical treatments.

The forward bias I-V of solvent-treated diodes showed similar behavior to the as-grown samples, as shown in Fig. 3.6(a). The ideality factor of these diodes is n ~1.1. The C-V barrier heights of IPA and MIBK-IPA treated diodes, Fig. 3.6(b), are 0.60 eV and 0.61 eV, respectively. The temperature-dependent I-V barrier heights of the IPA and MIBK:IPA

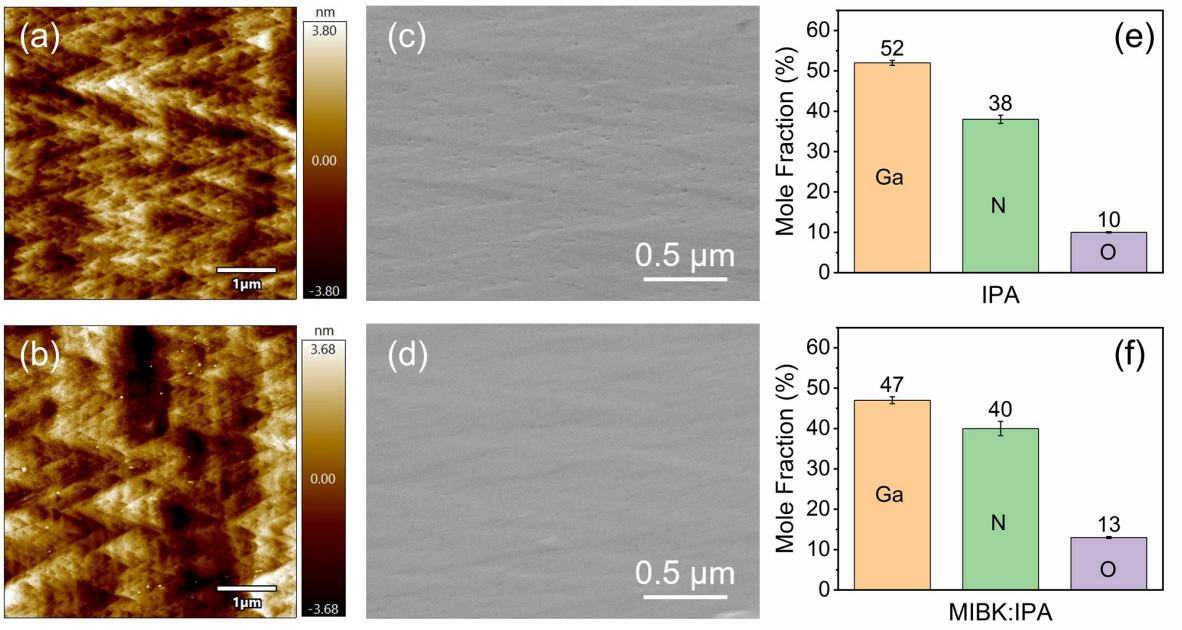

Figure 3.5: (a & b) AFM, (c & d) tilted-view SEM images, and (e & f) the mole fraction (in %) of Ga, N, and O for the 1 min IPA and 1 min MIBK:IPA (e-beam resist developer) treated samples, respectively.

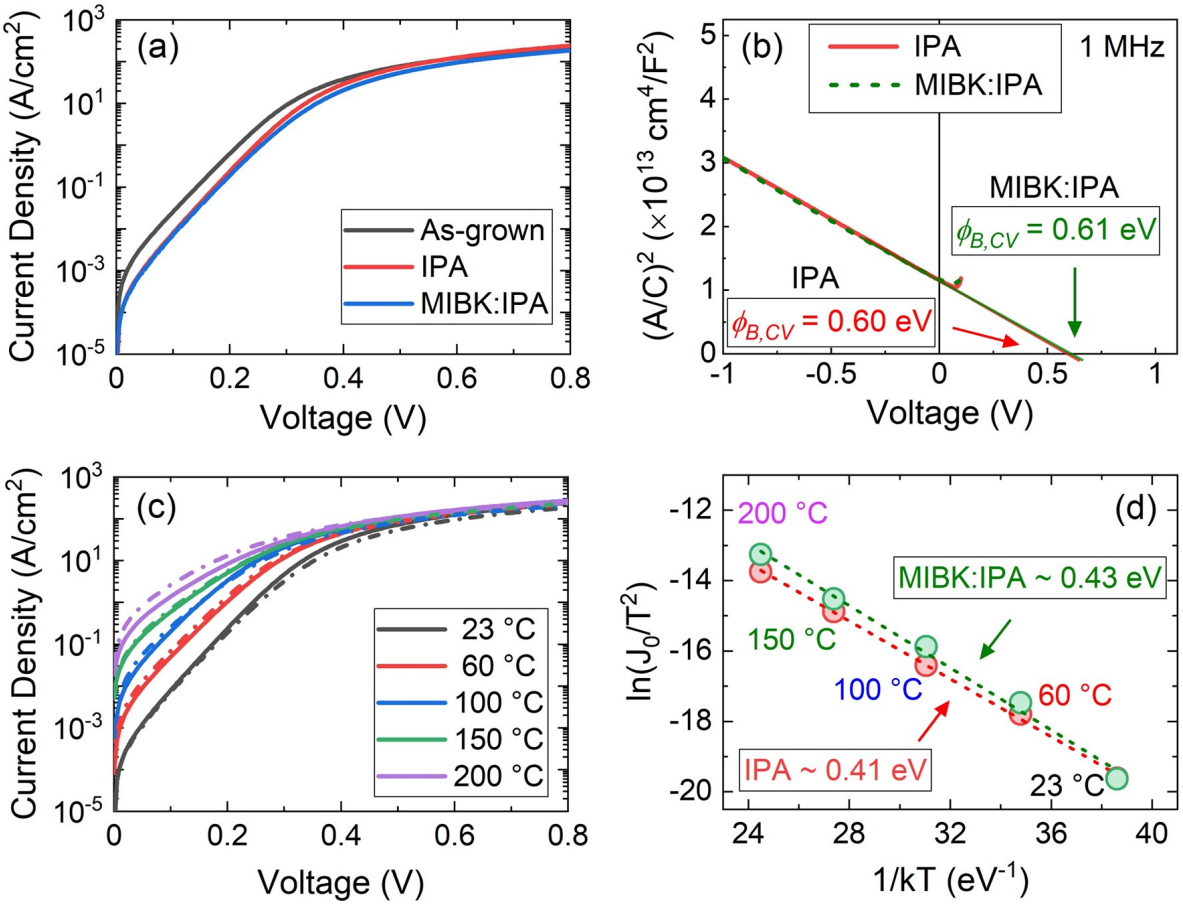

Figure 3.6: Room temperature (a) forward bias current-voltage (I-V), (b) capacitance-voltage (C-V) (solid: IPA and dash: MIBK:IPA), (c) temperature-dependent I-V characteristics (solid: IPA and dash: MIBK:IPA), and (d) Richardson plot for IPA and MIBK:IPA treated Ni/N-polar GaN Schottky diodes.

treated diodes are 0.41 eV and 0.43 eV, shown in Figs. 3.6(c) and 3.6(d), with a measured spread amongst diodes of around ±0.03 eV. The barrier height values from I-V and C-V for the solvent-treated diodes are similar to the as-grown diodes. Thus, solvent-based chemical treatments do not alter the N-polar GaN surface.

3.3.3 Base-treated Schottky Diodes

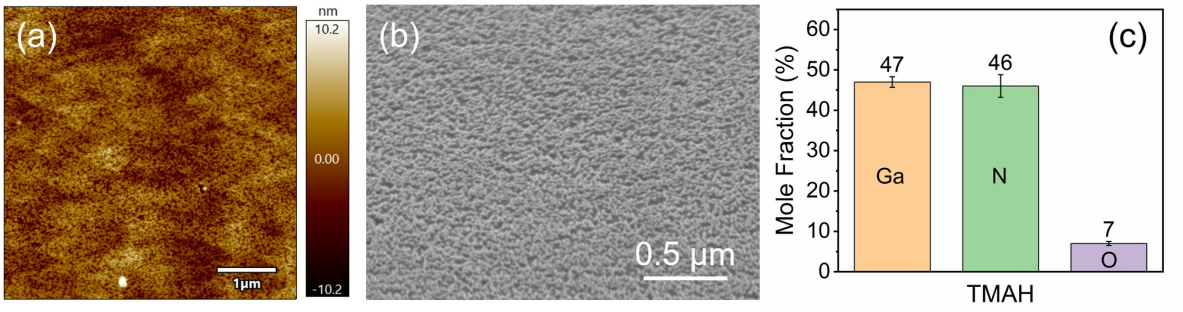

Figure 3.7: (a) AFM, (b) tilted-view SEM images, and (c) the mole fraction (in %) of Ga, N, and O for the 1 min 3% TMAH (photoresist developer) treated sample.

Per the AFM and SEM images of the TMAH-treated sample in Figs. 3.7(a) and 3.7(b), an increase in surface roughness compared to the as-grown samples is observed. High-resolution SEM indicates that base treatment roughened the N-polar surface by creating triangular/hexagonal features with crystallographic facets different from the flat N-polar surface. XPS was used to determine if the newly exposed facets represented bare or oxidized GaN. According to Fig. 3.7(c), it is found that the oxygen mole fraction on these surfaces is low compared to the surface of the as-grown samples. This indicates that the crystallographic facets may not be covered with a significantly thick oxide layer. Moreover, we expect these sidewalls to be semi-polar/non-polar with different properties than the top N-polar GaN surface [44]. This is further discussed in Section 3.4.

The room-temperature forward-bias I-V, Fig 3.8(a), showed that the current in the TMAH-treated sample is lower than the as-grown sample. The ideality factor of the TMAH-treated diode is n ∼1.15, which also suggests the minor or insignificant presence of a treatment-induced surface oxide barrier. As shown in Fig. 3.8(b), the C-V barrier height following base treatment is 0.98 eV, which is ∼0.38 eV higher than the as-grown C-V barrier height. The

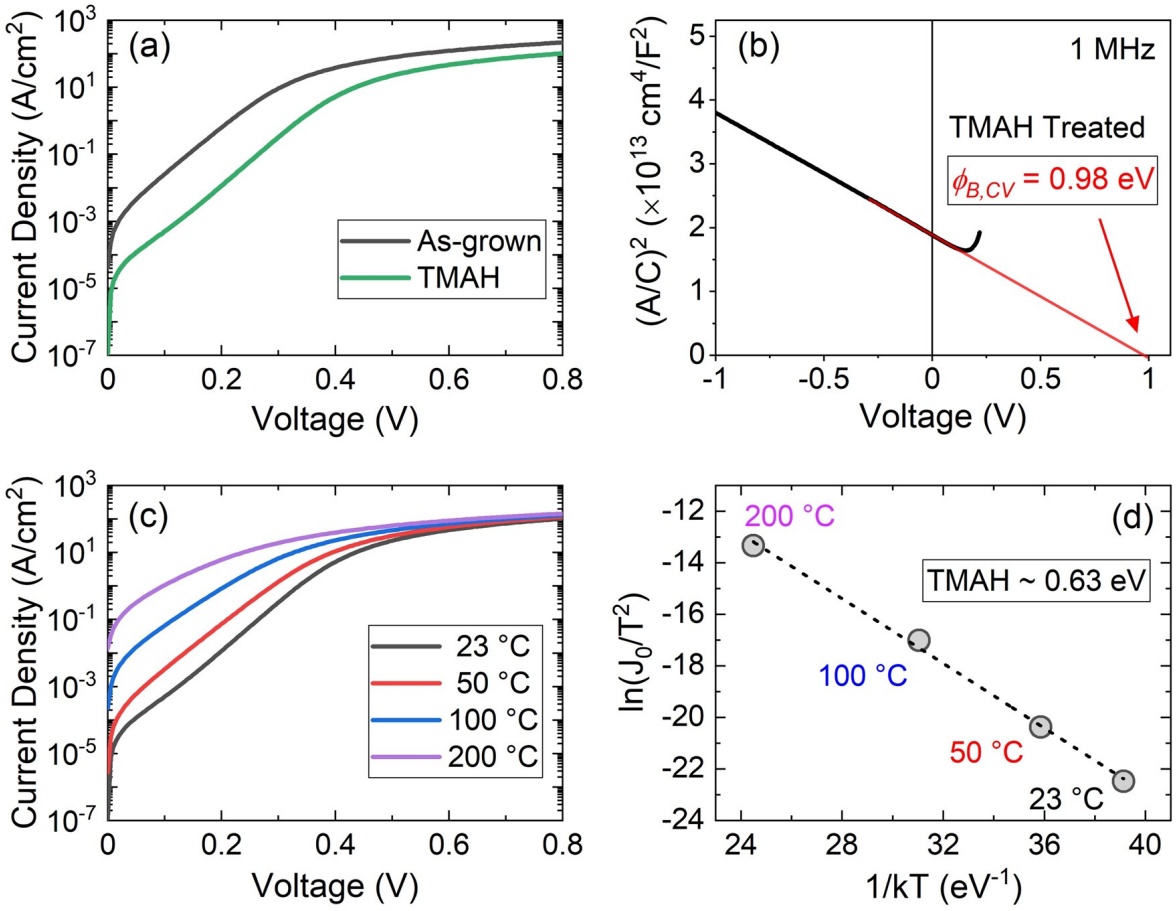

Figure 3.8: Room temperature (a) forward bias current-voltage (I-V), (b) capacitance-voltage (C-V), (c) temperature-dependent I-V characteristics, and (d) Richardson plot for TMAH treated Ni/N-polar GaN Schottky diodes.

temperature-dependent I-V barrier height, Figs. 3.8(c) and 3.8(d), of the TMAH-treated sample is 0.63 eV with a spread of ±0.03 eV, which is ∼0.23 eV higher than the as-grown samples.

3.3.4 Acid-treated Schottky Diodes

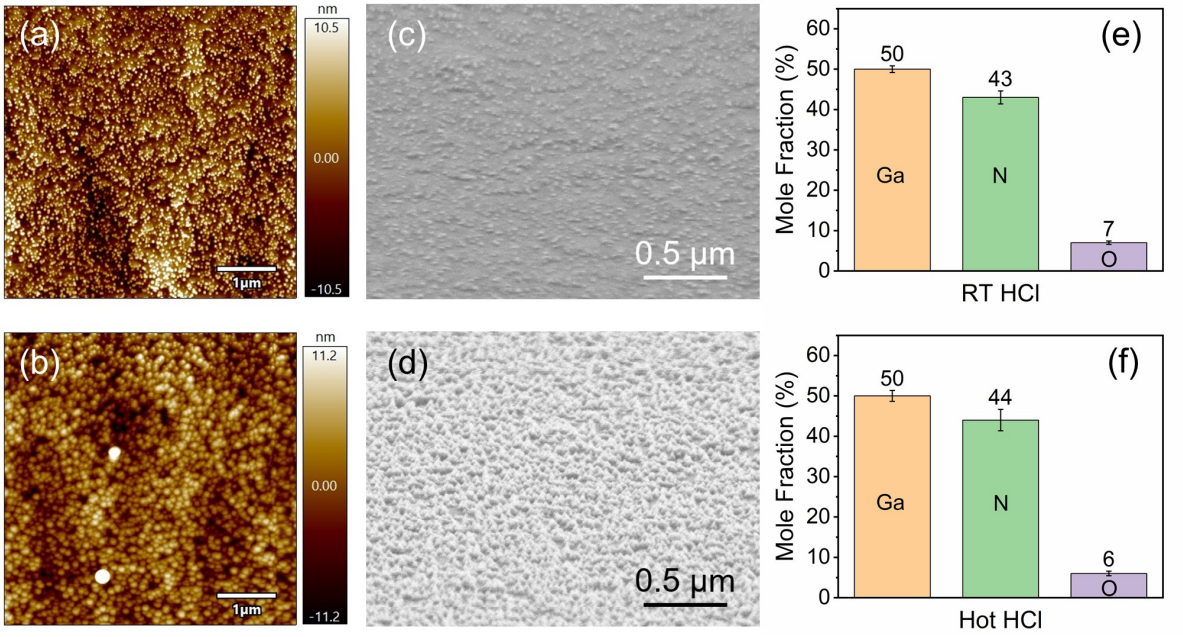

Figure 3.9: (a & b) AFM, (c & d) tilted-view SEM images, and (e & f) the mole fraction (in %) of Ga, N, and O for the 1 min room temperature HCl and 1 min hot (75 °C) HCl treated samples, respectively.

Figures 3.9(a) and 3.9(b) represent AFM images of the room-temperature HCl treated and hot HCl treated N-polar GaN surfaces, respectively. Compared to the other chemical treatments, it is found that acid exposure most severely etches the surface, especially when hot acid is used. Furthermore, from the SEM images, Figs. 3.9(c) and 3.9(d), it appears that the acid treatment creates triangular/hexagonal crystallographic facets on the surface similar to the base treatment. XPS performed on the acid-treated samples, shown in Figs. 3.9(e) and 3.9(f) indicate that the crystallographically etched GaN surface may have less oxygen atomic coverage than the as-grown surface.

Figure 3.10(a) represents the room temperature forward bias I-V comparison between acid-treated and as-grown sample Schottky diodes. It is seen that the hot HCl treated diodes

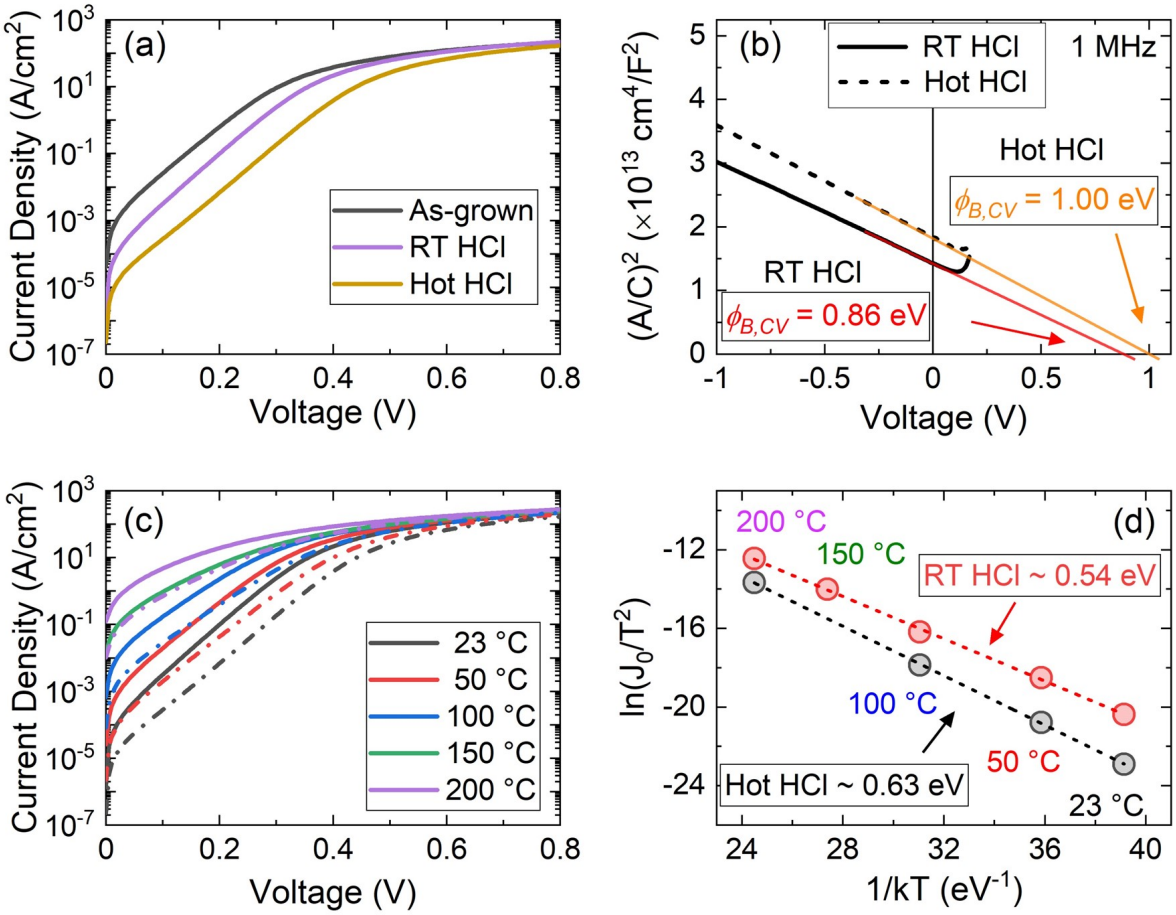

Figure 3.10: Room temperature (a) forward bias current-voltage (I-V), (b) capacitance-voltage (C-V) (solid: RT-HCl and dash: hot-HCl), (c) temperature-dependent I-V characteristics (solid: RT-HCl and dash: hot-HCl), and (d) Richardson plot for RT and hot HCl treated Ni/N-polar GaN Schottky diodes.

showed the lowest current, whereas the RT HCl treated diodes showed slightly higher current than hot HCl, but it is still lower than the as-grown diodes. The ideality factor of RT HCl treated diode is n ∼1.13, and hot HCl treated is n ∼1.17. Again, the ideality factor values of the diodes show that the surface of the facets was not oxidized significantly and support our XPS observations. As shown in Fig. 3.10(b), the C-V barrier height for the hot-HCl-treated diodes is 1.00 eV, whereas for the RT HCl-treated diodes is 0.86 eV. These barrier

height values for acid-treated samples are higher than the as-grown sample surface diodes. Figures 3.10(c) and 3.10(d) show the temperature-dependent I-V characteristics for RT and hot HCl treated diodes. The extracted I-V barrier height for RT and hot HCl treated diodes is 0.54 eV and 0.63 eV, respectively, which is higher than the as-grown samples. The spread in barrier heights across the diodes for acid-treated samples was ± 0.03 eV. As with the case of base treatment, we expect the surface of the exposed facets would be semi-polar/non-polar GaN rather than the N-polar GaN.

3.4 Discussion

The I-V-extracted barrier height of the as-grown N-polar GaN samples is 0.40 eV, which is lower compared to what Kim *et al.* [128] reported for nonpolar a-plane GaN (0.51 eV) and Reddy *et al.* [125] (0.70 eV) reported for Ga-polar GaN. This difference of 0.30 eV between Ga- and N-polar GaN surfaces is consistent with the literature and has been attributed to the different polarization-induced charges at the different GaN polar surfaces [119, 129]. Theoretical calculations, for example, performed by Rizzi and Luth [131], predicted a 0.33 eV barrier height difference, which aligns with our results. Via a combination of AFM and SEM, we have observed that solvent treatment does not modify the surface morphology of the N-polar GaN surface. Electrical characterization also confirms that the Schottky barrier height of solvent-treated samples does not significantly change with respect to the as-grown samples. However, it has been found that base and acid treatments severely roughen the N-polar GaN film by creating triangular and hexagonal crystallographic facets on the surface. The peak-to-valley roughness (R) for each chemical treatment is shown in Table 3.2. The barrier height of these samples increased with respect to the as-grown case, yet XPS precludes the formation of a thick oxide as a cause for the change since the O molar fraction remained

Table 3.2: Summary of extracted Schottky barrier height using C-V ($\phi_{B,CV}$) and I-V-T ($\phi_{B,IV}$) methods and calculated interlayer dielectric thickness (δ) for different chemical treatments. R denotes peak-to-valley roughness, n denotes ideality factor at room temperature, $\Delta\phi_{B,IV}$ denotes the barrier height lowering, CF denotes a correction factor we apply to account for surface roughness effects, and t_{SCL} denotes the thickness of the space charge layer at zero-bias voltage.

Treatment	**R**	$\mathbf{N_D}$	$\phi_{B,CV}$	$\phi_{B,IV}$	$\boldsymbol{n}$	$\Delta\phi_{B,IV}$	**CF**	$\mathbf{C_{eff}}$	$\mathbf{t_{SCL}}$	δ
	(nm)	**(cm^{-3})**	**(eV)**	**(eV)**		**(eV)**		**(F/cm^2)**	**(nm)**	**(nm)**
as-grown	2	7.4×10^{17}	0.60	0.40	1.07	0.067	1	3.1×10^{-7}	27	0.3
IPA	2	7.0×10^{17}	0.60	0.41	1.1	0.066	1	2.9×10^{-7}	28	0.3
MIBK	2	7.1×10^{17}	0.61	0.43	1.1	0.067	1	2.9×10^{-7}	28	0.3
TMAH	14	7.1×10^{17}	0.98	0.63	1.15	0.074	2	2.3×10^{-7}	36	0.4
RT HCl	13	8.3×10^{17}	0.86	0.54	1.13	0.074	2	2.6×10^{-7}	31	0.4
Hot HCl	20	7.6×10^{17}	1.00	0.63	1.17	0.075	2	2.3×10^{-7}	34	0.5

below the monolayer limit. Instead, we hypothesize that the exposed crystallographic facets are semi-polar/non-polar GaN surfaces that increase the barrier height compared to the original N-polar surface. Therefore, the increase in the Schottky barrier height following base and acid treatments is dominated by the polarity differences of these surfaces. The ideality factor measured at room temperature for different treatments is shown in Table 3.2. Again, the ideality factors for base and acid treated samples remain less than 1.2, which is in accordance with XPS measurements and suggests that the higher barrier height is not due to the thick native oxide on the surface.

The extracted barrier heights using I-V-T and C-V methods for the different chemical treatment samples are listed in Table 3.2. As noted previously, both the C-V- and I-V-extracted barrier heights increased in the samples that underwent base and acid treatments. It is also seen that the C-V barrier height value in all samples is ∼50% higher than the

I-V-T barrier height; similar results have been reported in both Ga-polar and N-polar GaN Schottky diodes previously [117, 119, 125, 133]. There are several reasons for such an outcome, which can be explained to first order. Firstly, C-V measures the flat band condition barrier height, whereas I-V measures the barrier height at zero-bias voltage, which would be lower than the flat band condition due to the barrier height lowering [126]. In addition, C-V is more sensitive to barrier height changes due to the possible presence of a thin interlayer dielectric between the metal and semiconductor [126]. Finally, if barrier height inhomogeneity exists, the effective I-V barrier height is expected to be lower than the effective C-V barrier height [148–150]. However, barrier height inhomogeneity is expected to result in a temperature-dependent barrier height [148] and not the practically temperature-independent barrier height we observed up to 200 °C, as seen in Figs. 3.3, 3.6, 3.8, and 3.10.

From Table 3.2, it is also observed that the C-V barrier height values are once again higher for base- and acid-treated samples than for the as-grown and solvent-treated samples. One could argue that the higher barrier height in C-V could be because of a thick surface oxide grown on the unstable etched/roughened GaN surface after the base and acid treatments in this work. We instead attribute the barrier height increase to surface roughening caused by base and acid treatments, which exposes semi-polar/non-polar GaN facets with higher barrier heights compared to the original N-polar GaN surface. This hypothesis is supported by our XPS measurements, which point to a decrease in the oxide thickness when acid or base treatments are used. As previously mentioned, the barrier height differences are also consistent with previous experimental and theoretical reports. However, the difference between C-V and I-V barrier heights is larger for the samples subjected to acid and base treatments even though there is a reduction in the interfacial layer thicknesses, as seen by XPS.

In order to support the hypothesis that the increase in barrier height is due to the exposure of semi-polar/nonpolar GaN facets due to the roughening and electrical analysis-

based estimation of the potential oxide thickness that could grow due to the base/acid treatment is needed. Based on this hypothesis, a similar oxide thickness to the one on as-grown or solvent-treated diodes is expected. For the electrical-based estimation, we employ a first-order analysis to calculate the equivalent thickness of the interlayer dielectric for each treatment case. For this, we need to consider and correct the contributions to the barrier height from image forces and any other deviations from a flat surface assumption. We first calculate the contribution of image force lowering using the following equations:

$$\Delta\phi_{B,IV} = \sqrt{\frac{qE_M}{4\pi\varepsilon_S}} \tag{3.3}$$

and,

$$E_M = \sqrt{\frac{2qN_D\,\phi_{B,IV}}{\varepsilon_S}} \tag{3.4}$$

where, $\Delta\phi_{B,IV}$ is the barrier height lowering in eV, E_M is the maximum electric field at zero-bias voltage, $\phi_{B,IV}$ is the barrier height in eV extracted using the I-V-T method, N_D is the net doping concentration in the n-type region, and ε_S ($= 10.4\varepsilon_0$) is the permittivity of GaN. The values for $\Delta\phi_{B,IV}$ for each treatment were calculated using the doping value extracted from respective $1/C^2$-V measurements and are in general less than 75 meV, as seen in Table 3.2. It should be noted that Eqs. 3.3 and 3.4 assume that the Schottky diode's surface is smooth and uniform, which is not the case for the samples exposed to acid and base treatments, based on evidence from AFM and SEM.

Therefore, to consider the effect of surface roughness in the barrier height lowering, two-dimensional (2D) numerical simulations were done with Silvaco ATLAS, comparing the electric field at zero bias in smooth and rough surface Schottky diodes, as shown in Figs. 3.11(a) and

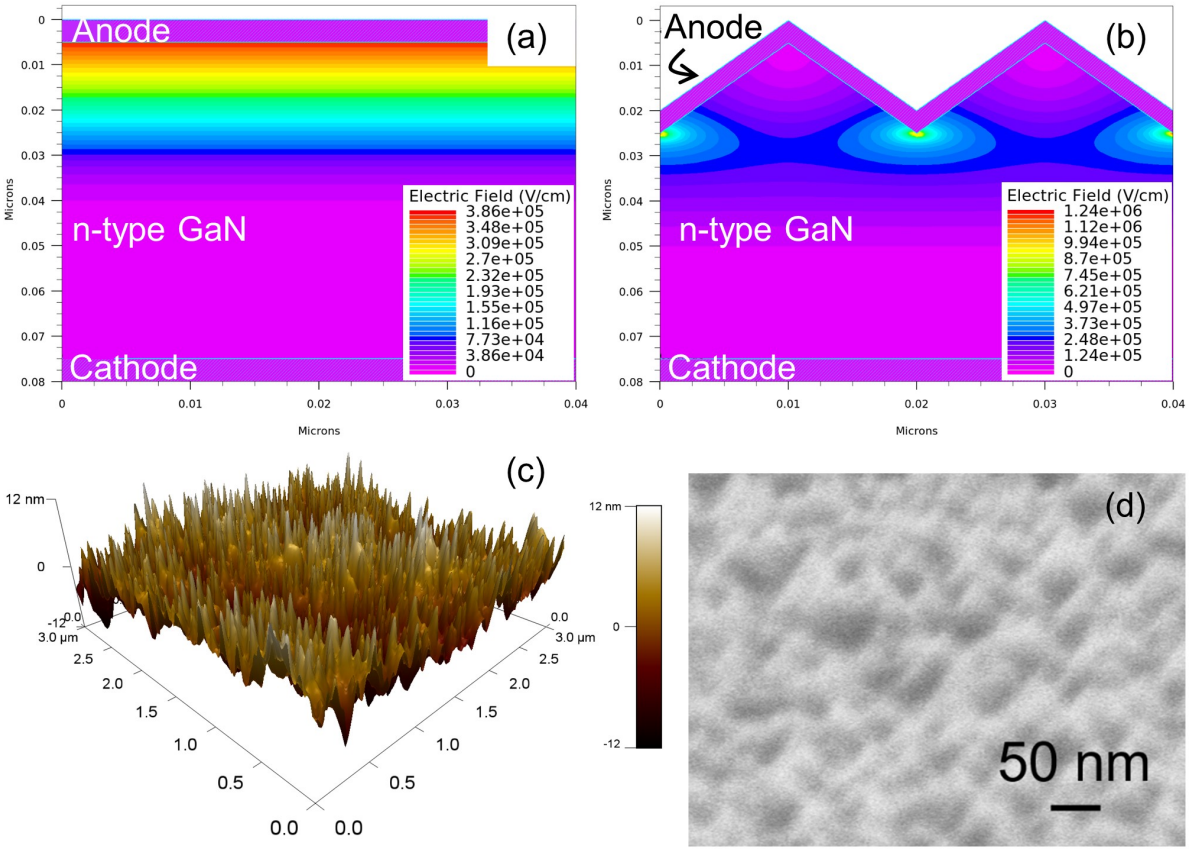

Figure 3.11: The E-field profile of simulated Schottky diodes with (a) smooth surface and (b) rough surface at zero bias voltage. (c) Three-dimensional AFM and (d) tilted-view SEM image of the surface morphology of Hot HCl treated sample.

3.11(b). A barrier height of 0.63 eV was assumed for both cases, corresponding to $\phi_{B,IV}$ of the hot HCl-treated diodes. This was included in the simulation as the difference between the anode metal work function and the electron affinity of the GaN. Three-dimensional AFM and SEM micrographs, Figs. 3.11(c) and 3.11(d), show that the crystallographic features can have different sizes and angles, ranging from tens to hundreds of nm. Thus, in order to illustrate the barrier height lowering dependence on roughness, we have chosen the size of the feature to be 20 nm with an angle of 60°. The doping value used for the simulations is 7.5×10^{17} cm^{-3}. The simulation results show that the maximum electric field at the zero-bias

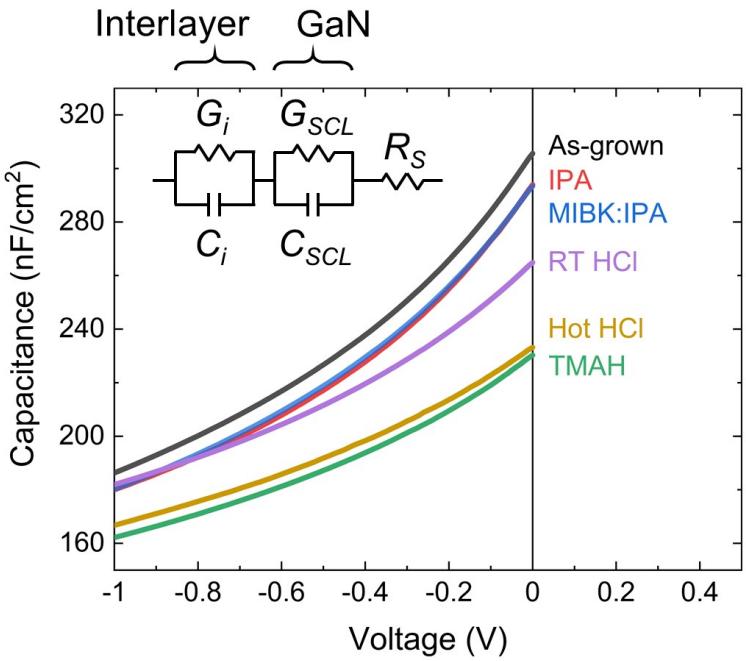

Figure 3.12: Capacitance-voltage (C-V) measurements for different chemical treatments. The inset image on the top-left of the graph represents the equivalent circuit model for the measured capacitance. The equivalent circuit consists of a series combination of two parallel G-C pairs for the interlayer dielectric and GaN space charge layer, respectively, as well as the series resistance associated with lateral contacts. Here, G denotes conductance, C denotes capacitance, and RS denotes series resistance.

voltage in the rough surface diode is approximately 4-times higher than in the smooth surface diode. Since, per Eq. 3.3, $\Delta\phi_{B,IV}$ is proportional to $\sqrt{\mathrm{E_M}}$, we expect that the image force barrier lowering for the base and acid-treated surfaces could be two times higher than the theoretically calculated values using Eqs. 3.3 and 3.4. To account for this, we introduce a correction factor (CF) in Table 3.2, which is used in the subsequent calculations.

The interlayer dielectric thickness can be estimated using the effective capacitance measured at a zero-bias voltage from the C-V graph. The C-V measurements for different chemical treatments are shown in Fig. 3.12. It should be noted that this effective capacitance would be the series combination of interlayer dielectric capacitance and space charge layer capacitance

present at zero-bias voltage. The equivalent circuit model for the measured capacitance is shown in the inset of Fig. 3.12. Therefore, the effective capacitance can be written as:

$$\frac{1}{C_{eff}} = \frac{1}{C_{SCL}} + \frac{1}{C_i} \tag{3.5}$$

where, C_{eff} is the effective capacitance measured at zero-bias voltage, C_{SCL} is the space charge layer capacitance at zero-bias voltage, and C_i is the interlayer dielectric capacitance. The space charge layer thickness (t_{SCL}) in GaN at zero-bias voltage can be calculated using the following equation:

$$t_{SCL} = \sqrt{\frac{2\varepsilon_S \left(\phi_{B,IV} + CF \times \Delta\phi_{B,IV}\right)}{qN_D}} \tag{3.6}$$

where $\phi_{B,IV}$ is barrier height extracted using the I-V-T method, $\Delta\phi_{B,IV}$ is barrier height lowering, CF is the correction factor which we apply to account for surface roughness effects, and N_D is the doping in the n-type region. Thus, the interlayer dielectric thickness (δ) is calculated using:

$$\delta = \varepsilon_i \left[\frac{1}{C_{eff}} - \frac{t_{SCL}}{\varepsilon_S}\right] \tag{3.7}$$

where ε_i ($= 1\varepsilon_0$) is the effective permittivity of the interlayer dielectric. Table 3.2 summarizes the interlayer dielectric thicknesses for each treatment case. It should be noted that the dielectric constant 1.0 is used to calculate the interlayer thickness as the coverage of the grown oxide would probably be non-continuous or patchy, and the oxide would be porous. As shown in Table 3.2, the dielectric layer thicknesses for the as-grown and solvent treated samples are similar, which is in accordance with the XPS results. By contrast, δ is larger

for the base and acid-treated samples, which is not consistent with XPS. The XPS results suggest that the amount of surface oxygen is reduced for the base and acid-treated diodes, in contrast to the as-grown and solvent-treated ones. This trend is opposite to the expected slight increase in dielectric layer thickness based on the C-V measurements for the electrical-based analysis. We propose that an overestimation of interlayer dielectric thickness occurs due to the underestimation of the space charge layer thickness for the base and acid treatments since Eqs. 3.5, 3.6, and 3.7 assume a flat surface. If the surface roughness is accounted for, as in Fig. 3.11(b), the estimated space charge layer thickness is found to increase, which can be represented by a third series capacitance. It should be noted that a strong relationship exists between δ and t_{SCL}: according to Eq. 3.7, a smaller than 10% increment in the space charge layer thickness would result in estimated interlayer dielectric thicknesses that are significantly lower than the reported values in Table 3.2 for base- and acid-treated cases. For a detailed understanding, a forward bias capacitance study with impedance spectroscopy would have been required, which is left for future work. Thus, it is evident from this electrical-based analysis that the higher I-V and C-V barrier height for the base- and acid-treated surfaces are not due to the thicker interlayer dielectric layer. This supports the general hypothesis that the increase in barrier height is due to the exposure of semi-polar/nonpolar GaN facets. Further evidence of this could be obtained by measuring the areal density of the observed facets and consequently relating the crystallographic planes of these facets to their specific barrier height and density.

3.5 Conclusion

To summarize, the choice of chemical treatment prior to Schottky metal deposition on N-polar GaN impacts the electrical behavior of these contacts. It is observed that solvent-based treatment (i.e., MIBK and IPA) results in minimal change to the material's surface roughness. In contrast, exposure to acid (pH < 1) and base (pH $= 13$) treatments etch the surface and increases roughness, exposing semi-polar planes. The barrier height is found to increase as the surface roughness increases, thus changing the I-V behavior. Since XPS measurements rule out the presence of a significant surface oxide with thickness dependence on chemical treatment, it is proposed that the increased barrier height arises from exposed facets that present a mixture of N-polar and semi-polar crystal faces to the metal contact. It is also observed that the difference between I-V- and C-V-extracted barrier heights increases as the surface roughness increases. By modeling the surface, we demonstrate that this could be explained by field enhancement and subsequent barrier lowering as measured by I-V. The results of this study underline the critical role played by common processing chemicals in determining the performance of N-polar GaN devices. The chemical sensitivity of N-polar GaN makes it a challenging material to work with and demands advanced approaches to stabilize the surface in order to achieve ideal behavior.

In general, the measured Schottky barrier height of N-polar GaN is very low compared to Ga-polar GaN and SiC diodes. This is a major impediment for device applications, as it increases the leakage current and makes the device less thermally stable. Therefore, further studies are required to find solutions that increase the barrier height and stabilize the surface chemically.

Chapter 4

SiN-based Schottky Contacts for Barrier Height Control and Thermal/Chemical Stability

From the results in the previous chapter, it is evident that the N-polar GaN Schottky diodes have a very low barrier height compared to Ga-polar GaN [125] and SiC [151] Schottky diodes. Also, due to the highly reactive nature of the surface, standard photolithography processes may damage the surface, thereby making it difficult to achieve ideal device performance. One alternative to stabilize the surface and achieve high barrier height can be the realization of dielectric-assisted Schottky diodes. In recent studies, an ultra-thin layer of SiN realized via low-pressure chemical vapor deposition (LPCVD) has been used to passivate the GaN as well as GaN-based HEMT surfaces [135, 152, 153]. The key lies in the concept of using SiN as a dielectric with a point defect level of high density above 10^{19} cm^{-3}, forming a defect band aligned with the semiconductor conduction band edge to deposit the polarization countercharge within the tunneling distance from interface [135, 153, 154]. Before depositing SiN, an in-situ cleaning step inside the LPCVD chamber (above 700 °C) in NH_3 helps to remove a few monolayers of the native interfacial oxide layer, which helps to obtain ideal interface properties between the SiN and GaN [135, 153, 154].

Therefore, in this chapter, LPCVD SiN is deposited to stabilize the N-polar GaN surface and control the barrier height for potential use in GaN SJ devices. This chapter is divided into three parts. The first part presents a historical perspective of SiN and the literature on the

properties, interface analysis, and concept of SiN when deposited on GaN. The second part unveils the properties of thin LPCVD SiN deposited on N-polar GaN. To do that, 7 nm of LPCVD SiN was chosen, which is beyond that of a pure tunneling barrier, making it akin to a metal-insulator-semiconductor (MIS) system. At last, in the third part, 5 nm thin LPCVD SiN is deposited on N-polar GaN to obtain high-performance N-polar GaN Schottky contacts. This SiN interlayer helps tune the barrier height, reduces reverse bias leakage, and allows reliable operation at elevated temperatures. Parts of the results presented in this chapter are reported in our recent publications [135, 154].

4.1 Part-I: Background on SiN Technology

4.1.1 History of SiN

The deposition of amorphous SiN thin films on Si started to be reported in the mid-1960s using two techniques. First, using radio frequency (RF) discharge promoted chemical vapor deposition (CVD) at temperatures above 200 °C, which developed into plasma-enhanced CVD (PECVD) [155]. And second, using CVD at temperatures above 700 °C, developing into low-pressure CVD (LPCVD) [156]. In an early study on CVD, the temperature range was scanned from 600 °C to above 1200 °C, when crystallites appeared. Such amorphous SiN was used as a mask for thermal gate oxide growth in metal-oxide-semiconductor field-effect transistors (MOSFETs) and as a cap-layer in the high-temperature damage anneal of ion-implanted patterns. It showed exceptional stability and diffusion barrier characteristics. Crystalline Si_3N_4 phases, such as α (trigonal) and β (hexagonal), formed only above 1327 °C [157].

This changed in the 1970s, particularly with the development of metal-oxide-semiconductor (MOS) storage transistors, where nm thin SiN charge storage layers were inserted into MOS

structures with SiO_2 or Al_2O_3 tunneling barriers, like those reported at the IEDM 1974 by Van Overstraeten [158]. The entire materials structure was amorphous. The intermediate SiN was used for charge storage and thus appeared heavily trap-loaded. It contained disorder-induced band edge tails and a high density of deep levels up to the concentration when defect bands could form. In these structures, it became an electrically functional material in the active area of the FET device structure beyond that of electrical, chemical, and mechanical surface passivation. This application triggered continuous efforts to identify and analyze defect structures in SiN both experimentally [159] and theoretically [160–163] through density functional theory (DFT). However, atomistic modeling was widely based on crystalline phases like the α-Si_3N_4 and β-Si_3N_4, and the correlation with amorphous film properties was complex. Nevertheless, these results gave essential inputs for the SiN_x on GaN study discussed below.

III–V materials whose surface electronic properties and chemical reactivity were highly dependent on surface facets, polarization and counter charges, and oxidation states, all of which are interdependent and dependent on surface treatments appeared for high-speed applications [130, 153, 164–168]. High-temperature processing in such a material system was more challenging. Thus, as related to SiN_x, there were two mainstream deposition technologies: LPCVD at high temperatures (700 to 900 °C) and PECVD at moderate or mid temperatures (250 to 350 °C). The mid-temperature techniques were quickly adopted for GaAs and InP; they also included remote plasma generation to minimize surface damage. PECVD Si-nitrides could, however, be somewhat different in their composition and electronic behavior, depending on the precursors and reactions involved. Usually, Si would be supplied by SiH_4 or $SiCl_2H_2$ and nitrogen by NH_3 or N_2. The equipment was typically designed to operate in a temperature range below 350 °C, limited by the thermal stability of the seals used in the deposition chambers. However, in this temperature regime, NH_3 may not totally crack into N^* (nitrogen free radicals) and H^* (hydrogen free radicals). Instead, intermediate reactions products may

form in the gas phase as described by the following intermediate reactions [169]:

$$SiH_4 + NH_3 \rightleftharpoons SiNH + 3H_2 \tag{4.1}$$

and,

$$2SiH_4 + N_2 \rightleftharpoons 2SiNH + 3H_2 \tag{4.2}$$

Thus, NH-radicals could be incorporated depending on the gas phase composition, chamber temperature, and pressure, resulting in the material usually labeled as 'H-rich'-SiN. On the other hand, not all Si-bonds in the Si_3N_4 matrix may become saturated, and Si-related defects and clusters would remain. This material was usually labeled as 'Si-rich'-SiN. Over the last two decades, the mainstream technology for III-nitrides has also been RF-enhanced PECVD at mid-temperatures with SiH_4 or Si_2ClH_2 and NH_3 or N_2 as precursors. Recently, however, high-temperature LPCVD has become of interest.

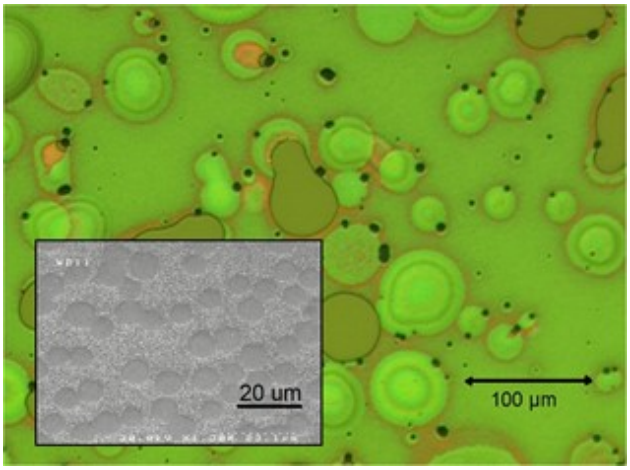

Figure 4.1: Optical and SEM (inset) micrograph of H-rich SiN capped with 50 nm of sputtered Si and then annealed at 650 °C. Figure from [135].

PECVD SiN could result in H-rich SiN. In that case, the SiN would densify during high-temperature treatments, and H would outgas. If coated with a non-transparent cap (like sputtered Si or nanodiamond), this process can be observed as bubble formation and cracking (see Fig 4.1). Thus, the H- (or rather NH-radical-) content could be substantial in PECVD grown SiN. In contrast, Si-rich SiN remains stable with temperature. However, if the material became excessively Si-rich, Si would cluster, and the appearance would become grainy. In contact with metals, a silicide could form, making the film slightly conductive. In the case of LPCVD, which operates at temperatures above 700 °C, all NH_3 is expected to split, and intermediate radicals are unlikely to be incorporated. Thus, LPCVD SiN should not be H-rich. Thus, LPCVD SiN would not suffer from H-outgassing or be excessively Si-rich.

4.1.2 Historical Perspective of SiN on GaN

The GaN-based materials platform was the first polar semiconductor materials platform extensively used in electronics. The Ga-polar surface of the wurtzite phase with a strong vertical polarization field is almost exclusively used in GaN high electron mobility transistor (HEMT) technologies. In AlGaN/GaN heterostructures [170], the (differential) bound polarization charge density at the surface and interface is in the order of 10^{13} cm^{-2}, inducing surface countercharges of the same magnitude to maintain charge neutrality. In Ga-polar HEMTs, the interfacial countercharge is the negative 2DEG (2D electron gas) used as the HEMT channel. The positive surface countercharge can be located in surface states, in the passivation dielectric, on the surface of the passivation dielectric, or in adsorbates. In equilibrium, and as long as a field-effect transistor (FET) channel current is present, the surface is charged [171]. A similar conclusion was arrived at by surface Fermi level measurements via x-ray photoelectron spectroscopy (XPS) studies [130].

The situation may be reflected on by the following two results published in 2000. In the

first result, the potential of the free surface on an $Al_{0.3}Ga_{0.7}N$/GaN heterostructure was investigated by Ibbetson *et al.* in 2000 [170], analyzing HEMTs with different AlGaN barrier layer thicknesses, and determined to be approximately 1.65 eV for an AlGaN barrier of 30% Al-content. In their analysis, the surface trap, labeled as a surface donor, was ionized when the FET 2DEG channel was fully developed and would gradually be filled with electrons when the FET was driven into pinch-off. Switching the device on, electrons would be emitted, following their emission/capture dynamics. Thus, this region would act as a distributed second gate and essentially as a current limiter and was thus labeled 'virtual gate' or 'slow gate', giving rise to current clipping and power slump effects.

The second report was from Green *et al.*, also in 2000 [172]. The investigation showed that the deep surface donor trap and the related 2DEG depletion effect could be removed by SiN passivation, the SiN being deposited by PECVD. Depletion mode devices could be switched on without delay. It was thought that deep surface states were H-passivated. Unfortunately, H-passivation is not reliable on wide bandgap semiconductor surfaces with desorption occurring at relatively low processing temperatures of 300 to 400 °C [173, 174]. Many experiments with a large number of dielectrics, including gadolinium and scandium oxides in addition to more 'traditional' choices such as SiO_2 and Al_2O_3, have followed, often claiming the removal of the current slump phenomenon, however, generally, only for the specific experiment discussed [175–183]. If the picture of a deep surface donor state being the source of the 2DEG applies, GaN-based HEMT's have to generally cope with its charging/discharging characteristics, and stable performance, in general, may remain out of reach.

Interestingly, SiN deposition by LPCVD was also already reported in 2003 by Shealy *et al.*, where SiN was deposited at 700 °C [152]. Their report concluded that, in the HEMT structure, the depletion of the underlying 2DEG was virtually eliminated, and the surface polarization

charge would reside as a fixed charge in the SiN (and not in a surface donor). This was an important result, but not many details were given, and the technology did not mature to a mainstream technology in GaN-based HEMTs.

4.1.3 SiN on Al(GaN) – Properties, Interface Analysis, & Concept

As mentioned above, amorphous SiN is a heavily trap-loaded dielectric with defect centers well analyzed, characterized, and calibrated in Si-MOS memory device technologies [156, 184–187]. Depending on the deposition parameters, Si-rich and H-rich compositions are obtained [169, 188–191]. Band tails and defect-related trap levels in the upper and lower half of the bandgap have been identified by electrical and optical analyses as well as by atomistic modeling [156, 161, 162, 184–187, 192]. In many cases, the Fermi level can be identified and located in the upper or lower half of the bandgap, making the material either n-type or p-type. Depending on stoichiometry, the electronic bandgap may not be sharply defined, can vary substantially, and may deviate from the optical one [193]. SiN has been incorporated, albeit with some success, in dielectric passivation schemes on AlGaN barrier layers in HEMTs and lateral power diodes [194–198]. However, the success is limited, maybe due to the polar nature of the nitride heterostructure, which yields a charged surface and is the primary difference between GaN-based HEMTs and FET structures from other semiconductor materials. The surface charge is thought to be located in a surface defect donor state, where the energetic position and chemical structure of this state are technology-dependent [130]. Accordingly, the hypothesis mentioned above of the surface donor configuration and alternative surface countercharge configurations is possible when employing SiN. This hypothesis was hinted from the XPS studies of SiN/(Al)GaN interfaces on epitaxial layers deposited on sapphire (not involving a HEMT barrier layer) [153]. Here, the Fermi level lineup could be identified between SiN and the (Al)GaN conduction band edge over a wide range of compositions

from GaN to AlN. To understand these results, it may be helpful to remember that SiN is a highly charge-compensated dielectric, where defect complexes could pin the Fermi level in the upper or lower half of its bandgap. In the investigation by Reddy *et al.*, there was a Fermi level lineup between the SiN overlayer and the (Al)GaN conduction band edge (for Al composition $< 60\%$), and thus no deep donor state was observed [153]. CV measurements on p-type GaN showed a high barrier on the order of the bandgap, indicating no dominating additional deep surface state level in the lower half of the bandgap either [153]. Thus, the AlGaN/SiN interface seemed (within the resolution limits of the measurement) a perfect, interface-state-free semiconductor/amorphous heterojunction.

In the experiments performed by Reddy *et al.*, the SiN layer was 2 to 4 nm thin slightly Si-rich film deposited by LPCVD at 800 °C and 300 mTorr with dichlorosilane (40 sccm) and ammonia (120 sccm) [135]. The measured refractive index was ∼2.02 at 632 nm (a dielectric constant of $4.1\varepsilon_0$), indicating nearly stoichiometric Si_3N_4. Its Fermi level was found at approx. 3.5 eV above its valence band edge [153], making this configuration appearing n-type. This position would indeed allow a lineup with the conduction band edge of (Al)GaN. Si defects in various configurations are likely candidates found in the upper half of the bandgap to provide for the trap band configuration that would determine the Fermi level. Specifically, the ≡Si defect center could be the possible defect configuration. This defect has a (0/-1) higher energy acceptor level and (0/+1) lower energy donor level that are energetically close. These configurations were first calculated by J Robertson's group in 1984, using an early tight-binding model [192], and reconfirmed by DFT calculations in 2001 [199]. If this were the dominating defect complex in a slightly Si-rich configuration, this could pin the Fermi level near the GaN conduction band edge [153]. Later, related to the SiN charge storage properties, more detailed atomistic calculations revealed a complex picture of the ≡Si center and double bond configurations with partially amphoteric characteristics [160, 163]. The two

above-discussed results are shown combined in Fig. 4.2. Assuming this hypothesis applies, the necessary polarization countercharge could be located in the related defect band in close proximity to the interface. Furthermore, following the earlier analysis by Reddy *et al.* [153], assuming a defect concentration of $\sim 5 \times 10^{19}$ cm^{-3}, a polarization countercharge density of 10^{13} cm^{-2} could be deposited within 2 nm and could be charged/discharged by direct tunneling from the GaN or AlGaN conduction band or assisted by conduction with low activation energy within a related trap band.

An equally important part of the SiN deposition process was an in-situ pre-cleaning step in the LPCVD deposition chamber at high-temperature (> 700 °C) by NH_3, with identical parameters as used in the pre-cleaning process of GaN templates in the MOCVD chamber before further GaN growth [153]. When inserting a short *in-situ* oxygen pulse between pre-cleaning and SiN deposition, the interfacial Fermi level was moved by approximately 1.4 eV into the GaN bandgap. The structure of the surface oxide was recently determined to

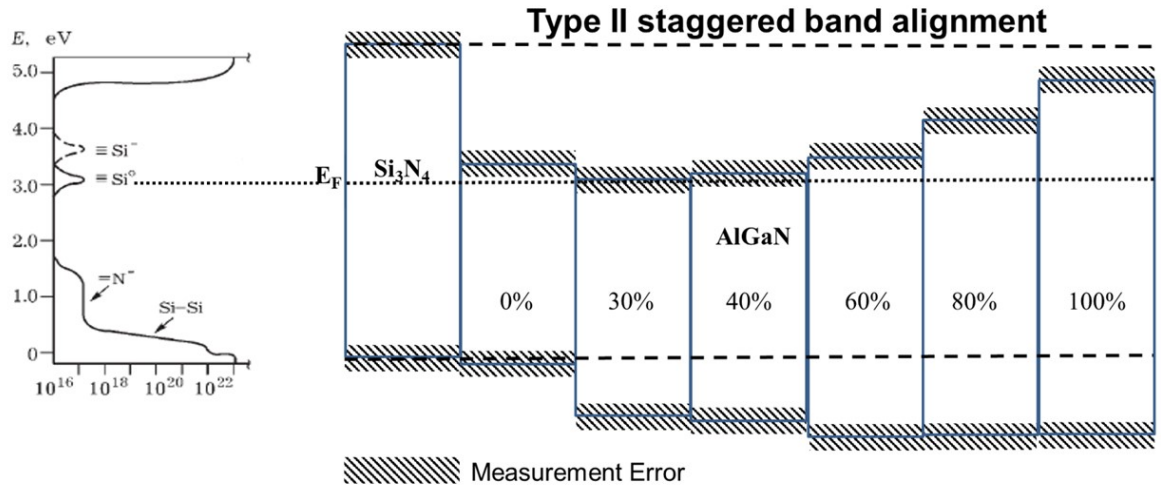

Figure 4.2: Left: trap distribution within the SiN bandgap, calculated by the tight-binding recursion method in 1984 [192]. Right: Band structure lineup of LPCVD deposited SiN on AlGaN of various compositions [153].

be similar to β-Ga_2O_3 with three monolayers of oxygen [200] and is likely patchy, based on XPS results showing an average between 0.5 and 1 monolayer of oxygen [130]. This likely produces deep interface states and inhomogeneity in surface electronic properties, which lead to stability/reliability issues. It seemed, therefore, essential to reduce all of the Ga-oxide patches on the GaN surface and desorb all oxygen from this surface [153, 201].

With the above-mentioned experiments, the following picture has emerged. It seems possible to produce a SiN/(Al)GaN amorphous/crystalline heterointerface free of deep donor interface states, in this case, by LPCVD deposition at high temperature in an oxygen-free environment. The polarization countercharge to the polarization charge was then located above this interface in a thin (several nm) SiN electron source/sink layer (hypothetically) consisting of activated $Si^{+/0}$ and $Si^{0/-1}$ defect centers within tunneling distance from the (Al)GaN interface.

However, with a defect density of this order, the defect level may start to be distributed and form a defect band. This would result in residual conduction with low activation energy, in essence representing a lossy dielectric with a resistivity still in the MΩcm range. Thus, these characteristics are, in general, not directly visible. In HEMTs, they would appear in the lateral gate/drain diode leakage behavior, their dynamic behavior causing current clipping or power slump effects. A lossy dielectric would be a conductor at low frequency and a capacitor above the dielectric cutoff frequency. Its signature is thus a sharp transition with a single RC-time constant. Such single RC-time constant signatures have been observed already at the beginning of the development of GaN-based HEMT technologies for a variety of heterostructure configurations as well as passivation schemes [170]. A spread of transition frequencies over 12 orders of magnitude was observed in one experiment, indicating the difficulty of correlating such an electrical behavior with chemical/physical configurations [202]. Plotting such a dispersion curve as a function of temperature would allow the extraction

of activation energy for the conduction path. An example is discussed by Neuburger *et al.*, where transport-related activation energy of $E_{act} = 0.3$ eV was extracted (for a dielectric cutoff frequency in the MHz range) [203].

To verify the above concept, Reddy *et al.* reported a series of experiments where thin SiN interlayers were inserted into standard metal contacts on GaN, making them dielectric-assisted [135]. Those results were mainly focusing on the Ga-polar GaN and only glancing over the N-polar GaN. The following section discusses the case of a SiN interlayer on N-polar GaN in great detail.

4.2 Part-II: Study of LPCVD SiN Properties Deposited on N-polar GaN

Schottky contacts to N-polar GaN have been widely considered a challenging technical building block due to the material's polar orientation and a rather reactive surface. On N-polar GaN, the inverse (positive) polarization surface charge (σ_P) with respect to the Ga-polar surface yields a lower Schottky barrier height, leading to higher leakage currents and lower breakdown strength [116, 119, 130, 131, 133, 134, 204]. In addition, the N-polar GaN surface reacts readily with many chemicals used in standard fabrication processes [112–116]. It is thus difficult to form reliable Schottky barrier contacts for diodes and field-effect transistor (FET) gates.

A possible solution to overcome these challenges is to insert a thin dielectric interlayer between the metal contact and N-polar GaN, making it a dielectric-assisted Schottky barrier system [135]. The most commonly used passivation dielectric in GaN technology is silicon nitride (SiN) [152, 172, 175–177, 183, 194, 205–207]. SiN interlayers have also been implemented in gate contacts of N-polar GaN FETs [198, 208–210]. Recent studies have examined the

SiN/N-polar GaN interface and proposed associated energy band diagrams [211–213]. In these studies, SiN films ranging in thickness from 5 to 30 nm have been deposited on N-polar GaN via in-situ metalorganic chemical vapor deposition (MOCVD), and the resulting structure has been analyzed as a metal-insulator-semiconductor capacitor (MIS-CAP). The SiN is often assumed to behave as a charge-containing insulator, with few details provided regarding the DC conductance of SiN, especially when very thin films have been used, or the barrier height at the metal/SiN interface.

SiN employed in this study has been deposited via low-pressure chemical vapor deposition (LPCVD) at 725 °C, which is within the temperature range to obtain a near stoichiometric or slightly Si-rich SiN amorphous layer [156, 214, 215]. Slightly Si-rich LPCVD contains a Si dangling bond-related defect center (≡Si) within the upper half of the bandgap, which is amphoteric in nature and may become the dominating defect [135, 192]. This characteristic is often exploited as a charge storage layer in Si memory device technologies [161, 216–218]. When deposited on N-polar GaN, the negative counter charge can be placed within the SiN interlayer; a band diagram including bulk charge states for this system has been previously drawn [135, 153]. This leads to the formation of a defect miniband within the SiN, grossly aligned with the conduction band edge of GaN [135]. Thus, the system represents a tri-layer one, containing barriers between the metal/SiN and SiN/N-polar GaN as well as a trap-determined dielectric in between. A first-order model was proposed in our recent work, primarily focusing on the Ga-polar case and only briefly on the N-polar case [135]. It is worth noting that miniband conduction has also been reported in a tri-layer GaAs metal-insulator-semiconductor (MIS) diode system consisting of Al metal and an insulating layer of low temperature (LT) GaAs on n^+ GaAs [219].

This section provides a detailed analysis of the interlayer-modified Schottky system consisting of metal/SiN/N-polar GaN and focuses on the electrical behavior of LPCVD SiN

in this system. To identify the interlayer behavior clearly, a thickness of 7 nm of LPCVD SiN was chosen, which is beyond that of a pure tunneling barrier, making it akin to an MIS system. In addition, we have accounted for the chemical termination of the SiN surface, which may result in a highly oxidized state [220, 221]. Measurements show that the LPCVD SiN film does not behave as a charge-containing insulator, and that the previously identified amphoteric miniband must be included. We thus propose a modified band structure compared to previous studies that capture the properties of the specific LPCVD constellation employed.

4.2.1 Experimental Details

N-polar GaN layers were grown on a c-plane sapphire substrate with a 4° offcut towards the m-plane using a vertical, cold-wall, radio frequency (RF) heated, low-pressure MOCVD system. A 0.6 μm thick n^+-doped layer followed by a 2.6 μm thick n-type layer were grown with carrier concentrations of 5.0×10^{19} cm^{-3} and 3.5×10^{17} cm^{-3}, respectively. Both layers were unintentionally doped with oxygen. Then, a 7 nm thick SiN film was deposited using LPCVD at 725 °C and 320 mTorr with dichlorosilane and ammonia precursors. Before depositing SiN, an *in-situ* cleaning step with ammonia was performed to remove native oxides. The deposited SiN layer thickness was confirmed using reflectometry.

Device fabrication started with deposition of a large area ohmic contact (V/Al/Ni/Au – 30/100/70/70 nm) on top of the SiN surface using e-beam evaporation. The ohmic contacts were annealed at 850 °C for 30 sec in N_2 ambient [135]. It should be noted that the SiN is present during this short annealing step. However, the quality of the SiN is not affected as it was already deposited at a high temperature. Measurements of the current between two ohmic contacts in forward and reverse bias confirmed a linear relationship in both directions. This is in agreement with our previous results when forming large area ohmic contacts on LPCVD SiN/Ga-polar GaN heterostructures [135]. Prior to the Schottky metal deposition (Ni, 250 nm)

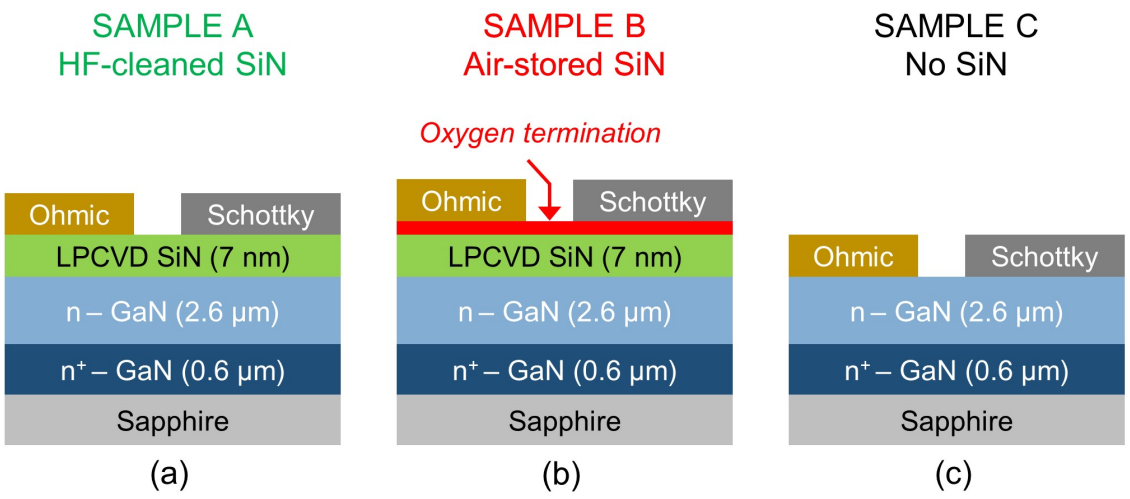

Figure 4.3: Schematic cross-sections of Schottky diodes on (a) HF-cleaned and (b) air-stored SiN interlayers, as well as on (c) bare N-polar GaN. Not drawn to scale.

on the SiN surface, Sample A was cleaned with 10% hydrofluoric (HF) acid for 1 min, followed by a DI water rinse, while Sample B was kept in an ambient environment. It is expected that HF cleaning removes several angstroms of oxidized SiN [152, 220]. The experiment was designed to determine the influence of the surface termination on the electrical characteristics of the three-layer structure. Schottky diodes without SiN (Sample C) were also fabricated as control samples. The Schottky metal pattern was deposited using a metal shadow mask to avoid exposure of the N-polar GaN and SiN-coated diodes to photolithography developer [116]. Cross-section diagrams of the fabricated devices are shown in Fig. 4.3.

4.2.2 Results and Discussion

X-ray photoelectron spectroscopy (XPS) was used to determine the band offsets, Fermi level (EF), and barrier height at the interface between the SiN and N-polar GaN. Both thick (150 nm) and thin (∼3-4 nm) SiN films were deposited on two separate N-polar GaN samples (without subsequent metal deposition) to determine the parameters mentioned above. The

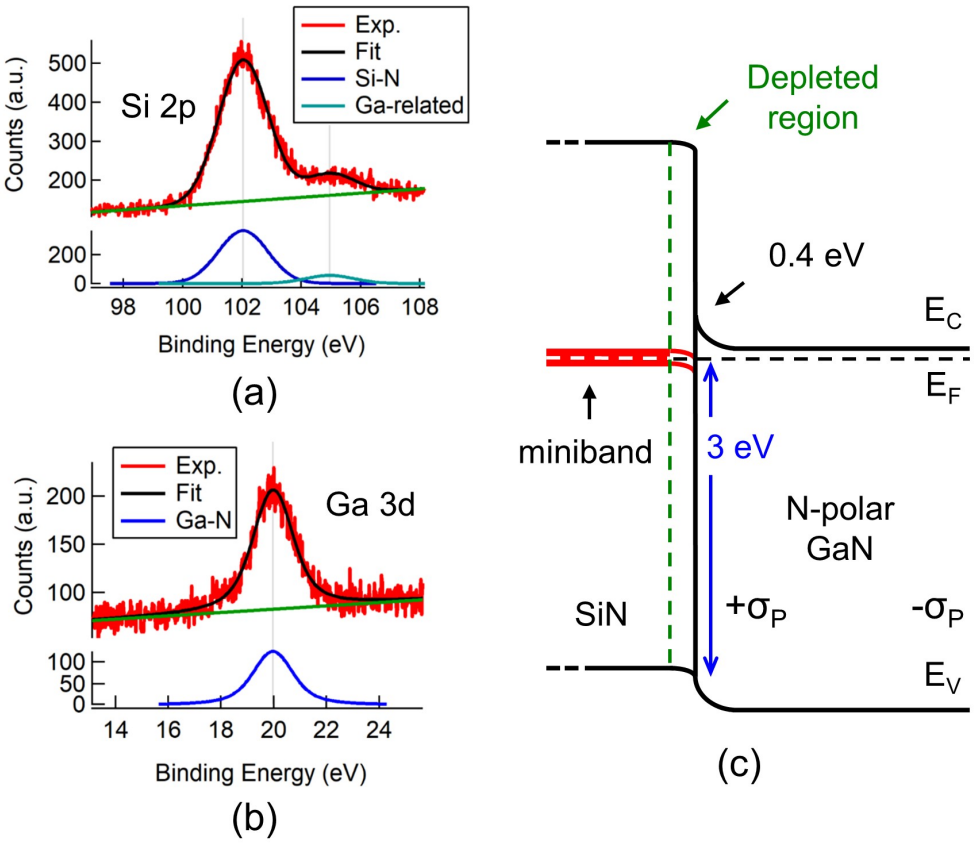

Figure 4.4: XPS spectra of (a) Si core level (Si 2p) and (b) GaN core level (Ga 3d) peaks measured on SiN/N-polar GaN. (c) A tentative energy band diagram of SiN deposited on N-polar GaN without metal/SiN interface. σ_P denotes polarization charge in N-polar GaN.

procedure, experimental setup, and Au- and C-based charging correction during XPS data analysis are described in [153, 183].

The core level binding energies of Si 2p and Ga 3d at the interface were determined with respect to the interface Fermi level, as shown in Figs. 4.4(a) and 4.4(b), respectively. Employing the valence band and core level characterization in thick SiN films [153], thick N-polar GaN films [130], and the core level binding energies at the interface, we can determine the SiN/N-polar GaN valence band offset to be ∼0 eV. Interestingly, the interface Fermi level is at 3 eV from the valence bands of GaN and SiN. Based on the doping in N-polar GaN, $n =$

3.5×10^{17} cm^{-3}, the difference between the conduction band and Fermi level ($E_C - E_F^{bulk}$) in the bulk region would be less than 0.05 eV. Hence, the barrier height at the charge neutrality level, i.e., the energy difference between the interface Fermi level and conduction band of GaN, is 0.4 eV. Furthermore, since this energy level lineup coincides with the ≡Si defect level in slightly Si-rich SiN, it may be reasonable to assume that a defect miniband is formed in this case, determining the Fermi level throughout the SiN interlayer. A tentative energy band diagram at the SiN/N-polar GaN interface is created using these findings, as shown in Fig. 4.4(c). It shows a very low barrier system when SiN is deposited on N-polar GaN.

The N-polar GaN diodes were then electrically characterized to study the barrier at the metal/SiN interface and confirm whether the Fermi level in SiN is pinned due to the miniband. Temperature-dependent current-voltage measurements (I-V-T) were performed in a vacuum probe station (base pressure $\sim1\times10^{-7}$ Torr) using a Keithley 4200 semiconductor parameter analyzer. Capacitance-voltage (C-V) measurements were conducted at 1 MHz using the parallel R-C circuit mode.

The room temperature I-V characteristics of all three diodes are shown in Figs. 4.5(a) and 4.5(b). The ideality factors (n) of Samples A and B are > 1.6, and exhibit a slight voltage dependence. Their threshold voltages are $V_{th,A}$ ∼0.6 V and $V_{th,B}$ ∼5.0 V, respectively, as extracted from the linear representation. Sample C showed an n_A ∼1.07, which represents near-ideal Schottky diode behavior, and $V_{th,C}$ ∼0.4 V.

Figures 4.6(a) to 4.6(c) show the temperature-dependent I-V characteristics for HF-cleaned SiN, air-stored SiN, and no SiN (as-grown) surface Schottky diodes, respectively. The I-V barrier heights ($\phi_{B,IV}$) for all three samples are calculated by extracting the saturation current density (J_0) that is extrapolated from the exponential region of the forward bias I-V measurements as a function of temperature up to 200 °C. The procedure is described elsewhere [116, 125]. As shown in Fig. 4.6(d), $\phi_{B,IV}$V in Samples A, B, and C are 0.4 eV, 1.1

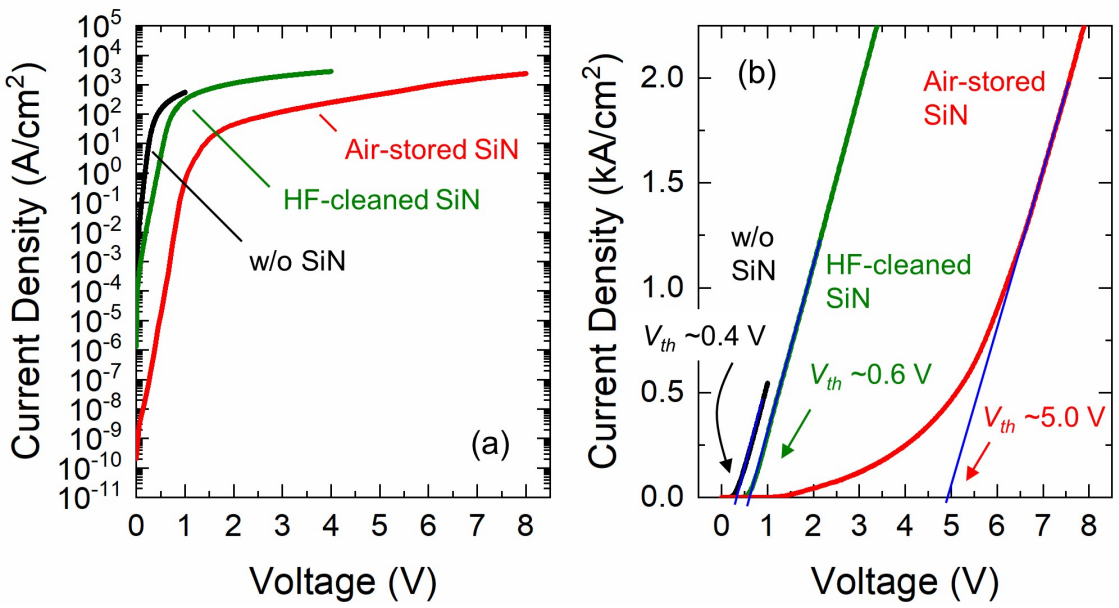

Figure 4.5: Room temperature forward bias I-V characteristics in (a) semilog-scale and (b) linear-scale for the fabricated Schottky diodes with different surfaces.

eV, and 0.4 eV, respectively. It should be noted that $\phi_{B,IV}$ for Samples A and B are apparent barrier heights due to the higher ideality factors (> 1.6) of these diodes.

The $\phi_{B,IV}$ in Sample A is consistent with the XPS results, indicating that the barrier is determined by the SiN/N-polar GaN interface, with no or negligible barrier at the metal/SiN interface. Thus, the reason that $V_{th,A}$ ~0.6 V is that the lossy SiN interlayer drops an additional 0.2 V across it with respect to Sample C. Under forward bias, the charge is injected from GaN into the lossy SiN, which conducts through the defect miniband. I-V measurements show an observable temperature dependence [see Fig. 4.6(a)] that confirms that defect-assisted tunneling is not the dominant conduction mode when 7 nm thick LPCVD SiN is used. This is in contrast with our previous experiments [153] where 2-4 nm of LPCVD SiN were deposited on Ga-polar GaN. There, a weak temperature dependence was observed in forward bias, which is indicative of tunneling. Here, we note that more than one conduction mechanism may be involved. Due to the overall low barrier, the current through the diode reaches the

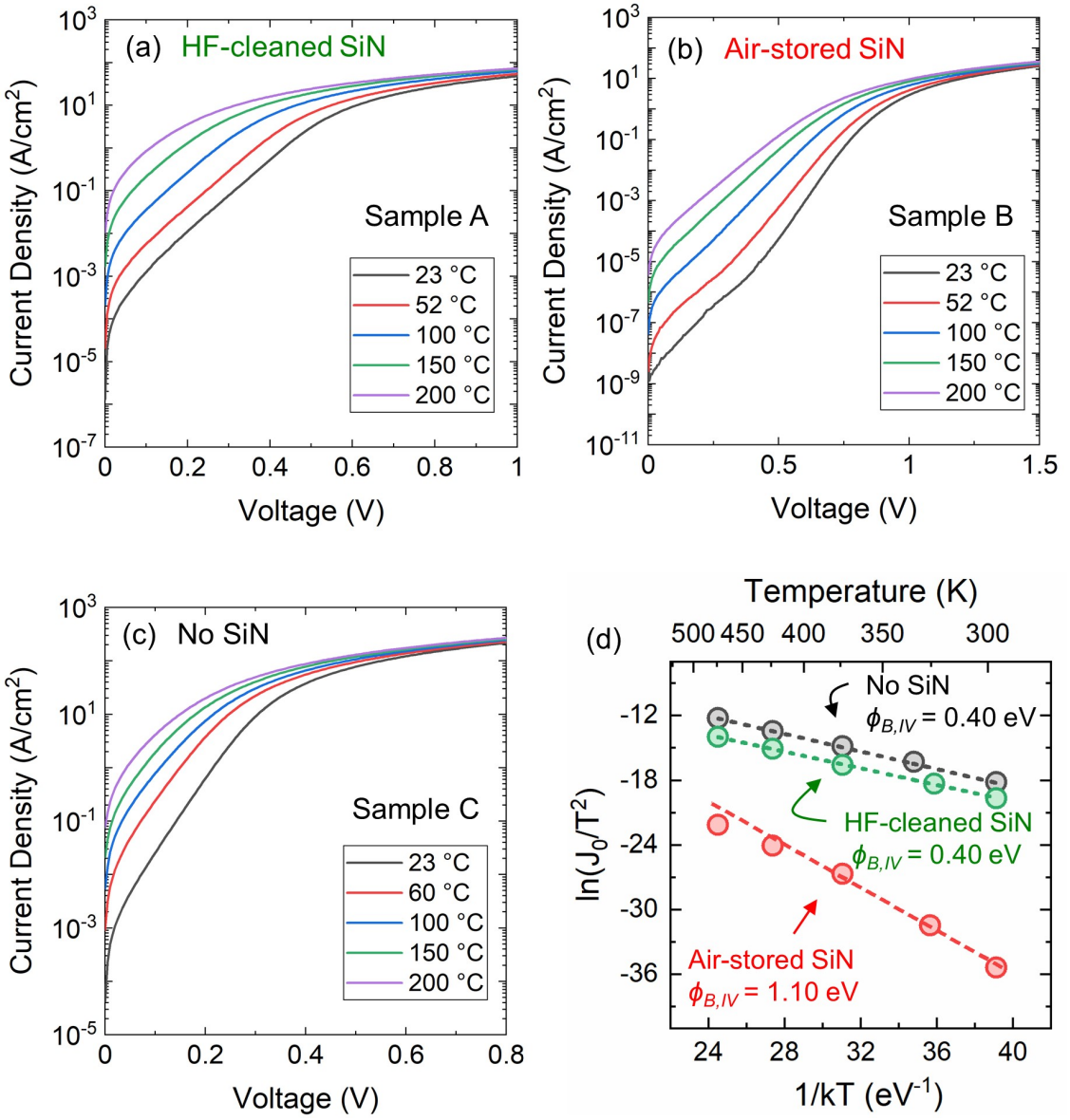

Figure 4.6: Temperature-dependent I-V characteristics of (a) HF-cleaned SiN, (b) air-stored SiN, and (c) without SiN Schottky diodes. (d) I-V barrier height extraction using [$\ln(J_0/T^2)$ vs. 1/kT] generated from temperature-dependent I-V characteristics shown in figures (a) to (c).

metal series resistance level at very low voltages, so identifying the exact current mechanism through the SiN interlayer is complex and not attempted in this work.

The semilog I-V of Sample B shows two distinct current regimes: one at lower voltages (< 2 V) and another above it, before reaching the metal series resistance limit at around 8

V. The first regime is exponential, while the second regime is a current limiter; the linear I-V reveals that this is a superlinear transition region at medium voltages. That $V_{th,B}$ ~5.0 V is well above GaN's bandgap indicates a strong influence of the oxygen termination on the SiN surface. I-V-T reveals a very high barrier height of ~1.1 eV for this case, which is extracted from the first exponential at lower voltages. From XPS, the barrier at SiN/N-polar GaN is 0.4 eV, so the measured I-V barrier height in Sample B must be at the metal/SiN interface. Consequently, the current limiter could be related to the SiN interlayer, the barrier at the metal/SiN interface, or both, and the current transport mechanism could be one or many of the different mechanisms mentioned earlier. To summarize, I-V measurements reveal a low barrier system in the HF-cleaned SiN MIS diodes, with a dominating barrier at the SiN/GaN interface, no barrier at metal/SiN interface, and neutral defect miniband in-between. In comparison, the air-stored SiN MIS diodes are characterized by a high barrier at the metal/SiN interface and high overall resistance, indicating that much of the SiN is depleted.

C-V measurements were performed to support the I-V findings and estimate the upper limit of the defect concentration, which forms the defect miniband in SiN. Fig. 4.7 shows the C-V barrier height ($\phi_{B,CV}$) extracted from $1/C^2$-V for all three cases, and the top-right corner of the graph shows the modified equivalent circuit of the C-V measurements. Although the C-V barrier height equation consists of the intercept voltage, (kT/q), and the energy difference between the conduction band and Fermi level, the sum of the total energy for those additional two terms is within 0.05 eV for the doping level of our N-polar GaN diodes. Thus, these additional terms do not significantly impact our estimate of the C-V barrier height [116]. It should be noted that the circuit shown here is not developed using impedance spectroscopy; it is a representation of the extended R-C circuit by considering the two series components of R-C from the SiN interlayer and GaN space charge layer. The reason for this

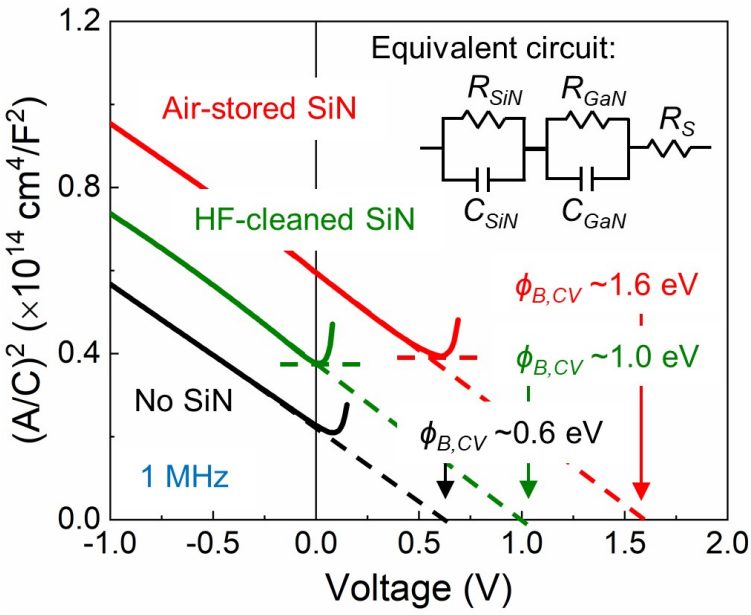

Figure 4.7: C-V barrier height extraction for without SiN, HF-cleaned, and air-stored SiN surface Schottky diodes. The top-right corner of the graph shows the equivalent circuit of the diode for the C-V measurements.

additional SiN R-C parallel element is that in reverse-bias, SiN becomes capacitive, while in forward-bias, it becomes conductive due to the conduction through the miniband. This is evidenced by the sudden drop in capacitance at distinct forward bias voltages corresponding to the onset of charge injection [222].

All three diodes appear linear in the $1/C^2$-V plots measured at 1 MHz, as shown in Fig. 4.7. The $\phi_{B,CV}$ values for Samples A, B and C are ~1.0 eV, ~1.6 eV, and ~0.6 eV, respectively. The net doping concentration is extracted for all three cases using the slope of the $1/C^2$-V curve and is found to be around 3.5×10^{17} cm^{-3}, as expected. Thus, the modulated capacitance in all three diodes is of the SiN/N-polar GaN junction, and no additional modulation of a metal/SiN junction capacitance is observed. Whereas $\phi_{B,IV}$ of Samples A and C were found to be equivalent, the $\phi_{B,CV}$ of Sample A is now larger due to the additional capacitance presented by SiN in series with the GaN space charge layer capacitance in reverse bias. By

calculating the difference in the 1/C values in Samples A and C, it is estimated that SiN has a thickness of 6.5 nm, which agrees with the reflectometry measurements.

The C-V behavior of Sample A suggests that the SiN acts as a capacitor in reverse bias up to zero bias. The I-V behavior of the same sample suggests that the SiN is neutral and acts as a resistor since there is no barrier at the metal/SiN interface. This is characteristic of a lossy dielectric that experiences dielectric relaxation (below 1 MHz), and it confirms that, in the case where an HF-cleaned SiN interlayer is used, there is no noticeable barrier between the top metal and SiN.

The $1/C^2$-V characteristic of Sample B is shifted upwards as compared to Sample A, which results from a higher barrier at the metal/SiN surface and is consistent with the same sample's I-V behavior. It should be noted that the impedance bridge cannot balance anymore at approx. 0.6 V, which is the beginning of the transition region where the resistive behavior takes over. The large transition region in I-V [see Fig. 4.5(b)] shows that transport increases gradually, and there may be a mixture of the transport mechanisms mentioned earlier. This transition region appears exponentially increasing with a shallow slope in semilog I-V, whereas in linear I-V, it appears as a superlinear rise. Thus, the metal/SiN barrier dominates the overall barrier behavior, and this higher barrier is caused by the oxygen termination of the SiN interlayer in Sample B. Since capacitance modulation is not observed in SiN, it is concluded that the metal/SiN barrier results in complete depletion of the SiN interlayer. Using the I-V-extracted barrier of 1.1 eV, the upper limit in defect density within the miniband can be estimated. Considering that 2 to 2.5 nm SiN is already depleted at the SiN/GaN interface due to the countercharge of $\sim 10^{13}$ cm^{-2} polarization charge of N-polar GaN, 1.1 eV needs to deplete the remaining 4.5 to 5 nm SiN. Therefore, the upper limit of the defect density is found to be around 2 to 5×10^{19} cm^{-3} in this LPCVD SiN.

Based on the above analysis, energy band diagrams for Samples A and B are proposed and

schematically depicted in Figs. 4.8(a) and 4.8(b), respectively. HF treatment of the LPCVD SiN prior to metal deposition results in a system dominated by the SiN/GaN interface, whereas oxide formation on the SiN surface leads to a dominating barrier at the metal/SiN interface. Whereas previous depictions of SiN on GaN have assumed that SiN acts as a charge-containing insulator [213], our results reveal that the picture may be more complex. Si dangling bonds in LPCVD SiN can lead to the formation of a defect miniband [192]. It was predicted that a trapped electron level ($\equiv Si^{-}$) and trapped hole level ($\equiv Si^{0}$) are separated by 0.4 eV [192]. Our analysis also shows evidence that the formed miniband is amphoteric, pointing to an overlap of the distribution of trapped charge states (depicted by the shaded regions in Fig. 4.8(a)). Due to its shallow energy level, conduction can occur through the interlayer. Consequently, the amphoteric nature of the miniband is also responsible for the depletion of donors and acceptors at the metal/SiN and SiN/GaN junctions, respectively.

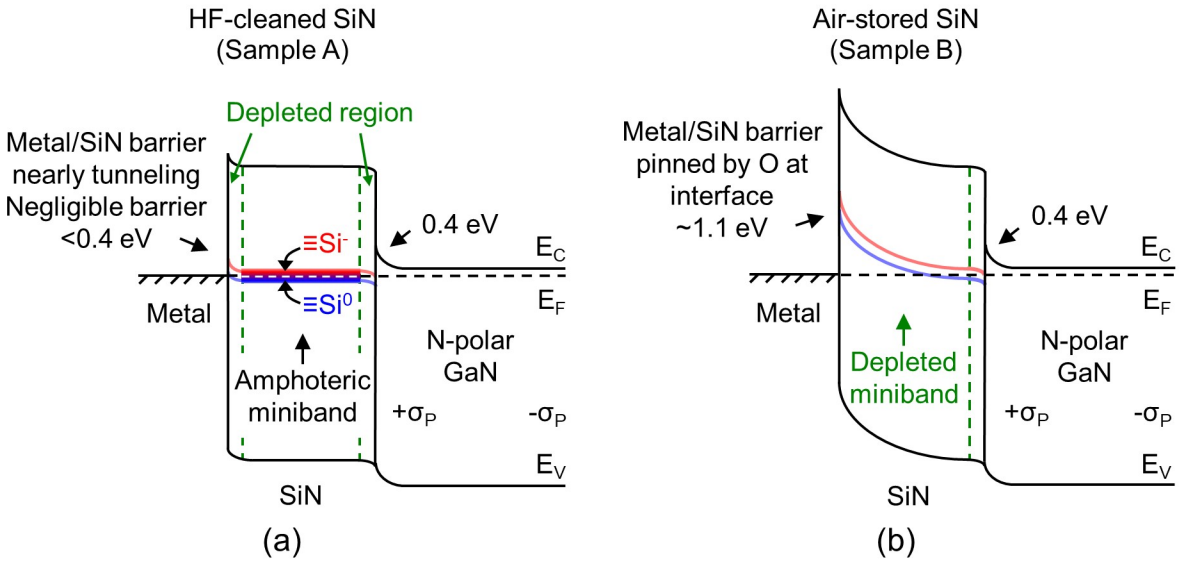

Figure 4.8: Band structure alignment at equilibrium between metal, SiN, and N-polar GaN for (a) HF-cleaned and (b) air-stored SiN surface Schottky diodes. Not drawn to scale.

This is key, since the presence of a unipolar miniband would lead to the formation of two back-to-back diodes. This would limit current flow until one of the two diodes would break down. Instead, we observe a behavior that is consistent with two series-connected diodes, where the potential across them adds up.

4.2.3 Summary

In summary, this work considers the defect- and surface-dependent properties of LPCVD SiN in determining the electrical behavior of Metal/SiN/N-polar GaN diodes. Based on XPS, I-V-T, and C-V measurements, band diagrams are proposed which account for an amphoteric miniband formed in the LPCVD SiN, where both the donor and acceptor state distributions overlap. When metal is deposited on HF-treated SiN, the SiN/GaN interface is responsible for determining the system's barrier height, whereas the use of oxidized SiN leads to a metal/SiN-dominant barrier. Due to the amphoteric nature of the miniband configuration, the top and bottom barriers in this tri-layer system are not back-to-back biased but in series, which is a highly unusual configuration. SiN deposited on GaN has long been considered a charge-containing insulator in dielectric-assisted Schottky barrier systems, MIS-gate structures, and as a passivation layer. However, this picture may be oversimplified. The tri-layer system analyzed here contains a barrier-controlled lossy dielectric. Thus, rigorous analysis of SiN properties is important in determining its behavior on GaN, and further quantitative studies are needed to optimize such structures in devices.

4.3 Part-III: Schottky Contacts to N-polar GaN with 5 nm LPCVD SiN Interlayer for Elevated Temperature Operation Capability

4.3.1 Introduction

In recent years, N-polar GaN material has demonstrated great potential for electronic and optoelectronic device applications [55, 112, 209, 223–225]. One such example is N-polar GaN-based high electron mobility transistors (HEMTs). The two-dimensional electron gas (2DEG) in N-polar GaN HEMTs is formed by an AlGaN back-barrier rather than a barrier directly below the gate because of the opposite polarization field compared to Ga-polar GaN [112, 224]. This permits superior device scaling and reduced contact resistance for the source and drain terminals, which have made it possible for N-polar GaN HEMTs to experimentally outperform Ga-polar GaN HEMTs [208, 226]. Of great interest in this thesis is the use of N-polar GaN as the n-type pillar in superjunction devices [51, 94, 227].

In Schottky barrier diodes and HEMTs, the quality of the Schottky contact plays an essential role in determining the device's performance. Usually, a higher Schottky barrier is required to reduce leakage. The opposite polarization field in N-polar vs. Ga-polar GaN means that the barrier height in N-polar GaN is actually very low compared to that observed in Schottky contacts to Ga-polar GaN [46, 116, 130, 131, 133, 134, 204]. This low barrier leads to higher reverse bias leakage and limits high-temperature operation. Liu *et al.* recently demonstrated that Ru-based Schottky contacts yield a higher Schottky barrier and reduce the reverse bias leakage compared to other contact schemes [228]. However, the temperature-dependent I-V (I-V-T) characteristics of the devices were only reported up to 175 °C. To date, there are no reports in the literature of N-polar GaN Schottky diodes operating at elevated temperatures (>200 °C). High temperature operation is not only a requirement for deployment

of a device in harsh environments, but it also translates to reliable performance. Moreover, relaxed cooling requirements eliminate the need for bulky cooling systems, making it easier to integrate these systems into automotive, aerospace, and energy production sectors [229].

In Section 4.2, we demonstrated that a thin SiN dielectric layer deposited via low-pressure vapor deposition (LPCVD) between the N-polar GaN and Schottky metal passivates the surface polarization charge and raises the barrier height [154]. In this section, the high temperature operational limit of N-polar GaN Schottky diodes with a 5 nm LPCVD SiN interlayer is explored.

4.3.2 Experimental Details

N-polar GaN layers were grown on a c-plane sapphire substrate with a 4° offcut towards the m-plane using a vertical, cold-wall, radio frequency (RF) heated, low-pressure metal-organic chemical vapor deposition (MOCVD) system. A 0.4-μm-thick n^+-doped layer followed by a 0.4-μm-thick n-type layer was grown with unintentional oxygen carrier concentrations of 5.0×10^{19} cm^{-3} and 5.0×10^{17} cm^{-3}, respectively. Then, a 5-nm-thick SiN (slightly Si-rich) film was deposited using LPCVD at 725 °C and 320 mTorr with dichlorosilane and ammonia precursors. Before depositing SiN, an in-situ cleaning step with ammonia was performed to remove native oxides. The deposited SiN layer thickness was confirmed using ellipsometry and reflectometry [135, 153, 154].

After the growth, a metal stack consisting of Ti/Al/Ni/Au (30/100/70/70 nm) was deposited over a large area using e-beam evaporation and annealed at 850 °C for 30 s in N_2 ambient to obtain ohmic behavior through the SiN interlayer [135, 154]. Schottky contacts were then formed via e-beam evaporation of Ni (250 nm). Figs. 4.9(a) and 4.9(b) shows the schematic cross-section and tilted-view scanning electron microscope (SEM) image of a fabricated N-polar GaN Schottky barrier diode with a 5 nm SiN interlayer. Henceforth, this

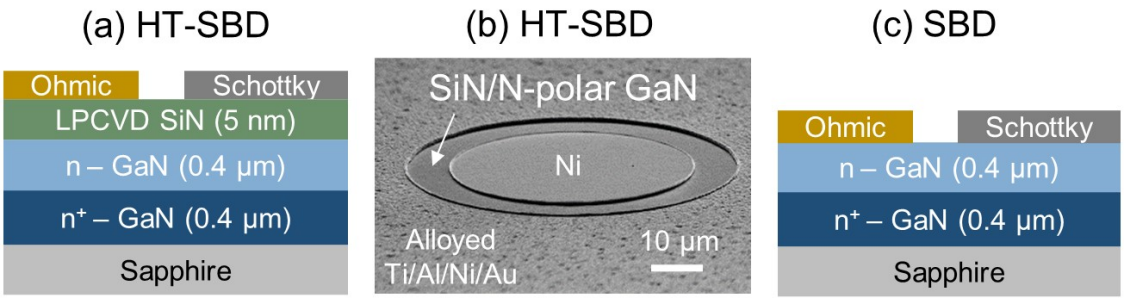

Figure 4.9: (a) Schematic cross-section and (b) tilted view SEM image of the fabricated N polar GaN Schottky diode with 5 nm LPCVD SiN interlayer (HT-SBD). (c) Schematic cross-section of conventional N polar GaN Schottky diode (SBD).

device is referred to as the HT-SBD. Conventional Schottky barrier diodes lacking the SiN interlayer, henceforth referred to as SBD, were also fabricated for a controlled comparison of the HT-SBD's properties. The schematic cross-section of the SBD is shown in Fig. 4.9(c). It should be noted that the Schottky metal for the SBD was deposited using a metal shadow mask to avoid exposing the N-polar GaN surface to photolithography developer [116, 154].

I-V-T measurements were performed on a heated stage mounted in a vacuum chamber ($\sim 10^{-7}$ Torr) using a Keithley 4200 semiconductor parameter analyzer. All the devices were stressed for at least 1 hour at each temperature measurement. The temperature readings were taken by placing the thermocouple directly on the surface of the sample since it was noticed that the temperature on the sample surface was always lower than the heated stage due to the thermal isolation from the sapphire substrate.

4.3.3 Results and Discussion

To validate the ohmic behavior of alloyed Ti/Al/Ni/Au to N-polar GaN through the 5 nm SiN layer, circular transfer length measurement (CTLM) structures were fabricated and tested before and after contact alloying. Figure 4.10(a) shows a tilted-view SEM image of one of the CTLM structures with a 4 μm contact distance. The I-V measurements before and after the

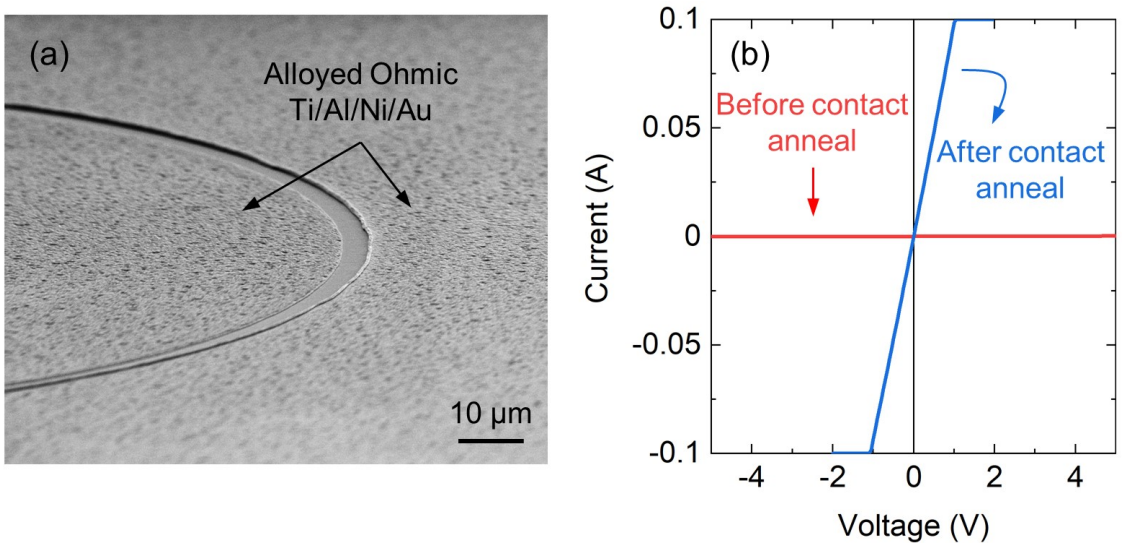

Figure 4.10: Circular TLM structures were fabricated to evaluate the ohmic nature of the Ti/Al/Ni/Au contact to SiN/N-polar GaN. (a) Tilted-view SEM image of two alloyed ohmic contacts with 4 μm spacing. (b) Current-voltage measurements between the same contacts before (red line) and after (blue line) contact alloying at 850 °C for 30 sec in N_2 ambient.

contact alloying are shown in Fig. 4.10(b). From the graph, it is observed that the current flow between two ohmic contacts is linear only after the contact alloying.

A comparison of room temperature (22 °C) I-V characteristics in linear and semilog scale for both the HT-SBD and SBD is shown in Fig. 4.11(a). The ideality factors (n) for the SBD and HT-SBD are ∼1.1 and ∼1.4, respectively. The threshold voltage (V_{th}), extracted from the linear I-V in forward bias, is ∼0.4 V in the SBD. In contrast, V_{th} ∼0.9 V in the HT-SBD because of the additional voltage drop across the SiN interlayer. It is worth noting that the slope of the I-V after knee voltage for both cases is similar. This means the on-resistance does not change after inserting a 5 nm SiN interlayer. The semilog I-V for both diodes shows that the leakage current measured at zero bias is ∼4 orders of magnitude lower in the HT-SBD than in the SBD at room temperature, as seen in Fig. 4.11(b). At 200 °C, the leakage current for the SBD increases significantly, which renders a leakage current ratio difference of ∼5 orders [see dashed lines in Fig. 4.11(b)]. Thus, adding an ultra-thin SiN interlayer indeed

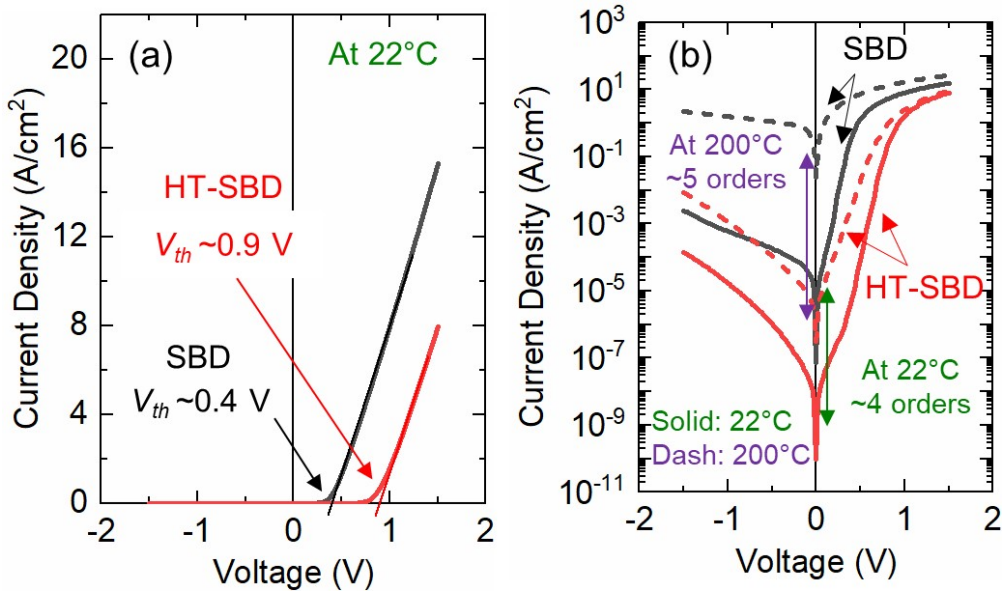

Figure 4.11: (a) Comparison of room temperature (22 °C) I-V characteristics of the HT-SBD and SBD in linear scale. (b) I-V comparison of the HT-SBD and SBD at 22 °C and at 200 °C in semilog scale. Solid lines are for 22 °C, and dashed lines are for 200 °C. There is a 4-order of magnitude difference in leakage current at zero bias at 22 °C between the HT-SBD and SBD, which increases to ∼5 orders of magnitude at 200 °C.

reduces the leakage current compared to conventional N-polar GaN Schottky diodes.

The I-V-T characteristics of the SBD from 22 °C to 250 °C are shown in Fig. 4.12(a). The leakage current, in this case, increases significantly as the temperature increases. At 250 °C, the rectification ratio (I_{ON}/I_{OFF}) at voltage bias ±1.5 V reduces to less than one order of magnitude, as seen in Fig. 4.12(a). After 250 °C, the SBDs were cooled to room temperature and measured again [dashed line Fig. 4.12(a)]. It is seen that the I-V measured before and after 250 °C overlaps, meaning no chemical degradation happened between Ni and N-polar GaN surface during the high-temperature measurements. Fig. 4.12(b) shows the I-V-T characteristics of HT-SBD from 22 °C to 400 °C. The rectification ratio at 400 °C is still ∼2 orders of magnitude. When going back to room temperature again from 400 °C, a negligible change is observed in I-V characteristics [dashed line in Fig. 4.12(b)] after high-temperature stress. This suggests no chemical degradation at the Ni/SiN/N-polar GaN interfaces, and

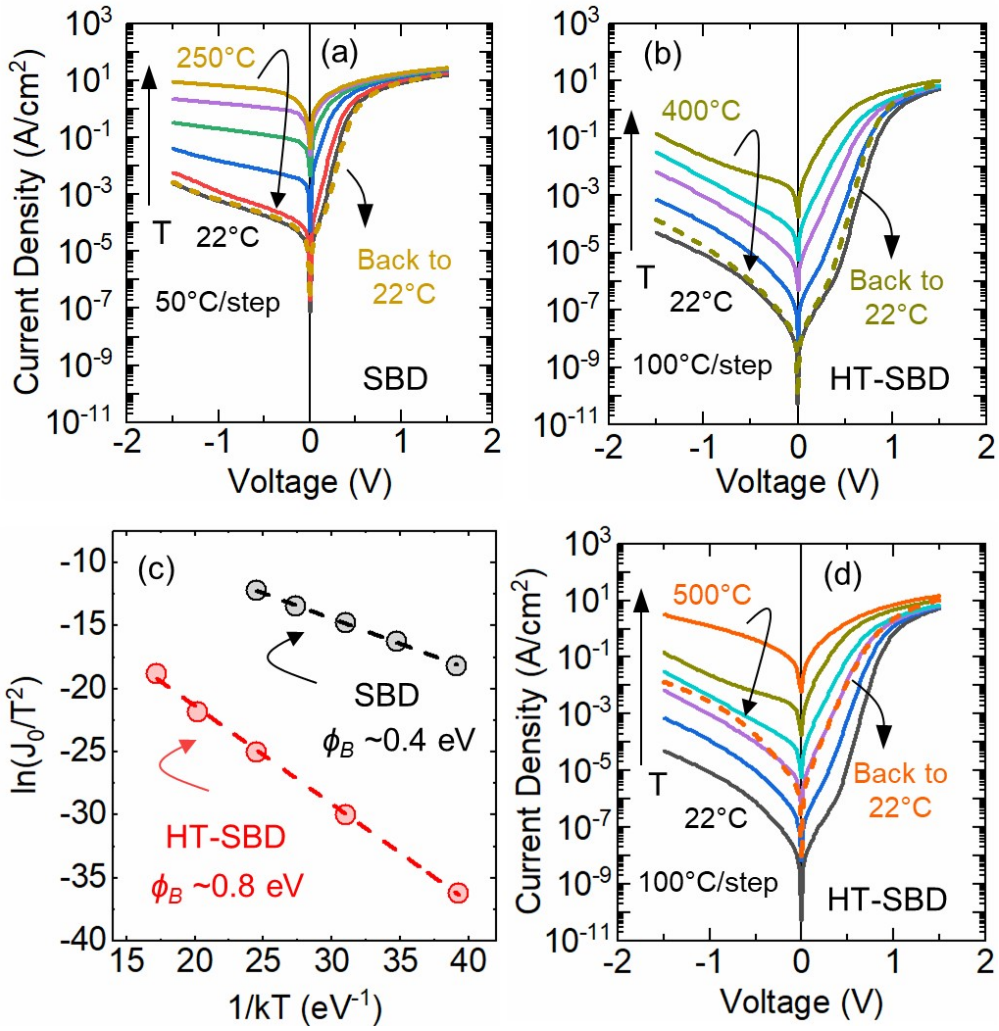

Figure 4.12: Temperature-dependent I-V (I-V-T) characteristics of (a) SBD diode from room temperature (22 °C) to 250 °C with a step of 50 °C and (b) with 5 nm SiN (HT-SBD) diode from 22 °C to 400 °C with a step of 100 °C. (c) Barrier height extracted from I-V-T. (d) I-V-T characteristics of diode with HT-SBD diode from 22 °C to 500 °C For (a), (b), and (d), dashed line represents the I-V at 22 °C after cooling down from respective high-temperature measurement in all cases.

repeatable Schottky diode performance can be expected. These results affirm that N-polar GaN Schottky diodes with an ultrathin SiN interlayer can be operated at significantly higher temperatures compared to conventional N-polar GaN Schottky diodes.

Barrier heights (ϕ_B) for both devices were extracted from the I-V-T characteristics, as

shown in Fig. 4.12(c). The ϕ_B for SBD and HT-SBD are ∼0.4 eV and ∼0.8 eV, respectively. It should be noted that the barrier height values for both diodes match with the threshold voltage extracted from room temperature linear I-V for each case. The barrier for the HT-SBD should be at the Ni/SiN interface; our previous work has demonstrated that the barrier at the SiN/N-polar GaN interface should not be more than 0.4 eV [154]. Thus, an ultra-thin SiN interlayer does indeed increase the barrier height. This, in turn, helps reduce leakage current and increase temperature operation capability.

Fig. 4.12(d) shows I-V-T characteristics of the HT-SBD from 22 °C to 500 °C. Interestingly, the rectification ratio is still around one order of magnitude at 500 °C. Although, when coming back to room temperature, the I-V behavior [dashed line in Fig 4.12(d)] deviates from what has been measured at room temperature before 500 °C stress. It should be noted that the diode is not destroyed, and the rectification ratio is still more than 3 orders of magnitude. This I-V behavior change must be due to chemical degradation in the diode after the 400 °C temperature operation. It may be speculated to be due to the interaction between Ni and Si-rich SiN instead of the chemical reaction at SiN/N-polar GaN since Ni-silicide usually forms at around 400 °C [230].

To investigate further, the devices operated at 500 °C were analyzed using scanning electron microscopy (SEM) and atomic force microscopy (AFM). Figs. 4.13(a) and 4.13(b) show tilted-view SEM images before any temperature measurements (as fabricated) and after 500 °C temperature measurements, respectively. From SEM, the surface of the Ni appears to be alloyed after 500 °C. The AFM scan on the Ni metal surface reveals changes in the surface morphology, which indicates alloying might happened after 400 °C, as seen in the inset of Fig. 4.13(b). However, the SiN/N-polar GaN surface between the Ni metal and ohmic contacts is similar for both cases. Thus, most likely, the chemical degradation only happened at Ni/SiN interface due to the interaction of Ni and Si-rich SiN, possibly forming Ni-silicide

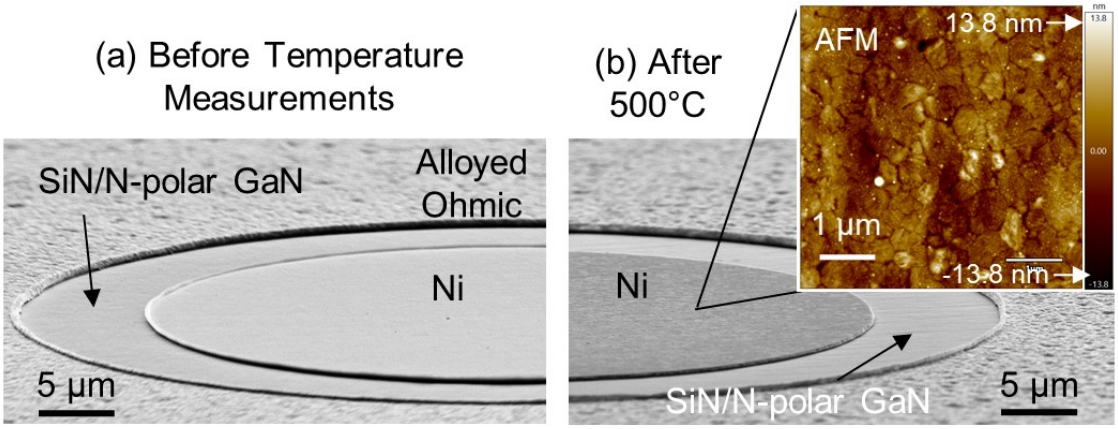

Figure 4.13: Tilted view SEM images of HT-SBD (a) before any temperature measurements (as fabricated) and (b) after 500 °C exposure in a vacuum. The inset of (b) shows AFM scan on Ni metal surface after 500 °C.

phases, after 400 °C. The results call for further exploration of the metal contact system in order to avoid silicide formation and increase the elevated temperature operation capability of N-polar GaN Schottky diodes, which is left for future work.

4.3.4 Summary

In summary, high-temperature stable Schottky contacts to N-polar GaN are achieved using LPCVD SiN interlayers. The ultra-thin SiN layer increases the barrier height, reduces the leakage current, and increases the thermal stability of the N-polar GaN Schottky diode. The SiN interlayer diodes show reproducible electrical properties even after being operated up to 400 °C. However, degradation happens at 500 °C, which could be due to the reaction at Ni/SiN interface. To the best of our knowledge, this is the first time N-polar GaN Schottky diodes have been shown to operate up to 500 °C. These results should enable reliable N-polar GaN devices with better performance.

4.4 Conclusion

To conclude, a detailed overview of the properties of SiN when deposited on GaN is provided. The key lies in the concept of using the amphoteric nature of SiN dielectric interlayer with a point-defect level of high density, above 10^{19} cm^{-3}, forming a defect band aligned with the semiconductor conduction band edge, to deposit the polarization countercharge within the tunneling distance from the interface. This amphoteric nature of defects in LPCVD SiN passivates not only the Ga-polar GaN but also the N-polar GaN. Stable dielectric-assisted Schottky contacts to N-polar GaN are achieved in this work. The thin SiN layer passivates the N-polar GaN surface charge, introduces a chemical diffusion barrier, and increases the barrier height as well as the thermal stability of the N-polar GaN Schottky diode. From the experiments reported above, it is observed that the surface termination of the SiN interlayer had a significant influence on the diode barrier characteristics. The insertion of 5 nm SiN between the Ni and N-polar GaN raised the temperature operation capability of the diodes showing repeatable operation up to 400 °C. Tuning the thickness of SiN and the choice of Schottky metal could lead to even better-performing devices from the reported devices in this work. Thus, a thin layer of SiN could offer a reliable solution to N-polar GaN technology, which would help to realize GaN SJ devices using the lateral polar junction approach. On the other side, due to the low dielectric constant of the SiN than GaN, the maximum electric field in SiN would be higher than GaN, which could cause the dielectric breakdown. Thus, the early time-dependent dielectric breakdown can be a bottleneck due to the high electric fields inside the dielectric as a result of high drift region doping in GaN SJ. For that, future studies and optimizations of devices with SiN interlayer on high breakdown GaN structures are required.

Chapter 5

N-polar GaN Camel Diode

5.1 Introduction

It has been demonstrated that LPCVD SiN can passivate and stabilize the N-polar GaN surface. It also increases the barrier height of the diode with a slight increment in the ideality factor. However, further increasing the SiN interlayer thickness to increase the barrier height is an unattractive solution, as it would eventually worsen the device's performance. With thicker SiN, the device would no longer be dielectric-assisted Schottky diode, and instead, it would turn to MIS-capacitor. In addition, the risk of dielectric breakdown at lower voltages would represent a bottleneck for high power SJ devices. Another solution to increase the barrier height would be to design a p-n diode. However, this is a bipolar device, in which the turn-on voltage and the reverse recovery would increase the conduction and switching losses, respectively. Instead of turning to a p-n diode, which would sacrifice the advantage of unipolar operation, a thin ionized charge layer can be deposited to create abrupt band banding and increase the barrier height. The device obtained via creating this potential hump in the band is called a "camel diode" [231–234]. This ionized charge layer can be realized with p-type doping on top of n-type N-polar GaN.

Achieving p-type doping is especially challenging in N-polar GaN as background oxygen and nitrogen vacancies (V_N) would compensate incorporated Mg dopants. In addition, the formation of hillocks due to the inversion domains on the N-polar GaN surface also hamper the device performance as the oxygen level might change around the hillocks [55, 111, 235].

To date, there have only been a few investigations on p-type doping in N-polar GaN, and most of those reports did not conduct a comprehensive electrical characterization of p-n diodes [236–239]. Also, so far, there are no reports on the camel diode in GaN technology.

In this chapter, p-type doping in N-polar GaN is demonstrated first. For that, consistent feedback was provided to the material grower via electrical characterization such as Hall measurements. Before realizing the camel diode directly, the N-polar GaN p-n diodes were designed and fabricated. A detailed electrical characterization of these diodes is then presented to investigate the incorporation of Mg and oxygen. The N-polar GaN diodes are also compared with Ga-polar GaN p-n diodes. This chapter provides theoretical design equations for the camel diodes validated with TCAD simulations. Based on these design rules, two different camel diodes were fabricated using different p^+ layer doping levels. Their electrical properties are presented and analyzed too.

5.2 N-polar GaN p-n Diode

5.2.1 p-type Doping in N-polar GaN

To investigate p-type conductivity in N-polar GaN, 0.5-μm-thick layer, doped with Mg, was grown on a *c*-plane sapphire with a 4° offcut towards the *m*-plane using MOCVD system. Immediately after the film growth, a Mg activation anneal was performed *in-situ* at 900 °C under N_2 ambient and UV illumination for 20 min. This annealing step dissociates H from the neutral Mg-H complex and activates Mg as an acceptor charge [240, 241]. After the activation anneal, Ni/Au (20/40 nm) were deposited via e-beam evaporated as metal contacts in the van der Pauw geometry for Hall measurements. The contacts were then annealed at 600 °C for 10 min in air ambient to obtain ohmic behavior. Figure 5.1 shows the temperature-dependent Hall effect measurements performed using an 8400 series LakeShore

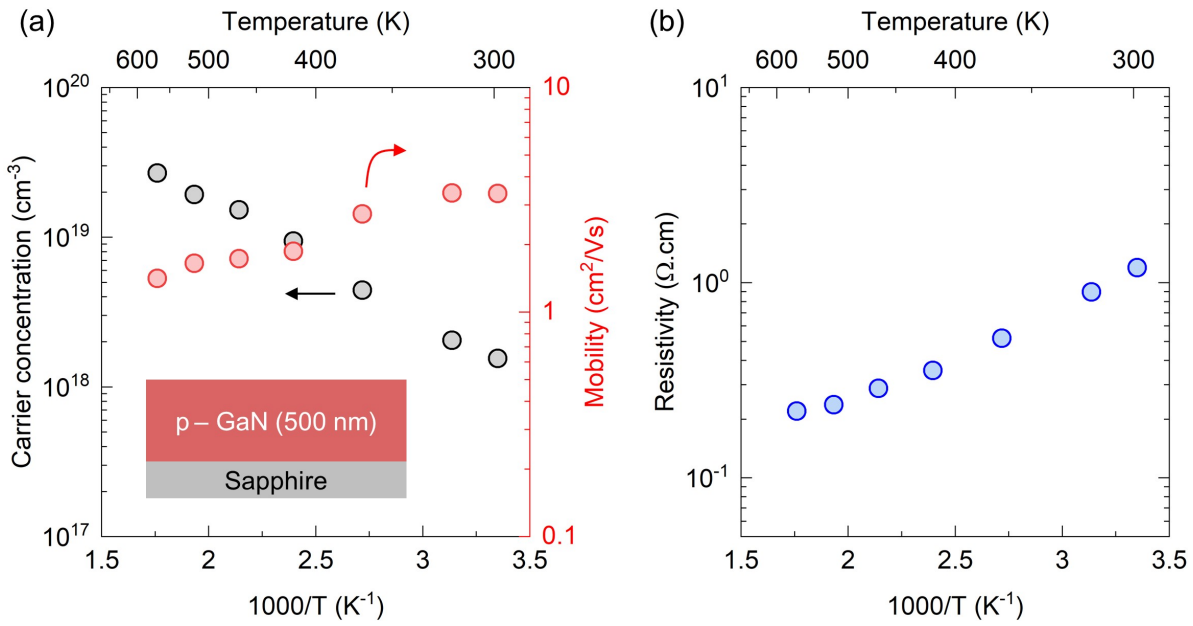

Figure 5.1: Temperature-dependent (a) free hole carrier concentration (black), mobility (red), and (b) resistivity for p-type N-polar GaN film measured via AC Hall. The inset of (a) shows the schematic cross-section of the grown film.

AC/DC Hall measurement system. A hole carrier concentration of $\sim 1.5\times10^{18}$ cm^{-3}, mobility of $\sim$3.4 cm^2/Vs, and resistivity of $\sim$1.2 Ω·cm are measured at room temperature ($\sim$300 K), as shown in Figs. 5.1(a) and 5.1(b). These results are comparable to the reported values for the p-type doping in Ga-polar GaN [241, 242]. As per the graphs, at 573 K, the hole carrier concentration increases to $\sim 3\times10^{19}$ cm^{-3}, mobility reduces to $\sim$1.4 cm^2/Vs, and resistivity reduces to $\sim$0.2 Ω·cm. The ionization energy of Mg is found to be $\sim$150 meV, which is comparable to the reported ionization energy for p-type Ga-polar GaN [242]. From the temperature-dependent Hall measurements, extracted compensation ratio is around $\sim$10%, which indicates that the concentrations of compensating oxygen and nitrogen vacancies are low. The Hall measurement results confirm that the p-type conductivity can be achieved in N-polar GaN. This achievement opens the door to designing, fabricating and testing N-polar GaN p-n and camel diodes, which is the focus of the following subsection.

5.2.2 Growth and Fabrication of p-n Diode

An N-polar GaN p-n diode structure was grown on a *c*-plane sapphire substrate with a 4° offcut towards the m-plane using a vertical, cold-wall, radio frequency (RF) heated, low-pressure MOCVD system. The p-n diode structure consists, bottom to top, of a 400 nm n^+-type layer (O: $>10^{19}$ cm^{-3}), a 400 nm n-type layer (O: $\sim 5\times10^{17}$ cm^{-3}), and a 300 nm p^+-type layer (Mg: $\sim 3\times10^{19}$ cm^{-3}). Immediately after film growth, Mg was activated via an *in-situ* anneal at 900 °C under N_2 ambient and UV illumination for 20 min. As a reference or control, an equivalent Ga-polar GaN structure was also grown. Since Ga-polar GaN does not incorporate oxygen unintentionally, Si was introduced during the n^+- and n-type layer growth. Due to growth limitations, the Si doping level in the n^+-type layer was somewhere in the range of mid to high 10^{18} cm^{-3}.

The p-n diode fabrication process on both Ga- and N-polar GaN started with the ohmic metal contact for the p^+-type layer. For that, Ni/Au (20/40 nm) metal contacts were deposited using an e-beam evaporation system (base pressure: 10^{-9} Torr). After the deposition, the devices were alloyed at 600 °C for 10 min in air ambient to obtain ohmic contacts to p^+-GaN. Then mesa etching was done using Cl_2-based inductively coupled plasma reactive ion etching (ICP-RIE) to access the bottom n^+-type layer. During the mesa etching, it was observed that the etch rate for Ga-polar GaN is around 8 to 10 nm/min lower than N-polar GaN even though the same etching recipe was used. Due to that, the mesa height in N-polar GaN was around 750 nm to 800 nm, whereas the mesa height in Ga-polar GaN p-n diode resulted around 600 nm to 650 nm. Then the large area ohmic contact for the n^+-type GaN layer was formed with Ti/Al/Ni/Au (30/100/70/70 nm) using the same e-beam evaporation system. It should be noted that the n^+-contacts were not alloyed after the deposition as the contacts were large in area and deposited on a highly doped layer. The schematic cross-section of the fabricated N-polar GaN p-n diode is shown in Fig. 5.2(a). Also, a tilted-side SEM image

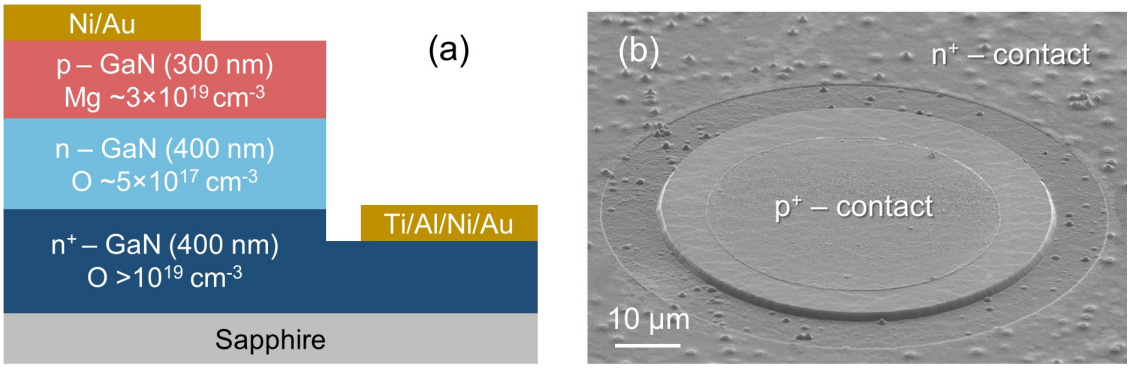

Figure 5.2: (a) The schematic cross-section and (b) a tilted-side SEM image of fabricated N-polar GaN p-n diode.

of the fabricated N-polar GaN p-n diode is shown in Fig. 5.2(b). It should be noted that the cathode contact for Ga-polar GaN diodes is on the n-type layer instead of the n^+-type layer due to the mesa height mismatch in both cases. This may affect the series resistance part of the p-n diode, which is discussed later in this section. In addition to the p-n diodes, 100×200 μm^2 contact pads on the p^+-type surface were made for transfer length method (TLM) measurements on both samples.

5.2.3 Electrical Results and Analysis

Figure 5.3(a) compares the current-voltage (I-V) characteristics for both Ga- and N-polar GaN p-n diodes measured at room temperature. The electroluminescence spectra of N-polar GaN was obtained at 8 V forward bias, as shown in Fig. 5.3(b). The electroluminescence response shows near band edge emission for GaN, which confirms the presence of free holes and thus p-type conductivity in N-polar GaN film. From the room-temperature I-V, the ideality factors (n) for Ga- and N-polar GaN diodes are extracted, which are 2.54 and 3.13, respectively. The higher ideality factors in both diodes could be due to the leakage current through the dislocations in the film [243, 244]. The N-polar GaN diode has a higher ideality

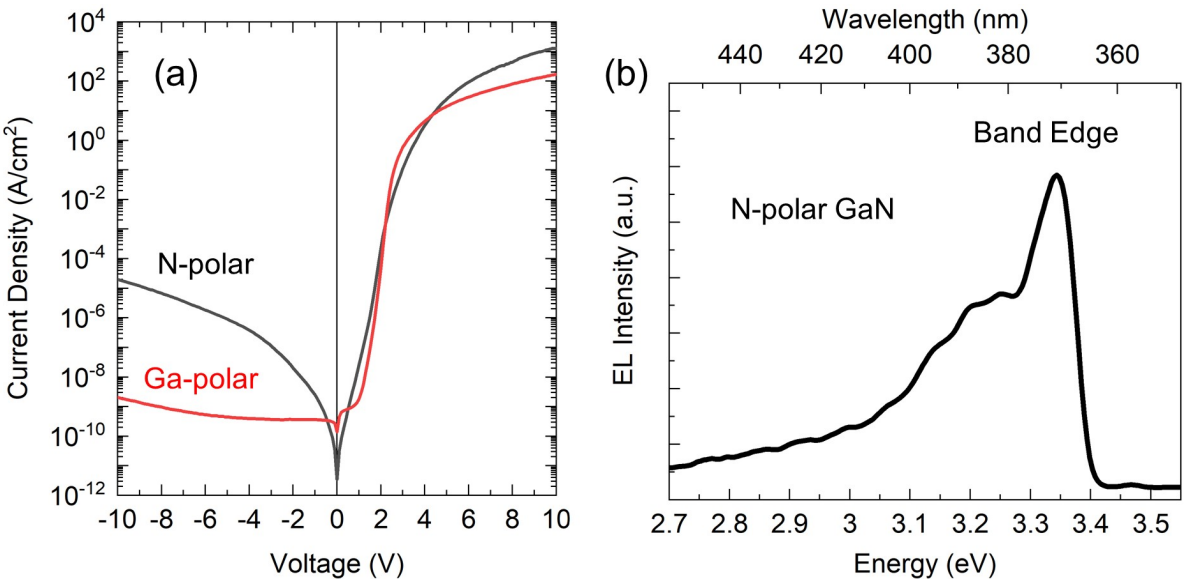

Figure 5.3: (a) Room-temperature I-V characteristics comparison of Ga- and N-polar GaN p-n diodes. (b) Electroluminescence spectra of N-polar GaN p-n diode measured at 8 V in forward bias.

factor than the Ga-polar diode, again due to higher dislocation density and/or presence of inversion domains in N-polar GaN. This could also be responsible for the higher reverse bias leakage in the N-polar GaN diode than Ga-polar, as seen in Fig. 5.3(a). The graph shows, at higher forward biases, the current in N-polar GaN is almost one order higher than the Ga-polar GaN. This could be due to the one-order low n^+-layer doping in Ga-polar ($\sim 5\times10^{18}$ cm^{-3}) than N-polar ($>10^{19}$ cm^{-3}) and the difference in mesa heights for both diodes, as mentioned previously.

From Fig. 5.3(a), it is observed that the current in N-polar GaN at forward biases from 3 V to 6 V has a sublinear transition instead of a sharp transition from exponential to series resistance regime, which is seen in the Ga-polar diode case. This current limiter in N-polar GaN could be due to the presence of a native interfacial oxide between the anode contact and p^+-layer or a highly compensated layer between p^+- and n-type N-polar GaN layer as a result of growth non-ideality, or both. A detailed investigation of this hypothesis is performed via different electrical measurements and discussed throughout this section.

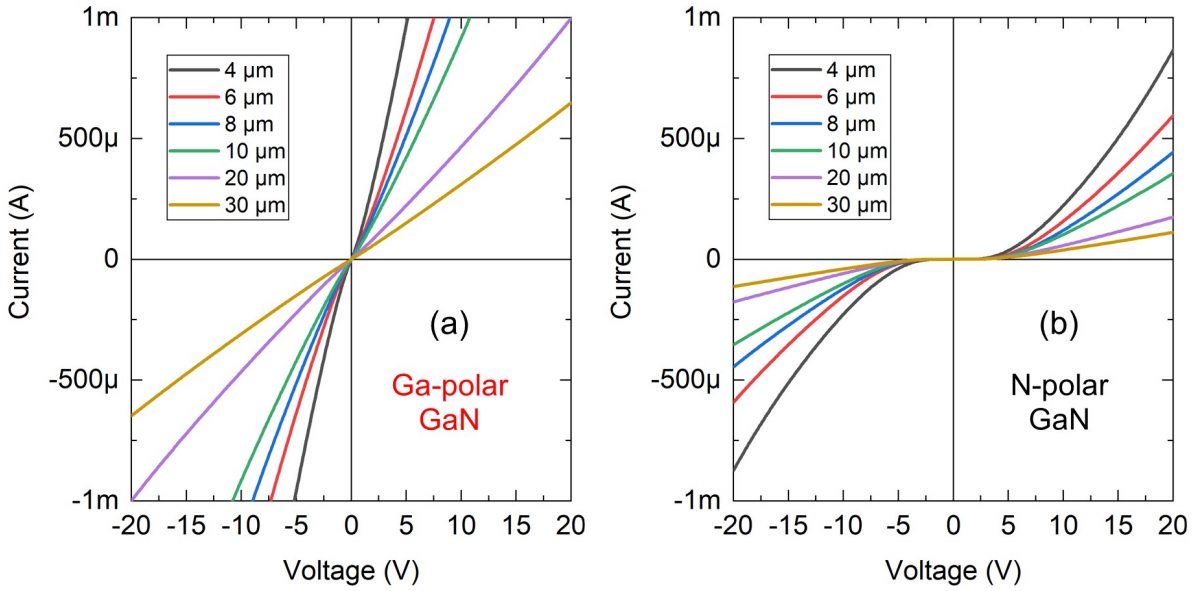

Figure 5.4: TLM measurements measured via alloyed Ni/Au contacts on the p^+-type layer for (a) Ga- and (b) N-polar GaN p-n diode structure with various contact separations.

To investigate the hypothesis, TLM measurements were performed on the p^+-GaN layer of the p-n diode using alloyed Ni/Au contacts. Figures 5.4(a) and 5.4(b) show the TLM data measured with different contact separations for Ga- and N-polar GaN, respectively. The alloyed contacts for the Ga-polar GaN case show linear I-V, as seen in Fig. 5.4(a). The alloyed contacts in N-polar GaN show Schottky-type behavior with turn-on at around 3 V, as seen in Fig. 5.4(b). This suggests that a current limiting layer is located between the N-polar GaN and metal contacts and prevents linear ohmic contacts from being obtained. It is postulated that this layer is a native oxide.

Figures 5.5(a) and 5.5(c) show temperature-dependent I-V characteristics for Ga- and N-polar GaN, respectively. The energy bandgap for both cases can be extracted using the following equation [245, 246]:

$$J_0 \propto \exp\left(-qE_g/nkT\right) \tag{5.1}$$

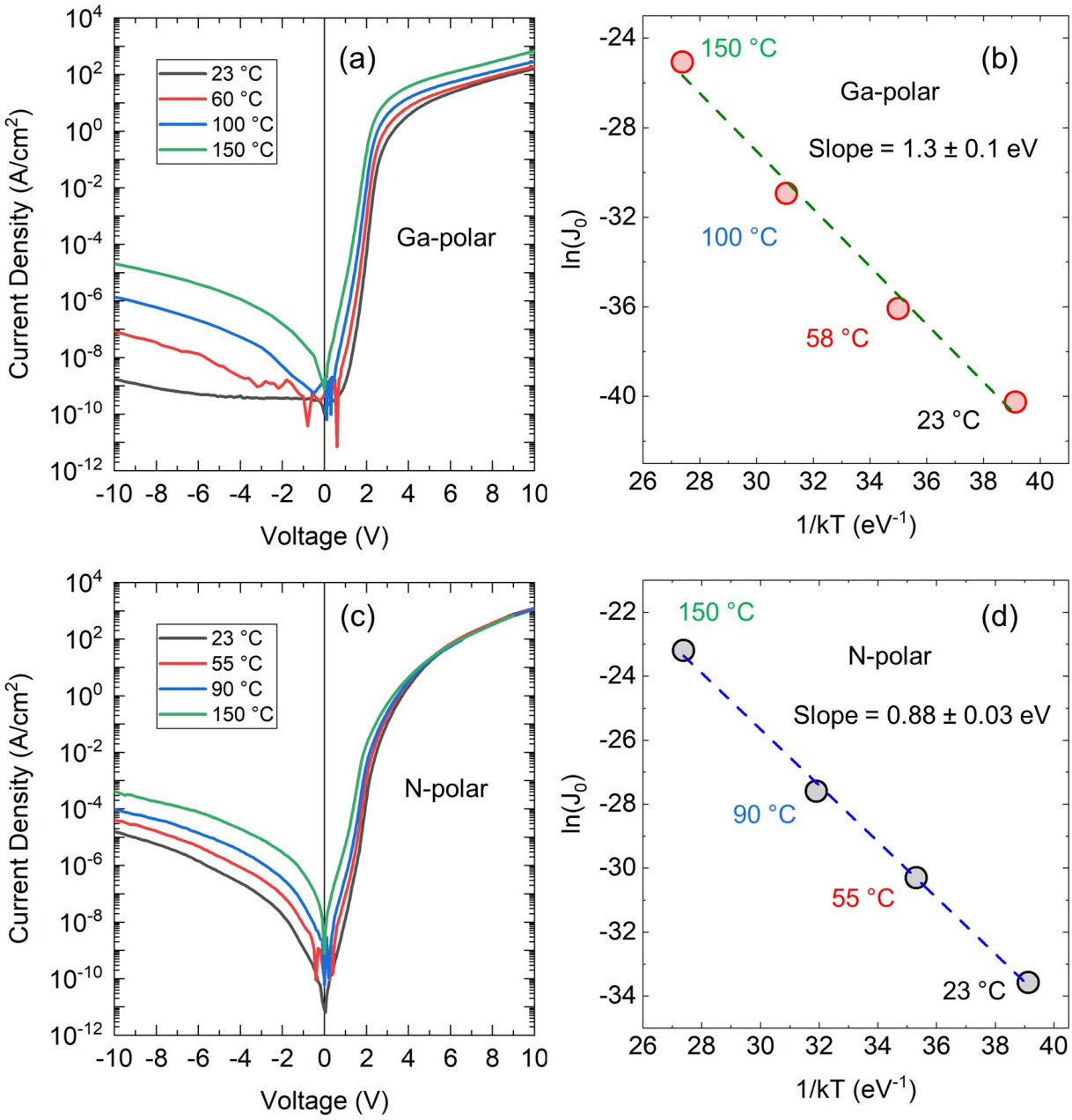

Figure 5.5: Temperature-dependent I-V characteristics and $\ln(J_0)$, extracted from forward bias between 2 V to 3 V at each temperature, vs. 1/kT for Ga-polar (a & b) and N-polar (c & d) GaN.

where, J_0 is the saturation current, q is the elementary charge, E_g is the energy bandgap, n is the ideality factor, k is the Boltzmann constant, and T is the temperature. The saturation current is extracted by extrapolating the current from the exponential region where the

ideality factor value is lowest (between 1.5 V to 2 V in forward bias) in both cases. Thus, based on the Eq. 5.1, E_g/n can be calculated by plotting $\ln(J_0)$ vs. $1/kT$ graph. Figures 5.5(b) and 5.5(d) show the $\ln(J_0)$ vs. $1/kT$ for Ga- and N-polar GaN, respectively, where the slope of the graph provides the E_g/n value. Using the ideality factor values at room temperature for both diodes, the estimated E_g values, at room temperature, for Ga- and N-polar GaN diodes are 3.3 eV and 2.75 eV, respectively. The value extracted for the Ga-polar GaN case agrees with the bandgap of GaN. However, the estimated energy gap obtained for N-polar GaN is lower than the bandgap of GaN. This suggests that there might be parallel current paths to the fabricated N-polar GaN p-n junction due to the defects or inversion domains. Interestingly, these low-barrier parallel current paths are also masked at the higher forward biases in the N-polar GaN as the current is low (sublinear rise instead of sharp transition from exponential to series resistance) at higher forward biases [see Fig. 5.3(a)]. Thus, it is proposed that a current limiter impacts the performance at high forward bias and that it is located either at the surface and/or between p^+- and n-type layers.

To investigate further, capacitance-voltage (C-V) measurements were done on both diodes using a parallel RC circuit model at 1 MHz frequency. The $1/C^2$-V characteristics for both Ga- and N-polar GaN diodes are plotted and shown in Fig. 5.6(a). The doping as a function of applied bias is also extracted and shown in Fig. 5.6(b) for both cases. As the diode structure in both cases is a p^+-n diode, the extracted doping should be the doping in the n-type layer for both diodes as the charge would be modulated only in the lower doped region with the applied bias. The N_D-N_A in the n-type layer for Ga- and N-polar diodes are $\sim 1.5\times10^{17}$ cm^{-3} and $\sim 3.5\times10^{17}$ cm^{-3}, respectively, as seen in Fig. 5.6(b).

From the $1/C^2$-V graph, it is seen that the built-in potential for Ga-polar diode is 3.4 V, which agrees with the estimated value extracted from temperature-dependent I-V, as reported earlier. For the N-polar case, the extracted built-in potential from $1/C^2$-V is 3.8 V,

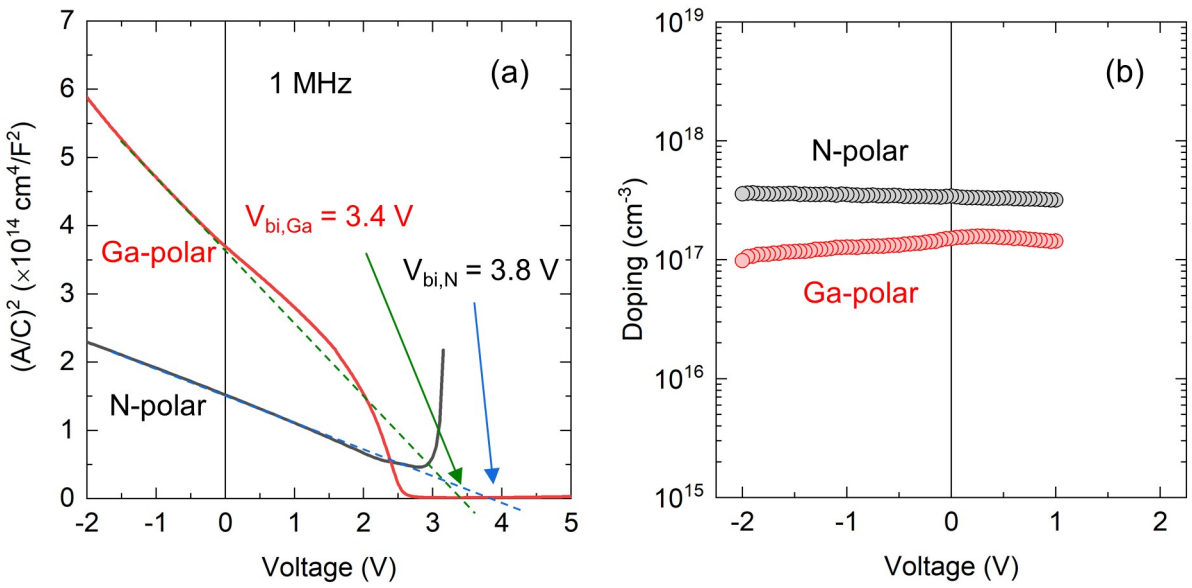

Figure 5.6: (a) Capacitance-voltage characteristics and (b) The extracted doping vs. voltage profile for both Ga- and N-polar GaN p-n diodes.

which is not only higher than the extracted value from temperature-dependent I-V but also in agreement with the bandgap of GaN. The higher built-in potential obtained by C-V could be due to an additional capacitance either from the surface native oxide between the anode metal and p^+-type layer and/or from the compensated insulating layer within the p-n diode. It appears that C-V is less sensitive to the presence of low-barrier parallel current paths revealed by the I-V in Fig. 5.5.

From Fig. 5.6(a), for the Ga-polar case, it is seen that the $1/C^2$ starts reducing at 1.5 V forward bias and becomes constant at 2.5 V forward bias. This is due to the increment in capacitance as a result of the decrement in depletion width with the applied forward bias. At 2.5 V forward bias, the depletion region is almost negligible, and thus $1/C^2$ is negligible. After 2.5 V forward bias, no change in $1/C^2$ is observed, probably due to no further modulation of depletion. Also, after that bias, the conductance takes over the capacitance due to the charge injection. However, in the N-polar GaN diode, the $1/C^2$ does not go to zero, and

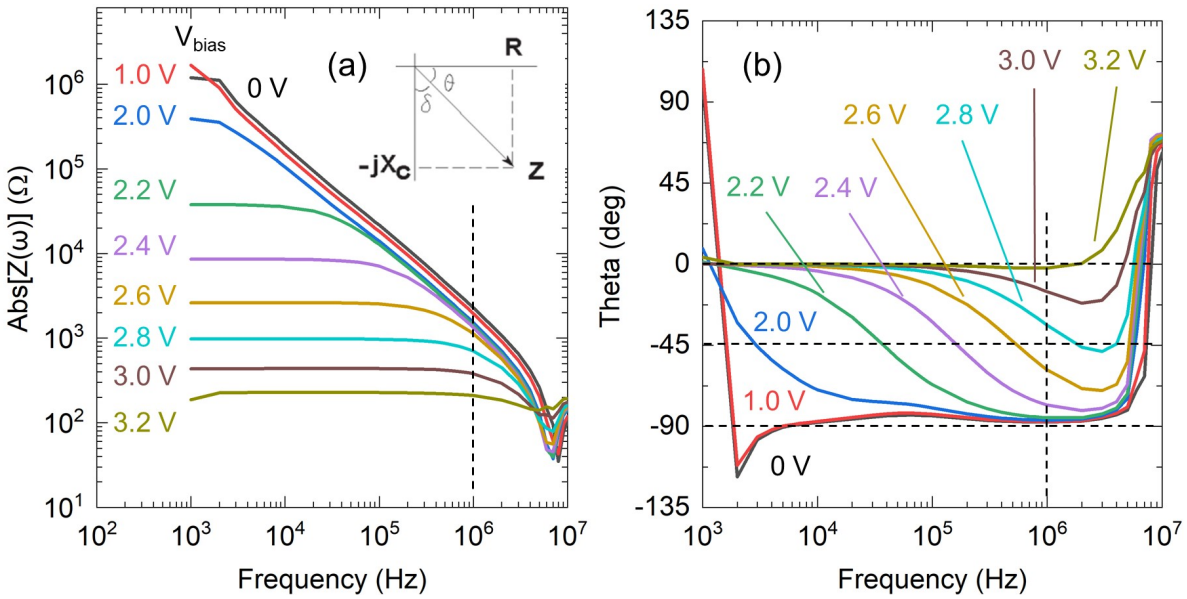

Figure 5.7: Z-theta measurements for N-polar GaN p-n diode with (a) impedance vs. frequency and (b) theta vs. frequency at different forward biases from 0 V to 3.2 V.

instead, it rises after a 2.8 V forward bias. Two things should be noted here. First, the $1/C^2$ not being zero indicates the presence of a fixed capacitance in the circuit, which could arise for the aforementioned reasons. Second, the conductance takes over the capacitance after 2.8 V, and the RC bridge is not balanced after that bias point. The latter part is seen in the Z-theta measurement for the N-polar GaN diode, as shown in Figs. 5.7(a) and 5.7(b). These graphs show that, at 1 MHz, the impedance starts reducing, and the theta changes from -45° to 0° after a 2.8 V forward bias. These results prove that the conductance takes over the capacitance after 2.8 V at 1 MHz in C-V measurements.

To investigate the thickness of the constant depletion layer, the depletion width as a function of applied bias is extracted. In Fig. 5.8, this is done while assuming a dielectric constant of 10.4 to represent GaN. This assumption represents the case that the depletion layer is located between the p^+- and n-GaN regions. The graph shows that the remaining depletion thickness, at forward bias higher than 2.8 V, in Ga-polar GaN is 8 nm and in

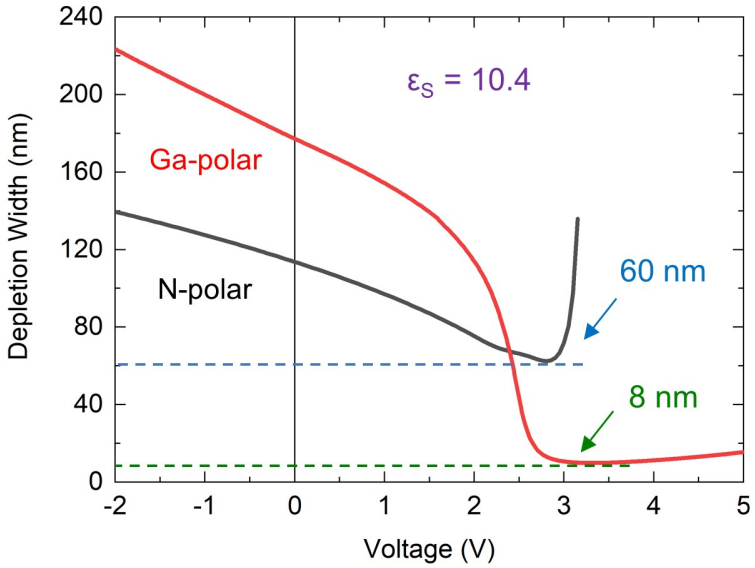

Figure 5.8: Depletion width vs. voltage extracted from C-V measurements using GaN dielectric constant 10.4 for both Ga- and N-polar GaN diodes.

N-polar GaN is 60 nm. Thus, if any compensated or insulating GaN layer is present in the p-n diode structure, that layer should be 8 nm and 60 nm for Ga- and N-polar GaN, respectively. A similar calculation can be conducted to capture the effect of a surface oxide located in between the anode metal and p^+ layer. In this case, it is assumed that the oxide is gallium oxide with a dielectric constant of 3.57 [247]. The resulting interlayer has an estimated thickness of 2 nm and 20 nm for Ga-polar and N-polar GaN, respectively.

Thus, from the N-polar GaN C-V measurements, it is observed that there is a constant capacitance layer present in the p-n diode after 2.8 V. And, after that bias, the current might be flowing through that contact capacitance region. This explains why the current, after that bias in the I-V [see Fig. 5.3(a)], flows with some power-law to voltage, which could be Poole-Frenkel or space charge limited current. Considering this capacitance is only due to the native oxide interlayer, it is very thin in the Ga-polar GaN diode; however, it is significant in the N-polar GaN diode.

To investigate the presence of a native oxide interlayer, secondary ion mass spectroscopy

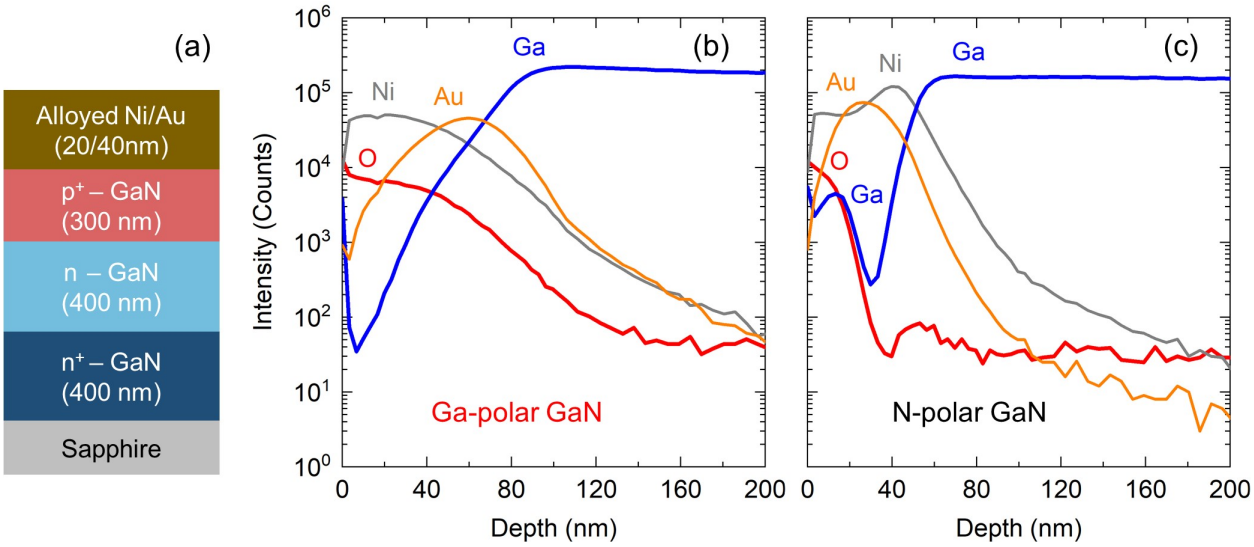

Figure 5.9: (a) The schematic cross-section of the analyzed structure under secondary ion mass spectroscopy (SIMS). The intensity vs. depth for (b) Ga- and (c) N-polar GaN measured via SIMS.

(SIMS) is performed on both samples, as shown in Fig. 5.9. The schematic cross-section of the analyzed area under the SIMS is shown in Fig. 5.9(a). It should be noted that the SIMS was done after the Ni/Au contact alloying step for both p-n diodes. For p-GaN ohmic contact formation, it is usually observed that Ni and Au interchange places after contact alloying in air ambient. In this process, Ni mixes with oxygen from the air and forms nickel oxide, allowing Au to diffuse in and mix with Ga [248]. Figures 5.9(b) and 5.9(c) show Ni, Au, Ga, and O intensity as a function of the depth for Ga- and N-polar GaN p-n diodes, respectively. In the case of Ga-polar GaN diode, SIMS confirms the forming of nickel oxide as Ni and O intensity curves follow each other, as shown in Fig. 5.9(b). It can be observed that this nickel oxide allowed Au to diffuse, and thus the peak intensity of Au is seen between Ni and Ga peaks. In comparison, in the N-polar GaN p-n diodes, Ni and Au did not switch places. Instead, a Ga peak is observed near the surface with O, indicating the formation of gallium oxide in the N-polar GaN diode, as shown in Fig. 5.9(c). The thicknesses of the Ga and O peaks are around 20 nm. This thickness matches the extracted oxide interlayer thickness via

C-V, suggesting that the native oxide interlayer could be the reason for additional capacitance. This native oxide layer might be formed during the Mg activation anneal, or p-type metal contact anneal, which needs further investigation and left for future work.

In addition to the intensity profile, SIMS atomic concentration depth profiles for both Ga- and N-polar GaN were performed. Figures 5.10(a) and 5.10(b) show Mg concentration (right y-axis) as a function of depth for Ga- and N-polar GaN p-n diode, respectively. The left y-axis shows the same intensity of different atoms in the graph, which are presented in Fig 5.9. Now, looking at the Mg depth profiles in both diodes, it is observed that the Mg concentration is not constant throughout the p^+-GaN layer. The intended Mg doping in both structures was $\sim 3\times10^{19}$ cm^{-3} within 300 nm of p^+-GaN film. However, the SIMS depth profile reveals that Mg concentration is constant only for total depth around 250 nm for both Ga- and N-polar GaN. As per the SIMS, the peak Mg concentrations for Ga- and N- polar GaN are around $\sim 2\times10^{19}$ cm^{-3} and $\sim 4\times10^{19}$ cm^{-3}, respectively. Both samples show a delay in Mg incorporation before it reaches the steady-state doping value in the film when p^+-GaN layer growth starts after the n-GaN layer. This delay in Mg incorporation is a well-established challenge in GaN growth [249–251]. In addition, thermal diffusion of Mg atoms towards the n-GaN layer might be possible during the growth. For both Ga- and N-polar GaN samples, the delay rate in Mg incorporation is about 100 nm/decade. It is important to note that even though the O intensity level in both Ga- and N-polar GaN are at the same level after 100 nm depth, the level of O incorporation in both polarities is not the same. Also, the measured O intensity in both cases after 100 nm depth is the noise level of the SIMS instrument used here.

As mentioned before, N-polar GaN always incorporates oxygen unintentionally, even during the p^+-type layer growth. Thus, it could be possible to have a compensated region in the N-polar GaN p-n diode. The compensated region could be where Mg rises to its steady-state doping value, which might be compensated by unintentional oxygen. So, the

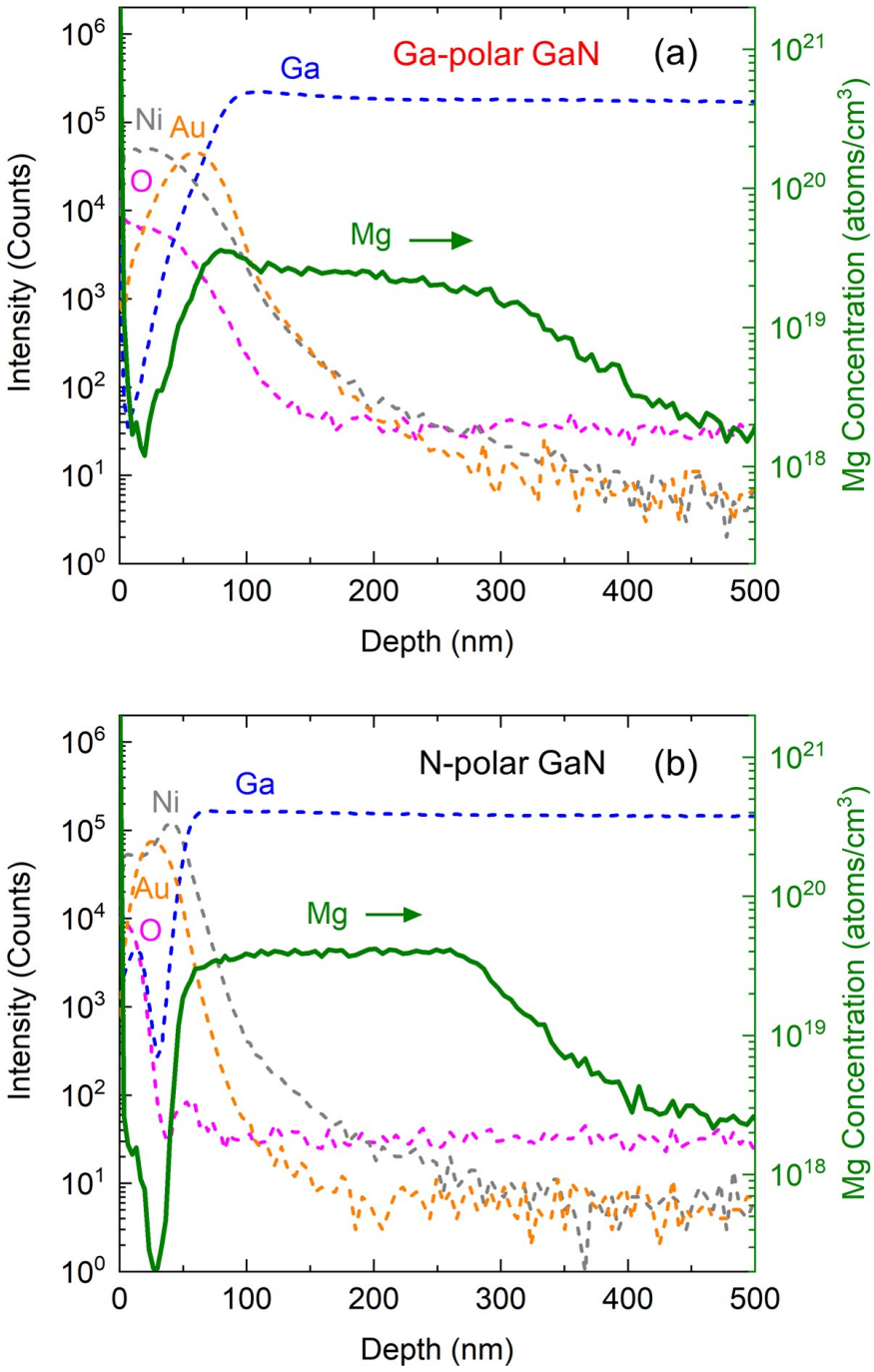

Figure 5.10: Mg concentration depth profile (right y-axis) obtained using SIMS for (a) Ga- and (b) N-polar GaN p-n diodes.

reason for the sublinear current in the N-polar GaN p-n diode at higher forward biases might be due to a presence of either native oxide interlayer at anode metal and a p^+-GaN layer or the compensated GaN layer or both.

Figure 5.11(a) shows the modified schematic cross-section of the N-polar GaN p-n diode based on the discussed probable causes for the deviation in the measured I-V characteristics. Figure 5.11(b) shows the N-polar GaN I-V characteristics with the ideal current path in the forward bias. It is seen that, at lower forward bias voltages, the current is higher due to the inversion domains and dislocations. At higher forward biases, current increases in a sublinear manner deviating from the ideal current path. As mentioned before, this is due to the presence of the native oxide at the metal and p^+-GaN interface or compensated layer between the p^+- and n-GaN.

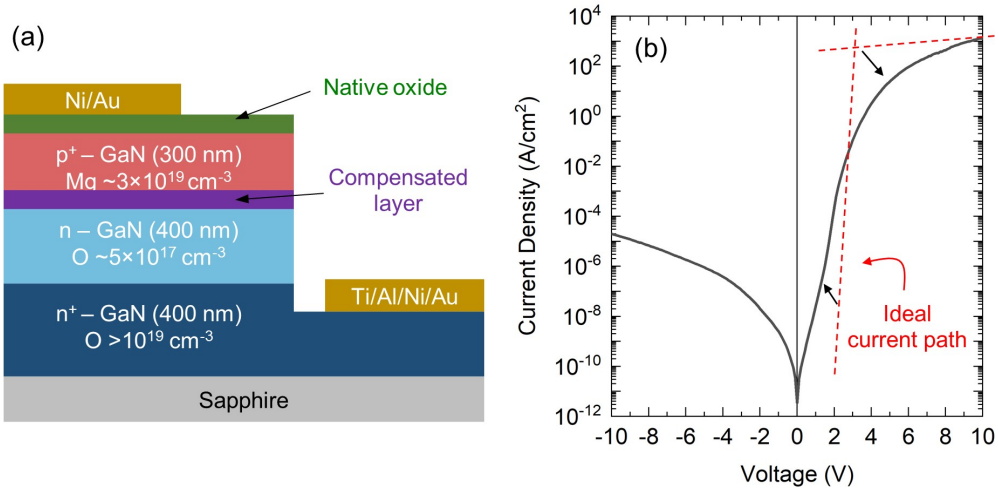

Figure 5.11: (a) The modified schematic cross-section of the N-polar GaN p-n diode based on the I-V characteristics. (b) Room temperature I-V characteristics of N-polar GaN p-n diode compared to the ideal current path in forward bias.

5.2.4 Summary

In summary, p-type conductivity was achieved in N-polar GaN and confirmed via hall measurements. This prompted the fabrication of N-polar GaN p-n diodes. Higher ideality factor and reverse leakage current were observed at room temperature in N-polar GaN p-n diodes compared to reference Ga-polar GaN p-n diodes. The bandgap extracted from I-V-T for N-polar p-n diodes shows a lower value than the bandgap of GaN, which is attributed to the presence of a parallel leakage current path. This leakage path could be related to the defects and/or inversion domains in N-polar GaN. The N-polar GaN p-n diode I-V reveals a presence of the current limiter at biases above 3 V. This could be due to either native oxide interlayer at anode metal and a p^+-GaN layer or the compensated GaN layer region or both, based on the analysis of different electrical characteristics. The native oxide could be resulted from the Mg activation anneal or during the Ni/Au contact annealing in the ambient air. In comparison, the compensated GaN layer could be formed due to the delay in Mg rise, which is compensated by unintentional oxygen in N-polar GaN.

5.3 N-polar GaN Camel Diode

The results presented in Section 5.2 demonstrate the ability to p-type dope N-polar GaN, which represents an important technological milestone. While the p-n diode was used to investigate this capability, there are performance trade-offs to consider when comparing it to the Schottky diode studied in Chapter 3. P-n diodes benefit from improved breakdown capability due to the larger barrier and reduced reverse bias leakage current. However, the higher turn-on voltage and reverse recovery time also increase the conduction and switching losses of the circuit. Therefore, this section investigates a third device known as the camel diode. In these devices, the barrier height can be controlled using a potential hump, created

by a thin and fully depleted p^+ layer in the bulk of semiconductor while maintaining the majority-carrier current flow in the diode. This potential hump can be controlled by controlling the thickness and doping of this p^+ layer. This allows tuning the barrier height value between the Schottky and p-n diode barrier.

Early work on controlling the Schottky barrier heights were reported by Shannon [232,233]. The Schottky barrier to n-type and p-type Si diodes were raised by introducing shallow and fully depleted p^+ and n^+ layers, respectively, near the surface and beneath the Schottky metal. Later, this fully depleted layer was sandwiched between highly doped and low doped layers. For example, Shannon reported the camel diode with a thin p^+ layer sandwiched between n^{++} and n^- layers in Si [234]. Throne *et al.* utilized the same concept and realized camel gate GaAs field-effect transistors where the barrier height of the gate contact was increased by adding a p^+ GaAs layer in between n^+ and n^- GaAs layer [252].

In this thesis, a similar type of framework is applied to N-polar GaN material to increase the barrier height from its Schottky limit while avoiding p-n diode formation and maintaining the camel diode's unipolar nature. This camel diode structure can then be utilized in the GaN SJ design to increase the barrier height of the N-polar domain. More details on the GaN SJ design using camel diode structure are presented in Chapter 6.

As shown in the previous section, the successful demonstration of p-type N-polar GaN enables the realization of the camel diode in N-polar GaN. Instead of sandwiching the p^+ layer between n^+ and n^- layer, only the p^+ layer is deposited on an n-type layer to tune the barrier height in this work. To this end, first, the theoretical model of N-polar GaN is developed to predict the barrier height for a particular thickness and doping of the p^+-GaN layer. The theoretical model is verified using Silvaco TCAD simulations. Later, the experimental results on N-polar GaN camel diodes with two different p^+-GaN layer doping are provided.

5.3.1 Design Space for GaN Camel Diode

The theory behind the camel diode operation was first developed by Shannon [234]. A small number of later reports have also been published in the literature detailing how the barrier heights and ideality factors can be calculated for camel diodes [231, 252]. The schematic cross-section of the camel diode structure and its energy band diagram is shown in Fig. 5.12. The graph shows that the potential hump in the conduction band between a degenerate region (n^{++}) in the semiconductor and the lightly doped n^- layer is formed using a thin and highly doped p^+ layer.

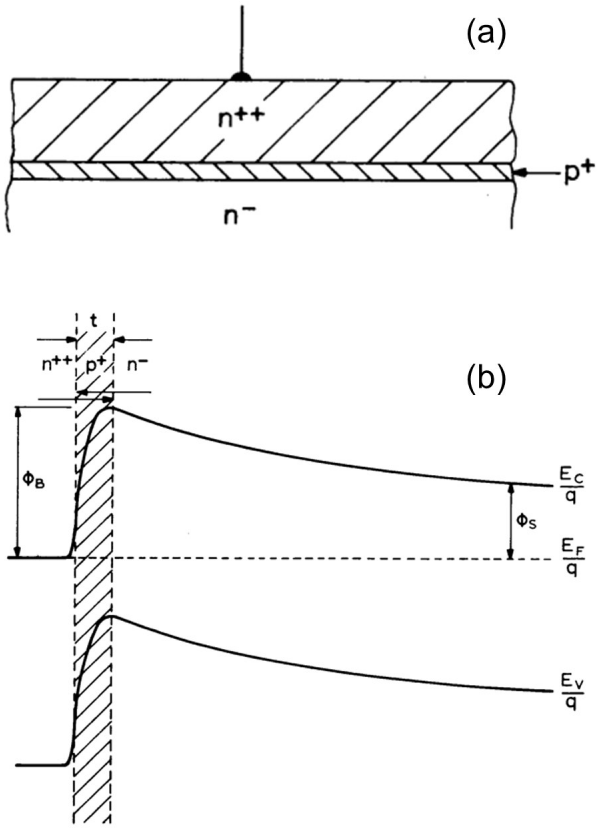

Figure 5.12: (a) The schematic cross-section of the camel diode structure. (b) The energy band diagram of the camel diode structure showing the potential hump. Figure from [231].

The doping and thickness for the p^+ layer are chosen so that it is fully depleted of holes at all values of the bias across the diode. In short, the p^+ layer must always be depleted, in other words [234]:

$$\frac{qt^2N_A}{2\varepsilon_S} < \frac{E_g}{q} \tag{5.2}$$

where, t and N_A are the thickness and doping of the p^+ layer, E_g is the bandgap of the material, q is the elementary charge, and ε_S is the dielectric permittivity of the material. The barrier height of the camel diode structure, shown in Fig. 5.12, can be calculated by solving the Poisson's equation, given as [252]:

$$\phi_B = \frac{qN_A^+}{2\varepsilon}\left(t - \frac{WN_D}{N_A^+}\right)^2 + \frac{qN_D^+}{2\varepsilon}\left[\frac{N_A^+}{N_D^+}\left(t - \frac{WN_D}{N_A^+}\right)\right]^2 \tag{5.3}$$

where, ϕ_B is the barrier height of the camel diode, N_A^+, N_D^+, and N_D are the doping concentrations in p^+, n^{++}, and n^- layers, respectively, t is the thickness of p^+ layer, and W is the depletion region in the n^- layer at zero bias. The depletion width (W), at zero bias, in n^- layer depends on the barrier height of the camel diode, which can be obtained by solving the following Poisson's equality [252]:

$$\frac{qW^2N_D}{2\varepsilon} + \frac{qN_A^+}{2\varepsilon}\left(\frac{WN_D}{N_A^+}\right)^2 + \phi_S = \frac{qN_A^+}{2\varepsilon}\left(t - \frac{WN_D}{N_A^+}\right)^2 + \frac{qN_D^+}{2\varepsilon}\left[\frac{N_A^+}{N_D^+}\left(t - \frac{WN_D}{N_A^+}\right)\right]^2 \tag{5.4}$$

where, ϕ_S is the Fermi potential in the n^- layer. Using Eqs. 5.3 and 5.4, the barrier height for the camel diode can be calculated theoretically. As seen in these equations, this mainly depends on the thickness of the p^+ layer and the doping levels of p^+, n^{++}, and n^- layers.

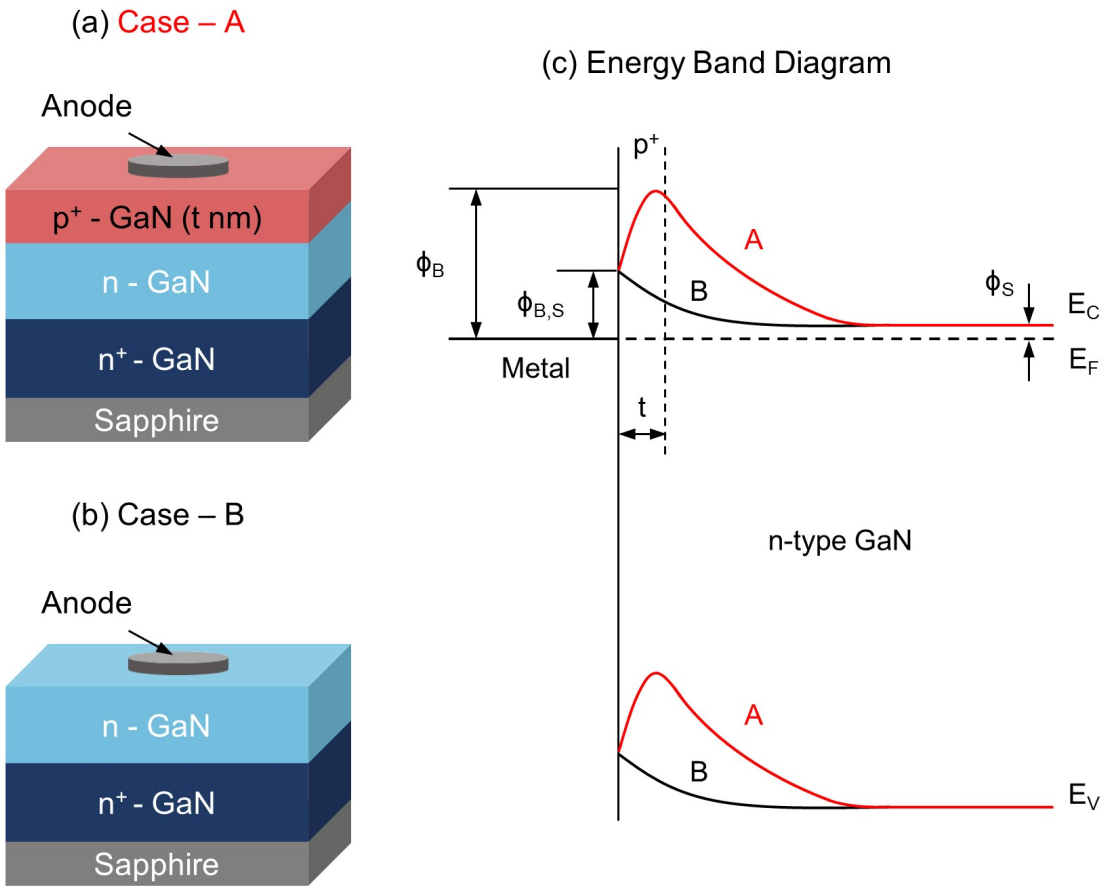

Figure 5.13: The schematic cross-section of the (a) camel and (b) Schottky diode structures. (c) Comparison of the energy band diagrams for both the diode structures.

The above-mentioned equations are for the camel diode structure shown in Fig. 5.12. However, in this work, the employed camel diode structure does not have an n^{++} layer at the top. Instead, due to the difficulties associated with abruptly ending Mg incorporation during epitaxy, the diode is designed with a thin p^{+}-GaN layer on top of the n-type GaN, as shown in Fig. 5.13(a), unlike the traditional Schottky diode structure shown in Fig. 5.13(b). The energy band diagram of both the structures is shown in Fig. 5.13(c). As shown in the band diagram, it can be observed that the barrier height for the camel diode rises due to the insertion of the p^{+} layer. It is important to note that the p^{+} layer in the camel diode design

stays fully depleted or ionized at all forward biases. Thus, there are no free holes available in the p^+ layer, and the conduction happens due to the injection of electrons (majority carriers) only.

The design equations are modified and reported below based on the camel diode structure, shown in Fig. 5.13(a), can be calculated using the following equation:

$$\phi_B = \phi_{B,S} + \frac{qN_A}{2\varepsilon}\left(t - \frac{WN_D}{N_A}\right)^2 \tag{5.5}$$

where, ϕ_B is the barrier height of the camel diode, $\phi_{B,S}$ is the barrier height of the n-type Schottky diode without any p^+ layer, N_A and N_S are the doping level in the p^+- and n-type layers, respectively. The depletion width (W) can be calculated by solving the following equality:

$$\frac{qW^2N_D}{2\varepsilon} + \frac{qN_A}{2\varepsilon}\left(\frac{WN_D}{N_A}\right)^2 + \phi_S = \phi_{B,S} + \frac{qN_A}{2\varepsilon}\left(t - \frac{WN_D}{N_A}\right)^2 \tag{5.6}$$

where, ϕ_S is the Fermi potential in the n^- layer. Using Eqs. 5.5 and 5.6, the barrier height for the N-polar GaN camel diode can be calculated theoretically.

According to the equations, the camel diode barrier height depends on three parameters: the thickness of the p^+ layer and doping levels of p^+ and n-type layers. In Fig. 5.14(a), the barrier height for the camel diode as a function of p^+ layer thickness (t) is calculated with constant doping in p^+ (N_A: 1×10^{19} cm^{-3}) and n-type (N_D: 5×10^{17} cm^{-3}) layers. It is assumed that the Schottky barrier height ($\phi_{B,S}$) for n-type N-polar GaN is 0.4 eV, which is based on the experimentally measured value presented in Chapters 3 and 4. As seen in the graph, the barrier height increases with increasing p^+ layer thickness. After 23 nm of p^+ layer thickness, the structure does not remain camel diode, instead, it becomes p-n diode. Silvaco ATLAS

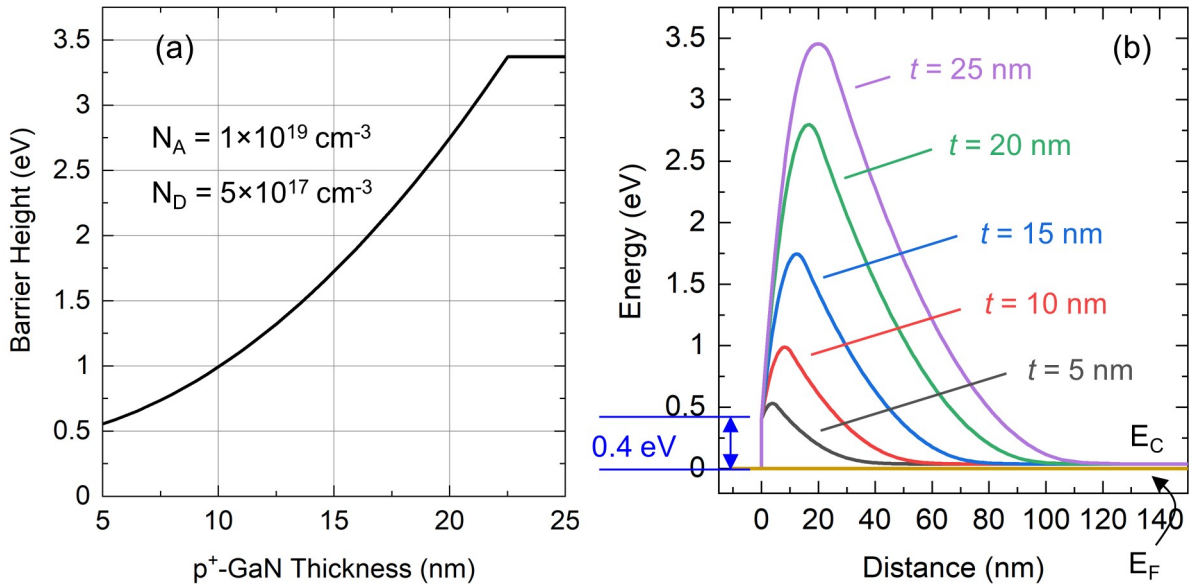

Figure 5.14: (a) Barrier height of the N-polar GaN camel diode as a function of p$^+$-GaN layer thickness with constant N_A and N_D calculated using the analytical equations. (b) Simulated N-polar GaN conduction band diagram for different p$^+$-GaN layer thickness with constant N_A and N_D.

simulations are performed to verify the barrier height values using the energy band diagram. Figure 5.14(b) shows the conduction band diagram of the camel diodes for different p$^+$ layer thicknesses with constant doping in p$^+$ (N_A: 1×10^{19} cm^{-3}) and n-type (N_D: 5×10^{17} cm^{-3}) layers. Again, N-polar Schottky barrier height is fixed to 0.4 eV in simulations. It should be noted that the analytical calculations and numerical simulations consider the doping in the p$^+$-type layer is constant throughout its thickness. From Figs. 5.14(a) and 5.14(b), it can be observed that the analytical calculations match the simulation results. Thus, these designed equations can predict the barrier height of the camel diode for the given design parameters mentioned above.

The barrier heights as a function of the p$^+$-GaN layer thickness for three different N_A values 5×10^{18} cm^{-3}, 1×10^{19} cm^{-3}, and 2×10^{19} cm^{-3} are calculated using design equations while keeping the n-type layer doping fixed (N_D = 5×10^{17} cm^{-3}), as shown in Fig. 5.15. As seen in the graph, the barrier height increases with the doping of the p$^+$ layer for the same p$^+$

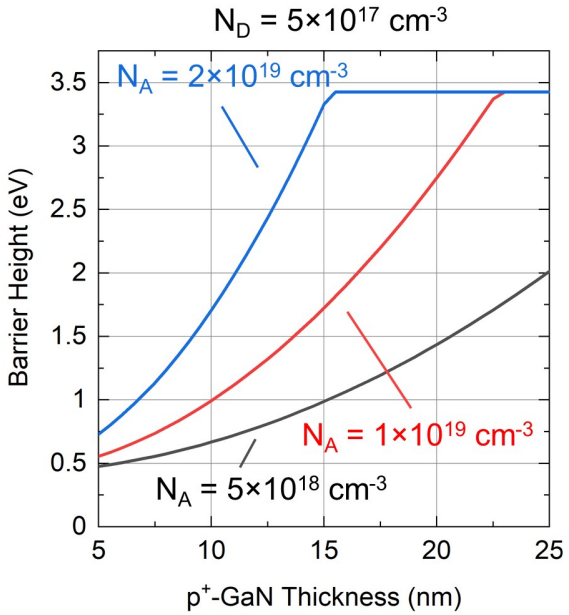

Figure 5.15: Barrier height of the N-polar GaN camel diode as a function of the p^+-GaN layer thickness for three different N_A with constant N_D.

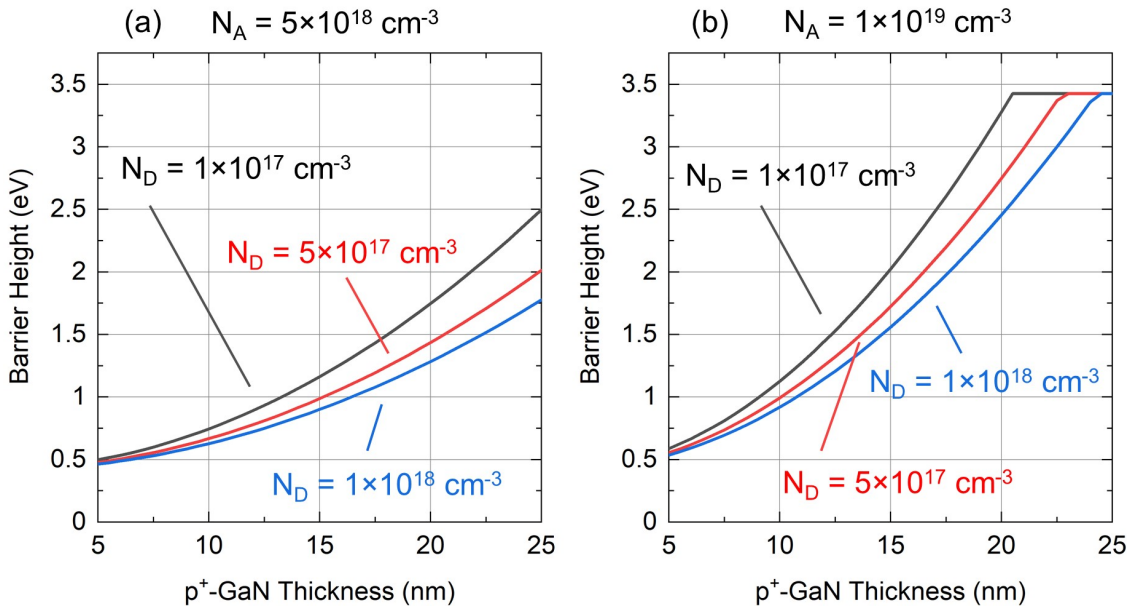

Figure 5.16: Barrier height of the N-polar GaN camel diode as a function of p^+-GaN layer thickness for three different N_D with constant (a) $N_A = 5\times10^{18}$ cm^{-3} and (b) $N_A = 1\times10^{19}$ cm^{-3}.

layer thickness. It is noticed that the diode turns into a p-n diode at lower p^+ layer thickness if the doping of that layer is relatively higher.

To understand the role of n-type layer doping on the camel diode barrier height, it is varied as a function of the p^+ layer thickness for a constant N_A. Figure 5.16(a) shows the barrier height values for three different n-type layer doping $N_D = 1\times10^{17}$ cm^{-3}, $N_D = 5\times10^{17}$ cm^{-3}, and $N_D = 1\times10^{18}$ cm^{-3} for fixed $N_A = 5\times10^{18}$ cm^{-3}. Similarly, Fig. 5.16(b) shows the barrier height values for three different n-type layers doping for fixed $N_A = 1\times10^{19}$ cm^{-3}. From these graphs, it can be observed that a lower n-type doping camel diode would have a higher barrier height.

The current-voltage and capacitance-voltage characteristics for the camel diodes are simulated using Silvaco. The I-V and C-V characteristics for the Schottky diode are also simulated for comparison. The C-V characteristics are simulated for 1 MHz frequency. Two different camel diode structures are simulated, where the doping in n-layer and the thickness of p^+ layer are kept constant, which are 5×10^{17} cm^{-3} and 10 nm, respectively. Two p^+ layer doping scenarios are considered: 5×10^{18} cm^{-3} (Diode C1) and 1×10^{19} cm^{-3} (Diode C2). The n-type doping in the Schottky diode structure (Diode S) is kept 5×10^{17} cm^{-3} also. The I-V characteristics of all three diodes are shown in Fig. 5.17(a). The threshold voltages for diodes S, C1, and C2 are ∼0.4 V, ∼0.6 V, and ∼1.1 V, respectively, as shown in Fig. 5.17(a) with dashed lines. These threshold voltages of simulated camel diodes match with the barrier height values shown in Fig. 5.15. Thus, as per the simulation results, it is evident that the camel diode structure can increase the barrier height from the Schottky counterparts. From Fig. 5.17(a), it is important to note that the on-resistance does not change even though the barrier is raised for camel diode as the doping level in the n-type drift region is the same for all cases.

The $1/C^2$-V characteristics of all three diodes are shown in Fig. 5.17(b). The extracted

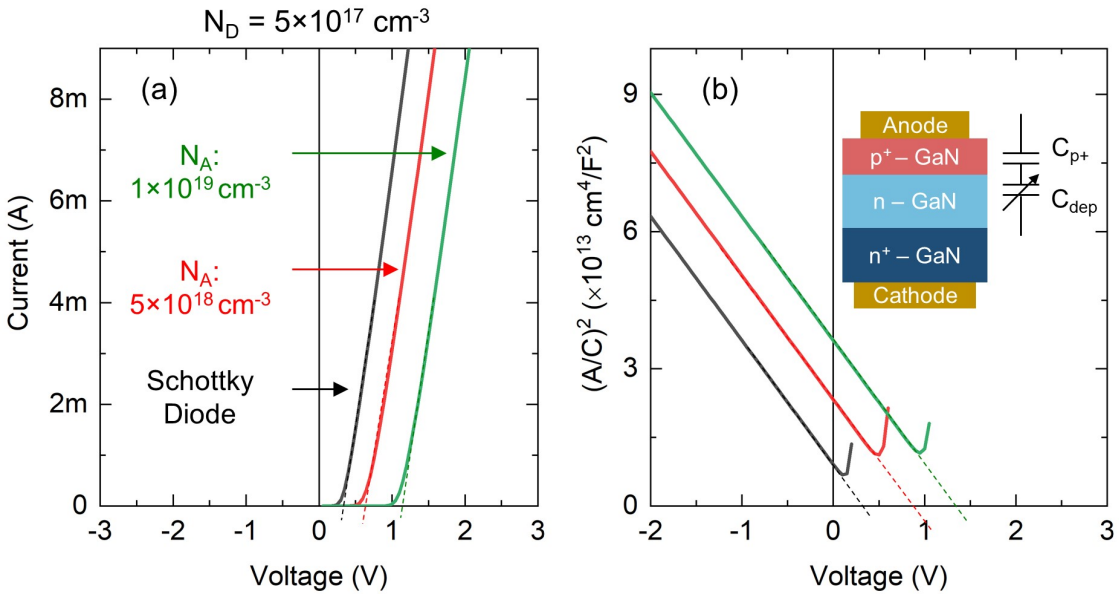

Figure 5.17: Simulated (a) current-voltage and (b) capacitance-voltage characteristics for Schottky and two different camel diodes. The n-type layer doping, in all diodes, is 5×10^{17} cm^{-3}. The p$^+$ layer thickness is 10 nm for both camel diodes. For two different camel diodes, the p$^+$ layer doping levels are 5×10^{18} cm^{-3} and 1×10^{19} cm^{-3}. The inset of figure (b) shows the schematic cross-section and equivalent circuit in C-V. C_{p+} and C_{dep} denote the capacitance of the p$^+$ layer and depletion layer in n-type GaN, respectively.

built-in potentials from the forward bias of $1/C^2$-V for diodes S, C1, and C2 are ∼0.4 V, ∼0.9 V, and ∼1.4 V, respectively, as shown in Fig. 5.17(b). It can be observed that, for the Schottky diode, the threshold voltage and built-in potential extracted from I-V and C-V matches. However, the built-in potential for both the camel diodes is higher than the threshold voltages. The reason for that is the additional constant capacitance (C_{p+}) due to the fully depleted p$^+$ layer in camel diodes. This capacitance is in series with the depletion layer capacitance (C_{dep}) of the n-type layer, which modulates with applied bias. Thus, the overall capacitance reduces, and $1/C^2$ shifts up. The equivalent capacitance circuit for the camel diode is shown in the inset of Fig. 5.17(b). In comparison, in the Schottky diode, only one capacitance modulates with the bias, which is why the extracted built-in potential from C-V matches with the threshold voltage from I-V.

5.3.2 Experimental Details and Results

Two N-polar GaN camel diode structures were grown on a *c*-plane sapphire substrate with a 4° offcut towards the *m*-plane using a vertical, cold-wall, radio frequency (RF) heated, low-pressure MOCVD system. Both camel diode structures consist, a 400 nm of n^+-type layer (O: $>10^{19}$ cm^{-3}), a 400 nm of n-type layer (O: $\sim 5\times10^{17}$ cm^{-3}). In the first camel diode (Diode D1), 10 nm of a p^+-type layer is grown with Mg doping of $\sim 5\times10^{18}$ cm^{-3}. Whereas in the second camel diode (Diode D2), 10 nm of a p^+-type layer is grown with Mg doping of $\sim 1\times10^{19}$ cm^{-3}. With these design parameters, the expected barrier heights for the diodes D1 and D2 are around ∼0.6 eV and ∼1 eV, respectively, as seen in Figs. 5.15 and 5.17(a). Immediately after the film growth, Mg activation anneal was performed *in-situ* at 900 °C under N_2 ambient and UV illumination for 20 min.

The diode fabrication process on camel diodes started with the Ni (250 nm) metal contact to the p^+-type layer using an e-beam evaporation system (base pressure: $\sim 10^{-9}$ Torr). It should be noted that the metal contacts were not alloyed. Then mesa etching was done using Cl_2-based inductively coupled plasma reactive ion etching (ICP-RIE) to access the bottom n-type layer. A 100 nm thick layer was etched using ICP-RIE followed by large area ohmic contact for the n-type GaN layer. The Ti/Al/Ni/Au (30/100/70/70 nm) metal stack was deposited using the same e-beam evaporation for the cathode contact. The schematic cross-section of the fabricated camel diodes is shown in Fig. 5.18(a).

The room temperature I-V characteristics for both camel diodes, in linear scale, are reported in Fig. 5.18(b). For comparison, the Schottky diode (Diode D3) without any p^+-type layer is also shown. The I-V for the Schottky diode shown in the graph is taken from the as-grown N-polar GaN Schottky diode reported in Chapter 3. From the linear I-V, it can be observed that the threshold voltages for the camel diode D1 and D2 are ∼0.5 V and ∼1 V, respectively. In comparison, the threshold voltage for the Schottky diode (D3) is ∼0.4 V. The

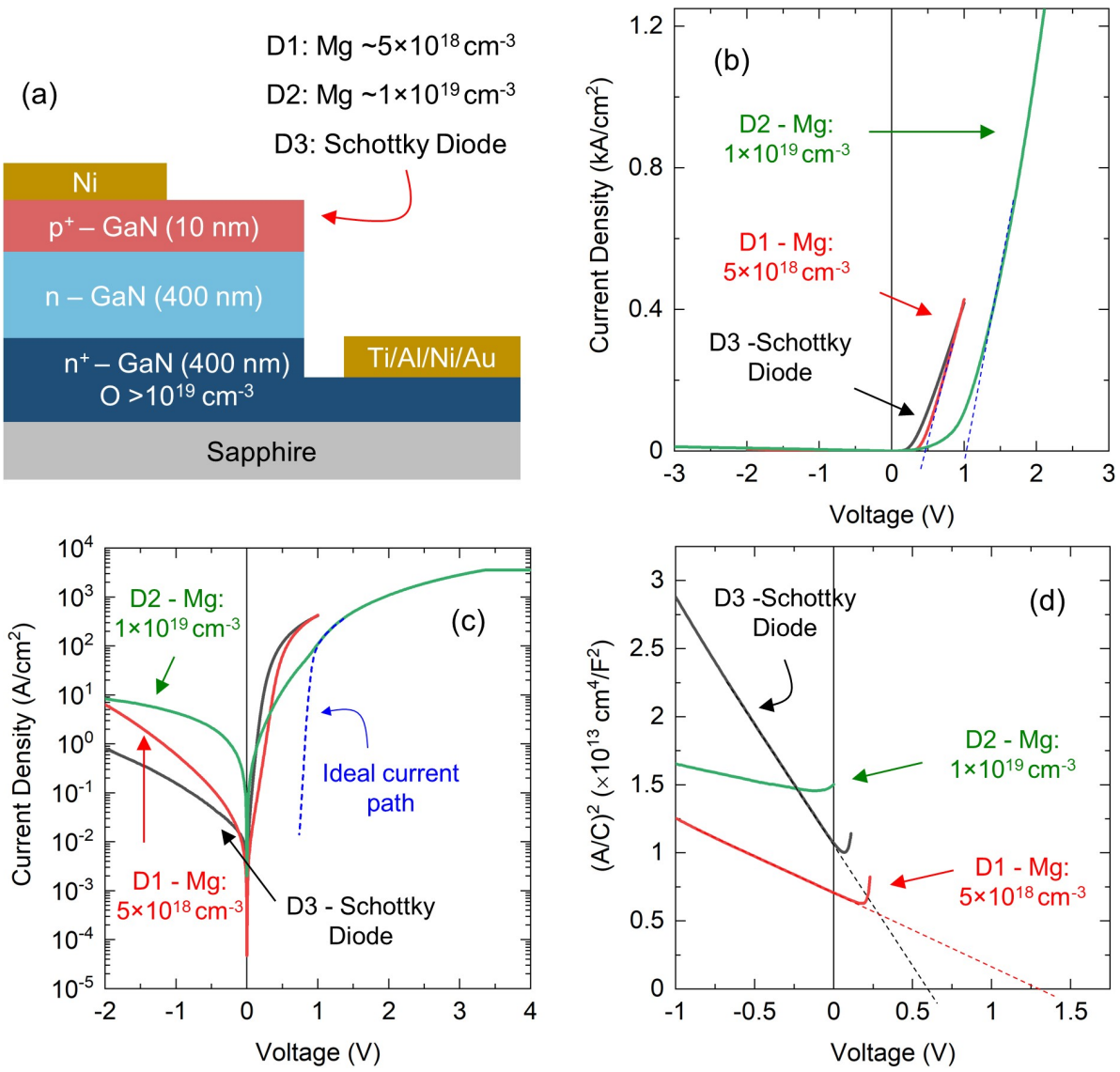

Figure 5.18: (a) The schematic cross-section of the fabricated camel diode. The doping levels for two different p^+ layers are $\sim 5\times10^{18}$ cm^{-3} and $\sim 1\times10^{19}$ cm^{-3}. Room temperature I-V characteristics of two camel diodes and a Schottky diode in (b) linear and (c) semilog scale. (d) $1/C^2$-V characteristics for two camel diodes and a Schottky diode measured at 1 MHz frequency.

comparison of room temperature I-V characteristics for both camel diodes, in semilog scale, are reported in Fig. 5.18(c). From the graph, it can be observed that the camel diodes have significant reverse bias leakage compared to the Schottky diode. For the camel diode D2, it is seen that, in forward bias, there are two current paths. At lower biases, below 1 V, the

current could be mainly due to the leakage in the diode. Whereas, at higher biases, above 1 V, the actual barrier current takes over. For reference, the ideal current path is highlighted with a blue dashed line. A detailed explanation is given in the discussion section.

Figure 5.18(d) compares the $1/C^2$-V characteristics for the camel diodes and the Schottky diode measured at 1 MHz frequency. As per the graph, the C-V built-in potential for the Schottky diode is around 0.6 V, which is higher than the I-V threshold voltage due to the presence of the native oxide interlayer, as mentioned in Chapter 3. In comparison, the C-V built-in potential for the camel diode D1 is higher than the Schottky diode, and it is around 1.25 V. The built-in potential for the camel diode D2 seems to be higher than the bandgap of GaN, which is not possible. This means the equivalent circuit (parallel R and C) used for C-V measurement of the camel diode D2 is not accurate. Instead, it might be possible that the resistance is in series to capacitance which is why the built-in potential is larger than the bandgap of GaN.

The net doping levels for all three diodes are calculated using the $1/C^2$-V characteristics. The method of doping extraction using the $1/C^2$-V characteristics is mentioned in Chapter 3. As the charge modulation happens only in the n-type layer of the camel diode, the extracted doping level would be for the n-type N-polar GaN in all diodes. The extracted net doping level for the diodes D1 and D2 are $\sim 2\times10^{18}$ cm^{-3} and $\sim 5\times10^{18}$ cm^{-3}, respectively. These extracted n-type GaN doping levels are much higher than the intended unintentional oxygen level ($\sim 5\times10^{17}$ cm^{-3}) in the material. Again, the extracted doping level for the camel diode D2 is not valid because the equivalent circuit used for C-V is inaccurate. The extracted doping level for the Schottky diode is $\sim 7\times10^{17}$ cm^{-3}.

5.3.3 Discussion

As per the linear I-V characteristics shown in Fig. 5.18(b), both N-polar GaN camel diodes have higher threshold voltages than the Schottky diode. The absence of electroluminescence (not shown) confirms that there are no free holes in the diode at those biases. This confirms the unipolar nature of the camel diode, and the increase of the barrier is purely due to the fully depleted p^+ layer. Thus, the camel diode, indeed, increases the barrier height of the diode while maintaining the unipolar nature of the device. Nonetheless, the actual I-V barrier heights need to be calculated for these diodes to observe the actual increment in the barrier height compared to the Schottky diodes, which is left for future work.

The main reason for adopting the camel diode structure from the GaN SJ device perspective is to reduce the reverse bias leakage by increasing the effective barrier height of the diode compared to the Schottky diode structure. However, from the semilog scale I-V characteristics, shown in Fig. 5.18(c), it is noticed that the reverse bias leakage in both camel diodes is even higher than the Schottky diode. This high reverse bias leakage could be due to the high hillock density present in both camel diodes. The surface AFM images of the camel diode D2 are shown in Fig. 5.19. In comparison, the camel diode D1 also has a slightly lower hillock density than the camel diode D2 (not shown). As these hillocks are made of different polarity facets such as semi-polar or non-polar, it is found, in the literature, that the incorporation of oxygen is even higher in certain semi-polar films than N-polar GaN films [55, 111, 235]. Thus, it could be possible that the higher leakage level in camel diodes could be due to the high hillock density. In addition, the oxygen level in the n-type layers of both camel diodes is higher than 10^{18} cm^{-3}, which could also be responsible for the higher leakage than the Schottky diode shown here. This high leakage current is also responsible for the deviation of the current from an ideal path at lower forward biases in the camel diode D2, as seen in Fig. 5.18(c). To achieve ideal camel diode performances, the leakage current needs to be

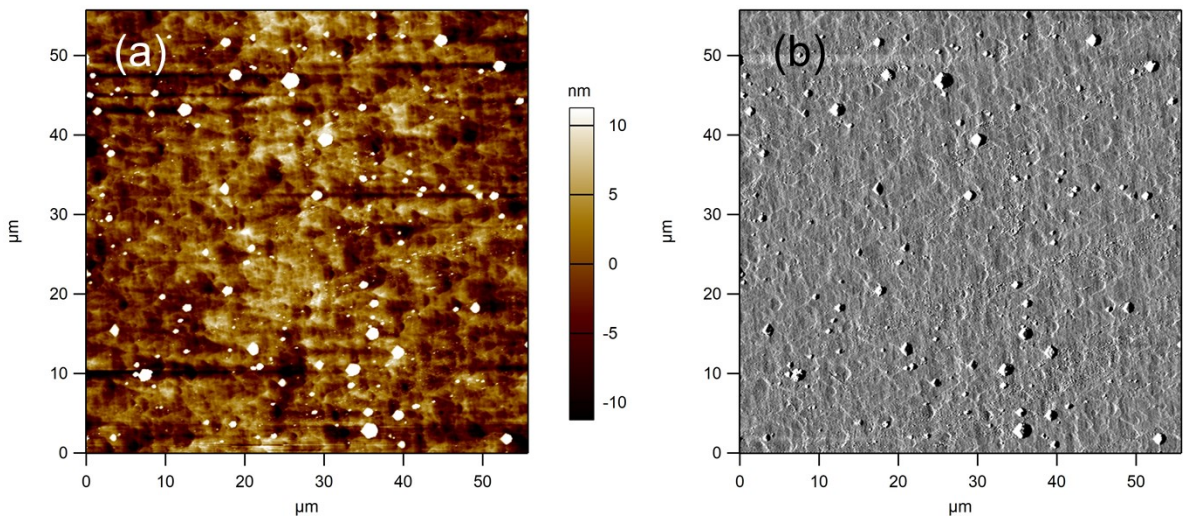

Figure 5.19: The surface AFM (a) height and (b) amplitude scan to highlight the high hillock density on the surface of camel diode D2.

reduced, which could be possible by growing a smooth and hillock-free surface, as well as by lowering the oxygen level to the order of mid to low 10^{17} cm^{-3}.

The extracted built-in potential (V_{bi} = 1.25 V), for the camel diode D1 from C-V measurements, is a significantly higher value than the measured threshold voltage (V_{th} = 0.5 V) from the linear I-V characteristics. This is due to the additional constant capacitance from the p^+ layer in series with the depletion layer capacitance of the n-type layer. To verify that, simulations are performed with the same doping levels and thicknesses of each layer for the camel diode D1. Figures 5.20(a) and 5.20(b) show the simulated I-V and C-V characteristics of the camel diode D1 using Silvaco ATLAS. It can be observed that the threshold voltage is around 0.6 V which is 0.1 V higher than the measured threshold voltage for the experimental device. The reason for that could be the non-uniform Mg distribution in the whole 10 nm of p^+ layer due to the delay in Mg incorporation during the growth, as shown in the SIMS graphs earlier (see Fig. 5.10). In addition, the background unintentional oxygen also compensates for p-type doping. All these parameters could lead to a lower effective charge

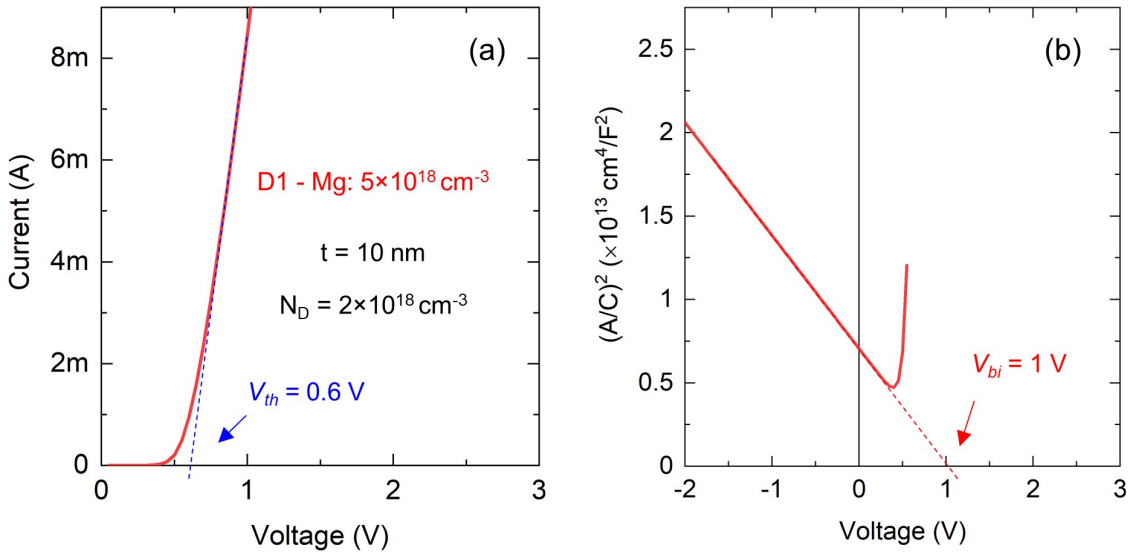

Figure 5.20: Simulated (a) I-V and (b) $1/C^2$-V characteristics for the camel diode D1.

in the p^+ layer, which would be responsible for the lower threshold voltage experimentally. As per simulated $1/C^2$-V characteristics, the built-in potential of the camel diode D1 is 1 V, which is 0.25 V lower than the measured value from the experimental result. The reason for the higher built-in potential in experimental could be due to the additional capacitance from a native oxide layer, or due to a thicker depleted region arising from a non-abrupt p-n junction due to Mg doping delay, as argued above. Due to that additional capacitance, the $1/C^2$-V is shifted upwards, resulting in a higher experimental C-V potential than the simulated one.

5.3.4 Summary

To summarize, first-order analytical design equations are provided to design the camel diodes using a thin p^+ layer and validated with TCAD simulations. The barrier height of the camel diode can be controlled using mainly three parameters: doping levels in the p^+ and n-type layer and the thickness of the p^+ layer. The thickness and doping of the p^+ layer should be

designed in such a way that it stays depleted at all bias, meaning there should not be any free holes available in the layer. To validate the theoretical analysis, two different N-polar GaN camel diodes are fabricated by adding 10 nm of p^+ layer with doping levels of 5×10^{18} cm^{-3} and 1×10^{19} cm^{-3} on top of the n-type layer. It is observed that the threshold voltages are increased for both the camel diodes compared to the Schottky diode. Also, the increment in the p^+ layer doping increased the threshold voltage, suggesting that the barrier height can be controlled by tuning the doping of the p^+ layer. A similar effect should be observed experimentally by varying the thickness of the p^+ layer, which is left for future work. It is observed that the reverse bias leakage current in these camel diodes is higher than the Schottky diode reverse leakage. The probable cause of the higher leakage is attributed to the high hillock density on the surface of these camel diodes and the high oxygen level in the n-type layer. Thus, by obtaining smooth surface morphology and lower oxygen levels, the camel diode should have a lower leakage current and better performance than the Schottky diode.

5.4 Conclusion

To conclude, this chapter demonstrated that the p-type conductivity is obtained in the MOCVD-grown N-polar GaN film. The N-polar GaN p-n and camel diodes are designed and fabricated. Extensive electrical characteristics are reported and analyzed in-depth for p-n and camel diodes to optimize the material properties for future growth runs. The primary motivation for realizing the N-polar GaN p-n diodes was to study the material properties such as Mg and oxygen levels in the device structure, obtained via SIMS and CV analysis. From the standpoint of realizing the GaN SJ device, the camel diode is preferred over the p-n diode as it allows unipolar operation. The experimental results of the camel diode presented in this work showed higher threshold voltage and unipolar nature of the diode. Adjustment

of doping in the p^+ layer also tuned the threshold voltage of the camel diode, which enables the barrier height to be adjusted in camel diodes. However, it is noticed that the leakage current in these camel diodes is higher due to the high hillock density on the surface and high unintentional oxygen level. The leakage current issue could be mitigated by obtaining smooth surface morphologies and reducing the oxygen level to mid to low 10^{17} cm^{-3}, which is anyhow necessary to realize high-performance GaN SJ devices. The results presented in this chapter motivates to employ camel diode design structure for N-polar GaN domains to increase the barrier height of the SJ diode. The detailed design, fabrication, and characterization of GaN SJ devices using the LPJ approach are presented in the next chapter.

Chapter 6

First Demonstration of Charge-balanced GaN Lateral Polar Junctions

6.1 Motivation

As mentioned in the introduction chapter, the main objective of this thesis is to demonstrate selective area doping control for the realization of GaN-based vertical superjunction using a novel lateral polar junction (LPJ) approach. In this LPJ approach, both Ga- and N-polar GaN domains grow simultaneously with asymmetric dopant incorporation. Thus, this approach bypasses the challenges of ion implantation and etching/regrowth in GaN technology. In order to obtain GaN vertical SJs using the LPJ approach, several technological challenges need to be addressed. One such challenge is to achieve proper charge balance ($N_D \cdot W_N = N_A \cdot W_P$) between Ga- and N-polar domains while maintaining equal heights of these domains during the growth. As described in Chapter 2, the charge balance in the SJ structure is of utmost necessity to obtain a 2D electric field profile across the drift region, which maximizes the breakdown capability of the designed device. In case of charge imbalance, the breakdown performance of the device deteriorates significantly depending upon the level of charge imbalance. In the envisioned GaN SJ structure using the LPJ approach, the N-polar GaN domain would serve as an n-type column, whereas the Ga-polar domain would serve as a p-type column. The reason for choosing the N-polar GaN domain as an n-type column is the preferential incorporation of shallow donor oxygen during the growth, which does not incorporate into

Ga-polar GaN. In contrast, incorporation of Mg happens at a similar level in both Ga- and N-polar GaN domains. Thus, during the SJ growth, the Mg concentration level needs to be lower than the oxygen concentration in order to keep the N-polar domain as n-type while making the Ga-polar domain p-type column. For example, to obtain charge balance between Ga- and N-polar GaN domains with equal column widths ($W_N = W_P$), the introduction of Mg dopants during the growth should be half of the oxygen level in the N-polar domain so that the net doping in the N-polar domain ($O^+ - Mg^-$) remains equal to Ga-polar domain (Mg^-). In addition to the requirement of charge balance between the polar domains, achieving equal heights of these polar domains is necessary to obtain ideal performance of the SJ device. If the height of both columns is not equal, that would again create a charge imbalance between the columns, which would deteriorate the SJ performance. Early III-Nitride LPJ growth studies did not achieve adjacent pillars with equal heights [253, 254]. Later, Hoffmann *et al.* performed a growth study of varying V/III ratio using ammonia (NH_3) flow while keeping constant triethylgallium (TEG) flow on patterned 10 μm period AlN buffer layer [255] to achieve equal domain heights in lateral polar junctions. Their study found that one polarity may be dominant over the other based on the V/III ratio during the growth. It was observed that there is no thickness difference, meaning equal heights, between Ga- and N-polar domains in LPJ at the V/III ratio of 225 [255]. Even though Hoffmann *et al.* devised equal height LPJ growth conditions in GaN, the doping levels were not controlled, especially in N-polar GaN domains, as the motive of their study was for a different application other than SJ. This means the doping levels in the N-polar GaN might be higher than 10^{19} cm^{-3}, which is too high from the SJ device design perspective.

In this chapter, the first major milestone towards achieving the GaN-based vertical SJ devices is demonstrated by obtaining the charge balance between Ga-polar and N-polar domains while maintaining the equal heights of these domains. This chapter presents the

material and electrical characterization of the grown lateral polar junction. This is the first demonstration of achieving equal doping levels selectively in GaN technology.

6.2 LPJ Growth and Material Characterization

To obtain equal domain heights in LPJs with controlled doping levels for SJs, recently, Szymanski *et al.* performed a growth study by not only varying the V/III ratio but also the growth temperature and diluent gas species, in essence by varying the supersaturation [256]. In their work, the process flow to obtain GaN LPJs on the patterned AlN buffer was similar to the method shown in Fig. 1.15. These studies found that at high V/III ratios, meaning at higher gallium supersaturations, N-polar GaN growth is dominant. Whereas at low V/III ratios, low gallium supersaturations, Ga-polar GaN growth is dominant. Using these findings, Szymanski *et al.* developed a supersaturation modulated growth (SMG) scheme to realize equal height GaN lateral polar junction by implementing chemical potential control to lower unintentional oxygen incorporation [256]. In this SMG technique, supersaturation was periodically modulated to grow the Ga-polar domain at low supersaturation and N-polar GaN at high supersaturation. The supersaturation was periodically modulated every 15-sec corresponding to 10 nm of film growth by changing the flow of NH_3 between 0.3 and 6 slm.

Now that the growth technique is developed to obtain low doping levels with equal height lateral polar domains, a device structure is designed to investigate if equal doping levels in Ga- and N-polar can be obtained. A schematic of the envisioned quasi-vertical GaN LPJ structure is shown in Fig. 6.1. In order to grow that structure, a 20 nm thin AlN buffer layer was first grown on a *c*-sapphire substrate, with a miscut of 4° toward *m*-plane, in a vertical, cold-wall, rf-heated, low-pressure MOCVD reactor. As shown in Fig. 6.1, the alternating polar domains can be achieved by patterning this AlN buffer layer. To facilitate that, photolithography

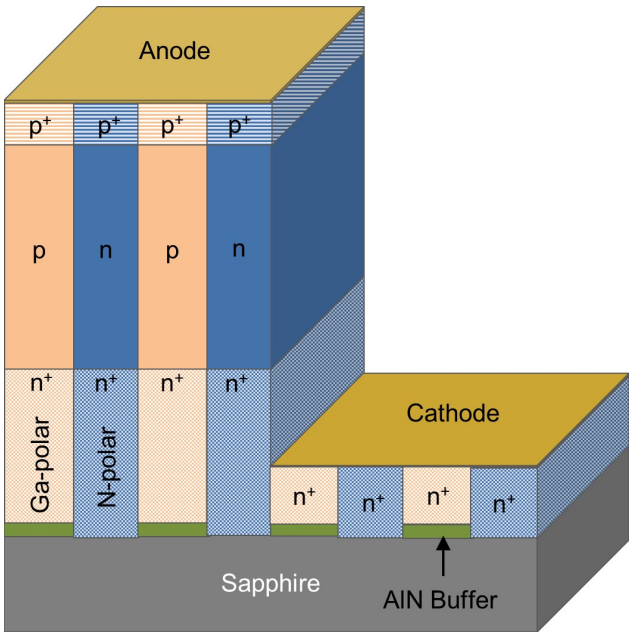

Figure 6.1: The schematic of GaN-based SJ device structure using lateral polar junction approach.

using a stepper tool followed by reactive ion etching (RIE) was performed to pattern the buffer layer to obtain stripes of AlN and bare sapphire with a period of 2 μm (W_N+W_P; $W_N = W_P = 1$ μm). The SEM image after the lithography patterning and AFM image after patterning the AlN buffer layer using RIE are shown in Figs. 6.2(a) and 6.2(b), respectively. These graphs confirm that 2 μm periods are obtained.

Later, GaN LPJ was grown on this patterned AlN layer using the SMG technique mentioned above to achieve equal height domains. First, 4.5 μm of the n^+-type layer was grown for the cathode contact with silicon doping of 2×10^{18} cm^{-3}. The reason for introducing the Si doping for this layer is to obtain n^+-type doping in both Ga- and N-polar domains. The thickness of this n^+ layer was kept higher to mitigate the impact of etching thickness variations on the cathode contact's behavior (see Fig. 6.1). After the n^+ layer growth, a controlled amount of Mg dopants were introduced into the reactor to dope the Ga-polar domains p-type while maintaining n-type GaN in the N-polar domain for charge balance

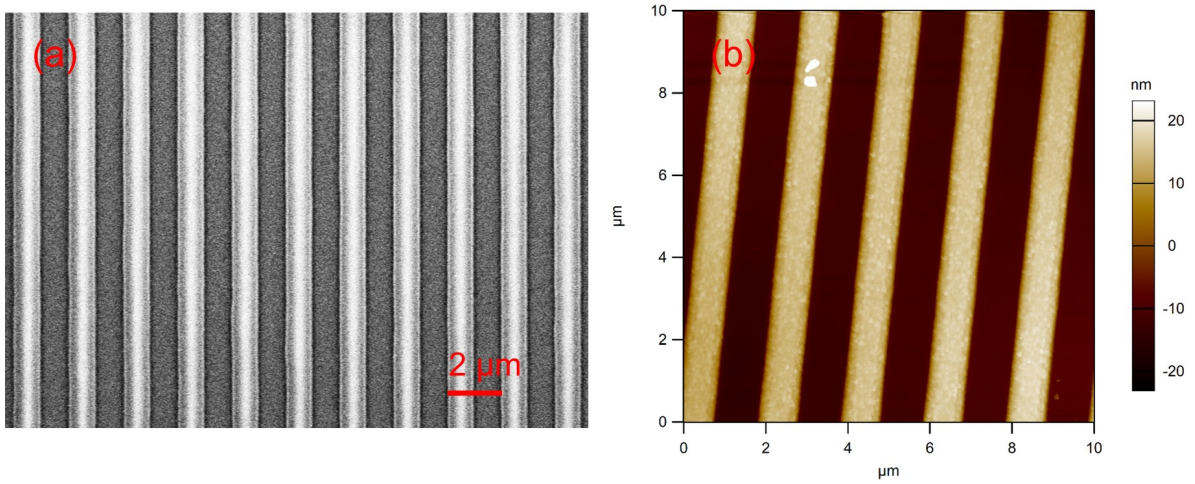

Figure 6.2: (a) Top view SEM image of patterned 2 μm stripes using stepper-based photolithography. The bright areas are the photoresist, and the darker areas are the AlN buffer layer. (b) AFM height scan after the reactive ion etching to pattern AlN buffer layer. The bright areas are the AlN buffer layer, and the darker areas are the bare sapphire substrate.

purposes. The introduced Mg concentration was $\sim 1\times10^{18}$ cm^{-3}, with the thickness of this charge-balanced drift layer around 0.5 μm. The structure was then terminated with 20 nm of Mg-doped GaN with a Mg concentration of $\sim 10^{19}$ cm^{-3} to ensure both Ga- and N-polar domains are p$^+$-type. The reason for adding this p$^+$ layer on top is to form a camel diode for the N-polar GaN domain. At the same time, the Ga-polar domain would not have any impact of this p$^+$ layer as it would only create a p$^+$/p junction. Immediately after the growth, an *in-situ* activation anneal at 900 °C under N_2 ambient for 20 min was performed to activate Mg in the structure. It should be emphasized that the primary objective of adapting this growth structure here is to demonstrate charge balance in both Ga- and N-polar GaN domains. Therefore, the specific doping levels and the thickness of the drift region employed are relaxed compared to those that would be used to obtain a GaN SJ device with high breakdown voltage. A successful demonstration of charge balance would lead to realizing a high-performance GaN SJ device structure. The schematic cross-section of the grown lateral polar junction with thickness and doping of each layer is shown in Fig. 6.3(a). A tilted-view SEM image

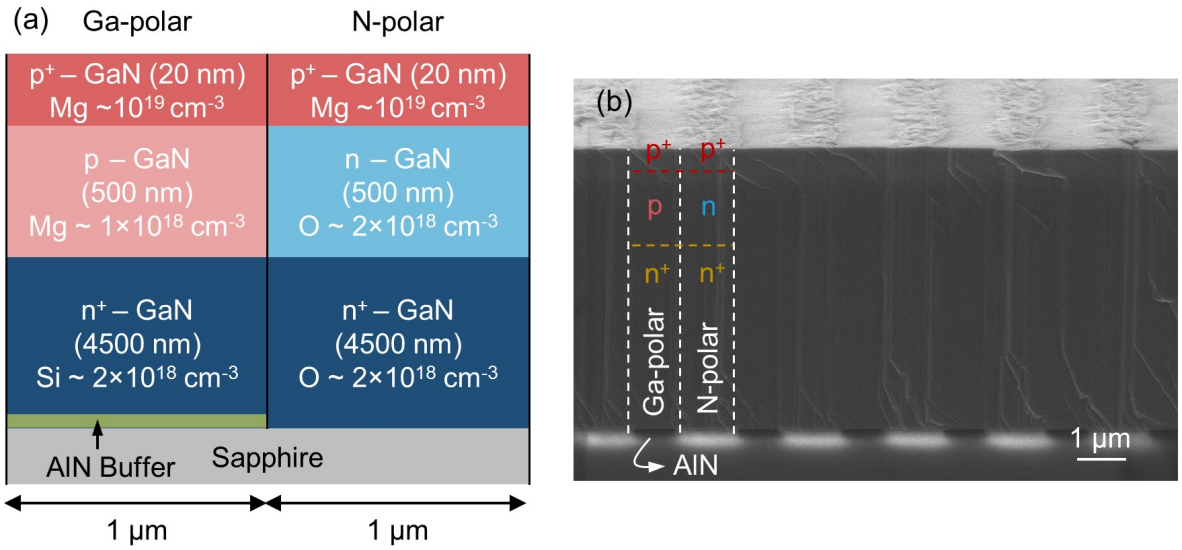

Figure 6.3: (a) Schematic cross-section with intended thickness and doping levels of each layer. (b) A tilted-view SEM image of the grown GaN lateral polar junction demonstrating the equal height of both domains.

demonstrating the equal height Ga- and N-polar GaN domains is shown in Fig. 6.3(b).

To confirm whether the grown LPJ structure has alternating Ga- and N-polar GaN domains, the sample was submerged into 70 °C 1 M potassium hydroxide (KOH) for 2 hours. KOH etches N-polar GaN 20 times faster than Ga-polar GaN [165]. Thus, this wet chemical etching of grown LPJ structure using KOH should etch N-polar GaN domains if they are present. A tilted-view SEM image after 2 hours of KOH etching is shown in Fig. 6.4. The graph suggests that indeed the grown LPJ structure has alternating Ga- and N-polar GaN domains.

Following confirmation that the grown LPJ structure consists of Ga- and N-polar GaN side-by-side, it is crucial to investigate the interface between these domains. The interface between these opposite polarity domains is noted as the Inversion Domain Boundary (IDB). Ideally, a single atomic layer IDB is desired as the wider IDB might have a mixture of Ga- and N-polar material [257, 258]. The boundary between the polar domains in LPJ

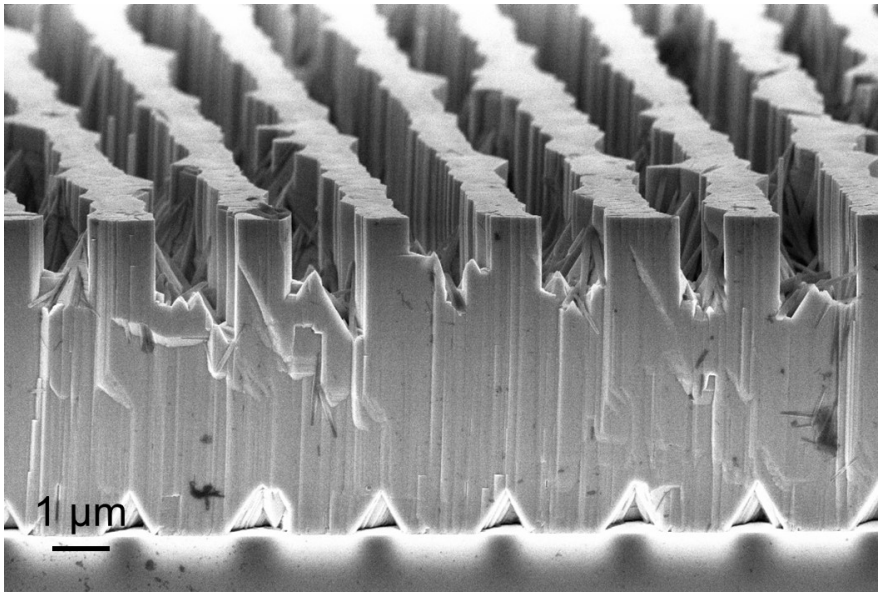

Figure 6.4: A tilted-view SEM image of GaN LPJ after 2 hours of wet etching into 70 °C 1 M KOH. As a result of the etch selectivity, N-polar GaN domains etches away in KOH, confirming the LPJ structure consists of Ga- and N-polar GaN domains.

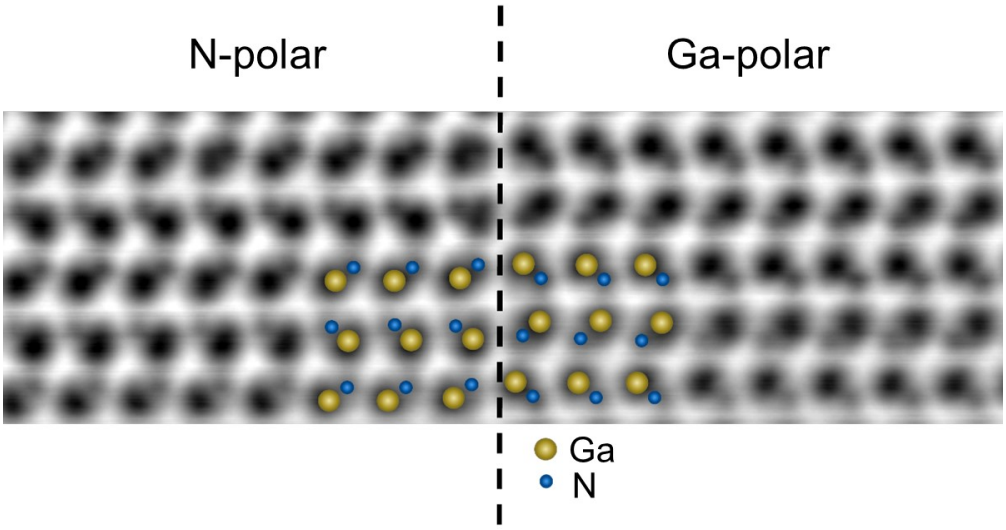

Figure 6.5: Atomic resolution iDPC demonstrating that both N-polar and Ga-polar domains are separated by a single atomic layer IDB. Figure from [256].

was characterized using integrated differential phase contrast (iDPC) imaging in STEM. Figure 6.5 shows the abrupt transition across the length of a single atomic plane between Ga- and N-polar domains. The graph also confirms that the grown LPJ structure indeed has alternating Ga- and N-polar domains.

Secondary ion mass spectroscopy (SIMS) is performed to investigate the doping levels in the grown LPJ structure. As shown in Fig. 6.3, the Ga-polar domain consists of $p^+/p/n^+$ layers, and the N-polar domain consists of $p^+/n/n^+$ layers. In the SIMS analysis, magnesium, silicon, and oxygen are tracked as a function of depth in LPJ. Figure 6.6 shows the SIMS results of the grown LPJ structure. The doping level of the Si in the n^+ layer is confirmed to be $\sim 2\times10^{18}$ cm^{-3}. The doping level of Mg is $\sim 1\times10^{18}$ cm^{-3} in the drift region of the LPJ. It should be noted that the Mg concentration for the top p^+ layer might not be observed

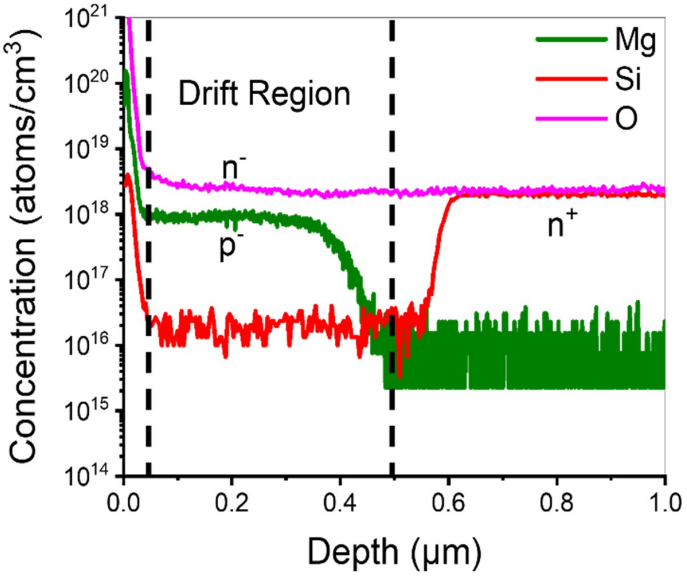

Figure 6.6: A SIMS analysis of the grown LPJ structure. The drift region of this LPJ has Mg $\sim 10^{18}$ cm^{-3}, which should be in both domains, and O $\sim 2\times10^{18}$ cm^{-3}, which should be in the N-polar domain. This demonstrates a charge balance between Ga-polar (Mg) and N-polar (O-Mg) GaN domains. Figure from [256].

here in the SIMS as the layer thickness is only 20 nm. The estimated doping level of oxygen in the LPJ is $\sim 2\times10^{18}$ cm^{-3}. The sampling area of the SIMS analysis was much large than the 2 μm period of the LPJ. Thus, the SIMS data includes many Ga- and N-polar domains, and the data in Fig. 6.6 is from both types of domains simultaneously. Therefore, to estimate the oxygen concentration in the N-polar domains, the measured concentration was doubled when presented in Fig. 6.6, as the counts arise only from half the sampling volume (Ga-polar domains have negligible oxygen content). In contrast, the Mg impurities should be incorporated in both Ga- and N-polar domains as Mg was introduced uniformly during the growth, and both domains incorporate Mg at the same level. These results confirm that the drift region of the Ga-polar domain is p-type with a concentration of $\sim 1\times10^{18}$ cm^{-3} assuming it does not incorporate oxygen during the growth. And the drift region of the N-polar domain should be n-type with a concentration of $\sim 1\times10^{18}$ cm^{-3} (O-Mg). Thus, it can be observed that both domains in the grown LPJ are charge-balanced, meaning both domains would have equal and opposite ionized impurity concentrations under total depletion. It is worth noting that the total impurity concentration in the N-polar domain would be donors plus acceptors (O+Mg). As a result, the carriers' mobility would be slightly lower for N-polar GaN in this LPJ approach than standard SJ, where the n-type column would contain only donors. The electron mobility in the case of 1×10^{18} cm^{-3} impurities would be $\sim$670 cm^2/Vs [10]. In comparison, the electron mobility for 3×10^{18} cm^{-3} impurities would be $\sim$470 cm^2/Vs [10]. This reduction in mobility would increase the on-resistance by $\sim$1.4 times for these impurity concentrations in LPJ based SJ compared to standard SJ.

In the SIMS analysis, it is assumed that the Ga-polar domain does not incorporate oxygen impurities. As the sampling size in the SIMS analysis was much larger than 1 μm wide domains, it was difficult to analyze single domains under SIMS. Thus, to prove the hypothesis that Ga-polar does not incorporate unintentional oxygen, the domain needs to

be analyzed with a probe size smaller than 1 μm. To investigate this hypothesis, the LPJ structure was analyzed using atom probe tomography (APT), and the results are shown in Figs. 6.7(a) to 6.7(d). APT specimens from each domain were prepared with a lift-out process and sharpened using focused ion beam (FIB) milling [259]. To enable tracking of the position of the IDB during tip sharpening, a nominally 200 nm wide Pt fiducial layer (Figs. 6.7(a) and 6.7(b)) was placed at the IDB prior to the larger-area Pt protective layer deposition. The details on the APT processing are reported in [256]. Oxygen concentrations were calculated from ions with mass-to-charge (m/z) ratios of 16 for both Ga- and N-polar GaN domains individually, as shown in Figs. 6.7(c) and 6.7(d). These graphs show that the Ga-polar domain does not have any oxygen and is only present in the N-polar GaN. Thus, it

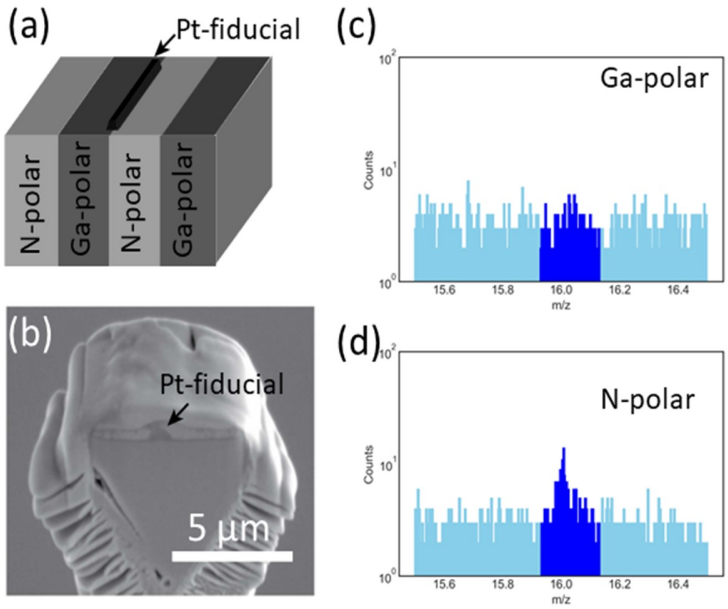

Figure 6.7: (a) A schematic of the APT sample containing GaN LPJ and (b) an SEM image of the fiducial Pt layer to identify the position of inversion domain boundary during the tip shaping process. Mass spectra of (c) Ga-polar and (d) N-polar GaN domains near oxygen peak at mass to charge ratio (m/z) 16. Figure from [256].

is clear that there is a charge balance between those domains in the drift region of LPJs. To this end, the diodes are fabricated on this grown LPJ structure to characterize it electrically via current-voltage (I-V) and capacitance-voltage (C-V) characteristics.

6.3 Device Fabrication

The diode fabrication process started with the anode metal contact deposition for the top p^+ layer. For that, a Ni/Au (20/40 nm) metal stack was deposited using an e-beam evaporation system (base pressure: $\sim 10^{-9}$ Torr). For the anode metal contact deposition, a thin metal shadow mask was used to define various circular contacts ranging from diameter 50 μm to 300 μm. Shadow masking was employed to avoid exposure to chemicals that might alter the surface as standard device fabrication chemicals roughen the N-polar GaN surface, as shown in Chapter 3. Following the anode metal deposition, 1.5 μm thick mesa etching was done using Cl_2-based inductively coupled plasma reactive ion etching (ICP-RIE) to access the bottom n^+ layer. After the mesa etching, Ti/Al/Ni/Au (30/100/70/70 nm) metal stack was deposited using the same e-beam evaporation system for the cathode contact on the n^+ layer.

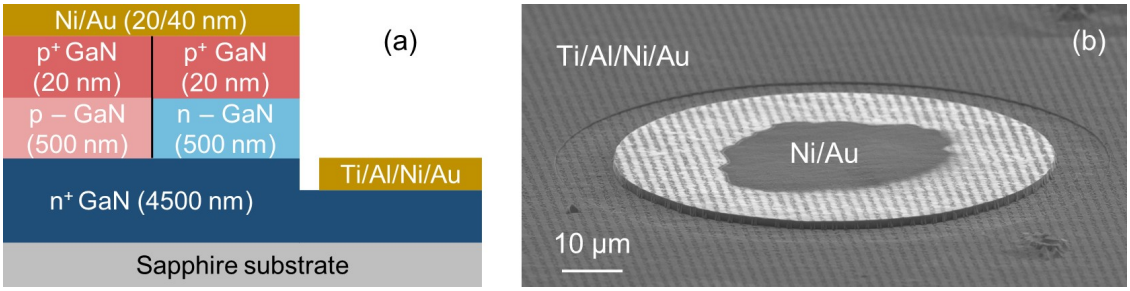

Figure 6.8: A schematic cross-section and (b) a tilted-side SEM image of the fabricated diode on the LPJ structure.

It should be noted that the anode and cathode contacts are not alloyed here. The anode contact should form ohmic contact to the Ga-polar domain. Whereas the anode contact should form rectifying contact for the N-polar GaN domain as the thin p^+ layer on the top should form the camel diode. The schematic cross-section and a tilted-side SEM image of the fabricated diode are shown in Figs. 6.8(a) and 6.8(b), respectively.

6.4 Electrical Results and Discussion

As shown in Fig. 6.8(a), the Ga-polar domain has a p-n^+ junction, and N-polar GaN has a p^+-n junction. It is important to note that the 20 nm thick p^+ layer on the N-polar domain side should be totally depleted due to the opposite charge from the bottom n-type layer: thus, forming a camel junction for the N-polar domain. The formation of the camel junction on the N-polar domain was intentional as it would increase the barrier height, which helps to reduce the leakage current compared to pure Schottky contact. In contrast, for the Ga-polar domain, this top p^+ layer would only form the p^+/p junction, and the barrier would be at the bottom p-n^+ layer. Now, if the applied bias voltage is lower than the bandgap of GaN, the current would flow only through the N-polar domain depending upon the barrier height of the camel junction. The current flow, in this case, would be due to majority carriers, which is consistent with the desired unipolar nature of the device. When the applied bias is higher than the bandgap of GaN, the p-n^+ junction in Ga-polar, as well as the p-n junction between two lateral domains, would be turned on, and the current flow would be due to both carriers meaning the bipolar nature of the device. Therefore, the forward bias operating point should be lower than 3.4 V, which is the bandgap of GaN, to maintain the unipolar nature of the device from an SJ application standpoint.

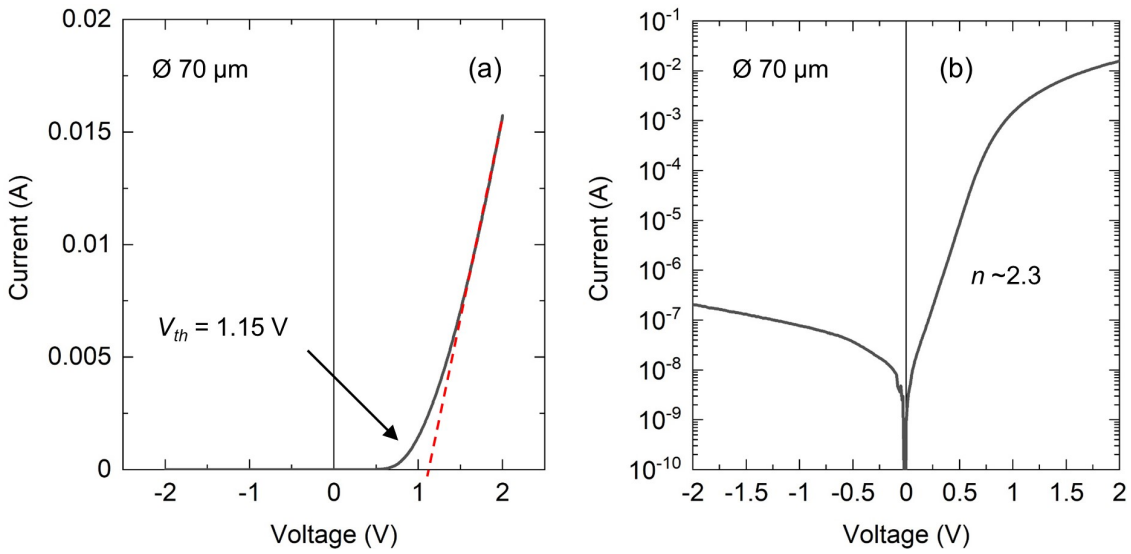

Figure 6.9: Room temperature I-V characteristics of the grown LPJ structure in (a) linear and (b) semilog scale. The measured diode was 70 μm in diameter.

Figures 6.9(a) and 6.9(b) show measured room temperature I-V characteristics for the grown LPJ structure in linear and semilog scale, respectively. The diameter of the analyzed diode was 70 μm. In these I-V characteristics, the current was measured up to the maximum forward-bias voltage of 2 V to ensure the unipolar operation of the diode. The threshold voltage (V_{th}) of the diode, extracted from the linear I-V, is around 1.15 V. It can be observed that the V_{th} of the diode is higher than the observed V_{th} for the N-polar GaN Schottky diode ($\sim$0.4 V) reported in Chapters 3 and 4. Here, the measured V_{th} for the LPJ is closer to the reported value for the camel diode D2 (10 nm thick p^+ layer with 1×10^{19} cm^{-3} doping level) [see Fig. 5.17(b)] in Chapter 5. Thus, it is clear that the LPJ structure grown here has a camel diode junction in the N-polar GaN domain. The ideality factor (n) for the LPJ diode, extracted from the semilog I-V between 0.3 V to 0.6 V, is $\sim$2.3. The reason for the higher ideality factor could be the slightly thicker and fully depleted p^+ layer. As per the graph, the current on/off ratio at $\pm$2 V is around 10^5, which is higher than the on/off ratio measured for the bulk N-polar GaN camel diode D2 in chapter 5 [see Fig. 5.17(c)]. This could be due

to the slightly thicker p^+ layer (20 nm) as well as lower background oxygen level achieved in the LPJ compared to the diode D2. Nonetheless, the expected V_{th} for 20 nm p^+ layer with Mg doping $\sim 10^{19}$ cm^{-3} should be more than 2 V if the doping level is constant throughout the p^+ layer. As we know from chapter 5, the Mg dopants have a delay in their incorporation during the growth; thus, the doping level might not be constant and abrupt. In addition, there might be variations in the p^+ layer during the film growth such as thickness and doping of p^+ layer, which would affect the V_{th}. Thus, Silvaco TCAD simulations are performed to investigate the effective Mg doping level and thickness of the p^+ layer corresponding to the experimental results.

Figure 6.10(a) shows the cross-section structure of the simulated device with the thickness and doping levels of each layer. Three different cases are considered for the simulations by varying thickness and the doping level of the top p^+ layer: 15 nm with 5×10^{18} cm^{-3}, 20 nm with 5×10^{18} cm^{-3}, and 20 nm with 1×10^{19} cm^{-3}. Figure 6.10(b) shows the I-V characteristic comparison of these three cases in a linear scale. As per the graph, the 15 nm thick p^+ layer with a 5×10^{18} cm^{-3} doping level matches the experimental results. Thus, it might be possible that in the experimental device, the effective doping is around 5×10^{18} cm^{-3} with a thickness of 15 nm. As mentioned above, the lower effective doping could be the compensating background unintentional oxygen and the turn-on delay of Mg incorporation. Figure 6.10(c) shows the I-V characteristics of the same devices in a semilog scale. It is noted that the ideality factor of the device with a 15 nm thick p^+ layer with N_A-$N_D = 5\times10^{18}$ cm^{-3} is $\sim$1.6. In comparison, the ideality factor of the experimental device is $\sim$2.3, as reported above. The higher ideality factor observed experimentally might be due to the additional leakage current at lower biases. Figure 6.10(d) shows the linear I-V characteristics simulated till 4 V in the forward bias. As per the graph, the I-V has another turn-on at 3.4 V. This is due to the turn-on of the p-n^+ junction in the Ga-polar domain and the turn-on of the p-n junction

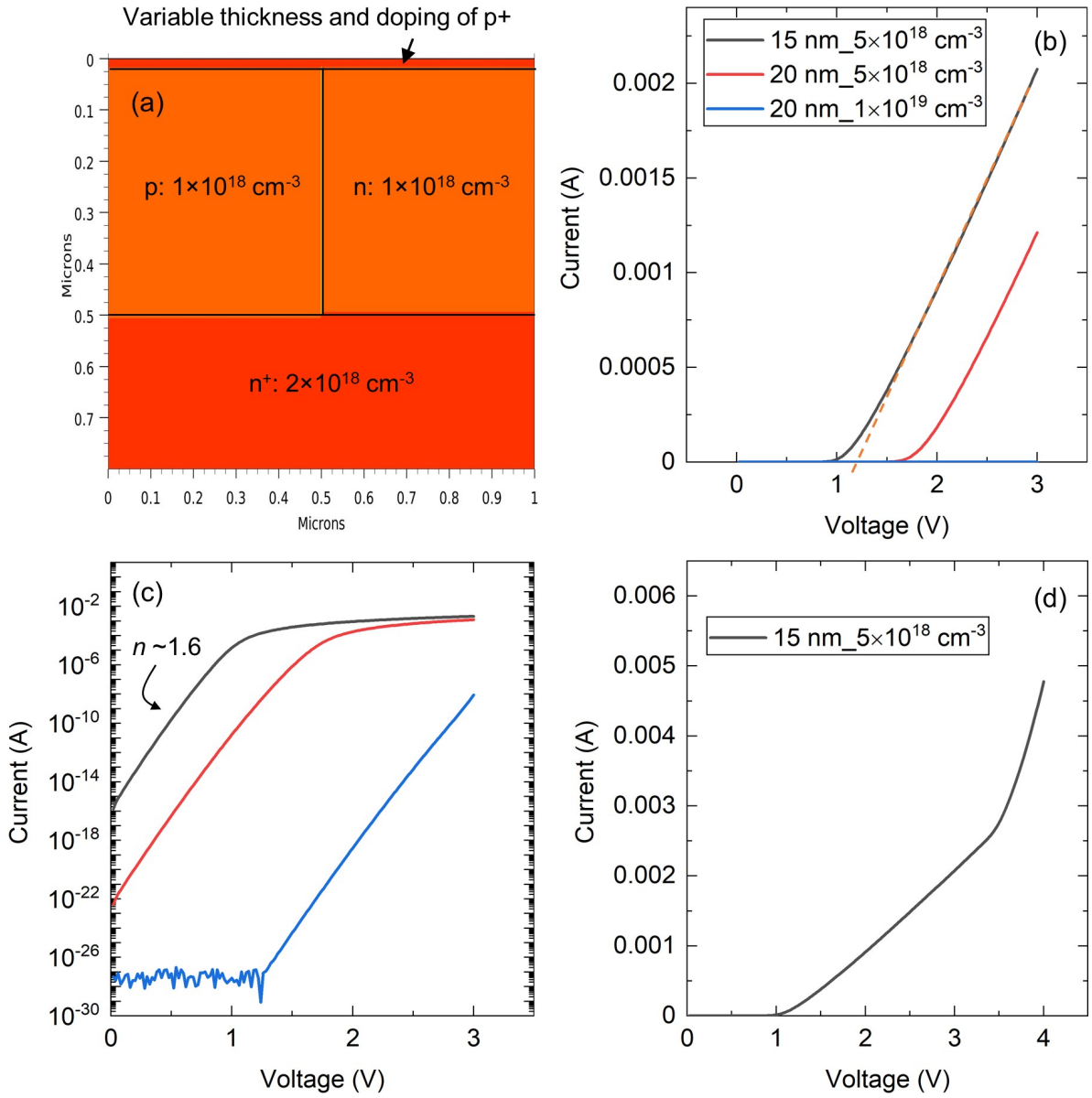

Figure 6.10: (a) Cross-section of the simulated LPJ structure using Silvaco. The I-V characteristics comparison of three different top p^+ layer designs (mentioned in the legend of the figure) in (b) linear and (c) semilog scale. (d) The I-V characteristics of 15 nm thick p^+ layer with doping level 5×10^{18} cm^{-3} operated up to 4 V in forward bias.

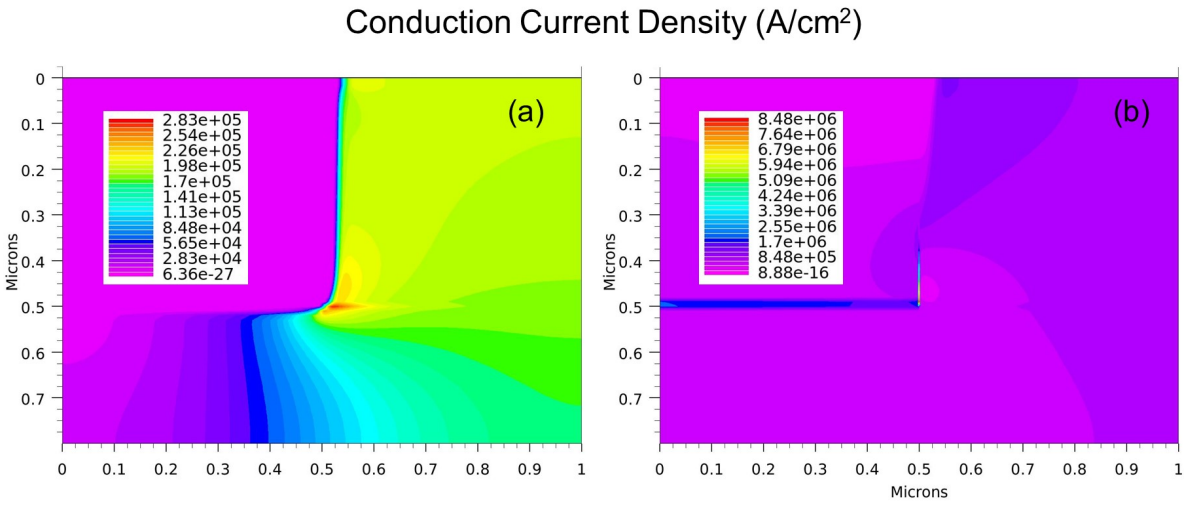

Figure 6.11: 2D contour of simulated conduction current density across the LPJ for the case of top 15 nm thick p^+ layer with doping level 5×10^{18} cm^{-3} diode at a forward bias of (a) 2 V and (b) 4 V.

between the lateral domains. To confirm that, the 2D contour of conduction current density across the structure, for the case of 15 nm thick p^+ layer with doping level 5×10^{18} cm^{-3}, at forward bias 2 V and 4 V are shown in Figs. 6.11(a) and 6.11(b), respectively. As per the graphs, it is evident that at 2 V, the current flows only through the N-polar domain, whereas at 4 V, the current flows across both the domains.

C-V measurements are performed to estimate the doping level in the LPJ structure. Figure 6.12(a) shows the $1/C^2$-V characteristics of the fabricated LPJ diode measured at 100 kHz frequency. As per the graph, the built-in potential measured using $1/C^2$-V is ~3.4 V, which is the bandgap of GaN. This could be due to the dominant capacitance from the p-n^+ junction in the Ga-polar domain or the p-n junction at the lateral polar domain. In any case, it is evident that the Ga-polar domain has a p-type layer, which again proves that there are no oxygen impurities in it. To estimate the doping level, the correct area needs to be divided by the measured capacitance. If the wrong area is assumed in this calculation, it could lead to an incorrect estimation of the doping level. For reference, the equation for the net doping level calculation is shown as follows:

$$N = -\frac{2}{q\varepsilon_S} \frac{1}{d\left(\frac{A^2}{C^2}\right)/dV} \tag{6.1}$$

where, N is the net doping level, q is the elementary charge, ε_S is the dielectric permittivity, A is the cross-section area of the diode, C is the capacitance, and V is the voltage. In the case of SJ diode, there are three capacitances in parallel, which are from a p^+-n junction in N-polar domain (C_N), p-n^+ junction in Ga-polar domain (C_{Ga}), and a lateral p-n junction between two domains($C_{Ga\text{-}N}$). To demonstrate that, the exact fabricated structure is simulated. Figure 6.12(b) shows the depletion regions inside the structure at reverse bias -5 V. As per the graph, it can be observed that there are three depletion regions at the junctions mentioned above. Now, as these three capacitances are in parallel, the effective area of the diode would be different than the actual cross-section area of the diode. In addition, the value of these capacitances would not be the same. Thus, the area of the diode is estimated based on the following analysis. First, the total capacitance (C_{LPJ}) of the diode can be written as:

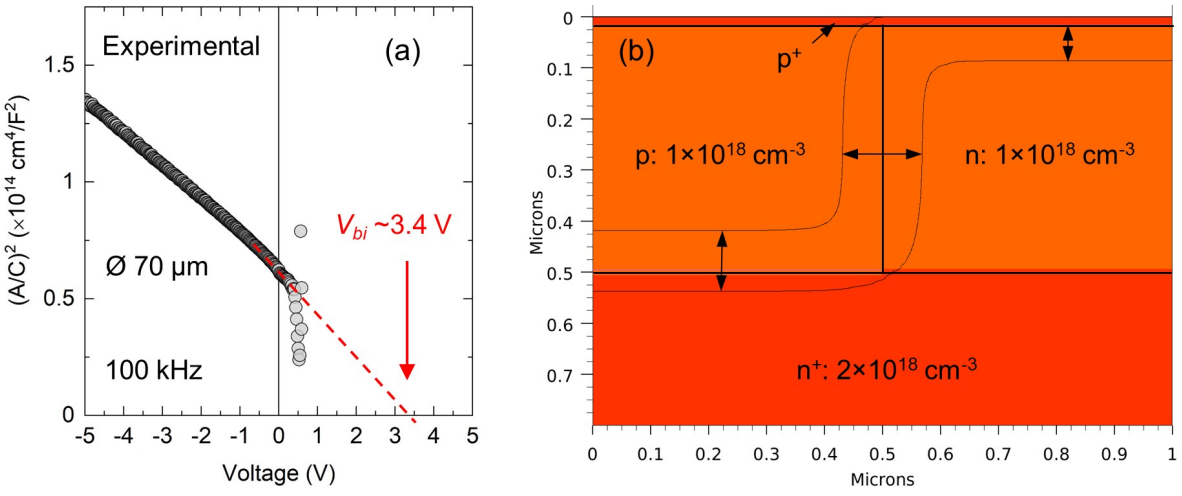

Figure 6.12: (a) $1/C^2$-V characteristics of the LPJ structure measured at 100 kHz frequency. (b) Cross-section of the simulated LPJ structure demonstrating depletion boundary at reverse bias -5V.

$$C_{LPJ} = C_N + C_{Ga} + C_{Ga-N} \tag{6.2}$$

where, C_{LPJ} is the total capacitance of the LPJ structure, C_N is the capacitance from a p^+-n junction in the N-polar domain, C_{Ga} is the capacitance from a p-n^+ junction in the Ga-polar domain, and $C_{Ga\text{-}N}$ is the capacitance from the lateral p-n junction between both domains. The above equation can also be written as:

$$C_{LPJ} = \frac{\varepsilon_S A_N}{t_N} + \frac{\varepsilon_S A_{Ga}}{t_{Ga}} + \frac{\varepsilon_S A_{Ga-N}}{t_{Ga-N}} \tag{6.3}$$

where, A and t are the area and the depletion width of each capacitance mentioned above.

For the area (A=X×Z) of the simulated structure shown in Fig. 6.12(b), one side (Z direction) of the area is the same for all three cases. For the other side (X) in the area, for A_N and A_{Ga} cases, the dimension is 0.5 μm for each case. In contrast, for $A_{Ga\text{-}N}$, the dimension for the X is only 0.3 μm, subtracting 0.2 μm from 0.5 μm due to depletion from the top and bottom junctions [see Fig. 6.12(b)]. Now, comparing the A/t ratios for all three capacitances, the portion from the lateral p-n junction can be neglected as the area is smaller than the other two junctions. Thus, it can be assumed that the total capacitance could be mainly from the two parallel capacitances from p^+-n and p-n^+ junctions. This assumption is only valid as the drift region thickness is comparable to the column widths. In the case that a thicker drift region would be used, however, the capacitance from the lateral junction would be higher than the other two capacitances.

Using the above assumption, the doping level of the LPJ structure is calculated from the experimental C-V analysis by considering the area of the diode based on 70 μm diameter. The calculated doping level as a function of the bias is shown in Fig. 6.13. It can be observed that

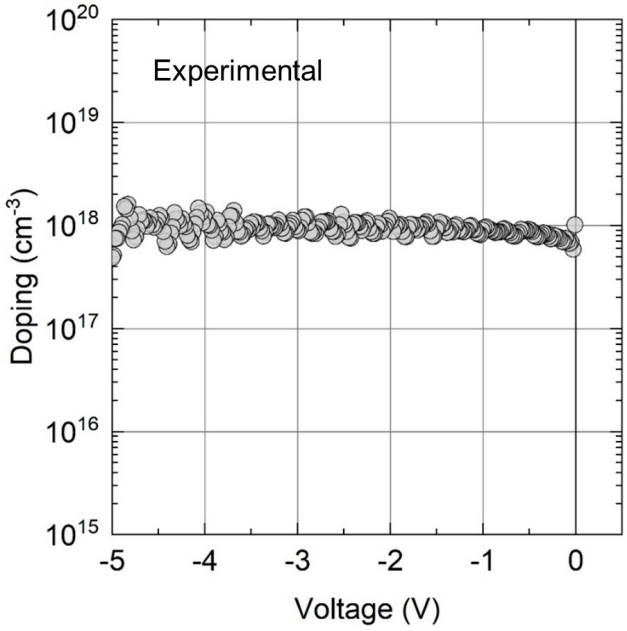

Figure 6.13: Extracted net doping level as a function of the bias extracted from the C-V measurements.

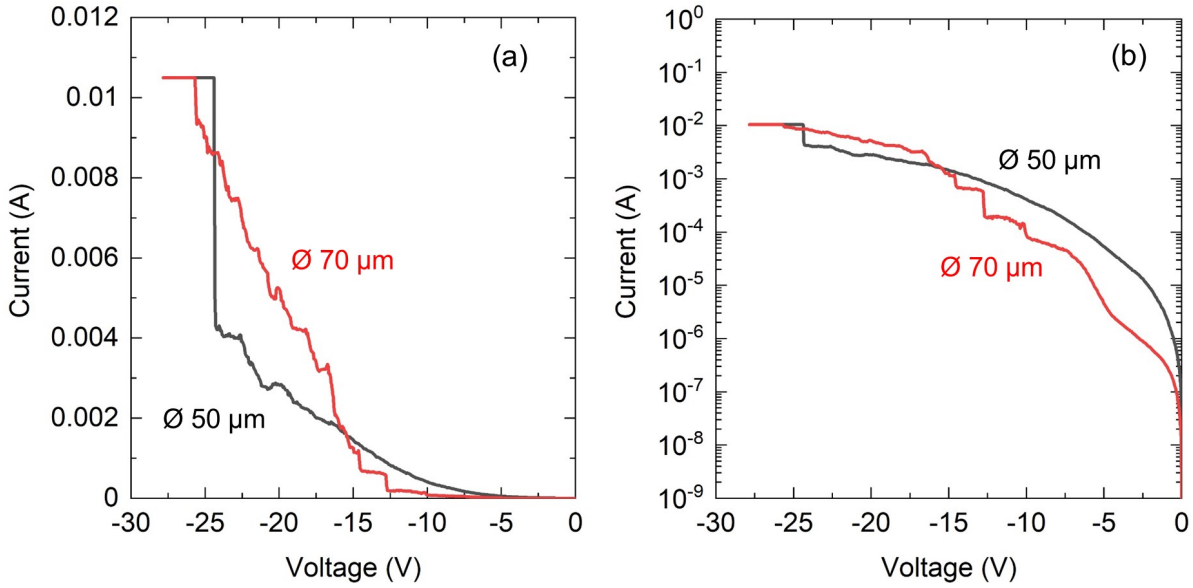

Figure 6.14: Experimental I-V characteristics of the grown LPJ structure for two different diameter devices in (a) linear and (b) semilog scale.

the effective doping obtained for the LPJ structure is $\sim 1\times10^{18}$ cm^{-3} which is in agreement with SIMS and APT results.

Figures 6.14(a) and 6.14(b) show the reverse bias I-V measurements to investigate the breakdown performance of the grown LPJ structure for two different diameters (50 μm and 70 μm) in linear and semilog scales, respectively. Per the linear I-V shown in Fig. 6.14(a), the breakdown voltages are around 25 V for both the diodes. This is a minimal value from a GaN SJ standpoint as the doping levels in the lateral p-n drift region are 4 times higher than the required doping level to obtain complete lateral depletion for the designed column width. Thus, the LPJ structure grown here behaves as a camel diode rather than a SJ diode, which is why the breakdown voltage is reduced. For future devices, either the column width can be reduced to 1/4 for the obtained doping ($\sim 1\times10^{18}$ cm^{-3}) here, or the doping level in the drift region can be reduced to 1/4 for the designed column width (1 μm) here. In addition, a thicker drift region is also necessary to obtain higher breakdown voltages. For example, Fig. 6.15 shows required device design parameters to obtain 1750 V breakdown voltage GaN SJ using LPJ approach.

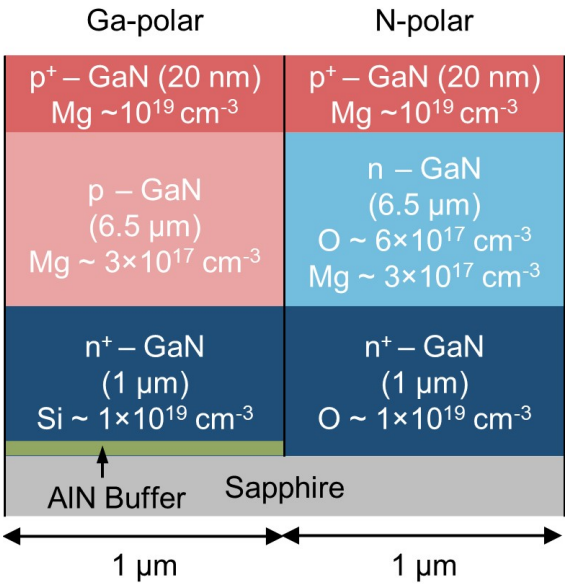

Figure 6.15: Proposed 1750 V breakdown voltage GaN SJ device using LPJ approach.

6.5 Conclusion

In conclusion, the development of supersaturation modulated growth technique allowed to obtain equal height and charge-balanced lateral polar junctions in a single and continuous growth run. The SEM and TEM images confirmed that the surface of the LPJ is smooth, and the IDB is abrupt. The SIMS and APT results confirmed that the drift region of the Ga-polar domain is p-type and the N-polar domain is n-type and have equal doping levels $\sim 1 \times 10^{18}$ cm^{-3} in both domains. The C-V characteristics are also in agreement with the SIMS and APT analysis. The I-V characteristics confirmed the formation of the camel diode on the N-polar GaN domain with the help of an additional thin p^+ layer on top of the drift region. The breakdown voltage of the fabricated LPJ is around 25 V only. This is due to the wider column width (1 μm) than the required column width (<250 nm) in order to have complete lateral depletion. Nonetheless, the experiment designed here demonstrates the necessary charge balance from a SJ application perspective and serves as a pathway for future GaN-based vertical superjunction devices. High-performance GaN SJ devices can be realized in the future by reducing the doping or column widths further and increasing the drift region thickness.

Chapter 7

GaN-on-GaN PN Diodes using Mg Ion Implantation

Besides LPJs, ion implantation can be another approach to obtain the p- and n-type columns needed to construct SJ devices, and has already been demonstrated in Si and SiC technology. In GaN technology, the SJ would be realized by forming n-type regions during epitaxy, while p-type doping would be achieved via selective-area Mg ion implantation. However, GaN does not possess a robust ion implantation toolbox that allows for reliable implantation control and activation. Recent advances in the realization of p-type GaN via Mg ion implantation and high-temperature and ultra-high-pressure post-implantation annealing techniques have opened a path to achieve SJ devices in GaN. A detailed review on the state-of-the-art p-type ion implantation post-activation annealing techniques was presented in Chapter 1.

7.1 Introduction

Mg implantation into GaN represents a critical technological step required to realize p-type selective area doping for various devices such as GaN Junction Barrier Schottky (JBS) diodes, Junction Field Effect Transistors (JFETs), and Superjunction diodes and transistors with a high voltage blocking capability. For simplicity, in this work, a p-n diode is fabricated with uniform Mg ion implantation across the wafer to demonstrate the capability of achieving p-type doping. The p-n diode is fabricated with a 2 μm junction depth and n-GaN drift

region thickness of 5 μm. A negative bevel edge termination with a shallow angle of 30° is used to suppress surface electric field crowding and achieve a maximum breakdown electric field strength. To this end, this chapter presents a GaN-on-GaN p-n diode whose p-region is formed by Mg implantation into a GaN epitaxial layer and exhibits a breakdown voltage of 1 kV. The maximum electric field measured across the p-n diode is 3.36 MV/cm at 1 kV. This is among the best reported measured breakdown fields for a vertical GaN p-n diode, and, to the best of our knowledge, the first for Mg-implanted devices of this type. The successful demonstration of Mg activation and achieving p-type doping in GaN opens up a path to realize GaN SJ devices using selective area p-type doping.

7.2 Experimental Details

A total 7 μm-thick Si doped n-GaN epilayer (N_D ~2×10^{16} cm^{-3}) was grown using MOCVD on n^+-GaN substrate to fabricate a p-n diode as shown in Fig. 7.1(a). Using Monte Carlo

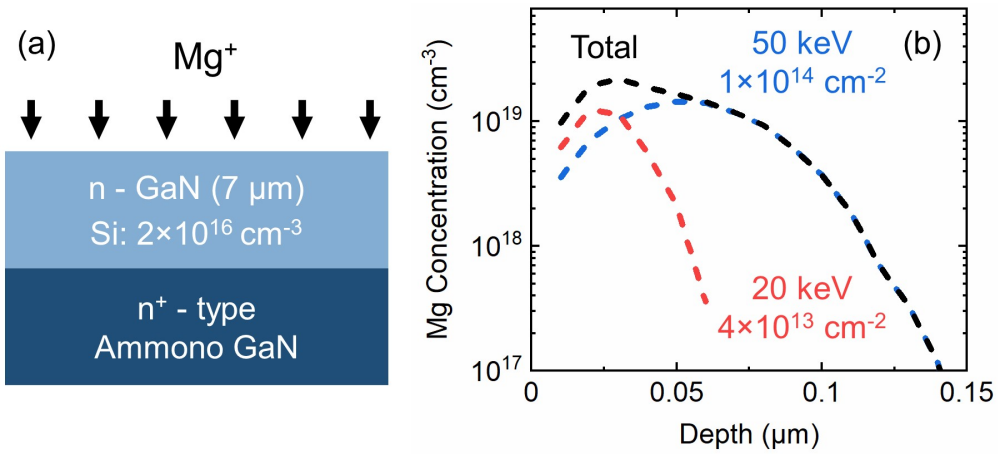

Figure 7.1: (a) Schematic cross-section of an epi-layer grown on Ammono GaN substrate used for Mg ion implantations. (b) Monte Carlo simulation predicting the implanted Mg ion profiles.

simulation (Fig. 7.1(b)), a Mg box profile with a depth of 50 nm was designed using ion implantations at 20 and 50 keV energies and 4×10^{13}, 1×10^{14} cm^{-2} doses, respectively. The Mg activation anneal was performed at 1300 °C for 100 minutes, at a high-pressure of 1 GPa in N_2 ambient, and without a capping layer [87]. Fig. 7.2 show SIMS results of Mg and Si concentration profiles in the device, respectively. The as-implanted Mg ion profile matches our Monte Carlo simulations. After the high-temperature activation process, the Mg ion profile forms a 2 μm diffusion tail into n-GaN, as shown in Fig. 7.2. The Mg concentration decreases from 2×10^{18} cm^{-3} to 5×10^{16} cm^{-3} over the 2 μm depth.

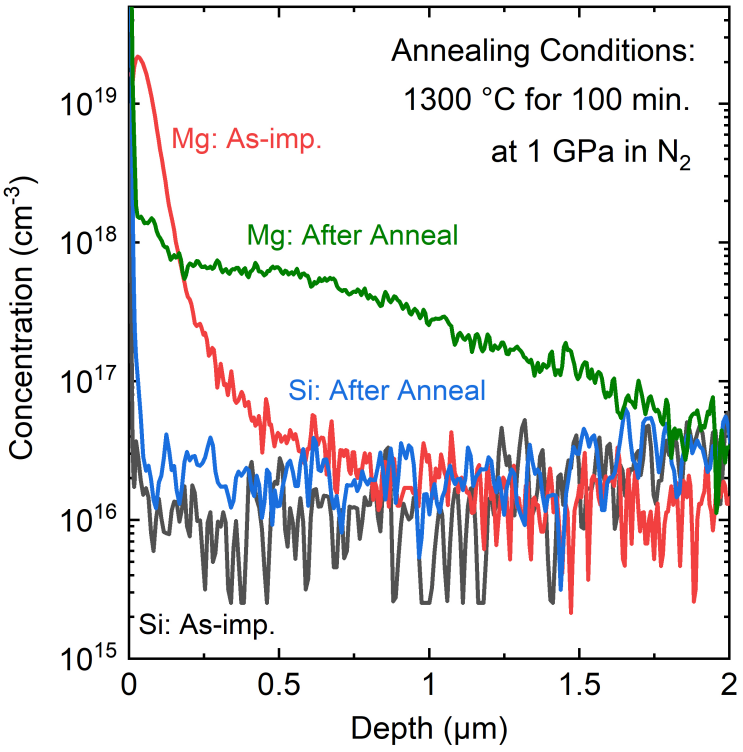

Figure 7.2: Secondary ion mass spectroscopy (SIMS) depth profiles of Si and Mg concentration immediately following implantation and after high-pressure, high-temperature annealing (HPHT) at 1 GPa and 1300 °C for 100 minutes in N_2 ambient.

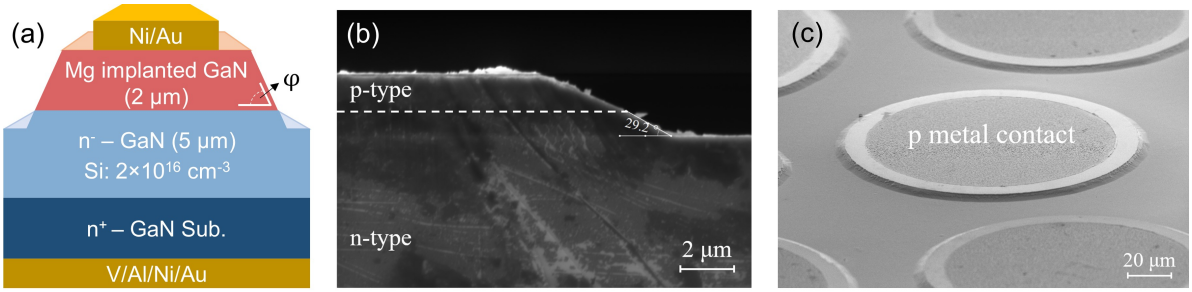

Figure 7.3: (a) Schematic cross section of a vertical GaN p-n diode with bevel edge termination. (b) Cross-sectional SEM showing 30° bevel edge termination, and (c) tilted SEM image of the fabricated p-n diode.

After Mg activation anneal, the p-n diode fabrication process started with the formation of a bevel edge termination. A 4 μm thick photoresist was used for photolithography, followed by a high-temperature hard bake anneal at 125 °C and for 2 min on a hot plate. Mesa etching was done using Cl_2-based inductively coupled plasma reactive ion etching (ICP-RIE). The height of the bevel edge was 2.5 μm with an edge angle of approximately 30°. The electrodes were then deposited by e-beam evaporation with Ni/Au (20/40 nm) on the epitaxial layer for the anode and V/Al/Ni/Au (30/100/70/70) for the cathode on the backside of the substrate, respectively. The contacts were then alloyed at 600 °C for 10 min in air ambient to achieve ohmic behavior. The schematic cross-section of the fabricated p-n diode is shown in Fig. 7.3(a). Fig. 7.3(b) shows the cross-sectional scanning electron microscopy (SEM) image of the bevel edge termination. The SEM image of the fabricated p-n diode is shown in Fig. 7.3(c).

7.3 Results and Discussion

Capacitance-voltage (C-V) measurements were done to extract the built-in potential and the effective doping concentration in the drift region. Fig. 7.4(a) shows that the built-in potential of the diode is around 4 V. The effective doping concentration vs. voltage profile for the

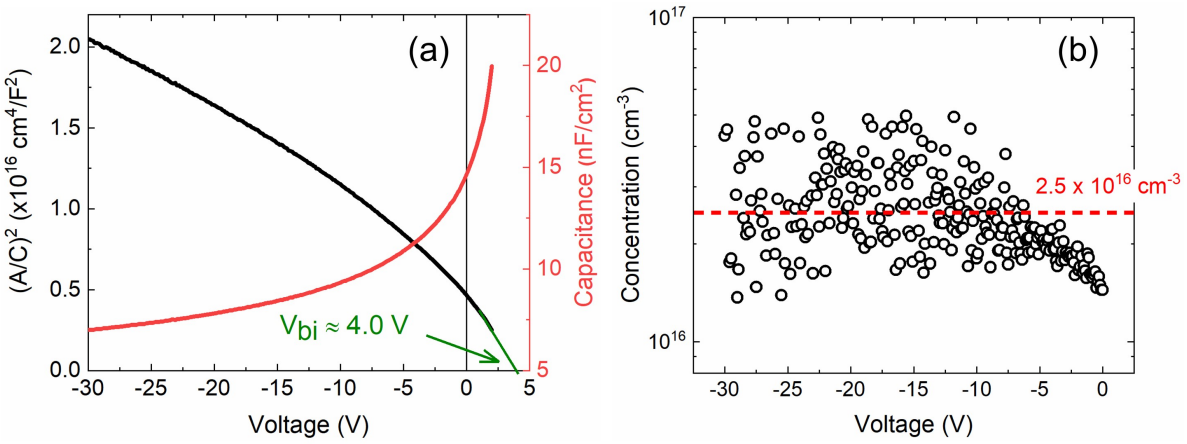

Figure 7.4: (a) The C-V and the $1/C^2$-V characteristics of the fabricated p-n diode. (b) The extracted charge concentration up to -30 V. The average charge concentration in n-GaN is 2.5×10^{16} cm^{-3}.

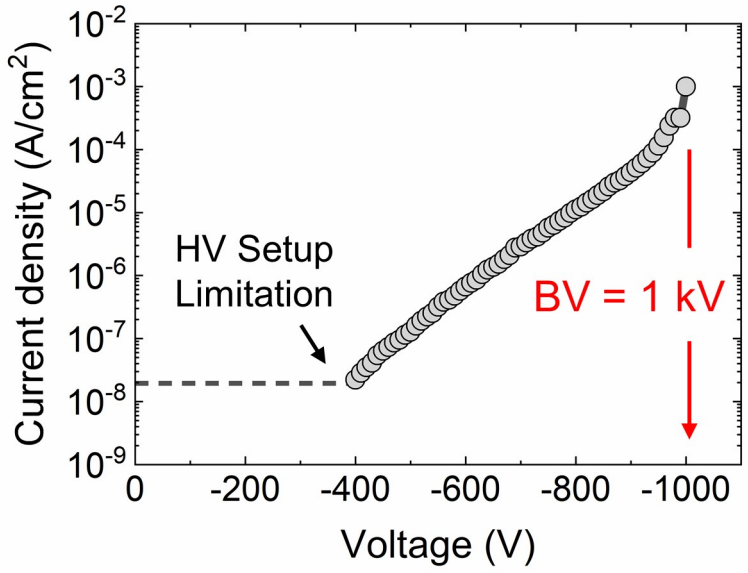

Figure 7.5: Reverse bias I-V characteristic of the fabricated GaN p-n diode.

n-GaN layer can be obtained using the $1/C^2$-V plot shown in Fig. 7.4(b). The net doping concentration for the n-GaN layer is thus confirmed to be around 2.5×10^{16} cm^{-3}. Figure 7.5 shows the reverse bias characteristic of the device, which exhibits a breakdown voltage of 1 kV. This result points to the effectiveness of the bevel edge termination. The minimum measurable reverse leakage current was limited by the Keithley 2657A that was used.

To estimate the maximum electric field in the device at 1 kV, TCAD simulations were performed using Silvaco. The p-type doping profile was modeled to fit the Mg doping profile obtained from SIMS in order to most accurately and realistically represent the measured device's behavior. The simulated p-type doping profile to match SIMS Mg doping profile after UHPA activation anneal is shown in Fig. 7.6(a). The n-type doping value that is used

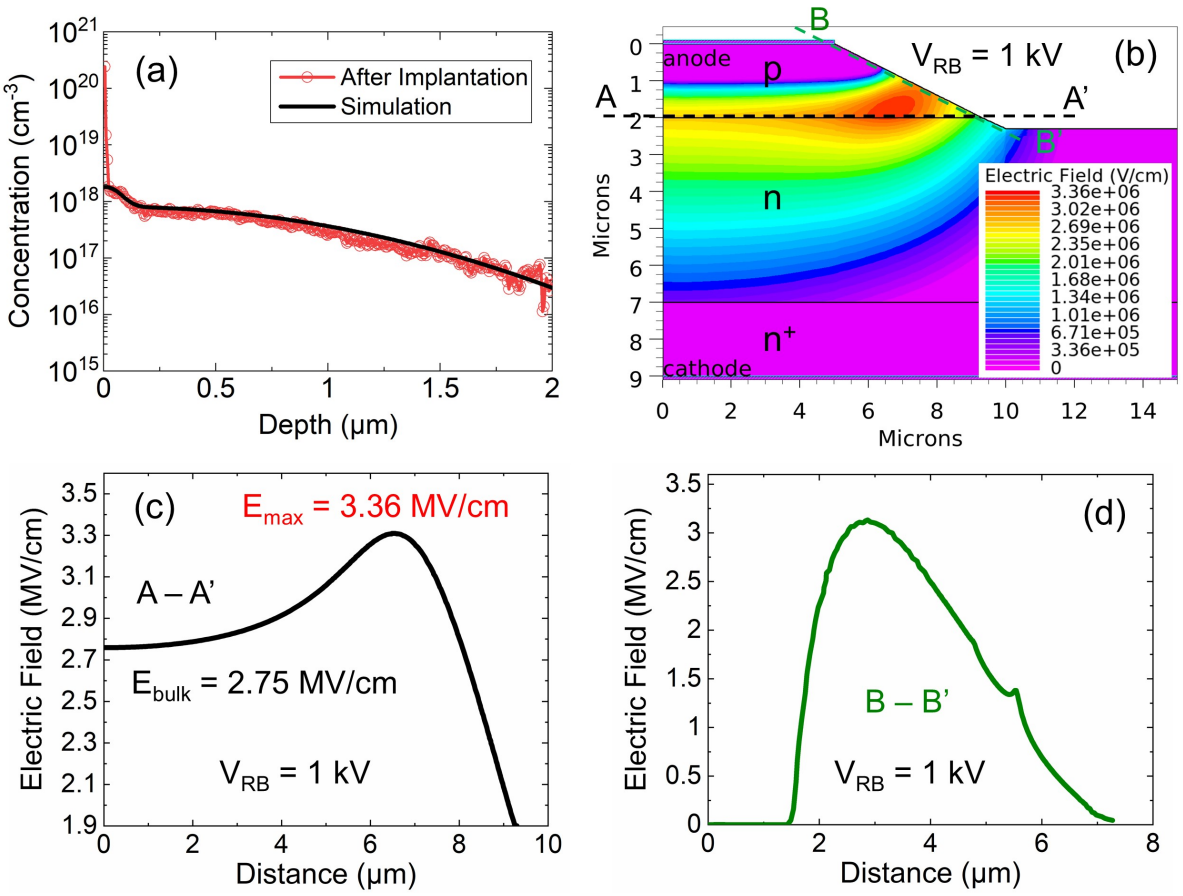

Figure 7.6: (a) The fitted Mg doping profile used in TCAD compared with the obtained Mg profile from SIMS after implantation and activation anneal. (b) The 2-dimensional electric field distribution at 1 kV calculated by TCAD simulation. The maximum electric field in the device is 3.36 MV/cm. The electric field profile (c) at the p-n junction interface (d) at the bevel edge surface. The max. E-field is inside the device rather than the bevel edge surface.

comes from the $1/C^2$-V graph. The 2D electric field contour in the device at 1 kV reverse bias voltage is obtained and shown in Fig. 7.6(b). Fig. 7.6(c) displays the electric field distribution in the x-direction (A-A') along the p-n junction. It is found that the electric field in the bulk of the p-n diode is 2.75 MV/cm, and the maximum electric field of 3.36 MV/cm is located below the surface and away from the mesa sidewall. For comparison, the electric field distribution along the surface of the bevel edge is shown in Fig. 7.6(d). A maximum surface electric field strength of 3.0 MV/cm demonstrates that the negative bevel edge termination helps to reduce the electric field at the surface with respect to the bulk. It is worth noting that even though the bevel angle is relatively high (30°), the negative bevel edge termination is effective here because of the low N_A/N_D ratio [260]. These results demonstrate that the p-type GaN via Mg implantation can be achieved and used to block high voltages.

7.4 Conclusion

In conclusion, Mg implantation was used to form p-n junctions in GaN with 1 kV blocking capability. Both the 1 kV breakdown voltage and the maximum electric field of 3.36 MV/cm are among the best reported thus far and compare favorably with the p-n diodes formed via epitaxy. This represents a critical milestone towards the realization of selective area p-type doping from the GaN SJ design perspective. This technology can also be leveraged in the future to create GaN-based junction barrier Schottky (JBS) diodes, vertical GaN MOSFETs/JFETs, or highly efficient edge terminations, such as floating field rings (FFRs).

Chapter 8

Conclusions and Outlook

8.1 Conclusions

The objective of this thesis has been to explore techniques to realize GaN-based vertical SJ devices. The use of LPJ's has been principally studied, as it represents a unique growth approach heretofore unavailable in traditional Si and SiC technologies. The chemical and electronic properties of N-polar GaN were studied to systematically establish, for the first time, methods to fabricate barrier-controlled and thermally-stable diodes. Moreover, the first charge-balanced GaN SJ structure was designed and characterized. Both of these outcomes represent key technological milestones towards the realization of LPJ-based GaN SJ devices. The viability of Mg implantation for selective area p-type doping in GaN was also established for SJ devices, edge terminations or both. Overall, the designed experiments and their outcomes demonstrate that these techniques provide a path towards realizing GaN SJ devices in the future.

Chapter 2 provided a simple theoretical model to predict GaN SJ device design parameters such as drift region columns thickness, widths, and doping levels for a given breakdown voltage application. An ideal specific on-resistance vs. breakdown voltage performance for GaN SJ devices was reported for three different column widths ($W_N = W_P$) 0.2 μm, 0.5 μm, and 1 μm. Compared to conventional GaN unipolar devices, these GaN SJ devices showed significantly lower on-resistance at given breakdown voltages. Using the developed analytical model, a GaN SJ drift region with 1750 V breakdown voltage was designed and simulated using Silvaco.

TCAD simulation results were in agreement with the developed theoretical model for GaN SJ, which indicated that the GaN SJ device parameters could be predicted using these designed equations. The developed theroretical model in this work provides a simplified and more intuitive approach to design GaN SJ devices in comparison to the literature, which would save substantial computation and time. The impact of charge imbalance on GaN SJ performances was studied by varying the doping levels in either p- or n-type columns when the doping in the other column is at the optimum level.

In Chapter 3, n-type N-polar GaN material properties were studied by forming Schottky contacts on them. From I-V characteristics, the extracted threshold voltage, ideality factor, and Schottky barrier height for as-grown N-polar GaN surface are 0.4 V, 1.07, and 0.4 eV, respectively. The extracted doping for n-type N-polar GaN via C-V measurements is 7×10^{17} cm^{-3}. This demonstrates that the unintentional oxygen level is reduced in N-polar GaN substantially from high 10^{19} cm^{-3} to lower than 10^{18} cm^{-3} doping range, which is necessary for the n-type drift region of the envisioned GaN SJ. From the high voltage rating SJ device application perspective, the measured barrier height for the N-polar GaN Schottky diode was very low. In addition, it was observed that the N-polar GaN surface reacts to different chemicals such as bases and acids. A thorough investigation of how these chemicals alter the electrical properties of the Schottky contacts was provided. It was observed that bases and acids can etch the surface and increase the roughness by forming triangular/hexagonal crystallographic facets. It was observed that the sizes of these features are in the range of tens to hundreds of nm. This etching would create an issue especially when a few nm thin p^+-type layer would be grown on n-type N-polar GaN to form camel junction. The Schottky diodes on this rough N-polar GaN surface showed slightly higher barrier height, as a result of the metals in contact to the exposed facets that were a mixure of N-polar and semi-polar crystal faces. Also, the diodes showed higher ideality factors, which could be due to the

additional tunneling components at lower biases as a result of enhaced filed at the sharp crystal facets. It was noticed that the solvent-based e-beam lithography resist developer (MIBK) does not damage the N-polar GaN surface, which demonstrates a possible solution to process N-polar GaN devices. The results of this study underline the critical role played by common processing chemicals in determining the performance of the N-polar GaN devices.

To tackle the challenges associated with N-polar GaN, such as chemical sensitivity and low barrier height, an ultra-thin LPCVD SiN interlayer was introduced in Chapter 4. First, 7 nm LPCVD SiN was deposited on N-polar GaN to investigate its properties. It was found that the SiN interlayer has a high density ($>10^{19}$ cm^{-3}) of point-defect level, which forms the defect band aligned with the N-polar GaN conduction band edge. It was observed that the surface termination of the SiN interlayer had a significant influence on the diode barrier characteristics. When metal is deposited on HF-treated SiN, the SiN/GaN interface is responsible for determining the system's barrier height (0.4 eV), whereas the use of oxidized SiN leads to a metal/SiN-dominant barrier (1.1 eV). Using this knowledge, a 5 nm SiN interlayer was introduced between the metal and N-polar GaN to leverage high-performance Schottky diodes. The barrier height was increased to 0.8 eV, which is 0.4 eV higher than as-grown surface Schottky diodes. The increment in barrier height helped reduce the reverse bias leakage and improved the elevated temperature operation capabilities of the N-polar GaN diodes. Reliable operation of N-polar GaN diodes with SiN interlayer was demonstrated till 400 °C. In contrast, before this study, the highest reported temperature of operation for an N-polar GaN Schottky diode was 175 °C. This could offer a reliable solution to N-polar GaN technology, which would help to realize GaN SJ devices using the LPJ approach. Further performance improvement can be achieved by tuning the thickness of the SiN layer and the choice of metal. This work is the first demonstration of increasing the barrier height with the use of thin SiN interlayer in N-polar GaN technology.

As an alternative approach to increase the barrier height of the N-polar GaN diode, camel diodes are proposed in Chapter 5. Not only do camel diodes offer a pathway to even higher barrier heights than diodes with SiN interlayers, but they also avoid the reliability issues associated with time-dependent dielectric breakdown, which would represent a major bottleneck. To obtain camel diodes, first p-type doping in N-polar GaN was demonstrated via Hall measurements. The free hole carrier concentrations, mobility, and resistivity at room temperature were reported to be around 1.5×10^{18} cm^{-3}, 3.4 cm^2/Vs, and 1.2 $\Omega\cdot cm$. Mg ionization energy in the p-type N-polar GaN was around 150 meV, and the compensating oxygen and nitrogen vacancies were only 10% of the total Mg. Later, N-polar GaN p-n diodes were fabricated and compared to Ga-polar GaN diodes. Extensive electrical characteristics are reported and analyzed. It was observed that the N-polar GaN p-n diodes showed inferior characteristics compared to the diodes made with Ga-polar GaN. SIMS measurements were performed on both polarity diodes, which demonstrated the delay in Mg incorporation at the start of the p-type layer growth. The theoretical design for the GaN camel diode is first presented and validated with the TCAD simulations. Two different p^+ layer doping camel diode were fabricated and characterized. Although these diodes showed poor reverse bias performance due to high unintentional background oxygen incorporation, the threshold voltage of these camel diodes was higher than the Schottky diodes. The threshold voltage was increased to 1 V in the case of 10 nm p^+ layer with Mg doping level 10^{19} cm^{-3}, which is 0.6 V higher than the Schottky diode. The observed higher reverse bias leakage could be reduced by lowering the unintentional oxygen level in the camel diode's p^+- and n-type layer. The demonstration of achieving higher threshold voltage using the camel junction in N-polar GaN realizes an essential design requirement in the pathway towards a GaN SJ.

By integrating all the developed building blocks mentioned above, a charge-balanced GaN lateral polar junction with equal domain heights is reported in Chapter 6. Prior to LPJ

growth, the AlN buffer layer was patterned with a 2 μm pitch size to realize 1 μm wide Ga- and N-polar GaN domains. The topmost layer of the grown LPJ structure consisted of a 20 nm p^+ layer with a 10^{19} cm^{-3} Mg doping level to form a camel junction in the N-polar domain. The grown LPJ structure was then analyzed using different material characterization techniques. First, the SEM and TEM analysis demonstrated that the LPJ domains have equal heights and have a single atomic layer IDB. SIMS and APT analysis demonstrated that the Ga-polar domains were p-type with doping level $\sim 1\times10^{18}$ cm^{-3} (Mg), and N-polar domains were n-type with net doping level $\sim 1\times10^{18}$ cm^{-3} (O-Mg). Later, LPJ diodes were fabricated and performed electrical characterizations. The I-V characteristics demonstrated a higher threshold voltage (1.15 V) than the Schottky diode, which suggested the formation of camel junction. Using the C-V analysis, the extracted net doping level in the LPJ structure was around 1×10^{18} cm^{-3}, which again confirmed the SIMS and APT analysis results. It is worth noting that these charge balanced domains were obtained in a single growth run, which means a desired drift region thickness could be achieved without any issues related to regrowth requirements or lithographic misalignments errors for regrowth. This is a fundamentally new approach to SJ growth compared to traditional techniques used in Si and SiC technology. The result presented here is the first demonstration of achieving equal p- and n-type doping levels selectively in GaN technology. Additionally, the demonstration of low oxygen concentration level in N-polar GaN domain opens up a path towards achieving high breakdown voltage drift regions for SJ devices, which had not been demonstrated in previously reported lateral polar junctions. All these results concluded that the lateral polar junction approach could be utilized to obtain GaN-based vertical SJ devices in the future.

In an alternative approach to LPJ to realize GaN SJ, selective area p-type doping using Mg ion implantation was proposed. To this end, p-n diodes were realized via blanket Mg ion implantation on n-type epi-layer grown on GaN substrate. After the implantation, Mg ions

were activated using the UHPA technique at 1300 °C and 1 GPa pressure for 100 min under N_2 ambient. Electrical characterization results demonstrated that 1 kV breakdown voltage was achieved in these p-n diodes. The estimated maximum electric field using TCAD simulations was 3.36 MV/cm. These results are the first demonstration of such high breakdown voltage and electric field in GaN technology using Mg ion implantation. This was only possible due to the full activation of Mg ions as a result of successful post-implnatation activation anneal using UHPA technique. These results motivate that the selective area doping in GaN can be obtained via Mg ion implantation coupled with UHPA post-implantation activation anneal.

8.2 Future Work

In addition to the studies presented in this thesis, the following future research work is proposed.

- **High-temperature stable SiN/N-polar GaN diodes:** In Chapter 4, the high-temperature performance of the SiN interlayer N-polar GaN Schottky diodes were reported reliable operation up to 400 °C. Operating devices higher than that temperature might have caused reaction at the interface of the Ni Schottky metal and the Si-rich SiN. Because of that, the I-V characteristics at room temperature after operating at 500 °C were changed. Thus, to further improve the elevated temperature operation capability, different refractory metals such as Pt or W could be used as a Schottky metal. Another alternative could be the *in-situ* surface passivation of the SiN at the end of LPCVD deposition by passing oxygen gas. This would passivate the free Si on the SiN surface and prevent the formation of metal silicide.

- **Further improvements in N-polar GaN camel diode:** As reported in Chapter 5, the fabricated N-polar GaN camel diodes suffered from high reverse bias leakage due to the higher oxygen doping in the p^+- and an n-type layer. Thus, the first improvement in the device performance could be realized by reducing the oxygen level to the order of 10^{17} cm^{-3}. Once the oxygen level is controlled, camel diodes with different p^+ layer thickness and doping levels could be fabricated using the reported model in Chapter 5. The barrier height should be extracted using temperature-dependent I-V measurements to investigate whether different design parameters correspond to barrier height change accordingly.

- **Ga-polar GaN camel diode:** The barrier height for the Ga-polar GaN Schottky diodes is reported to be ∼0.7 eV [125], which is still lower in comparison to SiC Schottky diodes. Thus, a camel diode design could also increase the barrier height similar to what has been demonstrated in this thesis for N-polar GaN. This way, the barrier can be tuned from the Schottky limit to the p-n diode built-in potential depending upon the application. The increment in the barrier height should reduce the leakage current and improve the device performance.

- **Development of edge termination techniques for LPJ-based GaN SJ:** Due to the electric field crowding near the device periphery, a better edge termination is required to achieve maximum possible breakdown voltage near to its theoretical value. As the electric field would be higher throughout the drift region, as shown in Chapter 2, compared to its conventional device, it is critical to develop an edge termination for SJ devices. In literature, an edge termination technique compatible with the standard SJ fabrication process is developed [6] in which dielectric is refilled to the same thickness of the p/n column to get a breakdown within the drift region rather than at the periphery

of the SJ device. As the GaN SJ fabrication process flow using the LPJ approach is different from Si and SiC SJ devices, an edge termination technique needs to be developed for LPJ-based GaN SJ devices.

- **Realization of a kV-class vertical GaN SJ:** As reported in this thesis, the first major milestone towards achieving the GaN-based vertical SJ devices is demonstrated by obtaining the charge balance between the Ga-polar and N-polar domains while maintaining the equal heights of these domains. Nonetheless, the doping levels in these domains were around 1×10^{18} cm^{-3}, and the columns' width was 1 μm each. The total thickness of the drift region was only 0.5 μm. Based on the developed theoretical device design in Chapter 2, the drift region should be at least 4 μm thick to obtain at least a kV-class device. In the case of 1 μm column width for each domain, the required doping level should be in the order of $\sim3\times10^{17}$ cm^{-3} or lower than that. If the doping levels cannot be reduced from 1×10^{18} cm^{-3}, each column width needs to be at least 250 nm or lower. In addition, edge termination needs to be employed to obtain the breakdown voltage near the designed value, as mentioned above.

In general, the experiments and results of this thesis provided a pathway towards achieving GaN-based vertical SJ devices.

REFERENCES

[1] L. Mari, "The Importance of Power Engineering and Power Electronics: A Brief History - Market Insights," May 2020.

[2] B. J. Baliga, "Enhancement- and depletion-mode vertical-channel m.o.s. gated thyristors," *Electronics Letters*, vol. 15, no. 20, pp. 645–647, Sep. 1979. doi: 10.1049/el:19790459

[3] B. Baliga, M. Adler, P. Gray, R. Love, and N. Zommer, "The insulated gate rectifier (IGR): A new power switching device," in *1982 International Electron Devices Meeting*, Dec. 1982, pp. 264–267. doi: 10.1109/IEDM.1982.190269

[4] B. J. Baliga, *Fundamentals of Power Semiconductor Devices*. Springer US, 2008. doi: 10.1007/978-0-387-47314-7

[5] B. J. Baliga, *Advanced Power Rectifier Concepts*. Springer US, 2009. doi: 10.1007/978-0-387-75589-2

[6] B. J. Baliga, *Advanced Power MOSFET Concepts*. Springer US, 2010. doi: 10.1007/978-1-4419-5917-1

[7] B. J. Baliga, *Advanced High Voltage Power Device Concepts*. New York: Springer-Verlag, 2012. doi: 10.1007/978-1-4614-0269-5

[8] B. Baliga, "Power semiconductor device figure of merit for high-frequency applications," *IEEE Electron Device Letters*, vol. 10, no. 10, pp. 455–457, Oct. 1989. doi: 10.1109/55.43098

[9] J. Millán, P. Godignon, X. Perpiñà, A. Pérez-Tomás, and J. Rebollo, "A Survey of Wide Bandgap Power Semiconductor Devices," *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2155–2163, May 2014. doi: 10.1109/TPEL.2013.2268900

[10] B. J. Baliga, *Gallium Nitride and Silicon Carbide Power Devices*. World Scientific Publishing Company, 2016.

[11] J. Y. Tsao, S. Chowdhury, M. A. Hollis, D. Jena, N. M. Johnson, K. A. Jones, R. J. Kaplar, S. Rajan, C. G. V. d. Walle, E. Bellotti, C. L. Chua, R. Collazo, M. E. Coltrin, J. A. Cooper, K. R. Evans, S. Graham, T. A. Grotjohn, E. R. Heller, M. Higashiwaki, M. S. Islam, P. W. Juodawlkis, M. A. Khan, A. D. Koehler, J. H. Leach, U. K. Mishra, R. J. Nemanich, R. C. N. Pilawa-Podgurski, J. B. Shealy, Z. Sitar, M. J. Tadjer, A. F. Witulski, M. Wraback, and J. A. Simmons, "Ultrawide-Bandgap Semiconductors: Research Opportunities and Challenges," *Advanced Electronic Materials*, vol. 4, no. 1, p. 1600501, 2018. doi: 10.1002/aelm.201600501

[12] A. M. Ozbek and B. J. Baliga, "Planar Nearly Ideal Edge-Termination Technique for GaN Devices," *IEEE Electron Device Letters*, vol. 32, no. 3, pp. 300–302, Mar. 2011. doi: 10.1109/LED.2010.2095825

[13] J. W. Palmour, "Silicon carbide power device development for industrial markets," in *2014 IEEE International Electron Devices Meeting*, Dec. 2014, pp. 1.1.1–1.1.8. doi: 10.1109/IEDM.2014.7046960

[14] B. J. Baliga, "Silicon Carbide Power Devices: A 35 Year Journey from Conception to Commercialization," in *2018 76th Device Research Conference (DRC)*, Jun. 2018, pp. 1–2. doi: 10.1109/DRC.2018.8442172

[15] E. A. Jones, F. F. Wang, and D. Costinett, "Review of Commercial GaN Power Devices and GaN-Based Converter Design Challenges," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 707–719, Sep. 2016. doi: 10.1109/JESTPE.2016.2582685

[16] H. Amano, Y. Baines, E. Beam, M. Borga, T. Bouchet, P. R. Chalker, M. Charles, K. J. Chen, N. Chowdhury, R. Chu, C. De Santi, M. M. De Souza, S. Decoutere, L. Di Cioccio, B. Eckardt, T. Egawa, P. Fay, J. J. Freedsman, L. Guido, O. Häberlen, G. Haynes, T. Heckel, D. Hemakumara, P. Houston, J. Hu, M. Hua, Q. Huang, A. Huang, S. Jiang, H. Kawai, D. Kinzer, M. Kuball, A. Kumar, K. B. Lee, X. Li, D. Marcon, M. März, R. McCarthy, G. Meneghesso, M. Meneghini, E. Morvan, A. Nakajima, E. M. S. Narayanan, S. Oliver, T. Palacios, D. Piedra, M. Plissonnier, R. Reddy, M. Sun, I. Thayne, A. Torres, N. Trivellin, V. Unni, M. J. Uren, M. Van Hove, D. J. Wallis, J. Wang, J. Xie, S. Yagi, S. Yang, C. Youtsey, R. Yu, E. Zanoni, S. Zeltner, and Y. Zhang, "The 2018 GaN power electronics roadmap," *J. Phys. D: Appl. Phys.*, vol. 51, no. 16, p. 163001, Apr. 2018. doi: 10.1088/1361-6463/aaaf9d

[17] T. Ueda, "GaN power devices: current status and future challenges," *Jpn. J. Appl. Phys.*, vol. 58, no. SC, p. SC0804, Jun. 2019. doi: 10.7567/1347-4065/ab12c9

[18] J. Appels and H. Vaes, "High voltage thin layer devices (RESURF devices)," in *1979 International Electron Devices Meeting*, Dec. 1979, pp. 238–241. doi: 10.1109/IEDM.1979.189589

[19] T. Fujihira, "Theory of Semiconductor Superjunction Devices," *Jpn. J. Appl. Phys.*, vol. 36, no. 10R, p. 6254, Oct. 1997. doi: 10.1143/JJAP.36.6254

[20] G. Deboy, N. Marz, J.-P. Stengl, H. Strack, J. Tihanyi, and H. Weber, "A new generation of high voltage MOSFETs breaks the limit line of silicon," in *International Electron Devices Meeting 1998. Technical Digest (Cat. No.98CH36217)*, Dec. 1998, pp. 683–685. doi: 10.1109/IEDM.1998.746448

[21] M. Saggio, D. Fagone, and S. Musumeci, "MDmesh^{TM}: innovative technology for high voltage Power MOSFETs," in *12th International Symposium on Power Semiconductor Devices ICs. Proceedings (Cat. No.00CH37094)*, May 2000, pp. 65–68. doi: 10.1109/ISPSD.2000.856774

[22] F. Udrea, G. Deboy, and T. Fujihira, "Superjunction Power Devices, History, Development, and Future Prospects," *IEEE Transactions on Electron Devices*, vol. 64, no. 3, pp. 713–727, Mar. 2017. doi: 10.1109/TED.2017.2658344

[23] T. Minato, T. Nitta, A. Uenisi, M. Yano, M. Harada, and S. Hine, "Which is cooler, trench or multi-epitaxy? Cutting edge approach for the silicon limit by the super trench power MOS-FET (STM)," in *12th International Symposium on Power Semiconductor Devices ICs. Proceedings (Cat. No.00CH37094)*, May 2000, pp. 73–76. doi: 10.1109/ISPSD.2000.856776

[24] J. Sakakibara, Y. Noda, T. Shibata, S. Nogami, T. Yamaoka, and H. Yamaguchi, "600V-class Super Junction MOSFET with High Aspect Ratio P/N Columns Structure," in *2008 20th International Symposium on Power Semiconductor Devices and IC's*, May 2008, pp. 299–302. doi: 10.1109/ISPSD.2008.4538958

[25] A. Steiner, "Infineon's most well balanced high voltage MOSFET technology," p. 36, Mar. 2019.

[26] X. Zhong, B. Wang, J. Wang, and K. Sheng, "Experimental Demonstration and Analysis of a 1.35-kV 0.92-mΩ·cm^2 SiC Superjunction Schottky Diode," *IEEE Transactions on Electron Devices*, vol. 65, no. 4, pp. 1458–1465, Apr. 2018. doi: 10.1109/TED.2018.2809475

[27] R. Kosugi, S. Ji, K. Mochizuki, K. Adachi, S. Segawa, Y. Kawada, Y. Yonezawa, and H. Okumura, "Breaking the Theoretical Limit of 6.5 kV-Class 4H-SiC Super-Junction (SJ) MOSFETs by Trench-Filling Epitaxial Growth," in *2019 31st International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, May 2019, pp. 39–42. doi: 10.1109/ISPSD.2019.8757632

[28] H. Wang, C. Wang, B. Wang, N. Ren, and K. Sheng, "4H-SiC Super-Junction JFET: Design and Experimental Demonstration," *IEEE Electron Device Letters*, vol. 41, no. 3, pp. 445–448, Mar. 2020. doi: 10.1109/LED.2020.2969683

[29] R. Ghandi, A. Bolotnikov, S. Kennerly, C. Hitchcock, P.-m. Tang, and T. P. Chow, "4.5kV SiC Charge-Balanced MOSFETs with Ultra-Low On-Resistance," in *2020 32nd International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, Sep. 2020, pp. 126–129. doi: 10.1109/ISPSD46842.2020.9170171

[30] H. Kawai, S. Yagi, S. Hirata, F. Nakamura, T. Saito, Y. Kamiyama, M. Yamamoto, H. Amano, V. Unni, and E. M. S. Narayanan, "Low cost high voltage GaN polarization superjunction field effect transistors," *physica status solidi (a)*, vol. 214, no. 8, p. 1600834, 2017. doi: 10.1002/pssa.201600834

[31] A. Nakajima, Y. Sumida, M. H. Dhyani, H. Kawai, and E. M. Narayanan, "GaN-Based Super Heterojunction Field Effect Transistors Using the Polarization Junction Concept," *IEEE Electron Device Letters*, vol. 32, no. 4, pp. 542–544, Apr. 2011. doi: 10.1109/LED.2011.2105242

[32] R. Chu, "GaN power switches on the rise: Demonstrated benefits and unrealized potentials," *Appl. Phys. Lett.*, vol. 116, no. 9, p. 090502, Mar. 2020. doi: 10.1063/1.5133718

[33] A. Nakajima, K. Adachi, M. Shimizu, and H. Okumura, "Improvement of unipolar power device performance using a polarization junction," *Appl. Phys. Lett.*, vol. 89, no. 19, p. 193501, Nov. 2006. doi: 10.1063/1.2372758

[34] V. Unni and E. M. S. Narayanan, "Breaking the GaN material limits with nanoscale vertical polarisation super junction structures: A simulation analysis," *Jpn. J. Appl. Phys.*, vol. 56, no. 4S, p. 04CG02, Apr. 2017. doi: 10.7567/JJAP.56.04CG02

[35] S.-W. Han, J. Song, and R. Chu, "GaN Super-Heterojunction Schottky Barrier Diode with Over 10 kV Blocking Voltage," in *2021 5th IEEE Electron Devices Technology Manufacturing Conference (EDTM)*, Apr. 2021, pp. 1–3. doi: 10.1109/EDTM50988.2021.9420906

[36] P. Reddy, M. P. Hoffmann, F. Kaess, Z. Bryan, I. Bryan, M. Bobea, A. Klump, J. Tweedie, R. Kirste, S. Mita, M. Gerhold, R. Collazo, and Z. Sitar, "Point defect reduction in wide bandgap semiconductors by defect quasi Fermi level control," *Journal of Applied Physics*, vol. 120, no. 18, p. 185704, Nov. 2016. doi: 10.1063/1.4967397

[37] P. Reddy, S. Washiyama, F. Kaess, R. Kirste, S. Mita, R. Collazo, and Z. Sitar, "Point defect reduction in MOCVD (Al)GaN by chemical potential control and a comprehensive model of C incorporation in GaN," *Journal of Applied Physics*, vol. 122, no. 24, p. 245702, Dec. 2017. doi: 10.1063/1.5002682

[38] R. Collazo, S. Mita, A. Aleksov, R. Schlesser, and Z. Sitar, "Growth of Ga- and N- polar gallium nitride layers by metalorganic vapor phase epitaxy on sapphire wafers," *Journal of Crystal Growth*, vol. 287, no. 2, pp. 586–590, Jan. 2006. doi: 10.1016/j.jcrysgro.2005.10.080

[39] H. P. Maruska and J. J. Tietjen, "THE PREPARATION AND PROPERTIES OF VAPOR-DEPOSITED SINGLE-CRYSTAL-LINE GaN," *Appl. Phys. Lett.*, vol. 15, no. 10, pp. 327–329, Nov. 1969. doi: 10.1063/1.1652845

[40] H. Amano, N. Sawaki, I. Akasaki, and Y. Toyoda, "Metalorganic vapor phase epitaxial growth of a high quality GaN film using an AlN buffer layer," *Appl. Phys. Lett.*, vol. 48, no. 5, pp. 353–355, Feb. 1986. doi: 10.1063/1.96549

[41] T. Sasaki and T. Matsuoka, "Substrate-polarity dependence of metal-organic vapor-phase epitaxy-grown GaN on SiC," *Journal of Applied Physics*, vol. 64, no. 9, pp. 4531–4535, Nov. 1988. doi: 10.1063/1.341281

[42] I. Akasaki, H. Amano, Y. Koide, K. Hiramatsu, and N. Sawaki, "Effects of AlN buffer layer on crystallographic structure and on electrical and optical properties of GaN and $Ga_{1-x}Al_xN$ ($0 < x \leq 0.4$) films grown on sapphire substrate by MOVPE," *Journal of Crystal Growth*, vol. 98, no. 1, pp. 209–219, Nov. 1989. doi: 10.1016/0022-0248(89)90200-5

[43] M. Asif Khan, J. N. Kuznia, D. T. Olson, and R. Kaplan, "Deposition and surface characterization of high quality single crystal GaN layers," *Journal of Applied Physics*, vol. 73, no. 6, pp. 3108–3110, Mar. 1993. doi: 10.1063/1.352999

[44] C. J. Sun, P. Kung, A. Saxler, H. Ohsato, E. Bigan, M. Razeghi, and D. K. Gaskill, "Thermal stability of GaN thin films grown on (0001) Al_2O_3, $(01\bar{1}2)$ Al_2O_3 and $(0001)_{Si}$ 6H-SiC substrates," *Journal of Applied Physics*, vol. 76, no. 1, pp. 236–241, Jul. 1994. doi: 10.1063/1.357133

[45] M. Sumiya, K. Yoshimura, K. Ohtsuka, and S. Fuke, "Dependence of impurity incorporation on the polar direction of GaN film growth," *Appl. Phys. Lett.*, vol. 76, no. 15, pp. 2098–2100, Apr. 2000. doi: 10.1063/1.126267

[46] M. Stutzmann, O. Ambacher, M. Eickhoff, U. Karrer, A. L. Pimenta, R. Neuberger, J. Schalwig, R. Dimitrov, P. J. Schuck, and R. D. Grober, "Playing with Polarity," *physica status solidi (b)*, vol. 228, no. 2, pp. 505–512, 2001. doi: 10.1002/1521-3951(200111)228:2¡505::AID-PSSB505¿3.0.CO;2-U

[47] M. Sumiya and S. Fuke, "Review of polarity determination and control of GaN," *MRS Internet j. nitride semicond. res.*, vol. 9, p. e1, 2004. doi: 10.1557/S1092578300000363

[48] S. Keller, B. P. Keller, Y. Wu, B. Heying, D. Kapolnek, J. S. Speck, U. K. Mishra, and S. P. DenBaars, "Influence of sapphire nitridation on properties of gallium nitride grown by metalorganic chemical vapor deposition," *Appl. Phys. Lett.*, vol. 68, no. 11, pp. 1525–1527, Mar. 1996. doi: 10.1063/1.115687

[49] O. Ambacher, "Growth and applications of Group III-nitrides," *J. Phys. D: Appl. Phys.*, vol. 31, no. 20, pp. 2653–2710, Oct. 1998. doi: 10.1088/0022-3727/31/20/001

[50] A. Aleksov, R. Collazo, S. Mita, R. Schlesser, and Z. Sitar, "Current-voltage characteristics of n/n lateral polarity junctions in GaN," *Appl. Phys. Lett.*, vol. 89, no. 5, p. 052117, Jul. 2006. doi: 10.1063/1.2244046

[51] R. Collazo, S. Mita, A. Rice, R. F. Dalmau, and Z. Sitar, "Simultaneous growth of a GaN p/n lateral polarity junction by polar selective doping," *Appl. Phys. Lett.*, vol. 91, no. 21, p. 212103, Nov. 2007. doi: 10.1063/1.2816893

[52] S. Keller, N. A. Fichtenbaum, F. Wu, D. Brown, A. Rosales, S. P. DenBaars, J. S. Speck, and U. K. Mishra, "Influence of the substrate misorientation on the properties of N-polar GaN films grown by metal organic chemical vapor deposition," *Journal of Applied Physics*, vol. 102, no. 8, p. 083546, Oct. 2007. doi: 10.1063/1.2801406

[53] N. A. Fichtenbaum, T. E. Mates, S. Keller, S. P. DenBaars, and U. K. Mishra, "Impurity incorporation in heteroepitaxial N-face and Ga-face GaN films grown by metalorganic chemical vapor deposition," *Journal of Crystal Growth*, vol. 310, no. 6, pp. 1124–1131, Mar. 2008. doi: 10.1016/j.jcrysgro.2007.12.051

[54] S. R. Xu, Y. Hao, J. C. Zhang, Y. R. Cao, X. W. Zhou, L. A. Yang, X. X. Ou, K. Chen, and W. Mao, "Polar dependence of impurity incorporation and yellow luminescence in GaN films grown by metal-organic chemical vapor deposition," *Journal of Crystal Growth*, vol. 312, no. 23, pp. 3521–3524, Nov. 2010. doi: 10.1016/j.jcrysgro.2010.09.026

[55] S. Keller, H. Li, M. Laurent, Y. Hu, N. Pfaff, J. Lu, D. F. Brown, N. A. Fichtenbaum, J. S. Speck, S. P. DenBaars, and U. K. Mishra, "Recent progress in metal-organic chemical vapor deposition of $(000\bar{1})$ N-polar group-III nitrides," *Semicond. Sci. Technol.*, vol. 29, no. 11, p. 113001, Aug. 2014. doi: 10.1088/0268-1242/29/11/113001

[56] S. N. S. Nakamura, "GaN Growth Using GaN Buffer Layer," *Jpn. J. Appl. Phys.*, vol. 30, no. 10A, p. L1705, Oct. 1991. doi: 10.1143/JJAP.30.L1705

[57] K. Uchida, A. Watanabe, F. Yano, M. Kouguchi, T. Tanaka, and S. Minagawa, "Nitridation process of sapphire substrate surface and its effect on the growth of GaN," *Journal of Applied Physics*, vol. 79, no. 7, pp. 3487–3491, Apr. 1996. doi: 10.1063/1.361398

[58] Mita, Seiji, "Polarity Control in GaN Epilayers Grown by Metalorganic Chemical Vapor Deposition," Ph.D. Dissertation, North Carolina State University, Aug. 2008.

[59] F. Liu, R. Collazo, S. Mita, Z. Sitar, G. Duscher, and S. J. Pennycook, "The mechanism for polarity inversion of GaN via a thin AlN layer: Direct experimental evidence," *Appl. Phys. Lett.*, vol. 91, no. 20, p. 203115, Nov. 2007. doi: 10.1063/1.2815748

[60] R. Collazo, S. Mita, J. Xie, A. Rice, J. Tweedie, R. Dalmau, and Z. Sitar, "Implementation of the GaN lateral polarity junction in a MESFET utilizing polar doping selectivity," *physica status solidi (a)*, vol. 207, no. 1, pp. 45–48, 2010. doi: 10.1002/pssa.200982629

[61] S. Mita, R. Collazo, and Z. Sitar, "Fabrication of a GaN lateral polarity junction by metalorganic chemical vapor deposition," *Journal of Crystal Growth*, vol. 311, no. 10, pp. 3044–3048, May 2009. doi: 10.1016/j.jcrysgro.2009.01.075

[62] M.-D. Park, J.-W. Min, J.-Y. Lee, J.-H. Park, S.-Y. Choi, and D.-S. Lee, "Single-crystal GaN growth and polarity control using an E-beam evaporated aluminum layer," *Opt. Mater. Express, OME*, vol. 11, no. 4, pp. 955–964, Apr. 2021. doi: 10.1364/OME.419734

[63] H. Matsumura, Y. Kanematsu, T. Shimura, T. Tamaki, Y. Ozeki, K. Itoh, M. Sumiya, T. Nakano, and S. Fuke, "Lateral Polarity Control in GaN Based on Selective Growth Procedure Using Carbon Mask Layers," *Appl. Phys. Express*, vol. 2, no. 10, p. 101001, Oct. 2009. doi: 10.1143/APEX.2.101001

[64] H. Yagi, N. Osumi, Y. Inoue, and T. Nakano, "Double-Polarity Selective-Area Growth of GaN by Metal-Organic Vapor-Phase Epitaxy Using Narrow-Pitch Patterns," *physica status solidi (b)*, vol. 255, no. 5, p. 1700475, 2018. doi: 10.1002/pssb.201700475

[65] J. Hite, M. Twigg, M. Mastro, J. Freitas, J. Meyer, I. Vurgaftman, S. O'Connor, N. Condon, F. Kub, S. Bowman, and C. Eddy, "Development of periodically oriented gallium nitride for non-linear optics [Invited]," *Opt. Mater. Express, OME*, vol. 2, no. 9, pp. 1203–1208, Sep. 2012. doi: 10.1364/OME.2.001203

[66] J. K. Hite, N. Y. Garces, R. Goswami, M. A. Mastro, F. J. Kub, and C. R. Eddy, "Selective switching of GaN polarity on Ga-polar GaN using atomic layer deposited Al $_2$ O $_3$," *Appl. Phys. Express*, vol. 7, no. 2, p. 025502, Feb. 2014. doi: 10.7567/APEX.7.025502

[67] T. K. Zywietz, J. Neugebauer, and M. Scheffler, "The adsorption of oxygen at GaN surfaces," *Appl. Phys. Lett.*, vol. 74, no. 12, pp. 1695–1697, Mar. 1999. doi: 10.1063/1.123658

[68] E. Frayssinet, W. Knap, P. Prystawko, M. Leszczynski, I. Grzegory, T. Suski, B. Beaumont, and P. Gibart, "Infrared studies on GaN single crystals and homoepitaxial layers," *Journal of Crystal Growth*, vol. 218, no. 2, pp. 161–166, Sep. 2000. doi: 10.1016/S0022-0248(00)00537-6

[69] M. Sheikhi, J. Li, F. Meng, H. Li, S. Guo, L. Liang, H. Cao, P. Gao, J. Ye, and W. Guo, "Polarity Control of GaN and Realization of GaN Schottky Barrier Diode Based on Lateral Polarity Structure," *IEEE Transactions on Electron Devices*, vol. 64, no. 11, pp. 4424–4429, Nov. 2017. doi: 10.1109/TED.2017.2750710

[70] S. Mukhopadhyay, H. Pal, S. R. Narang, C. Guo, J. Ye, W. Guo, and B. Sarkar, "Self-powered ultraviolet photodiode based on lateral polarity structure GaN films," *Journal of Vacuum Science & Technology B*, vol. 39, no. 5, p. 052206, Sep. 2021. doi: 10.1116/6.0001196

[71] W. Guo, H. Xu, L. Chen, H. Yu, J. Jiang, M. Sheikhi, L. Li, Y. Dai, M. Cui, H. Sun, and J. Ye, "Polarity control and fabrication of lateral polarity structures of III-nitride thin films and devices: progress and prospects," *J. Phys. D: Appl. Phys.*, vol. 53, no. 48, p. 483002, Nov. 2020. doi: 10.1088/1361-6463/abaf7b

[72] J. K. Hite, N. D. Bassim, M. E. Twigg, M. A. Mastro, F. J. Kub, and C. R. Eddy, "GaN vertical and lateral polarity heterostructures on GaN substrates," *Journal of Crystal Growth*, vol. 332, no. 1, pp. 43–47, Oct. 2011. doi: 10.1016/j.jcrysgro.2011.08.002

[73] J. A. Van Vechten, "Quantum Dielectric Theory of Electronegativity in Covalent Systems. III. Pressure-Temperature Phase Diagrams, Heats of Mixing, and Distribution Coefficients," *Phys. Rev. B*, vol. 7, no. 4, pp. 1479–1507, Feb. 1973. doi: 10.1103/PhysRevB.7.1479

[74] H. W. Choi, M. A. Rana, S. J. Chua, T. Osipowicz, and J. S. Pan, "Surface analysis of GaN decomposition," *Semicond. Sci. Technol.*, vol. 17, no. 12, pp. 1223–1225, Dec. 2002. doi: 10.1088/0268-1242/17/12/304

[75] T. J. Anderson, B. N. Feigelson, F. J. Kub, M. J. Tadjer, K. D. Hobart, M. A. Mastro, J. K. Hite, and C. R. Eddy, "Activation of Mg implanted in GaN by multicycle rapid thermal annealing," *Electronics Letters*, vol. 50, no. 3, pp. 197–198, 2014. doi: 10.1049/el.2013.3214

[76] M. J. Tadjer, B. N. Feigelson, J. D. Greenlee, J. A. Freitas, T. J. Anderson, J. K. Hite, L. Ruppalt, C. R. Eddy, K. D. Hobart, and F. J. Kub, "Selective p-type Doping of GaN:Si by Mg Ion Implantation and Multicycle Rapid Thermal Annealing," *ECS J. Solid State Sci. Technol.*, vol. 5, no. 2, pp. P124–P127, 2016. doi: 10.1149/2.0371602jss

[77] V. Meyers, E. Rocco, T. J. Anderson, J. C. Gallagher, M. A. Ebrish, K. Jones, M. Derenge, M. Shevelev, V. Sklyar, K. Hogan, B. McEwen, and F. Shahedipour-Sandvik, "p-type conductivity and damage recovery in implanted GaN annealed by rapid gyrotron microwave annealing," *Journal of Applied Physics*, vol. 128, no. 8, p. 085701, Aug. 2020. doi: 10.1063/5.0016358

[78] A. G. Jacobs, B. N. Feigelson, J. K. Hite, C. A. Gorsak, L. E. Luna, T. J. Anderson, and F. J. Kub, "Role of Capping Material and GaN Polarity on Mg Ion Implantation Activation," *physica status solidi (a)*, vol. 217, no. 7, p. 1900789, 2020. doi: 10.1002/pssa.201900789

[79] Y. Zhang, Z. Liu, M. J. Tadjer, M. Sun, D. Piedra, C. Hatem, T. J. Anderson, L. E. Luna, A. Nath, A. D. Koehler, H. Okumura, J. Hu, X. Zhang, X. Gao, B. N. Feigelson, K. D. Hobart, and T. Palacios, "Vertical GaN Junction Barrier Schottky Rectifiers by Selective Ion Implantation," *IEEE Electron Device Letters*, vol. 38, no. 8, pp. 1097–1100, Aug. 2017. doi: 10.1109/LED.2017.2720689

[80] A. D. Koehler, T. J. Anderson, M. J. Tadjer, A. Nath, B. N. Feigelson, D. I. Shahin, K. D. Hobart, and F. J. Kub, "Vertical GaN Junction Barrier Schottky Diodes," *ECS J. Solid State Sci. Technol.*, vol. 6, no. 1, pp. Q10–Q12, 2017. doi: 10.1149/2.0041701jss

[81] E. Landi, A. Armigliato, S. Solmi, R. Kögler, and E. Wieser, "Electrical activation of boron-implanted silicon during rapid thermal annealing," *Appl. Phys. A*, vol. 47, no. 4, pp. 359–366, Dec. 1988. doi: 10.1007/BF00615499

[82] T. Kimoto, K. Kawahara, N. Kaji, H. Fujihara, and J. Suda, "Ion implantation technology in SiC for high-voltage/high-temperature devices," in *2016 16th International Workshop on Junction Technology (IWJT)*, May 2016, pp. 54–58. doi: 10.1109/IWJT.2016.7486673

[83] S. Porowski, I. Grzegory, D. Kolesnikov, W. Lojkowski, V. Jager, W. Jager, V. Bogdanov, T. Suski, and S. Krukowski, "Annealing of GaN under high pressure of nitrogen," *J. Phys.: Condens. Matter*, vol. 14, no. 44, pp. 11 097–11 110, Nov. 2002. doi: 10.1088/0953-8984/14/44/433

[84] H. Sakurai, M. Omori, S. Yamada, Y. Furukawa, H. Suzuki, T. Narita, K. Kataoka, M. Horita, M. Bockowski, J. Suda, and T. Kachi, "Highly effective activation of Mg-implanted p-type GaN by ultra-high-pressure annealing," *Appl. Phys. Lett.*, vol. 115, no. 14, p. 142104, Sep. 2019. doi: 10.1063/1.5116866

[85] K. Hirukawa, K. Sumida, H. Sakurai, H. Fujikura, M. Horita, Y. Otoki, K. Sierakowski, M. Bockowski, T. Kachi, and J. Suda, "Isochronal annealing study of Mg-implanted p-type GaN activated by ultra-high-pressure annealing," *Appl. Phys. Express*, vol. 14, no. 5, p. 056501, Apr. 2021. doi: 10.35848/1882-0786/abf4f3

[86] K. Sierakowski, R. Jakiela, B. Lucznik, P. Kwiatkowski, M. Iwinska, M. Turek, H. Sakurai, T. Kachi, and M. Bockowski, "High Pressure Processing of Ion Implanted GaN," *Electronics*, vol. 9, no. 9, p. 1380, Sep. 2020. doi: 10.3390/electronics9091380

[87] M. H. Breckenridge, J. Tweedie, P. Reddy, Y. Guan, P. Bagheri, D. Szymanski, S. Mita, K. Sierakowski, M. Boćkowski, R. Collazo, and Z. Sitar, "High Mg activation in implanted GaN by high temperature and ultrahigh pressure annealing," *Appl. Phys. Lett.*, vol. 118, no. 2, p. 022101, Jan. 2021. doi: 10.1063/5.0038628

[88] M. Matys, T. Ishida, K. P. Nam, H. Sakurai, T. Narita, T. Uesugi, M. Bockowski, J. Suda, and T. Kachi, "Mg-implanted bevel edge termination structure for GaN power device applications," *Appl. Phys. Lett.*, vol. 118, no. 9, p. 093502, Mar. 2021. doi: 10.1063/5.0039183

[89] M. Matys, T. Ishida, K. P. Nam, H. Sakurai, K. Kataoka, T. Narita, T. Uesugi, M. Bockowski, T. Nishimura, J. Suda, and T. Kachi, "Design and demonstration of

nearly-ideal edge termination for GaN p–n junction using Mg-implanted field limiting rings," *Appl. Phys. Express*, vol. 14, no. 7, p. 074002, Jun. 2021. doi: 10.35848/1882-0786/ac0b09

[90] A. Strollo and E. Napoli, "Optimal ON-resistance versus breakdown voltage tradeoff in superjunction power devices: a novel analytical model," *IEEE Transactions on Electron Devices*, vol. 48, no. 9, pp. 2161–2167, Sep. 2001. doi: 10.1109/16.944211

[91] L. Yu and K. Sheng, "Modeling and Optimal Device Design for 4H-SiC Super-Junction Devices," *IEEE Transactions on Electron Devices*, vol. 55, no. 8, pp. 1961–1969, Aug. 2008. doi: 10.1109/TED.2008.926648

[92] Z. Li and T. P. Chow, "Design and Simulation of 5–20-kV GaN Enhancement-Mode Vertical Superjunction HEMT," *IEEE Transactions on Electron Devices*, vol. 60, no. 10, pp. 3230–3237, Oct. 2013. doi: 10.1109/TED.2013.2266544

[93] B. Song, M. Zhu, Z. Hu, K. Nomoto, D. Jena, and H. G. Xing, "Design and optimization of GaN lateral polarization-doped super-junction (LPSJ): An analytical study," in *2015 IEEE 27th International Symposium on Power Semiconductor Devices IC's (ISPSD)*, May 2015, pp. 273–276. doi: 10.1109/ISPSD.2015.7123442

[94] D. Khachariya, D. Szymanski, P. Reddy, E. Kohn, Z. Sitar, R. Collazo, and S. Pavlidis, "(Invited) A Path Toward Vertical GaN Superjunction Devices," *ECS Trans.*, vol. 98, no. 6, p. 69, Sep. 2020. doi: 10.1149/09806.0069ecst

[95] A. G. Chynoweth, "Ionization Rates for Electrons and Holes in Silicon," *Phys. Rev.*, vol. 109, no. 5, pp. 1537–1540, Mar. 1958. doi: 10.1103/PhysRev.109.1537

[96] K. Kunihiro, K. Kasahara, Y. Takahashi, and Y. Ohno, "Experimental evaluation of impact ionization coefficients in GaN," *IEEE Electron Device Letters*, vol. 20, no. 12, pp. 608–610, Dec. 1999. doi: 10.1109/55.806100

[97] B. J. Baliga, "Gallium nitride devices for power electronic applications," *Semicond. Sci. Technol.*, vol. 28, no. 7, p. 074011, Jun. 2013. doi: 10.1088/0268-1242/28/7/074011

[98] Z. Li, V. Pala, and T. P. Chow, "Avalanche Breakdown Design Parameters in GaN," *Jpn. J. Appl. Phys.*, vol. 52, no. 8S, p. 08JN05, May 2013. doi: 10.7567/JJAP.52.08JN05

[99] L. Cao, J. Wang, G. Harden, H. Ye, R. Stillwell, A. J. Hoffman, and P. Fay, "Experimental characterization of impact ionization coefficients for electrons and holes in GaN grown on bulk GaN substrates," *Appl. Phys. Lett.*, vol. 112, no. 26, p. 262103, Jun. 2018. doi: 10.1063/1.5031785

[100] D. Ji, B. Ercan, and S. Chowdhury, "Experimental determination of impact ionization coefficients of electrons and holes in gallium nitride using homojunction structures," *Appl. Phys. Lett.*, vol. 115, no. 7, p. 073503, Aug. 2019. doi: 10.1063/1.5099245

[101] T. Maeda, T. Narita, S. Yamada, T. Kachi, T. Kimoto, M. Horita, and J. Suda, "Impact ionization coefficients and critical electric field in GaN," *Journal of Applied Physics*, vol. 129, no. 18, p. 185702, May 2021. doi: 10.1063/5.0050793

[102] A. M. Ozbek, "Measurement of Impact Ionization Coefficients in Gallium Nitride," PhD Thesis, North Carolina State University, Raleigh, NC, USA, 2012.

[103] W. Fulop, "Calculation of avalanche breakdown voltages of silicon p-n junctions," *Solid-State Electronics*, vol. 10, no. 1, pp. 39–43, Jan. 1967. doi: 10.1016/0038-1101(67)90111-6

[104] C.-H. Chang, Y. Zhao, R. K. Heilmann, and M. L. Schattenburg, "Fabrication of 50 nm period gratings with multilevel interference lithography," *Opt. Lett., OL*, vol. 33, no. 14, pp. 1572–1574, Jul. 2008. doi: 10.1364/OL.33.001572

[105] M. Ellman, A. Rodríguez, N. Pérez, M. Echeverria, Y. K. Verevkin, C. S. Peng, T. Berthou, Z. Wang, S. M. Olaizola, and I. Ayerdi, "High-power laser interference lithography process on photoresist: Effect of laser fluence and polarisation," *Applied Surface Science*, vol. 255, no. 10, pp. 5537–5541, Mar. 2009. doi: 10.1016/j.apsusc.2008.07.201

[106] C. Lu and R. H. Lipson, "Interference lithography: a powerful tool for fabricating periodic structures," *Laser & Photonics Reviews*, vol. 4, no. 4, pp. 568–580, 2010. doi: 10.1002/lpor.200810061

[107] H. van Wolferen and L. Abelmann, "LASER INTERFERENCE LITHOGRAPHY," p. 16.

[108] X. Zhou, J. R. Howell-Clark, Z. Guo, C. W. Hitchcock, and T. P. Chow, "Performance limits of vertical GaN of conventional doped pn and natural polarization superjunction devices," *Appl. Phys. Lett.*, vol. 115, no. 11, p. 112104, Sep. 2019. doi: 10.1063/1.5109389

[109] E. Napoli and A. Strollo, "Design consideration of 1000 V merged PiN Schottky diode using superjunction sustaining layer," in *Proceedings of the 13th International Symposium on Power Semiconductor Devices ICs. IPSD '01 (IEEE Cat. No.01CH37216)*, Jun. 2001, pp. 339–342. doi: 10.1109/ISPSD.2001.934624

[110] E. Napoli, H. Wang, and F. Udrea, "The Effect of Charge Imbalance on Superjunction Power Devices: An Exact Analytical Solution," *IEEE Electron Device Letters*, vol. 29, no. 3, pp. 249–251, Mar. 2008. doi: 10.1109/LED.2007.915375

[111] J. L. Rouvière, M. Arlery, R. Niebuhr, K. H. Bachem, and O. Briot, "Transmission electron microscopy characterization of GaN layers grown by MOCVD on sapphire," *Materials Science and Engineering: B*, vol. 43, no. 1, pp. 161–166, Jan. 1997. doi: 10.1016/S0921-5107(96)01855-7

[112] S. Rajan, A. Chini, M. H. Wong, J. S. Speck, and U. K. Mishra, "N-polar GaN/AlGaN/GaN high electron mobility transistors," *Journal of Applied Physics*, vol. 102, no. 4, p. 044501, Aug. 2007. doi: 10.1063/1.2769950

[113] M. H. Wong, Y. Pei, T. Palacios, L. Shen, A. Chakraborty, L. S. McCarthy, S. Keller, S. P. DenBaars, J. S. Speck, and U. K. Mishra, "Low nonalloyed Ohmic contact resistance to nitride high electron mobility transistors using N-face growth," *Appl. Phys. Lett.*, vol. 91, no. 23, p. 232103, Dec. 2007. doi: 10.1063/1.2820381

[114] C. R. English, V. D. Wheeler, N. Y. Garces, N. Nepal, A. Nath, J. K. Hite, M. A. Mastro, and C. R. Eddy, "Impact of surface treatments on high-κ dielectric integration with Ga-polar and N-polar GaN," *Journal of Vacuum Science & Technology B*, vol. 32, no. 3, p. 03D106, May 2014. doi: 10.1116/1.4831875

[115] D. Wei, T. Hossain, D. P. Briggs, and J. H. Edgar, "A Comparison of N-Polar $(000\bar{1})$ GaN Surface Preparations for the Atomic Layer Deposition of Al_2O_3," *ECS J. Solid State Sci. Technol.*, vol. 3, no. 10, p. N127, Aug. 2014. doi: 10.1149/2.0201410jss

[116] D. Khachariya, D. Szymanski, R. Sengupta, P. Reddy, E. Kohn, Z. Sitar, R. Collazo, and S. Pavlidis, "Chemical treatment effects on Schottky contacts to metalorganic chemical vapor deposited n-type N-polar GaN," *Journal of Applied Physics*, vol. 128, no. 6, p. 064501, Aug. 2020. doi: 10.1063/5.0015140

[117] P. Hacke, T. Detchprohm, K. Hiramatsu, and N. Sawaki, "Schottky barrier on n-type GaN grown by hydride vapor phase epitaxy," *Appl. Phys. Lett.*, vol. 63, no. 19, pp. 2676–2678, Nov. 1993. doi: 10.1063/1.110417

[118] L. Wang, M. I. Nathan, T. Lim, M. A. Khan, and Q. Chen, "High barrier height GaN Schottky diodes: Pt/GaN and Pd/GaN," *Appl. Phys. Lett.*, vol. 68, no. 9, pp. 1267–1269, Feb. 1996. doi: 10.1063/1.115948

[119] U. Karrer, O. Ambacher, and M. Stutzmann, "Influence of crystal polarity on the properties of Pt/GaN Schottky diodes," *Appl. Phys. Lett.*, vol. 77, no. 13, pp. 2012–2014, Sep. 2000. doi: 10.1063/1.1313275

[120] F. Iucolano, F. Roccaforte, F. Giannazzo, and V. Raineri, "Barrier inhomogeneity and electrical properties of Pt/GaN Schottky contacts," *Journal of Applied Physics*, vol. 102, no. 11, p. 113701, Dec. 2007. doi: 10.1063/1.2817647

[121] P. K. Rao, B. Park, S.-T. Lee, Y.-K. Noh, M.-D. Kim, and J.-E. Oh, "Analysis of leakage current mechanisms in Pt/Au Schottky contact on Ga-polarity GaN by Frenkel-Poole emission and deep level studies," *Journal of Applied Physics*, vol. 110, no. 1, p. 013716, Jul. 2011. doi: 10.1063/1.3607245

[122] J. D. Guo, F. M. Pan, M. S. Feng, R. J. Guo, P. F. Chou, and C. Y. Chang, "Schottky contact and the thermal stability of Ni on n-type GaN," *Journal of Applied Physics*, vol. 80, no. 3, pp. 1623–1627, Aug. 1996. doi: 10.1063/1.363822

[123] L. S. Yu, Q. Z. Liu, Q. J. Xing, D. J. Qiao, S. S. Lau, and J. Redwing, "The role of the tunneling component in the current–voltage characteristics of metal-GaN Schottky diodes," *Journal of Applied Physics*, vol. 84, no. 4, pp. 2099–2104, Aug. 1998. doi: 10.1063/1.368270

[124] A. R. Arehart, B. Moran, J. S. Speck, U. K. Mishra, S. P. DenBaars, and S. A. Ringel, "Effect of threading dislocation density on Ni/n-GaN Schottky diode I-V characteristics," *Journal of Applied Physics*, vol. 100, no. 2, p. 023709, Jul. 2006. doi: 10.1063/1.2219985

[125] P. Reddy, B. Sarkar, F. Kaess, M. Gerhold, E. Kohn, R. Collazo, and Z. Sitar, "Defect-free Ni/GaN Schottky barrier behavior with high temperature stability," *Appl. Phys. Lett.*, vol. 110, no. 1, p. 011603, Jan. 2017. doi: 10.1063/1.4973762

[126] E. H. Rhoderick and R. H. Williams, *Metal-semiconductor contacts*. Oxford [England]; New York: Clarendon Press ; Oxford University Press, 1988.

[127] W.-C. Yang, B. J. Rodriguez, M. Park, R. J. Nemanich, O. Ambacher, and V. Cimalla, "Photoelectron emission microscopy observation of inversion domain boundaries of GaN-based lateral polarity heterostructures," *Journal of Applied Physics*, vol. 94, no. 9, pp. 5720–5725, Nov. 2003. doi: 10.1063/1.1618355

[128] H. Kim, S.-N. Lee, Y. Park, J. S. Kwak, and T.-Y. Seong, "Metallization contacts to nonpolar a-plane n-type GaN," *Appl. Phys. Lett.*, vol. 93, no. 3, p. 032105, Jul. 2008. doi: 10.1063/1.2963492

[129] H. W. Jang, J.-H. Lee, and J.-L. Lee, "Characterization of band bendings on Ga-face and N-face GaN films grown by metalorganic chemical-vapor deposition," *Appl. Phys. Lett.*, vol. 80, no. 21, pp. 3955–3957, May 2002. doi: 10.1063/1.1481782

[130] P. Reddy, I. Bryan, Z. Bryan, W. Guo, L. Hussey, R. Collazo, and Z. Sitar, "The effect of polarity and surface states on the Fermi level at III-nitride surfaces," *Journal of Applied Physics*, vol. 116, no. 12, p. 123701, Sep. 2014. doi: 10.1063/1.4896377

[131] A. Rizzi and H. Lüth, "Comment on "Influence of crystal polarity on the properties of Pt/GaN Schottky diodes" [Appl. Phys. Lett. 77, 2012 (2000)]," *Appl. Phys. Lett.*, vol. 80, no. 3, pp. 530–531, Jan. 2002. doi: 10.1063/1.1435067

[132] Z.-Q. Fang, D. C. Look, P. Visconti, D.-F. Wang, C.-Z. Lu, F. Yun, H. Morkoç, S. S. Park, and K. Y. Lee, "Deep centers in a free-standing GaN layer," *Appl. Phys. Lett.*, vol. 78, no. 15, pp. 2178–2180, Apr. 2001. doi: 10.1063/1.1361273

[133] J. Osvald, J. Kuzmik, G. Konstantinidis, P. Lobotka, and A. Georgakilas, "Temperature dependence of GaN Schottky diodes I–V characteristics," *Microelectronic Engineering*, vol. 81, no. 2, pp. 181–187, Aug. 2005. doi: 10.1016/j.mee.2005.03.004

[134] B. P. Downey, D. J. Meyer, D. S. Katzer, D. F. Storm, and S. C. Binari, "Electrical characterization of Schottky contacts to N-polar GaN," *Solid-State Electronics*, vol. 86, pp. 17–21, Aug. 2013. doi: 10.1016/j.sse.2013.04.002

[135] P. Reddy, D. Khachariya, D. Szymanski, M. H. Breckenridge, B. Sarkar, S. Pavlidis, R. Collazo, Z. Sitar, and E. Kohn, "Role of polarity in SiN on Al/GaN and the pathway to stable contacts," *Semicond. Sci. Technol.*, vol. 35, no. 5, p. 055007, Mar. 2020. doi: 10.1088/1361-6641/ab7775

[136] Q. Z. Liu and S. S. Lau, "A review of the metal–GaN contact technology," *Solid-State Electronics*, vol. 42, no. 5, pp. 677–691, May 1998. doi: 10.1016/S0038-1101(98)00099-9

[137] C. Huh, S.-W. Kim, H.-S. Kim, I.-H. Lee, and S.-J. Park, "Effective sulfur passivation of an n-type GaN surface by an alcohol-based sulfide solution," *Journal of Applied Physics*, vol. 87, no. 9, pp. 4591–4593, May 2000. doi: 10.1063/1.373107

[138] O. Ambacher, J. Smart, J. R. Shealy, N. G. Weimann, K. Chu, M. Murphy, W. J. Schaff, L. F. Eastman, R. Dimitrov, L. Wittmer, M. Stutzmann, W. Rieger, and J. Hilsenbeck, "Two-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in N- and Ga-face AlGaN/GaN heterostructures," *Journal of Applied Physics*, vol. 85, no. 6, pp. 3222–3233, Mar. 1999. doi: 10.1063/1.369664

[139] H. Kim, J.-H. Ryou, R. D. Dupuis, S.-N. Lee, Y. Park, J.-W. Jeon, and T.-Y. Seong, "Electrical characteristics of contacts to thin film N-polar n-type GaN," *Appl. Phys. Lett.*, vol. 93, no. 19, p. 192106, Nov. 2008. doi: 10.1063/1.3013838

[140] J.-Y. Duboz, F. Binet, N. Laurent, E. Rosencher, F. Scholz, V. Harle, O. Briot, B. Gil, and R. L. Aulombard, "Influence of Surface Defects on the Characteristics of GaN Schottky Diodes," *MRS Online Proceedings Library (OPL)*, vol. 449, 1996. doi: 10.1557/PROC-449-1085

[141] R. Kirste, R. Collazo, G. Callsen, M. R. Wagner, T. Kure, J. Sebastian Reparaz, S. Mita, J. Xie, A. Rice, J. Tweedie, Z. Sitar, and A. Hoffmann, "Temperature dependent photoluminescence of lateral polarity junctions of metal organic chemical vapor deposition grown GaN," *Journal of Applied Physics*, vol. 110, no. 9, p. 093503, Nov. 2011. doi: 10.1063/1.3656987

[142] L. L. Smith, S. W. King, R. J. Nemanich, and R. F. Davis, "Cleaning of GaN surfaces," *JEM*, vol. 25, no. 5, pp. 805–810, May 1996. doi: 10.1007/BF02666640

[143] R. France, T. Xu, P. Chen, R. Chandrasekaran, and T. D. Moustakas, "Vanadium-based Ohmic contacts to n-AlGaN in the entire alloy composition," *Appl. Phys. Lett.*, vol. 90, no. 6, p. 062115, Feb. 2007. doi: 10.1063/1.2458399

[144] B. B. Haidet, B. Sarkar, P. Reddy, I. Bryan, Z. Bryan, R. Kirste, R. Collazo, and Z. Sitar, "Nonlinear analysis of vanadium- and titanium-based contacts to Al-rich n-AlGaN," *Jpn. J. Appl. Phys.*, vol. 56, no. 10, p. 100302, Sep. 2017. doi: 10.7567/JJAP.56.100302

[145] D. Briggs and M. P. Seah, *Practical Surface Analysis by Auger and X-ray Photoelectron Spectroscopy*. Wiley, 1983.

[146] D. K. Schroder, *Semiconductor material and device characterization*, 3rd ed. John Wiley & Sons, 2006.

[147] H. S. Craft, A. L. Rice, R. Collazo, Z. Sitar, and J.-P. Maria, "Spectroscopic measurements of the surface stoichiometry of chemical vapor deposited GaN," *Appl. Phys. Lett.*, vol. 98, no. 8, p. 082110, Feb. 2011. doi: 10.1063/1.3554762

[148] P. Reddy and J. Kumar, "Modified approach to modeling barrier inhomogeneity in Schottky diodes," *Semicond. Sci. Technol.*, vol. 34, no. 3, p. 035004, Jan. 2019. doi: 10.1088/1361-6641/aafcc2

[149] J. H. Werner and H. H. Güttler, "Barrier inhomogeneities at Schottky contacts," *Journal of Applied Physics*, vol. 69, no. 3, pp. 1522–1533, Feb. 1991. doi: 10.1063/1.347243

[150] R. T. Tung, "Electron transport of inhomogeneous Schottky barriers," *Appl. Phys. Lett.*, vol. 58, no. 24, pp. 2821–2823, Jun. 1991. doi: 10.1063/1.104747

[151] V. Saxena, J. N. Su, and A. Steckl, "High-voltage Ni- and Pt-SiC Schottky diodes utilizing metal field plate termination," *IEEE Transactions on Electron Devices*, vol. 46, no. 3, pp. 456–464, Mar. 1999. doi: 10.1109/16.748862

[152] J. R. Shealy, T. R. Prunty, E. M. Chumbes, and B. K. Ridley, "Growth and passivation of AlGaN/GaN heterostructures," *Journal of Crystal Growth*, vol. 250, no. 1, pp. 7–13, Mar. 2003. doi: 10.1016/S0022-0248(02)02187-5

[153] P. Reddy, S. Washiyama, F. Kaess, M. Hayden Breckenridge, L. H. Hernandez-Balderrama, B. B. Haidet, D. Alden, A. Franke, B. Sarkar, E. Kohn, R. Collazo, and Z. Sitar, "High temperature and low pressure chemical vapor deposition of silicon nitride on AlGaN: Band offsets and passivation studies," *Journal of Applied Physics*, vol. 119, no. 14, p. 145702, Apr. 2016. doi: 10.1063/1.4945775

[154] D. Khachariya, D. Szymanski, M. H. Breckenridge, P. Reddy, E. Kohn, Z. Sitar, R. Collazo, and S. Pavlidis, "On the characteristics of N-polar GaN Schottky barrier contacts with LPCVD SiN interlayers," *Appl. Phys. Lett.*, vol. 118, no. 12, p. 122103, Mar. 2021. doi: 10.1063/5.0039888

[155] H. F. Sterling and R. C. G. Swann, "Chemical vapour deposition promoted by r.f. discharge," *Solid-State Electronics*, vol. 8, no. 8, pp. 653–654, Aug. 1965. doi: 10.1016/0038-1101(65)90033-X

[156] K. E. Bean, P. S. Gleim, R. L. Yeakley, and W. R. Runyan, "Some Properties of Vapor Deposited Silicon Nitride Films Using the SiH_4 - NH_3 - H_2 System," *J. Electrochem. Soc.*, vol. 114, no. 7, p. 733, Jul. 1967. doi: 10.1149/1.2426719

[157] R. Riedel and M. Seher, "Crystallization behaviour of amorphous silicon nitride," *Journal of the European Ceramic Society*, vol. 7, no. 1, pp. 21–25, Jan. 1991. doi: 10.1016/0955-2219(91)90049-6

[158] H. Maes and R. Van Overstraeten, "Charge storage in the nitride layer of MNOS structures," in *1974 International Electron Devices Meeting (IEDM)*, Dec. 1974, pp. 119–122. doi: 10.1109/IEDM.1974.6219628

[159] E. Vianello, F. Driussi, L. Perniola, G. Molas, J.-P. Colonna, B. De Salvo, and L. Selmi, "Explanation of the Charge-Trapping Properties of Silicon Nitride Storage Layers for NVM Devices Part I: Experimental Evidences From Physical and Electrical Characterizations," *IEEE Transactions on Electron Devices*, vol. 58, no. 8, pp. 2483–2489, Aug. 2011. doi: 10.1109/TED.2011.2140116

[160] V. A. Gritsenko, S. S. Nekrashevich, V. V. Vasilev, and A. V. Shaposhnikov, "Electronic structure of memory traps in silicon nitride," *Microelectronic Engineering*, vol. 86, no. 7, pp. 1866–1869, Jul. 2009. doi: 10.1016/j.mee.2009.03.093

[161] E. Vianello, L. Perniola, P. Blaise, G. Molas, J. P. Colonna, F. Driussi, P. Palestri, D. Esseni, L. Selmi, N. Rochat, C. Licitra, D. Lafond, R. Kies, G. Reimbold, B. De Salvo, and F. Boulanger, "New insight on the charge trapping mechanisms of SiN-based memory by atomistic simulations and electrical modeling," in *2009 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2009, pp. 1–4. doi: 10.1109/IEDM.2009.5424414

[162] E. Vianello, F. Driussi, P. Blaise, P. Palestri, D. Esseni, L. Perniola, G. Molas, B. De Salvo, and L. Selmi, "Explanation of the Charge Trapping Properties of Silicon Nitride Storage Layers for NVMs—Part II: Atomistic and Electrical Modeling," *IEEE Transactions on Electron Devices*, vol. 58, no. 8, pp. 2490–2499, Aug. 2011. doi: 10.1109/TED.2011.2156407

[163] M.-E. Grillo, S. D. Elliott, and C. Freysoldt, "Native defects in hexagonal β-Si_3N_4 studied using density functional theory calculations," *Phys. Rev. B*, vol. 83, no. 8, p. 085208, Feb. 2011. doi: 10.1103/PhysRevB.83.085208

[164] C. M. Foster, R. Collazo, Z. Sitar, and A. Ivanisevic, "Aqueous Stability of Ga- and N-Polar Gallium Nitride," *Langmuir*, vol. 29, no. 1, pp. 216–220, Jan. 2013. doi: 10.1021/la304039n

[165] W. Guo, J. Xie, C. Akouala, S. Mita, A. Rice, J. Tweedie, I. Bryan, R. Collazo, and Z. Sitar, "Comparative study of etching high crystalline quality AlN and GaN," *Journal of Crystal Growth*, vol. 366, pp. 20–25, Mar. 2013. doi: 10.1016/j.jcrysgro.2012.12.141

[166] X. Wang, X. Zhang, H. Zhang, J. Zhao, Z. Wu, Q. Dai, S. Wang, G. Hu, and Y. Cui, "Influence of nitridation process on characteristics of N-polar AlGaN films grown by MOCVD," *Materials Science in Semiconductor Processing*, vol. 64, pp. 147–151, Jun. 2017. doi: 10.1016/j.mssp.2017.03.025

[167] J. Xie, S. Mita, R. Collazo, A. Rice, J. Tweedie, and Z. Sitar, "The effect of N-polar GaN domains as Ohmic contacts," *Appl. Phys. Lett.*, vol. 97, no. 12, p. 123502, Sep. 2010. doi: 10.1063/1.3491173

[168] M. Foussekis, J. D. Ferguson, J. D. McNamara, A. A. Baski, and M. A. Reshchikov, "Effects of polarity and surface treatment on Ga- and N-polar bulk GaN," *Journal of Vacuum Science & Technology B*, vol. 30, no. 5, p. 051210, Sep. 2012. doi: 10.1116/1.4751276

[169] W. a. P. Claassen, W. G. J. N. Valkenburg, M. F. C. Willemsen, and W. M. v. d. Wijgert, "Influence of Deposition Temperature, Gas Pressure, Gas Phase Composition, and RF Frequency on Composition and Mechanical Stress of Plasma Silicon Nitride Layers," *J. Electrochem. Soc.*, vol. 132, no. 4, p. 893, Apr. 1985. doi: 10.1149/1.2113980

[170] J. P. Ibbetson, P. T. Fini, K. D. Ness, S. P. DenBaars, J. S. Speck, and U. K. Mishra, "Polarization effects, surface states, and the source of electrons in AlGaN/GaN heterostructure field effect transistors," *Appl. Phys. Lett.*, vol. 77, no. 2, pp. 250–252, Jul. 2000. doi: 10.1063/1.126940

[171] U. Mishra, P. Parikh, and Y.-F. Wu, "AlGaN/GaN HEMTs-an overview of device operation and applications," *Proceedings of the IEEE*, vol. 90, no. 6, pp. 1022–1031, Jun. 2002. doi: 10.1109/JPROC.2002.1021567

[172] B. Green, K. Chu, E. Chumbes, J. Smart, J. Shealy, and L. Eastman, "The effect of surface passivation on the microwave characteristics of undoped AlGaN/GaN HEMTs," *IEEE Electron Device Letters*, vol. 21, no. 6, pp. 268–270, Jun. 2000. doi: 10.1109/55.843146

[173] R. Shekhar and K. F. Jensen, "Temperature programmed desorption investigations of hydrogen and ammonia reactions on GaN," *Surface Science*, vol. 381, no. 1, pp. L581–L588, Jun. 1997. doi: 10.1016/S0039-6028(97)00085-X

[174] V. J. Bellitto, Y. Yang, B. D. Thoms, D. D. Koleske, A. E. Wickenden, and R. L. Henry, "Desorption of hydrogen from GaN(0001) observed by HREELS and ELS," *Surface Science*, vol. 442, no. 2, pp. L1019–L1023, Nov. 1999. doi: 10.1016/S0039-6028(99)00973-5

[175] D. Gregušová, R. Stoklas, K. Čičo, T. Lalinský, and P. Kordoš, "AlGaN/GaN metal–oxide–semiconductor heterostructure field-effect transistors with 4 nm thick Al2O3 gate oxide," *Semicond. Sci. Technol.*, vol. 22, no. 8, pp. 947–951, Jul. 2007. doi: 10.1088/0268-1242/22/8/021

[176] T. Hashizume, S. Ootomo, T. Inagaki, and H. Hasegawa, "Surface passivation of GaN and GaN/AlGaN heterostructures by dielectric films and its application to insulated-gate heterostructure transistors," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena*, vol. 21, no. 4, pp. 1828–1838, Jul. 2003. doi: 10.1116/1.1585077

[177] N. Ramanan, B. Lee, C. Kirkpatrick, R. Suri, and V. Misra, "Properties of atomic layer deposited dielectrics for AlGaN/GaN device passivation," *Semicond. Sci. Technol.*, vol. 28, no. 7, p. 074004, Jun. 2013. doi: 10.1088/0268-1242/28/7/074004

[178] B. S. Eller, J. Yang, and R. J. Nemanich, "Electronic surface and dielectric interface states on GaN and AlGaN," *Journal of Vacuum Science & Technology A*, vol. 31, no. 5, p. 050807, Sep. 2013. doi: 10.1116/1.4807904

[179] T. Hashizume, S. Ootomo, and H. Hasegawa, "Suppression of current collapse in insulated gate AlGaN/GaN heterostructure field-effect transistors using ultrathin Al2O3 dielectric," *Appl. Phys. Lett.*, vol. 83, no. 14, pp. 2952–2954, Oct. 2003. doi: 10.1063/1.1616648

[180] Q. Wang, X. Cheng, L. Zheng, P. Ye, M. Li, L. Shen, J. Li, D. Zhang, Z. Gu, and Y. Yu, "Band alignment between PEALD-AlNO and AlGaN/GaN determined by angle-resolved X-ray photoelectron spectroscopy," *Applied Surface Science*, vol. 423, pp. 675–679, Nov. 2017. doi: 10.1016/j.apsusc.2017.06.192

[181] J. Yang, B. S. Eller, and R. J. Nemanich, "Surface band bending and band alignment of plasma enhanced atomic layer deposited dielectrics on Ga- and N-face gallium nitride," *Journal of Applied Physics*, vol. 116, no. 12, p. 123702, Sep. 2014. doi: 10.1063/1.4895985

[182] B. P. Gila, J. W. Johnson, R. Mehandru, B. Luo, A. H. Onstine, V. Krishnamoorthy, S. Bates, C. R. Abernathy, F. Ren, and S. J. Pearton, "Gadolinium Oxide and Scandium Oxide: Gate Dielectrics for GaN MOSFETs," *physica status solidi (a)*, vol. 188, no. 1, pp. 239–242, 2001. doi: 10.1002/1521-396X(200111)188:1¡239::AID-PSSA239¿3.0.CO;2-D

[183] P. Reddy, S. Washiyama, W. Mecouch, L. H. Hernandez-Balderrama, F. Kaess, M. Hayden Breckenridge, B. Sarkar, B. B. Haidet, A. Franke, E. Kohn, R. Collazo, and Z. Sitar, "Plasma enhanced chemical vapor deposition of SiO2 and SiNx on AlGaN: Band offsets and interface studies as a function of Al composition," *Journal of Vacuum Science & Technology A*, vol. 36, no. 6, p. 061101, Nov. 2018. doi: 10.1116/1.5050501

[184] X. Jiang, Z. Ma, J. Xu, K. Chen, L. Xu, W. Li, X. Huang, and D. Feng, "a-SiNx:H-based ultra-low power resistive random access memory with tunable Si dangling bond conduction paths," *Sci Rep*, vol. 5, no. 1, p. 15762, Oct. 2015. doi: 10.1038/srep15762

[185] H.-D. Kim, H.-M. An, and T. G. Kim, "Resistive-switching behavior in Ti/Si3N4/Ti memory structures for ReRAM applications," *Microelectronic Engineering*, vol. 98, pp. 351–354, Oct. 2012. doi: 10.1016/j.mee.2012.07.052

[186] S. M. Hong, H.-D. Kim, H.-M. An, and T. G. Kim, "Effect of Work Function Difference Between Top and Bottom Electrodes on the Resistive Switching Properties of SiN Films," *IEEE Electron Device Letters*, vol. 34, no. 9, pp. 1181–1183, Sep. 2013. doi: 10.1109/LED.2013.2272631

[187] N. Jehanathan, Y. Liu, B. Walmsley, J. Dell, and M. Saunders, "Effect of oxidation on the chemical bonding structure of PECVD SiNx thin films," *Journal of Applied Physics*, vol. 100, no. 12, p. 123516, Dec. 2006. doi: 10.1063/1.2402581

[188] G. N. Parsons, J. H. Souk, and J. Batey, "Low hydrogen content stoichiometric silicon nitride films deposited by plasma-enhanced chemical vapor deposition," *Journal of Applied Physics*, vol. 70, no. 3, pp. 1553–1560, Aug. 1991. doi: 10.1063/1.349544

[189] F. H. P. M. Habraken, R. H. G. Tijhaar, W. F. van der Weg, A. E. T. Kuiper, and M. F. C. Willemsen, "Hydrogen in low-pressure chemical-vapor-deposited silicon (oxy)nitride films," *Journal of Applied Physics*, vol. 59, no. 2, pp. 447–453, Jan. 1986. doi: 10.1063/1.336651

[190] W. a. P. Claassen, W. G. J. N. Valkenburg, F. H. P. M. Habraken, and Y. Tamminga, "Characterization of Plasma Silicon Nitride Layers," *J. Electrochem. Soc.*, vol. 130, no. 12, p. 2419, Dec. 1983. doi: 10.1149/1.2119600

[191] J. Yota, J. Hander, and A. A. Saleh, "A comparative study on inductively-coupled plasma high-density plasma, plasma-enhanced, and low pressure chemical vapor deposition silicon nitride films," *Journal of Vacuum Science & Technology A*, vol. 18, no. 2, pp. 372–376, Mar. 2000. doi: 10.1116/1.582195

[192] J. Robertson and M. J. Powell, "Gap states in silicon nitride," *Appl. Phys. Lett.*, vol. 44, no. 4, pp. 415–417, Feb. 1984. doi: 10.1063/1.94794

[193] J. G. E. Gardeniers, H. a. C. Tilmans, and C. C. G. Visser, "LPCVD silicon-rich silicon nitride films for applications in micromechanics, studied with statistical experimental design*," *Journal of Vacuum Science & Technology A*, vol. 14, no. 5, pp. 2879–2892, Sep. 1996. doi: 10.1116/1.580239

[194] A. Alexewicz, M. Alomari, D. Maier, H. Behmenburg, C. Giesen, M. Heuken, D. Pogany, E. Kohn, and G. Strasser, "Current collapse reduction in InAlGaN/GaN high

electron mobility transistors by surface treatment of thermally stable ultrathin in situ SiN passivation," *Solid-State Electronics*, vol. 89, pp. 207–211, Nov. 2013. doi: 10.1016/j.sse.2013.09.001

[195] H. Sun, M. Wang, R. Yin, J. Chen, S. Xue, J. Luo, Y. Hao, and D. Chen, "Investigation of the Trap States and v_{th} Instability in LPCVD Si_3N_4/AlGaN/GaN MIS-HEMTs with an In-Situ Si_3N_4 Interfacial Layer," *IEEE Transactions on Electron Devices*, vol. 66, no. 8, pp. 3290–3295, Aug. 2019. doi: 10.1109/TED.2019.2919246

[196] X. Wang, S. Huang, Y. Zheng, K. Wei, X. Chen, G. Liu, T. Yuan, W. Luo, L. Pang, H. Jiang, J. Li, C. Zhao, H. Zhang, and X. Liu, "Robust SiNx/AlGaN Interface in GaN HEMTs Passivated by Thick LPCVD-Grown SiNx Layer," *IEEE Electron Device Letters*, vol. 36, no. 7, pp. 666–668, Jul. 2015. doi: 10.1109/LED.2015.2432039

[197] Z. Zhang, W. Li, K. Fu, G. Yu, X. Zhang, Y. Zhao, S. Sun, L. Song, X. Deng, Z. Xing, L. Yang, R. Ji, C. Zeng, Y. Fan, Z. Dong, Y. Cai, and B. S. Zhang, "AlGaN/GaN MIS-HEMTs of Very-Low V_{th} Hysteresis and Current Collapse With In-Situ Pre-Deposition Plasma Nitridation and LPCVD-Si_3N_4 Gate Insulator," *IEEE Electron Device Letters*, vol. 38, no. 2, pp. 236–239, Feb. 2017. doi: 10.1109/LED.2016.2636136

[198] X. Zheng, H. Li, M. Guidry, B. Romanczyk, E. Ahmadi, K. Hestroffer, S. Wienecke, S. Keller, and U. K. Mishra, "Analysis of MOCVD SiNx Passivated N-Polar GaN MIS-HEMTs on Sapphire With High $f_{max} \cdot V_{DS,Q}$," *IEEE Electron Device Letters*, vol. 39, no. 3, pp. 409–412, Mar. 2018. doi: 10.1109/LED.2018.2799160

[199] V. I. Belyi and A. A. Rastorguyev, "A New View on the Nature of Electron Levels in Amorphous Silicon Nitride," p. 8.

[200] J. H. Dycus, K. J. Mirrielees, E. D. Grimley, R. Kirste, S. Mita, Z. Sitar, R. Collazo, D. L. Irving, and J. M. LeBeau, "Structure of Ultrathin Native Oxides on III–Nitride Surfaces," *ACS Appl. Mater. Interfaces*, vol. 10, no. 13, pp. 10 607–10 611, Apr. 2018. doi: 10.1021/acsami.8b00845

[201] Z. Zhang, M. Hua, J. He, G. Tang, Q. Qian, and K. J. Chen, "Ab initio study of impact of nitridation at amorphous-SiNx/GaN interface," *Appl. Phys. Express*, vol. 11, no. 8, p. 081003, Jul. 2018. doi: 10.7567/APEX.11.081003

[202] I. Daumiller, D. Theron, C. Gaquiere, A. Vescan, R. Dietrich, A. Wieszt, H. Leier, R. Vetury, U. Mishra, I. Smorchkova, S. Keller, C. Nguyen, and E. Kohn, "Current instabilities in GaN-based devices," *IEEE Electron Device Letters*, vol. 22, no. 2, pp. 62–64, Feb. 2001. doi: 10.1109/55.902832

[203] M. Neuburger, I. Daumiller, M. Kunze, M. Seyboth, T. Jenkins, J. V. Nostrand, and E. Kohn, "Influence of polarization on the properties of GaN based FET

structures," *physica status solidi (c)*, vol. n/a, no. 6, pp. 1919–1939, 2003. doi: 10.1002/pssc.200303134

[204] T. Suemitsu and I. Makabe, "Effective Schottky Barrier Height Model for N-Polar and Ga-Polar GaN by Polarization-Induced Surface Charges with Finite Thickness," *physica status solidi (b)*, vol. 257, no. 4, p. 1900528, 2020. doi: 10.1002/pssb.201900528

[205] B. Luo, J. W. Johnson, J. Kim, R. M. Mehandru, F. Ren, B. P. Gila, A. H. Onstine, C. R. Abernathy, S. J. Pearton, A. G. Baca, R. D. Briggs, R. J. Shul, C. Monier, and J. Han, "Influence of MgO and Sc2O3 passivation on AlGaN/GaN high-electron-mobility transistors," *Appl. Phys. Lett.*, vol. 80, no. 9, pp. 1661–1663, Mar. 2002. doi: 10.1063/1.1455692

[206] M. Hua, C. Liu, S. Yang, S. Liu, K. Fu, Z. Dong, Y. Cai, B. Zhang, and K. J. Chen, "Characterization of Leakage and Reliability of SiNx Gate Dielectric by Low-Pressure Chemical Vapor Deposition for GaN-based MIS-HEMTs," *IEEE Transactions on Electron Devices*, vol. 62, no. 10, pp. 3215–3222, Oct. 2015. doi: 10.1109/TED.2015.2469716

[207] V. K. Surana, N. Bhardwaj, A. Rawat, Y. Yadav, S. Ganguly, and D. Saha, "Realization of high quality silicon nitride deposition at low temperatures," *Journal of Applied Physics*, vol. 126, no. 11, p. 115302, Sep. 2019. doi: 10.1063/1.5114927

[208] B. Romanczyk, S. Wienecke, M. Guidry, H. Li, E. Ahmadi, X. Zheng, S. Keller, and U. K. Mishra, "Demonstration of Constant 8 W/mm Power Density at 10, 30, and 94 GHz in State-of-the-Art Millimeter-Wave N-Polar GaN MISHEMTs," *IEEE Transactions on Electron Devices*, vol. 65, no. 1, pp. 45–50, Jan. 2018. doi: 10.1109/TED.2017.2770087

[209] O. S. Koksaldi, J. Haller, H. Li, B. Romanczyk, M. Guidry, S. Wienecke, S. Keller, and U. K. Mishra, "N-Polar GaN HEMTs Exhibiting Record Breakdown Voltage Over 2000 V and Low Dynamic On-Resistance," *IEEE Electron Device Letters*, vol. 39, no. 7, pp. 1014–1017, Jul. 2018. doi: 10.1109/LED.2018.2834939

[210] S. Rajabi, S. Mandal, B. Ercan, H. Li, M. A. Laurent, S. Keller, and S. Chowdhury, "A Demonstration of Nitrogen Polar Gallium Nitride Current Aperture Vertical Electron Transistor," *IEEE Electron Device Letters*, vol. 40, no. 6, pp. 885–888, Jun. 2019. doi: 10.1109/LED.2019.2914026

[211] I. Sayed, W. Liu, S. Chan, C. Gupta, M. Guidry, H. Li, S. Keller, and U. Mishra, "Net negative fixed interface charge for Si_3N_4 and SiO_2 grown in situ on $000\bar{1}$ N-polar GaN," *Appl. Phys. Lett.*, vol. 115, no. 3, p. 032103, Jul. 2019. doi: 10.1063/1.5111148

[212] I. Sayed, W. Liu, S. Chan, C. Gupta, H. Li, S. Keller, and U. K. Mishra, "Flatband voltage stability and time to failure of MOCVD-grown SiO_2 and Si_3N_4 dielectrics on N-polar GaN," *Appl. Phys. Express*, vol. 12, no. 12, p. 121001, Oct. 2019. doi: 10.7567/1882-0786/ab4d39

[213] W. Liu, I. Sayed, C. Gupta, H. Li, S. Keller, and U. Mishra, "An improved methodology for extracting interface state density at Si_3N_4/GaN," *Appl. Phys. Lett.*, vol. 116, no. 2, p. 022104, Jan. 2020. doi: 10.1063/1.5125645

[214] R. S. Rosler, "Low pressure CVD production processor for poly, nitride, and oxide," *Slid State Technology*, pp. 63–70, 1977.

[215] H. J. Stein, "Thermally annealed silicon nitride films: Electrical characteristics and radiation effects," *Journal of Applied Physics*, vol. 57, no. 6, pp. 2040–2047, Mar. 1985. doi: 10.1063/1.334393

[216] H. Wong, M. C. Poon, Y. Gao, and T. C. W. Kok, "Preparation of Thin Dielectric Film for Nonvolatile Memory by Thermal Oxidation of Si-Rich LPCVD Nitride," *J. Electrochem. Soc.*, vol. 148, no. 5, p. G275, May 2001. doi: 10.1149/1.1362552

[217] S. Choi, H. Yang, M. Chang, S. Baek, H. Hwang, S. Jeon, J. Kim, and C. Kim, "Memory characteristics of silicon nitride with silicon nanocrystals as a charge trapping layer of nonvolatile memory devices," *Appl. Phys. Lett.*, vol. 86, no. 25, p. 251901, Jun. 2005. doi: 10.1063/1.1951060

[218] Y. Sun, H. Y. Yu, N. Singh, K. C. Leong, E. Gnani, G. Baccarani, G. Q. Lo, and D. L. Kwong, "Vertical-Si-Nanowire-Based Nonvolatile Memory Devices With Improved Performance and Reduced Process Complexity," *IEEE Transactions on Electron Devices*, vol. 58, no. 5, pp. 1329–1335, May 2011. doi: 10.1109/TED.2011.2114664

[219] P. Arifin, T. L. Tansley, and E. M. Goldys, "Conduction mechanism in a metal-insulator-semiconductor structure with a low temperature GaAs insulating layer," *Solid-State Electronics*, vol. 41, no. 8, pp. 1075–1078, Aug. 1997. doi: 10.1016/S0038-1101(97)00061-0

[220] S. I. Raider, R. Flitsch, J. A. Aboaf, and W. A. Pliskin, "Surface Oxidation of Silicon Nitride Films," *J. Electrochem. Soc.*, vol. 123, no. 4, p. 560, Apr. 1976. doi: 10.1149/1.2132877

[221] H. Du, R. E. Tressler, and K. E. Spear, "Thermodynamics of the Si-N-O System and Kinetic Modeling of Oxidation of Si3 N 4," *J. Electrochem. Soc.*, vol. 136, no. 11, p. 3210, Nov. 1989. doi: 10.1149/1.2096427

[222] L. Stauffer and K. Instruments, "Fundamentals of Semiconductor C-V Measurements," *Keithley Instruments, Inc.*, no. 3019, p. 4, Feb. 2009.

[223] F. Akyol, D. N. Nath, S. Krishnamoorthy, P. S. Park, and S. Rajan, "Suppression of electron overflow and efficiency droop in N-polar GaN green light emitting diodes," *Appl. Phys. Lett.*, vol. 100, no. 11, p. 111118, Mar. 2012. doi: 10.1063/1.3694967

[224] M. H. Wong, S. Keller, S. D. Nidhi, D. J. Denninghoff, S. Kolluri, D. F. Brown, J. Lu, N. A. Fichtenbaum, E. Ahmadi, U. Singisetti, A. Chini, S. Rajan, S. P. DenBaars, J. S. Speck, and U. K. Mishra, "N-polar GaN epitaxy and high electron mobility transistors," *Semicond. Sci. Technol.*, vol. 28, no. 7, p. 074009, Jun. 2013. doi: 10.1088/0268-1242/28/7/074009

[225] Y. Cho, J. Encomendero, S.-T. Ho, H. G. Xing, and D. Jena, "N-polar GaN/AlN resonant tunneling diodes," *Appl. Phys. Lett.*, vol. 117, no. 14, p. 143501, Oct. 2020. doi: 10.1063/5.0022143

[226] B. Romanczyk, X. Zheng, M. Guidry, H. Li, N. Hatui, C. Wurm, A. Krishna, E. Ahmadi, S. Keller, and U. K. Mishra, "W-Band Power Performance of SiN-Passivated N-Polar GaN Deep Recess HEMTs," *IEEE Electron Device Letters*, vol. 41, no. 3, pp. 349–352, Mar. 2020. doi: 10.1109/LED.2020.2967034

[227] R. Collazo, S. Mita, A. Rice, R. Dalmau, P. Wellenius, J. Muth, and Z. Sitar, "Fabrication of a GaN p/n lateral polarity junction by polar doping selectivity," *physica status solidi c*, vol. 5, no. 6, pp. 1977–1979, 2008. doi: 10.1002/pssc.200778624

[228] W. Liu, I. Sayed, B. Romanczyk, N. Hatui, M. Guidry, W. J. Mitchell, S. Keller, and U. K. Mishra, "Ru/N-Polar GaN Schottky Diode With Less Than 2 μA/cm^2 Reverse Current," *IEEE Electron Device Letters*, vol. 41, no. 10, pp. 1468–1471, Oct. 2020. doi: 10.1109/LED.2020.3014524

[229] P. Neudeck, R. Okojie, and L.-Y. Chen, "High-temperature electronics - a role for wide bandgap semiconductors?" *Proceedings of the IEEE*, vol. 90, no. 6, pp. 1065–1076, Jun. 2002. doi: 10.1109/JPROC.2002.1021571

[230] A. Noya and M. B. Takeyama, "Low-Temperature Formation of NiSi2 Phase in Ni/Si System," *Electronics and Communications in Japan*, vol. 99, no. 9, pp. 85–91, 2016. doi: 10.1002/ecj.11860

[231] J. M. Shannon, "A New Majority Carrier Diode–The Camel Diode," *Jpn. J. Appl. Phys.*, vol. 19, no. S1, p. 301, Jan. 1980. doi: 10.7567/JJAPS.19S1.301

[232] J. M. Shannon, "Increasing the effective height of a Schottky barrier using low-energy ion implantation," *Appl. Phys. Lett.*, vol. 25, no. 1, pp. 75–77, Jul. 1974. doi: 10.1063/1.1655287

[233] J. M. Shannon, "Control of Schottky barrier height using highly doped surface layers," *Solid-State Electronics*, vol. 19, no. 6, pp. 537–543, Jun. 1976. doi: 10.1016/0038-1101(76)90019-8

[234] J. M. Shannon, "A majority-carrier camel diode," *Appl. Phys. Lett.*, vol. 35, no. 1, pp. 63–65, Jul. 1979. doi: 10.1063/1.90931

[235] S. C. Cruz, S. Keller, T. E. Mates, U. K. Mishra, and S. P. DenBaars, "Crystallographic orientation dependence of dopant and impurity incorporation in GaN films grown by metalorganic chemical vapor deposition," *Journal of Crystal Growth*, vol. 311, no. 15, pp. 3817–3823, Jul. 2009. doi: 10.1016/j.jcrysgro.2009.02.051

[236] N. A. Fichtenbaum, C. Schaake, T. E. Mates, C. Cobb, S. Keller, S. P. DenBaars, and U. K. Mishra, "Electrical characterization of p-type N-polar and Ga-polar GaN grown by metalorganic chemical vapor deposition," *Appl. Phys. Lett.*, vol. 91, no. 17, p. 172105, Oct. 2007. doi: 10.1063/1.2800304

[237] T. Aoki, T. Tanikawa, R. Katayama, T. Matsuoka, and K. Shiojima, "Electrical characteristics of N-polar p-type GaN Schottky contacts," *Jpn. J. Appl. Phys.*, vol. 55, no. 4S, p. 04EJ09, Mar. 2016. doi: 10.7567/JJAP.55.04EJ09

[238] A. Krishna, A. Raj, N. Hatui, S. Keller, and U. K. Mishra, "Investigation of nitrogen polar p-type doped GaN/AlxGa(1-x)N superlattices for applications in wide-bandgap p-type field effect transistors," *Appl. Phys. Lett.*, vol. 115, no. 17, p. 172105, Oct. 2019. doi: 10.1063/1.5124326

[239] E. Rocco, O. Licata, I. Mahaboob, K. Hogan, S. Tozier, V. Meyers, B. McEwen, S. Novak, B. Mazumder, M. Reshchikov, L. Douglas Bell, and F. Shahedipour-Sandvik, "Hillock assisted p-type enhancement in N-polar GaN:Mg films grown by MOCVD," *Sci Rep*, vol. 10, no. 1, p. 1426, Jan. 2020. doi: 10.1038/s41598-020-58275-1

[240] S. Nakamura, N. Iwasa, M. S. M. Senoh, and T. M. T. Mukai, "Hole Compensation Mechanism of P-Type GaN Films," *Jpn. J. Appl. Phys.*, vol. 31, no. 5R, p. 1258, May 1992. doi: 10.1143/JJAP.31.1258

[241] A. Klump, M. P. Hoffmann, F. Kaess, J. Tweedie, P. Reddy, R. Kirste, Z. Sitar, and R. Collazo, "Control of passivation and compensation in Mg-doped GaN by defect quasi Fermi level control," *Journal of Applied Physics*, vol. 127, no. 4, p. 045702, Jan. 2020. doi: 10.1063/1.5126004

[242] B. Sarkar, S. Mita, P. Reddy, A. Klump, F. Kaess, J. Tweedie, I. Bryan, Z. Bryan, R. Kirste, E. Kohn, R. Collazo, and Z. Sitar, "High free carrier concentration in p-GaN grown on AlN substrates," *Appl. Phys. Lett.*, vol. 111, no. 3, p. 032109, Jul. 2017. doi: 10.1063/1.4995239

[243] S. Usami, R. Miyagoshi, A. Tanaka, K. Nagamatsu, M. Kushimoto, M. Deki, S. Nitta, Y. Honda, and H. Amano, "Effect of dislocations on the growth of p-type GaN and on the characteristics of p–n diodes," *physica status solidi (a)*, vol. 214, no. 8, p. 1600837, 2017. doi: 10.1002/pssa.201600837

[244] S. Usami, Y. Ando, A. Tanaka, K. Nagamatsu, M. Deki, M. Kushimoto, S. Nitta, Y. Honda, H. Amano, Y. Sugawara, Y.-Z. Yao, and Y. Ishikawa, "Correlation between dislocations and leakage current of p-n diodes on a free-standing GaN substrate," *Appl. Phys. Lett.*, vol. 112, no. 18, p. 182106, Apr. 2018. doi: 10.1063/1.5024704

[245] B. G. Cohen, W. B. Snow, and A. R. Tretola, "GaAs p-n Junction Diodes for Wide Range Thermometry," *Review of Scientific Instruments*, vol. 34, no. 10, pp. 1091–1093, Oct. 1963. doi: 10.1063/1.1718140

[246] Y. B. Acharya, "Effect of temperature dependence of band gap and device constant on I–V characteristics of junction diode," *Solid-State Electronics*, vol. 45, no. 7, pp. 1115–1119, Jul. 2001. doi: 10.1016/S0038-1101(01)00139-3

[247] M. Rebien, W. Henrion, M. Hong, J. P. Mannaerts, and M. Fleischer, "Optical properties of gallium oxide thin films," *Appl. Phys. Lett.*, vol. 81, no. 2, pp. 250–252, Jul. 2002. doi: 10.1063/1.1491613

[248] B. Sarkar, P. Reddy, A. Klump, F. Kaess, R. Rounds, R. Kirste, S. Mita, E. Kohn, R. Collazo, and Z. Sitar, "On Ni/Au Alloyed Contacts to Mg-Doped GaN," *Journal of Elec Materi*, vol. 47, no. 1, pp. 305–311, Jan. 2018. doi: 10.1007/s11664-017-5775-3

[249] A. Castiglia, J.-F. Carlin, and N. Grandjean, "Role of stable and metastable Mg–H complexes in p-type GaN for cw blue laser diodes," *Appl. Phys. Lett.*, vol. 98, no. 21, p. 213505, May 2011. doi: 10.1063/1.3593964

[250] S. Neugebauer, M. P. Hoffmann, H. Witte, J. Bläsing, A. Dadgar, A. Strittmatter, T. Niermann, M. Narodovitch, and M. Lehmann, "All metalorganic chemical vapor phase epitaxy of p/n-GaN tunnel junction for blue light emitting diode applications," *Appl. Phys. Lett.*, vol. 110, no. 10, p. 102104, Mar. 2017. doi: 10.1063/1.4978268

[251] R. Soman, S. Raghavan, and N. Bhat, "An in situ monitored and controlled etch process to suppress Mg memory effects in MOCVD GaN growth on Si substrate," *Semicond. Sci. Technol.*, vol. 34, no. 12, p. 125011, Nov. 2019. doi: 10.1088/1361-6641/ab5006

[252] R. E. Thorne, S. L. Su, W. Kopp, R. Fischer, T. J. Drummond, and H. Morkoç, "Normally-on and normally-off camel diode gate GaAs field effect transistors for large scale integration," *Journal of Applied Physics*, vol. 53, no. 8, pp. 5951–5958, Aug. 1982. doi: 10.1063/1.331385

[253] J. K. Hite, R. Zoll, M. A. Mastro, and C. R. Eddy Jr., "Role of growth parameters in equalizing simultaneous growth of N- and Ga-polar GaN by MOCVD," *physica status solidi c*, vol. 11, no. 3-4, pp. 458–461, 2014. doi: 10.1002/pssc.201300675

[254] M. P. Hoffmann, R. Kirste, S. Mita, W. Guo, J. Tweedie, M. Bobea, I. Bryan, Z. Bryan, M. Gerhold, R. Collazo, and Z. Sitar, "Growth and characterization of $Al_xGa_{1-x}N$

lateral polarity structures," *physica status solidi (a)*, vol. 212, no. 5, pp. 1039–1042, 2015. doi: 10.1002/pssa.201431740

[255] M. Hoffmann, "Polarity Control and Doping in Aluminum Gallium Nitride," PhD Thesis, TU Berlin, 2013.

[256] D. Szymanski, "Development of III-Nitride Superjunctions," PhD Thesis, North Carolina State University, Raleigh, NC, USA, 2021.

[257] F. Liu, R. Collazo, S. Mita, Z. Sitar, S. J. Pennycook, and G. Duscher, "Direct Observation of Inversion Domain Boundaries of GaN on c-Sapphire at Sub-ångstrom Resolution," *Advanced Materials*, vol. 20, no. 11, pp. 2162–2165, 2008. doi: 10.1002/adma.200702522

[258] W. Guo, H. Sun, B. Torre, J. Li, M. Sheikhi, J. Jiang, H. Li, S. Guo, K.-H. Li, R. Lin, A. Giugni, E. Di Fabrizio, X. Li, and J. Ye, "Lateral-Polarity Structure of AlGaN Quantum Wells: A Promising Approach to Enhancing the Ultraviolet Luminescence," *Advanced Functional Materials*, vol. 28, no. 32, p. 1802395, 2018. doi: 10.1002/adfm.201802395

[259] O. Branson, E. A. Bonnin, D. E. Perea, H. J. Spero, Z. Zhu, M. Winters, B. Hönisch, A. D. Russell, J. S. Fehrenbacher, and A. C. Gagnon, "Nanometer-Scale Chemistry of a Calcite Biomineralization Template: Implications for Skeletal Composition and Nucleation," *PNAS*, vol. 113, no. 46, pp. 12 934–12 939, Nov. 2016. doi: 10.1073/pnas.1522864113

[260] T. Maeda, T. Narita, H. Ueda, M. Kanechika, T. Uesugi, T. Kachi, T. Kimoto, M. Horita, and J. Suda, "Design and Fabrication of GaN p-n Junction Diodes With Negative Beveled-Mesa Termination," *IEEE Electron Device Letters*, vol. 40, no. 6, pp. 941–944, Jun. 2019. doi: 10.1109/LED.2019.2912395