ABSTRACT

MEHROTRA UTKARSH, Methodologies of Cascading and Scaling to Realize High Voltage Cascaded SuperCascode Power Switch. (Under the direction of Dr. Douglas C. Hopkins)

Medium Voltage (MV), High Current (HC) switches are growing in demand for MV applications in land, sea and air transport, fast charging, renewable energy, and a host of applications in pulsed power, e.g. solid-state protection. However, widespread adoption of commercially available MV-HC power devices is limited in application due to retracted dynamic performance from paralleling many high voltage, low current semiconductors. The associated cost is relatively high because of low yield, and expensive material and fabrication. An alternative is a series connection of Low Voltage (LV)-HC semiconductors to form a SuperCascode (SC) power switch. This research introduces a Cascaded SuperCascode (CSC) power switch topology that can be further cascaded to very high voltages (>100 kV) or applied to optimize previously reported MV SCs to achieve higher switching speed, reduced balancing network size and lower switching losses. The topology can also be scaled to improve current handling capability and overcome the issues of current sharing by synchronizing the sequential turn-on. For validation, a 6.5kV 2S-3C CSCPS using TO-247 discretes was fabricated and tested showing 408 mΩ, 0.7 mA @ 4.8 kV and 40ns rise and 30ns fall in current at 4kV for 20A switching from double-pulse testing (DPT with a 6 mH load).

HV power packaging of WBG power devices is challenging due to the fast switching nature, high E-field density and operating temperature range. A common conductive layer, such as the baseplate or common backplane in typical power module structure limits voltage scalability due to excessive common-mode switching currents. This research introduces a “segmented baseplate” power packaging approach that utilizes a new organic laminate epoxy resin composite dielectric for packaging the CSC power switch to achieve elevated thermal,

mechanical and electrical performance. Two complete power module designs of a 6.5kV/105 A 2S-3C 1-layer CSCPS and a 24kV 2S-3C-2C-2C 3-layer CSCPS are provided. The six JFET 6.5kV/105A 2S-3C CSCPS power module is fabricated and evaluated for thermal performance and evaluating the substrate voltage blocking capability. The 2S-3C 6kV CSCPS has an $R_{th,ja}$ of 2.61^0C/W with leakage less than 50nA at 6kV. The overall power density of the module is 1.65 W/mm^3. Simulation results are discussed together with possible future work in the area.

Methodologies of Cascading and Scaling to Realize High Voltage Cascaded SuperCascode Power Switch

by
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DEDICATION

To my parents, Monica Mehrotra and Manish Mehrotra and my sister, Arsheya Mehrotra for their unconditional love and support throughout my pursuit of higher education, and for helping me become the best version of myself I can be. To my relatives, Ruchir Seth and Aparna Seth and my cousins, Ananya Seth and Arul Seth who have been an endless source of comfort and encouragement.

BIOGRAPHY

Utkarsh Mehrotra received his B.Tech in Electrical and Electronics Engineering from Manipal Institute of Technology, Manipal, India in 2017 and the M.S. degree in Electrical Engineering from North Carolina State University, Raleigh, NC, USA in 2020, where he pursued his Ph.D. degree in electrical engineering from the Future Renewable Electric Energy Delivery and Management (FREEDM) Systems Center in the Electrical and Computer Engineering Department. He has held Research Assistant positions with PowerAmerica, the Army Research Lab (ARL), and the Packaging Research in Electronic Energy Systems (PREES) Laboratory, North Carolina State University, Raleigh, NC, USA, under its director Dr. Douglas C. Hopkins. His research interests include the design, simulation, fabrication, and testing of power electronics packaging topologies that harness the capabilities of wide-bandgap semiconductor technology (GaN and SiC), with a focus on solid-state circuit protection and their controls, power converters and high voltage high-density power modules scalable to 25 kV voltage range.

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CHAPTER 1: Introduction and Background

Power semiconductor devices are fundamental components for power electronics. Devices are used to do power conversion, system protection, etc. and the requirement is usually ranging from a few kV to more than an MV. High Voltage (HV) power devices are used in high-power low-frequency applications such as the HVDC transmission grid, Flexible AC Transmission Systems (FACTs), renewable and storage integration at MV level, large data centers, and industrial motor drives [1]-[3]. Common semiconductor devices, such as Insulated-gate bipolar transistor (IGBT), Integrated gate-commutated thyristor (IGCT), gate turn-off thyristor (GTO), or Emitter turn-off thyristors (ETOs) are used for power switching [4]-[6]. The use of bipolar devices limits switching speed and increases switching losses (due to tail current and reverse recovery time) compared with field-effect devices and limits pulse repetition rate, converter efficiency and increases cooling system requirement. Wide Band Gap (WBG) semiconductors like Silicon Carbide (SiC) and Gallium Nitride (GaN) offer fast switching speed, low on-state resistance, the wide operating temperature can be further utilized to increase system efficiency and to develop high-power density converters [7].

SiC power devices compared to Si counterparts have a higher breakdown (*8x*), thermal conductivity (*3x*) and provide *>60X* reduction in size and *>8X* reduction in power loss [8]-[10]. WBG power-converters have (1) higher operating temperature range (2) higher voltage rating per unit area and (3) lower high-frequency losses compared to their Silicon counterparts. WBG materials are compared against Si for their relative material properties and shown in Fig. 1.1.

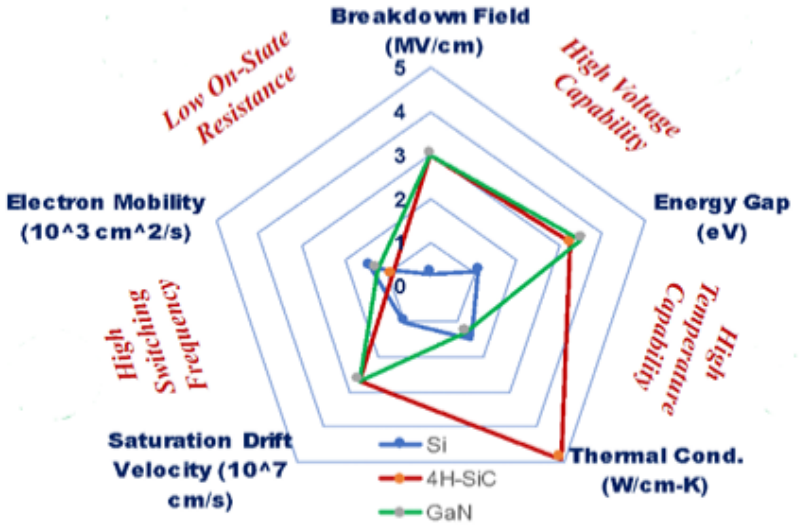


Fig. 1.1: Material property comparison of WBG (4H-SiC and GaN) w.r.t Si [11]

Two commonly used unipolar power devices vertical or lateral junction-gate-field effect transistors (JFET) and trench, and planar metal-oxide-field effect transistors (MOSFETs), are available in the few kV range (10 kV) [12]-[14]. MOSFETs are widely adopted for their normally OFF behavior and ease of design. Bipolar devices such as IGBTs and GTOs are preferred at voltages over 15kV, as the on-resistance of unipolar devices become significant making them unattractive in real applications. So far SiC IGBTs with voltage ratings from 12kV to 27kV have been reported in [15]-[19] and SiC GTOs up to 22kV have been developed and showcased in pulsed power applications [20]-[22]. However, the fabrication of these higher voltage bipolar devices is still under research. Current efforts mainly focus on increasing carrier lifetime, improving substrate quality, enlarging epi-layer thickness, and reducing defect density [23,24].

Unipolar devices (e.g. JFETs) in comparison to bipolar devices use majority carriers for conduction offering better switching performance [25,26]. Other advantages include low on-resistance from high-channel density, smaller miller and input capacitance and stable pinch-off at

elevated temperature. JFETs are normally-on and can be used in a cascode configuration with a low-voltage (LV) silicon (Si) MOSFET, as shown in Fig. 1.2(a). The configuration operates by biasing the gate-source voltage across the Si MOSFET which creates a short between the JFET drain-source driving the device into conduction mode. Alternatively, biasing the drain-source voltage of the Si MOSFET to a voltage lower than the JFET pinch-off blocking mode is realized. Any LV device can be used in place of the Si MOSFET as long as its operating voltage is greater than the driving gate-source voltage required to turn on the JFET. The LV device should contribute minimum on-resistance to the switching topology.

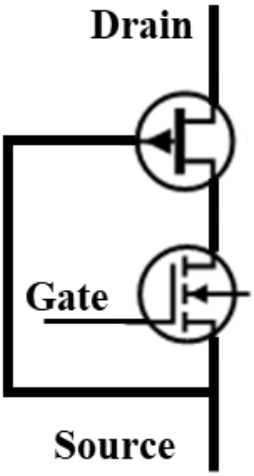


Fig 1.2(a): Baliga-pair/Cascode topology

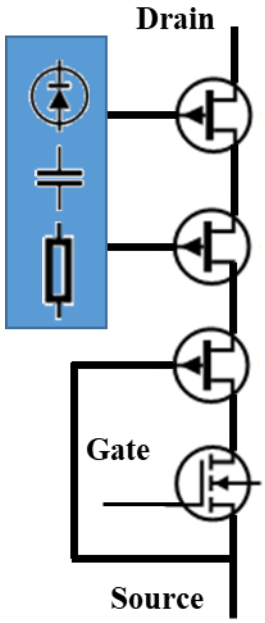


Fig. 1.2(b): SuperCascode topology

Due to the lack of commercially available medium or high voltage power devices for applications of Distributed FACTs and the Battery energy storage system (BESS), multilevel topologies are designed with a large number of current commercially available WBG devices stacked up in series-parallel combination. However, multiple device combinations increases system volumes and cooling requirement, makes the system complicated due to the relatively

large number of control signals which increases gate driver complexity due to the requirement of isolated gate drivers and reduce the reliability of the overall system.

As an alternative using fewer *>10kV* devices reduces the risk of potential failure, increases system reliability, and cost. HV WBG devices in the *3.3kV-15kV* have been researched and reported extensively in [27]-[29] and have shown significant technology maturation making systems compact, efficient, etc. In research, *10kV* and *15kV* SiC MOSFETs [30,31], *13kV* p-i-n diode [32] and *15kV* SiC IGBTs [33] have been developed and demonstrated to date. However, adoption is limited due to lack of commercial availability and high cost, creating the need for alternative approaches to realize HV switches. One such alternative to achieve HV-High Current (HC) power switches for MW power is a series connection of many low voltage (LV) – HC devices, another is a parallel connection of multiple HV-LC semiconductor devices (Si IGBTs, SiC MOSFETs, SiC JFETs).

Philosophically, ideal paralleling would have each parallel device trigger the next device when current levels begin to rise whereas series devices would have each trigger the next when the voltage levels rise. As most modern-day power devices are field triggered, (i.e voltage-driven) self-triggering series devices with voltage signals are natural and easily implemented with serial LV-HC devices. In self-triggering, the entire switch can be turned on or off by using auxiliary elements, such as resistors, capacitors, and avalanche diodes which re-circulate energy to synchronously power devices. An approach through duality may be possible with current-driven transistors such as bipolar devices. A broader perspective based on duality can be related to the foundations of electrical circuits where the Thevenin equivalent is for voltage-source circuits with components in series. Conversely, the Norton equivalent is for current-source circuits with components in parallel.

Serial connection of Si IGBTs [34] and SiC MOSFETs in Austin SuperMOS [35,36] have been documented to realize HV switches. However, these approaches have issues requiring individual gate drive signals per device in a string, isolated drivers, and unequal voltage stress among devices that limit scalability and performance. An alternative to simplify gate driver requirements is the Super Cascode Power Switch (SCPS) made by series connecting depletion-mode devices (JFETs) with one control input or gate and works on the principle of sequential switching. The SCPS similar to a Cascode, e.g. Baliga-pair configuration can take advantage of WBG high-speed switching while maintaining a commercial driver to control an LV Si switch [37]. The topology is scalable and applicable to any depletion mode device, such as JFETs, vacuum tubes, MEMS switches, etc. The SuperCascode concept can be applied to sequentially trigger serially connected greater than two power devices. In the SCPS approach, shown in Fig. 1.2(b) a static and passive balancing network composed of diodes, capacitors and resistors are used.

The following sections and chapters of this dissertation will discuss the challenges of different SuperCascode Power Switches (SCPS) which limit voltage scalability. Next, different configurations of balancing networks are discussed and further analyzed in the following sections. This chapter also discusses present-day challenges in High Voltage power packaging in regards to capacitive coupling with baseplate and parasitics resistance, capacitance and inductance internal to the power module.

1.1 Application areas for HV semiconductor devices

HVDC generation and transmission have gathered interest due to its potential benefits in reducing conduction losses, size and heat generation in cabling [38,39]. The loss reduction is proportional to the system voltage step up. For instance, a *1MW* system at *1kV,* cabling conducts

1kA producing *25kW* I^2R loss, where cable resistance is assumed to be *25m*Ω. The cable contributes *2.5%* to the net system efficiency. Whereas for a system operating at *10kV,* cabling conducts *100A* producing *250W* I^2R loss, contributing only *0.025%* to the net efficiency. Concluding that a *100x* loss reduction is possible stepping up the voltage by *10x* and so on. HVDC transmission is also free from radiation, induction and dielectric losses which increase the lifetime of the conductor [40].

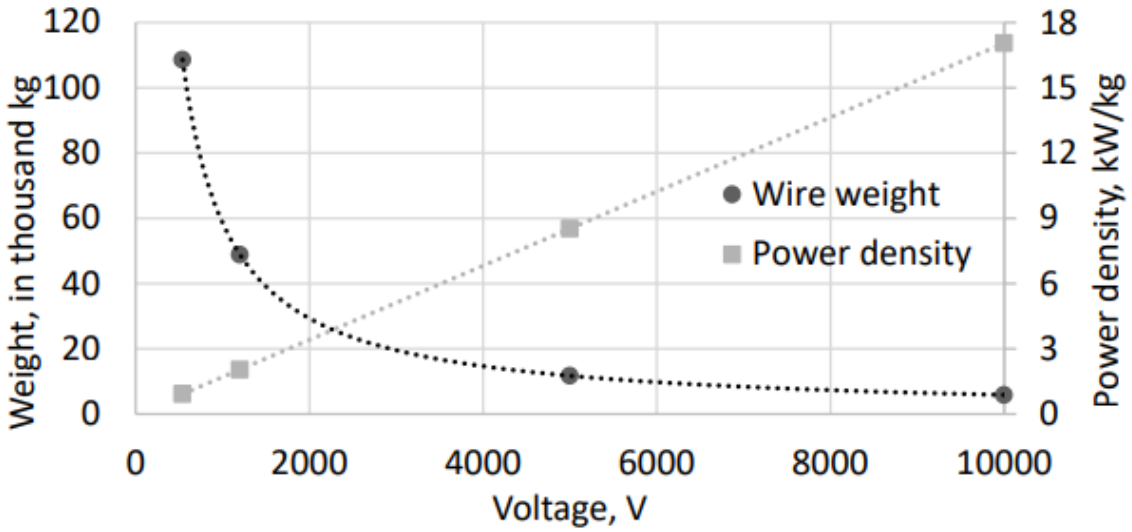


Fig. 1.3: Blocking Voltage vs Weight and Power density of cabling copper conductor [41]

Transitioning to HVDC also reduces the wire weight of the conductor and increases the gravimetric power density of cabling as shown in Fig. 1.3. For example: At a voltage of *1kV,* the weight of the copper wiring is estimated to be *51,800 kg*, whereas for a *10kV* the weight of the copper wiring is only *5,865 kg*, which is an *8.8*-fold weight reduction (The calculation assumes *8* x *45m* cables copper wire for a *100 MW* notional aircraft with *2x* redundancy and *2* generators) [41]. This shows that by scaling transmission line power rating its possible to achieve higher efficiency, power and weight density.

Solid-State Circuit Protection in Solid State Transformers (SSTs), etc are being developed to replace traditional line-frequency (*50/60 Hz*) transformers and provide numerous "smart" functions from regulating voltage to implementing distributed intelligence in the evolving smart grid [42]-[46]. The SSTs are considered for applications in power distribution for mobile platforms (EVs, shipboard power, electric aircraft, etc.), and energy management systems [47,48]. Of particular note are applications to incorporate energy storage systems (ESSs) [49]-[53] as shown in Fig. 1.4 [54].

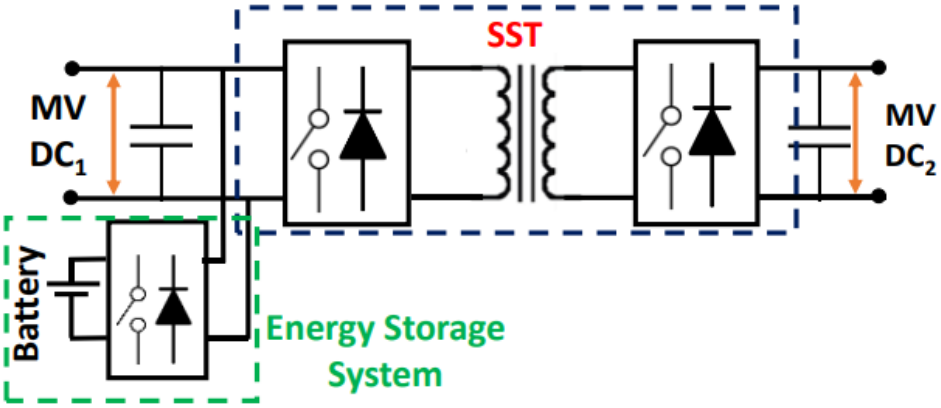


Fig. 1.4: SST with Energy Storage Systems (ESS) [54]

SSTs as with other power electronic equipment are more susceptible to overvoltage faults due to low system impedance and voltage sensitivity of accompanying power electronics creating a need for fast system protection. Solid-State Circuit Breakers (SSCBs) provide arc-less current in the bulk of semiconductors offering better lifecycle and limited arc flash hazards [55,56]. Further, SSCBs can be configured and digitally controlled providing flexibility to incorporate an adjustable trip curve and soft-switching, inrush algorithms [57]. For HV Bi-directional Solid-State Circuit Breaker (BSSCB) applications, an ultra-high conductance, high-voltage (HV), high-current (HC) power switch that can block the system rated voltage, handle

high impulse currents (*~5-10x* rated current for a short time interval *~ms*) and fast switching speeds. Medium Voltage DC (MVDC) are considered for shipboard power supply as an alternative to traditional ac shipboard networks for their ease of integration of energy storage modules, electric drivetrain and pulsed mission loads. MVDC operation simplifies generator synchronization routine and can be parallel and operated asynchronously allowing prime movers to operate at unmatched more economic optimized methods [58]. The process also eliminates reactive loss and voltage drop, removes the need for *60Hz* transformers and overcomes frequency instability issues. For this application, MV power devices in the *6-24kV* range are required to replace shipboard supplies which vary from *4.16kV* for aircraft carriers and $11kV_{ac}$ for commercial cruise liners [59]

1.2 Advantages of SuperCascode Power Switch compared to single power die

The use of low-voltage SiC devices to realize a SuperCascode Power Switch (SCPS) reduces cost [60]. It also simplifies realization as the SCPS can be fabricated with discrete devices on Printed Circuit Boards [61]. Other performance advantages of the SCPS over single SiC MOSFETs switches are :

a) Electrical Performance – SCPS structure use sequentially self-triggering serially connected SiC JFETs. SiC JFETs in comparison to power SiC MOSFETs have the advantages of *3X* lower $/Amp [62] and *3.3X* higher J/cm^2 energy capability before failure [63].
b) Less susceptible to TCR failures – Study in [64], reported HV rated devices (>10kV) are more susceptible to Terrestial Cosmic Radiation (TCR) failure and require high deration in the application. Whereas, as the SCPS is made of discrete LV JFETs, the margin of deration can be further reduced.

c) Thermal Performance – SCPS distributes dissipation over multiple devices facilitating heat extraction via thermal spreading across a larger physical area. Thermal spreading leads to lower thermal resistance (R_{jc}) and the net result is a higher RMS current rating in actual application. JFETs also have a stable threshold voltage over temperature, i.e JFET thresholds shift by $<10\ mV$ compared to $>300\ mV$ observed in MOSFETs at 175^0C [65]. This minimum threshold drift under continuous stress makes normally on JFETs easier to cascade, and balance.

d) Reliability – SCPS has higher reliability compared to a single HV device as a failed JFET doesn't compromise the entire switching string operation, through every failure increases voltage stress per JFET under blocking and should be considered in the design.

Table 1.1 compares the performance of UnitedSiC's SCPS with paralleled HVs MOSFETs scaled to the same voltage range. The table shows *23%* less SiC area requirement leading to lower cost and significantly lower gate charge with higher V_{TH} enabling fast and stable switching power devices in applications.

Table 1.1: Comparison of parallel SiC MOSFETs with SuperCascode Power Switch

Module Approach		Conventional	SuperCascode
SiC Chip Technology	Die	6.5 kV MOSFET [66]	1.2 kV JFET Chip (Using Gen4 UnitedSiC devices)
	$R_{dson}A$	30 mΩ-cm^2	1.3 mΩ-cm^2 [67]
	Die Size	8.33 x 8.33 mm^2	6.25 x 5.73 mm^2
	Die Max R_{on} @ RT	77 mΩ (39 mm^2 active, 69 mm^2 total)	3.85 mΩ (32.24 mm^2, 35.81 mm^2 total)
Half-Bridge Module Technology	Max R_{on} @ RT	20 mΩ	23 mΩ
	Switch Configuration	4 dies in parallel	6 JFETs in series
	Total Die Count	8	12
	Total SiC Area	552 mm^2	429.75 mm^2
Module Features	Typical V_{TH} @ 150^{0}C	2 V	3.7 V
	Practical Gate Drive	-5 V to +20V	Standard 0V to +12V
	Total Gate Charge, Q_g	2360 nC	100 nC
	Anti-parallel diode	Knee voltage: >2V High Q_{RR} (Built-in)	Knee voltage: 0.7V Low Q_C (Built-in)

1.3 Voltage clamping techniques in serially connected device

The rating of the SCPS is a summation of the individual blocking voltages of the LV JFETs. Under an ideal scenario, in the SCPS each JFET should block equivalent voltage under a steady (*off*) state and synchronize sequential switching. However, actual devices have inbuilt tolerances, gate drive delay, circuit parasitics and device parameter asymmetries [68] which limits equivalent blocking. To manage voltage imbalance during the transient state different active and passive balancing techniques can be incorporated as shown in Fig. 1.5.

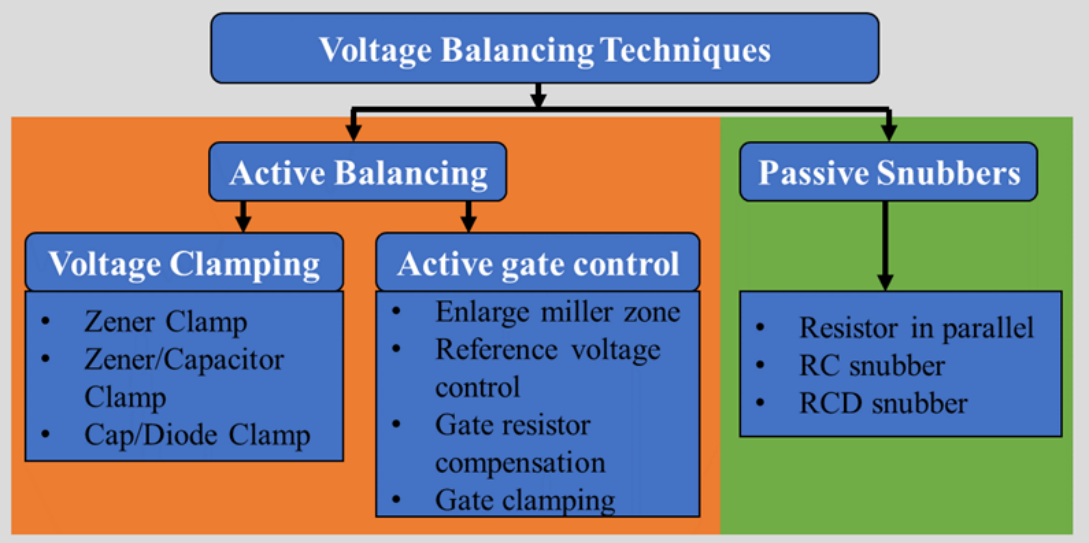


Fig. 1.5: Overview of voltage balancing techniques

The use of passive balancing techniques is the most popular technique for proportioning voltage in the serial connection of power devices. Resistor-Capacitor (RC) or Resistor-Capacitor-Diode (RCD) snubbers can be used in parallel to the power devices and the value of resistors and capacitors can be adjusted to obtain the desired blocking voltage per device [69]. However, for an HV serial string, large snubber capacitors minimize voltage unbalance but increase both power loss and commutation time of the device. The long commutation time slows down switching and limits operating frequency.

Another technique is active balancing which can be further subdivided into voltage clamping and active gate control. In active gate control, gate charge is controlled by a control circuit according to the voltage unbalance which increases or decreases the rate of change of drain-source voltage [70]. This technique increases complexity in the gate drive circuit and requires high-speed sensitive devices. Complexity often increases component count and decreases the overall reliability of the switch. Other active voltage clamping techniques include adding zener diodes in parallel to the power devices to clamp the drain-source voltage. The addition of zener clamps is simple and easy to implement and requires no complex analog/digital circuits [71]. However, one limitation of the method is that it increases power loss in the first device as it experiences higher current and voltages till the other devices turn off. This limits voltage scalability and reduces application efficiency.

Summing up, a good reliable voltage balancing technique should trade-off between active and passive methods and have the minimum number of components, simpler gate control circuit and should also minimize the device switching losses.

1.4 SuperCascode Power Switch Evolution

The SCPS was first reported by Friedrichs in 2003 [72] and uses self-triggering, normally-on, serially connected, SiC JFETs triggered sequentially by a single serial Si MOSFET and a balancing network as shown in Fig. 1.6. The balancing network consists of five low-power *avalanche*-rated Si diodes [73]. Subsequently, newer SuperCascode structures were reported which used passive balancing components resistors and capacitors, shown in Fig. 1.6 and reported superior switching to Friedrichs SCPS performance. Further discussion on each design, advantage and disadvantage is given below.

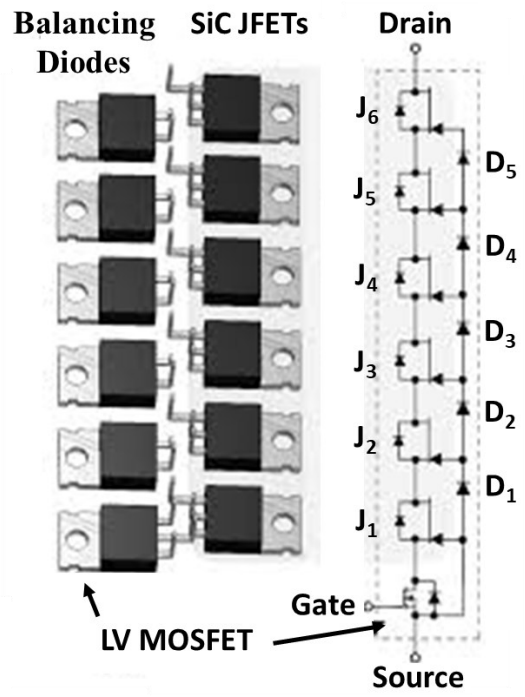


Fig. 1.6(a): Friedrichs SCPS [72]

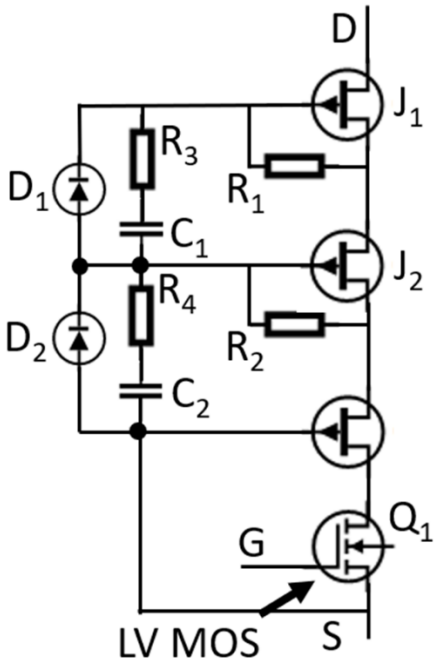


Fig. 1.6(b): Biela's SCPS [74]

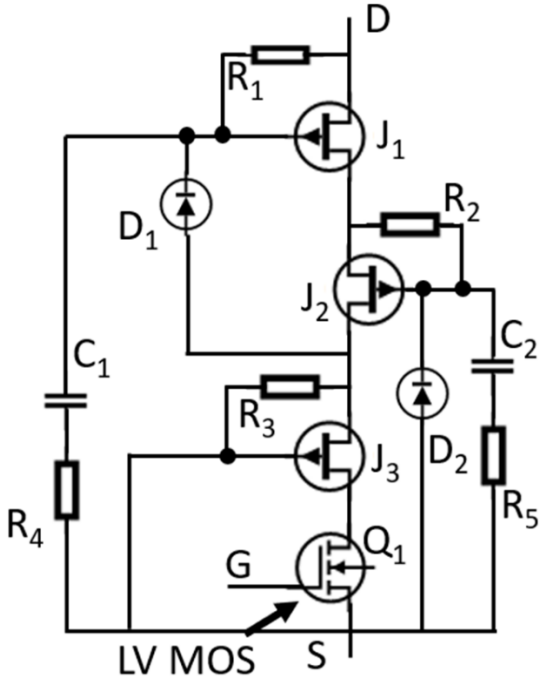


Fig. 1.6(c): Li's SCPS [75]

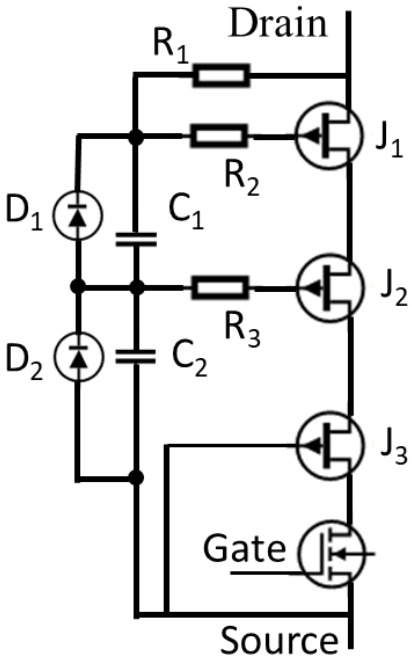


Fig. 1.6(d): Gao's SCPS

In Friedrichs SCPS (shown in Fig. 1.7), the static voltage distribution in the OFF state is dependent on the avalanche voltage of the passive balancing diodes, D_1-D_5, and leakage current through the diodes. The resistance and JFET pinch-off voltage regulate leakage current during the OFF state.

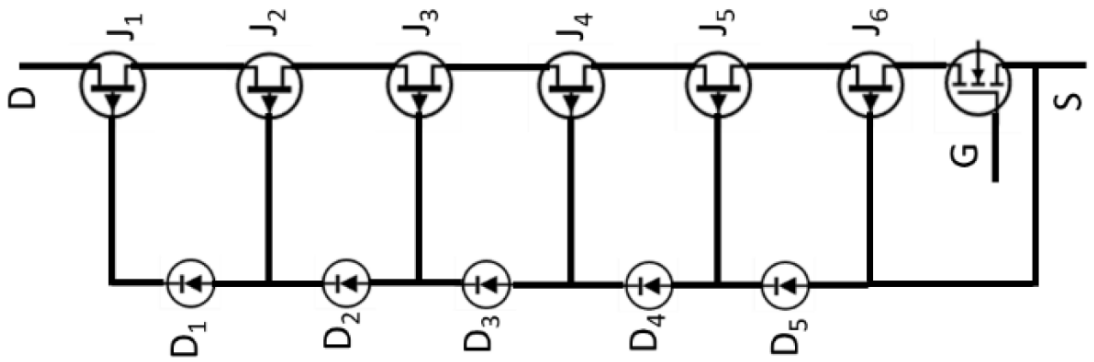


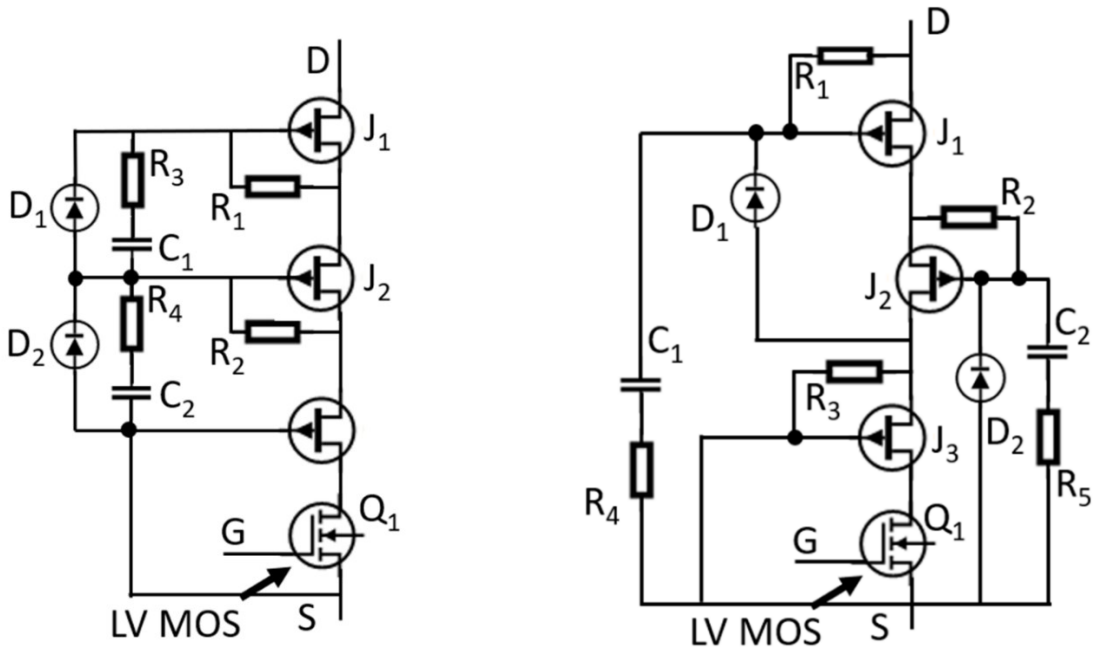
Fig. 1.7: Schematic of Friedrichs SuperCascode consisting of six series-connected SiC JFETs and a low-voltage Si MOSFET [72]

The SCPS shown in Fig. 1.7 consists of *6* SiC JFETs, J_1-J_6 connected in a serial string along with a Si LV MOSFET, Q_1. The balancing network comprised of avalanche diodes D_1-D_5 manages the static voltage distribution in the OFF state. The SCPS is controlled only via the gate of the LV MOSFET, Q_1. When Q_1 turns ON, the gate and source of the J_6 have a voltage differential much greater than the negative threshold voltage required to turn off the normally-on device. The diodes D_1-D_5 ensure that the gate-source voltages are less than $-V_F$ (pinch-off voltage of the JFET) required to turn off the device. The $V_{F,G}$, which is the forward voltage of the gate-source *p-n* junction of the JFET, depends on the leakage current distribution in the JFETs and diodes. To reduce the dependence of the $V_{F,G}$ on leakage current, additional elements are needed as discussed in the next section.

To turn off the SCPS, the LV MOSFET is turned OFF, J_6 gate-source voltage decreases until the channel pinch-off is achieved. Then J_6 turns off and blocks the rising SCPS drain-source

voltage until the avalanche voltage of diode *D5* is reached. At avalanche, the J_5 gate potential with respect to the source of SCPS becomes fixed and the J_5 source potential increases driving a negative gate-source voltage till the bias at the source of J_5 pinches off J_5. Similarly, *J1-J4* turns off sequentially. The structure reports 100ns and 180ns voltage rise and fall time respectively and less than 40ns current rise and fall time. Compared at the same voltage and current range, the Friedrichs SCPS is faster than Si IGBT with 3860 ns voltage rise and 410 ns voltage fall time [73].

The turn-on voltage distribution across the JFETs is dependent on close matching LV devices. Thus, to guarantee leakage and make operating voltage independent of power device parameters, resistors can be connected between the gate-source of JFETs (Fig. 1.8(a)). The overshoot can also be addressed by synchronizing the switching of JFETs with voltage balancing capacitors and creating a charge balance by using a voltage balancing technique. To improve switching speed, the Kolar team (Biela, et al.) from ETH in 2009 [74] and Xeuqing Li [75], employed a dynamic balancing network in parallel to the static balancing network, as shown in Fig. 1.8(a) and Fig 1.8(b) respectively.



(a) (b)

Fig. 1.8: Schematic of (a): Biela's SuperCascode power switch [74] and (b) Li's SuperCascode power switch [75]

Biela's basic SCPS operating principle is similar to Friedrichs. In the structure (Fig. 1.8(a)) R_1, R_2, D_1 and D_2 define the voltage stress on JFETs J_1-J_3 during turn-off. The switching slew rate is controlled by the RC network, comprising of R_3, C_1 and R_4, C_2. Capacitor C_1 supports all the charge of the J_1 gate, C_2 supports all the charge of J_2 gate, plus the charge flowing from C_1. The charge, ΔQ, on C_1 and C_2 in the first and second stage are:

$$\Delta Q_{C1} = Q_{G1} - Q_{D1} \tag{1.1}$$

$$\Delta Q_{C2} = \Delta Q_{C1} + Q_{G2} - Q_{D2} \tag{1.2}$$

Here, Q_G is the gate-to-source charge of the JFET (Q_{GS}+Q_{GD}) and Q_D is the anode-cathode charge of the avalanche diode. The capacitance of the nth capacitor in the balancing network are calculated from,

$$C_n = n * \frac{(\Delta Q_{Cn})}{V_{DS}} \tag{1.3}$$

Here, V_{DS} is the drain-to-source blocking voltage of each JFET of the respective JFET with all JFETs assumed to have the same V_{DS}, and n is a variable that varies from $1 \ldots N\text{-}1$, N is the number of serial JFETs in an SCPS string. Biela's SCPS was able to reduce the static voltage balancing mismatch reported in Friedrichs structure by matching leakage currents through the JFET forcing static equilibrium. However, the following limited voltage scalability of the structure.

a) The blocking voltage of each JFET during turn-off is dependent on I_{DS} leakage current of the "upstream" JFET, which has an inherent manufacturing tolerance.
b) Balancing capacitor value and charge requirement scale linearly with the number of JFETs in the SCPS string increasing network loss and decreasing switching speed.

For Fig. 1.8(a), starting at the topmost capacitor C_1, i.e. the capacitor at the highest voltage potential relative to the ground, the capacitance value scales as $C_n = n*C_1$ where "n" is the number of JFETs in the string and "$n\text{-}1$" capacitors. As an example, let $Q_{C1} = 300nC$ for Biela's SCPM with six JFETs, i.e "$n=6$" and each JFET blocks $1kV$. Then, $C_1 = 300, C_2 = 600, C_3 = 900 \ldots C_5 = 1500pF$. Biela's SCPS topology reports $50\ ns$ and $35\ ns$ voltage rise and voltage fall time respectively [74].

Li's SCPS, shown in Fig. 1.8(b) overcame the limitation reported in Biela's structure by modifying balancing network components. In Li's SCPS structure, capacitor C_1 supports all charges into and out-of-the J_1 gate, C_2 supports all the charges into and out-of-the J_2 gate and so on. The charges, ΔQ, in C_1 and C_2 in the first and second stage are:

$$\Delta Q_{C1} = Q_{G1} - Q_{D1} \tag{1.4}$$

$$\Delta Q_{C2} = Q_{G2} - Q_{D2} \tag{1.5}$$

The n^{th} capacitance in balancing network is calculated from,

$$C_n = \frac{(\Delta Q_{Cn})}{n * V_{DS}} \tag{1.6}$$

Since Q_{Cn} is dependent on the n^{th} JFET and avalanche diode, the capacitor is expected to support only the charge of one JFET, but should block *"n"* times voltage from $J_3 - J_1$ relative to ground. For example, as shown in Fig. 1.8(b), C_1 should block *3kV* and C_2 block *2kV*. However, this voltage scalability of the structure, such that capacitor blocking voltage scales by *n* times, for example in Fig. 18(d) the *3kV* example shown in Fig. 1.7(b). C_1 should block 3kV, C_2 should block *2kV*. HV capacitors increase the overall footprint of the SCPS leading to less power density. A complicated balancing network causes overlapping wire bonds, creating manufacturing difficulties. Summing up, this scaling in capacitor size limits voltage scalability as it scales linearly with number of devices in the string. Li's SCPS reported 50ns voltage rise and fall time. Dr Gao's dissertation research at NCSU in 2017 [76] developed a new hybrid SCPS (Fig. 1.9) which combines the dynamic balancing network from Biela's SCPS with leakage current limiting resistors from Li's SCPS structure.

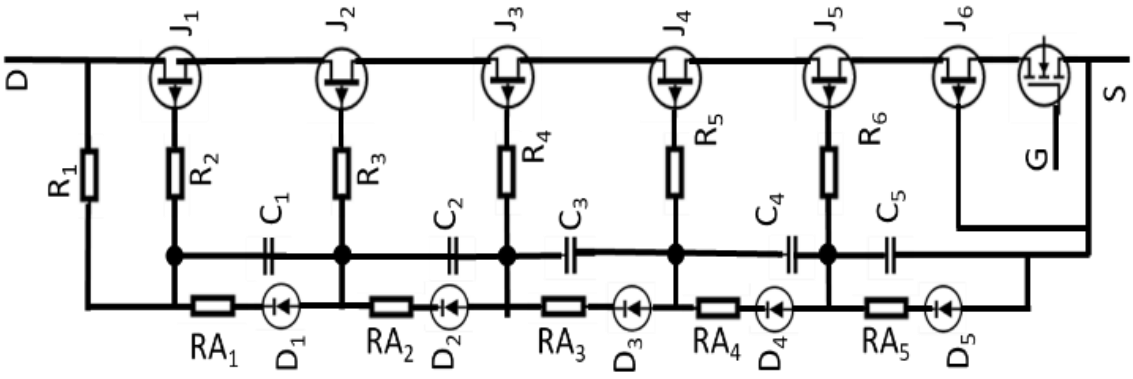


Fig. 1.9: Schematic of Gao's SuperCascode power switch [76]

The SCPS also included additional resistors in series with avalanche diodes to increase avalanche ruggedness. In the structure avalanche diodes, D_1-D_5 defines the voltage stress on the JFETs during turn-off. The C_1-C_5 and R_2-R_6 control switching slew rate, R_1 controls bias leakage current through D_1-D_5 and RA_1-RA_5 divert avalanche current from diodes to JFETs, increasing the avalanche current capability by causing the JFETs to slightly increase drain-source voltage and absorb avalanche energy [77]. However, the following limited voltage scalability and adoption.

a) Charges on the capacitors in the balancing network scale linearly, increasing capacitor size. The charge requirement increases the balancing network switching losses and physical size of the capacitors. the capacitance scales as $C_n = n*C_1$. For example - $C_1 = 300pF$, and $C_2 = 600pF$.
b) Balancing network switch loss is dependent on the number of JFETs in SuperCascode string which is given by:

$$E_{bSCPS} = \frac{1}{4} * (Q_G - Q_D) * V_{DS} * (N^2 - N) \tag{1.7}$$

The approach increases SCPS switching speed and decreases losses compared to the previously reported designs. The linear charge-scaling requirement in the voltage balancing network limits voltage scalability and number of devices in the SCPS string. Switching at *3kV/50A*, Gao's SCPS demonstrated *28ns* and *100 ns* voltage rise and voltage fall time respectively [76].

1.5 WBG power packaging consideration

A typical power module structure is shown in Fig. 1.10, that provides a thermal port for heat removal and mechanical mounting support. The dies are attached to a patterned metal-clad ceramic substrate, which is attached to a baseplate and connected to a heat sink or heat

exchanger. The *99.9 %* Al wire bonds electrically connect the source and gate to the package. Bonding wires have large parasitic inductances about 15–30 nH which decreases switching speed and requires an additional snubber circuit to protect the device [78]. The most common packaging approaches use metal-clad ceramics, e.g. Direct Bonded Copper (DBC), and Active Metal Braze (AMB), or use metal-clad organic Insulated Metal Substrate (IMS). Typical ceramic materials are *AlN*, Al_2O_3 or Si_3N_4, which have low coefficient of thermal expansion (CTE) and high thermal conductivity [79,80]. Common attachment materials for power die on the substrate and substrate onto baseplate are solder, sintered Ag and metal loaded epoxies. The baseplates are typically aluminum, copper or aluminum-silicon-carbide (*AlSiC*). The heatsink is attached to the baseplate using thermal interface materials (TIM) or directly incorporated into the baseplate configuration.

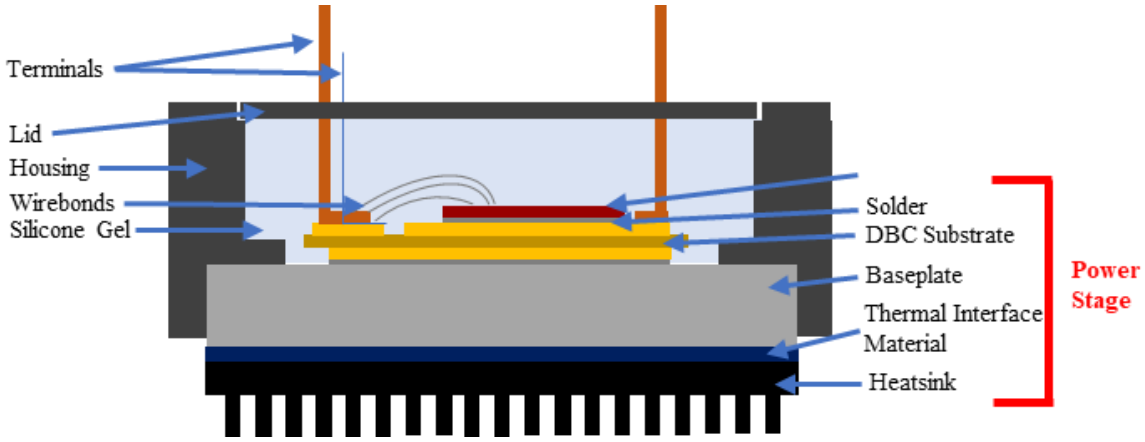


Fig. 1.10: Typical power module structure

1.5.1 State of Art reported power modules

Wolfspeed demonstrated two generation devices packages for *1200V* SiC MOSFETs. The internal and external layout of the 1^{st} generation *62mm* modules are shown in Fig. 1.11 [81]. The wide power terminals are directly soldered onto module to reduce parasitic inductance and uses silicon nitride (Si_3N_4) substrate with AlSiC baseplate to support 175^0C continuous operation

and match coefficient of thermal expansion (CTE) for good mechanical performance under extreme operation conditions. The next generation XM3 package shown in Fig. 1.12 places the *DC+* and *DC-* terminals next to each other to reduce power loop insertion inductance. It uses Si_3N_4 substrate, optimized busbar design and created creepage slots betwwen the *DC+* and the kelvin source terminals to prevent partial discharge and reduce leakage current.

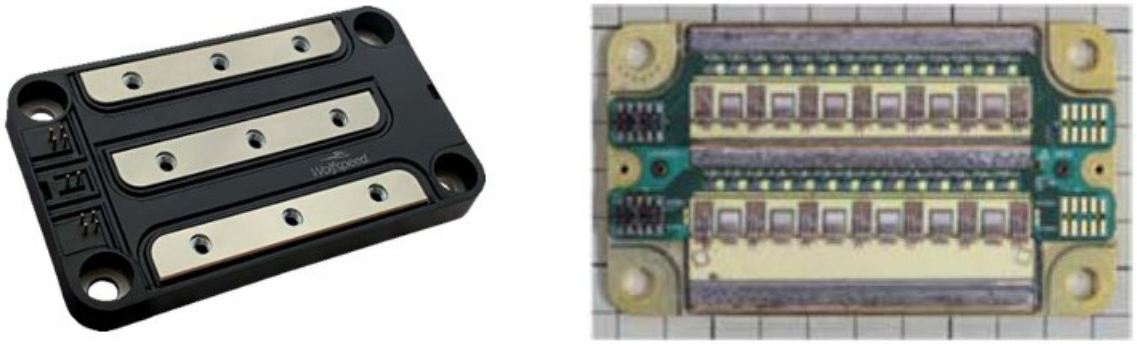


Fig. 1.11: Wolfspeed 62 mm power module (gen 1) (a) External package (b) Open cavity layout [81]

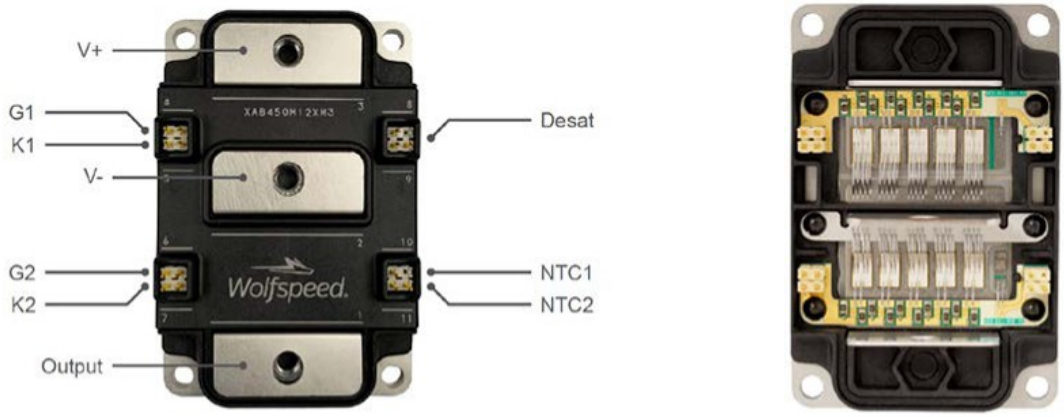


Fig. 1.12: Wolfspeed XM3 low inductance power module (gen 2) (a) External package (b) Open cavity layout [82]

Another way of reducing the interconnect inductance is by utilizing the spacing parallel to the substrate provides interconnects for the returning current path and introduces mutual inductance cancellation. This type of inductance cancellation is utilized by ABB in the *1.2*

kV/700 A. LinPaK package as shown in Fig. 1.13(a) [83]. The module utilizes stacked ceramic substrate structures to planarize the layers and distribute the power and gate signals in different layers. This technique reportedly has only *11 nH* inductance in the power path. Another configuration for inductance cancellation has the power terminals folded back on to the power path as shown in the NCSU *6.5 kV/200 A* super cascode power module in Fig. 1.13(b) [84]. This module configuration reported a *20%* reduction of power path inductance to *23 nH*. A similar concept based GaN high-electron-mobility transistor (HEMT) power module rated *270V/56A* was reported in [85]. The layout in GaN module reported *24%* reduction of power path inductance compared to single-layer layout and reduced inductance to *12 nH*.

Fig. 1.13: (a) ABB 1.2kV/700 A LinPAK [12] (b) NCSU 6.5kV/100 A SuperCascode Power Switch [84]

To enhance thermal performance and reduce parasitic inductance further double-sided wire-bondless power modules were reported in [86]-[88]. The effective thermal performance of the module is increased with double the surface area for heat extraction. The double-sided modules eliminate wire bonds by utilizing press-pack technology, from Westcode [89] or StakPak from ABB [90]. A press-pack SiC MOSFET has also been presented in [91], which combines the advantages of both press-pack package and SiC devices. However, double heatsink included in the power loop, increased the net parasitic inductance higher than *12 nH* and increased the volumetric size greater than SiC power modules [91].

Alternatively, a planar *2-D* structure for decreasing inductance uses an integrated topside connection (i.e., gate-source) and has been previously reported. Power overlay (POL) introduced by General Electric last century showed the capability of *2-D* packaging with *1200 V* IGBT devices [92] as shown in Fig. 1.14(a). The advanced chip on flex POL eliminates wire bonds and uses metalized through holes in flex circuitry to form power and control interconnects. Thermally, the chip on flex creates a planar interface allowing for heat extraction from the topside of the die where the bulk of heat generation takes place. Overall, the POL technology offers high packaging density, lower package parasitics, lower weight and size and higher reliability [93].

Semikron introduced the SkiN package structure [94], the technology replace solder joints and bond wires by silver diffusion sinter joints to significantly improve pulsating power capability and continuous high current operation. A *1200 V/400 A* SiC SkiN is presented in [95] with commutation loop inductance less than *5 nH*. The planar-bond-all (PBA) package was introduced by Oak Ridge National Lab (ORNL) as shown in Fig. 1.14(b), has power devices sandwiched between two DBC substrates [96]. The PBA package utilizes planar, large area bonds instead of multiple wire bonds to form the top interconnect. The PBA module reduced the parasitic related inductances by *75%* (*50.3* versus *12.8* nH) and resistance by *10%* (*23.5* versus *2.2* mΩ) compared to conventional modules [97]. However, the double-sided power modules and POL, PBA application has been reported to *1.2kV-1.7kV* voltage range. All these methods require solderable top-side power devices which are commercially non-available limiting wide usage for high power applications.

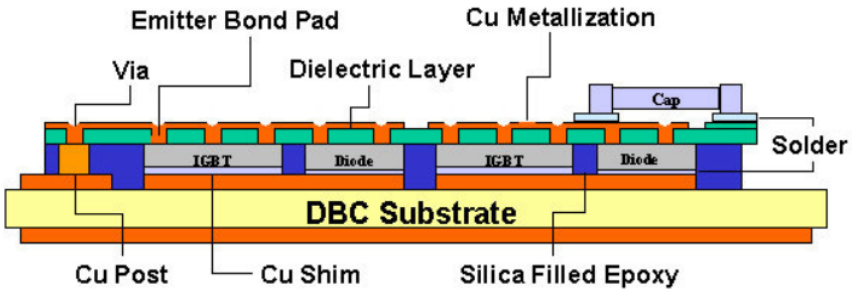


Fig. 1.14(a): IGBT Half bridge module using power overlay technology (POL) [92]

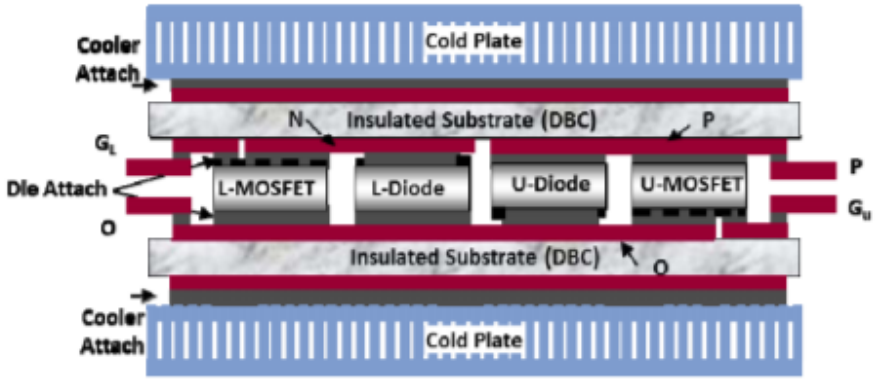


Fig. 1.14(b): Exploded schematic of planar-bond-all (PBA) module [97]

1.5.2 High Voltage power packaging

For HV power devices only single switch multi-parallel die power modules have been reported as of 2021 by GeneSiC, Fuji Electric, Wolfspeed and Mitusbishi in the *3.3-10kV* voltage range, shown in Fig. 1.15 [98]-[101]. The modules have special creepage patterns for external voltage isolation and a thick substrate for voltage isolation. Key application areas are device development and characterization.

(a) (b) (c)

Fig 1.15: Commercial available single switch HV power modules (a) *3.3kV* GeneSiC (b) *6.5kV* Mitsubishi (c) *10kV* Mitsubishi

(a) (b)

Fig. 1.16: Research prototypes for half-bridge power modules (a) 10kV SiC MOFET (b) 15kV 80A SiC IGBT module

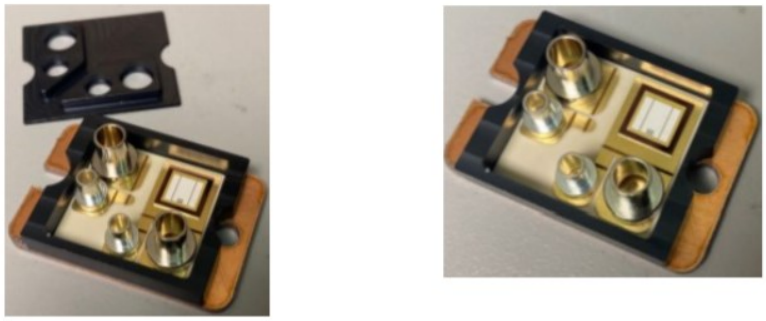


Fig. 1.17(a): 6.5 kV SOT-227 DBC Module with Cu baseplate and 5/25/5 mil Al_2O_3 DBC

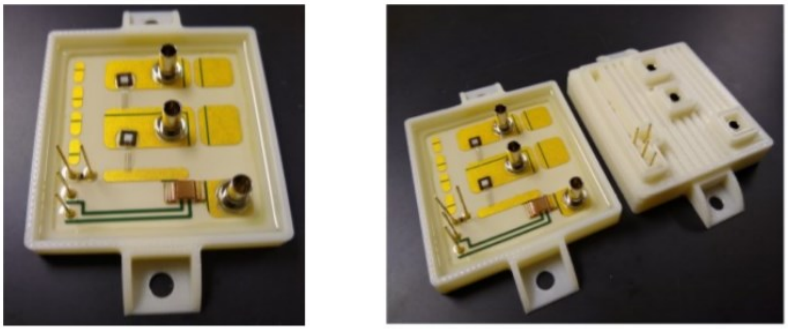


Fig. 1.17(b): 15 kV Half-Bridge power module with 12/40/12 mil AlN DBC

Open-cavity developmental test packages (shown in Fig. 1.17) to characterize HV 3.3-15kV power devices have been reported in [102]. These models have the same special creepage housing slots and *AlN* substrate for high voltage isolation. Research prototypes of a *10kV* and a *15kV* SiC IGBT half-bridge power module are shown in Fig. 1.16(a) and (b) respectively [103]. However, the utilization of a single substrate leads to a high leakage current during normal operation due to stray parasitic capacitance and high thermal resistance. Other disadvantages include bulky size compared to the semiconductor chip size and area per die in commercial power modules and high parasitic inductance which limits switching speed. All these together limit the overall advantages of the HV WBG power devices, creating the way for alternative and novel technologies.

1.6 Challenges in HV packaging

WBG devices with low C_{OSS} and Q_G allow switching transients at high *dv/dt* and *di/dt* enabling high-frequency operation, increasing power density and efficiency, and reducing converter size. However, fast switching speed also make the module design and performance of the device more sensitive to module design, parasitic control and operation. Thus, to capture full benefits of WBG performance in application an advanced power packaging approach with new materials are required which requires optimization around unit-cell architectures [104]. Key design points in designing a WBG power module design are listed below :

a) The packaging layout should be designed to minimize stray parasitics, symmetric for multi-die module layout, and should meet all isolation, clearance/creepage, and manufacturing guidelines and qualifications. Parasitic inductance in the power path adds to voltage overshoot and in the gate driving loops adds to oscillations in the driving circuitry, leading to false triggering, etc. Parasitic capacitance in the power path adds to common-mode (CM)

current, EMC issues, etc. Similarly, a non-symmetric layout can lead to a mismatch in triggering parallel dies, which can lead to current imbalance due to delays in triggering, etc.

b) The module should contribute minimally to forward voltage drop terminal-to-terminal. The module structure should contain a dielectric substrate that is sufficiently thick to provide HV isolation, while simultaneously not significantly adding to the net junction-to-case thermal resistance. Other considerations are CTE, elastic modulus, and change of material properties under continuous switching transients.

c) Advanced packaging materials like organic substrates, epoxy encapsulants, etc. can be utilized to develop new structures, as long as they are capable of operating continuously under high extreme working temperatures (e.g. to *-40 ^{0}C to 175 ^{0}C*) without degradation of material properties as a function of temperature, lifecycle, etc. For example, materials like *PEEK* (polyetheretherketone) and *ABS* (Acrylonitrile Butadiene Styrene) can be used to fabricate low-cost housing bodies using *3D* printing technology. The material selection should be optimized to increase manufacturability and decrease the cost for mass production.

Research Motivation and Objective

This research discusses a novel HV power switch and its power packaging. It has two main objectives described as :

1. This research proposes a new Cascaded SuperCascode (CSC) switching topology that scales to very high voltages (*>100kV*) or is applied to optimize previously reported MV SCs to achieve higher switching speed, reduced balancing network size and lower switching losses. The research also discusses practical challenges in switch design such as stray inductances which lead to delays in triggering serial devices, de-synchronization of triggering and

unexpected overvoltages that limit scalability. This work also provides an analytical model to enable optimization through simulation and provides experimental data verifying the model.

2. Next, a new packaging approach called the "segmented baseplate" approach to HV power packaging is proposed for elevated thermal, mechanical, electrical performance and low cost. The approach removes the common metal baseplate, uses an epoxy organic laminate material with thermal vias to achieve a direct heat transfer path. The research tradeoff the thermal resistance to substrate capacitive coupling by using thermal via's, separate electrically hot heatsinks per device and dielectric fluid cooling. The layout also aims at spreading the E-field density throughout the module making a power dense design and utilizes the 2D space to introduce mutual inductive cancellation in the power path.

Structure of the dissertation

In chapter 1, common system applications of High Voltage High Current switches are reviewed and discussed which provide guidance for new switching topologies. Then current state of art HV power devices and SuperCascode switching topologies are reviewed, their current implementations and limitations are discussed and the scope of further optimization for improved switching performance and low loss is discussed. The chapter also discusses the challenges and limitations of current High Voltage WBG power packaging which provides guidance for new power module structures.

In chapter 2, new methodologies of cascading and scaling to realize a new CSCPS switching topology is proposed with the aim to reduce switching loss, improve switching speed and reduce auxiliary balancing network size. The chapter discusses the CSCPS principle of operation, design of the CSCPS and proposes an optimization sequence that compares different configurations of CSCPS. The chapter also includes an analytical model which compensates the balancing network

for device tolerances and stray-parasitics that might limit the performance of the power switch, (delay in triggering serial devices, de-synchronization of triggering and unexpected overvoltages that limit scalability).

In chapter 3, the “segmented” baseplate power module is proposed with the aim to reduce thermal resistance by transferring the voltage isolation to the next level of power packaging. The chapter proposes a process for building a Cascaded SuperCascode power module by using the “segmented” baseplate packaging and exploiting the commutation lower inductance cancellation. A 6-JFET 2S-3C CSCPS is built, with the parasitic inductance simulated in Ansys Q3D and thermal resistance or performance simulated in COMSOL. With the parasitics extracted from the ERCD layout, circuit simulation is performed in Ltspice to validate the dynamic and static performance of the module.

In chapter 4, a 6kV/20A using discrete TO-247 power devices is fabricated and tested. Both static characterization and dynamic testing in a double pulse tester (DPT) are performed. To test the modules under condition that resembles real-world application conditions, the DPT controller generates a number of pulses before the main to precharge and pre-DPT pulses in order to equalize the static balancing network. To make the DPT signal generator a truly universal DPT test signal generator, the number and duration of pre-main pulses, as well as the main pulses, are all user-programmable.

CHAPTER 2: Cascaded SuperCascode Power Switch

A SuperCascode Power Switch (SCPS) consists of a voltage blocking circuit comprised of series-connected depletion mode power devices, and an auxiliary balancing network comprised of active and passive devices. The network is tuned to manage the electrical and switching performance of the SCPS. The circuitry should energize and de-energize the gates of the power devices, serially trigger and manage voltage stress equally among devices in the serial string, and act as a snubbing circuit to dynamically limit device overvoltage.

All previously reported SCPSs use a balancing network, whereas the number of devices scale either the blocking voltage requirement per component scales or the components in the lower stages have to support the additional charge of the devices in the upper half of the SC string causing linear-charge scaling, negatively affecting component size, device losses, scalability, etc [73]-[76]. The SCPS structures reported in [73]-[76] lacks voltage scalability due to increasing switching loss and capacitor form factor in the balancing network. The sizing of the SCPS balancing network components is dependent on the way charge flows into and out of the JFET gates in the four structures introduced earlier. To understand the net balancing network charge requirement and correlate the charge requirement to the physical form factor of the capacitors for packaging, a Cost Factor (CF) is introduced. Note: Cost Factor (CF) is equivalent to the net charge of the capacitor and can alternative represented as net balancing network capacitance time each capacitor blocking voltage.

For Gao's SCPS, the net balancing network switching loss and the CF scales with respect to the number of devices as shown in (2.1) and (2.2) respectively.

$$E_b = \frac{1}{4} * (Q_G - Q_D) * V_{DS} * (N^2 - N) \tag{2.1}$$

$$CF = \sum_{k=1}^{N-1} k * (Q_G - Q_D) \tag{2.2}$$

Here, Q_G is the gate charge of JFET i.e the summation of gate-drain charge, Q_{GD} and gate-source charge, Q_{GS}; Q_D is the anode-cathode charge of avalanche diode, V_{DS} is the drain-source blocking voltage per JFET and *N* is the number of JFETs in an SCPS string. For an *N*-string SCPS, there are *N-1* stages of balancing capacitors. Using (2.1) and (2.2), the capacitance and loss scaling challenge for a device with $Q_G = 300\ nC$, $Q_D = 0\ nC$ and each block *1kV* (V_{DS}) are summarized in Table 2.1.

Table 2.1: SuperCascode net capacitance and loss scaling with the number of JFETs in SC string

Number of JFETs in SC string (N)	Cost Factor (nFV)	Switching Loss (mJ)
1	-	-
2	300	0.15
3	600	0.45
4	1800	0.9
5	3000	1.5
6	4500	2.25

As shown in Table 2.1, the net capacitance and switching loss scales *15x* with the number of devices in the string; and *N* increases from *2* to *6*, which scales both the balancing network form factor and loss generated by the power switch in operation. This exponential scaling with the number of devices in the serial string limits voltage scalability of the existing SCPS structure reported by Gao.

2.1 Philosophy of Cascaded SuperCascode Design

This research overcomes this scaling problem, by proposing a novel Cascaded SuperCascode power switch designed using a multi-layer cascaded network approach. The approach periodically and optimally breaks down the linear charge scaling in the balancing network and resets *N* forming cascades. This partitioning of the balancing network modifies the JFET gate energizing and de-energizing path.

The intention of the Cascaded SuperCascode multi-cascade or multi-layer balancing approach is to achieve near-infinite voltage scalability (baring practical limitations discussed in Section 2.12), improve switching speed and reduce switching losses. If the selection of which capacitors (of balancing network) triggers which serial device is optimized and fine-tuned for performance, it will lead to the fastest and most efficient SCPS topology to date.

This chapter describes the philosophy, design, explains switching performance, simulation verification, design optimization, compares different CSCPS structures and lists practical challenges in hardware implementation and the way to overcome those.

2.2 Cascaded SuperCascode Power Switch Approach

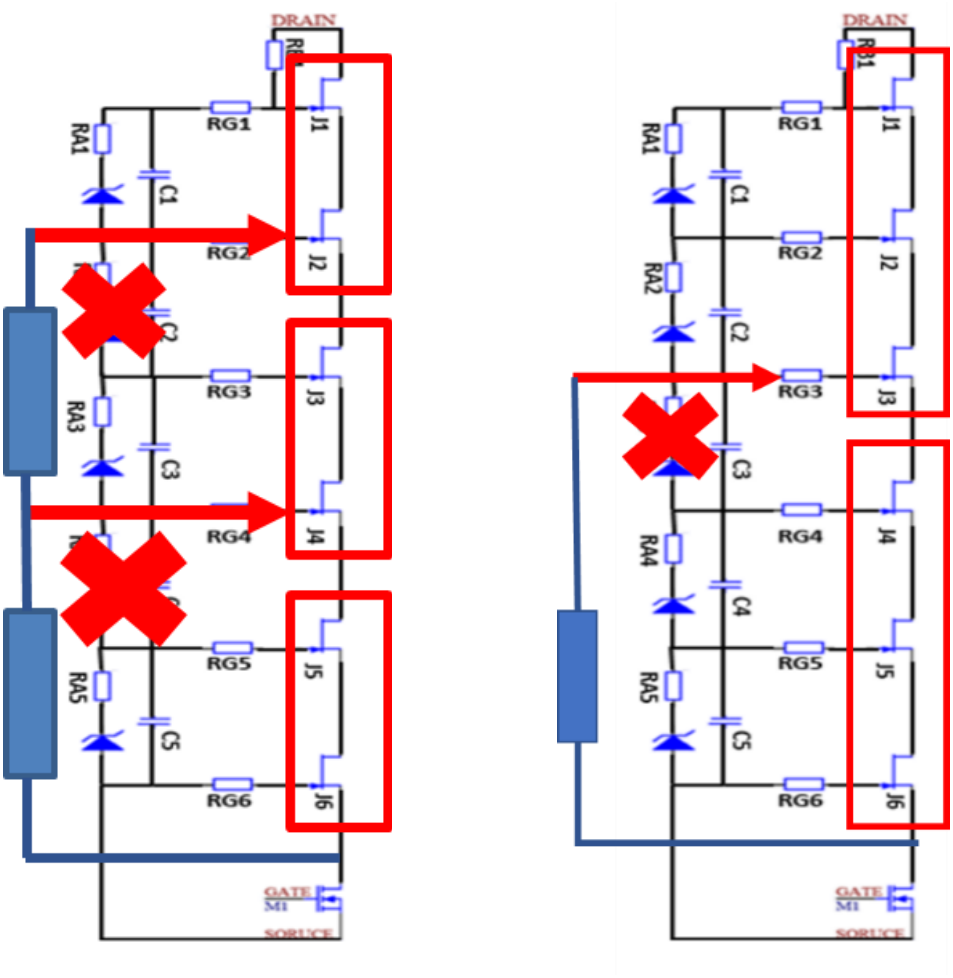
The CSCPS approach replaces the Si MOSFET and uses the JFET to control a SuperCascode cell referred to as a Unit SuperCascode (USC) (red box in Fig. 2.1). Each USC has an internal balancing network. Multiple USCs are serially connected to form a CSCPS, wherein each USC is triggered by an external network layer comprised of a capacitor, gate resistor and avalanche diode (blue box in Fig. 2.1).

Multiple CSCPS switches are possible from any *N* number of JFETs in a serial string. Let '*m*' be the number of JFETs in series forming a USC and '*n*' be the number of USCs connected in series forming a CSCPS. For any *N*-JFET CSCPS, multiple whole number values of '*m*' and '*n*' can exist as long as 'm' and 'n' are divisors of *N* and satisfy the following relationship :

$$m\,X\,n = \frac{V_S}{V_{DS}} = N \tag{2.3}$$

Here, V_S is the CSCPS rated voltage and V_{DS} is the per JFET blocking voltage. For example, for a *6* serial JFET, single layer Cascaded SuperCascode configuration, two possible configurations are the "*2S-3C"* and "*3S-2C"* as shown in Fig. 2.1(a) and Fig. 2.1(b) respectively.

In the "*2S-3C"* implementation, *2* JFETs are series-connected to form a USC, i.e. "2S" and *3* USCs are connected in series to form a Cascaded SuperCascode,i.e. "3C". In the *3S-2C* implementation, *3* JFETs are series-connected to form a USC "3S" and *2* USCs are connected in series to form a Cascaded SuperCascode "2C". In *2S-3C* CSCPS, J_2 and J_4 gates are charged by an external balancing network whereas in *3S-2C* CSCPS J_3 gate is charged by the external balancing network.



(a) (b)

Fig. 2.1 (a): 1-layer 2S-3C 6-JFET Cascaded SuperCascode Power Switch, (b): 1-layer 3S-2C Cascaded SuperCascode Power Switch

2.3 Design of 1-layer Cascaded SuperCascode

A *1*-layer *2S-3C* CSCPS is shown in Fig. 2.2. The utility of each passive and active element in the balancing network is discussed in this section.

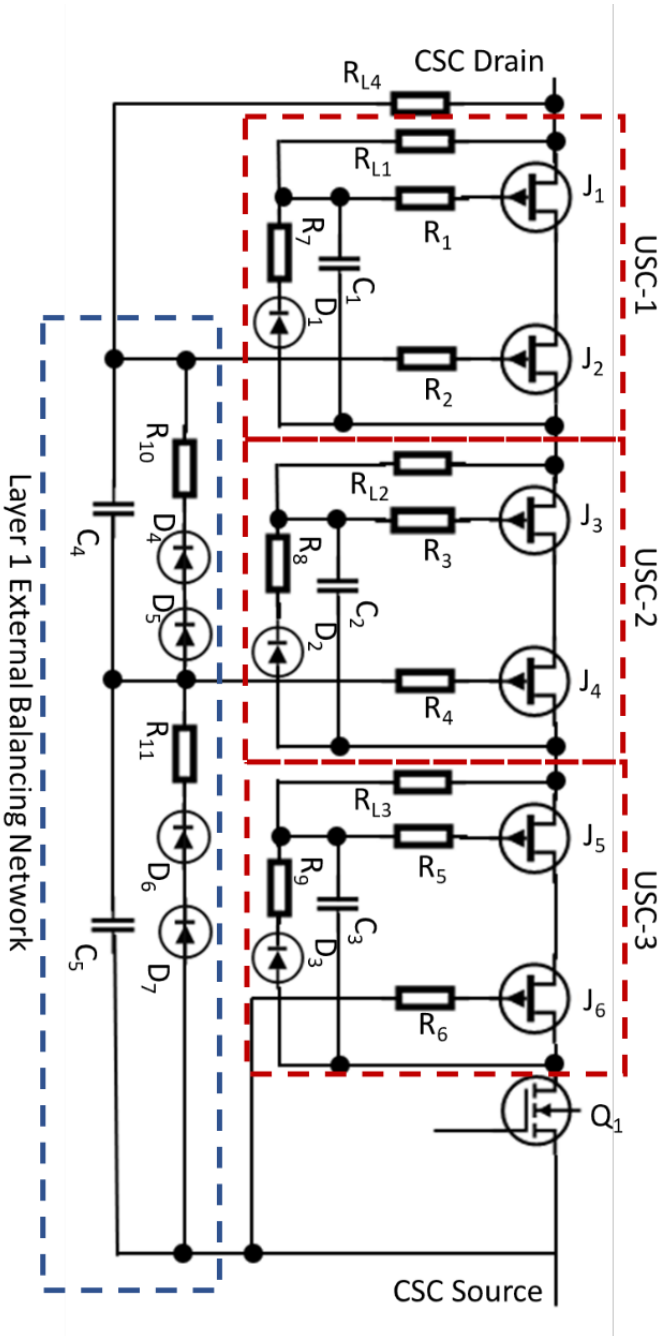


Fig. 2.2: Schematic of Cascaded SuperCascode power switch consisting of six series-connected SiC JFETs and a low-voltage Si MOSFET

In Fig.2.2, each USC consists of *2* JFETs in series and *3* USCs are connected in series to form a CSCPS. The passive components inside the USC manage the device switching internal to the USC and the "layer-1" external balancing network manages the switching of the 3 USCs. The balancing circuit internal to a USC-1 comprises C_1, R_1, D_1 and R_{L1}. The capacitor C_1 provides a current path for charging and discharging the reverse transfer (C_{rss}) capacitance of J_1 and synchronizes turn-on and turn-off of J_1-J_2. Similarly, C_2 and C_3 synchronize switching of J_3-J_4 and J_5-J_6 respectively. The gate resistor R_1 with C_1 together controls the switching slew rate of J_1. The avalanche diode D_1 clamps the gate potential of J_1. Similarly, D_2 and D_3 clamp the gate potential of J_3 and J_5 respectively. The resistor R_{L1} and the blocking voltage of J_1-J_2 together determine the bias current of D_1 for USC-1. This removes the dependency of the bias current from the number of devices in the serial string and JFET parameters, such as leakage current and threshold voltage. This is suitable for mass-production of Cascaded SuperCascodes and requires no pre-selection of JFETs. The resistors R_{L2}-R_{L3} manage the bias current for diodes D_2-D_3 in USC-2 and USC-3 respectively.

The layer-1 external balancing network comprises of R_{L4}, D_4-D_7, C_4-C_5, R_2, R_4 and R_6. The capacitor C_4-C_5 provides a current path for charging and discharging the reverse transfer (C_{rss}) capacitance of J_2 and synchronizes turn-on and turn-off of all USCs. The gate resistors R_2, R_4 and R_6 together with C_4-C_5 control the switching slew rate of all USCs. The resistor R_{L4} controls the leakage current through avalanche diodes to maintain equivalent turn-off blocking voltage across each USC. The 2S-3C CSCPS is shown in Fig. 2.2, herein the component selection and placement of the passive balancing components are optimized for switching speed. The topology has *2* JFETs in each USC building block with *3* identical USCs in series, with a layer-1 external balancing capacitor to form a 2S-3C configuration. The balancing circuit is comprised of

1. Clamping diodes (or avalanche diode), D_1-D_7 that limit the V_{DS} of the JFETs to an avalanche voltage, V_{aval}
2. Balancing capacitors, C_1-C_5 and resistors, R_1-R_6 control the switching slew rate. In synchronous switching, when the LV MOSFET turns on, the gate-source voltage of J_6 decreases and normally-on J_6 continues to conduct when gate voltage as $V_{GSJ1}>V_{th}$. With J_6 conducting, the source potential of J_5 increases. Capacitor C_3 fixes the gate potential of J_5 for a limited time, such that V_{GSJ2} starts to decrease leading to synchronous switching. Similarly, C_5 synchronizes the switching of *USC-3* and *USC-2* and C_4 synchronizes the switching of *USC-2* and *USC-1*.
3. Resistors, R_{L1}-R_{L4} control leakage current through avalanche diodes to maintain equivalent turn-off blocking voltages across each JFET.

The CSCPS can be under avalanche because of leakage internal inductance, input surge, voltage imbalance between serial devices, etc. In CSCPS operation, the static per-stage voltage is defined by avalanche diodes, which breakdown when per-stage voltage is excessive. Thus resistors, R_7-R_{11} are added in series with the avalanche diodes to increase avalanche ruggedness by diverting avalanche current from diodes to JFETs, thus sharing transient energy.

2.4 Mathematical Foundation of Cascaded SuperCascode Power Switch (CSCPS)

Each Unit SuperCascode (USC) has series-connected depletion-mode devices with a balancing network forming a SuperCascode without the LV MOSFET control switch. The "cascaded stage" in the CSCPS uses the lower JFET of a USC to control the "USC" building block. Multiple cascaded stages or external balancing networks can be connected in parallel to form a CSCPS and to drive theoretically infinite USCs.

2.4.1 Design of Unit SuperCascode Balancing Network

Fig. 2.3 similar to Fig. 2.1 shows a '*2* Series' '*3* Cascade' implementation using the CSC concept to realize a *6* JFET optimized power switch. The Fig. 2.3 topology is also the same as Fig. 2.2 but relabelled for mathematical consistency. The CSCPS has three USCs, which together with the external cascaded balancing network, compose the 2S-3C CSCPS. This section discusses the components internal to the USC (dotted box). The USC has an "*m*" number of JFETs in series.

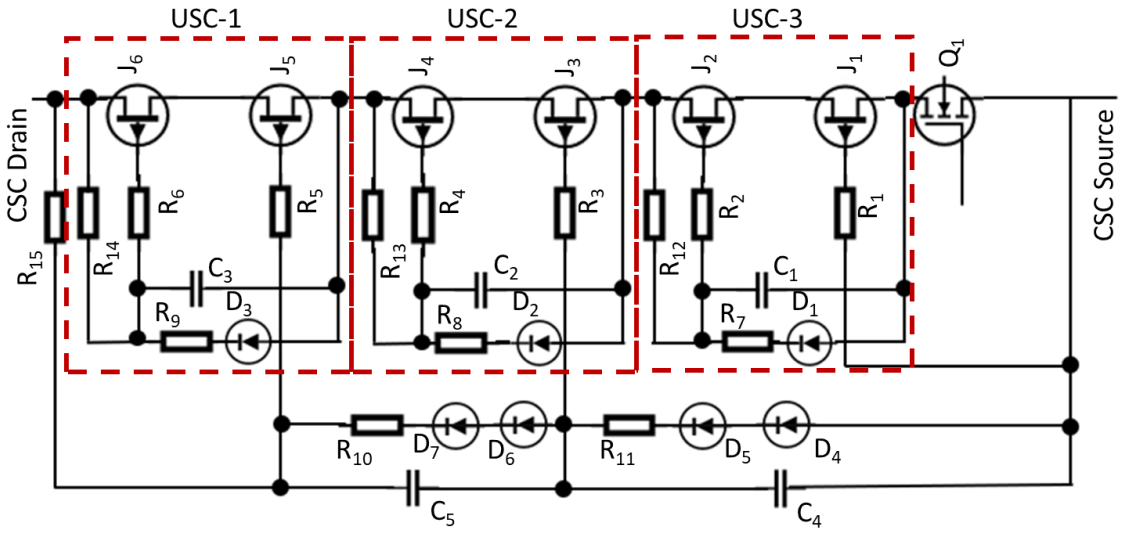


Fig. 2.3: Schematic of a *2S-3C* Cascaded SuperCascode Power Switch structure

In the *USC-3*, R_{12} provides a bias current for D_1 which sets the static balancing voltage. The resistor set R_1-R_2 controls the rise and fall times of J_1 and J_2 whereas C_1 is sized based on the sum of gate-to-source and gate-drain charges of JFETs, J_1-J_2 and body charge of D_1. In a perfectly balanced system where voltages across all JFETs and diodes are respectively identical, the charge on the balancing capacitor C_1 can be calculated as:

$$Q_{Cm} = m * (Q_G - Q_D) \tag{2.4}$$

Here "*m*" is the number of JFETs, Q_G is gate charge of JFET (Q_{GD}+Q_{GS}) and Q_D is the anode-cathode charge of avalanche diode. The balancing network capacitance C_1 can be calculated by Eq. 2.5; for an *m*-stage USC where there are *m-1* stages of balancing capacitors. The net USC balancing capacitance is

$$C_m = \sum_{j=1}^{m-1} \frac{j * (Q_G - Q_D)}{V_{DS}} \tag{2.5}$$

where, C_m is USC balancing network capacitor and V_{DS} is the drain-to-source voltage per JFET. The energy stored in USC capacitors is

$$E_{Cm} = \frac{1}{2} * C_m * {V_{ds}}^2 \tag{2.6}$$

The total balancing network capacitive net energy loss per USC, E_{bu} can be approximated using the gaussian formula in (Eq. 2.7). This is the net energy loss per *m-stage* JFET USC, and is equivalent to sum of the energies stored in *m-1* capacitors.

$$E_{bu} = \sum_{1}^{m-1} E_{Cm} = \frac{1}{4} * (Q_G - Q_D) * V_{DS} * (m^2 - m) \tag{2.7}$$

2.4.2 Design of External Balancing Network

In the cascading approach, each USC gate is triggered by another external balancing network layer as shown in Fig. 2.3. This section discusses the external balancing network which drives individual USCs. The *3rd* USC control JFET, J_1 is triggered by the control MOSFET, Q_1, *2nd* USC control JFET, J_3 is triggered and controlled by C_4 and diodes D_4-D_5, and *1st* USC control JFET J_5, is triggered and controlled by C_5 and diodes D_6-D_7. The CSCPS has "*n*" USCs series-connected and controlled by an external passive balancing network. In the external balancing network, R_{15} provides additional bias current for D_4-D_7 which sets the static balancing

voltage. The resistors R_3 and R_5 set rise and fall times of the USC. C_4 is sized based on gate charge of J_3 and body charge of D_4 and D_5, and C_5 is sized based on the gate charge of J_3 plus charge of J_5 and the body charge of D_6 and D_7. In a perfectly balanced system where voltage across each USC should be the same and all JFETs and diodes are identical. For a *n*-stage CSCPS there are *n-1* stages of balancing capacitors in the external balancing network. The net external balancing capacitance is

$$C_n = \sum_{k=1}^{n-1} \frac{k*(Q_g - Q_d)}{m*V_{ds}} \tag{2.8}$$

where "*n*" is the number of USCs forming a CSCPS, Q_G is gate charge of JFET (i.e. Q_{GD}+Q_{GS}), Q_D is the anode-cathode charge of avalanche diodes (D_4 and D_5), and V_{DS} is drain-to-source voltage per JFET. The energy stored in external balancing capacitors C_n is

$$E_{Cn} = \frac{1}{2} * C_n * (m * V_{ds})^2 \tag{2.9}$$

The total balancing network capacitive energy loss, E_{bc}, of the external balancing network forming the CSC, uses the gaussian formula, and expressed in Eq. 2.10. The E_{bc} is equivalent to sum of the energies stored in *n-1* capacitors.

$$E_{bc} = \sum_{1}^{n-1} E_{Cn} = \frac{1}{4} * (Q_G - Q_D) * (m * V_{DS}) * (n^2 - n) \tag{2.10}$$

The total balancing network loss in the CSCPS is the sum of internal USC switching losses and external cascode balancing capacitors. The *2S-3C* cascade of Fig 2.3 has three USCs, i.e *n=3*. The net balancing switching loss for the entire HV-CSC switch for an "*n*" cascade switch is

$$E_b = (n * E_{bu}) + E_{bc} \tag{2.11}$$

A reduction can be made with Eq. 2.7 and Eq. 2.10 substituted into Eq. 2.11 to obtain

$$E_b = \frac{1}{4} * \left(n * (Q_G - Q_D) * V_{DS} * (m^2 - m)\right) + (Q_G - Q_D) * (m * V_{DS}) * (n^2 - n) \quad (2.12)$$

Further simplifying the total net balancing energy is

$$E_b = \tfrac{1}{4} * mn * (Q_G - Q_D) * V_{DS} * (n + m - 2) \quad (2.13)$$

The Eq. 2.14 shows the net balancing energy loss in the CSC is directly proportional to

$$E_b \propto mn * (n + m - 2) \quad (2.14)$$

To understand the net balancing network charge requirement and correlate the charge requirement to the physical form factor of the capacitors for packaging, a cost factor (CF) is introduced. The CF is the product of capacitor and voltage ratings of the required capacitors in the CSC. Using Eq. 2.5 and Eq. 2.8 the cost factor of the *m*S-*n*C CSCPS can be represented as :

$$CF = \left[\left(n * \sum_{j=1}^{m-1} \frac{j*(Q_G - Q_D)}{V_{ds}}\right) + \sum_{k=1}^{n-1} \frac{k*(Q_G - Q_D)}{m*V_{ds}}\right] * V_{ds} \quad (2.15)$$

$$= \left(n * \sum_{j=1}^{m-1} j * (Q_G - Q_D)\right) + \sum_{k=1}^{n-1} \frac{k * (Q_G - Q_D)}{m} \quad (2.16)$$

When comparing Gao's Fig. 2.1 SCPS with the Fig. 2.3 CSCPS by comparing (2.1) and (2.2) with (2.13) and (2.16), i.e. the CSCPS approach has *40 %* less switching energy loss and achieves *53-60 %* reduction in balancing network capacitance. Multiple configurations are shown in Table 2.2. The equations also show for any *m*, *n* and *N* whole numbers where *N≥4,* the CSCPS has less net switching energy loss than the SCPS approach.

Table 2.2: Comparison of 6-JFET SuperCascode and Cascaded SuperCascode with net capacitance and switching loss			
Design Combination		Balancing Network Loss (mJ)	Charge Requirement (nFV)
JFETs in USC (m)	USCs in series (n)		
1	6	2.25	4500
2	3	1.35	1800
3	2	1.35	2100
6	1	2.25	4500

2.5 Multi-layer Cascaded SuperCascode Design

Section 2.3 discussed the design of a 1-layer CSCPS, but the philosophy of periodically and optimally breaking down the triggering or balancing circuitry can be extended to form multi-layer cascades, e.g. a two-layer *12* JFET CSCPS (Fig.2.4), three-layer *24* JFET CSCPS (Fig. 2.5) and so on.

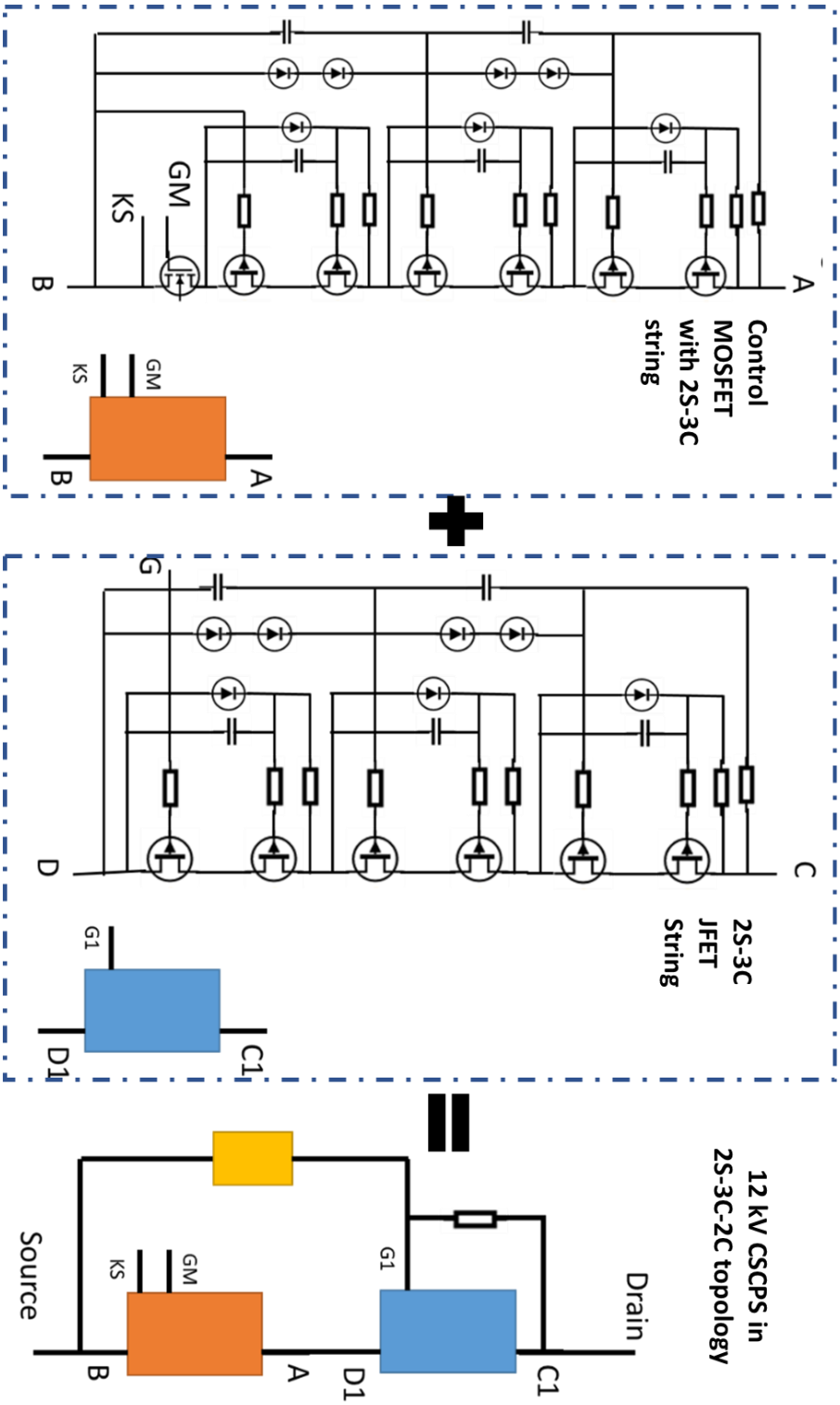


Fig. 2.4: Block diagram of two-layer 12 JFET Cascaded SuperCascode Power switch

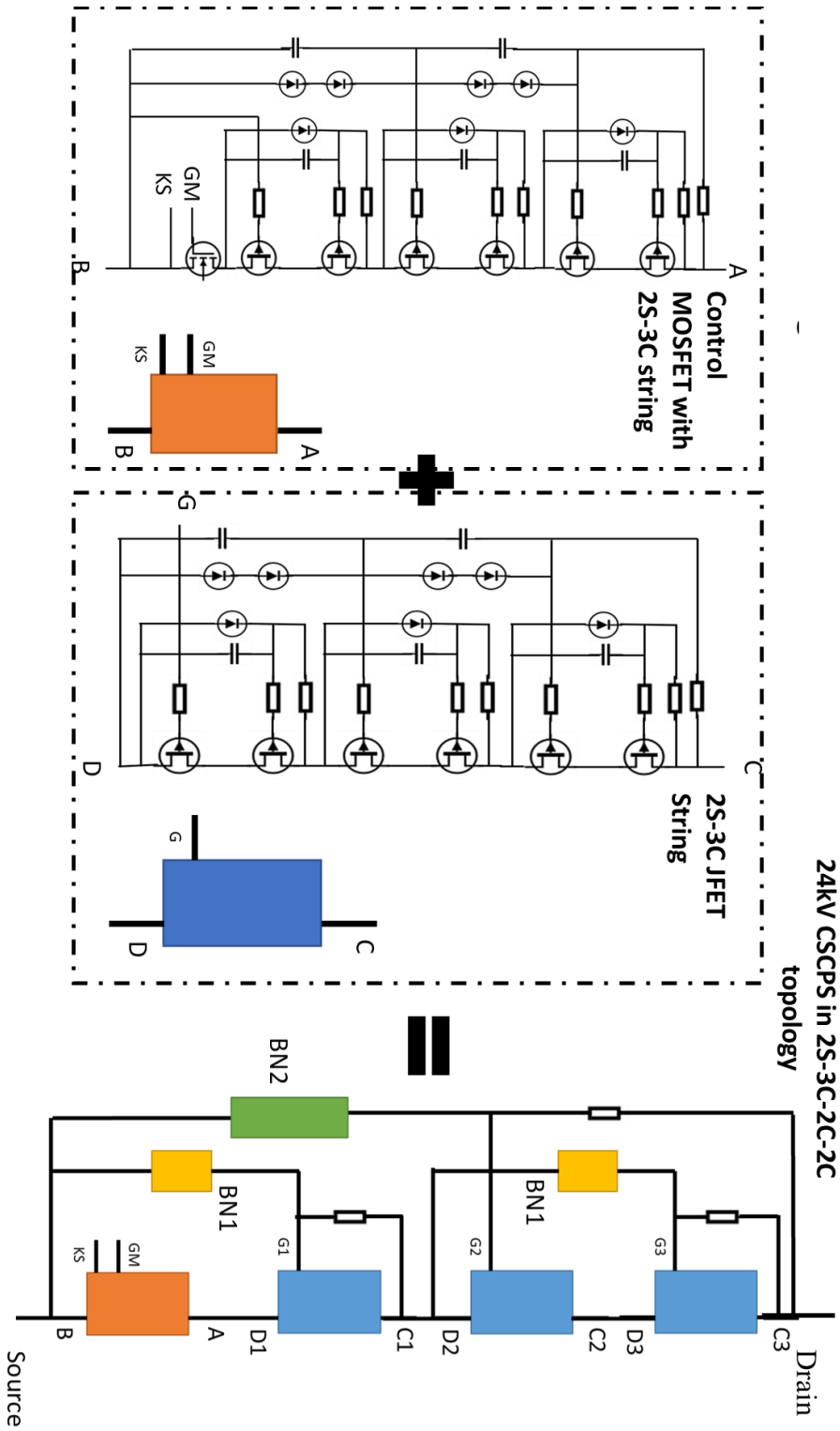


Fig. 2.5: Block diagram of three-layer 24 JFET Cascaded SuperCascode Power switch

In the *12* JFET CSCPS of Fig. 2.4 , the orange and blue box are both individual *1*-layer CSCPS and the yellow box forms the 2^{nd} layer balancing network which manages the two individual *6* JFET CSCPS (orange and blue box). In the *24* JFET CSCPS, the two BN1 layer (yellow box) forms the 2^{nd} layer balancing network which manages *6* JFET devices each and BN2 (green box) is the 3^{rd} layer balancing network which manages the two individual *12* JFET CSCPS. This concept can be extended and applied to *48* JFET CSCPS by forming 4^{th} layer balancing network, *96* JFET CSCPS by forming 5^{th} layer balancing network and so on.

2.6 Automated design optimization code for CSCPS comparisons

Multiple CSCPS switches are possible for any *N* number of JFETs in a serial string. However, there are optimum combinations of JFETs per USC and USCs in series for a CSCPS. Two variables: the net capacitor requirement, C_n calculated in (2.17) and net balancing switching loss, E_b calculated in (2.18) can be used to optimize any for the CSCPS.

$$C_n = \frac{\left(n * \sum_{j=1}^{m-1} j * (Q_G - Q_D)\right) + \sum_{k=1}^{n-1} \frac{k * (Q_G - Q_D)}{m}}{V_{DS}} \tag{2.17}$$

$$E_b = \frac{1}{4} * m * n * (Q_G - Q_D) * V_{DS} * (n + m - 2) \tag{2.18}$$

An automated design code, discussed in Appendix B, was written in MATLAB to compares CSCPS permutations for specific power switch ratings using the two equations shown above. For UJN1202z (UnitedSiC) JFETs and AU1PK avalanche diode, such that each *1.2 kV* JFET only blocks *1kV*, Table 2.3 compares *4* possible permutations to showcase the improvement offered by an optimization algorithm to realize a *6kV* JFET CSCPS, Table 2.4 compares *9* possible permutation to showcase the improvement offered by an optimization algorithm to realize a *12kV*

JFET CSCPS, and Table 2.5 compares *20* possible permutation to realize a *24kV* JFET string CSCPS.

Table 2.3: Possible permutations for a 6 JFET Cascaded SuperCascode Power Switch (CSCPS)			
Design Combinations		Balancing Network Loss (mJ)	Charge Requirement (nFV)
JFETs in USC (m)	USCs in series (n)		
1	6	2.25	4500
2	3	1.35	1800
3	2	1.35	2100
6	1	2.25	4500

Table 2.4: Possible permutations for a 12 JFET Cascaded SuperCascode Power Switch (CSCPS)				
Design Combinations in 1 layer CSC			Balancing Network Loss (mJ)	Charge Requirement (nFV)
JFETs in USC (m)	USCs in series (n)			
1	12		9.9	19800
2	6		5.4	6300
3	4		4.5	5400
4	3		4.5	6300
6	2		5.4	9300
12	1		9.9	19800
Design Combination of 2 layer CSC			Balancing network loss (mJ)	Charge Requirement (nFV)
JFETs in USC (m)	USCs in series (n)	CSCPS in series connected 2 at 2 layer cascade		
2	3	2	3.6	4200
3	2	2	3.6	4500
2	2	3	3.6	3600

Table 2.5: Possible permutations for a 24 JFET Cascaded SuperCascode Power Switch (CSCPS)

Design Combinations in 1 layer CSCPS		Balancing Network Loss (mJ)	Charge Requirement (nFV)
JFETs in USC (m)	USCs in series (n)		
1	24	41.4	82800
2	12	21.6	23400
3	8	16.2	15600
4	6	14.4	15300
6	4	14.4	19800
8	3	16.2	26100
12	2	21.6	39900
24	1	41.4	82800

Design Combination of 2 layer CSCPS			Balancing network loss (mJ)	Charge Requirement (nFV)
JFETs in USC (m)	USCs in series (n)	CSCPS in series connected at 2 layer cascade		
2	2	6	12.6	9900
2	6	2	12.6	12900
2	3	4	10.8	8400
3	2	4	10.8	9600
3	4	2	10.8	11100
4	2	3	10.8	9900
4	3	2	10.8	12900
6	2	2	10.8	18900

Design Combination of 3 layer CSCPS				Balancing network loss (mJ)	Charge Requirement (nFV)
JFETs in USC (m)	USCs in series (n)	CSCPS in series connected at 2 layer cascade	CSCPS in series connected at 3 layer cascade		
2	2	2	3	9	7200
2	2	3	2	9	7500
2	3	2	2	9	8700
3	2	2	2	9	9300

Inferring from Table 2.3, the CSCPS concept optimized for the *2S-3C* approach reduces switching losses by *40%* and cost factor by *60%* compared to *6S-1C* for a *6kV* CSCPS. From Table 2.4, the optimized 2S-3C-2C structure reduces switching losses by *63%* and cost factor by *79%* compared to *12S-1C* for the 12kV CSC, and from Table 2.5 the optimized *2S-2S-2C-3C* structure reduces switching losses by *79%* and cost factor by *91%* compared to the *24S-1C* for

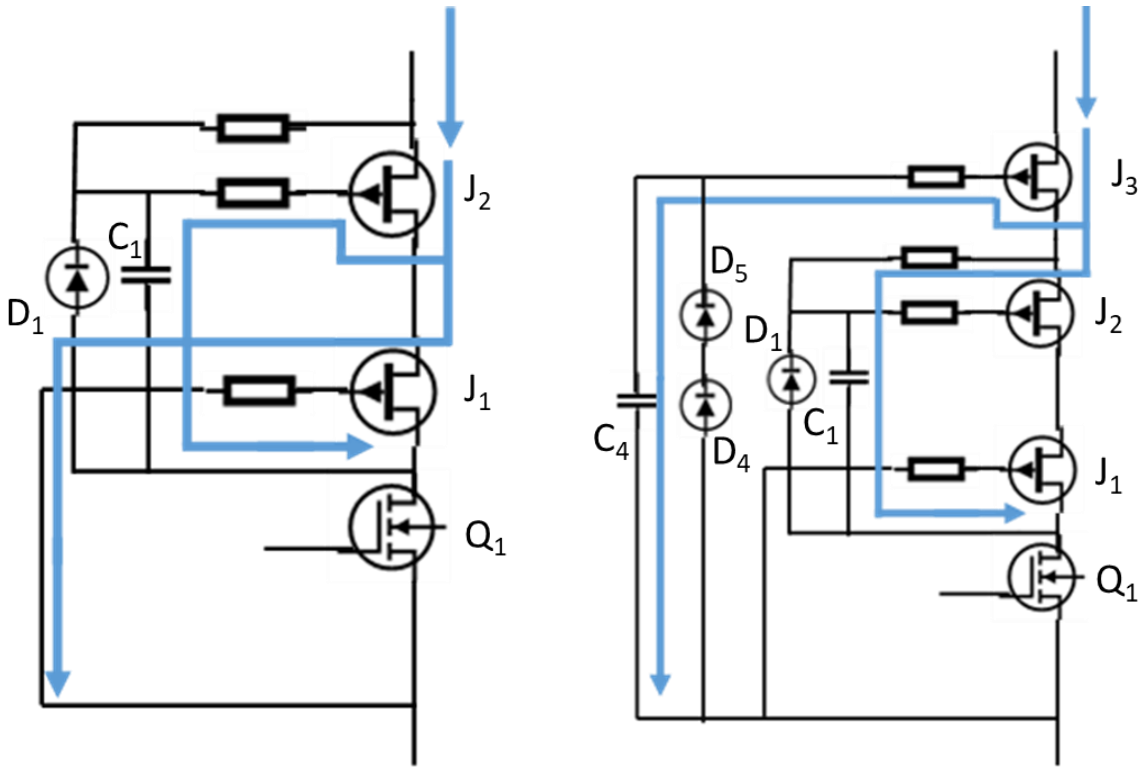
the *24 kV* CSC. This shows effectiveness of the CSCPS in comparison to the SCPS, where the net balancing network loss decreases with devices in a serial string promising voltage scalability of the CSCPS topology. This also shows that the CSCPS is effective in reducing the effective balancing network size and switching loss of all currently existing state-of-art SuperCascode topologies.

2.7 Switching Stages of the Cascaded SuperCascode Power Switch

2.7.1 CSCPS turn-off switching process

The turn-off process of the CSCPS has six stages of deactivation. The first stage begins when a control signal turns-off the Si MOSFET, Q_1. As the drain-to-source voltage V_{dsQ1} of Q_1 increases, the gate-to-source voltage V_{gsJ1} of the depletion-mode JFET, J_1, increases. As V_{dsJ1} increases C_1 is charged through C_{issJ2} reducing V_{gsJ2}. When V_{gsJ2} is lower (more negative) than $V_{th,\,J2}$ turns off. Then V_{dsJ2} starts to increase. This stage ends. The capacitor charging paths are shown in Fig. 2.6(a).

The second stage begins turning off when J_2 turns off and V_{dsJ2} begins to increase. When V_{dsJ2} increases, C_1 is charged through C_{issJ2}. The ratio between V_{dsJ1} and V_{dsJ2} is determined by C_1. As V_{dsJ2} increases, C_4 is also charged through C_{issJ3}, driving V_{gsJ3} more negative. When V_{gsJ3} is lower than $V_{th,\,J3}$ turn off. When V_{dsJ3} begins to increase this stage ends. The capacitor charging paths are shown in Fig. 2.6(b). The third and fifth stages of deactivation are similar to the first stage, and the fourth stage is similar to the second stage. In the sixth stage, when J_6 turns off, V_{dsJ6} starts to increase. The V_{dsCSC} reaches its blocking voltage that is applied to the CSCPS and completes the turn-off process.



(a) (b)

Fig. 2.6: Turn-off sequence (a) Phase I (b) Phase II

When the drain-to-source voltage of a JFET increases to an avalanche threshold of the avalanche diode, the diode begins to conduct with a large power loss. In a converter, series-connected switch voltage imbalance, leakage inductance, surge, etc., can all put power switches under avalanche conduction. For the CSCPS, the static per JFET voltage is defined by avalanche diodes, which breakdown when per-stage voltage increases in an avalanche condition. The relatively small size of the avalanche diodes in comparison to the JFET make them less capable of absorbing avalanche energy. To increase avalanche robustness a resistor is added in series with the avalanche diode to divert avalanche current from diodes to JFETs.

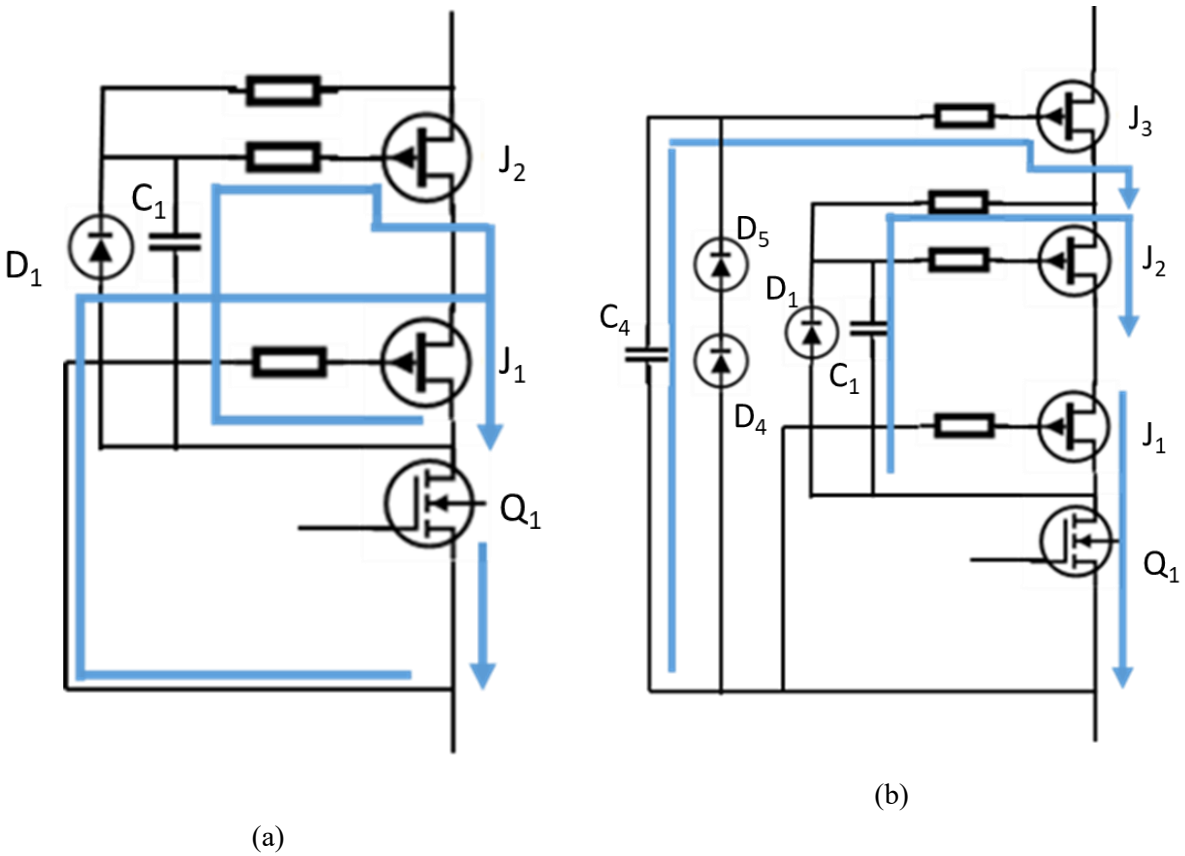
However, when the avalanche voltage is higher than the maximum drain-source voltage, V_{dsmax} of the CSCPS, JFET J_6 suffers from drain-gate junction avalanche because the gate of J_6 is connected to CSCPS source, which is the virtual ground for the switch. A gate resistor, R_6 limits

the maximum current flowing through drain-gate junction, forcing drain-source junction to absorb the majority of avalanche breakdown energy, not the diode. However, the higher the gate resistance, the slower the JFETs switch which increase switching loss.

2.7.2 CSCPS turn-on switching process

The turn-on process of proposed CSCPS has six stages for reactivation. The first stage begins when the MOSFET, Q_1 turns on and the drain-to-source voltage, V_{dsQ1} decreases. The blocking voltage of J_1 to J_6 increases to compensate for the decrease of V_{dsQ1}. As V_{ds_Q1} decreases, V_{gsJ1} increases turning J_1 ON when V_{gsJ1} is higher than V_{th}. Then V_{dsJ1} decreases and the blocking voltage of J_2 to J_6 increases. As drain-source voltage V_{dsJ1} decreases, capacitors C_1 and C_{d1} are discharged increasing V_{dsJ2} as shown in Fig. 2.7(a). When V_{dsJ1} starts to decrease, the stage ends.

The second stage begins when J_2 turns ON and the drain to source voltage, V_{dsJ2} starts decreasing. To compensate for the decrease in V_{dsJ2}, the blocking voltage of J_3 and J_6 increases. As V_{dsJ2} decreases, capacitors C_2 and C_{d2} are discharged increasing V_{dsJ3}. When V_{dsJ2} decreases and V_{dsJ3} increases the second stage ends. Discharge of C_2 and C_{D2} is shown in Fig. 2.7(b). The third and fifth stages are similar to first stage, and fourth stage is similar to second. The final sixth stage starts when J_6 turns ON and V_{dsJ6} decreases. The entire CSCPM turns on and V_{DSCSC} reaches near zero. Any overshoot normally occurs on V_{dsJ6}, so J_6 is first to fail. A higher voltage device or alternatively using a Transient voltage suppressor (TSV) or additional avalanche diode can placed across the JFET, J_6 to manage the overshoot.



(a) (b)

Fig. 2.7: Turn-on sequence (a): Phase I (b): Phase II

2.8 Simulation and Verification

To verify the CSCPS design methodology, a simulation was performed in LTSpice with six UJN1202Z JFETs and five AU1PK avalanche diode's connected in series in a 1-layer *2S-3C* configuration to verify the electrical performance and compare against previously reported Gao's 6-JFET SCPS. The simulation circuit is shown in Fig. 2.8. Firstly, for a resistive load of *120* Ω, the switching was studied to ensure each device blocks equivalent voltage and the result is shown in Fig. 2.9.

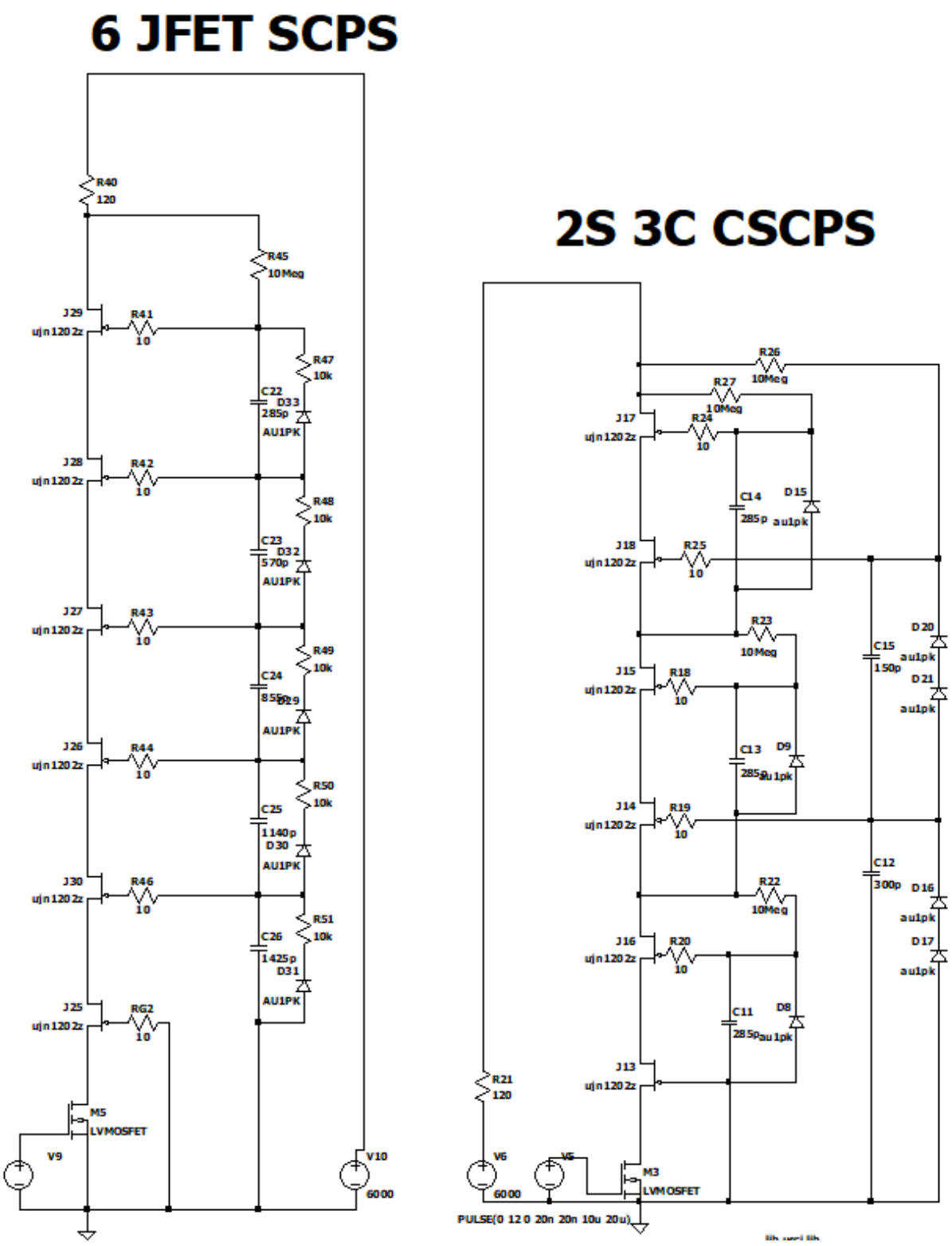


Fig. 2.8: LTSpice schematic of a 2S-3C 1-layer CSCPS with a pure resistive load

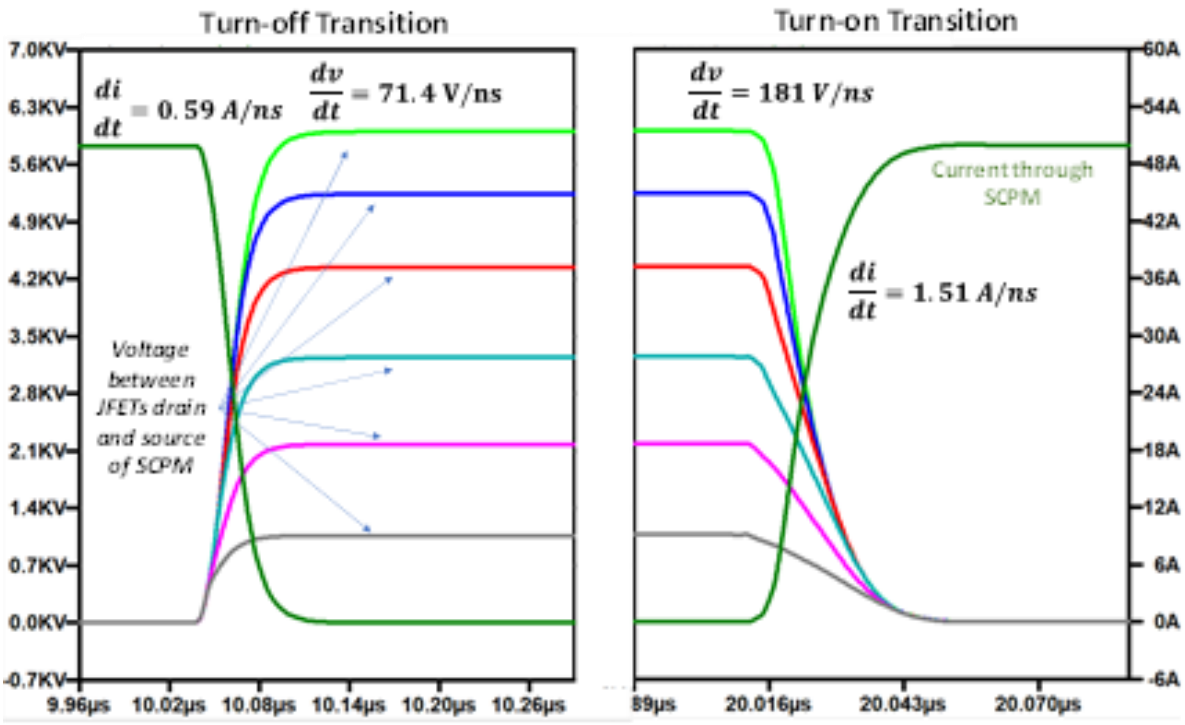


Fig. 2.9 : Simulated switching waveforms for the 2S-3C 1-layer CSCPS under pure resistive load

Voltage distributions across individual JFETs in a 2S-3C CSCPS structure are shown in Fig. 2.9. The proposed CSCPS has *26 ns* turn-on and *37 ns* turn-off for a 6kV DC bus, *120* Ω resistive load with *23 nH* of parasitic inductance considered in the power path. Fig. 2.9 shows equivalent static voltage distribution in the OFF state and each JFET shares ~*1kV* out of the 6kV CSCPS. A preliminary datasheet for a 6kV/50A CSCPS is attached in Appendix A.

Next, both the 6-JFET SCPS and the 2S-3C CSCPS is compared for switching performance and the switching transition and loss results are shown in Fig. 2.10.

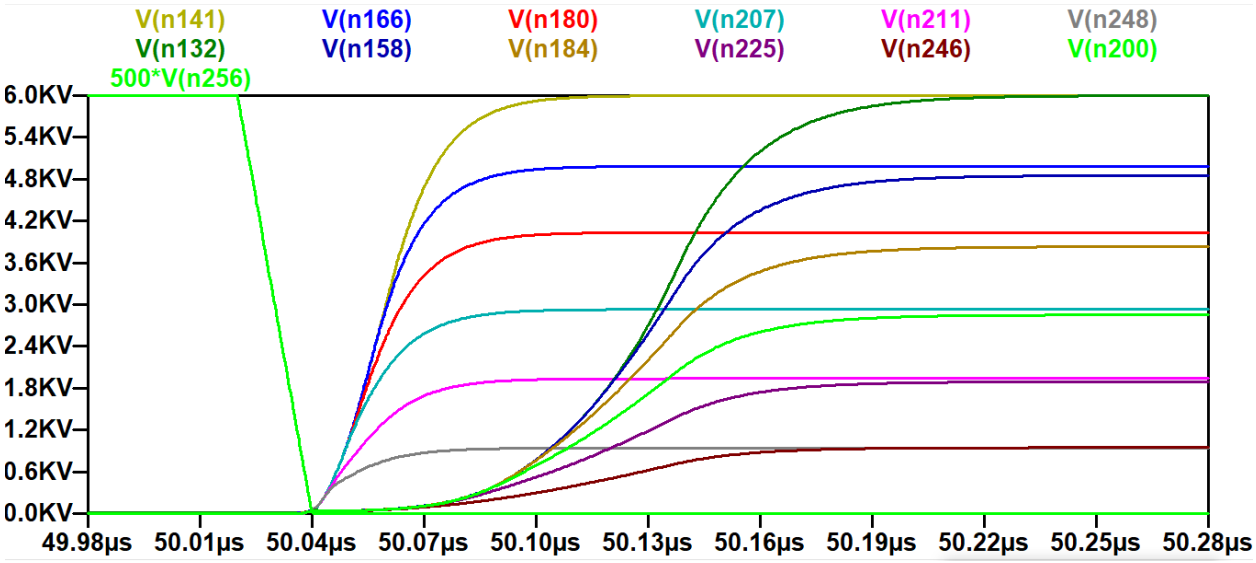


Fig. 2.10(a): Simulated turn-off switching transition

[For the 2S-3C CSCPS V(n141) is the voltage at the 6th JFET drain, V(n161) is the voltage at the 5th JFET drain, V(n180) is the voltage at the 4th JFET drain, V(n207) is the voltage at the 3th JFET drain, V(n211) is the voltage at the 2nd JFET drain, V(n248) is the voltage at the 1st JFET drain) (For the 6-JFET CSCPS : V(n132) is the voltage at the 6th JFET drain, V(n158) is the voltage at the 5th JFET drain, V(n184) is the voltage at the 4th JFET drain, V(n225) is the voltage at the 3rd JFET drain, V(n246) is the voltage at the 2nd JFET drain, V(n200) is the voltage at the 1st JFET drain]

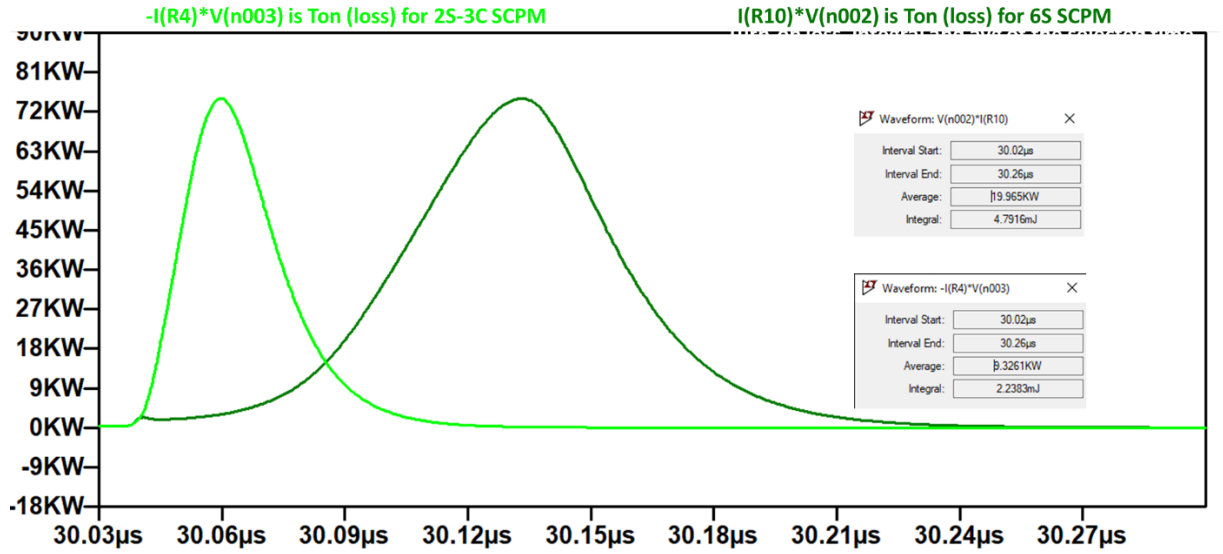


Fig. 2.10(b): Simulated turn-off switching loss

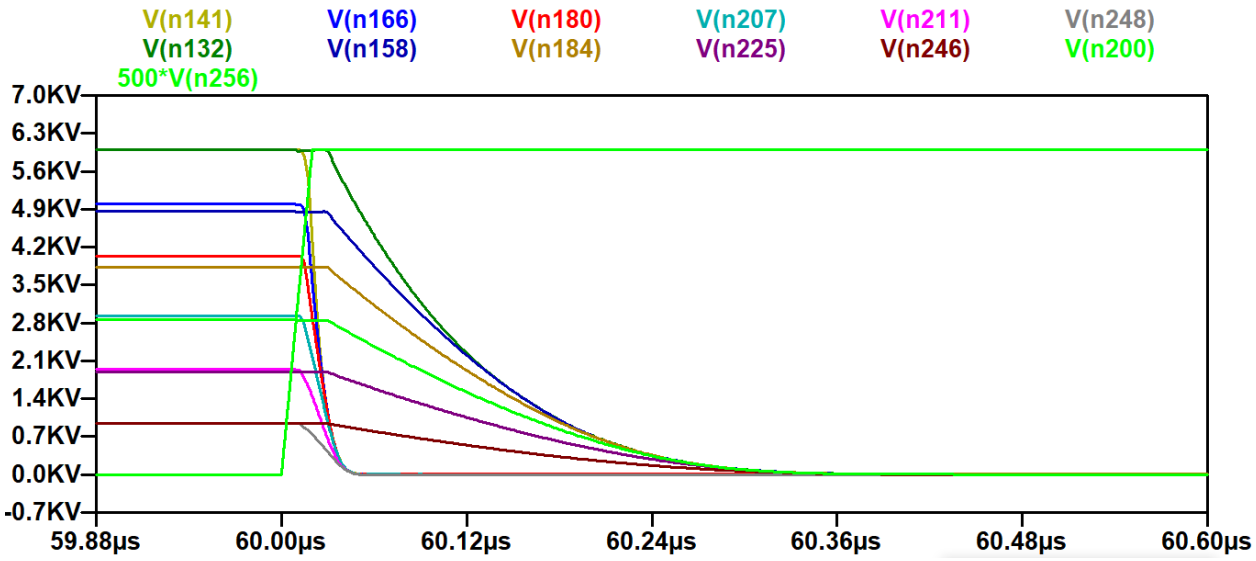


Fig. 2.10(c): Simulated turn-on switching transition [For the 2S-3C CSCPS V(n141) is the voltage at the 6th JFET drain, V(n161) is the voltage at the 5th JFET drain, V(n180) is the voltage at the 4th JFET drain, V(n207) is the voltage at the 3th JFET drain, V(n211) is the voltage at the 2nd JFET drain, V(n248) is the voltage at the 1st JFET drain) (For the 6-JFET CSCPS : V(n132) is the voltage at the 6th JFET drain, V(n158) is the voltage at the 5th JFET drain, V(n184) is the voltage at the 4th JFET drain, V(n225) is the voltage at the 3rd JFET drain, V(n246) is the voltage at the 2nd JFET drain, V(n200) is the voltage at the 1st JFET drain]

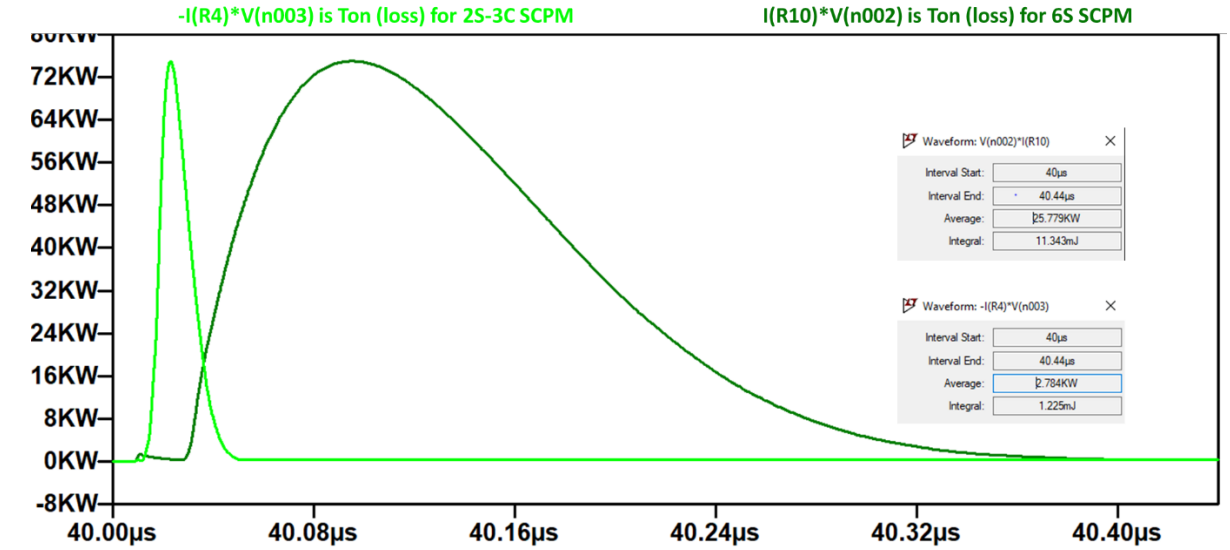


Fig. 2.10(d): Simulated turn-on switching loss comparison

From simulations, the 2S-3C CSCPS switches with 60 ns turn-off and 11 ns turn-on time respectively and the 6S SCPS switches in 200 ns turn-off and 300 ns turn-on. The simulation also shows that a 50% reduction in turn-off losses (4.79 mJ vs 2.24 mJ) and ~80% reduction in

turn-on losses (11.343 mJ vs 1.225 mJ) for 6 kV/50A operation. Herein the net balancing network loss for the 2S-3C 6kV CSCPS is 3.465 mJ wherein 1.35 mJ of loss is present in the balancing network.

2.9 Paralleling of Cascaded SuperCascode Power Switch

To scale current carrying capabilities at high voltage, multiple CSCPSs can be connected in parallel with a scaled and shared balancing network. The capacitance of the dynamic balancing network scales linearly to provide sufficient charge to trigger multiple parallel JFETs. The asymmetrices in layout can be compensated by the gate resistors. A two parallel *2S-3C 6kV* CSCPS is shown in Fig. 2.11, wherein one LV Si-MOSFET triggers multiple cascaded and scaled strings of SiC JFETs. The LV MOSFET may be composed of several paralleled MOSFETs. The dotted boxes show the components that need to be resized to accommodate multiple strings.

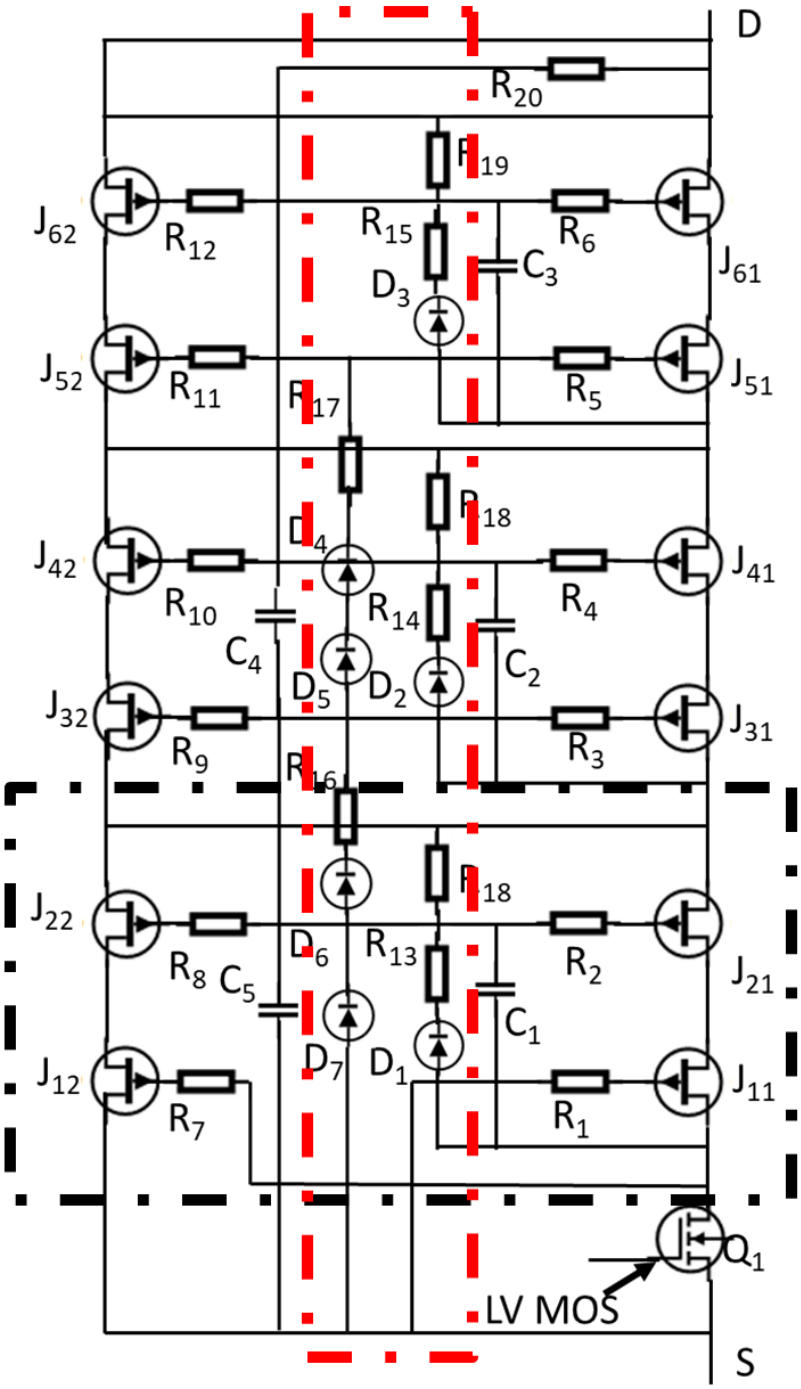


Fig. 2.11: Two parallel 2S-3C Cascaded SuperCascode Power Switch

2.9.1 Design of Unit SuperCascode Balancing network for scaled parallel CSC

Let '*m*' be the number of JFETs in series forming a unit SuperCascode (USC) and '*n*' be the number of USCs connected in series to form a CSCPS, and '*p*' are the number of CSCPSs connected in parallel. As shown in Fig. 2.11, three USCs are placed together with the help of an external balancing network to make the (*2S-3C*) CSCPS. Two of the (*2S-3C*) strings are placed in parallel, and share the same control switch, Q_1 and external (red box) and internal (black box) balancing network. The USC has "*m*" number of JFETs in series and *"p"* USCs in parallel. In the USC, R_{18} provides additional bias current for D_1 which sets the static balancing voltage. The resistor R_1, R_2, R_7 and R_8 set rise and fall times, whereas C_1 is sized based on the gate charge of JFET, J_{21} and J_{22} and the body charge of D_1. In a perfectly balanced system where voltage across all JFETs are the same and all JFETs and diodes are identical, the capacitor charge is determined by

$$\Delta Q_{Cm} = p * m * (Q_G - Q_D) \tag{2.19}$$

where *'p'* is the number of USCs in parallel and *'m'* the number of JFETs in series.

Thus, the capacitance of balancing capacitors for the unit SuperCascode to function are determined by (2.20) for an *m*-stage SuperCascode. There are *m-1* stages of balancing capacitors, which should have sufficient charge to trigger '*p*' strings in parallel.

$$C_{m\_s} = p * \sum_{j=1}^{m-1} \frac{j * (Q_G - Q_D)}{V_{DS}} \tag{2.20}$$

Using the capacitor energy formula, the loss per capacitor C_m is given by

$$E_{Cm\_s} = \frac{1}{2} * C_{m_s} * {V_{ds}}^2 \tag{2.21}$$

The total balancing network capacitive energy loss per unit SuperCascode (USC), E_{sbu} using gaussian formula, can be expressed as

$$E_{sbu} = \sum_{1}^{m-1} E_{Cm\_s} = \frac{1}{4} * (Q_G - Q_D) * V_{DS} * (m^2 - m) * p \qquad (2.22)$$

This is the net energy loss per USC comprising '*m*' JFETs in series and '*p*' in parallel, which is equivalent to sum of energy stored in *m-1* capacitors.

2.9.2 Design of Cascade (External) Balancing Network:

In the parallel-CSC approach, each USC gate is triggered by another external balancing network as shown in Fig. 2.11. The *2nd* USC control JFET J_{31}, J_{32} is triggered and controlled by C_5 and diodes D_6-D_7 in parallel and *3rd* USC control J_{51}, J_{52} is triggered and controlled by C_4 and diodes D_4-D_5 in parallel. This section discusses the external balancing network which drives individual USCs shown as red dotted box. The CSC has *'n'* USC connected and *'p'* USCs in parallel and controlled by an external passive balancing network. In the external balancing network, R_{20} provides additional bias current for D_4-D_7 which sets the static balancing voltage. The resistor R_3, R_5, R_9 and R_{11} set rise and fall times of the unit SCPM. C_5 is sized based on gate charge of J_{31}, J_{32} and body charge of D_6 and D_7 and C_4 is sized based on the gate charge of J_{51}, J_{52} and the body charge of D_4 and D_5 and so on.

In a perfectly balanced system where voltage across EACH USC should be the same and all JFETs and diodes are identical, the capacitance of the external balancing network is determined by (2.23), for a *n*-stage CSC there are *n-1* stages of balancing capacitors in the external balancing network. The net external balancing capacitance is

$$C_n = p * \sum_{k=1}^{n-1} \frac{k * (Q_g - Q_d)}{m * V_{ds}} \tag{2.23}$$

Where *'n'* is the number of USCs forming a CSC and 'p' USC are connected in parallel. Where Q_G is gate charge of JFET (Q_{GD}+Q_{GS}), Q_D is the anode-cathode charge of avalanche diodes (D_4 and D_5) in this case and V_{DS} is the drain-to-source voltage per JFET. The energy stored in external balancing capacitors C_n is

$$E_{Cn} = \frac{1}{2} * C_n * p * (m * V_{ds})^2 \tag{2.24}$$

To obtain total balancing network capacitive energy loss for external balancing network forming the cascaded SuperCascode (CSC), E_{sbc} using gaussian formula, can be expressed as

$$E_{sbc} = \sum_{1}^{n-1} E_{Cn} = \frac{1}{4} * (Q_G - Q_D) * (m * V_{DS}) * (n^2 - n) * p \tag{2.25}$$

This is the net energy loss in external balancing network of the CSCPS, which is equivalent to sum of energy stored in *'n-1'* capacitors. The total balancing network is the sum of switching losses in internal USC and external cascode balancing capacitors. As shown in Fig 2.7 the discussed *2S-3C-2P* cascade has three USC, i.e *n=3* and *p=2* in parallel. The net balancing switching loss for the entire switch for a "*n*" cascade switch is

$$E_{sb} = (n * E_{sbu}) + E_{sbc} \tag{2.26}$$

where E_{sb} is the net energy loss in the external and USC balancing network. Substituting equations (2.22) and (2.25) in (2.26) gives

$$E_b = \left(n * p * \frac{1}{4} * (Q_G - Q_D) * V_{DS} * (m^2 - m)\right) + \frac{1}{4} * (Q_G - Q_D) * (m * V_{DS}) * p * (n^2 - n) \quad (2.27)$$

Simplifying the above, the net balancing energy loss is

$$E_b = \frac{1}{4} * mn * (Q_G - Q_D) * V_{DS} * p * (n + m - 2) \quad (2.28)$$

The net balancing energy loss, E_b, in the CSC is proportional to a combination of stages which can be selected to minimize loss as shown in (2.29).

$$E_b \propto p * mn * (n + m - 2) \quad (2.29)$$

Comparing (2.29) and (2.14) we note that both the size of the balancing network and the balancing network switching loss directly scales with the number of devices in the serial string. Note: This is linear scaling and not exponential scaling as reported in Gao's SCPS.

2.9.3 Simualtion and Verification

To verify the parallel CSCPS design methodology, a simulation was performed in LTSpice with twenty-four UJN1202Z JFETs (depletion mode) and seven AU1PK avalanche diode's connected in series in a 1-layer 2S-3C-4P configuration to verify the electrical performance of the scaled and shared balancing network. The simulation circuit is shown in Fig. 2.12. The balancing network capacitors calculated are shown in Table 2.6 .

Table 2.6: Balancing network capacitor size for 1-layer 4 parallel		
Balancing Network Capacitors	2S-3C-4P CSCPS	2S-3C CSCPS
USC balancing capacitance, $C_1 = C_2 = C_3$	1140 pF	285 pF
External balancing capacitance, C_4	570 pF	150 pF
External balancing capacitance, C_5	1140 pF	600 pF

For a resistive load of *120* Ω, the switching was studied to ensure each device blocks equivalent voltage and the result is shown in Fig. 2.13. Voltage distributions across individual JFETs in a 4P-2S-3C CSCPS structure are shown in Figs. 2.13. Fig. 2.13 shows equivalent static voltage distribution in the OFF state and each JFET shares ~*1kV* out of the 6kV CSCPS.

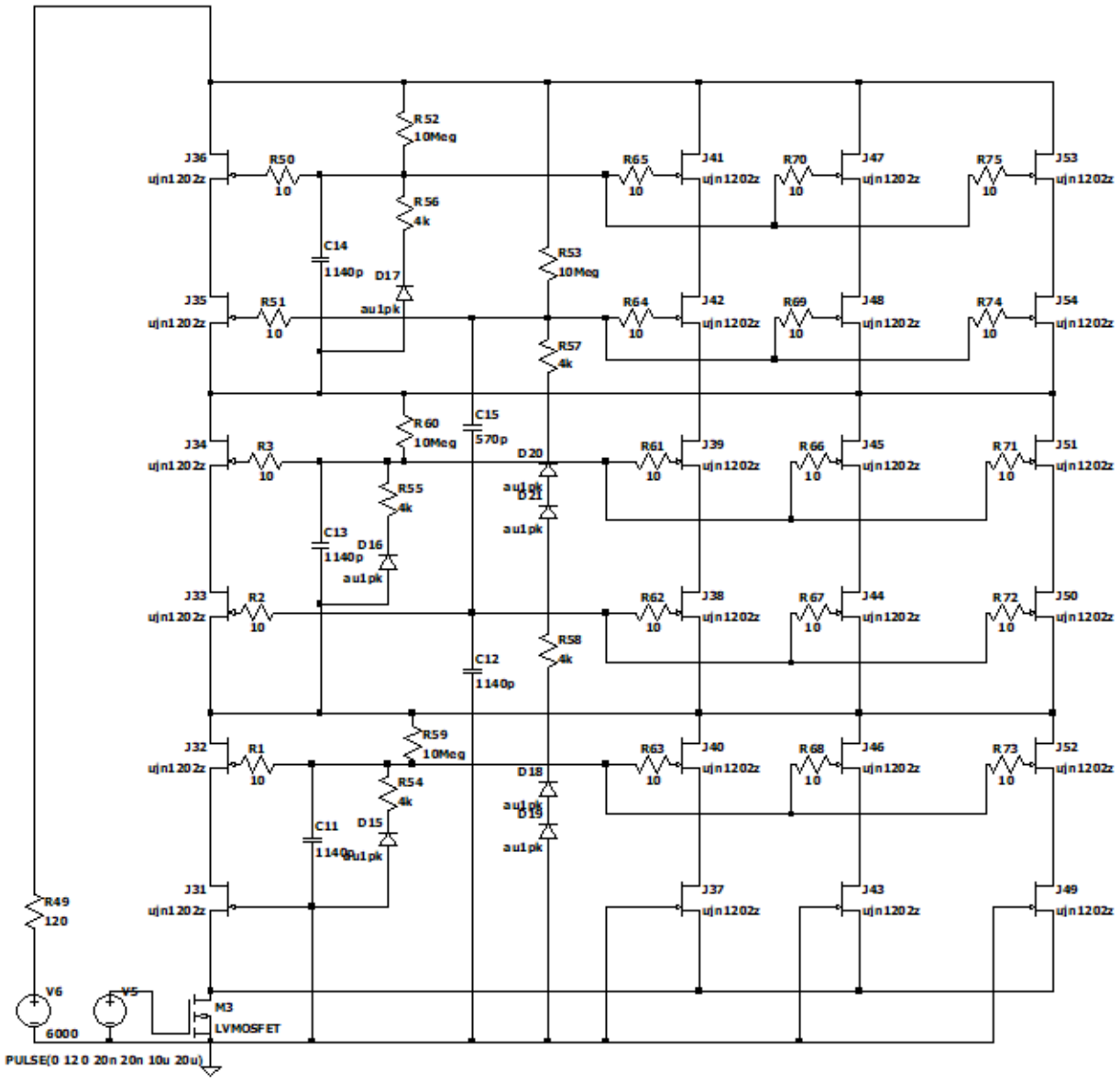


Fig. 2.12: LTSpice schematic of a 4 parallel 2S-3C 1-layer CSCPS with a pure resistive load

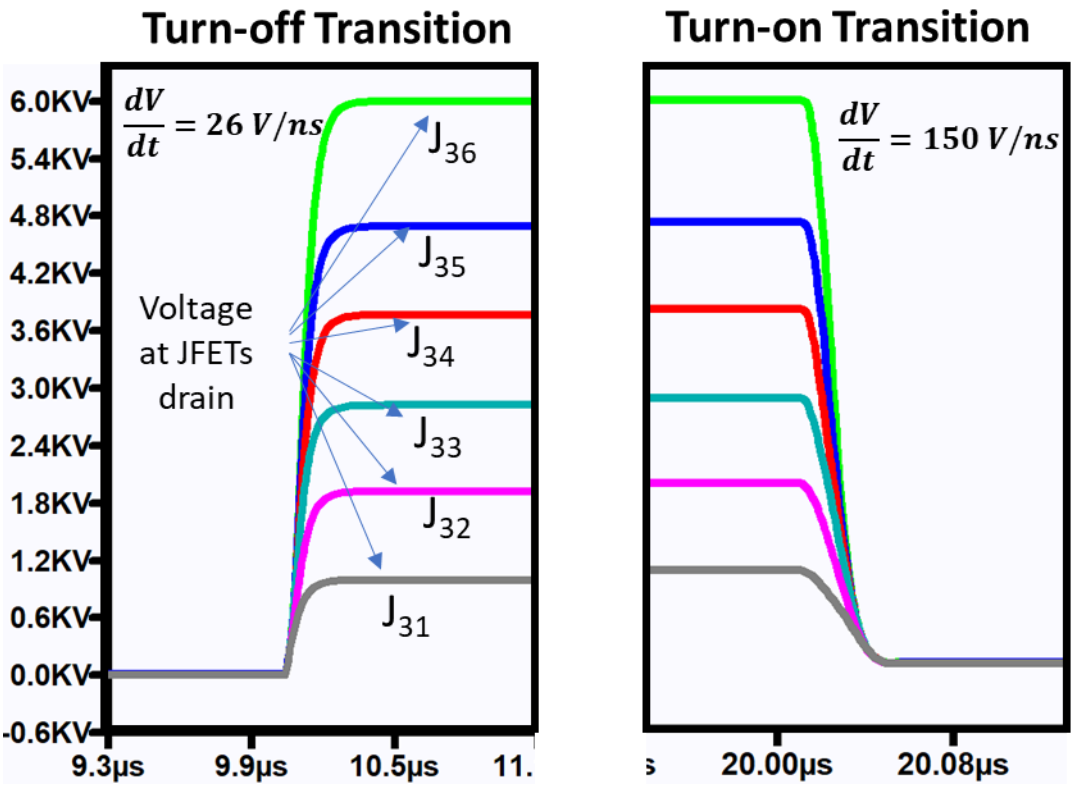


Fig 2.13: Simulated switching waveforms for the 4 parallel 2S-3C 1-layer CSCPS under pure resistive load

The result shows all devices are sequentially triggered and verifies that equations (2.19)-(2.23) can be used to do a first step optimization of balancing capacitors.

2.10 Selection of CSCPS Balancing Network Capacitances

The balancing capacitors in the network define the voltage distribution among the individual JFETs in the voltage balancing circuit. The capacitor capacitance can be fine-tuned to synchronize switching and ensure equal dissipation of power across all JFETs in the string. Capacitance optimization can also reduce switching loss during transients and JFET voltage overshoot.

The inputs for the model are gate charge of JFET, Q_G (Q_{GD}+Q_{GS}); anode-cathode charge of avalanche diode, Q_D; CSC power switch rated voltage, V_R ; JFET gate threshold voltage, *Vth* and JFET drain-source rated voltage, *VDS*. It is assumed *N* is the number of JFETs in the CSCPS, '*m*' is the number of JFETs in a USC and '*n*' is the number of USCs forming a CSCPS.

Step 1: The number of JFETs are calculated using the CSCPS rated voltage and JFET rated voltage:

$$N = \frac{V_R}{V_{DS}} \tag{2.30}$$

Step 2: The factors of *N* are represented as variables "$x_1, x_2, \ldots x_n$". For a single layer CSCPS, two factors are then selected in permutations and represented as *m* and *n* such that

$$N = m * n \tag{2.31}$$

For a two-layer CSCPS, three factors are selected in permutations represented as *m*, *n* and *o,* and repeated

$$N = m * n * o \tag{2.31}$$

Here, '*m*' is the number of JFETs forming a USC, '*n*' is the number of USCs connected in the *1st* CSCPS layer to form a CSCPS and '*o*' is the number of CSCPS connected in series and powered at the *2nd* layer.

Step 3: The USC internal capacitance is then calculated. For a *m* JFET USC, *m-1* capacitors are required and capacitors scale starting from the top most capacitor, C_1

$$C_m = m * \frac{Q_D - Q_G}{V_{DS}} \tag{2.32}$$

Starting at the topmost capacitor, C_1 i.e. the capacitor at the highest voltage potential relative to ground, scales as $C_m = m*C_1$ where *m* is the JFETs in an USC. As an example, let $Q_G = 300\ nC$,

$Q_D = 30\ nF$ and such that each JFET blocks 1kV. For m=2 the USC requires one capacitor, $C_1 = 270\ pF$ for $m = 3$ the USC requires two capacitors, $C_1 = 270\ pF$ and $C_2 = 540\ pF$ and so on.

Step 4 : For a single layer CSCPS, the external balancing capacitance is then calculated using (2.33). For a circuit with *n* USCs forming a CSCPS, *n-1* capacitors are required and scale with *n* starting from the capacitor, C_{11} . Note the scalability is representative of the number of USCs in string forming a *N*-JFET CSCPS.

$$C_m = \left(\frac{1}{m-1}\right) * \left(\frac{Q_D - Q_G}{V_{DS}}\right) \tag{2.33}$$

Starting, C_{11} i.e the capacitor at the highest voltage potential relative to the ground, scales as $C_{n1} = n*C_{11}$, where '*n*' is the number of USCs forming a single layer CSCPS. As an example, let $Q_G = 300\ nC$, $Q_D = 30\ nC$, *for a* six *JFET CSCPS let* $n = 2$, $m = 3$ and each JFET blocks *1kV*. Using (2.33), $C_{11}=135\ pF$. Similarly, for $n = 3$, $m = 2$ the capacitors are $C_{11} = 135\ pF$ and $C_{21} = 270\ pF$.

Similarly, the net capacitance requirement for a multi-layer *N*-JFET CSCPS can be calculated using the flowchart shown in Fig. 2.14. The flowchart calculates the net capacitance for an external layer CSCPS and net capacitance internal to a USC.

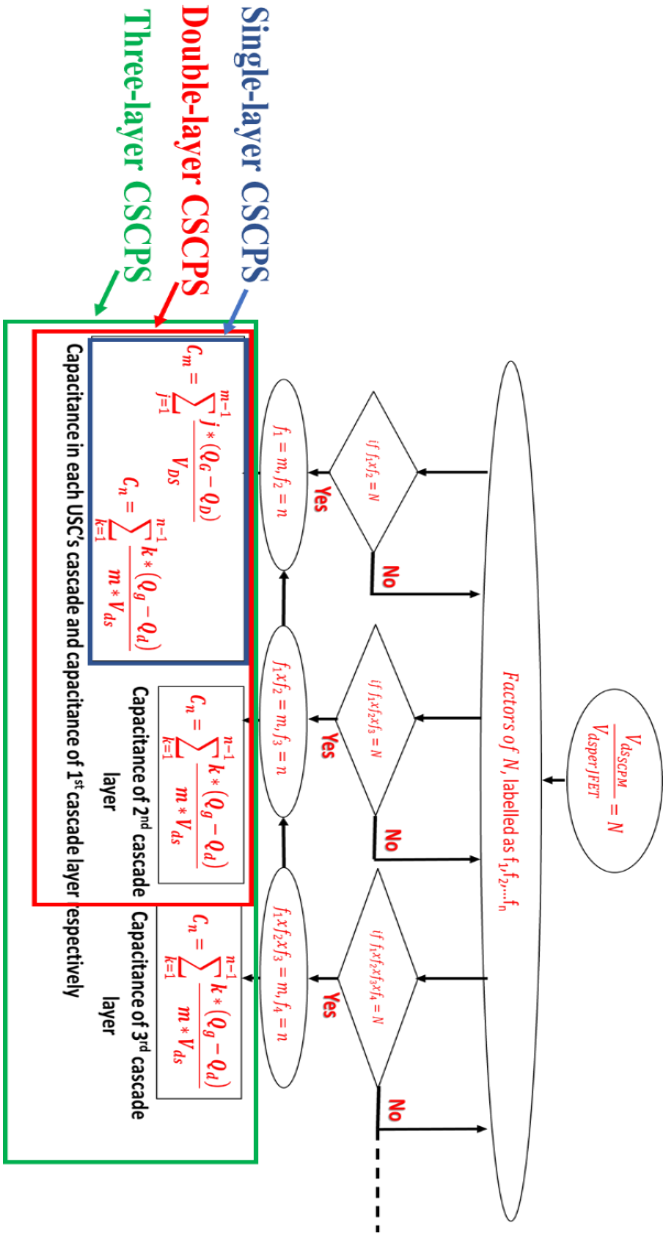


Fig. 2.14: Flowchart to calculate the net balancing network capacitors

Using, Fig. 2.14: To design a *12*-JFET CSCPS, let *m=2*, *n=3* and *o = 2* and JFET $V_{DS} \geq 1kV$ each. For example using (2.32), each USC requires one balancing capacitor, $C_1 = 270\ pF$. Then the *1st* layer balancing network has two balancing capacitor, $C_{11} = 135\ pF$ and $C_{21} = 270\ pF$ and the *2nd* layer balancing network has one balancing capacitor, using (2.33), $C_{12} = 100\ pF$.

2.11 Studies about Variabilities in Balancing Network

In the CSCPS structure, a sequential turn-off results in overvoltages of the upper JFETs, particularly, for example, in the case of hard commutation of a diode in a bridge leg. In the topology, first the current is commutated from the diode to the CSCPS before the voltage could decrease so that in a sequential turn-on, the most upper JFET would have to take the full blocking voltage for a short time. This sequential switching causes JFETs in the lower stages, i.e J_6 to dissipate more power than upper stage JFET, i.e J_1. Thus to avoid overvoltages and achieve synchronization of JFETs during switching transients, capacitors and gate resistors are added in the CSCPS. However, the devices in CSCPS have inbuilt manufacturing tolerances and balancing network components tolerances and layout parasitic can both affect the electrical and switching performance of the CSCPS power switch.

Variability Study 1 : Affect of non-optimized capacitance on JFET voltage distribution in Cascaded SuperCascode Power Switch (CSCPS)

The first variability study discusses the effect of capacitance variation in the USC and 1^{st} layer CSCPS on the voltage sharing across JFETs. A *2kV* Unit SuperCascode is chosen and shown in Fig. 2.15 for simplification. In the OFF state, C_1 is charged. To turn ON the SCPS, Q_1 is turned on by applying a gate voltage greater than the threshold voltage. When Q_1 turns on the J_1 gate-source voltage decreases. When it reaches pinch-off, J_1 starts to conduct and the source potential of J_2 starts decreasing. Capacitor C_1 fixes the potential for a limited time such that the gate voltage of J_2 increases as soon as the source potential decreases. Thus, proper sizing of C_1 will synchronize JFET turn-on and turn-off.

The C_1 is varied from *25pF* to *400pF* in *25pF* steps. Simulation results showing the turn-on and turn-off switching transient for C_1 is shown in Fig. 2.16. The plot of drain-source voltage

versus varying balancing capacitance and peak overshoot versus varying balancing capacitance is shown in Fig. 2.17(a) and Fig. 2.17(b) respectively.

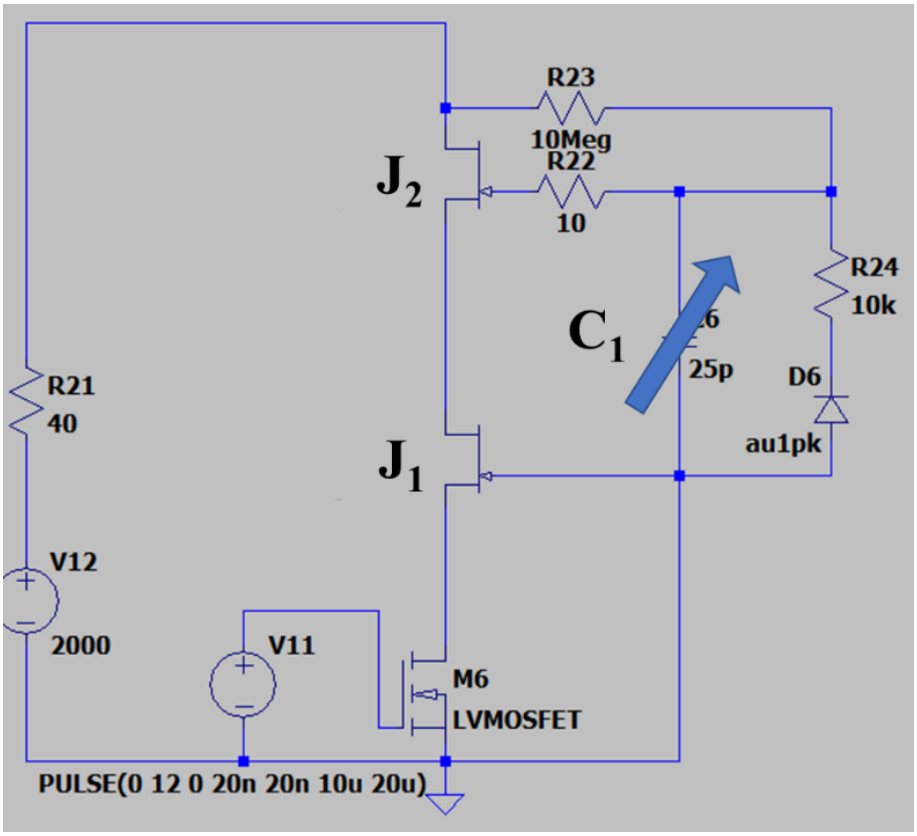
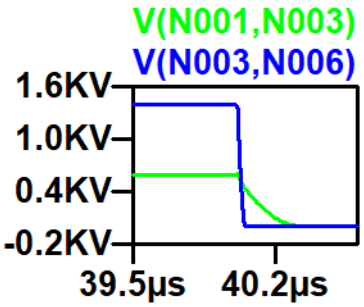
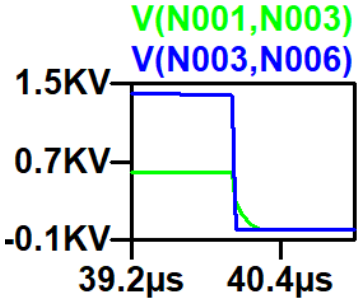


Fig. 2.15: LTSpice schematic of a 2kV SuperCascode

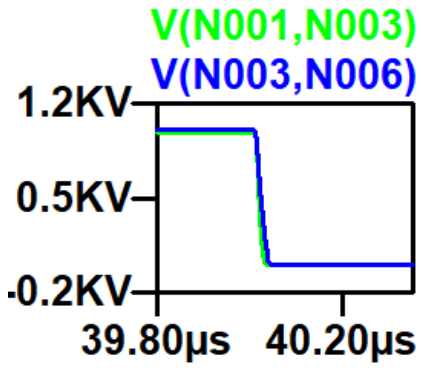
Turn-on Transient



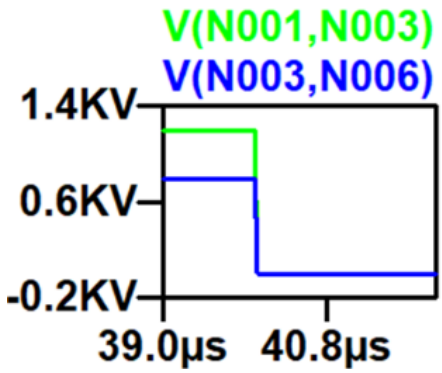
C=25 Pf



C=50 pF



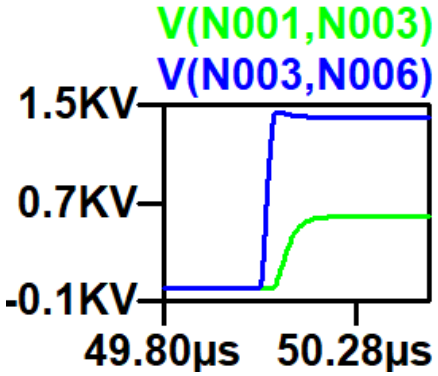
C=285 pF



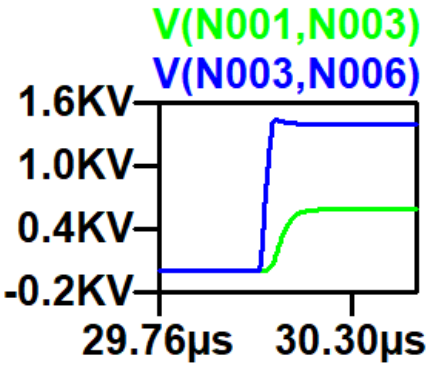
C=400 pF

Fig. 2.16 (a): Drain to source voltage and switching tranients across the serial JFETs under varied balancing capacitances (green trace : V_{ds} of J_1, blue trace : V_{ds} of J_2)

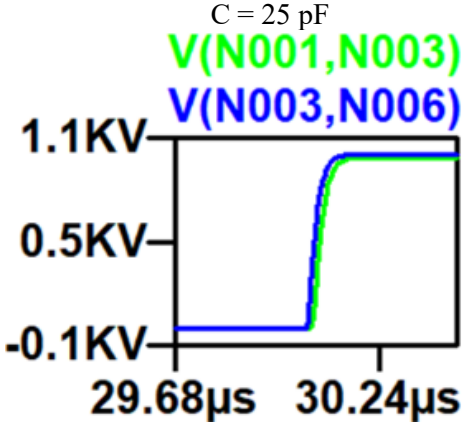
Turn-off transient



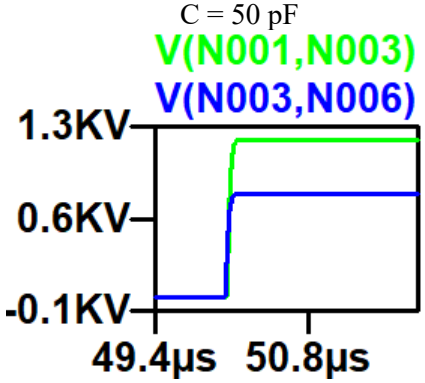
C = 25 pF



C = 50 pF



C = 285 pF



C = 400 pF

Fig. 2.16 (b): Drain to source voltage and switching tranients across the serial JFETs under varied balancing capacitances (green trace : V_{ds} of J_1, blue trace : V_{ds} of J_2)

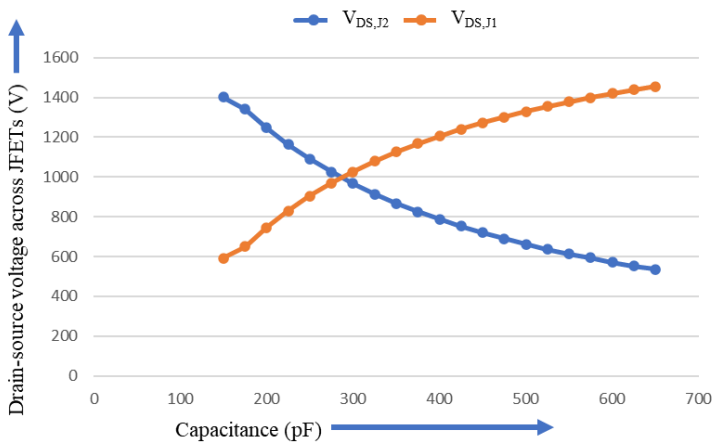


Fig. 2.17 (a): Plot of drain-to-source voltage across JFETs vs capacitance

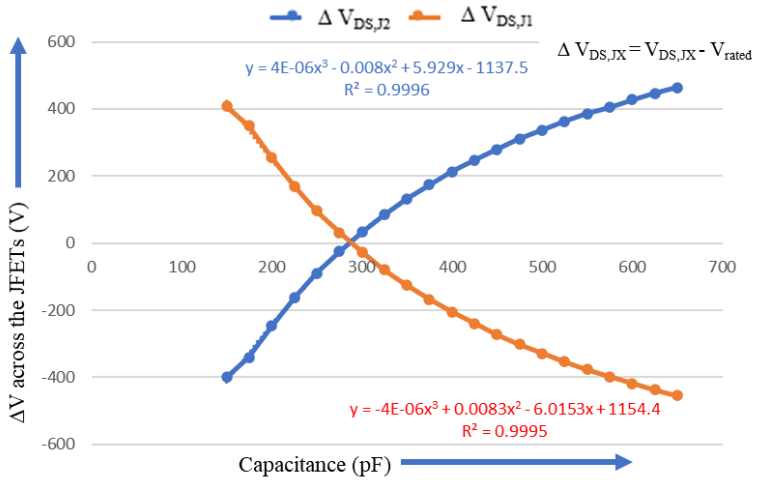


Fig. 2.17 (b) Plot of voltage difference across JFETs vs capacitance

The results show that with increasing capacitance value, greater synchronization in JFETs of the SuperCascode is achieved which manages the blocking capability of the serials JFETs. However, a large value of C_1 results in a more synchronous switching operation, but an unbalanced voltage distribution as shown in 2.15(a). The trend of voltage difference across JFETs vs capacitance, shown in Fig. 2.16 can be represented by the following polynomial expression.

$$\Delta V_{DS,J1} = -4 * 10^{-7} C^3 + 0.0083 C^2 - 6.0153 C + 1154.4 \qquad (2.34)$$

Note, the trend is valid for the UJN1202z JFET and any variation in Q_{GS}, Q_{DS}, transconductance, etc. alters the trend shown in Eqn 2.34.

Variability Study 2: Affect of capacitance variation in external balancing network on JFET voltage distribution in CSCPS

Similar to the previous variability study, tolerances in balancing capacitors of both the internal and external USC's affect the blocking voltage. Under ideal scenario, for a *6kV* 1-layer *2S-3C* CSC designed using UnitedSiC UJN1202z die, with $Q_g = 300\ nC$ and $Q_d = 15\ nC$. The capacitors calculated using Step 1-4 where $m=2$ and $n=3$ are $C_1 = 285\ pF$ and external capacitors are $C_{11} = 150\ pF$ and $C_{21} = 300\ pF$. To study the effect of capacitor tolerance, a *6* JFET *2S-3C* SuperCascode power switch LTSpice model is created and the balancing capacitors are one-by-one varied by *+20%* and the effect of drain-source voltage of each JFET is studied. The result is shown in Fig. 2.18.

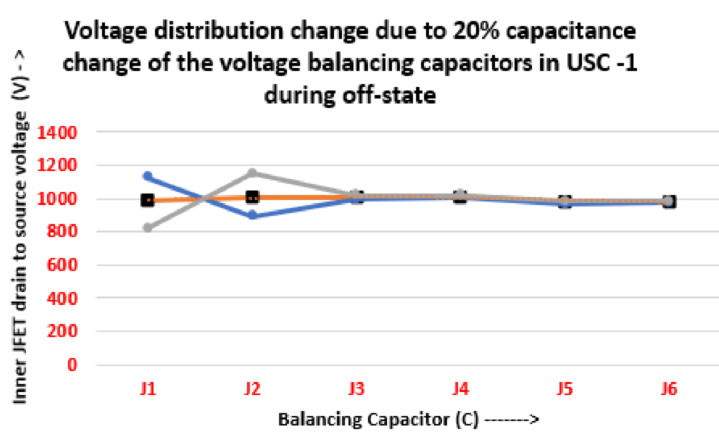


Fig. 2.18(a): Drain-to-source voltage of each JFET when USC-1 balancing capacitor is varied by +20%

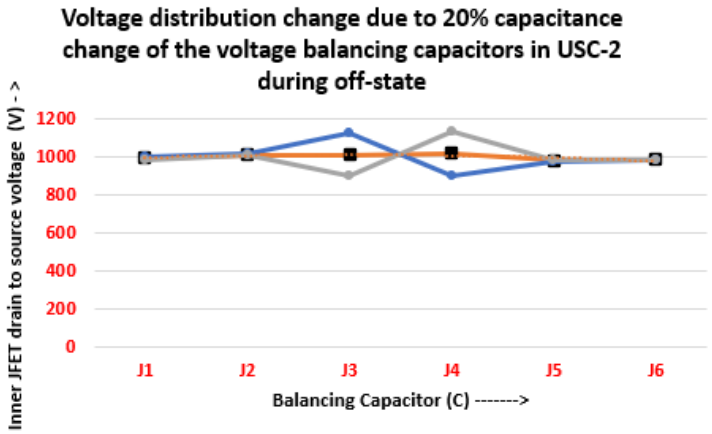


Fig. 2.18(b): Drain-to-source voltage of each JFET when USC-2 balancing capacitor is varied by +20%

Fig. 2.18(c): Drain-to-source voltage of each JFET when USC-3 balancing capacitor is varied by +20%

Fig. 2.18(d): Drain-to-source voltage of each JFET when external balancing capacitor, C_{11} is varied by +20%

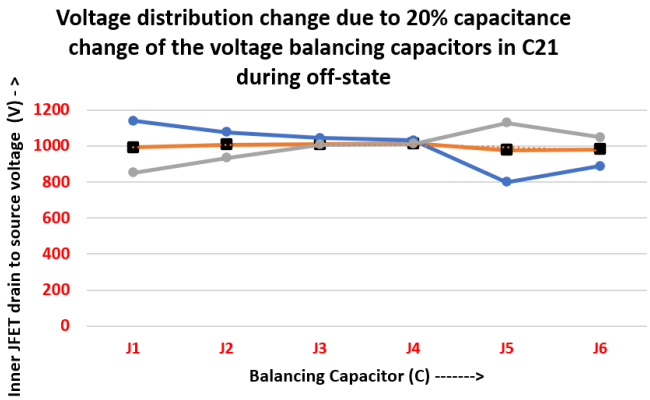


Fig. 2.18(e): Drain-to-source voltage of each JFET when external balancing capacitor, C_{21} is varied by +20%

Results shows unequal voltage stress on JFETs, the lower JFETs block a higher voltage level than the upper JFETs. Results also show that the internal USC balancing capacitors have a higher tolerance band than the external USC balancing cacpacitors, C_{11} and C_{21}.

2.12 Practical Challenges in CSCPS scaling

In the Cascaded SuperCascode structure, a non-synchronous turn-off causes overvoltages of the upper JFETs particularly for example, in case of hard commutation of a diode in a bridge leg. Further device internal tolerance (i.e. varied gate resistances, gate charge, etc.) and stray parasitics which limit a specific JFET switching rate and improper balancing network design. This section discusses compensation or fine tuning of the the balancing network components using the variability studies discussed in Section 2.11 against device tolerance and stray components to realize the optimum performance of the CSCPS tolopgy.

A. Unequal Power and voltage dissipation

In a CSCPS are sequentially triggered from J_6 to J_1 in Fig. 2.1. When a device blocks equivalent voltage during sequential turn-off a slight delay occurs between triggering J_1 and J_6,

which causes JFETs in lower stages (i.e. J_6) to dissipate more power than JFETs in upper stages (i.e. J_1) during switching as shown in Table 2.5 when each device blocks equivalent voltage.

By compensating or fine-tuning the balancing capacitors using equation (2.34) viable for JFETs to operate at different voltage rating in CSCPS string such that each device dissipates the same amount of power. To mitigate uneven dissipation, the balancing network is tuned such that J_6 operates at a lower voltage than J_1 offsetting the unequal power dissipation.

For example, for the LTSpice model, the simulated energy loss and blocking voltage of serial JFETs in a CSCPS is shown are Table 2.7. Shown is that by allowing J_1 to block $395\ V$ more than J_6 the change in power dissipation can be reduced from $0.21\text{-}0.85\ mJ$ to $0.37\text{-}0.61\ mJ$. Further reduction is possible by using $>1.2\ kV$ devices, and scaling upper stage device blocking capability as string size increases.

Table 2.7: Simulated switching energy loss and blocking voltages of serial JFETs in 2S-3C 6kV CSCPS

	Blocking voltage equated		Targeting equivalent power dissipation	
JFET	E_{SW}	V_{OFF}	E_{SW}	V_{OFF}
J1	0.21 mJ	942 V	0.37 mJ	1152 V
J2	0.32 mJ	980 V	0.44 mJ	1120 V
J3	0.42 mJ	1010 V	0.48 mJ	1041 V
J4	0.55 mJ	1014 V	0.48 mJ	1015 V
J5	0.61 mJ	1011 V	0.56 mJ	915 V
J6	0.85mJ	1023 V	0.61 mJ	757 V
M1	0.01 mJ	20 V	0.01 mJ	20 V

B. *Parasitic Capacitance and Inductance internal to a power module*

Unwanted parasitic circuit capacitances adding to C_{oss} and C_{gs}, or tolerance variations in the device pinch-off voltage, $V_{p\text{-}o}$, can affect the serial triggering of devices but can be adjusted by modifying the balancing network capacitance as shown in (2.35) where, ΔV is the per JFET blocking voltage.

$$\Delta C = \left(\Delta C_{gs} + \Delta C_{oss}\right)\frac{\Delta V_{p-o}}{V_{p-o}} \tag{2.35}$$

Here, Δ is change in capacitance and voltage due to tolerance and parasitics. Similarly, parasitic inductance in the CSCPS limits the rate at which the JFET is charged and discharged causing a time delay, t_d.

$$t_d = V_{p-o} * \frac{I_{gs}}{L_{par}} \tag{2.36}$$

This delay can cause loss of synchronization in sequential triggering and scales with the number of devices in the serial string. To compensate, gate resistors and balancing networks can be fine-tuned to adjust the RC switching rate.

2.13 Advantages of the Cascaded SuperCascode Structure

2.13.1 *Low thermal resistance*

The Cascaded SuperCascode Power Switch (CSCPS) distributes power dissipation over multiple devices facilitating heat exctraction via thermal spreading across a larger physical area. Thermal spreading leads to lower thermal resistance (R_{jc}) and the net result should be a higher RMS current rating. To conclude such a result and prove that the thermal resistance decreases with scaling N (i.e. more serial devices with lower V_{DS} ratings) , the following assumptions are used.

- An average spread angle for thermal dissipation of 45^0
- No thermal coupling exists between LV devices in the serail string of CSCPS
- Both the HV and the LV devices are square

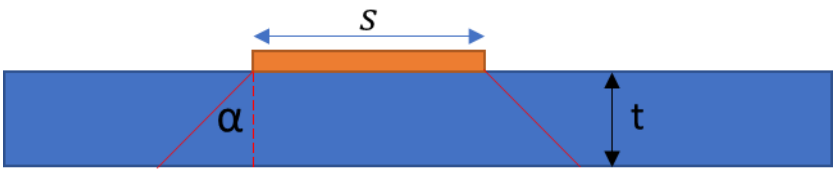


Fig. 2.19: Thermal spreading from power device with side, 's' through a substrate with 't' thickness

The thermal resistance of a power module stack with *dl* thickness and for a square power die with side, '*s*' can be represented as :

$$R_{th} = \frac{1}{k_{th}} \int_0^t \frac{dl}{A(l)} \tag{2.37}$$

The HV device thermal resistance can be simplified assuming average spreading angle, $\alpha = 45^0$; t is thickness of the stackup, s is the side of the HV single device and s^2 is the area of cross-section.

$$R_{thHV} = \frac{t}{k_{th}(s^2 + 2ts)} \tag{2.38}$$

For equivalent device specific on-resistance such that both the HV device and N-LV CSCPS approach can conduct the same current denisty. The cross-section area of LV semiconductor will be represented as :

$$A_{LV} = \frac{s^2 * R_{spHV}}{N * R_{spLV}} \tag{2.39}$$

Thus each side can be represented as $s/\sqrt{N * \frac{R_{spLV}}{R_{spHV}}}$. The thermal resistance of each LV devices in a CSCPS can be simplified as :

$$R_{thLV} = \frac{t}{k_{th}\left\{\frac{s^2 * R_{spHV}}{N * R_{spLV}} + \frac{2st}{\sqrt{N * \frac{R_{spLV}}{R_{spHV}}}}\right\}} \tag{2.40}$$

With *N* number of devices in series in a CSCPS, the net effective thermal resistance for each die can be represented as :

$$R_{thCSCPS} = \frac{1}{N} * R_{thLV} = \frac{t}{N * k_{th}\left\{\frac{s^2 * R_{spHV}}{N * R_{spLV}} + \frac{2st}{\sqrt{N * \frac{R_{spLV}}{R_{spHV}}}}\right\}} \tag{2.41}$$

The ratio of thermal resistance of CSCPS to single HV power die can be represented as :

$$\frac{R_{thCSCPS}}{R_{thHV}} = \frac{R_{spLV}}{R_{spHV}} * \frac{(s^2 + 2st)}{\left(s^2 + 2st\sqrt{N * \frac{R_{spLV}}{R_{spHV}}}\right)} \tag{2.42}$$

The current trend of 1.2kV JFET Rds-A for the UnitedSiC G4 SiC JFETs is 1.25 mΩ-cm^2 [110] and for the 15kV SiC MOSFETs for CREE power devices is 204 mΩ-cm^2 [112]. Thus, as shown in Equation (2.42), the net thermal resistance of the CSCPS approach is substantially smaller than a single HV approach.

If $\sqrt{N * \frac{R_{spLV}}{R_{spHV}}}$ >>> 2t/s , then the Cascaded SuperCascode power switch thermal resistance is $\sqrt{N * \frac{R_{spLV}}{R_{spHV}}}$ times smaller than thermal resistance of the HV device.

2.13.2 *Cost Comparison of CSCPS vs single HV MOSFET to realizing a power switch*

The cost of a semiconductor is determined by the die area, die thickness and manufacturing yield. Die area dictates the current carrying capacity, die thickness of a vertical device defines blocking voltage rating and manufacturing yield is dependent on the type of power semiconductor device. For this study the JFET based CSCPS is compared with a HV MOSFET configuration scaled to realize a single HV power switch using specific on-resistance, die dimension, wafer yield, processing and fabrication cost.

For this cost study, a SiC JFET-based Cascaded SuperCascode Power Switch (CSCPS) is compared against a High Voltage SiC MOSFET-based power switch for comparable voltage and current ratings. The switch series or parallel configuration are scaled to realized equivalent switches with same Rdson and voltage rating. The die yield per wafer was calculated using Murphy's model for the defined manufacturing specification[105]. The die size was procured through literature and validated to have the present state-of-art specific on-resistance Rds-A [106,107]. The cost of the wafer was picked from NREL and DOE reports [108,109]. Other cost overheads such as labor, electricity, equipment, facilities, maintenance were calculated from X-FAB reports required to fabricate 5k (6inch wafers per month) and averaged to per wafer [109].

Other costs such as R&D, SG&A and MSP were averaged from publicly- available financial reports from CREE, STMicroelectronics and Infineon.

Key properties of the two 1.2kV and 3.3kV wafers modeled are shown in Table 2.8. The thickness and the doping concentration of the epi-layer both for the 1.2kV SiC JFETs and the 3.3kV SiC MOSFETs were chosen based on literature [109]. Other properties such as the 4H polytype and the 350µm substrate were used as it is most prevalent .

Table 2.8: Key parameters of the SiC Wafer modeled

Property	1.2 kV wafer	3.3 kV wafer
Polytype	*4H-SiC*	
Wafer diameter	*6 inches(150 mm)*	
Epi-layer thickness	10 µm	30 µm
Wafer thickness	350 µm	350 µm
Doping conc.	8 e^{15} /cm^3	$3e^{15}$ /cm^3
Other notes	*N-Type, production grade, , 40 off-axis, 0.015-0.028 ohm-cm, ultra-low MPD ≤ 1/cm^2, 350 um thick w/ 47.5 mm flat, double sided polish Si face CMP epi ready, with SiC epi;*	

The present status of specific on-resistance Rds-A (mΩ-cm2) versus Blocking Voltage (BV) at room temperature is shown for a SiC JFET in Fig. 2.20(a) and for an HV SiC MOSFET in Fig. 2.20(b). One advertised datum of UnitedSiC (now part of Qorvo) Gen-4 (G4) 1.2kV SiC JFET has an Rds-A = 1.3 mΩ-cm^2 [1] as shown in Fig. 2.20(a). The best-in-class CREE and GeneSiC have reported Rds-A = 11-12 mΩ-cm^2 as shown in Fig. 2.20(b).

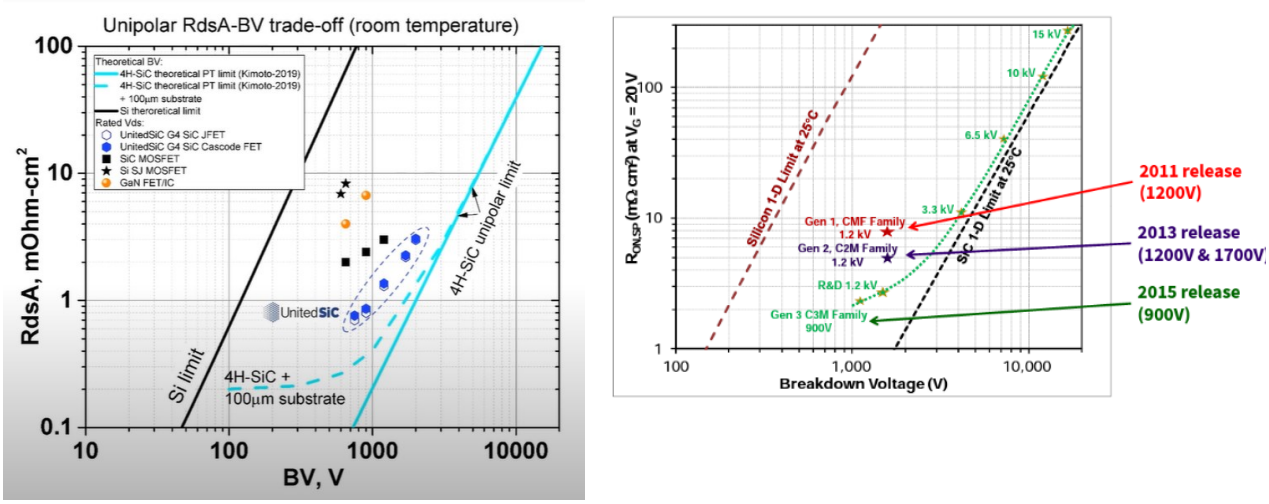


Fig. 2.20: Blocking voltage vs $R_{ps,on}$ trade-off for (a) SiC JFETs [110] (b) 4H-SiC vertical MOSFETs [111,112]

Using the specific on-resistance for a 1.2kV/4 mΩ SiC JFET device that measures 5.73 mm x 6.25 mm the die design is shown in Fig. 2.21(a). For the wafer or epi quality and manufacturing specifications below, the wafer map for 100% yield is shown in Fig. 2.21(b). (Using Murphy's Model of Die Yield). The device has a specific on-resistance of 1.3 mΩ-cm^2, measures 5.73 x 6.235 mm and has an active area of 0.32 cm^2, rest of the area is device passivation and guard rings. The device has a specific on-resistance of 11.3 mΩ-cm^2, measures 7.2 x 7.2 mm and has an active area of 0.33 cm^2, rest of the area is device passivation and guard rings.

Murphy's model is used to determine the number of dies per wafer. For the 1.2kV/4mΩ SiC JFET, the following manufacturing specifications are used:

Manufacturing specs: die width (w) = 5.625 mm, die height (h) = 6.25 mm, horizontal and vertical scribe lane = 1 mm, edge loss (mm) = 5 mm, defect density = 0 (#/sq. cm) (for 100% yield, i.e. 0% defects), centered die and no manual wafer placement.

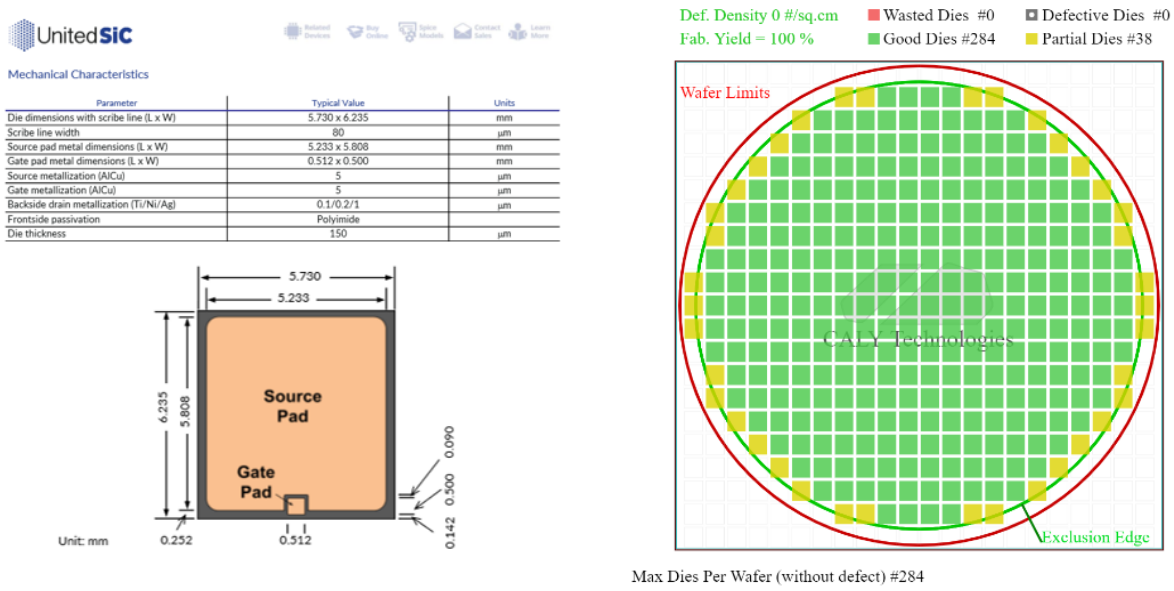


Fig. 2.21(a): Die design of 1.2kV/3.5 mΩ SiC JFET; (b): Wafer map for the 1.2kV/3.5 mΩ devices in a 6 inch wafer (for 100% yield) [105]

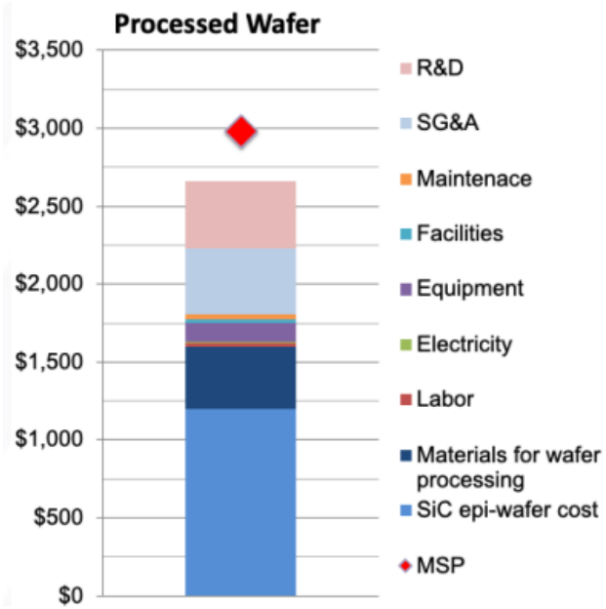


Fig. 2.21 (c): MSP breakdown for the SiC 10µm (i.e 1.2kV) epi-wafers

For 100% yield, each wafer produces 284 good power dies and 38 partial or non-usable power dies. The cost of each wafer is dependent on the volume of manufacturing, EPI layer and volume. With the given EPI layer, it is reasonable to assume $1200 (confirmed by multiple

sources) [108]. *Yole is predicting a 48% price drop by 2025. Fig. 2.21(c) shows the cost modeling results for SiC epi-wafers. The MSP (minimum sustainable price) that a company must sell is $2950 to pay back the capital and operating expenses during the plant lifetime [129]. The cost per die for different yield scenarios from the wafer is shown in Table 2.9.

Table 2.9: Cost/die for 1.2kV/3.5 mΩ devices for volume manufacturing

Scenario @ Volume pricing	$/die
Anticipating 100% Yield	$ 10.39
Anticipating 90% Yield	$ 11.54
Anticipating 80% Yield	$ 12.97
Anticipating 70% Yield	$ 14.84

Similarly, using the specific on-resistance for, a 3.3kV/34 mΩ SiC MOSFET device that measures 7.2 mm x 7.2 mm, the die design is shown in Fig. 2.22 (a). For the wafer or epi quality and manufacturing specifications below, the wafer map for 100% yield is shown in Fig. 2.22 (b). (Using Murphy's Model of Die Yield)

Manufacturing specs : *Die width (w) = 7.2 mm, Die height (h) = 7.2 mm, Horizontal and Vertical Scribe Lane = 1 mm, Wafer diameter (mm) = 150 mm (6 in), Edge loss (mm) = 5 mm, Defect Density = 0 (#/sq. cm) (For 100% yield, i.e. 0% defects), Centered die and no manual wafer placement*

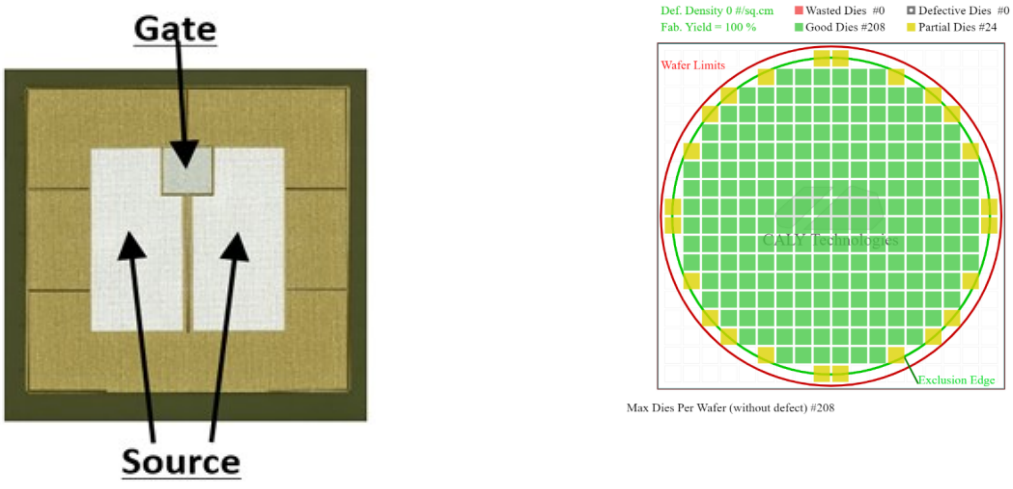


Fig. 2.22(a): Die design of 3.3kV/34 mΩ SiC JFET [106]; (b): Wafer map for the 3.3kV/34 mΩ devices in a 6 inch wafer (for 100% yield) [105]

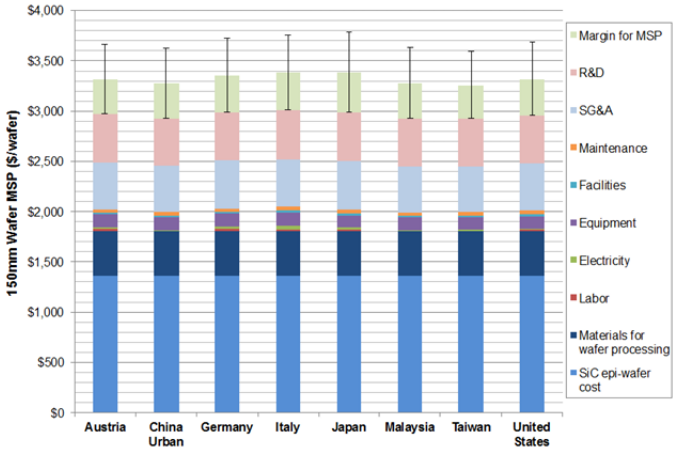


Fig. 2.22 (c): MSP breakdown for the SiC 30 µm epi-wafers

For 100% yield, each wafer produces 208 good power dies and 24 partial non-usable power dies. With the given EPI layer, it is reasonable to assume $1350 (confirmed by multiple sources) [130]. *Yole is predicting a 48% price drop by 2025. Fig. 2.22(c) shows the cost modeling results for SiC epi-wafers. The MSP (minimum sustainable price) that a company must sell is $3700 (in the USA) to pay back the capital and operating expenses during the plant's lifetime. The cost per die for different yield scenarios from the wafer is shown in Table 2.10.

Table 2.10: Cost / die for 3.3kV/40 mΩ SiC MOSET devices for volume manufacturing

Scenario @ Volume pricing	$/die
Anticipating 100% Yield	$ 17.79
Anticipating 90% Yield	$ 19.76
Anticipating 80% Yield	$ 22.24
Anticipating 70% Yield	$ 25.41

Cost Comparison :

Case 1: To realize a 6.5 kV/24 mΩ power switch, **six "1.2 kV SiC JFET/3.5 mΩ" or six "3.3kV SiC MOSFET/40 mΩ"** (2 in series, 3 in parllel) power devices are required. Thus, the net semiconductor cost is $ 62.28 for the Cascaded SuperCascode approach and $ 106.73 for an approach utilizing series and parallel connect HV SiC MOSFETs. Therefore, an HV SiC MOSFET approach is 71% higher in cost to realize a 6.5 kV/24 mΩ power module than a SiC

CSCPS approach.(assuming 100% die yield /wafer) The actual savings will be greater because low voltage device yields are generally higher.

Case 2: To realize a 12 kV/24 mΩ power switch, **twenty-four "1.2 kV SiC JFET/3.5 mΩ"** (with 12 in series, 2 in parllel) **or twenty-four "3.3kV SiC MOSFET/34 mΩ" (4 in series, 6 in parallel)** power devices are required. Thus, the net semiconductor cost of is $ 249.12 for the Cascaded SuperCascode approach and $ 426.92 for an approach utilizing series and parallel connect HV SiC MOSFETs (assuming 100% die yield /wafer). Therefore, an HV SiC MOSFET approach is 71% higher in cost to realize a 12 kV/24 mΩ power module than a SiC CSCPS approach. The actual savings will be greater because low voltage device yields are generally higher.

Also note that paralleling six (6) strings of four (4) serial 3.3kV MOSFETs (each needing individual gate drives) is much more difficult than paralleling two (2) strings of twelve (12) serial 1.2kV self-triggering JFETs. The other advantage is that the CSCPS uses a balancing circuit that inherently balances and removes the need for any conditioning circuits, such as snubbers, compared to MOSFET circuits.

CHAPTER 3: Segmented Baseplate High Voltage Packaging

This chapter focuses on power electronics packaging for high voltage (*3.3 kV to >25kV*), high temperature (≥ 225^0C) power modules operating for high-frequency Wide Band Gap (WBG) power semiconductor devices, i.e. SiC (and GaN). The goals for the packaging are high power density with long-term reliability to support system compatibility. The design utilizes ultra-thin substrate dielectrics with segmented baseplate with thermal via's to reduce ground current by minimizing coupling capacitances without trading-off thermal resistance. The research also explores dielectric fluid cooling for its thermal heat extraction and voltage isolation. The research also explores EHD challenges in dielectric field.

Two module design examples of a 1-layer *6.5kV/105 A 2S-3C* CSCPS and a 3-layer *24kV/105 A 2S-3C-2C-2C* CSCPS are described along with multiphysics simulations to analyze the thermal and electrical performance.

3.1 Organic Power Packaging

An ideal HV power module substrate should have high dielectric strength, provide CTE match, low modulus, high thermal conductivity, be cost-effective and lightweight and withstand high temperature (*>200*^0C). Copper-clad ceramic substrates, such as Direct-Bonded-Copper (DBC) with *AlN,* Al_2O_3 or Si_3N_4 is a benchmark with a relatively low coefficient of thermal expansion (CTE) and high thermal conductivity [113,114]. However, due to high cost of DBC substrates and high weight density, alterative approachs are required.

Organic laminate substrates, widely-commercialized for wearable electronics applications [115]-[117], are one such solution. As an attractive dielectric material, polyimides have been used widely as flexible printed circuit boards (Flex PCBs) in the field of aerospace, automotive, and wearable electronics, fulfilling an increasing need for materials that can perform well under

harsh conditions such as elevated temperatures up to 230^0C [116]. Another alternative is ultra-thin Epoxy Resin Composite Dielectric (ERCD), the resin material is filled with aluminum oxide (Al_2O_3) and aluminum nitride (AlN) resulting in thermal conductance comparable to Al_2O_3 based DBC substrates. The CTE of ERCD is also close to copper ($16.7\ ppm/^0C$), compared with ceramic in traditional DBC substrate ($4.5\text{-}7\ ppm/^0C$), which is beneficial for better thermal stress management on power module during fabrication and lifetime usage. The detailed composition of the epoxy-resin dielectric is also investigated as shown in Fig. 3.1, at *5000X* magnification [117]. There are large amounts of spherical particles distributed in the epoxy-resin, the particle size ranges from $5\ \mu m$ to $40\ \mu m$. The primary properties of the ERCD material and flex polymide are shown in Table.3.1. Low modulus of ERCD compared to *310~345 GPa* for Al based metal compounds makes it a softer material supporting higher reliability during thermal cycling. ERCD can withstand high voltage (*40 kV/mm*) and operate up to $300\ ^0C$ continuously while being easier to manufacture, which is indispensable for high power applications.

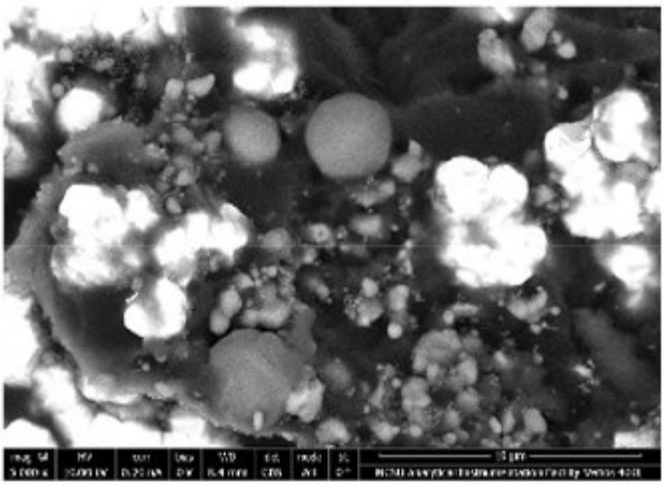


Fig. 3.1: SEM Image for internal Microstructure of the Epoxy-resin dielectric material [117]

Table 3.1: Material properties of ERCD laminates in comparison to Flex/Al_2O_3				
Parameter	Al_2O_3	Flex (Polyimide)	ERCD	Units
Thermal Conductivity	24	0.16	10	W/mK
T_g	-	300	270	^{0}C
Modulus	340	2.5	30	GPa
CTE (alpha 1)	4.5-7	14-17	10-17	ppm/^{0}C
Dielectric strength	20 / mm	5 @ 120 µm	5.6 @ 120 µm	kV

Epoxy-resin dielectric can be manufactured in ultra-thin thickness of 80 *µm* and 120 *µm*. The 120 *µm* had dielectric strength of *5.6 kV*. An *80µm* dielectric with *70µm* Top Cu and 210 *µm* bottom Cu was tested to measure leakage current at different voltage and temperature in [117]. The DC leakage current was measured at ≤1nA 25^{0}C up to *20uA* up to *250^{0}C* at *1200 V* , which is comparable with SiC devices leakage at similar conditions. The cost comparison of ERCD with DBC obtained using RFQs from organic (ERCD) and DBC substrate manufacturers in 2021 is shown in Fig. 3.2. As shown, the high-volume epoxy substrate from Brigitflex (US) and TCI (Taiwan) are substantially less than DBC. (Based on a *100/120/100 µm* Cu/ERCD/Cu substrate and an *200/635/200 µm* Cu/Ceramic/Cu DBC substrate).

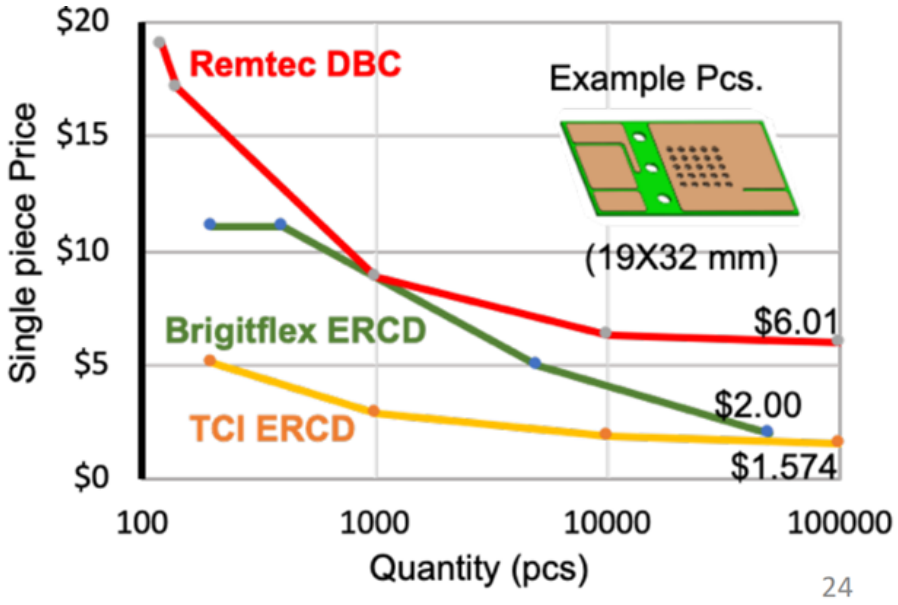


Fig. 3.2: Cost comparison of DBC with ERCD for a *19 x 32 mm* sample obtained using RFQs

3.2 Considerations in power module design with organic epoxy laminates

One of the challenges of using a thin substrate, ERCD which can be fabricated as thin as *120μm* is the increased dielectric coupling to baseplate which with a fast voltage change at the node draws additional current from the gate driver or the DC-bus, adding additional power loss on the devices. The inrush current can be calculated using the following equation:

$$i = \frac{\varepsilon A}{d} * \frac{dV}{dt} \tag{1.8}$$

Here, d is the seperation between the two parallel conductors, A is the area of cross-section and dV/dt is the voltage switching rate. The inrush current causes unexpected voltage sags which can limit driving speed and cause extra device loss, derating the application. Multiple techniques of reducing common-mode current have been discussed in the past (i) slowing down devices (ii) integrating a screen inside the power module (iii) stacking insulating substrates and (iv) connecting the switching node to either the positive or negative DC bus. In [118], Infineon patented a method to divert the current back to the DC bus, wherein the semiconductor devices are mounted to ceramic substrates, stacked on top of each other increasing the high-frequency impedance. By connecting the middle layer to capacitance, and lowering the impedance of the path. It is viable to re-circulate the current back into the bus instead of through the system ground.

This technique was utilized in the design of a 10kV SiC MOSFET, reported in [119]. Tested at *2kV/20A* the module switching at a *dV/dt* of *24V/ns* (turn-off transient rise time is *66 ns*) successfully demonstrated an order of magnitude reduction in common mode current (from *2* to *0.2A*) achieved by reducing parasitic capacitance form *46 pF* to *36 pF* . However, to compensate for the increased junction-to-case thermal resistance due to stacked substrate the

module required a direct-substrate, jet-impingement cooler integrated in the module housing [121,122] as shown in Fig. 3.3.

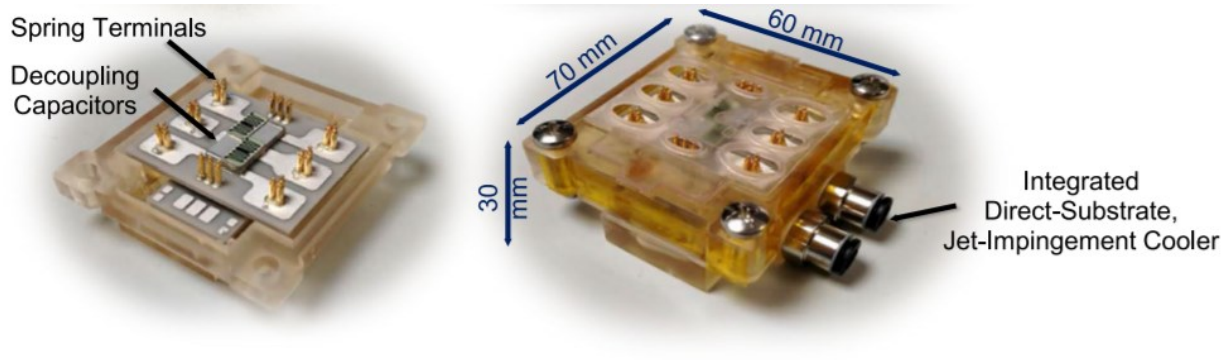


Fig. 3.3: Jet-impingement cooled 10kV SiC MOSFET power module [122]

WBG devices can be operated at 175^0C temperatures unlike Si devices which were limited to 125^0C, therefore with power cycling the devices can undergo larger temperature swing. Due to CTE mismatch between the ceramic substrates and copper this temperature swing can induce solder stress or cracking which is a concern for long term power module reliability. In comparison, ERCD is a relatively low modulus material which allows us to release stress and strain of solder layer under chip. Conventional power modules use silicone gel encapsulation to provide voltage isolation and protect the module from dust, moisture, etc. Epoxy resin based encapsulation materials can reduce solder cracks, enhance lifetime of thermal cycling and improve power cycling due to reduced stress on wire bonding.

Further using direct potting resin in liquid state in comparison to transfer molded epoxy resin encapsulation (solid state) allows higher flexibility in design and high density packaging, shown in Fig. 3.4.. The utilization of this direct plotted resin in IGBT power module has been reported by Mitushibi in developing their SLC package[122,123].

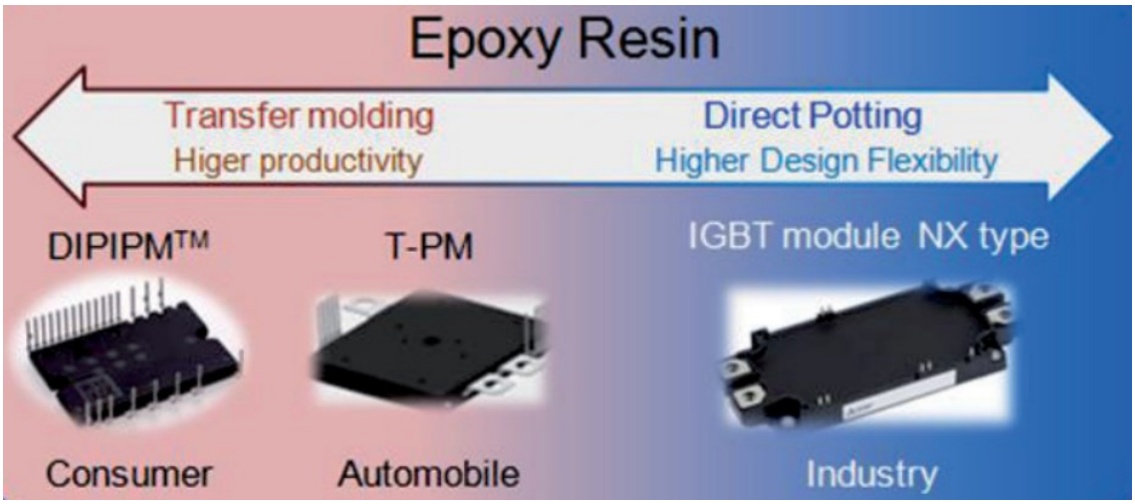


Fig. 3.4: Epoxy resin encapsulated power modules [122]

For design the direct potted resin should have T_g greater than the operating temperature of the power module, CTE of resin should match the dominant structural member causing the warpage [123]. The resin particle size should be optimized to reduce voids and enhance both thermal conductivity and withstand voltage characteristics. Properties of epoxy resin encapsulants with silicon gel is plotted in Table 3.2.

Table 3.2: Comparison of material properties of silicone gel vs epoxy encapsulates

	Coefficient of thermal conductivity (W/mK)	Dielectric Strength (kV/mm)	Coefficient of thermal expansion (ppm/K)	Volume Resistivity (Ω-cm)
Henkel LOCTITE® SI 5620™	0.16	21.14	315	3×10^{15}
Risho High thermal conductivity material [Confidential development material under NDA]	1.9	15	17	4×10^{16}

3.3 Common-coupling issue in thin substrates

Parasitics like resistance, inductance and capacitance in the electro-physical layout of the power module dampens the switching performance of the power device, causes EMC issues, etc. Here the key performance degrading inductance and resistance parasitics are present in the gate driving loop and the commutation loop whereas coupling capacitances, include, but are not limited to mutual inductance between two parallel conductors, which in case of DBC modules is through the substrate between the top and bottom copper or the common baseplate. Fig. 3.5 shows the coupling capacitance with reference to the bottom Cu, charging and discharging paths and common mode current flow direction in a half-bridge power module.

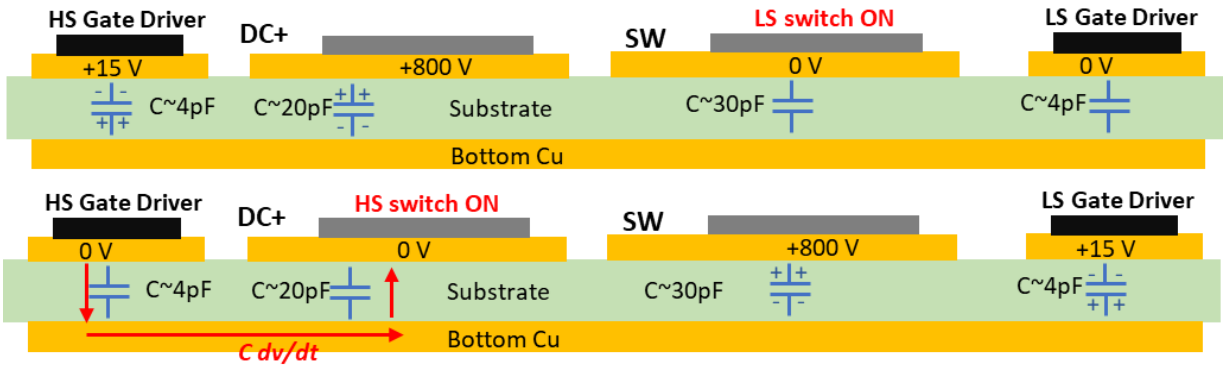


Fig. 3.5: Electro-physical layout of a half-bridge power module showing parasitic capacitance and resulting common mode current

This capacitance coupling is dependent on the substrate thickness and common mode current is directly proportional to the coupling capacitance.

3.4 Thermal and Capacitive coupling tradeoff in DBC modules

A typical Direct Bonded Copper (DBC) power module structure is shown in Fig. 3.6. The capacitive coupling with respect to the baseplate depends on the thickness of the dielectric and the size or area of the cross-section of the power module.

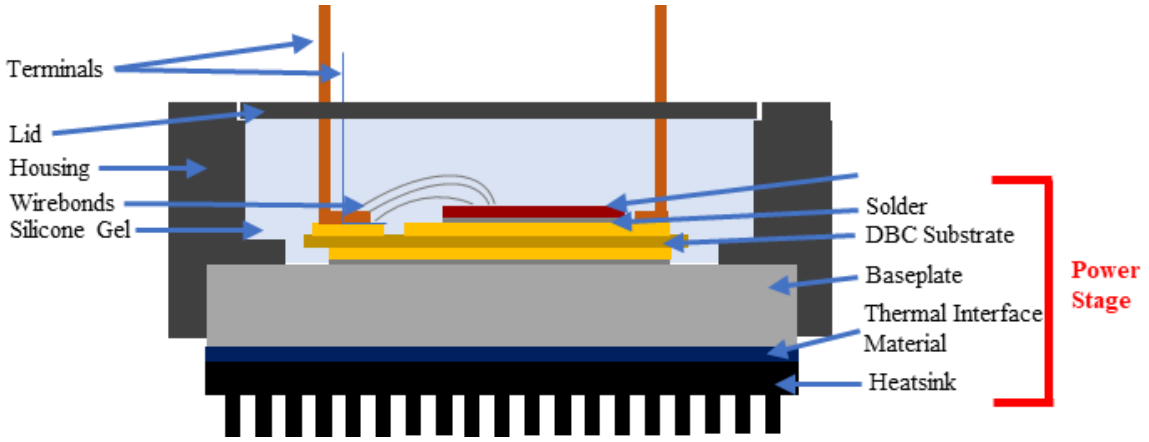


Fig. 3.6: Typical power module structure

This capacitance to the ground can be defined as:

$$C = \frac{\varepsilon_r \varepsilon_0 A}{t} \tag{3.1}$$

Here, *'A'* is the area of overlap of the between the top Cu and bottom Cu of the DBC substrate, shown in Fig. 3.5, '$\varepsilon_r \varepsilon_0$' is the dielectric constant, and '*t'* is the thickness of the substrate. The minimum dimension '*t'* is dictated by the dielectric properties of the substrate. As the voltage rating of the power module scales, '*t*' scales. The greater the *'t'* less will be the capacitive coupling and common mode current (or ground current) and vice versa. For a fixed '*t'* reducing the '*A'* by breaking down a common baseplate, also reduces the coupling capacitance. On the other hand, the thermal resistance and thermal capacitance of a module increase directly with '*t'* as:

$$R_{th} = \frac{t}{\lambda A} \tag{3.2}$$

$$C_{th} = c\rho tA \tag{3.3}$$

Here, λ (*W/mK*) is the thermal conductivity of the material, ρ (kg/m^3) is the material density, *c* (*J/kg.K*) is specific heat.

3.5 Philosophy of Segmented baseplate Power Module

Conventional power modules may use either a Direct bonded copper (DBC) or Insulated Metal Substrate (IMS), which have been proven over the years for Silicon (Si) devices. New age, Wide Band Gap (WBG) power devices require optimization of the physical stack-up to realize the potential of these power devices requiring exploration of new packaging materials, techniques, etc. One of the key challenges for HV power module design is the thick dielectric substrate which scales with voltage and also negatively affects thermal resistance, coolant system design and increases in-system complexity. This research introduces segmented-baseplate power packaging to tackle this key challenge.

Segmented-baseplate power packaging uses ultra-thin Epoxy Resin Composite Dielectrics (ERCDs) and moves the "electrical isolation" challenge into Level-2 packaging by placing segmented pin-fin heat sinks under the power semiconductors devices with interconnecting thermal via's to avoid a common metal baseplate under all devices. Using ERCD as an alternative to traditional metal-clad ceramics enables low-cost and highly reliable power modules with favorable mechanical and thermal properties. All segmented pin-fin heat sinks are dielectric cooled to eliminate having a continuously electrically conductive base plate. Dielectric fluids provide electrical insulation, suppress corona and arcing, and also serve as a coolant. Instead of creating a lumped capacitance the fluid creates distributed capacitance with each individual heatsink which helps with increasing the density of the power module. The segmented heat sink approach together with the Cascaded SuperCascode switching topology allows spreading the electric field density throughout the module, decreasing the peak field density offers a power-dense design.

3.6 *Design of a 6.5kV/105A 1-layer 2S-3C CSCPS with Segmented Baseplate*

The power module layout is designed to comply with isolation standards to minimize leakage current and peak electric field strength. The module is designed to accommodate one stacked Cascode (UnitedSiC – UF3S120009) and five individual JFETs (UnitedSiC – UF3N120008), shown in Fig. 3.7. The circuit schematic is shown in Fig. 3.8. The first pass physical layout of the power module is illustrated in Fig. 3.9. In the layout, the auxiliary balancing network of the CSCPS is split into two parts and placed on each side of the central Cu pads. Each of the central copper pads (underneath the die) has thermal via's (0.5 mm diameter) which when solder filled will electrically connect the top side copper to the backside copper of the substrate.

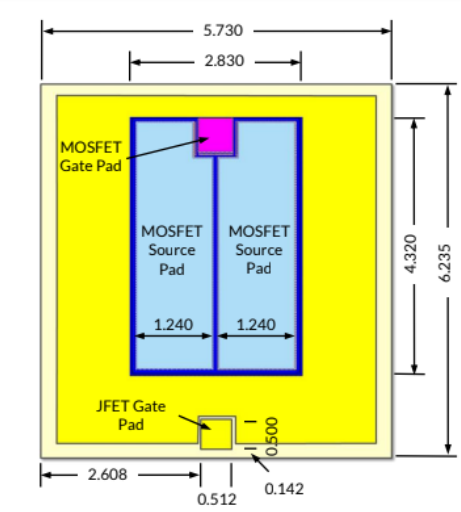


Fig. 3.7(a): 1.2kV/9 mΩ stacked SiC Cascode UF3S120009

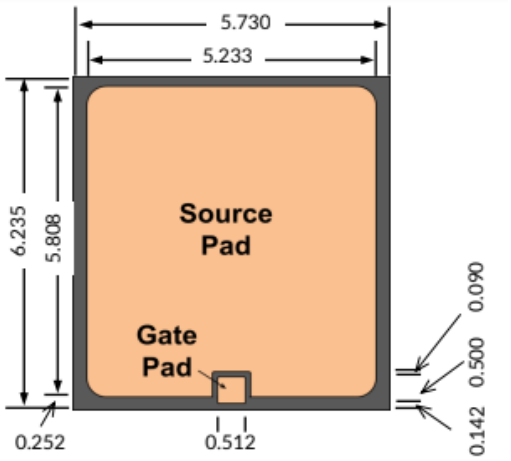


Fig. 3.7(b): 1.2kV/8 mΩ SiC JFET UF3N120008

For this application, class 1 ceramic capacitors in the 0805 form factor are used for their high stability and low losses. Their high accuracy and tolerance and stability to voltage, frequency and temperature make them suitable for balancing network.

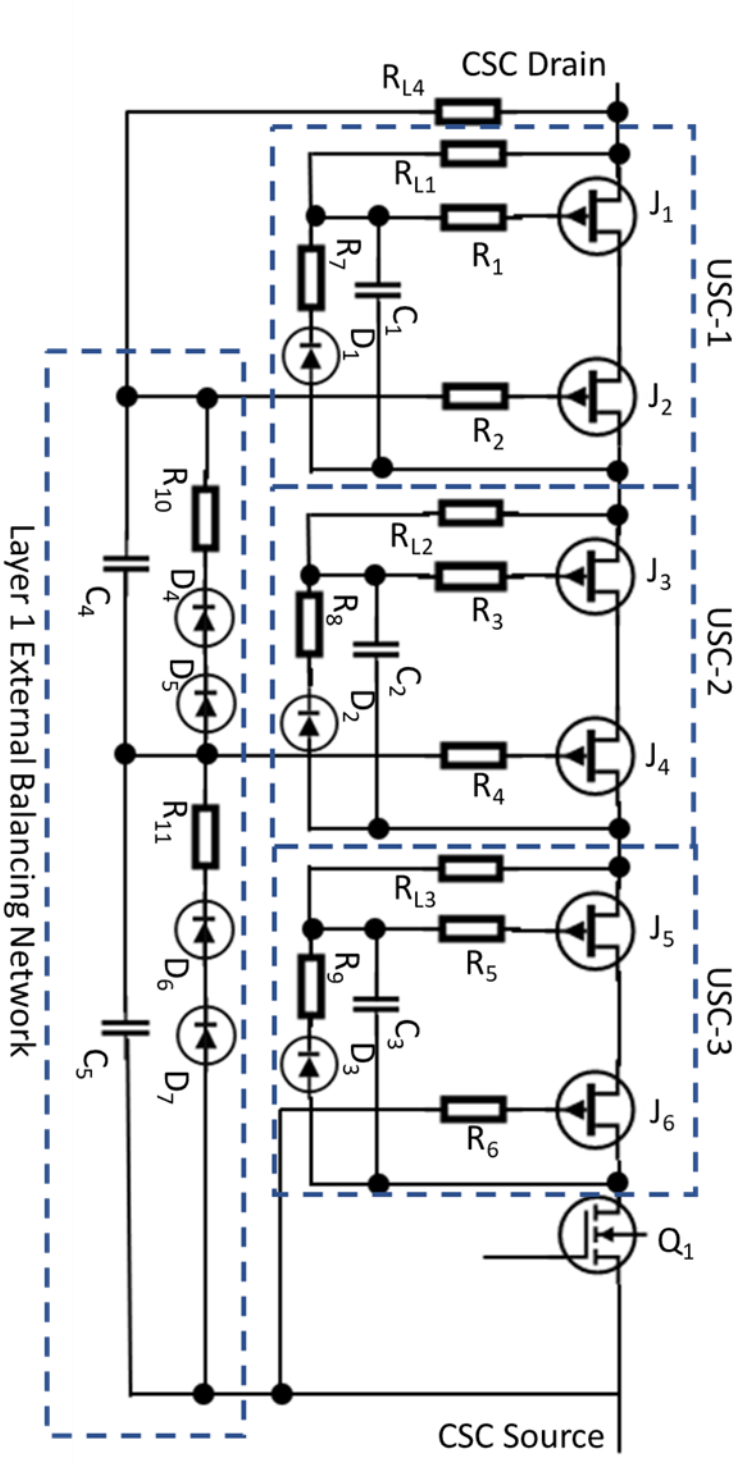


Fig. 3.8: Six-JFET 2S-3C Cascaded SuperCascode Power Switch

(Here Q1 is the MOSFET, J¬1-J6 is the JFET, R1-R6 are gate resistors, C1-C5 are balancing capacitors, RL1-RL4 are leakage resistors, D1-D7 are avalanche diode)

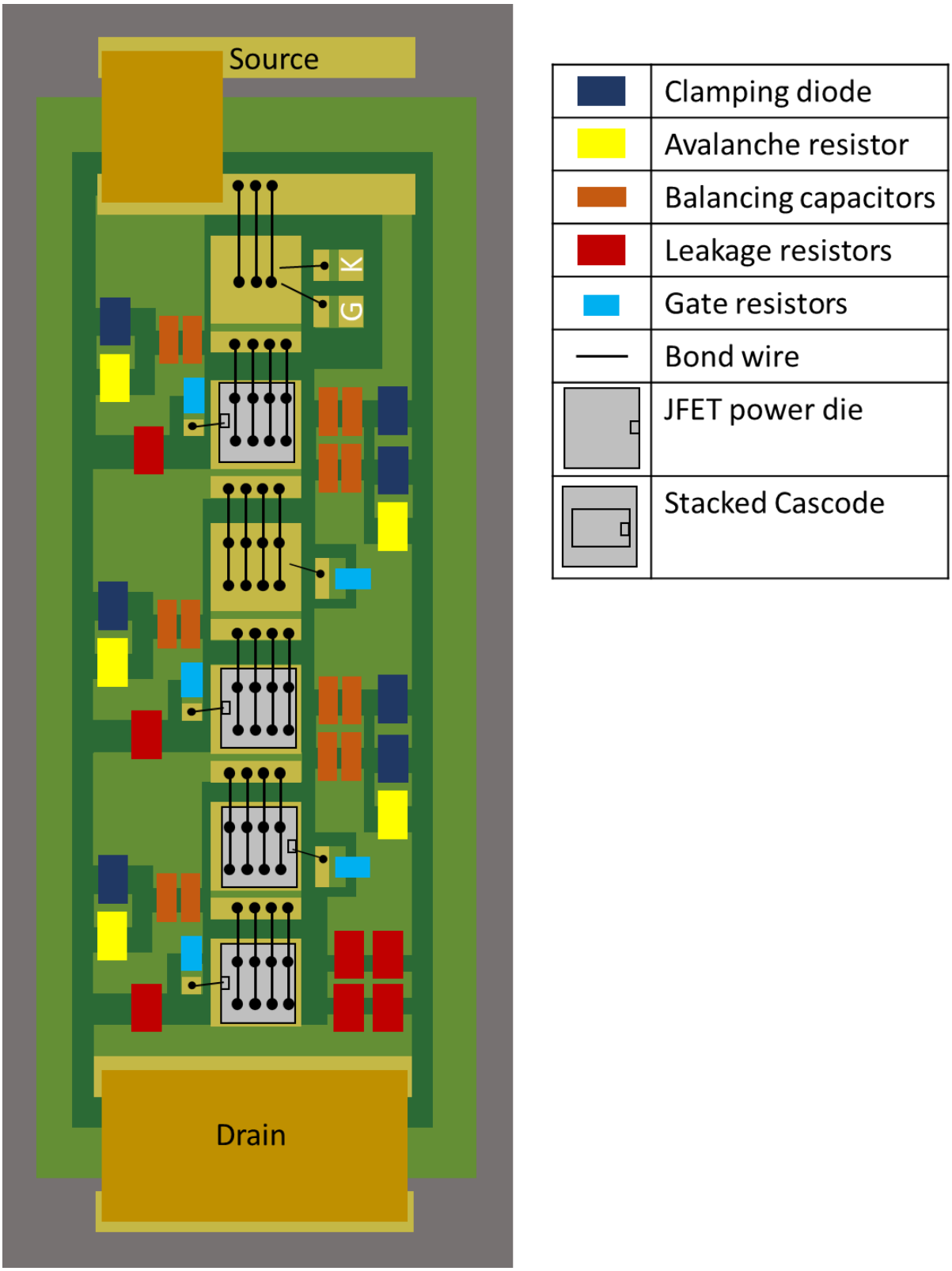


Fig. 3.9: Power module physical layout implementation

3.6.1 Thermal Via's

Thermal via's are placed below each die in the power module with a segmented baseplate or individual heatsink per die which transitions the voltage isolation requirement into the next level of power packaging, substantially reducing the thermal resistance. An array of solder-filled thermal via's are placed below each JFET power die to provide a direct thermal path enabling high power handling capability as shown in Fig. 3.10.

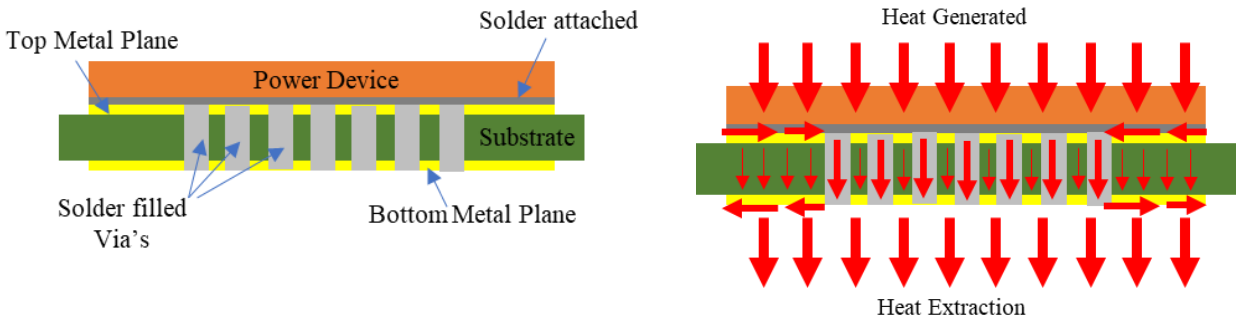


Fig. 3.10: (L) Thermal via's under SiC JFET die (R) Heat flow between the top surface of the die and the underside of the lower copper plane

Using the manufacturing and mechanical guidelines highlighted in [128], the separation between two thermal via's was kept fixed at ≥1 mm and 0.5 mm diameter thermal via's are set as boundary conditions for this study. Note, the guidelines used were taken from glass re-inforced FR4 PCBs and applied for Epoxy Resin Composite Dielectric (ERCD) due to the lack of similar guidelines for ERCD at the time of this research. The below guidelines only give first-step optimization and work can be expanded using the design discussion below.

For the power dies selected and shown in Fig 3.7, the number of via's and hole diameter were optimized using an analytical model based on the boundary conditions to achieve minimum junction-to-case thermal resistance. The optimal number of vias was calculated using a series of FEA simulations to calculate the peak power dissipation rating of the module. The study is done

following PCB manufacturing guidelines and uses the material thermal parameters highlighted in Table 3.3.

Table 3.3: Dimension and thermal properties of the power module stack up

Component	Thickness (mm)	Pad dimension (mm)	Thermal Conductivity (W/mK)
Power Device (SiC)	0.015	5.73 x 6.25	450
Solder (Die to DBC, Sn63Pb37)	0.050	8 x 7	50
Top Copper	0.2	8 x 7	400
Substrate (ERCD)	0.36	8 x 7	10
Via	0.36	0.5 (Diameter)	50
Bottom Copper	0.2	8 x 7	180

To run the simulation a heat flux is applied to the power die, (i.e the peak power dissipation) and diverging heat flux from the heatsink fins. All other surfaces are kept thermally isolated. The net thermal resistance is calculated using the difference between die junction temperature and the ambient temperature divided by the power dissipation applied. To determine the optimum number of thermal vias the number of via's and matrix arrangement were varied from 8 to 30. The thermal resistance for each stack is shown in Table 3.4 and the junction-to-case thermal resistance drops from 0.95 ^{0}C/W to 0.44 ^{0}C/W, which is a 54% reduction. The results also show that beyond 20 via's there was no significant decrease in thermal resistance, beyond <5%.

Table 3.4: Results of FEA calculations

Matrix	Number of via's	Via pitch (centered on 8 x 7 mm pad)	Thermal Resistance	
(Row x Column)		Row sep x Colum Sep	(^{0}C/W)	(% Reduction)
4 x 2	8	1 x 4	0.95	-
5 x 2	10	1 x 4	0.82	14 %
4 x 3	12	1 x 1.5	0.76	20 %
4 x 4	16	1 x 1	0.62	34 %
6 x 3	18	1 x 1.5	0.54	43 %
5 x 4	20	1 x 1	0.45	52 %
6 x 4	24	1 x 1.25	0.44	54 %
6 x 5	30	1 x 1	0.40	57 %

3.6.2 ERCD substrate layout

The ERCD top layer and bottom layer layout are designed in Altium Designer, shown in Appendix E. A 1 mm copper margin distance is guaranteed on both sides of the power die, to guarantee sufficient thermal spreading. A 2 mm spacing is kept between the central power die to ensure no thermal interface due to the neighboring power die and ensure low leakage based on the voltage blocking capability of the encapsulant. A 4 mm Cu-ring is added and silkscreened around the layout to add extra robustness to the thin brittle ERCD substrate. A 3D rendering of the overall masked ERCD board is shown in Fig. 3.11 and an optimized populated design is shown in Fig. 3.12.

The layout measures 89 x 45 mm and a further *41 %* size reduction is possible by optimizing component selection and sizing for the die shown in Fig. 3.7. Note: This design was made generic to house any JFET which measures less than 8 mm on the side with an option to put additional balancing network components to support different current and voltage rating.

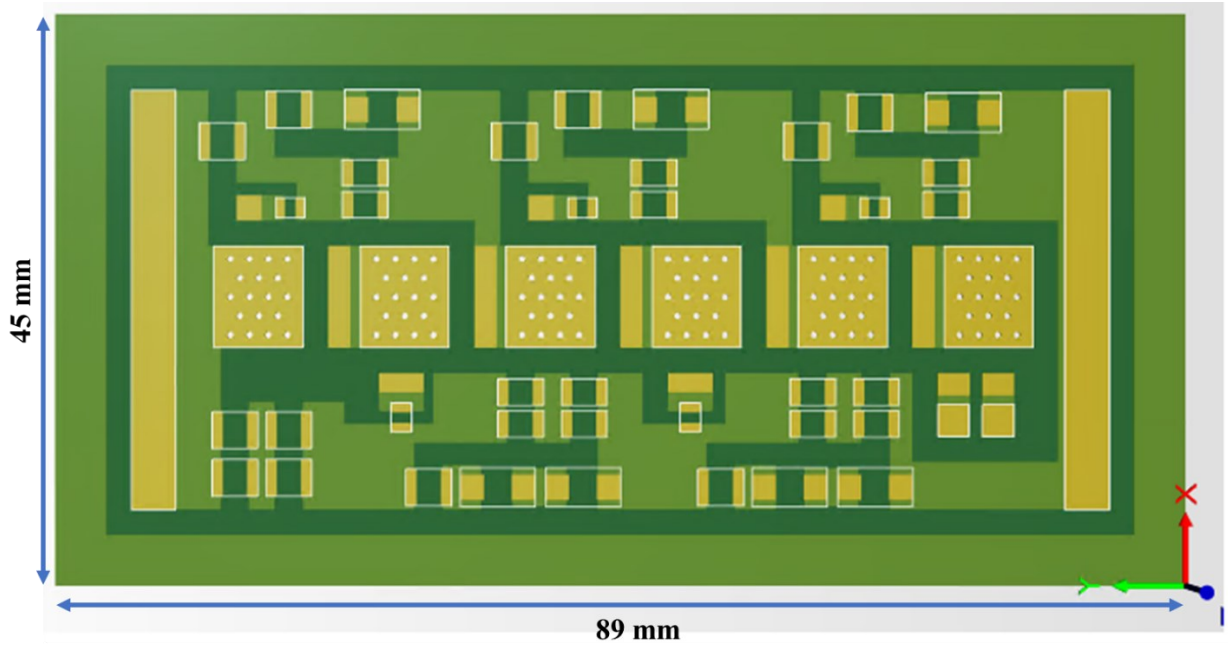


Fig. 3.11(a): Top view 2D rendering of the ERCD layout

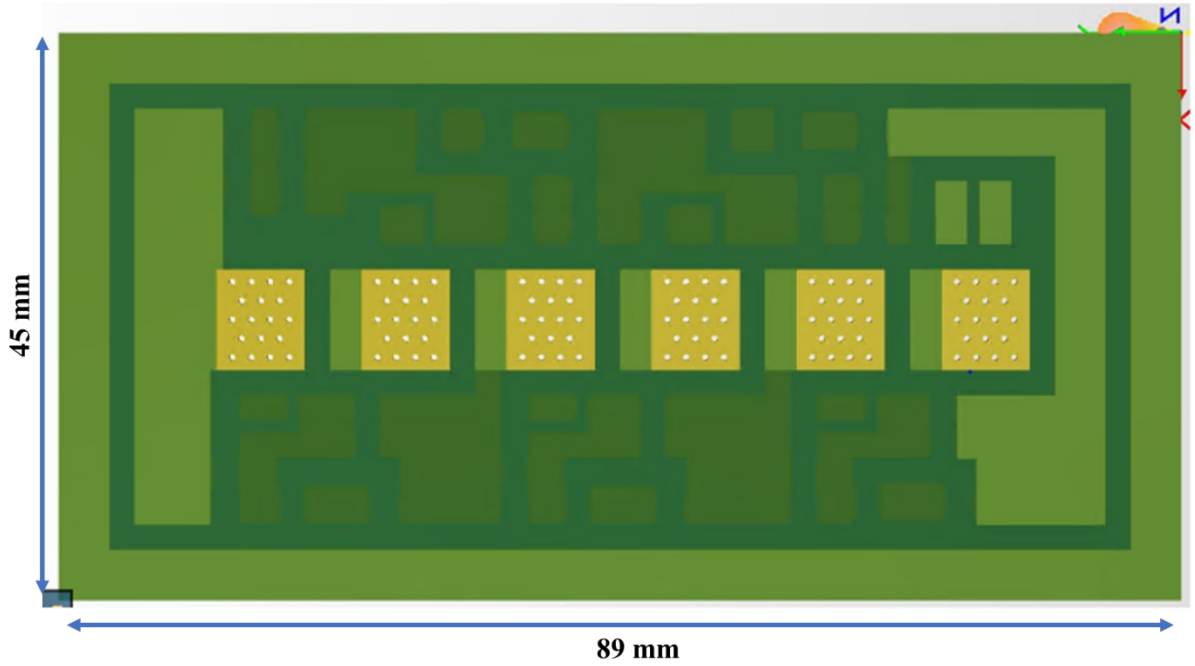


Fig. 3.11(b): Bottom view rendering of the ERCD design

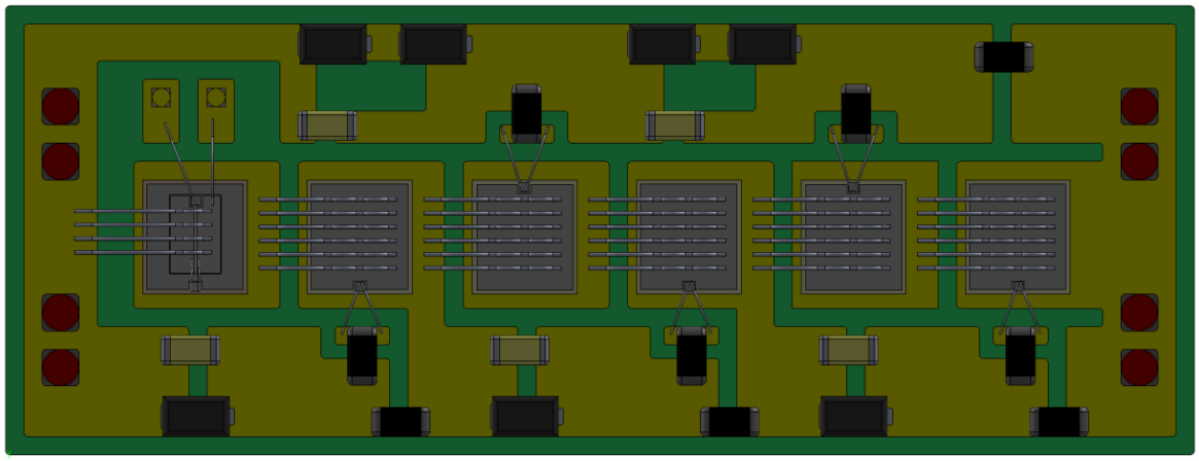


Fig. 3.12: 2D rendering of the size optimized module layout (components shown to scale) for a six JFET 2S-3C CSCPS shown in Fig. 3.7 and Fig. 3.8

3.6.3 Housing and Terminal design

The stray inductance in the copper trace along the power path induces a voltage overshoot when switching at high *di/dt*. Further, this inductance also causes avalanche energy power loss, which can cause device failure and additionally for CSCPS, can cause the failure of balancing network components, especially the diodes. For example, a stray inductance of 50 nH

in the decoupling loop at 100 A stores 0.25 mJ of energy, which at 10 kHz switching causes 25 W of power loss (assuming no junction capacitance). This energy, according to the avalanche diode datasheet (Vishay - AU1PM) is sufficient to cause breakdown and affect the working of the balancing network. Thus, for this terminal design, inductive cancellation is used.

Trace inductance can be closely approximated as

$$L = \frac{\mu A}{w} \tag{3.4}$$

here, μ is the absolute permeability of the dielectric, d is the thickness of the trace, A is the cross-section area of the trace. By folding the terminals onto the housing body and overlapping it in parallel space. The widths of both the traces are the same, the mutual inductive cancellation is a function of separation and length of the overlap and can be represented as (3.7) :

$$M_{12} = \frac{\mu_0}{2\pi}\left[l * log\frac{l+\sqrt{l^2+d^2}}{d} - \sqrt{l^2+d^2} + d\right] \tag{3.5}$$

Here l is the length of the trace (overlapp) and d is the separation between the traces. Assuming l is greater than the distance d, the equation can be simplified as

$$M_{12} = \frac{\mu_0}{2\pi} * l\left[log\frac{l+\sqrt{l^2+d^2}}{d} - 1 + \frac{l}{d}\right] \tag{3.6}$$

This cancellation reduces the inductance in the power-path as noted in (3.5) and (3.6).

$$L = \begin{bmatrix} L_1 & -M_{12} \\ -M_{21} & L_2 \end{bmatrix} \tag{3.7}$$

$$\Delta V = (L_1 + L_2)\frac{di}{dt} - 2(M_{12})\frac{di}{dt} \tag{3.8}$$

The housing body provides mechanical support to the ultra-thin ERCD substrate. The housing body and the top lid fabrication are documented in Appendix F.

An assembled power module 3D rendering is shown in Fig. 3.13. The drain and source terminals connections are on the left side of the power module as shown. The internal drain connection exists on the right and flows across the lid to the left termination. This flow path for current provides inductive cancellation in the main power loop. The module housing and power terminals interface are carefully designed to comply with clearance and creepage requirements, i.e $>6\ mm$ for $6kV$ DC bus blocking. The module interfaces with the next packaging level, i.e system PCB, with gate and kelvin-gate via recepticle pins.

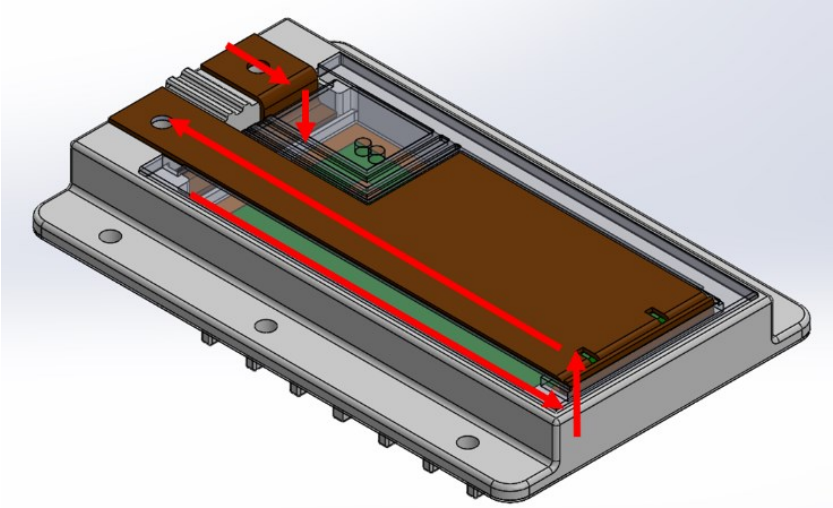


Fig. 3.13(a): Isometric view of power module (red arrow reflect current flow or power path)

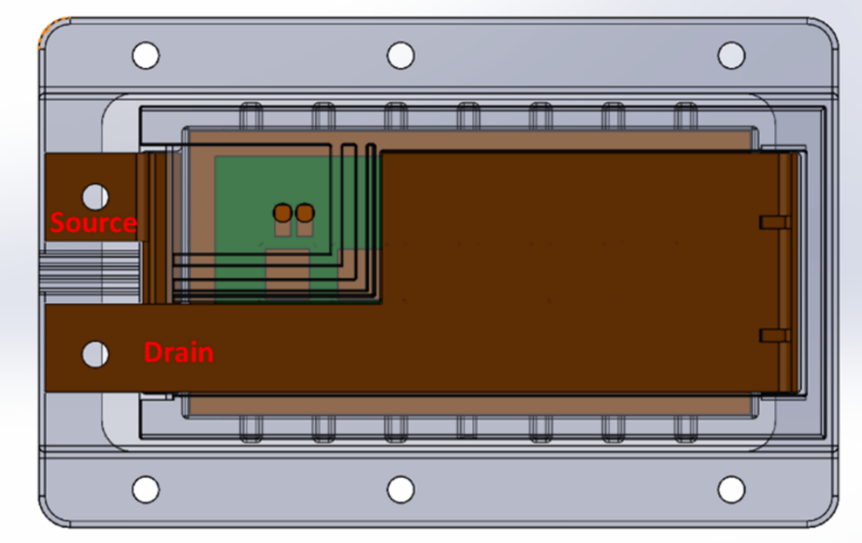


Fig. 3.13(b): Top view of power module terminal layout

3.7 Module simulation and characterization

The power rating of a power module depends on the thermal and electro-design of the power module. Module-level characterization was conducted through analysis of peak electric field, stray parasitics and thermal performance.

3.7.1 Extraction of distributed electrical elements

A Finite Element Analysis (FEA) simulation was performed using Ansys Q3D to evaluate the stray resistance and inductance in the power path. Design rendering of the PCB imported is shown in Fig. 3.14. An electrophysical model and a table with simulated values is shown in Fig. 3.13 and Table 3.5 respectively. The simulation indicates 28.8 nH power loop inductance at 250 kHz and has a DC resistance of 7.5 mΩ. The simulation also indictates that the inductive cancellation technique was able to obtain a 21% reduction in loop inductance. This reduction at 100 A turn-off current, reduces switching energy loss to 0.14 mJ compared to 0.25 mJ. The result shows compatibility and performance improvement over commercially available 6.5kV modules. The Infineon 57Pak IGBT power module typically has a power loop inductance of 50 nH.

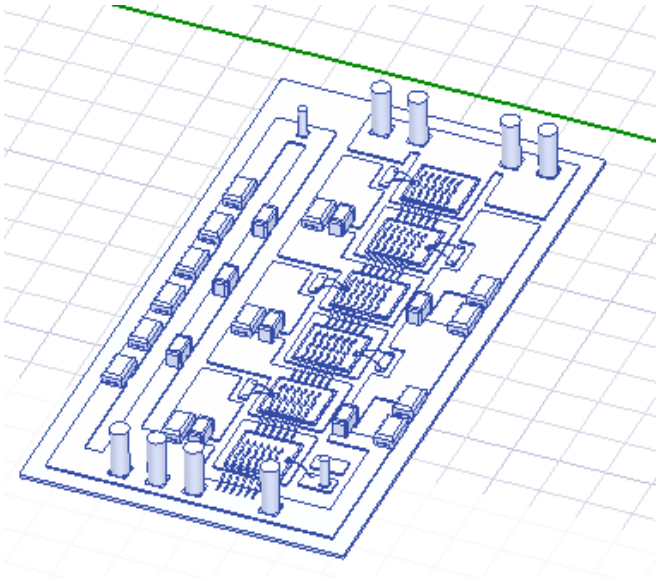


Fig. 3.14: Simulated rendering in Ansys Q3D

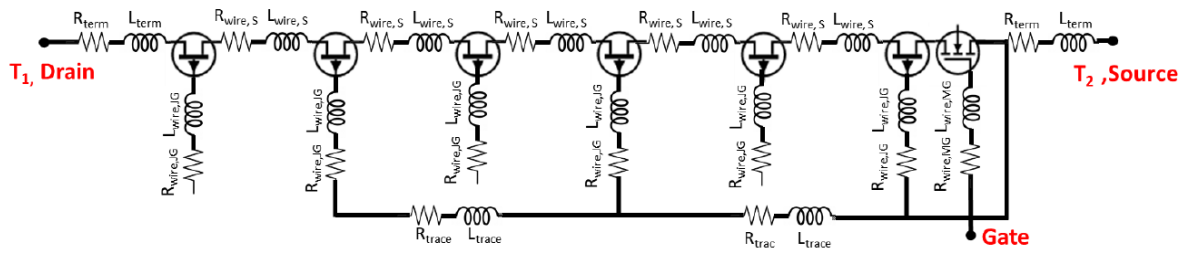


Fig. 3.15: Electrophysical model

Table 3.5: Component values for the electrophysical model shown in Fig. 3.13	
Parameter	Value
R_{term}	1.5 mΩ
L_{term}	7.4 nH
$R_{wire,\ s}$	0.9 mΩ
$L_{wire,S}$	2.8 nH
$R_{wire,\ JG}$	3.38 mΩ
$L_{wire,\ JG}$	7.25 nH
$R_{wire,\ JG}$	12.47 mΩ
$L_{wire,\ MG}$	8.61 nH
R_{trace}	0.82 mΩ
L_{trace}	3.5 nH

3.7.2 Thermal modeling

To evaluate junction-to-case thermal resistance COMSOL multi-physics is used for the simulation. A SolidWorks rendering for the 6.5kV CSCPS, shown in Fig. 3.14 is imported into the software.

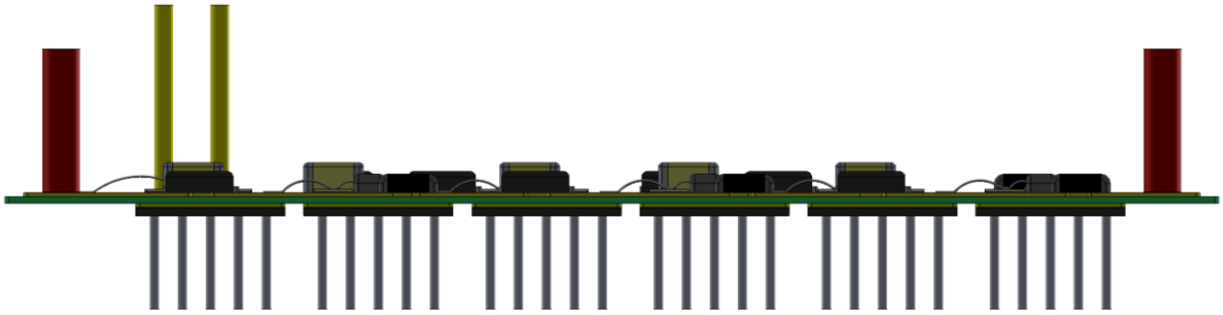


Fig. 3.16(a): Solidworks rendering - Side View of the 6.5 kV 2S-3C ERCD power module

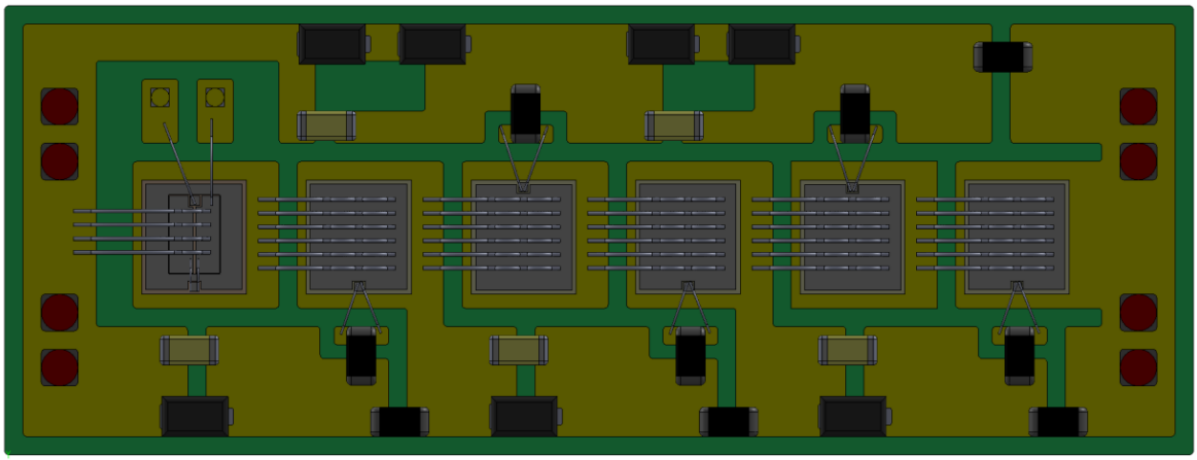


Fig. 3.16(b): Solidworks rendering - Top view of the 6.5 kV 2S-3C ERCD power module

The power module stackup is 200/360/200 µm Cu/ERCD/Cu which has thermal via's created on the center copper traces accounting for *7%* of the top Cu area to provide a direct heat transfer path. The thermal model simulation material and thermal conductivity is shown in Table 3.6. Firstly, 8W heat dissipation is applied to the JFET die and 10W of dissipation is applied to the stacked cascode keeping the backside (heatsink fins) at a constant temperature of 25^0C to calculate the thermal junction-to-case resistance. The surface temperature plots are shown in Fig. 3.17.

Table 3.6: Power module stackup and material properties

	Thickness (mm)	Thermal Conductivity
SiC Die	0.15	450
Die attach solder	0.05	50
Top copper	0.20	400
Solder filled via's	0.36	50
ERCD	0.36	10
Bottom Cu	0.20	400
Heatsink attach solder	0.05	50

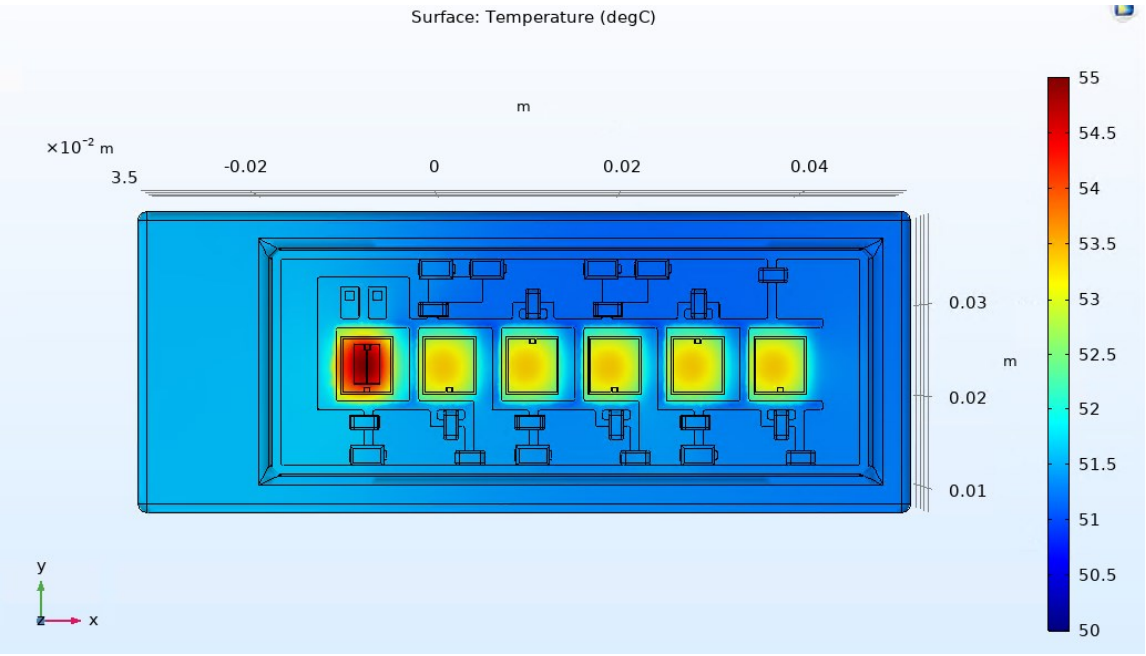


Fig. 3.17: COMSOL simulated surface temperature plot when 8W power applied to JFET and 10W applied to cascode

For the 3-layer (360µm) ERCD substrate the junction to case thermal resistance for the JFET (UnitedSiC – UF3N120008) is

$$R_{th_{jc}} = \frac{53.4 - 50}{8} = \frac{0.43^0 C}{W} \tag{3.11}$$

For the 3-layer (360µm) ERCD substrate the junction to case thermal resistance for the stacked cascode (UnitedSiC – UF3S120009) is

$$R_{th_{jc}} = \frac{54.9 - 50}{10} = \frac{0.49^0 C}{W} \tag{3.12}$$

The thermal resistance can be standardized to be 0.012 ^{0}C/W. mm^2 for the JFET (UnitedSiC – UF3N120008) and 0.014 ^{0}C/W. mm^2 for the stacked cascode(UnitedSiC – UF3S120009).

Next, all surfaces are defined as thermally insulating except a 1W of power applied to the power die and a heat transfer coefficient, '*h*' is applied to the heat sink fins as shown in Fig. 3.16.

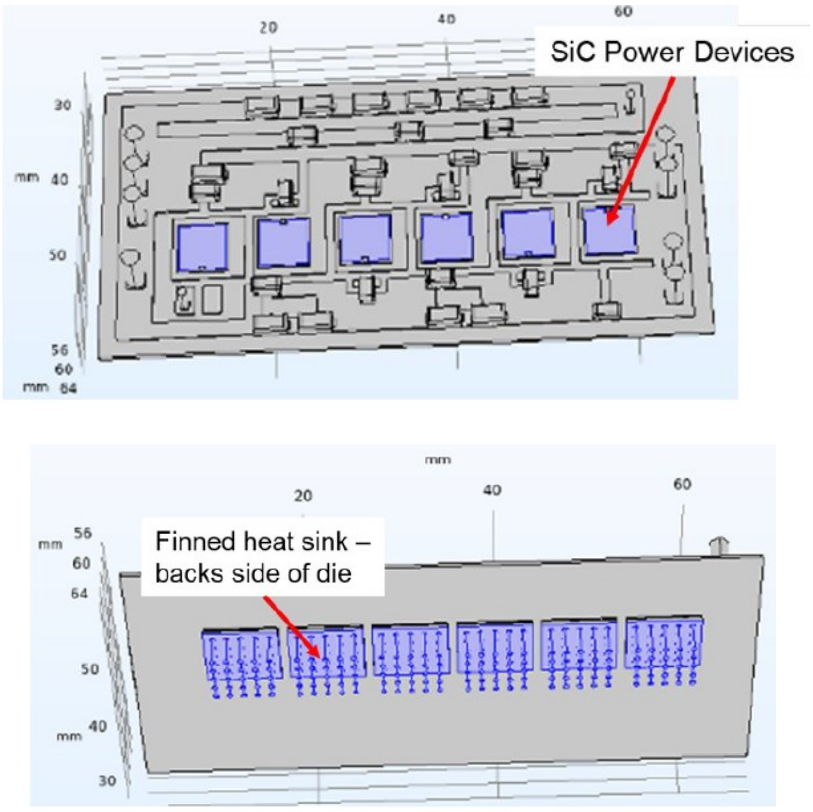


Fig. 3.18: COMSOL model with heat source applied to the SiC power devices and extracted from the heatsink fins

For this design the Cu custom heatsinks, "4-02027U" are chosen was from Cool Innovations shown in Fig. 3.19 which have tested case to ambient thermal resistance vs flow rate, shown in Table 3.7.

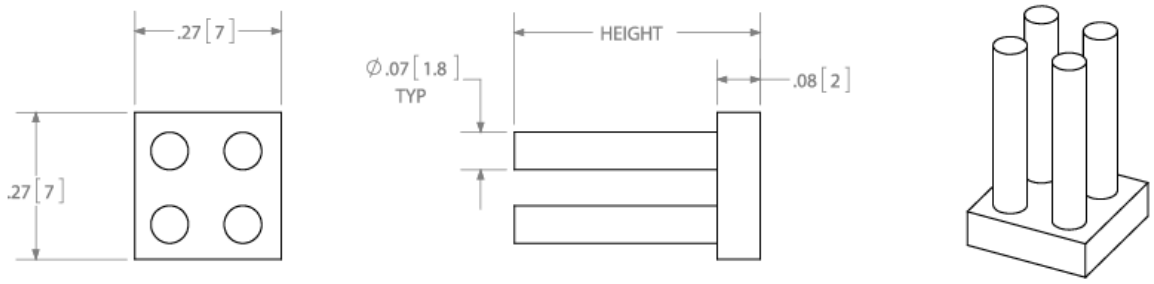


Fig. 3.19: Heatsink, 4-02027U mechanical drawing, where height = 17.2 mm

Table 3.7: Heatsink thermal resistance vs LFM						
P/N	Height in(mm)	Weight lb(g)	200	400	600	800
4-020207U	0.7(17.8)	0.0049(2.2)	31.5	21.7	16.6	13.4

A coolant chamber, shown in Fig. 3.20 is designed to provide dielectric flow across the heatsink fins. The coolant chamber has 3 inlet and 3 outlet valves designed for standard tubing with 6 mm inner diameter and 9 mm outer diameter. Flourinert-70 from 3M is the chosen dielectric liquid for its high dielectric strength and high boiling point for single-phase cooling. The housing body is mounted on the coolant chamber with M4 screws and a rubber sealant gasket, shown in Fig. 3.21.

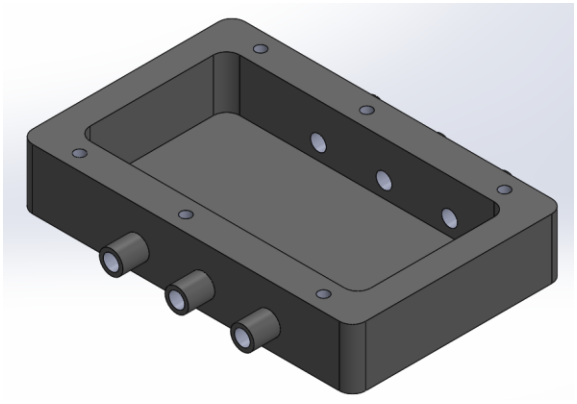


Fig. 3.20(a): Isometric view of coolant chamber

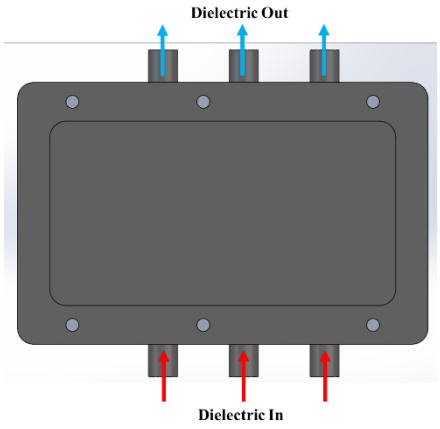


Fig. 3.20(b): Top view of coolant chamber

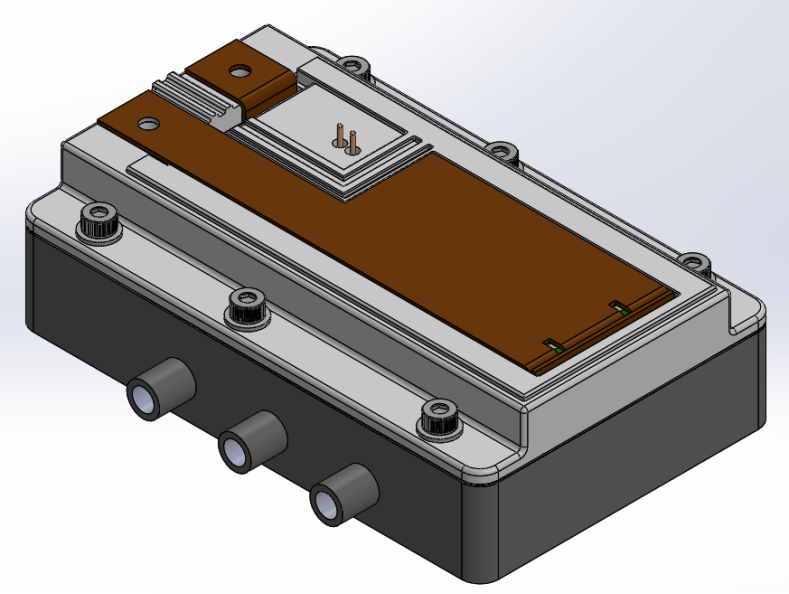


Fig. 3.21: Isometric view of the 2S-3C Cascaded SuperCascode Power Module with coolant chamber

To compare different thermal system designs and estimate their junction-to-ambient temperature a parametric study was performed in COMSOL for different *'h'* coefficients, 1W of power was applied to each power die and an *'h'* coefficient applied at all the heat sink fins approximately equivalent to the area in the final application.

The sweep is from 25 W/m^2K (air cooling) to 600 W/m^2K to an arbitrarily high liquid cooling value. Each power die dissipates 40W of power, calculated using the LTSpice model when the 2S-3C CSCPS operates at 6kV/50A and switches at 100kHz. Results in Fig. 3.22 shows that for the 40W (switching + on state losses) generated per die that a minimum heat transfer coefficient of 245 W/m^2K (red line on the graph) is required to ensure the device operates below 175ºC for 50ºC ambient. The graph also shows that air cooling is viable at a certain derated condition of 16.7 A continuous current. Thus, for a good cooling system the switch should be able to operate at 105A continuous current for a 4m/s dielectric flow with inlet dielectric fluid temperature set to 50ºC, through the cooling fins, which is the closer to the theoretical limit of the JFET power die.

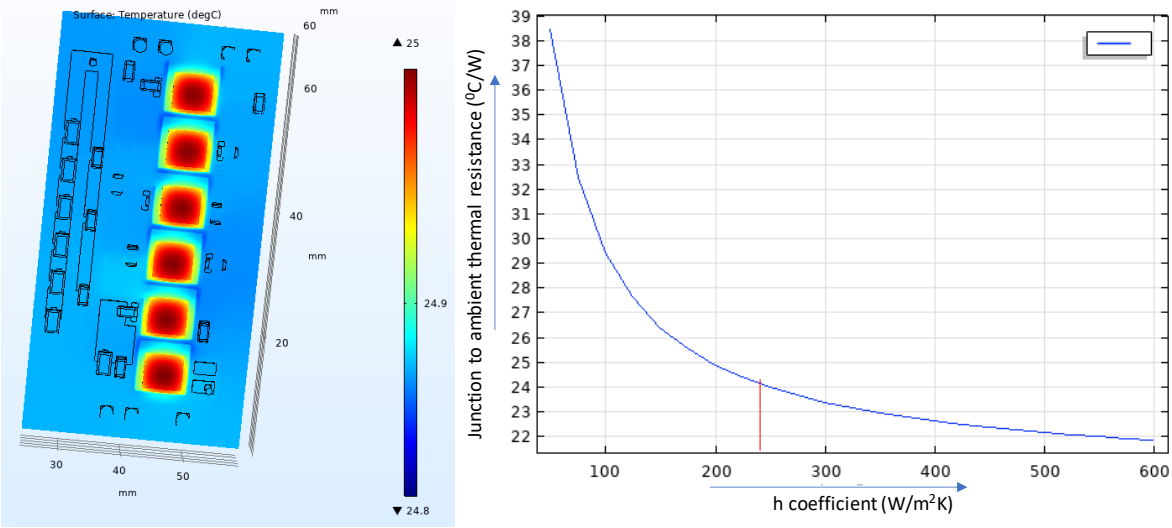


Fig 3.22(a) COMSOL Simulation done to measure the thermal resistance of the stack up (b) Parametric study result plotting junction to ambient thermal resistance vs heat transfer coefficient

3.8 Conceptualization of a 24kV 24-JFET 2S-3C-2C-2C Cascaded SuperCascode Box Design

The physical implementation of the 24kV HV-CSCPS uses four 6.5kV 2S-3C power modules discussed above connected in series in a 3-layer cascaded network to form a 2S-3C-2C-2C CSCPS. The progression is shown in Fig. 3.23. The 6kV (2S-3C) string of SiC JFETs and Si MOSFET is shown to the left, while a 2S-3C JFET without the MOSFET is shown in the middle. The full HV-CSCPS is shown to the right with the blocks combined as shown. Here, BN1 forms the second layer cascade and BN2 forms the third layer cascade and consists of an auxiliary balancing network that triggers and voltage balances, CSCPS-2,4 and CSCPS-3 respectively with the help of three resistors (RL1-RL3) that manage leakage current.

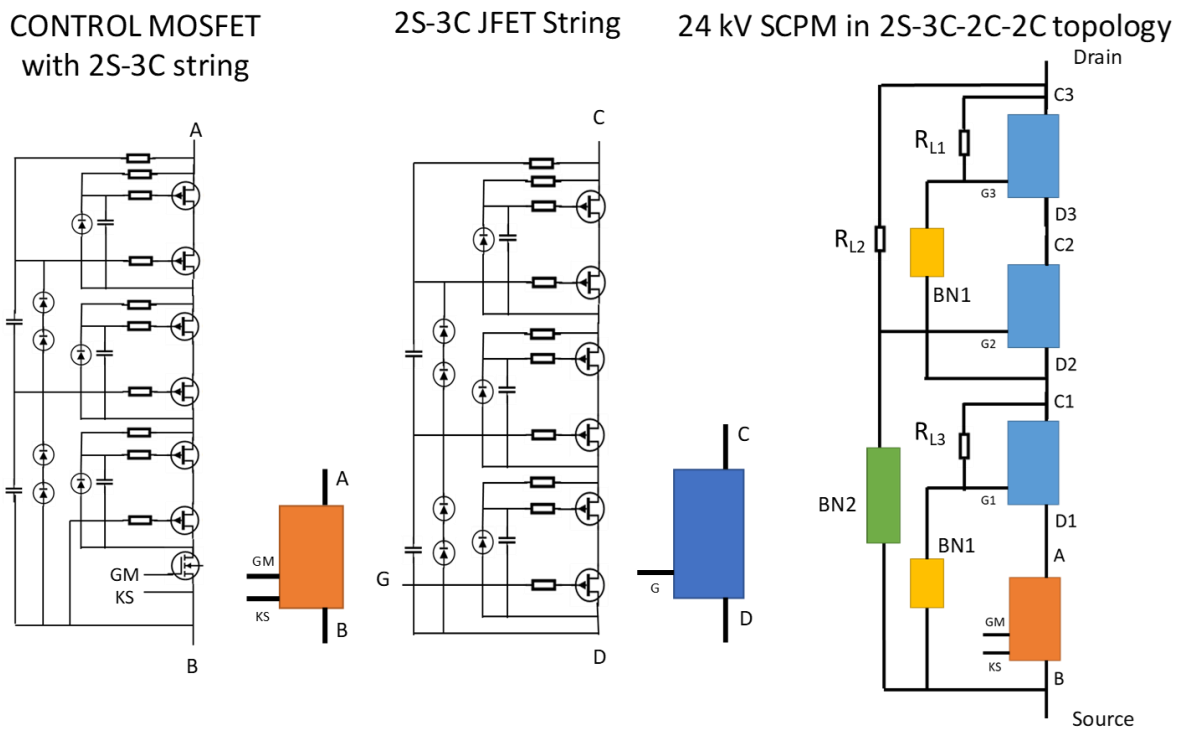


Fig. 3.23: Block Diagram of the 2S-3C-2C-2C 24 kV CSCPS with twenty-four 1.2 kV JFETs

To realize the circuit emphasis has been made on optimizing the electro-physical layout and thermal design. A mutual inductance cancellation is achieved by placing the returning current path close to the source current path. An electrical simplified schematic of *24kV* CSCPS is shown in Fig. 3.24. Here arrows show the direction of current flow.

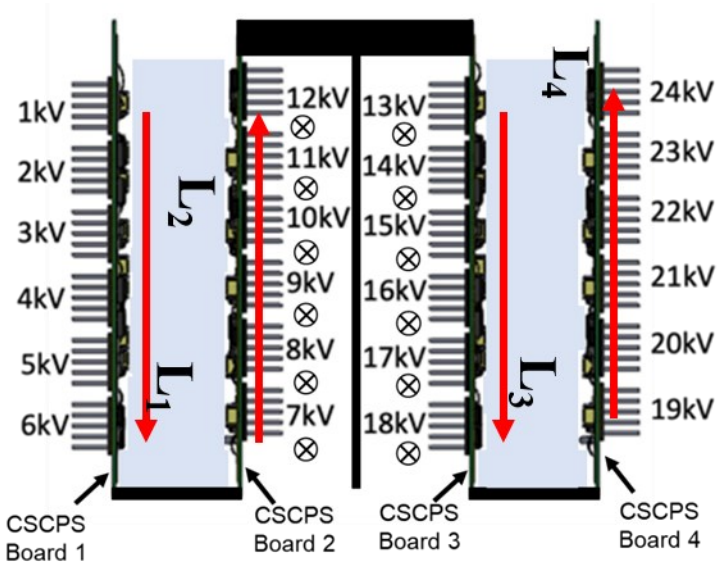


Fig. 3.24: 24kV serpentine approach to introduce mutual inductance for inductive cancellation

Here L_1, L_2, L_3 and L_4 are self-inductance in power path of each *6kV* CSCPS. The suppression is achieved by placing the two consecutive current paths triplets (0 to 6kV and 6kV to 12kV; 6kV to 12kV and 6kV to 12kV; 12kV to 18kV and 18kV to 24kV) close to each other. The inductor matrix is updated with the with M_{12}, M_{21}, M_{23} , M_{32}, M_{34}, M_{43} and shown in (3.13) .

$$L = \begin{bmatrix} L_1 & -M_{12} & & \\ -M_{21} & L_2 & -M_{23} & \\ & -M_{32} & L_3 & -M_{34} \\ & & -M_{43} & L_4 \end{bmatrix} \tag{3.13}$$

The net induced voltage due to the inductor matrix can be calculated using the equation below.

$$\begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} = \begin{bmatrix} L_1 & -M_{12} & & \\ -M_{21} & L_2 & -M_{23} & \\ & -M_{32} & L_3 & -M_{34} \\ & & -M_{43} & L_4 \end{bmatrix} \begin{bmatrix} \frac{di}{dt} \end{bmatrix} \tag{3.14}$$

This can be simplified as :

$$\Delta V = (L_1 + L_2 + L_3 + L_4)\frac{di}{dt} - 2(M_{12} + M_{23} + M_{34})\frac{di}{dt} \tag{3.15}$$

3.8.1 Box design conceptualization of a 24kV Design

Each 24 kV switch uses four individual 6kV/105A Cascaded SuperCascode Power Module (CSCPM) Epoxy-Resin Composite Dielectric (ERCD) boards as described in Section 3.3 and shown in Fig. 3.4(b) and Fig. 3.25(a). These individual boards are assembled as shown in Fig. 3.23(b) and are interconnected using flex circuitry.

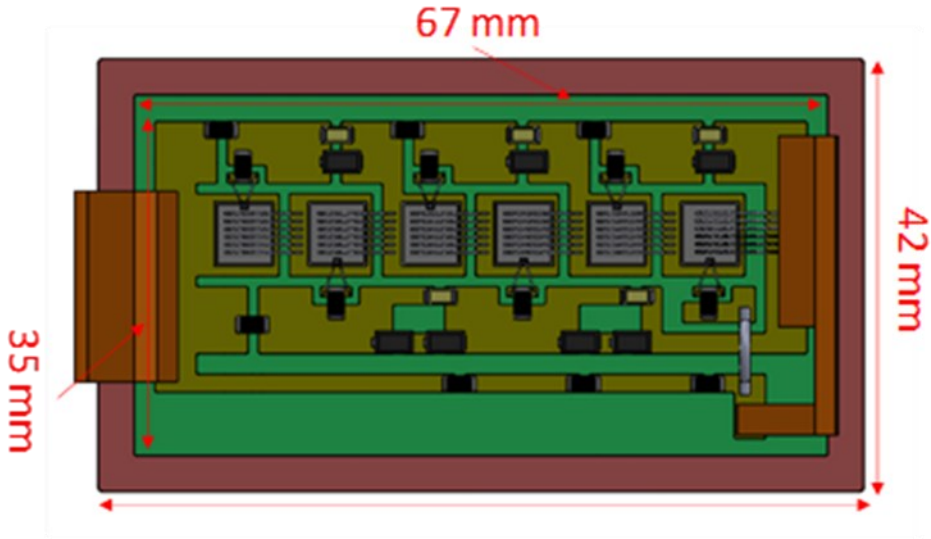


Fig.3.25(a): ERCD board with populated devices in a PEEK carrier board

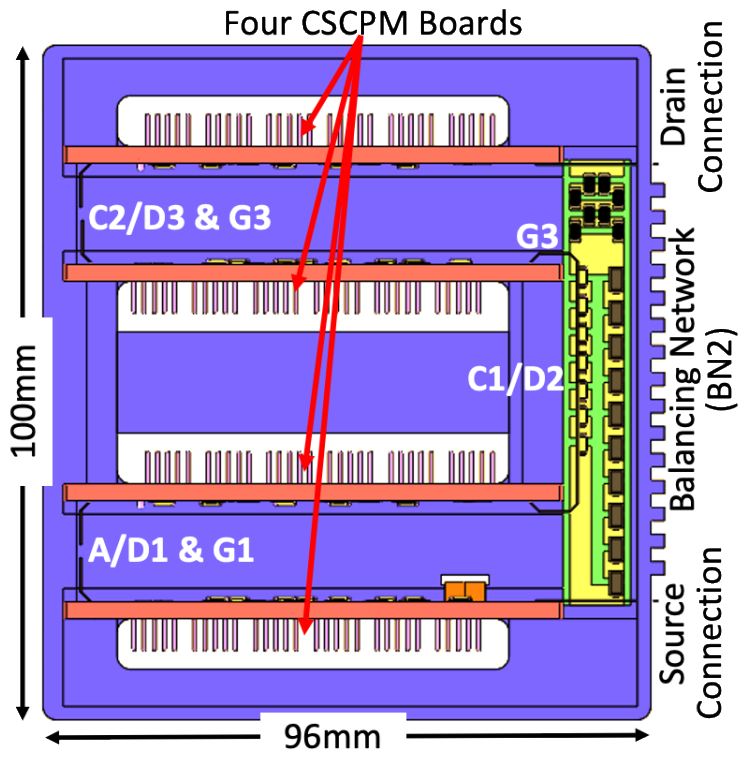
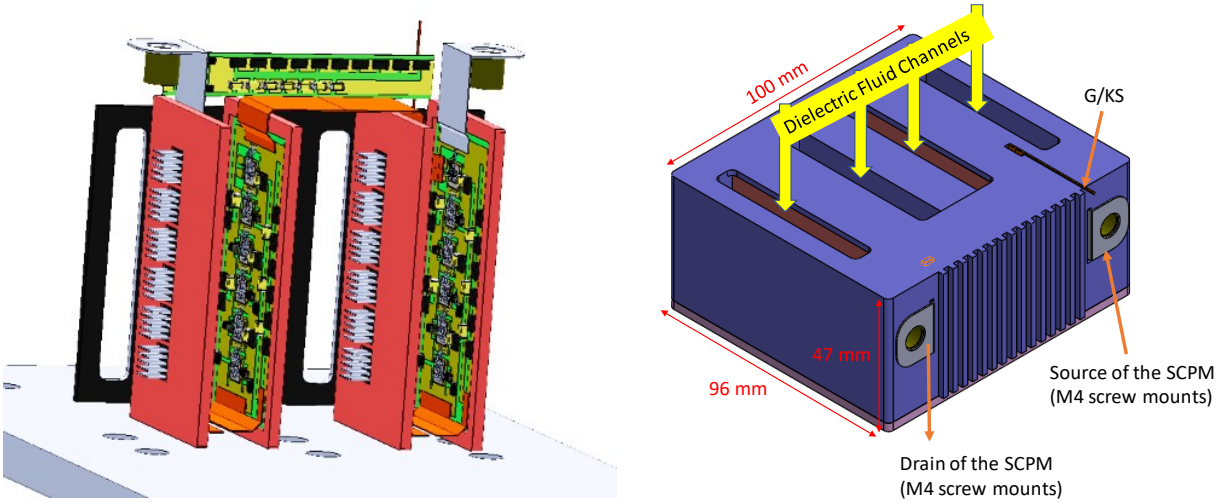


Fig.3.25(b): Box/Rack structure hosting four 6kV ERCD boards interconnected for 24 kV

The CSCPS boards shown in Fig. 3.25(a) and Fig. 3.25(b) are inset and sealed into the housing with Henkel cement. Dielectric fluids flow through channels passing over the heat sinks. A further concepualization with inlet and outlet pipes and mixing chambers is shown in Fig. 3.25(c). The 3M dielectric fluid flows into the mixing chamber which further divides dielectrically into 4 channels to pass dielectric cooling fluid over each CSCPS board. The fluid exits into the outlet mixing chamber and is then recirculated coooled.

The 24kV HV-CSCPM uses a standalone balancing network BN2 at the top as shown in Fig. 3.26(b). The 24kV module has two power terminals and two gate driving terminals including a kelvin source connection. The overall dimensions are 100 mm X 96 mm X 47 mm for the power module section (blue) in Fig. 3.26(c). Dielectric fluid is circulated through heat sinks to provide

electrical insulation, suppress corona and arcing and also serve as a coolant. For this application Flourinert-FC 70 from 3M is selected.



(a) (b)

Fig. 3.26(a): Solidworks rendering of the 24kV/105 A HV-CSCPS power switch box/rack section (b) Four 6.5 kV/105 A CSCPS without PEEK housing body

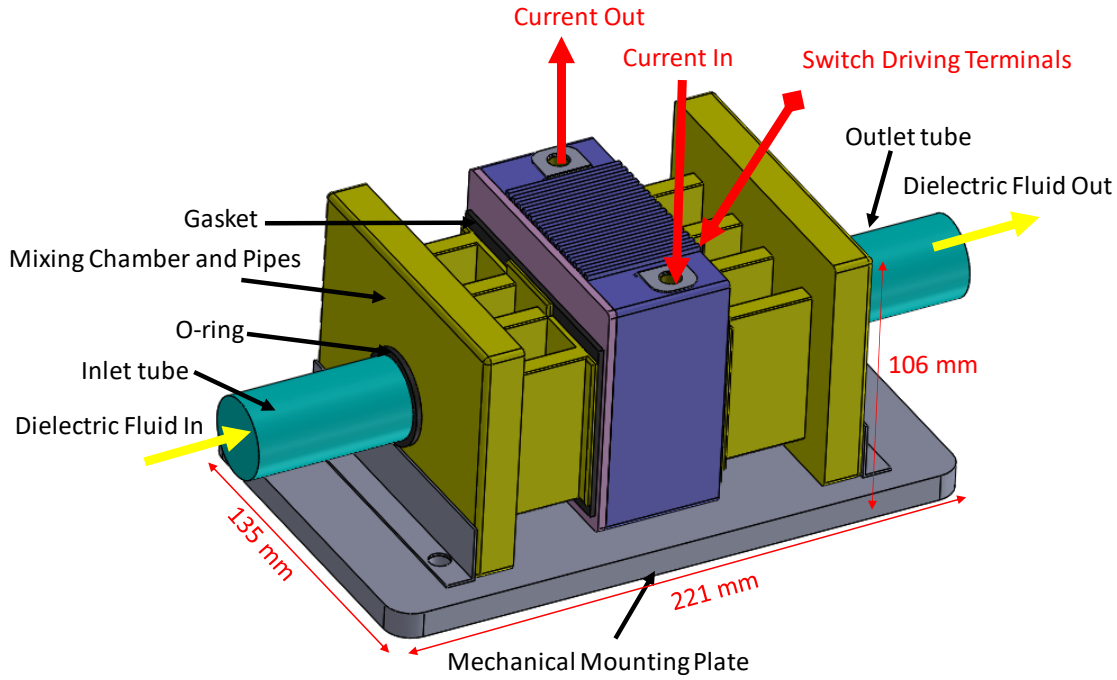


Fig. 3.26(c): Mounting and cooling chamber assembly with the 2S-3C-2C-2C 24kV Cascaded SuperCascode Power switch

The overall power module measures 100 x 96 x 47 mm (blue box in Fig. 3.26(b)) and the module with an integrated coolant chamber and a mechanical mounting plate measures 135 x 221 x 106 mm, shown in Fig. 3.26(c).

3.8.2 Electric field challenges

For application to high voltage packaging key emphasis has been put onto E-field management internal to power module at different levels of power packaging. The E-field contouring in solids in under-die layered structures for level-1.5 packaging (die on substrate and board packaging) is tackled by (1) using round copper edges, (2) using ERCD with a high dielectric strength versus ceramic substrates and (3) using electrically-conducting heatsinks which use dielectric coolant for cooling. The DC E-field minimization in topology layout in level-2 packaging of high voltage (6kV) cascaded-cascode submodules is achieved by (1) overlapping the busbars in the 2D space to introduce mutual inductive cancellation, (2) creating creepage and clearance slots in the power module and (3) using direct poured epoxy resin encapsulation with high thermal conductivity. Another challenge is Electro-Hydro Dynamic (EHD) field. Electro hydrodynamics (EHD) deals with the interaction between electric fields and fluid flow. Although numerous EHD applications have been explored and extensively studied, the fast-growing technologies in the power semiconductor industry, introduce new challenges and demands. These challenges require enhancement of heat transfer and mass transport in small scales (sometimes in molecular scales) to remove highly concentrated heat fluxes from reduced size devices. This interaction can result in electrically induced pumping, flow distribution control, or mixing of fluids.

Management at level-3 packaging submodules for 24kV/100A switch module and placing the modules in chassis arranged to keep high voltage points farthest apart. The EHD effect

minimization is essential to maintain a uniform coolant flow and limit electrically induced pumping in the heatsink fins. The mixing chambers in Fig. 3.26(c) are metal to neutralize EHD fields. The flow process is described numerically by coupling the Navier-Stokes equations to the Maxwell equations (Atten and Seyed-Yagoobi, 1999). [124] This is seen through the electric body force equation which describes the interaction of the electrical fields and flow fields:

$$\vec{f} = p_c\vec{E} - \frac{1}{2}\vec{E}^2\nabla\varepsilon + \frac{1}{2}\nabla\left[\vec{E}^2 p\left(\frac{\partial\varepsilon}{\partial p}\right)_T\right]$$

In the above equation, $\vec{f}$ is the total body force on the working fluid due to an applied electric field. The p_c represents the charge density, E represents the electric field strength, and ε is the permittivity of the working fluid. The ρ is the mass density of the working fluid and $\partial E/\partial\rho$ is determined at a constant temperature. The first term represents the Coulomb force that acts on free charges in an electric field and is the dominant force in EHD pumping. The second and third terms are the dielectrophoretic and electrostriction forces respectively, which represents the polarization force acting on polarized charges. The dielectrophoretic force is dependent on a gradient in permittivity which does not exist in an isothermal liquid. The electrostriction term requires permittivity to be a function of the density of the fluid at a constant temperature. For the case of incompressible fluids, this term is negligible. Therefore, the force on the free charges in the fluid is majorly dependent on the electric field vector.

The fundamental “SuperCascode” power switch, uses serial power semiconductor devices that self-trigger along a serial string during switching. This distributes the voltage and thermal load.

3.8.3 Simulation and Performance Estimation of the 24kV box design

The 24kV power module is imported in Ansys Q3D to study the effect of mutual inductive cancellation and COMSOL to study the E-field distribution in the center channel.

From ANSYS Q3D, the overall parasitic inductance was estimated to be 135 nH at 250kHz. A serpentine layout of the Cascaded SuperCascode Power Module (CSCPM) Boards was taken in the design to achieve two critical design challenges for a HV switch – parasitic inductance and high electric fields, which can lead to breakdown and EHD effects in dielectric fluids. The serpentine layout introduced *"Mutual Inductance Cancellation"* and provided a 25% reduction in power path insertion inductance. The worst case E-field in the serpentine layout is between two central boards, i.e CSCPS board 2 and CSCPS board 3 as shown in Fig. 3.27. The ΔV between the boards varies from 1-11kV and dielectric fluid flows perpendicular to the electrical current flow direction which is into the page.

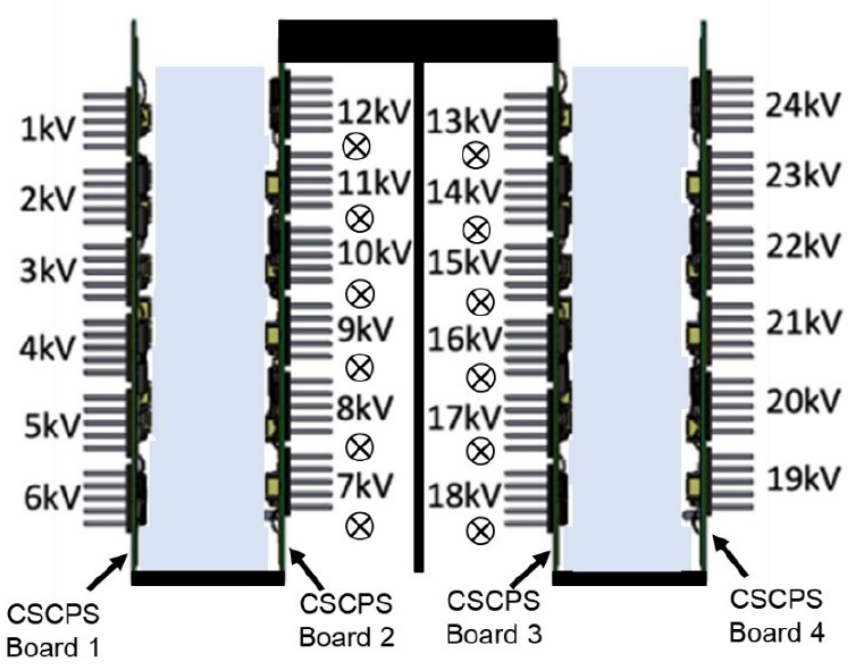


Fig. 3.27: 24kV power module, serpentine layout

To setup the simulator, the 3D model for the 24kV power module is imported into COMSOL multiphysics. The power devices are then excited to the potential they are expected to see during normal operation. The E-field contour is shown in Fig. 3.28.

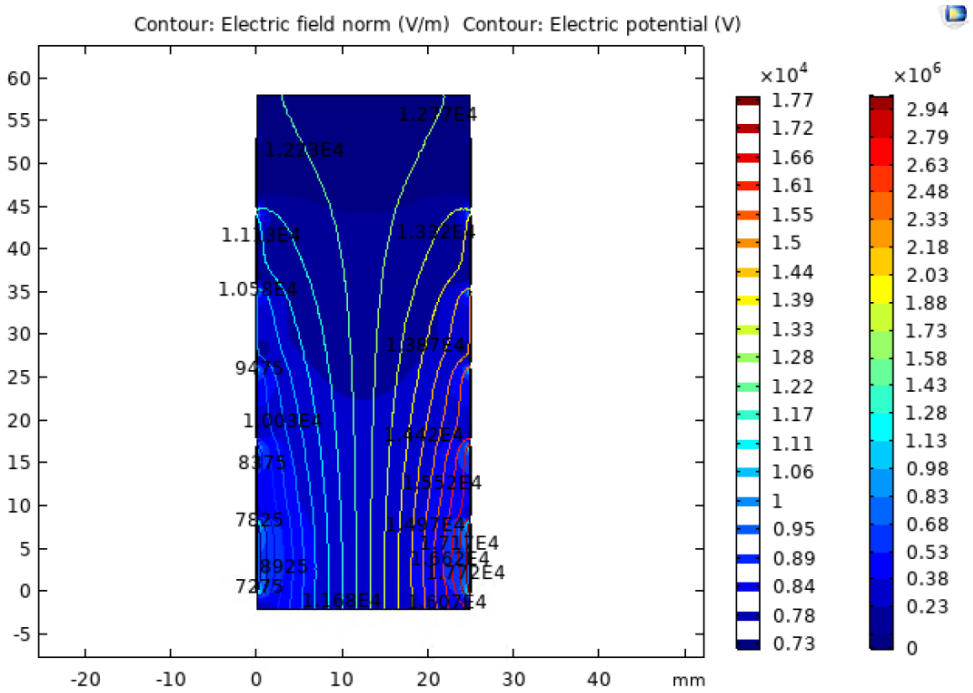


Fig. 3.28: E-field contour when board 2 and board 3 are 25 mm apart

The serpentine approach *limits the worst-case Electric Field to 3.6 x 10^6 V/mm* by moving the high potential points farthest away in the structure and evenly distributing voltage potentials across the entire volume of the power switch. The approach reduces the EHD impact on the liquid dielectric to within limits of 3M-Flourinert70 capabilities. The design of the 24kV 2S-3C-2S-2S power module is summarized in Table 3.7.

Table 3.7: 2S-3C-2C-2C CSCPS Switch Specification	
METRIC	RATING
Voltage Rating	28.8 kV (rated) 24 kV (set by the balancing network capacitors)
Current Rating	105 A with 4m/s dielectric fluid OR 16.7 A with forced convection of air cooling
Dimensions (mm)	100 * 96 * 47 (switch only); and 220 * 135 * 96 (Assembled switch with cooling channel and mechanical support structure)
Weight Density	1.43 MW/kg (switch only); and 1.16 MW/kg (with dielectric fluid – not including inlet and outlet chamber and Al Baseplate)
Efficiency	99.5 % (conduction + switching + loss due to parasitic resistance)
Power Density	2.66 kW/cm^3 or 2.66 MW/L

CHAPTER 4: Experimental Validation

This chapter discusses the empirical validation of the Cascaded SuperCascode power switch topologies discussed in the previous chapters. A *6.5kV/20 A* 2S-3C CSCPS prototype is fabricated using six serial TO-247 JFETs and put under static and dynamic characterization to validate simulated performance. Next, the fabricated power module is put under blocking voltage testing to qualify the segmented baseplate power module for HV application and thermal testing to evaluate the heatsink performance with forced air convection.

4.1. Cascaded SuperCascode topology testing

A *6kV/20A 2S-3C* CSCPS was built using six discrete TO-247 UnitedSiC UJN1208K JFETs with a balancing network as shown in Fig 4.1. The balancing network is distributed on both sides of the power devices for a symmetric layout. The component values of the balancing network are shown in Table 4.1.

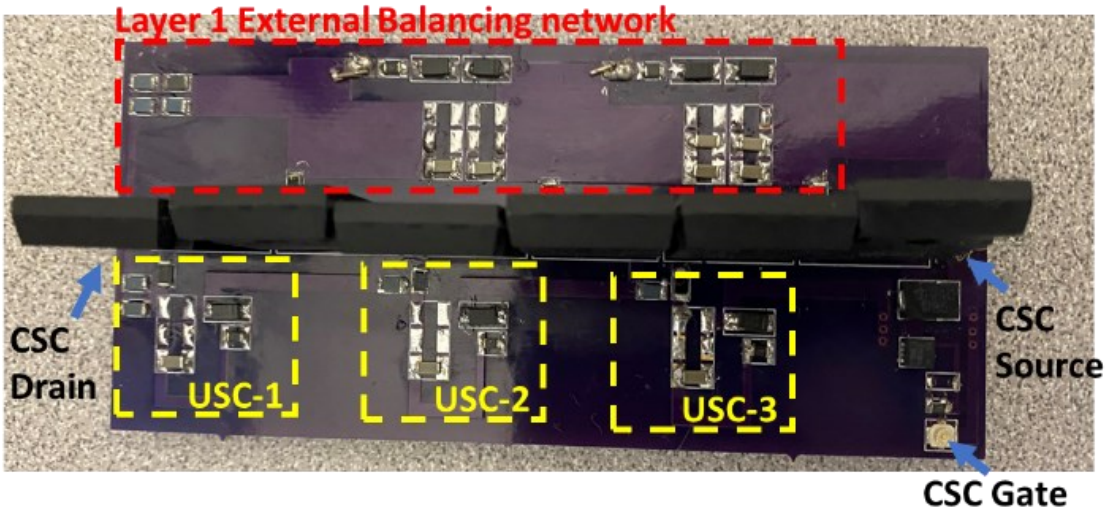


Fig. 4.1: 6.5kV 2S-3C CSCPS power switch developed using discrete SiC JFETs on PCB

Table 4.1: Component values for 6.5 kV CSC power switch	
C_1-C_3	68 pF, 1kV rated
C_4	34 pF, 2kV rated
C_5	68 pF, 2kV rated
R_{L1}-R_{L4}	Vishay 4MΩ high voltage
R_1-R_6	Vishay 10Ω high power
D_1-D_7	Vishay AU1PK

The device was first subjected to static electrical testing in the first and third quadrants of the I_D vs V_{DS} performance chart then subjected to dynamic tests in a Double Pulse Test (DPT) configuration. The forward I-V characteristics in Fig. 5.2 show the CSCPS has an $R_{ds(on)}$ of 408mΩ. This value conforms to the datasheet value of UJN1208Z (typical 67 mΩ per device or 402 mΩ for six) and the MOSFET (0.9 mΩ). The reverse I-V characteristics are shown in Fig. 4.2(b), showing a static reverse leakage current of 0.7 mA @ 4.8 kV which conforms to the datasheet maximum drain leakage current.

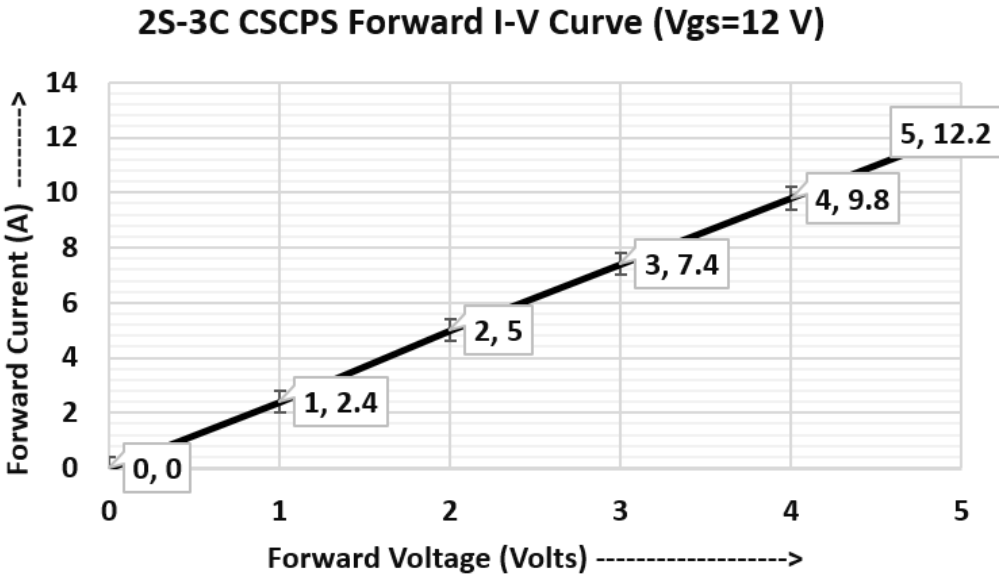


Fig. 4.2(a): Forward IV characteristics of the 6kV Cascaded SuperCascode Power Switch

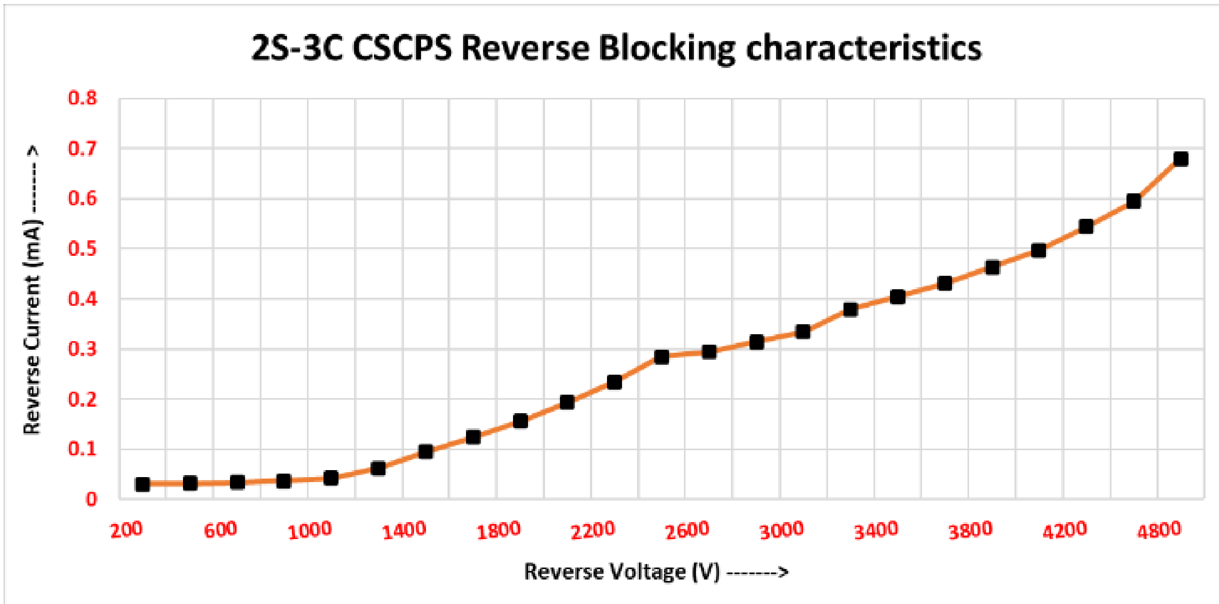


Fig. 4.2(b): Off-state blocking characteristics of the 6kV Cascaded SuperCascode Power Switch

The leakage current conforms to the expected leakage current dictated by the balancing network bias resistor plus the leakage current through JFETs which is individually tested to have a leakage current of 60µA/JFET according to the device datasheet. The device shows a sectioned exponential curve, unique to CSCPS caused by the successive breakdown of stages as blocking voltage increases.

The 2S-3C 6-JFET CSCPS 1st quadrant I/V characteristics at the room temperature are shown in Fig. 4.3(a). The SiC CSCPS becomes fully-on with a 12 V gate voltage and the corresponding on-state resistance is 408 mΩ. The majority of the on-state resistance, typical 402 mΩ, is from the six SiC JFETs and the on-state resistance of the bottom Si MOSFET is close to 3 mΩ. Comparing the I/V curves the device on-resistance does not change when the voltage changes from 8 to 12V. When the SiC device conducts a reverse current, JFETs J_1-J_6 are in the on-state and the reverse conduction characteristics are determined by the JFETs channel resistance and the bottom Si MOSFET's reverse conduction characteristics. The 3rd quadrant I/V

curves of the SiC super-cascode device are shown in Figure 4.3(b). Firstly, little difference can be observed between device's 3rd quadrant I/V curves with -5 V gate voltage and those with zero gate voltage. It indicates that negative turn-off gate voltages on the SiC super-cascode device will not lead to higher reverse conduction loss. This is different from SiC MOSFETs whose reverse conduction loss will increase significantly when a negative turn-off gate voltage is applied [7, 8]. Secondly, the device in the off-state has a 0.7 V knee voltage at the room temperature and it is much smaller than SiC MOSFETs' body diode knee voltages which are generally around 2-3 V [7, 8]. These two features suggest that the SiC super-cascode device, compared to SiC MOSFETs, have less reverse conduction loss.

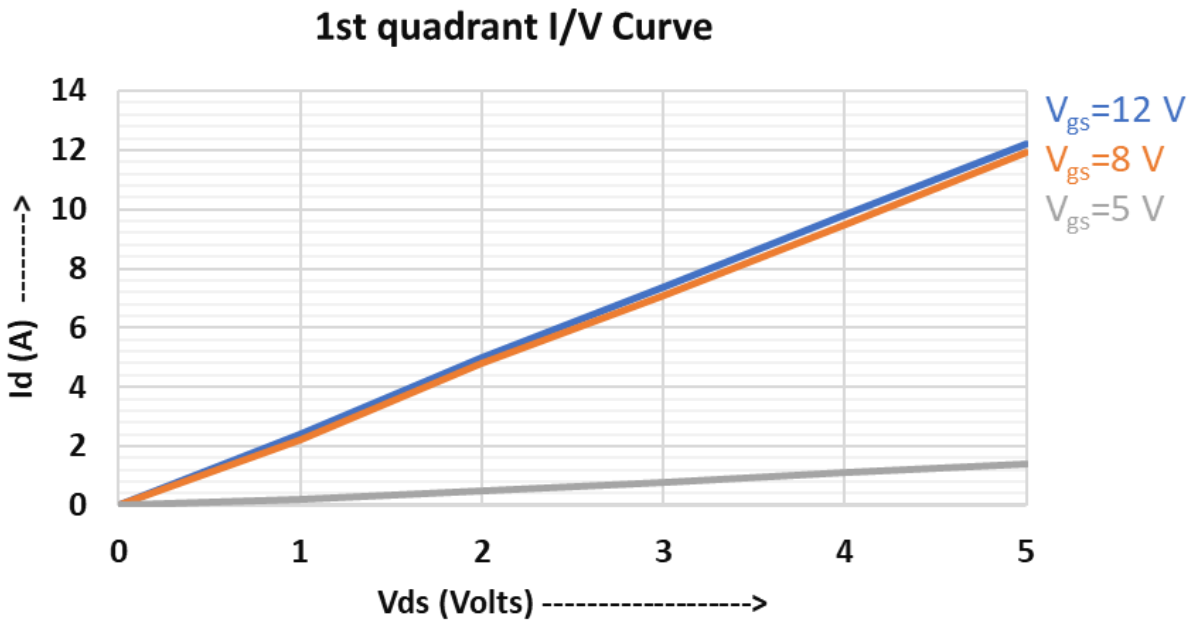


Fig. 4.3(a): 1st quadrant I/V Curve

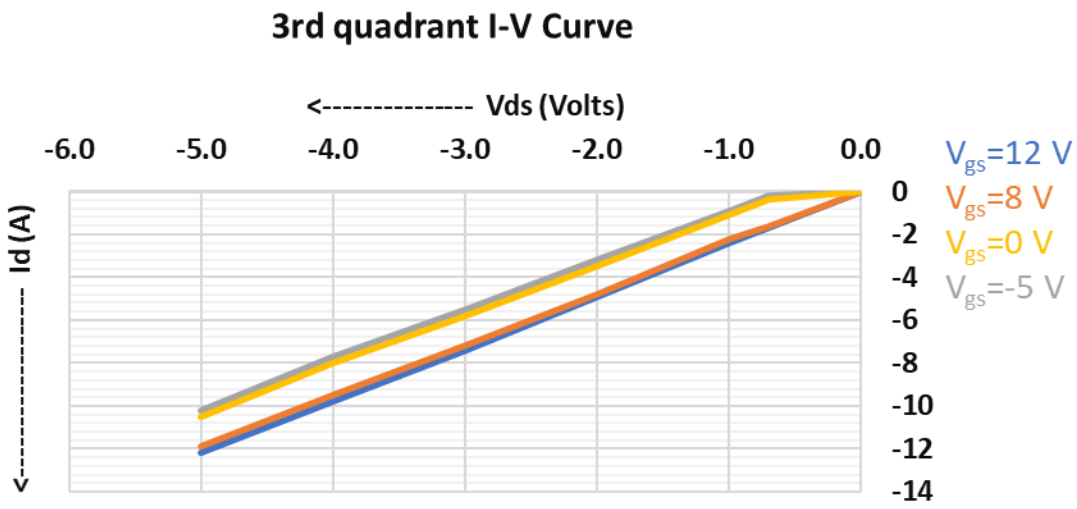


Fig. 4.3(b): 3rd quadrant I/V Curve

A Double pulse test (DPT) setup was built for dynamic switch characterization of the CSCPS (Fig. 4.4). The DPT setup consists of a 6kVdc supply, an *8μF* large decoupling capacitor, *6 mH* custom inductor and four 1.7kV/42A GeneSiC diodes (GB25MPS17-247) are connected in series. The diodes chosen are faster than the DUT to compute its fastest switching performance. The Cypress PSoC *5LP CY85C5888LTI* microcontroller board was used to generate trigger signals. In the test, a series of pre-pulses are sent before the main pulse to ensure that the DUT's dynamic balancing network goes into balancing mode, shown in Fig. 4.4 before applying the DPT dual pulse. The code for generating the trigger signals is given in Appendix G. The turn-on and turn-off at *4 kV/ 20 A* operation are shown in Fig. 4.5.

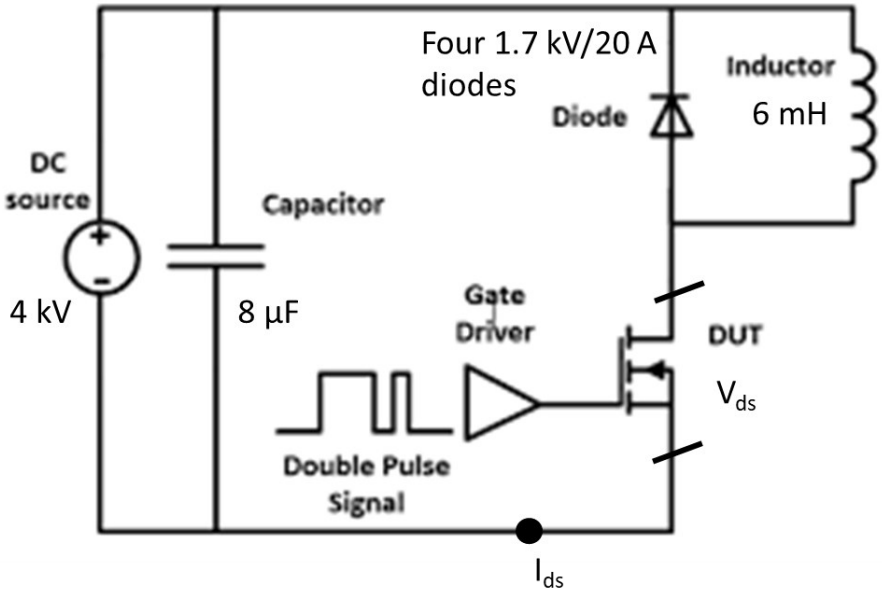


Fig. 4.4(a): DPT circuit diagram

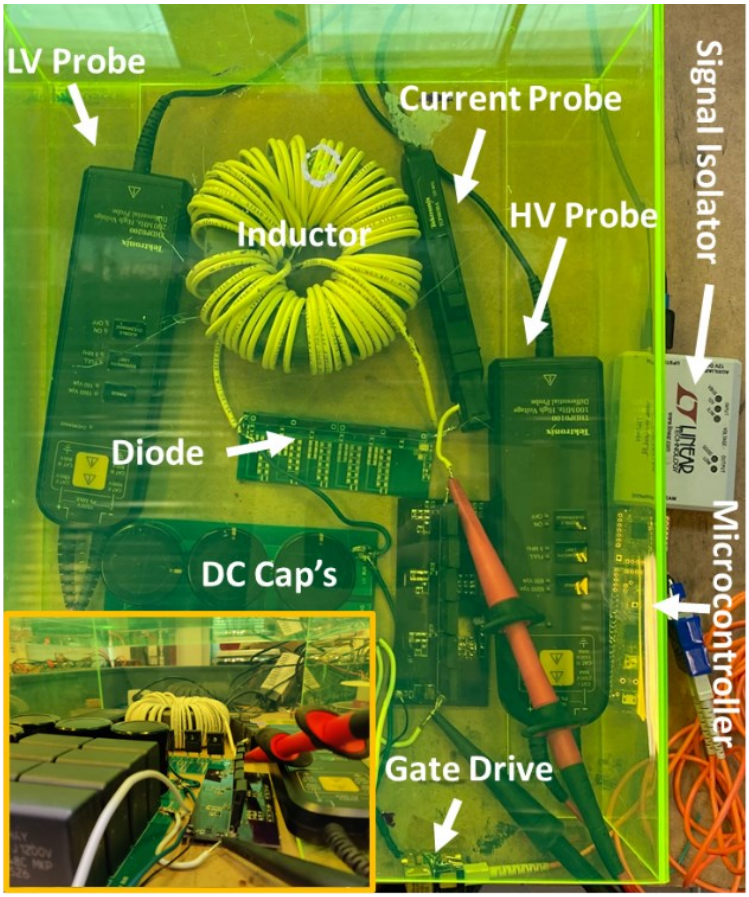


Fig. 4.4(b): Double pulse test setup

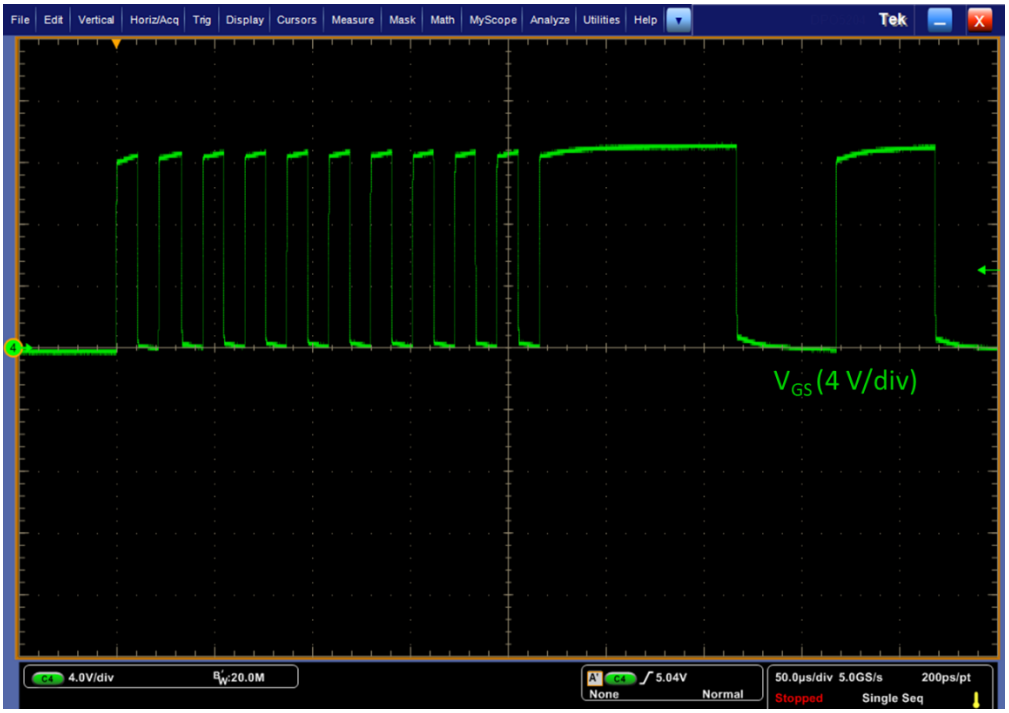


Fig. 4.5: Gate-source voltage waveform applied to the CSCPS

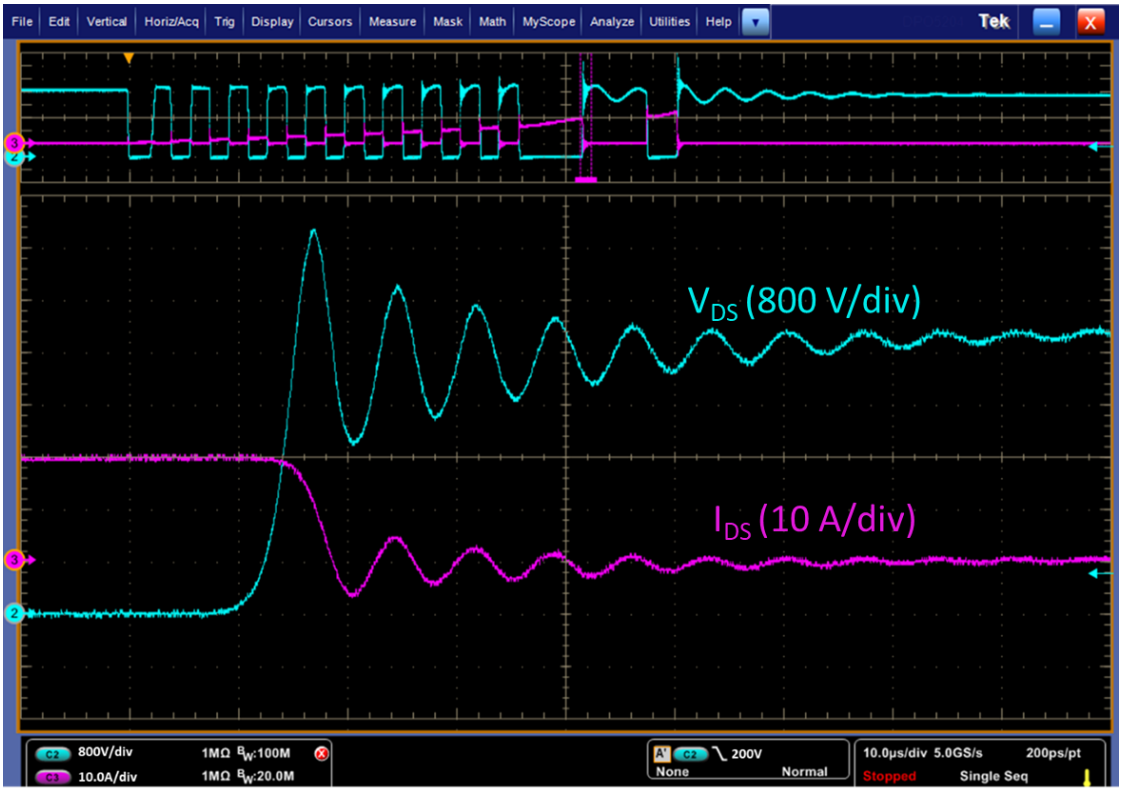


Fig. 4.6(a): DPT test with pre-pulse applied to ensure dynamic balance at 4kV/20 A (zoomed-in turn-off at 100ns/div)

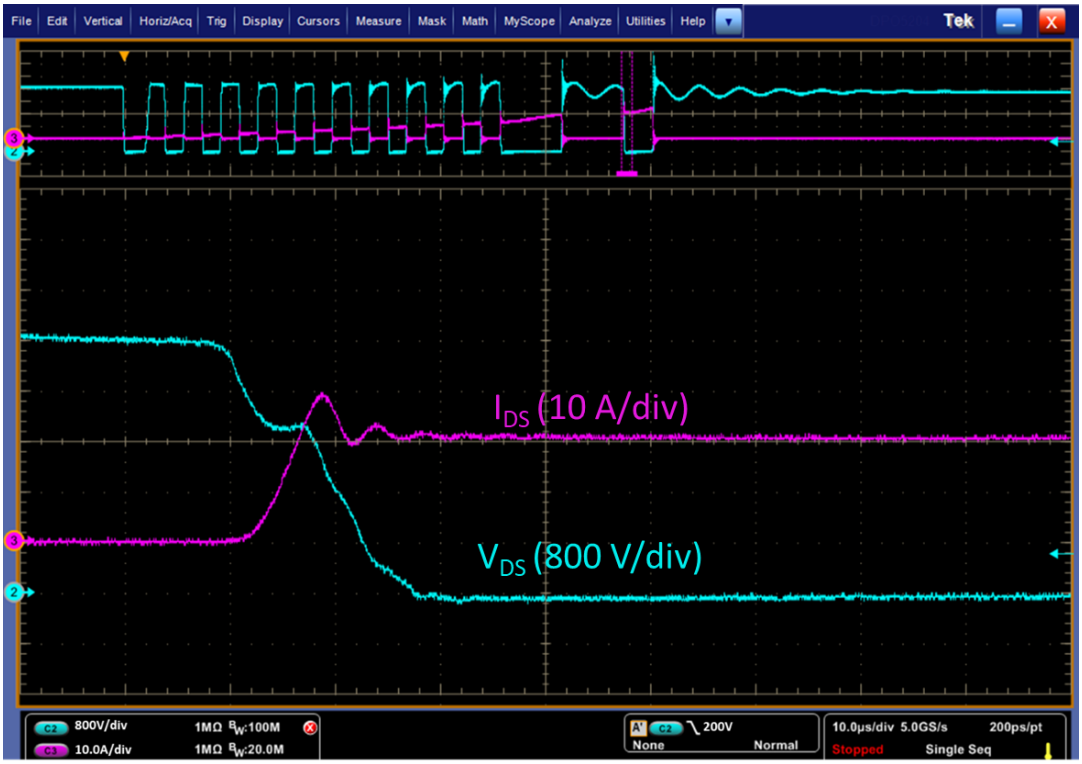


Fig. 4.6(b): DPT test with pre-pulse applied to ensure dynamic balance at 4kV/20 A (zoomed-in turn-on at 100ns/div)

The device shows a 90%-10% *40 ns* voltage rise time and 120 *ns* voltage fall time. The switch operated at *40 ns* current rise and *30 ns* current fall, corresponding to 500A/µs and 666A/µs. The device has 15.2 mJ turn-on loss, 3.7 mJ turn-off loss and 18.9 mJ net loss at 4kV/20 A operation. The device in comparison to Si 6.5kV (ABB 5SMX) IGBT device tested at the same voltage and current range shows, 5x lower switching loss.

4.2. *Power Module characterization*

Power module thermal testing and blocking voltage testing are done to demonstrate the module for 6.5kV application and for evaluating the heatsink performance.

4.2.1. *Thermal Test*

A thermal test for the packaged module is performed to evaluate its thermal performance, i.e. its junction-to-case thermal resistance and the performance of the heatsink. For this test, a

constant air flows across the heatsink and temperature is recorded with a thermocouple and an IR thermal camera. The test setup is shown in Fig. 4.6.

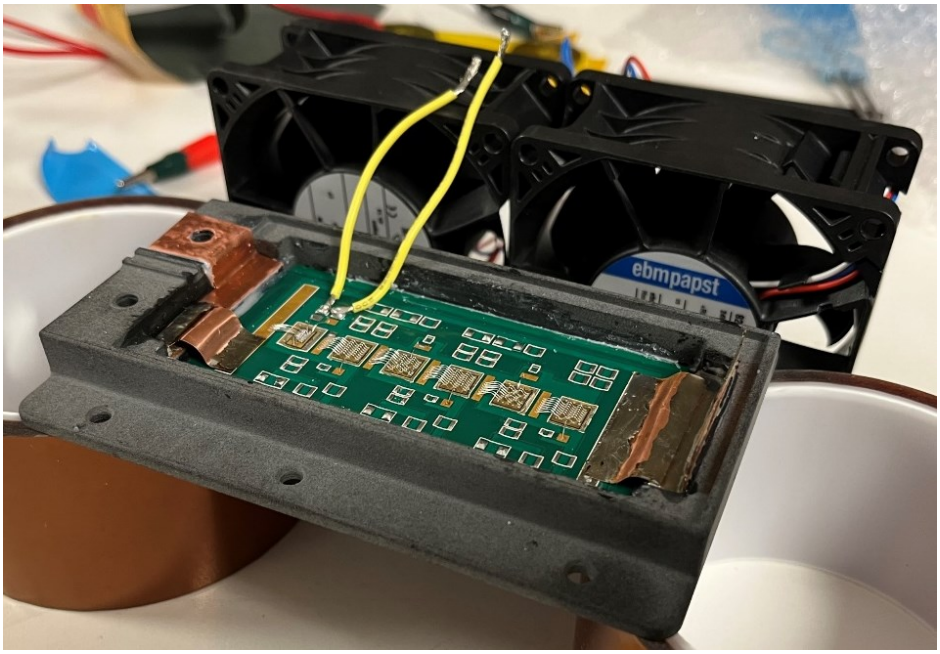


Fig. 4.7(a): Test setup (Isometric view)

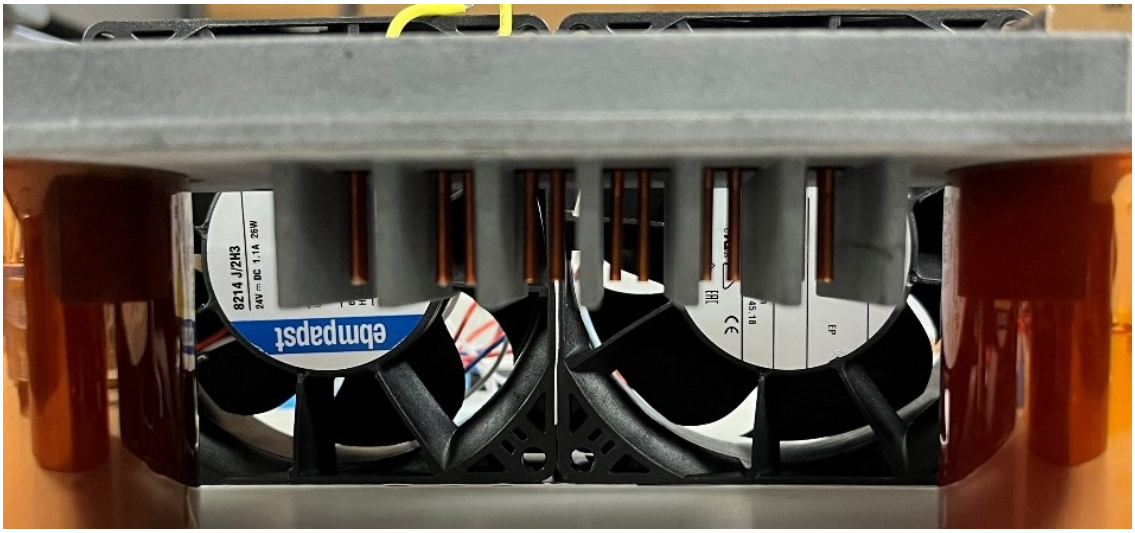


Fig. 4.7(b): Test setup (Side view)

A 12V gate-to-source voltage is applied to turn on the CSCPS power module and a 15 A current is conducted through the drain-source to observe the temperature distribution in and outside the power module. A thermocouple (Type K) and IR thermal camera (FLIR T62101) are

used to record the junction temperature and study thermal spreading through the module. Two DC fans (Ebmpast 8214 J/2H3) were connected as shown, operated at 24V, 1.1A to generate a constant airflow across the module heatsinks. An airflow sensor (UAS1200XS) is used to collect the real-time air velocity. The test module is connected to a Keysight E36313A DC power supply to provide a 15 A continuous DC current and a 12V gate-source voltage is applied using Keithley 2230-30-1 supply.

The initial ambient temperature was reported as 21^0C. Then the device is turned on by applying V_{GS} to the MOSFET gate and 15 A of continuous current is passed through the power device. At 15 A, each die dissipates 9.7 W. The measurements were taken after 5 minutes to ensure the temperature reaches equilibrium. The thermal image is shown in Fig. 4.7.

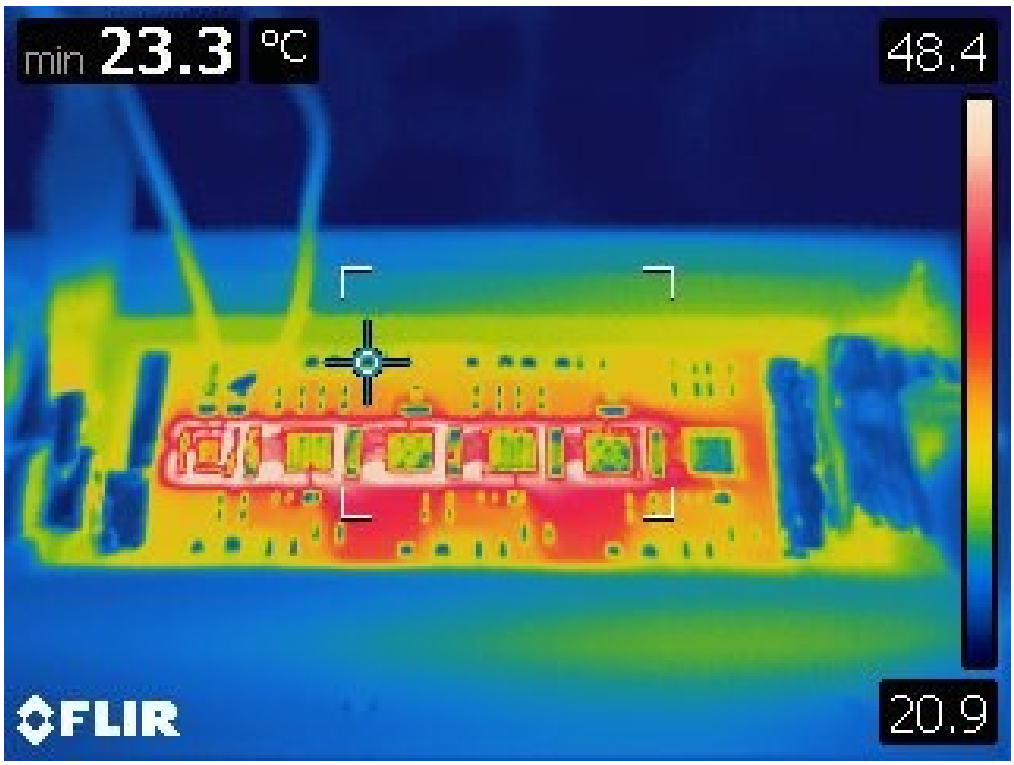


Fig. 4.8(a): Thermal IR image of the power module (Top View)

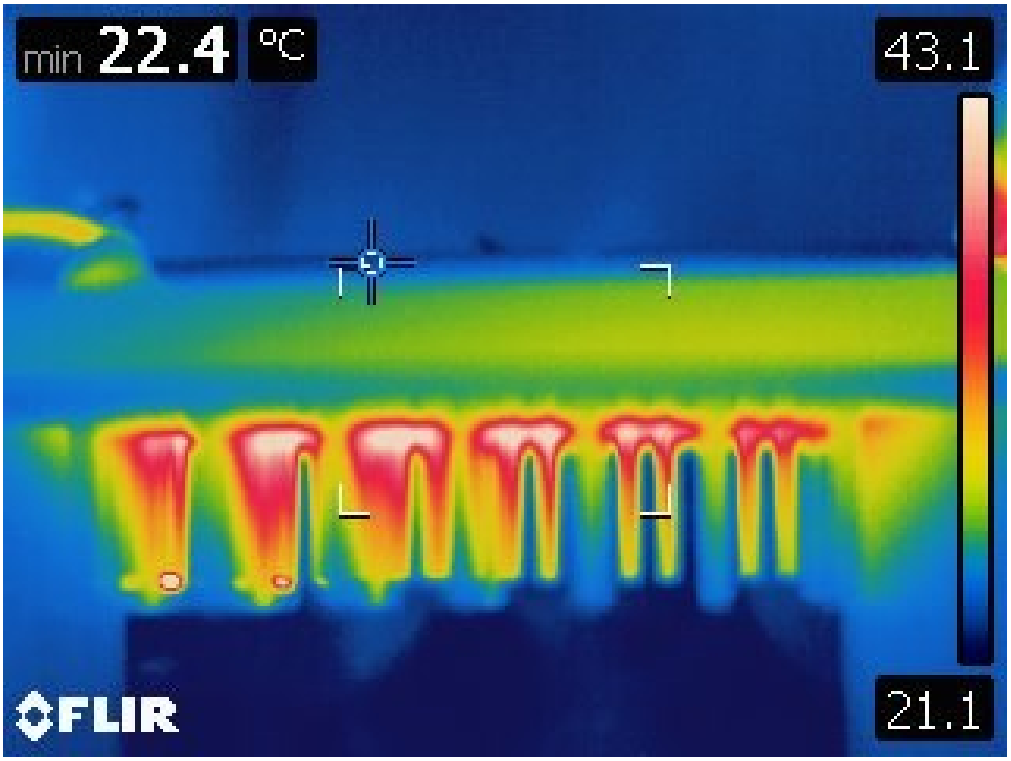


Fig. 4.8(b): Thermal IR image of the power module (Side View)

The thermocouple measures 47.5^{0}C, which represents the junction temperature verifying the accuracy of the image. The case temperature was measured to be 43.1^{0}C. The junction-to-case and junction-to-ambient thermal resistance can be calculated using (4.1) and (4.2) respectively. Here, $R_{\theta JA}$ and $R_{\theta CA}$ is the junction to case thermal resistance and case to ambient thermal resistance respectively. The T_J is the junction temperature, T_C is the case temperature, T_A is the ambient temperature and P_{loss} is the power loss.

$$R_{\theta JC} = \frac{T_J - T_A}{P_{loss}} = \frac{47.8 - 43.1}{9.7} = 0.48\ C/W \tag{4.1}$$

$$R_{\theta CA} = \frac{T_C - T_A}{P_{loss}} = \frac{43.1 - 22.4}{9.7} = 2.13\ C/W \tag{4.2}$$

The airflow sensor measures 6 m/s. The junction to ambient thermal resistance is calculated to be 2.61^{0}C/W, thus for a maximum junction temperature of 175^{0}C at 50^{0}C ambient,

the module can dissipate 47.8 W. Thus the power module can conduct 33 A (this assumes the device has equivalent conduction and switching loss).

4.2.2. *Leakage Current testing*

The test setup to measure the leakage current is shown in Fig. 4.8(a). Standing in for the power device, a small Alumina DBC (*12/40/12 mil*) island was used to validate the HV blocking capability of the aforementioned power module [125]. Multiple *5 mil* Al wire bonds were made between the topside of the DBC island to the Cu pads, and silicone gel (was vacuum cured over the entire power stage. The prototype power module tested is shown in Fig. 4.8(b).

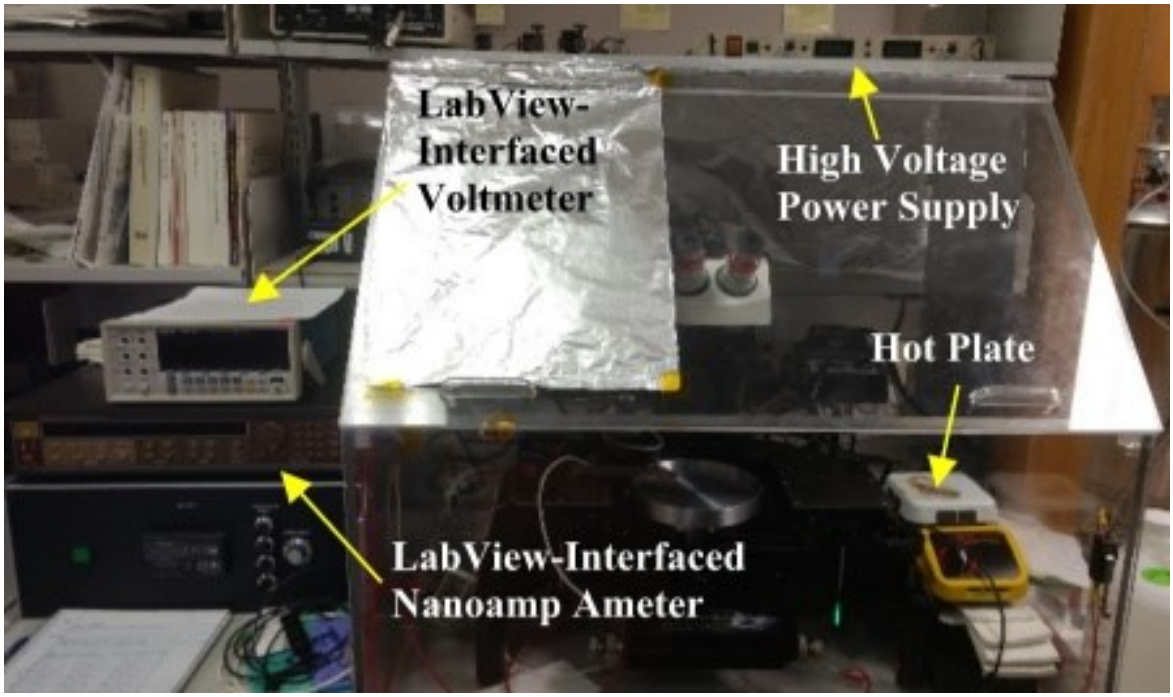


Fig. 4.9(a): Leakage current measurement test setup

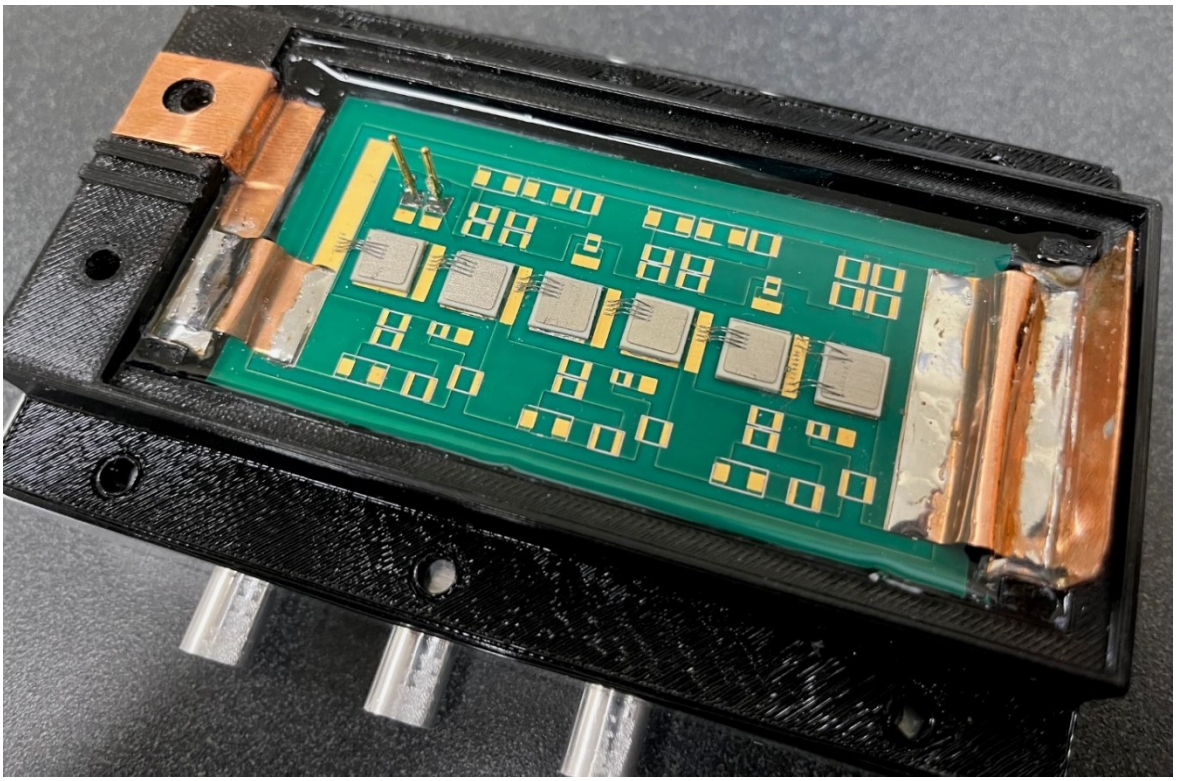


Fig. 4.9(b): Isolated DBC substrate replaces the power die inside the power module

The 6-digit Keysight B1505 multi-meter measured leakage current and plot of leakage current vs blocking voltage is shown in Fig. 4.9. The module demonstrated less than 50 nA at 25^0C. The testing validates the HV electrical operation of the Cascaded SuperCascode power module.

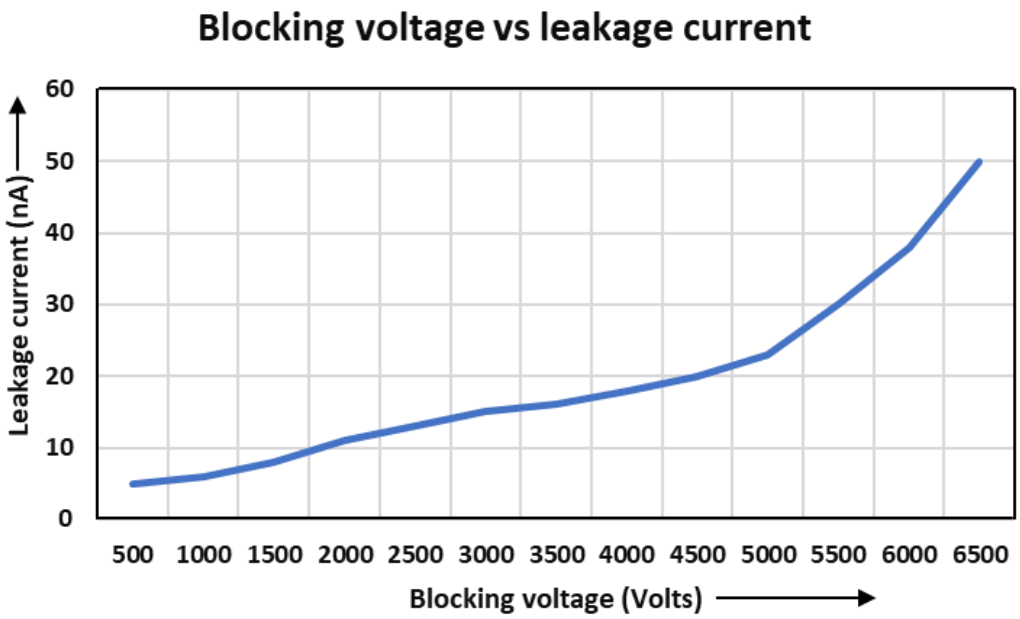


Fig. 4.10: Leakage current test result at room temperature

The power module device in comparison to Infineon 57Pak IGBT power module in the typical footprint size is shown to have 25% lower thermal resistance and 36% lower insertion inductance.

CHAPTER 5: Application of CSCPS in Solid-State Circuit Breaker

As more power electronics are introduced into the power system, the system becomes faster with lower impedance requiring even faster protection. Conventional fault interruption devices, such as fuses and circuit breakers, use thermal-mechanical means to melt materials to interrupt an arc path or rely on thermal-magnetic detection to operate contacts. The contacts use the zero crossing in the AC systems to extinguish an arc, while DC is more complex. Regardless, the thermal-mechanical means cannot provide the detection and actuation speeds for the evolving faster power grid. Other limitations such as limited lifecycle [131] and arc flash hazards further favor the development of dedicated highspeed Bidirectional Solid-State Circuit Breakers (BSSCBs) for both AC and DC systems. Note that the distinction between AC and DC BSSCBs becomes trivial, since the speed of sensing and actuation under worst-case peak currents in an AC cycle is in sub milliseconds, and bidirectional operation is generally needed in DC systems since faults can reverse power flows.

The Cascaded SuperCascode Power Switch, shown in Fig. 5.1(a) poses a promising solution is medium- and high-voltage circuit breaker applications [132] – [139]. The unique characteristics of SiC JFETs, such as robustness and reliability over repetitive cycles of switching make overall topology an attractive choice for enduring large energy stress during short circuit events. This chapter proposes a cost-efficient two-terminal BSSCB using CSCPS as the breaking element for MV harsh environment operation targeting protection in ultra-low inductance systems, as well as higher inductance systems, e.g. that use long cabling. The BSSCB incorporates an in-situ parallel transient energy absorption network to dissipate reactive system energy under fault.

Applying the Cascaded SuperCascode Power Switch (CSCPS) optimized for BSSCB operation has several advantages: (a) enables immediate fabrication of an MV power switch with commercially available *1.2kV* devices, reducing cost; (b) the balancing network enables direct paralleling of CSCPS, Fig. 5.1(b), to scale current; (c) increasing the number of serial devices scales the voltage from *6.5kV* to *>20kV*; (e) employing higher voltage JFETS, e.g. *3.3kV* SiC JFETs, would provide a fast *20kV* switch in nearly the same form factor; (f) rise and fall times are sub-microsecond to allow for ultra-fast BSSCB response from sensing to actuation; (g) distributed power dissipation over multiple devices facilitates heat extraction; and (h) a single JFET fail-short failure does not compromise the entire module, thus improving reliability. Paralleling strings shown in Fig. 5.1(b) is preferred versus paralleling HV-low current semiconductor devices to avoid the current sharing challenge described above, particularly under ultra-fast transient switching. The balancing network scales with the number of devices in serial and parallel strings. In Fig. 5.1(b) the current sharing is achieved by the balancing network capacitors which synchronously trigger JFETs J_{12} & J_6, J_{11} & J_5 and so on, design discussion is detailed in reference [139,140].

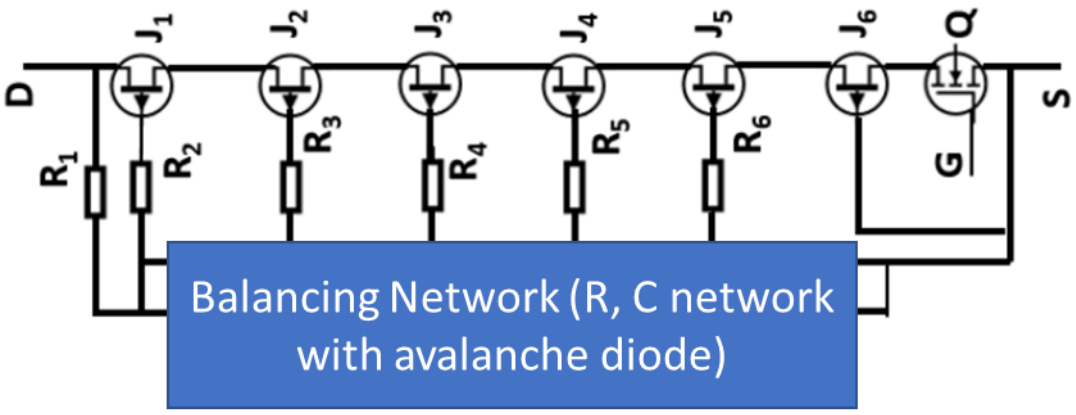


Fig. 5.1(a): 6-JFET 3 terminal Cascaded SuperCascode power switch [36]

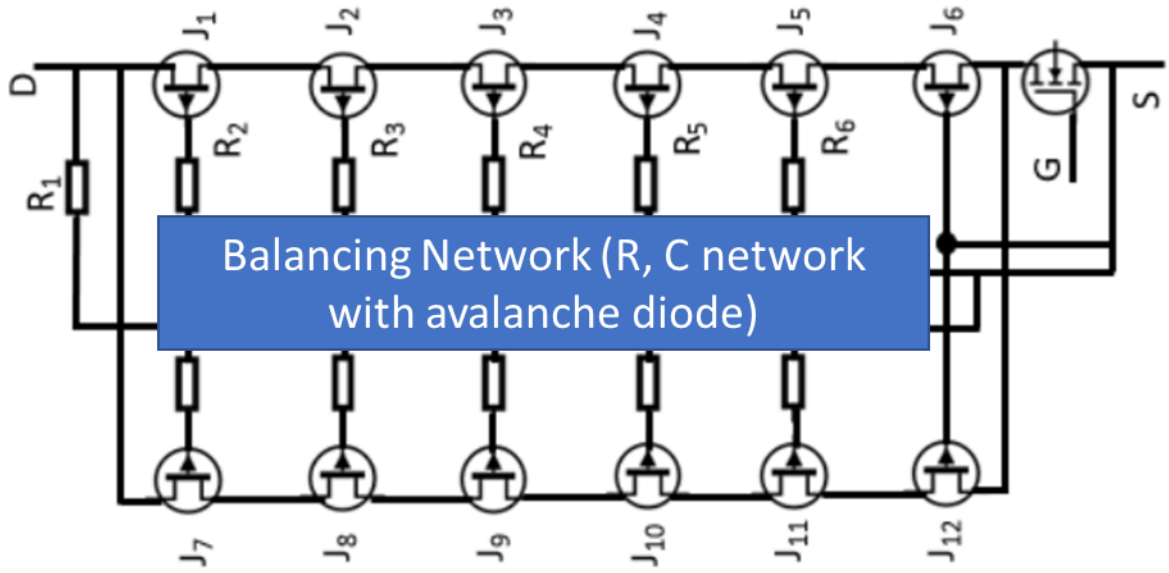


Fig. 5.1(b): 6-JFET two parallel string Cascaded SuperCascode power switch [36]

The CSCPS has drawbacks. In topology wherein each JFET blocks equivalent voltage, the lower JFET connected with the MOSFET has *30-50%* higher individual device heating due to charge flow through the string during switching [140]. Additionally, the balance network creates an additional leakage path in the off-state. Since a BSSCB spends the majority of time in the on-state, these factors are of little concern compared to other power applications. However, by adjusting the balancing network to manage the blocking voltage of each JFET in an SCPS string can enable more even heating, albeit at reduced switching speed [139].

5.1. Trip Curve

Similar to electric fuses, SSCBs are characterized by a trip curve or I^2t curve designed to protect cabling and sources [141]. The curve also defines the thermal energy relationship of the maximum time duration the semiconductor devices can conduct at different current levels constrained by the Safe Operating Area (SOA) of the devices. Unlike the trip curve for a mechanical circuit breaker, the curve represents the operational boundary and not the operating

point, and the breaker can be reprogrammed to operate anywhere below the curve and the SSCB must be designed to have fail-safe operation anywhere above the curve. A typical circuit breaker trip curve is shown in Fig. 5.2.

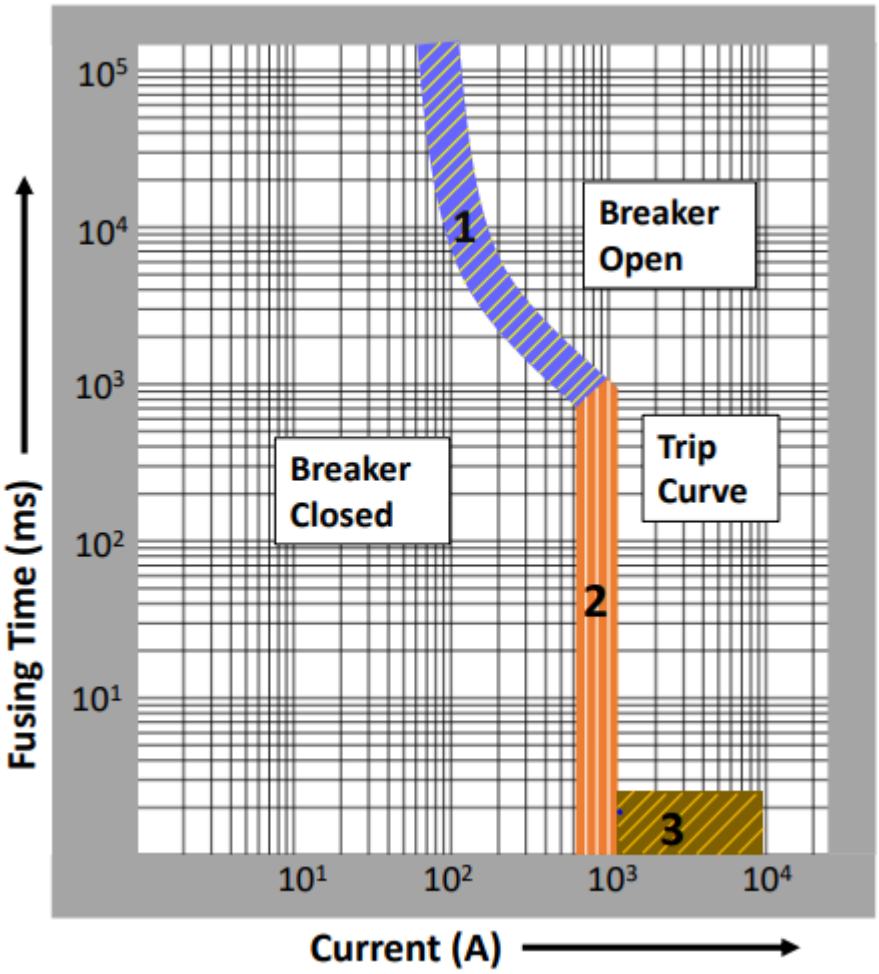


Fig. 5.2: Example of a Circuit Breaker trip curve

The trip curve is divided into three Trip Regions based on the type of response [26]. Region-1 denotes a slow cumulative RMS over-current trip response (above the *60A* nominal continuous rated current) with an inverse time relationship. The BSSCB design uses a microcontroller to monitor and integrate the current to determine a maximum cumulative heating effect in the system, e.g. cable heating. The BSSCB semiconductors also undergo current-

induced heating and are designed with a heat absorption capacity higher than the system rating. Region-2 denotes dwell time rating to prevent nuisance trips, and a maximum fault current threshold rating requiring an instant trip. Two monitoring schemes are used. One uses high-speed current monitoring and an integration algorithm to trip when rated maximum system (i.e. cable) heating occurs. The other is an instant threshold trip at maximum rated Trip Current (above *1,000A* in Fig. 5.2). Usually, the Region-1 operation is incorporated into the Region-2 algorithm.

Region-3 marks the maximum transient current values the breaker must carry during, e.g. motor starting, charge-current inrush, or an instantaneous bolted fault. This is the typical operating mode that many SSCB publications are focused, but is only of limited application. The BSSCB design for Region-3 operation uses a *di/dt* detection scheme to perform an instantaneous trip when the extended Trip Current magnitude is exceeded. As seen later, a small inductance integrated into the power module provides a minimum delay time as needed for rapid current sensing and actuation.

5.2. Overview of BSSCB CSCPS Design

The design of the BSSCBs considers the amount of fault current to be cleared, the dwell time (delay time) for fault clearing and control to allow for fault coordination, particularly in a cascading fault scenario. The non-hybrid BSSCB design is divided into four module layers as shown in Fig. 5.3.

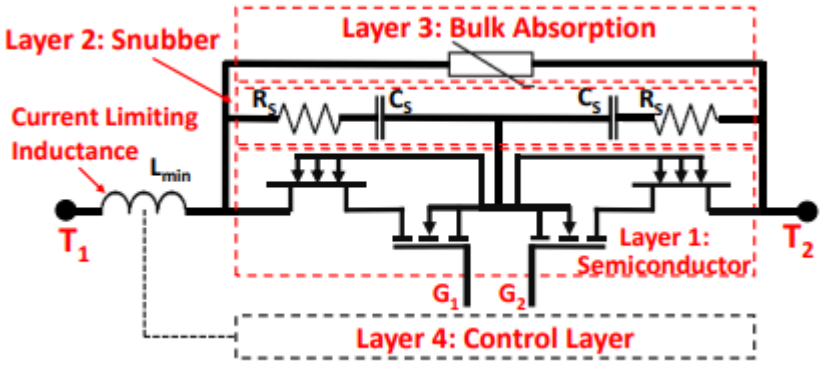


Fig. 5.3: Power stage schematic of BSSCB

During on-state operation the semiconductor switches are continuously on. Once switches actuate to open the circuit, all electrical energy is transitioned to the snubber and bulk absorption (MOV) layers. Either of two product ratings determines the design size of the needed semiconductor layer. One is the breaker 'on-state' efficiency or allowed continuous loss. The second is rated trip current and dwell time at rated trip (*1 kA* at *1 ms* in Fig. 5.2). The first determines the number of parallel semiconductors or equivalent semiconductor die area needed in the layer. The second determines the maximum required transient thermal energy absorption by the semiconductors. If the BSSCB is used in a "Hybrid Breaker" where the semiconductor layer is paralleled by mechanical metal contacts (for near-zero on-state loss), the transient thermal design is only considered. Though the on-state loss of a single BSSCB appears small in an MV system, the cumulative losses of many distributed BSSCBs becomes large. Thus, a design target of a BSSCB is an ultra-low on-resistance, which can be effectuated through use of WBG semiconductors.

The maximum inductive energy rating for the BSSCB, like traditional DC breakers, indicates the maximum energy absorption allowed by the breaker. The BSSCB design of the snubber and energy absorption layer (Fig. 5.3) is dictated by the cumulative system inductance, such that all

inductive energy is absorbed and dissipated by the snubber and MOV layers. Hence, the design of a family of BSSCBs would consider the amount of fault current to be cleared, the dwell time (delay time) for fault clearing, amount of allowed inductive energy, and control to allow for fault coordination, particularly in a cascading fault scenario.

5.3.BSSCB Power Stage Design

5.3.1. Layer 1: SuperCascode semiconductor layer

The design of the SuperCascode Power Switch (SCPS) as the breaking element of the BSSCB is given below. The number of JFETs '*N*' in the SCPS (Fig. 5.4(a)) is calculated from the BSSCB Voltage Rating, V_R, and JFET V_{DS} as:

$$N = \frac{V_R\left(1 + \frac{X_S}{100}\right)}{V_{DS}} \tag{5.1}$$

where X_S is the percent safety margin maintained in design to allow for voltage overshoot. The X_S value is representative of derating in switch selection considering the worst-case overshoot from the device layout. The number of parallel SuperCascode strings, N_P, to increase current capability is:

$$Int(N_P) = \frac{I_R}{I_{DS}} \tag{5.2}$$

where I_R is the BSSCB rated operating current (steady-state), I_{DS} is rated JFET continuous current, and N_P is rounded up to a whole integer. As shown in Fig 5.3, two SCPS are placed back to back in a common source topology. The common source topology allows for bidirectional flow and blocking capability and simplifies the gate driver design by providing a common ground. The total on-resistance of the BSSCB, R_T, is determined from the steady-state operation with current flowing through one set of SuperCascode JFETS and MOSFET, and the internal anti-parallel diodes of the other switching unit (Fig.5). Thus, the R_T is calculated as:

$$R_T = \frac{(N * (R_{DS} + R_M)) + R_D}{N_P} \tag{5.3}$$

where, R_M is the resistance of the LV Si MOSFET, R_{DS} is the on-resistance of the JFET and R_D is the forward resistance of the anti-parallel diodes. Thus, the breaker efficiency, η of the BSSCB can be represented as:

$$\eta = 1 - \frac{I_R}{V_R}\left(\frac{(N * (R_{DS} + R_M)) + R_D}{N_P}\right) \tag{5.4}$$

Equations (5.1)-(5.4) define the number of JFETs per SuperCascode string and the strings in parallel required to meet the electrical performance ratings of a BSSCB.

5.3.2. Layers 2 & 3: Energy Absorption Layers

The transient absorption layers, which parallel the SCPS, control the *di/dt*, *dv/dt*, and absorb and dissipate the reactive system energy guaranteeing a safe operating area for the SCPS. The Snubber and Bulk Energy Absorption layers are shown in Fig. 5.3. The Snubber layer shapes the fast di/dt limiting the initial voltage overshoot. The Bulk Energy (MOV) layer clamps the voltage and absorbs stored energy in the system inductance.

1. **Snubber Design**

When the breaker opens at maximum trip current, I_{Trip}, (Region-2), the snubber resistance, R_S, limits the overshoot voltage, V_N induced by the *di/dt* and system inductance, L_S. The V_N is a product parameter and determines the required semiconductor V_{DS}. The snubber capacitance, C_S, begins to absorb a portion of the system energy while the Bulk Energy Storage Layer (MOV) responds to clamp the full V_N. The C_S selection is highly dependent on the physical packaging of the BSSCB and interconnects impedances that limit the energy transfer from the Snubber to Bulk Energy layer. The C_S in (5.7) can be refined if specific packaging

information is known. An alternative calculation, as shown, uses the rated current, IR, to offload the energy requirement for the MOV layer.

$$R_S = \frac{V_N - V_R}{I_{Trip}} \tag{5.6}$$

$$C_S > \frac{L_S I_R^2}{V_R^2} \tag{5.7}$$

2. Bulk Energy (MOV) Design

An MOV layer (composed of many series and parallel MOV components) was selected. The maximum allowed current in the MOV is determined from the non-linear I-V characteristic [33] as

$$I_{mov} = kV_{mov}^{\alpha} \tag{5.8}$$

where, k is related to the series-parallel component structure and α is degree of nonlinearity dependent on the material properties. The nominal MOV voltage, $V_{mov}^{nom} > V_R$ to avoid current leakage during steady stage operation. For a ZnO MOV, α is between 5 and 20 [143]. The required bulk energy capacity is dependent on the extended maximum trip current, $I_{ext\text{-}Trip}$ defined in Region-3, and is

$$E_{mov} = L_S\left(I_{ext-Trip}^2 - I_N^2\right)/2 \tag{5.9}$$

3. Current Limiting Inductance

In the BSSCB, a delay time exists in current sensing, computation and actuation of the semiconductor string. Thus, to always ensure protection against a worst-case fast no-impedance fault, a current limiting inductance, L_{min} is built into the BSSCB to limit the switching *di/dt*. The L_{min} is sized according to the following relationship, where *dt* is the total time delay in the controller and V_R is the DC system voltage.

$$L_{min} \geq \frac{V_R}{di} * dt \tag{5.10}$$

A design target example is given in Table 5.1 for a *10kV/300A* breaker. A BSSCB design using SCPS breaking elements is presented and compared to Schnieder Electric EasyPact EXE (Part Number: EXE122006A1B) MV-AC 3 phase circuit breaker rated for *12kV/300A*. Equations (5.1)-(5.9) are applied to the design for a *3X* trip and *5ms* dwell (Region2). The BSSCB is designed to protect with *12μH* of cabling (*15m*). The maximum allowed overvoltage of the semiconductors is *11.9 kV*. The resulting design values are summarized in Table 5.2. A 3D rendering of the BSSCB is shown in Fig 5.4(a) and the size comparison to the EasyPact EXE is presented in Fig 5.4(b). The volumetric comparison showed that the 3-SSCB BSSCB fits within the EasyPact EXE footprint (*527 x 470 x 429 mm*).

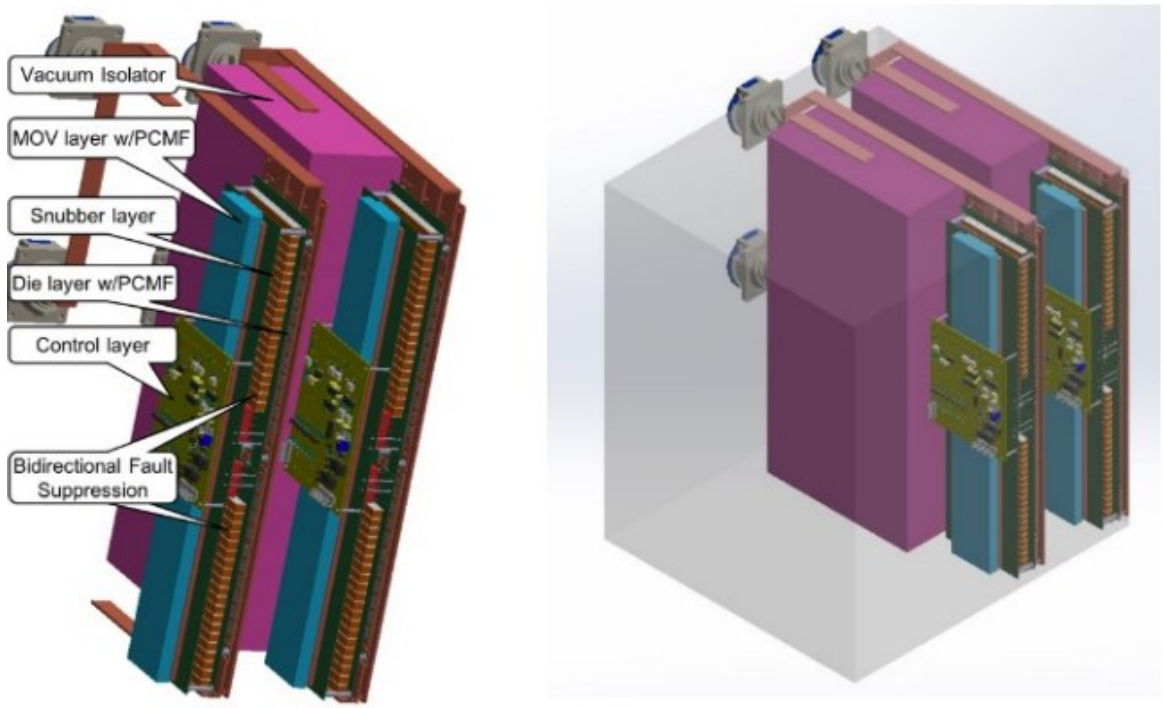


Fig 5.4(a): Strawman design of the BSSCB, (b) Three proposed SSCSBs fit within the EasyPact EXE footprint. Two are shown. Each are rated for V_R=10kV, I_R=300A, 10X.
(Purple lightning isolator)

Table 5.1: BSSCB Design Target	
Category	Design Target
Rated Voltage	10 kV
Rated Power	30 MW
Rated Current	300 A/ 3x w/ Dwell for > 5 ms
Response Time	Instant trip <300 ns

Table 5.2: Overall BSSCB Design	
Specification	Ratings
Semiconductor Layer : Common-source connected SCs	
Rated Voltage	10 kV
Rated Current	612 A @ 25^0C / 300 A @ 125^0C
Layout (x2 for bidirectional)	$N_{series} = 7$; $N_{parallel} = 3$
Efficiency	99.97 % @ RT
Snubber Layer	
Capacitance and Resistance	680 nF and 2Ω (Optimized by simulation)
MOV Layer (Stackpole Electronics ZOV680K23 is volumetrically scaled)	
Clamping Voltage	11.9 kV
Nominal Voltage	10.5 kV
Bulk energy capacity	8.125 W
BSSCB Current limiting inductance	1 μH

5.4.Physical SCPS Power Module Design

5.4.1. Power Circuit Design

Similar to the wire fuse trip curve, the SCPS design is thermally defined as previously discussed for the Regions of operation. For ultra-fast transient thermal operation, heating primarily occurs in the semiconductor layer with extension into the metal interconnect. This is particularly important for SiC power devices that undergo wafer thinning and have high thermal conductivity. For slower, but longer transients, more thermal energy diffuses further into the physical power switch structures [133]. To ensure that the BSSCB does not fail, the BSSCB SOA must keep the semiconductors within their SOA. Thus, the trip curve defines the minimum amount of time the BSSCB can sustain a given current before the devices exceed their critical junction temperature ($T_{j,c}$). This time is dependent on the ambient temperature and thermal

power stage design. As highlighted in Table 5.2, three SCPSs are placed in parallel to meet a user-defined ≥*99.7%* efficiency, i.e. low onstate loss, for a *10 kV/300 A* BSSCB. Each JFET only conducts *100 A* in steady-state. To define an equivalent fuse curve, time-dependent heat transfer simulations were performed in COMSOL Multiphysics, evaluating transient temperature rise for multiple trip currents up to *3X* nominal. A simplified *3D* geometry, Fig. 5.5, was imported into COMSOL. The simulation parameters are in Table 5.3. The AlSiC baseplate is cooled having a natural convection coefficient of $15W/m^2K$ at 20^0C ambient. Heat sources, I^2R_{DS}, are added to the JFETs and MOSFETs. The R_{DS} relationship (for UnitedSiC UJ3N17005 JFET) is:

$$R_{DS}(T) = 3 * 10^{-5}T^2 + 0.0015T + 0.9588 * R_D \tag{5.11}$$

where, T is the junction temperature (^{0}C) and R_D is the nominal resistance at 20^0C. All other surfaces are adiabatic.

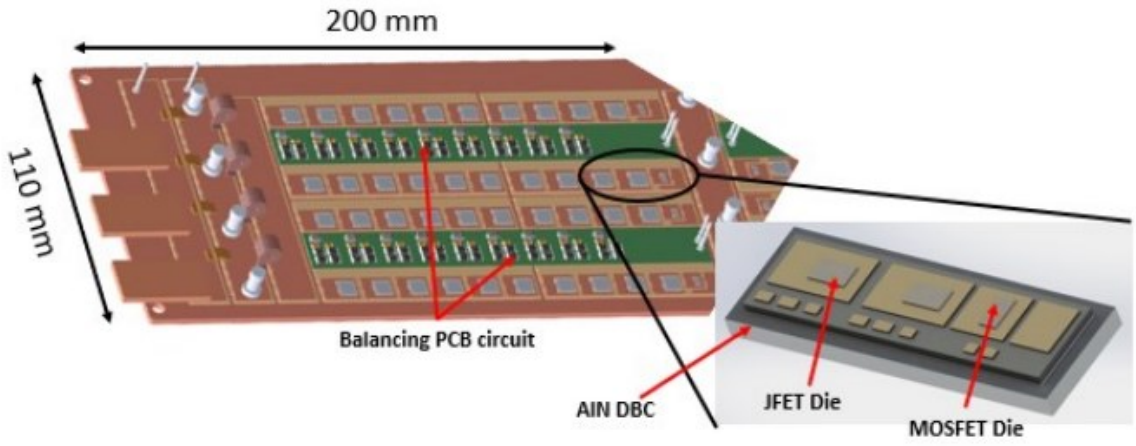


Fig. 5.5: 3D model of the SSCB semiconductor layer

Table 5.3: Material Thickness and Properties of simulated power module with Alumina DBC Substrate				
Layer	Thickness [mm]	C_p [J/kg]	P [kg/m^3]	K [W/mK]
SiC (8 mm x 8 mm)	0.15	1200	3200	450
Ag Sinter	0.035	235	10500	175
Cu pad	0.127	385	8700	400
Alumina	0.508	900	3900	27
Cu pad	0.127	385	8700	400
Ag Sinter	0.035	235	10500	175
AlSiC	2	741	3010	180

The equivalent fuse curve in Fig. 5.6 shows the time to reach critical $T_j = 175^0C$ from 20^0C ambient for multiple trip currents. The trip curve boundary is represented by the following trendline and utilized in the controller to assure operation within the SOA.

$$t = 0.118 * I^6 - 0.6514 * I^5 + 14.755 * I^4 - 176.2I^3 + 1182.3 * I^2 - 4307 * I + 6884.8 \quad (5.12)$$

where, t is the trip time in ms and I is the BSSCB current.

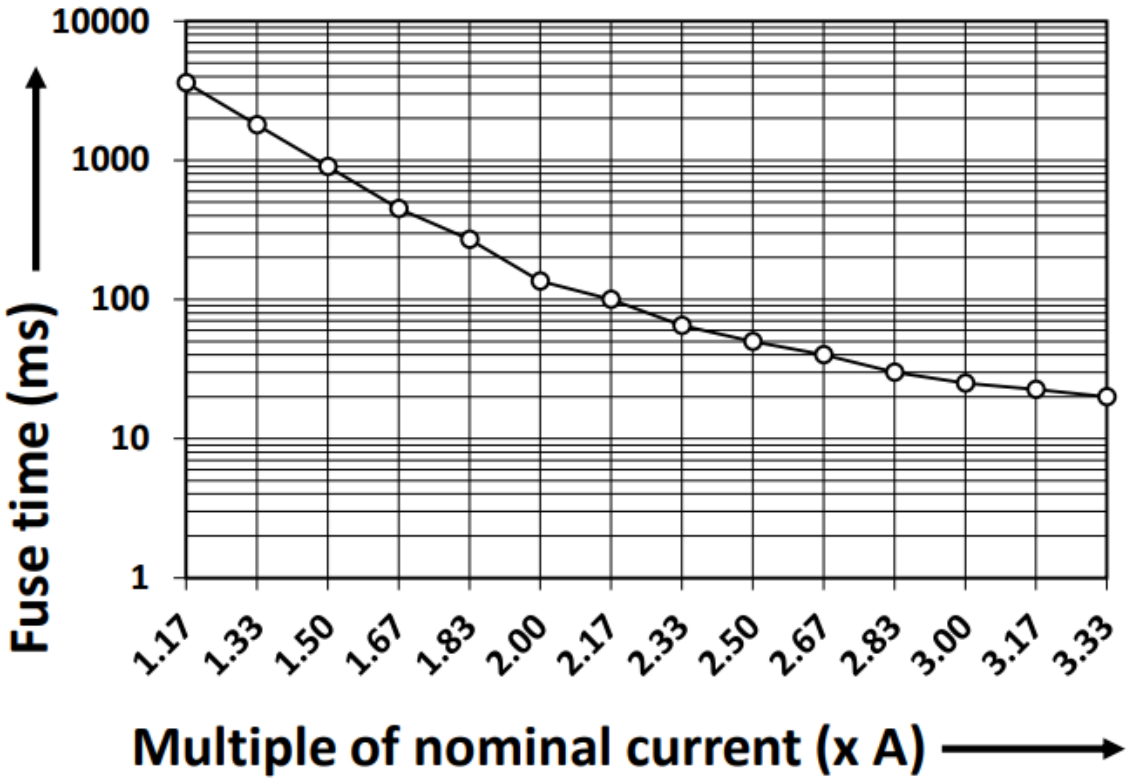


Fig. 5.6: Operational boundary fuse Curve of the Bidirectional Solid State Circuit Breaker

5.5. Control Scheme

The BSSCB control, Fig. 5.7, relies on a low-loss, compact high-bandwidth current sensor for fast response. High bandwidth current sensing techniques utilizing a magneto current sensor [40-42] have current saturation issues and are physically large making module integration difficult. A fast *100 m*Ω sensor [144] adds significant conduction losses, decreasing system efficiency. Previous work in [145] addresses both these issues by using a planar resistive current sensor composed of multiple parallel resistors configured with inductance cancelation among adjacent resistors, Fig. 5.8(a).

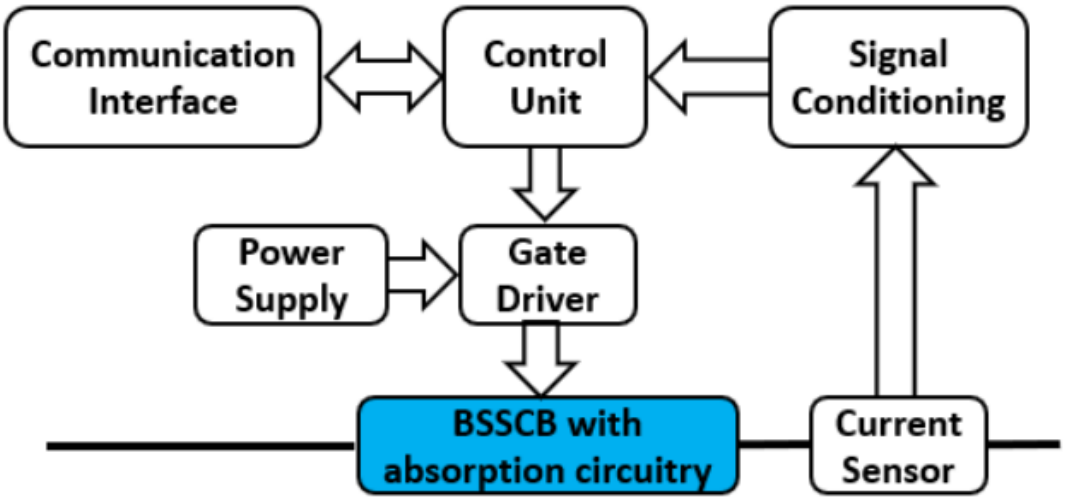


Fig. 5.7: BSSCB control scheme block diagram

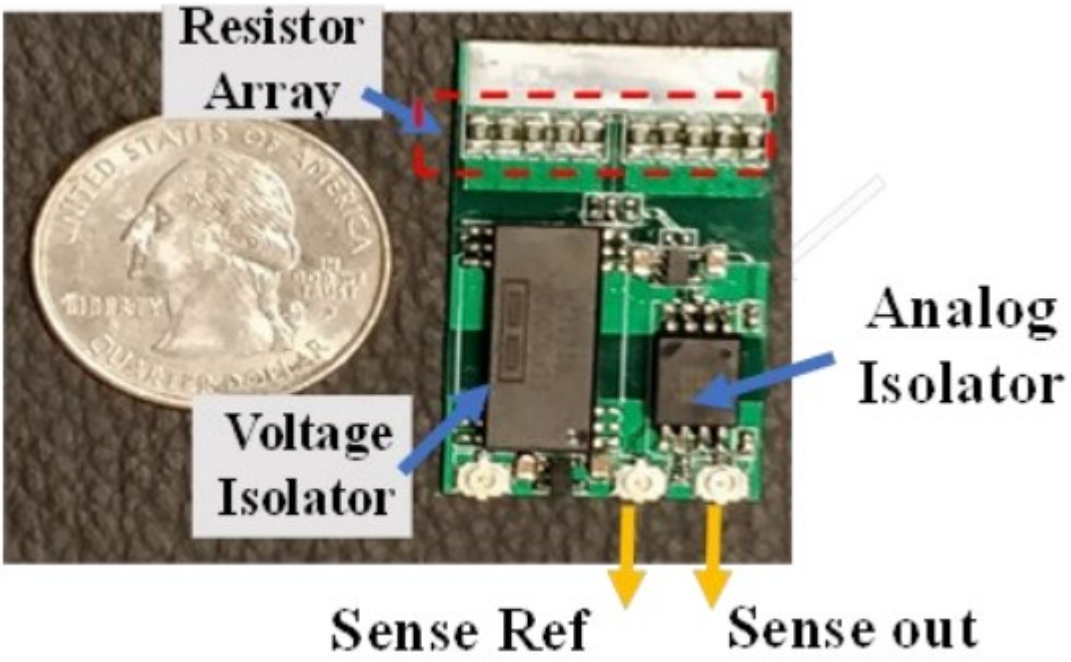


Fig. 5.8(a): High Bandwidth (20 MHz) resistive current sense [39]

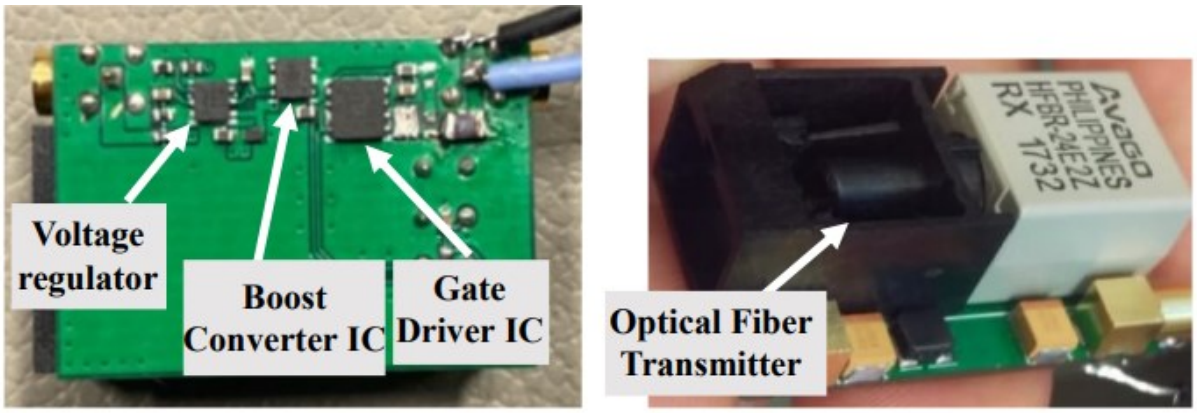


Fig. 5.8(b): HV Optically isolated Gate Driver (17 mm X 12 mm) (L) Bottom Side PCB (R) Top Side PCB

The current sense signal feeds a digital control unit, such as a DSP, FPGA, and microcontroller. For work reported here the PSoC 5LP:CY8CKIT-059 microcontroller was utilized for its low cost and high system clock of *80 MHz*. A USB UART serial communication interface performs serialparallel data conversion both on the receiver and transmitter sides, which can modify the trip curve boundaries in realtime. A digital isolator (LTP2884) provides additional voltage isolation. An optically isolated gate driver is fabricated and shown in Fig. 5.8(b). The driver utilizes a DC/DC *6kV* isolated converter (MORNSUN G_S-2WR2), and a fiberoptic cable for signal isolation. The driver is powered by a *9V* supply and a locally present isolator and boost converter can adjust the driver output from *-5* to *+20 V*. Self-oscillating gate drivers discussed in [146] can also be used in future BSSCB applications depending on the gate driver power requirement.

5.6.Hardware Results

To validate the SCPS as the breaking element and evaluate performance under a short circuit, a scaled *6kV/10A* SCPS is created using discrete commercially available JFETs. The physical prototype is shown in Fig. 5.9 and consists of six *1.2kV/80 mΩ* UnitedSiC JFETs (UJN1208K) controlled by a *25V* Si MOSFET (BSZ018NE2LSIATMA1). Table 5.4 lists the balancing

network component values. The SCPS is tested under two extreme fault scenario's, one addresses ultra high speed of response for no inductance when the switches open with need for snubbers. The second addresses a maximum line inductance when the open as in the first scenario, but then transitions current into the snubbers and absorption circuit.

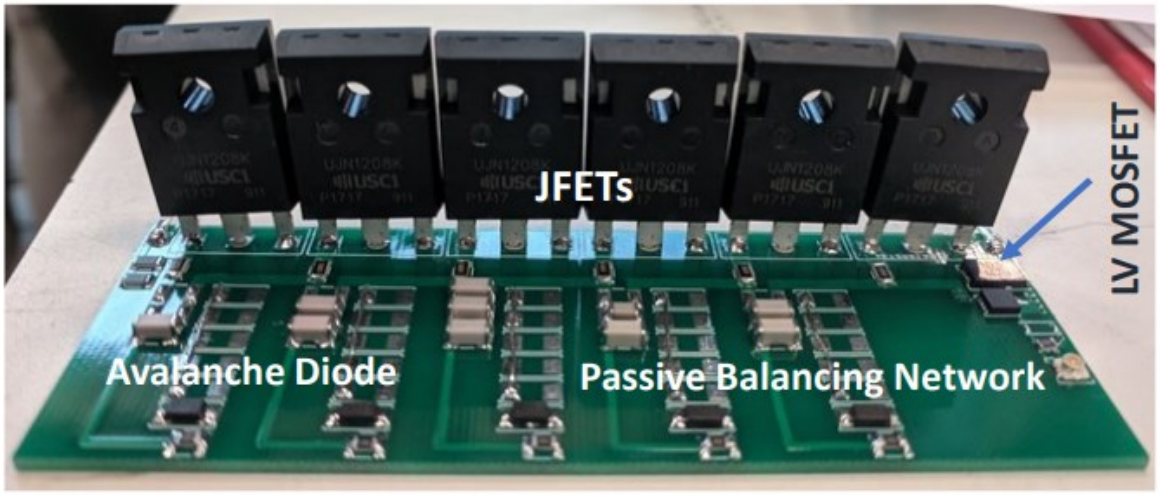


Fig. 5.9: 6kV/10 A SuperCascode Power Switch

Table 5.4: Component Values of 6kV/10 A SuperCascode	
Component	Value
C_1	68 pF
C_2	136 pF
C_3	214 pF
C_4	282 pF
C_5	340 pF
R_1	4 MΩ HV resistor
R_2-R_5	10 Ω high surge capacity
D_1-D_5	AU1PK Avalanche diode

In the first scenario, the SCPS is opened into a dead short fault without any resistance or inductance limiting the current for a $1\mu s$ at $2kV$, driving the switch into saturation, Fig. 5.10. Results show successful current interruption in $40\ ns$.

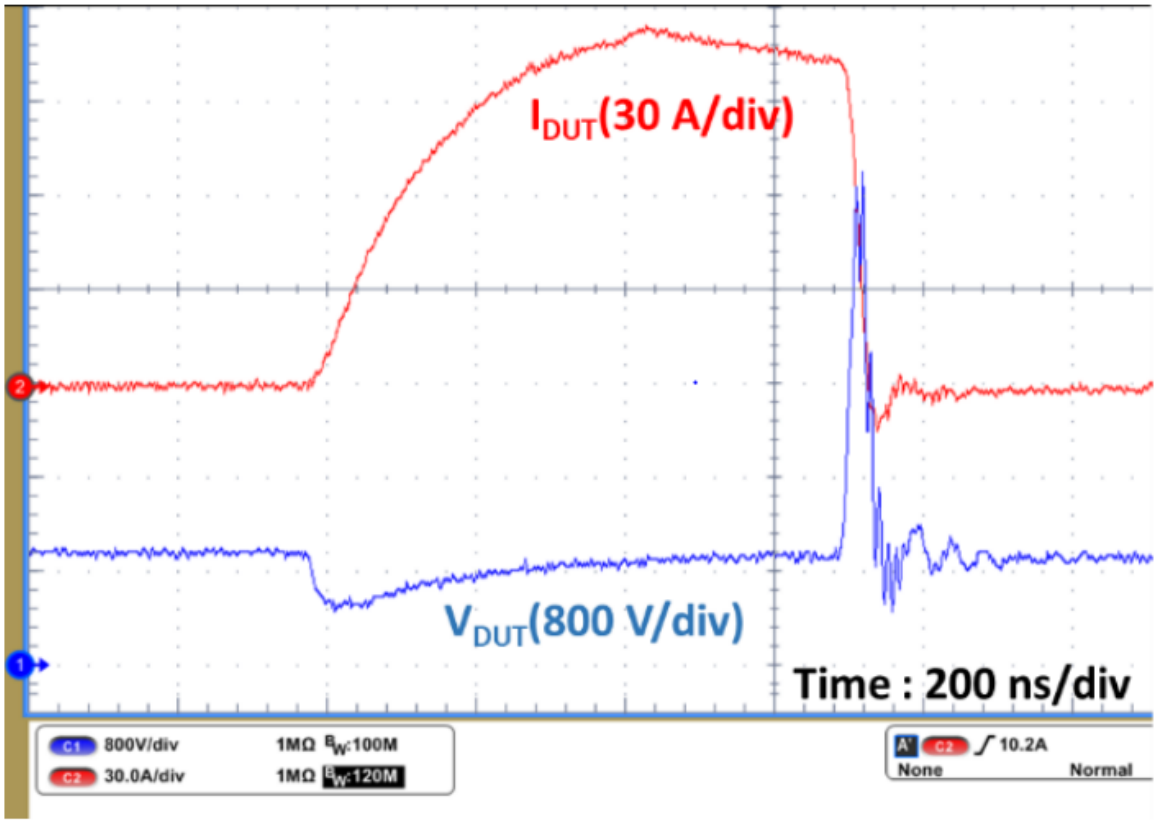


Fig. 5.10: Voltage and current waveforms of SCPS tested under a *2kV* dead short with no line inductance and resistance

In the second scenario, a *3kV* source is applied to the SCPS with an RL load in series with the DUT. The test circuit schematic and hardware setup is shown in Figs. 5.11(a) and 5.11(b) respectively.

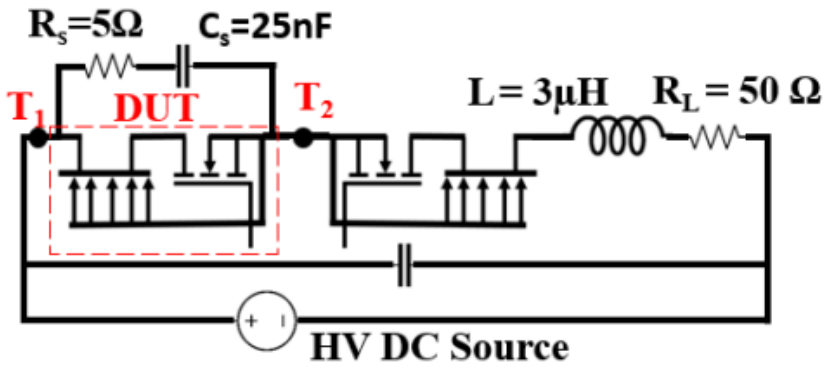


Fig. 5.11: Scenario 2 (a) Test setup schematic

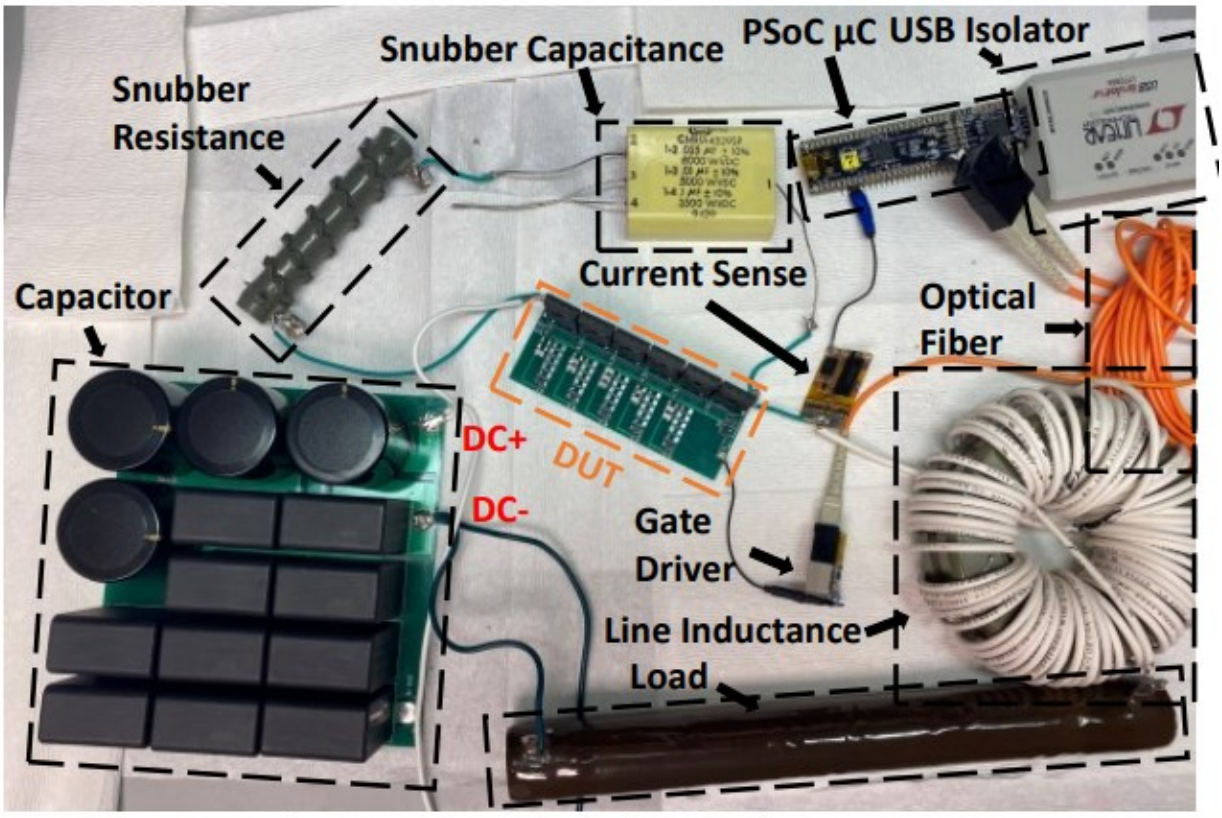


Fig. 5.11: Scenario 2 (b) Hardware setup

The SCPS conducts *70A*(*7X* of nominal *10A*) for *1µs* (thermally limited) and then the SCPS is triggered off, and the RC transient absorption circuitry absorbs the reactive R_L-L load energy. The results without and with the snubber are given in Figs. 5.12 and 5.13, respectively. Different overcurrent scenarios and voltage overshoots are summarized in Table 5.5. The current interruption was *60 ns*.

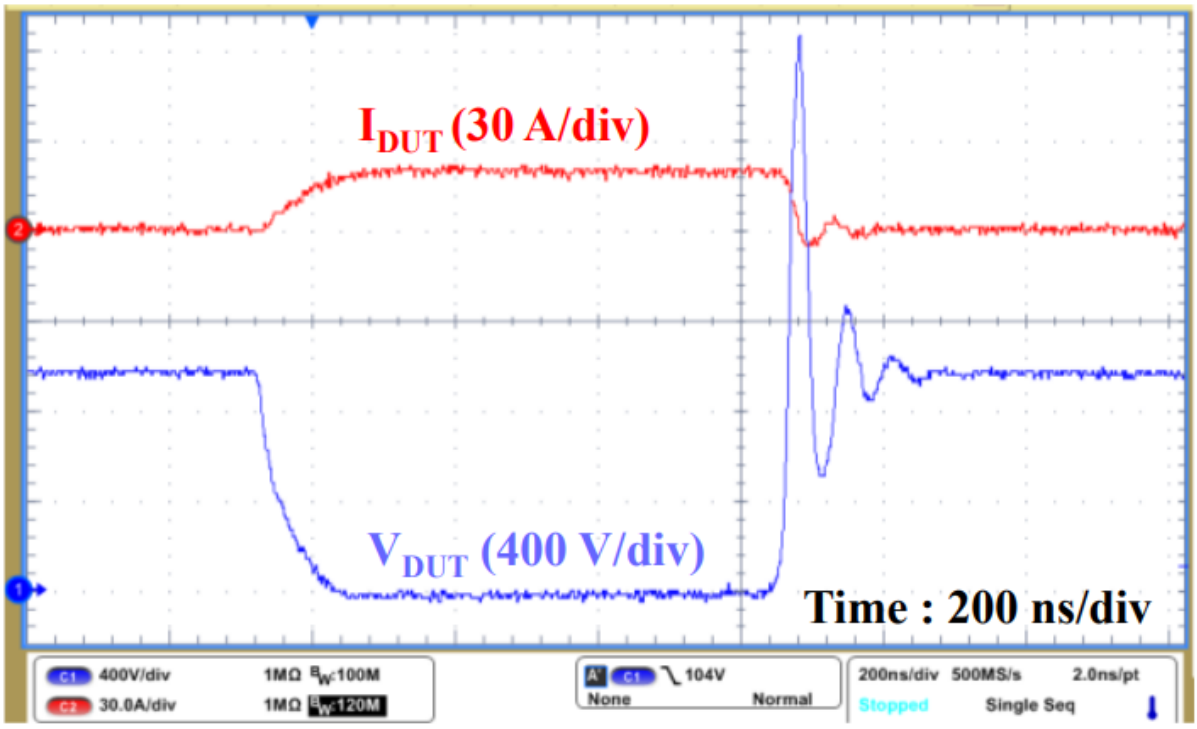


Fig 5.12 (a): Voltage and current waveforms of SCPS tested under 1kV 20 A operation as DUT without snubber/transient absorption circuitry

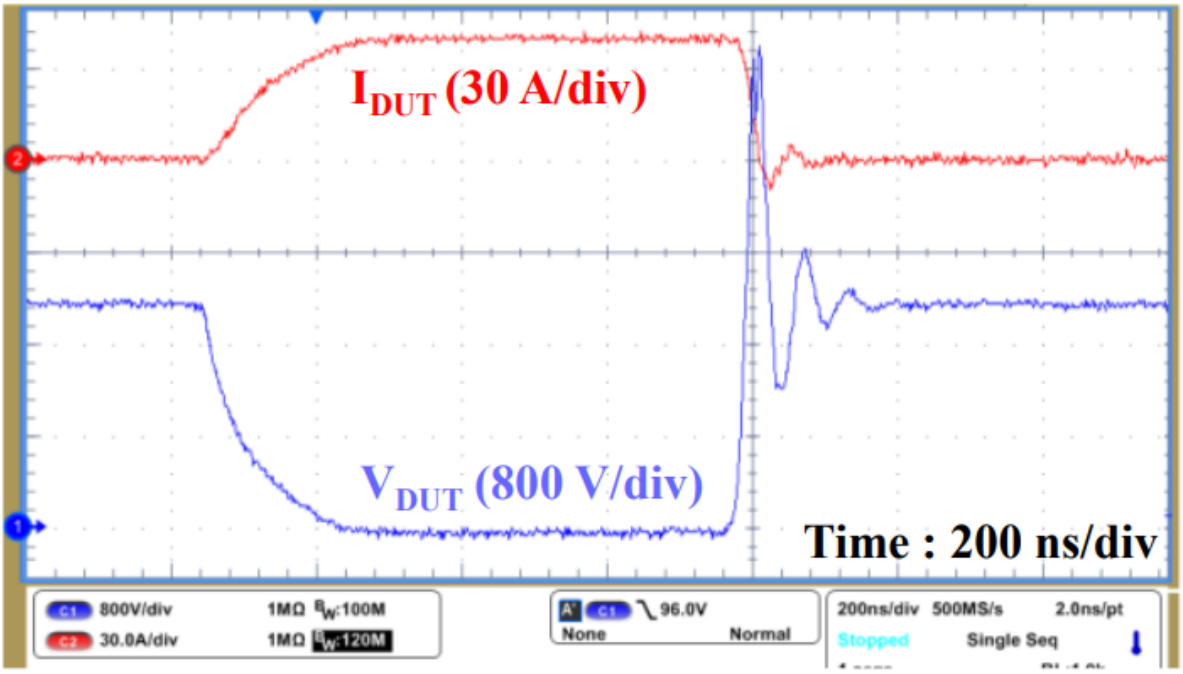


Fig 5.12 (b): Voltage and current waveforms of SCPS tested under 2kV 40 A operation as DUT without snubber/transient absorption circuitry

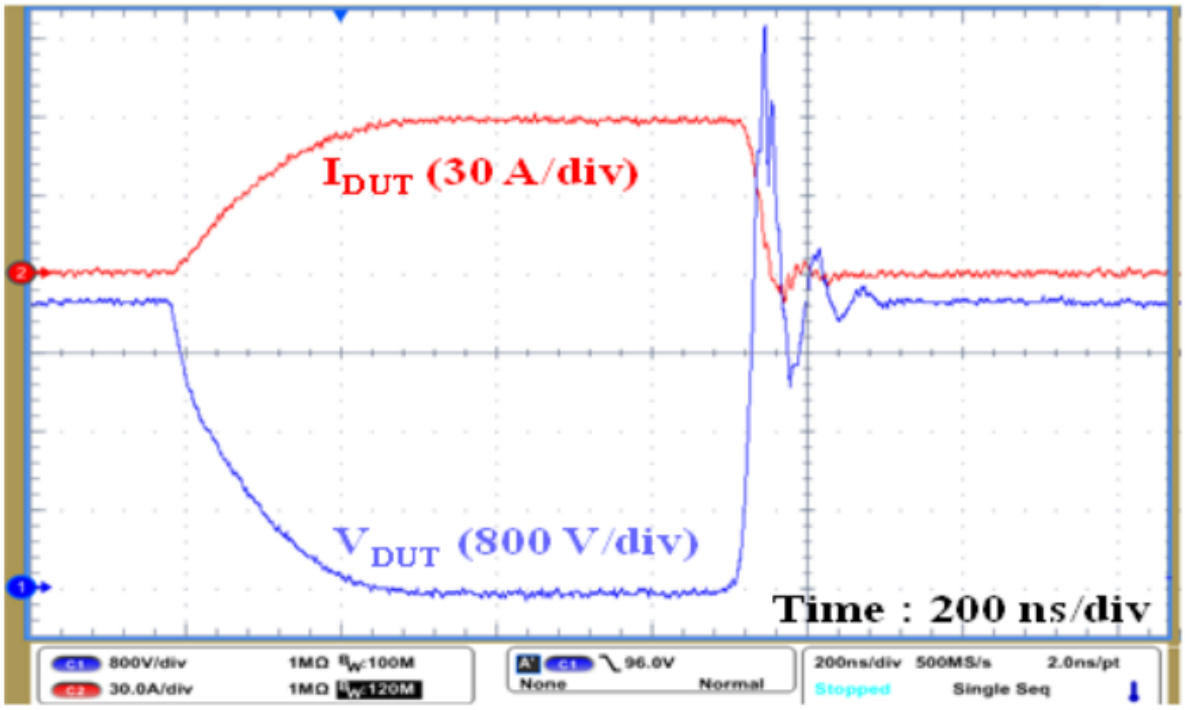


Fig 5.12 (c): Voltage and current waveforms of SCPS tested under 3kV 60 A operation as DUT without snubber/transient absorption circuitry

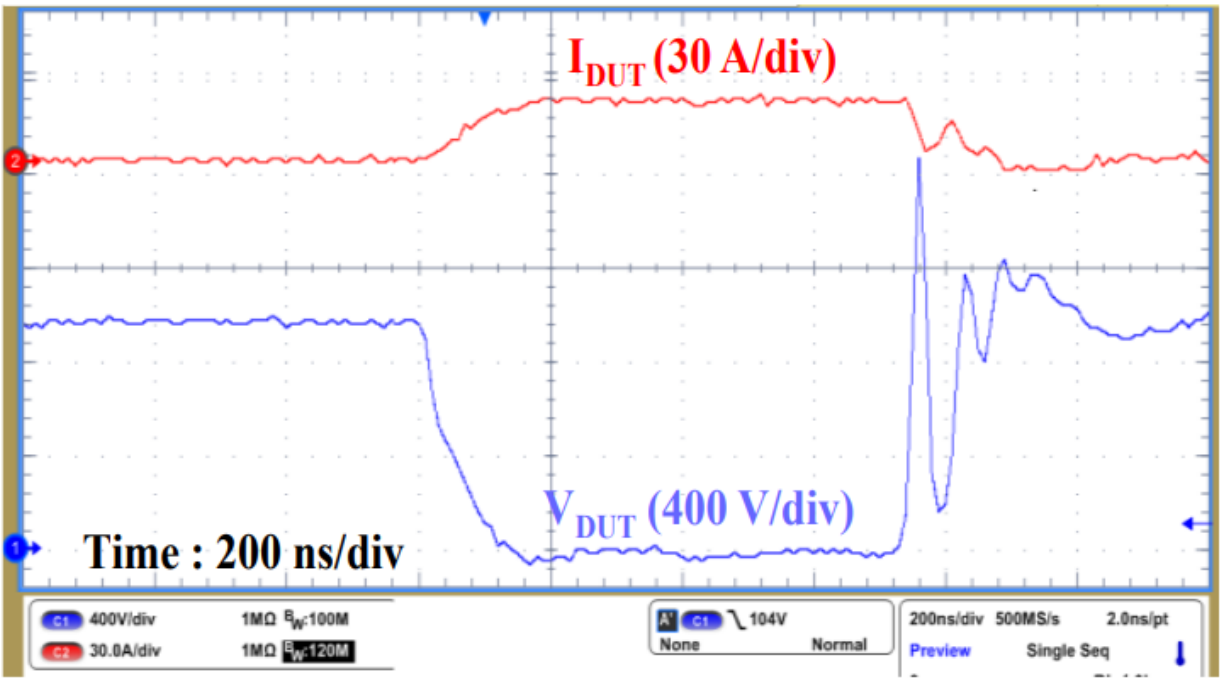


Fig 5.13 (a): Voltage and current waveforms of SCPS tested under 1kV 20 A operation as DUT with snubber/transient absorption circuitry

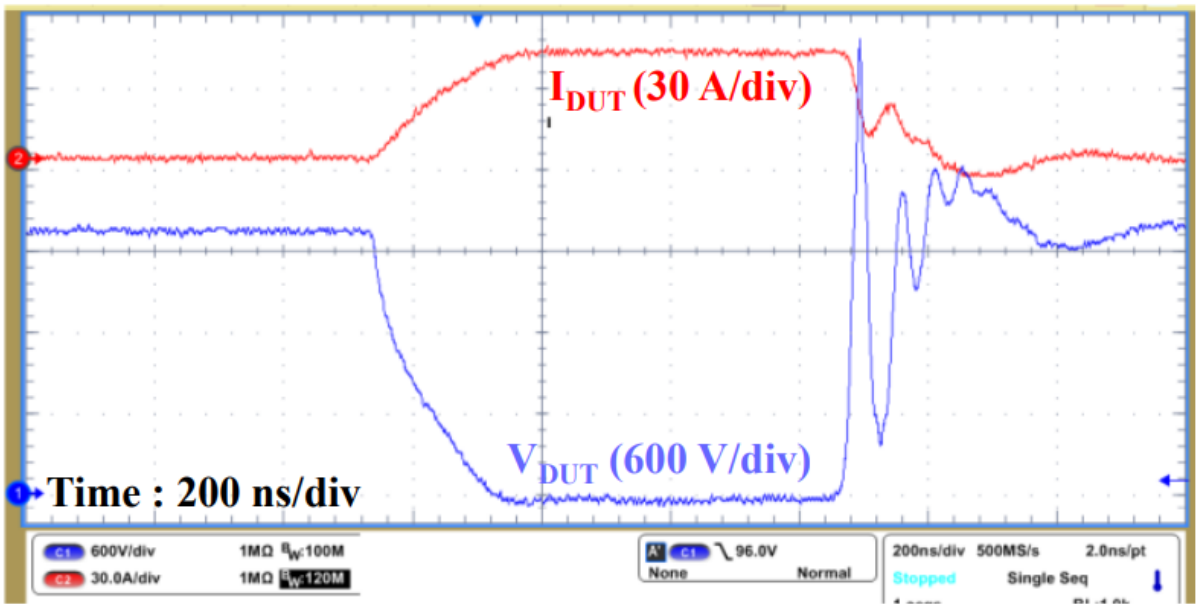


Fig 5.13 (b): Voltage and current waveforms of SCPS tested under 2kV 40 A operation as DUT with snubber/transient absorption circuitry

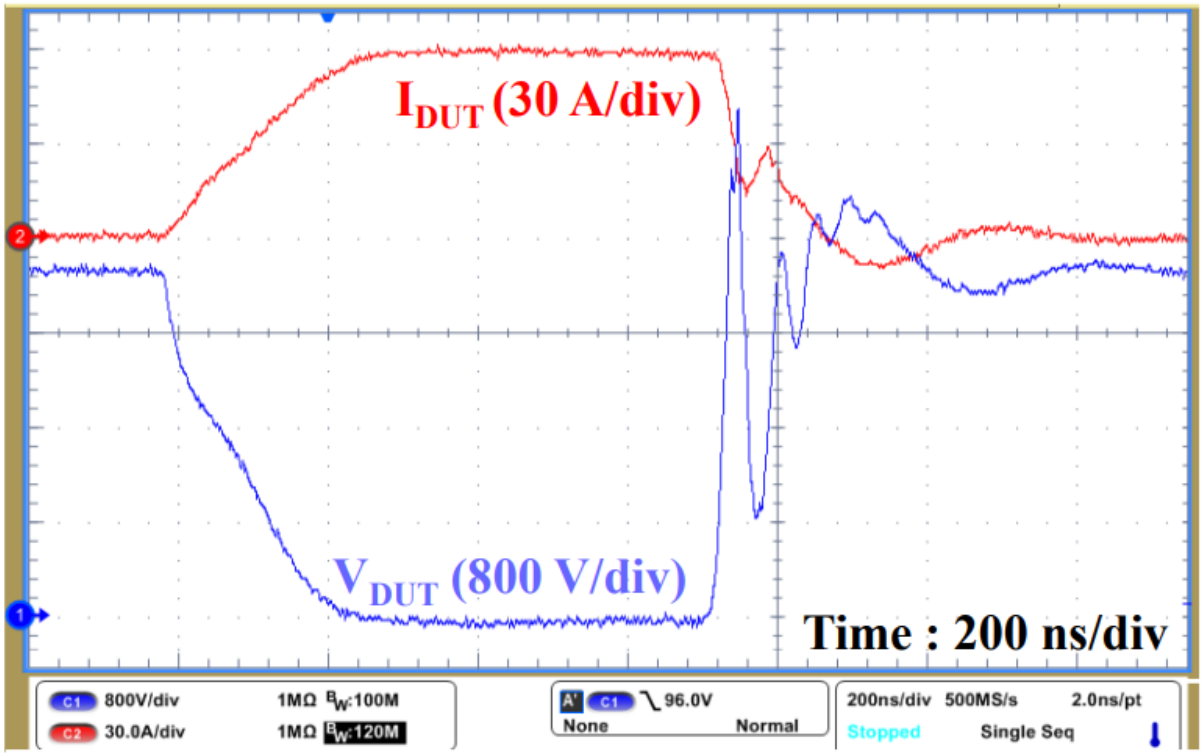


Fig 5.13 (c): Voltage and current waveforms of SCPS tested under 3kV 60 A operation as DUT with snubber/transient absorption circuitry

Table 5.5: Overshoot measured at different overcurrent test scenario's			
Test Condition (Device rated – 10 A)		Overshoot	
DC Bus	Current	Without Snubber	Snubber
1 kV	20 A i.e. 2X	1520 V	650 V
2 kV	40 A i.e. 4X	2240 V	1240 V
3 kV	60 A i.e 6X	2880 V	1520 V

The experimental results highlight that the SCPS is capable of maintaining sequential switching under high *di/dt* and *dv/dt* as required in SSCB applications. The results shown in Fig. 10, 12 and 13 demonstrate that the SCCB system, i.e the current sense, gate driver and the SCPS are capable of interrupting the current in *60 ns* and the addition of a simple transient energy absorption circuitry is able to reduce the peak voltage overshoot ensuring that the device always operates within its safe operating area.

The paper presents the mathematical design equations of the BSSCB as divided into four defined layers: semiconductor (SCPS), snubber, bulk absorption (MOV), and control. Design of the SCPS is given in detail, with references, including COMSOL thermal simulation identifying transient heating extremes in the semiconductor modules that drive the design. Also, described are operating region equivalencies for a fuse curve to define BSSCB design requirements. Design of the control hardware is given including a unique low-cost high bandwidth current sensor, high voltage fiberoptic signal isolator and gate driver.

A 6kV/10A/7X BSSCB is fabricated and tested in a 10Anominal, 70A-trip scenarion to confirm the design and operation of SuperCascode Power Switches (SCPS) in an BSSCB application. The BSSCB was designed to confirm a 99.7% efficiency. Results demonstrate fault detection and actuation in 200 ns with successful 70A current interruption in 60 ns (260 ns total)

CHAPTER 6: Conclusion and Future Work

This dissertation introduces methodologies of cascading and scaling to realize a novel high voltage Cascaded SuperCascode Power Switch (CSCPS). It focuses on analysis, optimization, implementation and testing of CSCPS. The dissertation also introduces a segmented baseplate power packaging approach for HV WBG power devices with a new sustrate material for elevated thermal, mechanical, electrical performance and low cost.

6.1. Summary of the dissertation

The dissertation starts with a discussion on the current state of art reported HV power switches and SuperCascode switching topologies. It then discusses the voltage scalability and performance limitation of each SuperCascode structure. The research introduces new methodologies of cascading and scaling to realize high voltage Cascaded SuperCascode power switch (CSCPS). This dissertation specifically discusses design with normally-on SiC JFETs devices however, the concepts are applicable to all normally-on switches having turn-on threshold control voltage >0V. The work explains the working of the CSCPS, design of the CSCPS and an optimization sequence which compares different configurations of CSCPS and selects the optimum. Also provided is an analytical model to enable optimization of the structure design to compensate for device tolerances and stray-parasitics that might limit the performance of the power switch, lead to delays in triggering serial devices, de-synchronization of triggering and unexpected overvoltages that limit scalability. Based on the analysis, a 6.5kV 2S-3C CSCPS topology opitimized for manufacturability and performance is proposed. Circuit simulations in LTSpice were performed using device models to estimate the static and dynamic performance of the CSCPS. The power switch is simulated to showcase improved switching and balancing performance over state-of-art solutions as summarized in Table 5.1.

Table 6.1: Switching time comparison between IGBTs, different SuperCascode Power Switch (SCPS) topologies and Cascaded SuperCascode Power Switch		
Design	Current t_r/t_f	Voltage t_r/t_f
Si IGBT	~400/5000	~400/500
Friedrichs SCPS	160/240	60/80
Kolar SCPS	161/41	31/182
X. Li SCPS	40/60	37/79
Gao SCPS	45/200	45/50
This work (CSCPS)	33/84	31/37

To fully utilize the benefits of the CSC switching topology and overcome the limitations of traditional HV power packaging a new "segmented baseplate" power packaging concept is proposed and developed. New processes and materials for fabricating the module were evaluated and tested. Epoxy resin substrates and dielectric coolant is discussed for future HV WBG power modules. A *6.5kV* CSCPS module is conceptualized and fabricated. A SolidWorks model is created prior to fabrication and simulated in COMSOL for estimating thermal performance. An Ansys Q3D analysis exctracts stray electrical parasitic elements and maps the E-field internal to the power module. A few demonstration modules are designed, fabricated and tested to prove the design concept. A series of static and dynamic tests were performed to characterize an open-cavity power module. The six JFET 6.5kV/105A 2S-3C CSCPS power module is fabricated and evaluated for thermal performance and evaluating the substrate voltage blocking capability. The 2S-3C CSCPS has an $R_{th,ja}$ of 2.61^0C/W with leakage less than 50nA at 6kV. Double-pulse testing (DPT) was performed to measure the turn-on and turn-off behaviors and calculate the losses.Switching at 4kV/50A the switch reported tr = 23 ns and tf = 50 ns for current and tr = 40 ns and tf = 55 ns for voltage. Results highlight the effectiveness of WBG-based Cascoded SuperCascodes for medium voltage fast transition switching.An example datasheet is provided of the final CSCPS.

This research advances the body of knowledge with the following additions,

1. Cascaded SuperCascode approach offers an opportunity to create low-cost High Voltage power switches beyond the present State of Art. The auxiliary balancing network which triggers serially connected depletion-mode devices is optimized to assure manufacturability and performance. The CSCPS switching topologies are a practical high-performance replacement of Si-IGBTs and SiC-MOSFETs.
2. New highly thermally conductive Epoxy Resin Composite Dielectrics (ERCDs) offer opportunities to create "segmented baseplate" modules and new electro-physical topologies. The ERCD materials are a low modulus (34 GPa), light-weight laminate (versus metal-clad ceramics) for high voltage (5kV/120μm), high temperature (≤300ºC) and high thermal impedance (10W/mK) packaging that can accommodate heavy metal interconnects at a higher reliability. Note: The 8W/mK @ 120 μm ERCD is the technical threshold to replace Al_2O_3 substrate at 381 μm.
3. A novel 2S-3C CSCPS segmented baseplate structure is proposed. The material and fabrication process is validated. The module is tested with its thermal and electrical functionality.

6.2. *Future work*

Based on the new Cascaded SuperCasscode switching topology introduced in this dissertation, future works in power semiconductor devices, the converter circuit topologies, and power conversion systems are possible.

1. Wirebondless double sided cooled power module

The ERCD can be used with new dielectric interface for double-sided power packaging. A complete virtual design of the proposed GaN HEMT module for demonstration is detailed in

Fig.1. The proposed module uses United SiC stacked die (Si-MOSFET on SiC JFET) and SiC JFET die mounts die drain down. To “planarize” the stacked die for mounting polymer silver can be used on drain pads to compensate for Si-MOSFET die thickness. The Ablestik ABP-8068T Series resin loaded Ag TSS does not flow out versus solder, provides low modulus stress and supports column formation at low sintering temperatures. To planarize the modules for single-step interconnection instead of wirebonding, an organic interposer hosting the pillars will be investigated to reduce manufacturing steps and reduce power path inductance. Exploration can also includes metal foam pillars for lower CTE and modulus.

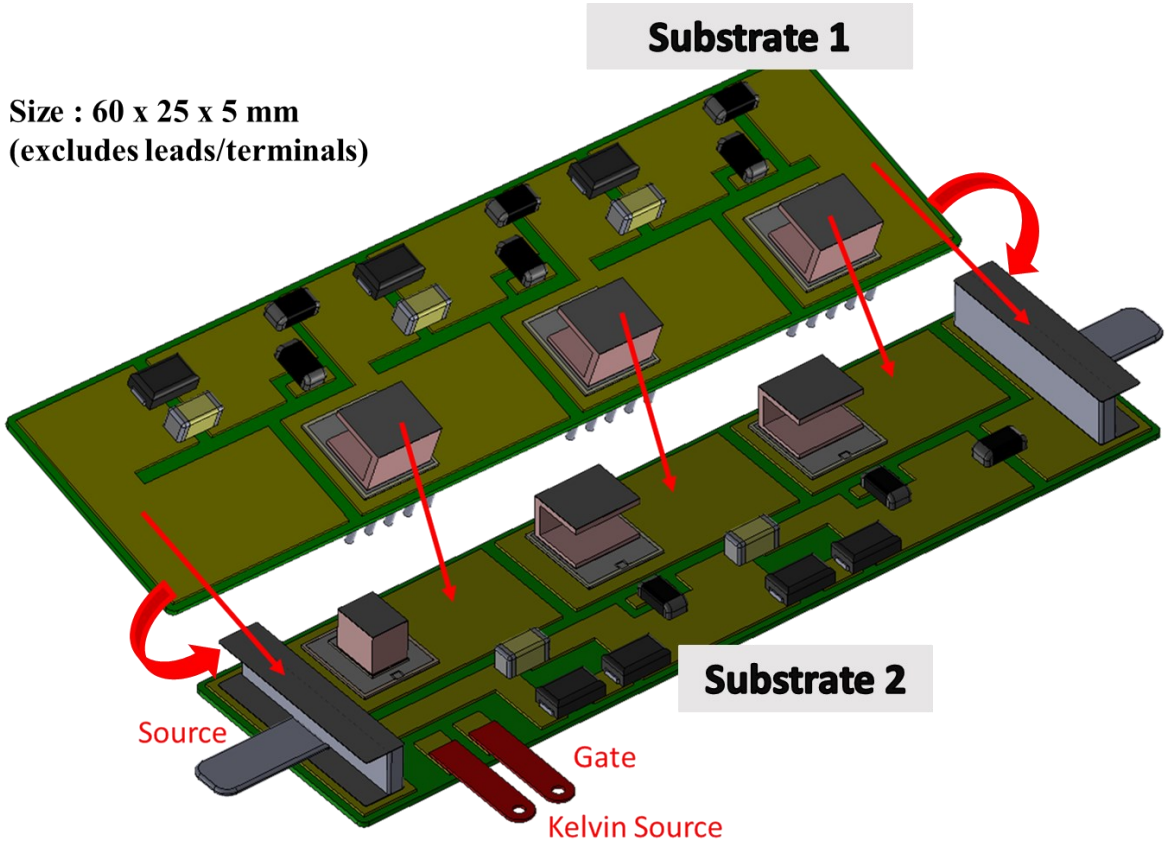


Fig. 6.1(a): Shown is a two substrate 6kV 2S-3C CSCPS module using one stacked Cascode (UnitedSiC – UF3S120009, five individual JFETs (UnitedSiC – UF3N120008) and auxillary balancing network components like resistors, capacitors and avalanche diode

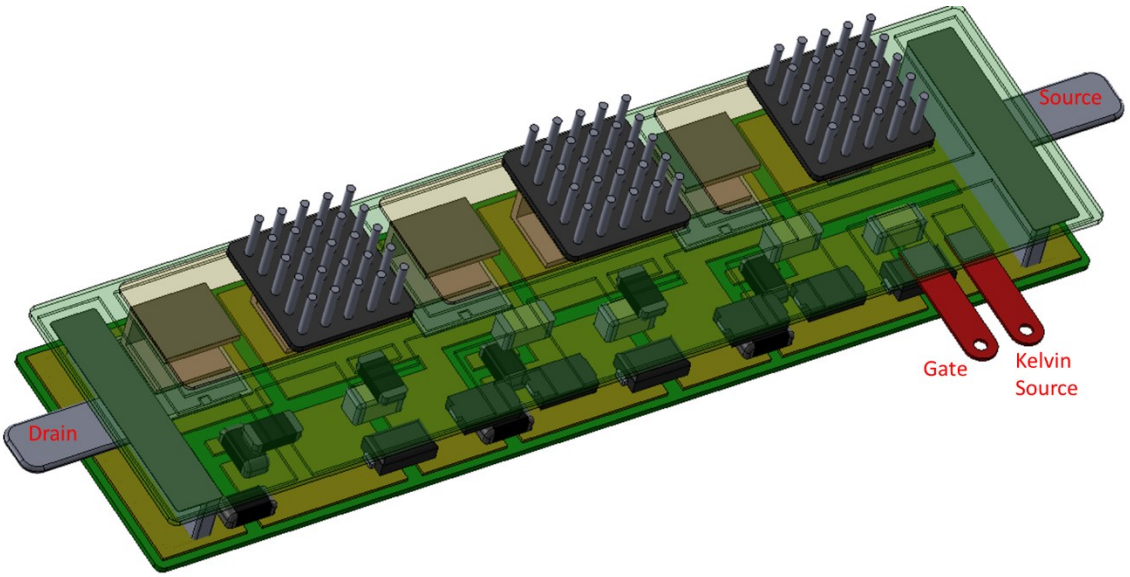


Fig. 6.1(b): 6kV 2S-3C CSCPS Wirebondless double sided cooled power module

The RISHO CC-7210N is Direct Bonded Copper (DBC) (Cu/ERCD/Cu at 100µm/120µm/100µm). The ERCD is rated for 40kV/mm, 10W/mK and Tg>300oC continuous. Through multiphysics simulation the substrates 1 and 2 have $R_{jc,S1}$ = 0.52 ºC/W & $R_{jc,S2}$= 0.72 ºC/W. An interposer will be explored to hold planarizing pillars and overall power module is epoxy encapsulated

2. *Extension of segmented baseplate power packaging*

The segmented baseplate approach can be applied with different organic substrates like polyimide (flex), FR4, etc, and can apply for the benefit in "all" high voltage power module applications. The technique of having a separate heatsink with dielectric fluid for each surface mount device can increase the power density of converters and power modules.

3. *GaN-based Cascaded SuperCascode*

The Cascading and scaling approach with the auxiliary balancing network can be extended and applied to any depletion mode power device. It can extend GaN-on-Silicon

technologies beyond 1 kV by connecting in series several depletion-mode GaN transistors (DHEMTs).

4. Application of HV Power and Aerospace

The CSCPS and the optimization approach discussed in this research is one of the only way for high voltage (HV) power to be established in aerospace and beyond. At high altitudes, the TCR (Cosmic Ray) effect on HV devices (>10kV) have caused randomly mis-trigger causing converter faults, solid-state breaker failures, critical load interruptions, etc. Research has reported that lowering the rated design voltage (V_{DS}) of SiC transistors reduces the effect.

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APPENDICES

APPENDIX A: 6kV CSCPS datasheet

CS65E2S12E2UM1

6.5 kV, 70 mΩ CSCFET

PREES Laboratory
NC STATE UNIVERSITY
POWER MODULES FOR DEVELOPMENT

2S-3C Cascaded SuperCascode FET

This SuperCascode FET is designed with six USCi UJN1202Z SiC JFETs and a USCi USM141A Si MOSFET in the PREES 2S-3C cascaded topology optimized for fast switching. The input is an N-Channel Trench Power MOSFET, rated 4.5 mΩ and 20V for easy gate drive applications.

Maximum Ratings (T_C = 25˚C unless otherwise specified)

Symbol	Parameter	Value	Unit	Test Conditions	Notes
V_{DSMAX}	Drain-Source Voltage	7.2	kV		
V_{GSMAX}	Gate-Source Voltage	-5/+20	V	Absolute Maximum values	
V_{GS}	Gate-Source Voltage	-5/+12	V	Recommended operational values	
I_D	Continous Drain Current	168	A	V_{GS} = 12 V, T_c = 25 ^{0}C, T_{Jmax} = 150^{0}C	
		117		V_{GS} = 12 V, T_c = 90 ^{0}C, T_{Jmax} = 150^{0}C	
$I_{D(pulse)}$	Pulse Drain Current	480	A	Pulse width t_p limited by $T_{j(max)}$	
T_{jmax}	Junction Temperature	-40 to 175	^{0}C		
T_{case}	Case Temperature	-40 to 150	^{0}C		
L_{stray}	Stray Inductance	28.3	nH	Measured between terminals 2 and 3	
P_D	Power Dissipation	1136	W	T_c = 25^{0}C, T_j=150^{0}C	

Electrical Characteristics (Tc=25^{0}C unless otherwise specified)

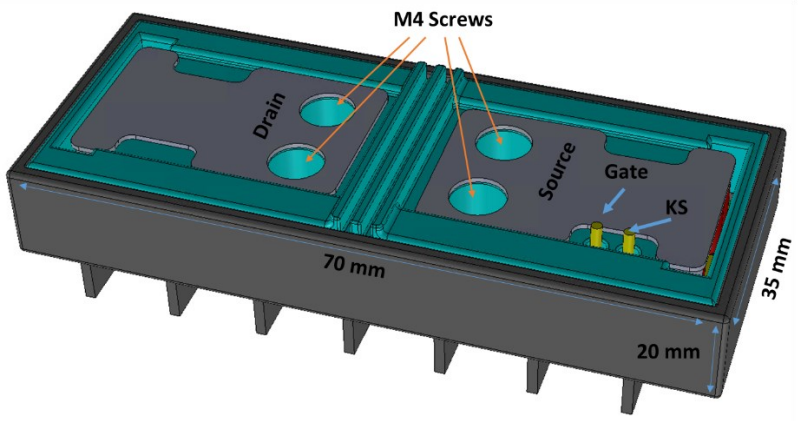
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions	Note
V_{DSS}	Drain-Source Blocking Voltage		6	7.2	kV	V_{gs}=-5V, I_D=2mA	
$V_{GS(th)}$	Gate Threshold Voltage	3.9	4.4	4.9	V	V_{ds}=V_{gs}, I_D=250µA	
I_{DSS}	Zero gate voltage drain current		TBD		µA		
I_{GSS}	Gate source leakage		TBD		µA		
$R_{DS(on)}$	On State Resistance		69.6	94.5	mΩ	V_{GS} = 12V, I_F = 50 A, T_J=	

						25^0C	
			196.5	198.3	mΩ	V_{GS} = 12V, I_F = 50 A, T_J= 125^0C	
G_{fs}	Transconductance		TBD				
C_{iss}	Input Capacitance		TBD				
C_{oss}	Output Capacitance		TBD				
E_{on}	Turn-on switching energy		2.24		mJ	V_{DS}=6 kV, I_D=50 A, V_{GS}=0/+12 V non-inductive load	
E_{off}	Turn-off switching energy		1.23		mJ		
E_{total}	Total switching energy		3.47		mJ		
$R_{G(int)}$	Internal Gate Resistance		1		Ω	V_{gs}=0V, f = 1 MHz	
Q_{gs}	Gate-Source Charge		13		nC	Testing Control MOSFET V_{DS} = 15V, I_D=20 A, V_{GS}=10V	
Q_{gd}	Gate-Drain Charge		12		nC		
Q_g	Total Gate Charge		36		nC		
$T_{d(on)}$	Turn-on delay time		TBD			V_{DS}=6 kV, I_D=50 A, V_{GS}=0/+12 V non-inductive load	
T_r	Rise time		11				
$T_{d(off)}$	Turn-off delay time		TBD				
T_f	Fall Time		60				
V_{SD}	Diode Forward Voltage		TBD				

Thermal Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition	Note
R_{thJCJ}	Thermal Resistance Junction-to-Case for JFET		0.11		^{0}C/W		
R_{thJCC}	Thermal Resistance Junction-to-Case for Cascode		0.13		^{0}C/W		

Package Dimensions



Note: Ver 0, June 2020, © NC State University

Appendix B: Matlab code to compare different Cascaded SuperCascode topologies

This program computes different possible arrangements to realize multi-layer Cascaded SuperCascodes for any *N* JFET string. It also computes its estimated balancing network gate charge and switching loss

```
%% Main Header
clc
clear
Qg=300e-9 ;                                  % Gate Charge of Device
Qd=0;                                        % Charge of the diode

%% Part 1 : Bo's SuperCascode switching topology
Vds = 1000;                                  % Drain to source voltage of JFETs(Allotted to
each device)
Vds_mod = 20000;                             % Drain to source voltage of module
N = Vds_mod/Vds;                             % Number of devices in series
Eb = (1/4)*(Qg-Qd)*Vds*(((N)^2)-(N));        % If we place 20 in series then Eb=0.0028 %
Switching energy loss

%% Initializing all energies to zero
Eb_tot=0;

%% The capacitor value for the balancing network
for i=1:1:N-1
   C(i)=(i*(Qg-Qd)*(1e12))/(Vds);            % This will be in pF
   CEb(i)=(1/2)*(C(i))*(Vds^2)/(1e12);
   Eb_tot=Eb_tot+CEb(i);                     % Total Energy
end


%% Part 2
% If we discuss a unit SCPM
% % SCPM-J with P stages per Unit SCPM and M Unit SCPMs per external cascode
div = divisors (N);
n = numel (div);                             % Number of elements in array, ie divisors

for i=1:1:n
  for i=1:1:n
N1(i)=div(n-i+1);                            % Stages of cascaded SCPM % (Internal)
N2(i)=div(i);                                % Stages in the unit SCPM % (External)
j=1:1:N1(i)-1
      C_N1_int(i,j)=(j*(Qg-Qd)*(1e12))/(Vds);
```

```
      CEb_N1_int(i,j)=(1/2)*(C_N1_int(i,j))*(Vds^2)/(1e12);
   for k=1:1:N2(i)-1
      C_N2_ext(i,k)=(k*(Qg-Qd)*(1e12))/(N1(i)*(Vds));
      CEb_N2_ext(i,k)=(1/2)*(C_N2_ext(i,k))*((N1(i)*Vds)^2)/(1e12);
   end
  end
end

%% Calculating string balancing network loss for CSCPS
E_tot_2Dnetwork(n)=0;
for a=1:1:n
  for b=1:1:N-1
    E_tot_2Dnetwork(a)=E_tot_2Dnetwork(a)+(N2(a)*CEb_N1_int(a,b))+CEb_N2_ext(a,b);
  end
end
for a=1:1:n
A=N1(a);
B=N2(a);
C=E_tot_2Dnetwork(a);
X=sprintf('%d per string and %d in cascade has %d mJ balancing network loss',A,B,C);
disp(X);
end


%% Calculating Cost Factor
C_N1_int_tot(n)=0;
C_N2_ext_tot(n)=0;
for a=1:1:n
   for b=1:1:N-1
      C_N1_int_tot(a)=C_N1_int_tot(a)+(N2(a)*C_N1_int(a,b));       % This will be in pF
      C_N2_ext_tot(a)=C_N2_ext_tot(a)+(C_N2_ext(a,b));             % This will be in pF
   end
end

CF = 0;                                                  % Initializing the cost factor to
zero
for a=1:1:n
CF(a)=((C_N1_int_tot(a)*Vds)+(C_N2_ext_tot(a)*Vds*N1(a)))*(10e9/10e12);    % Converting
units to nFV % This is representative of charge
end

for a=1:1:n
A=N1(a);
B=N2(a);
D=CF(a);
Z=sprintf('%d per string and %d in cascade has %d nFV cost factor',A,B,D);
```

```
disp(Z);
end

% %% Figure of merit
% FOM=0;
% for a=1:1:n
% FOM(a)=((E_tot_2Dnetwork(a))*1000)+(CF(a)*0.001);        % FOM is weighted and penalty
factors of Keb=1/mJ and Kcf=0.001 nFV
% end

function d = divisors (n)
%DIVISORS(N) Returns array of divisors of n
if ~isscalar(n)
   error('n must be a scalar');
end
if n < 1
   error('n must be positive integer');
end
if n == 1
   d = 1;
   return;
end
f = factor(n);
pf = unique(f);
for i = 1:length(pf)
   m(i) = sum(f == pf(i));
end
mi = zeros(size(m));
d = zeros(1,prod(m+1));
i = 1;
carry = 0;
while ~carry
   d(i) = prod(pf.^mi);
   i = i + 1;
   if mi(1) < m(1)
      mi(1) = mi(1) + 1;
   else
      mi(1) = 0;
      carry = 1;
   end
   for j = 2:length(m)
      if carry
         if mi(j) < m(j)
            mi(j) = mi(j) + 1;
            carry = 0;
         else
```

```
            mi(j) = 0;
            carry = 1;
        end
    end
  end
end
d = sort(d);
end
```

Appendix C: Gate Driver Specification and Design

An optically isolated gate driver is designed and fabricated, shown in Fig. C-1. The gate driver insertion inductance is minimized and the overall gate drive circuitry measures *17 mm* X *12 mm*.

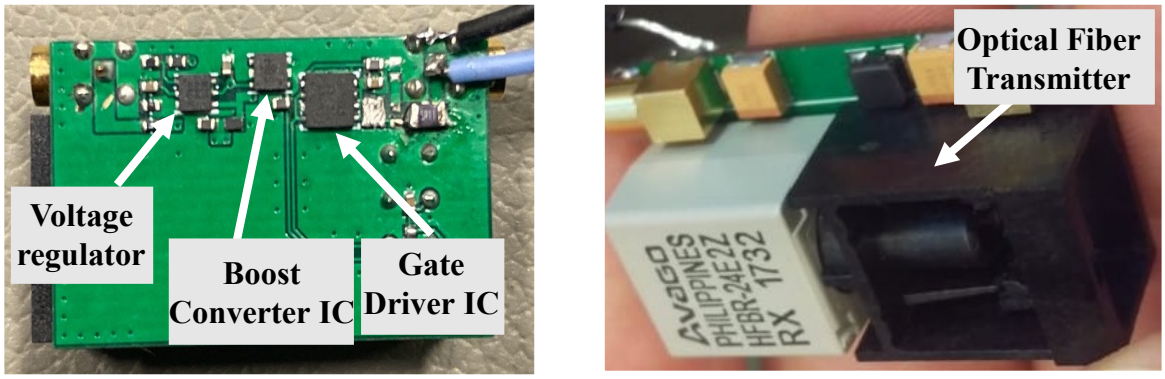


Fig. C-1: HV Optically isolated Gate Driver (17 X 12 mm) (L) Bottom Side PCB (R) Top Side PCB

The gate driver utilizes a DC/DC 6kV isolated converter (MORNSUN G_S-2WR2), and a fiberoptic cable for signal isolation. The driver has an onboard voltage regulator, boost converter and dual-channel gate drive. The voltage regulator steps down *9V* to *5V* which is used to enable the boost converter and gate driver IC. The boost converter steps provide the drain-source voltage swing and can be adjusted using the R_5:R_6 ratio, equation C-1. To drive the CSCPM a gate-to-source voltage of *0-12V* is required, so R_5:R_6 = *91kΩ:10kΩ*. A *10 Ω* gate resistor is used and both the channels of the gate driver are connected to limit the gate current to *1.2 A*. The final gate driver schematic, PCB layout and fabricated boards are shown in Fig C-2, Fig C-3 and Fig C-4 respectively.

$$V_{out} = 1.229 * \left(\frac{R_5}{R_6} + 1\right) \qquad (C-1)$$

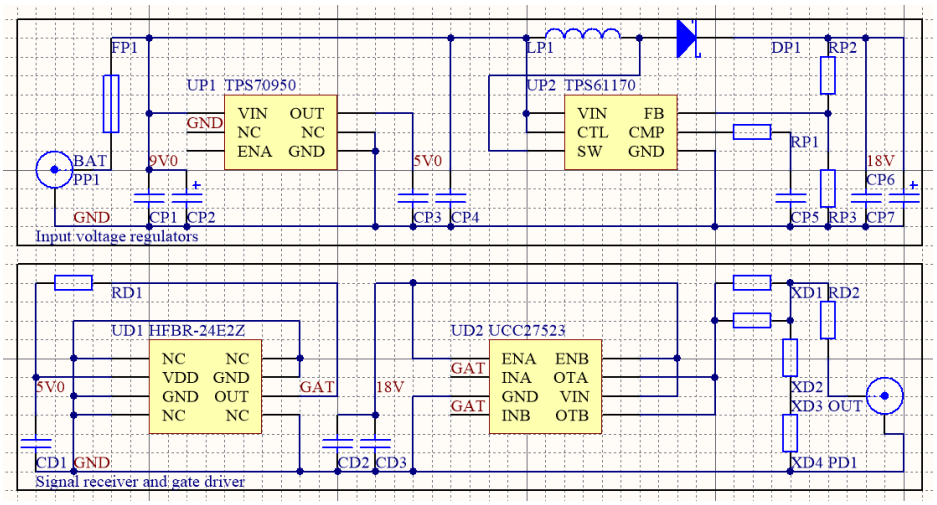


Fig. C-2: Final gate drive schematic

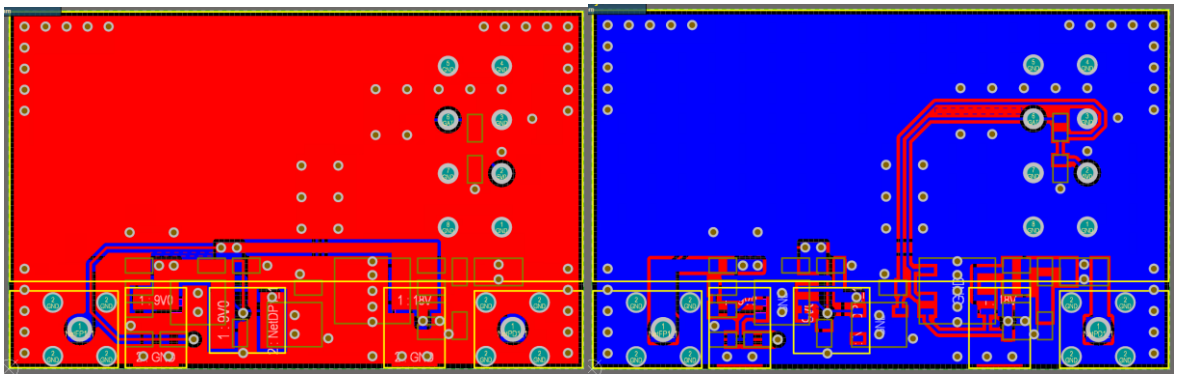


Fig. C-3: Top layer (L) and bottom layer (R) PCB layout

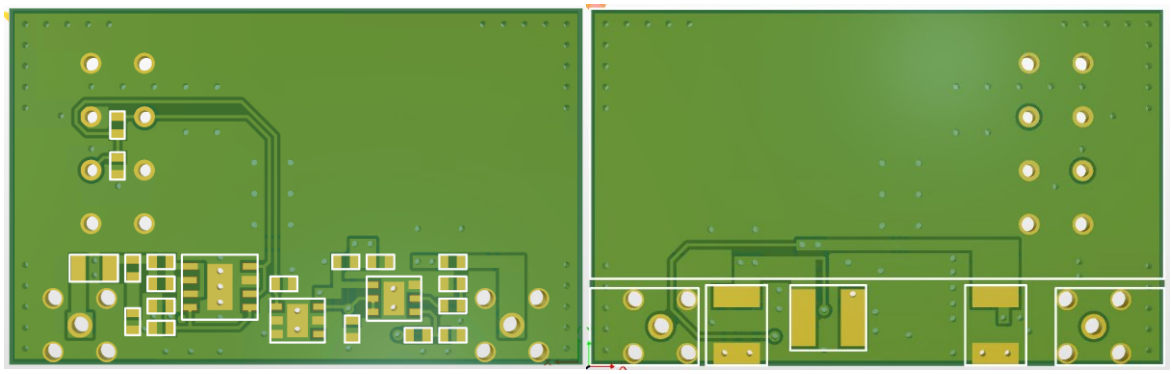


Fig. C-4: 2D rendering of the gate driver (L) Top View (R) Bottom View

APPENDIX D: STEP-BY-STEP VISUALIZATION OF THE 24kV HV-CSCPM

CSCPM on ERCD substrate layout of Power Devices, Passive balancing network, and Dynamic balancing network

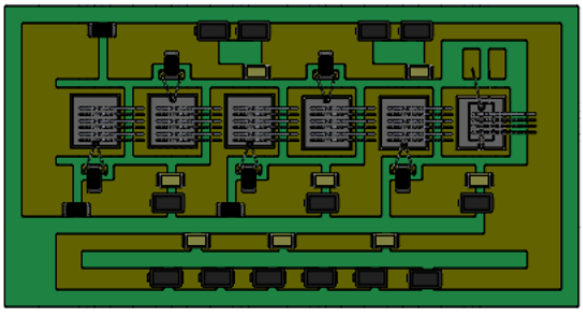


Fig D-1. 2S-3C Control CSCPM with 6 JFETs and stacked trigger MOSFET with balancing network (Layout 1)

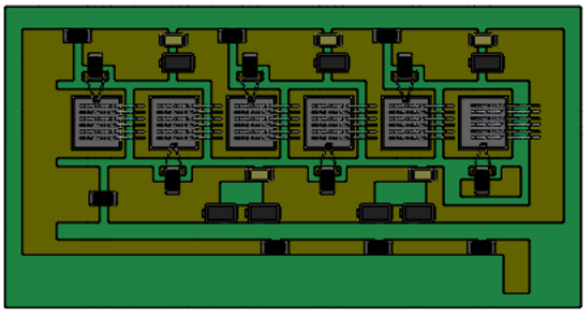


Fig D-2. 2S-3C CSCPM with 6 JFETs and balancing network (Layout 2)

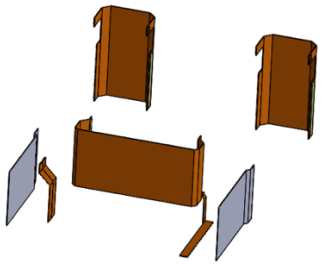


Fig D-3. Flex circuit forming interconnect

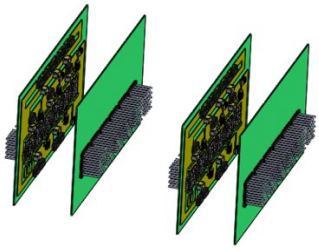


Fig D-4. ERCD substrates showing segmented backside heat sinks

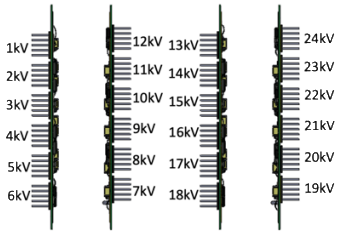


Fig D-5. Four serial CSCPMs to form the 24kV HV-CSCPM

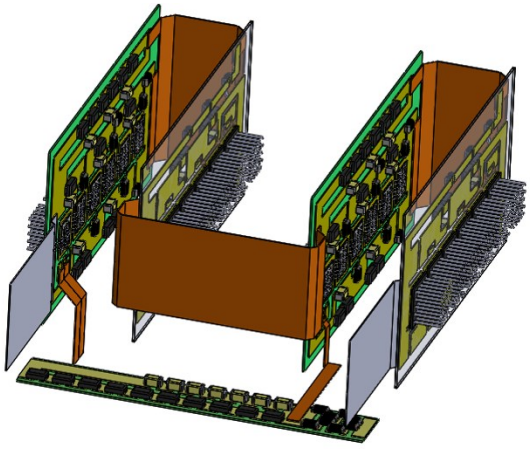


Fig D-6. Visualization of assembled boards w/o housing

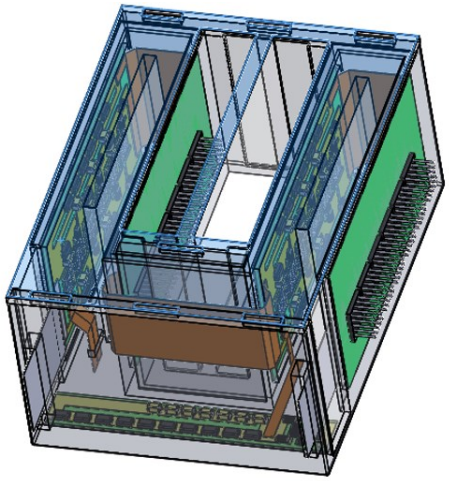


Fig D-7. Graphic adding housing

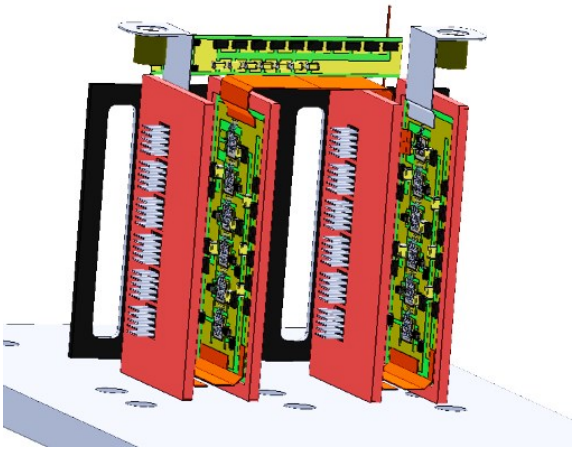


Fig D-8. Rotated boards show orientation to the bottom support structure.

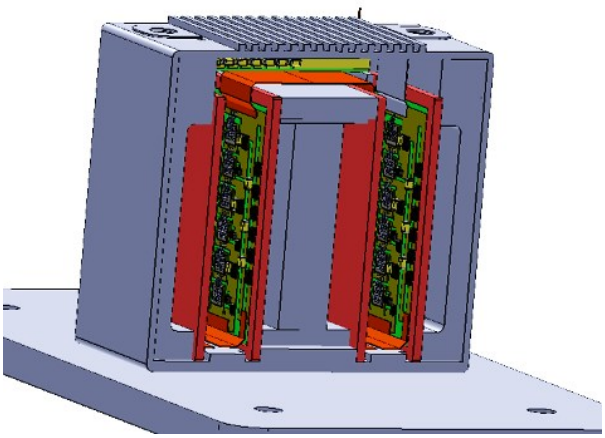


Fig D-9. The added housing shows the boards and fluid flow channels across the heat sinks

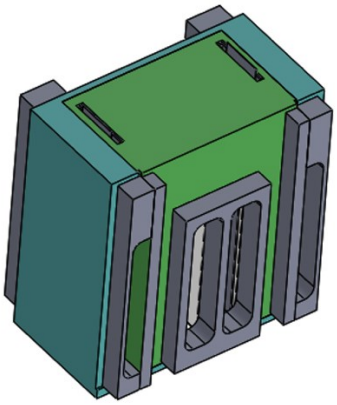


Fig D-10. Housing showing fluid ports (gasketing not shown)

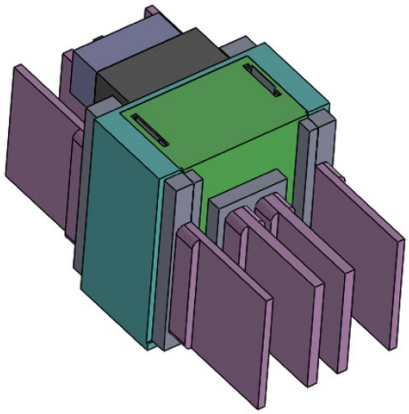


Fig D-11. Purple fins represent the cooling tubes

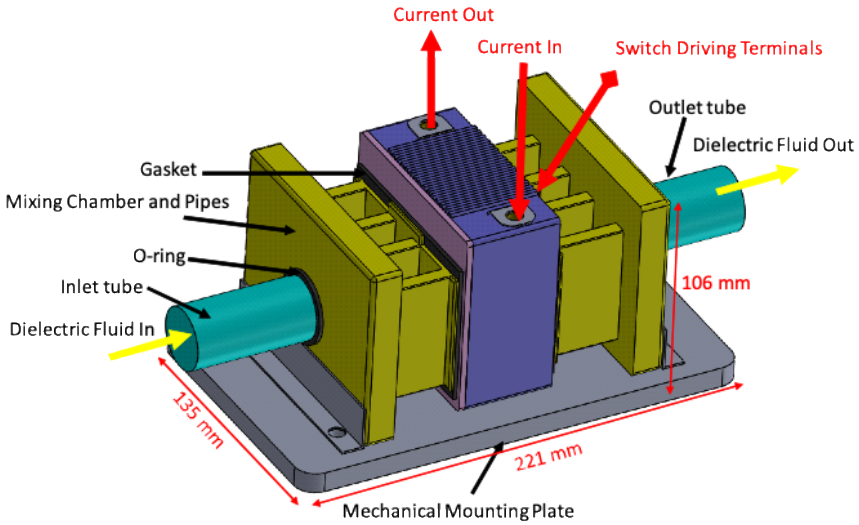


Fig D-12. Entire HV-CSCPM as a 24kV power switch.

Appendix E: Fabrication

The ERCD board top layer and bottom layer layout Alitum design is shown in Fig. E-1 and Fig. E-2.

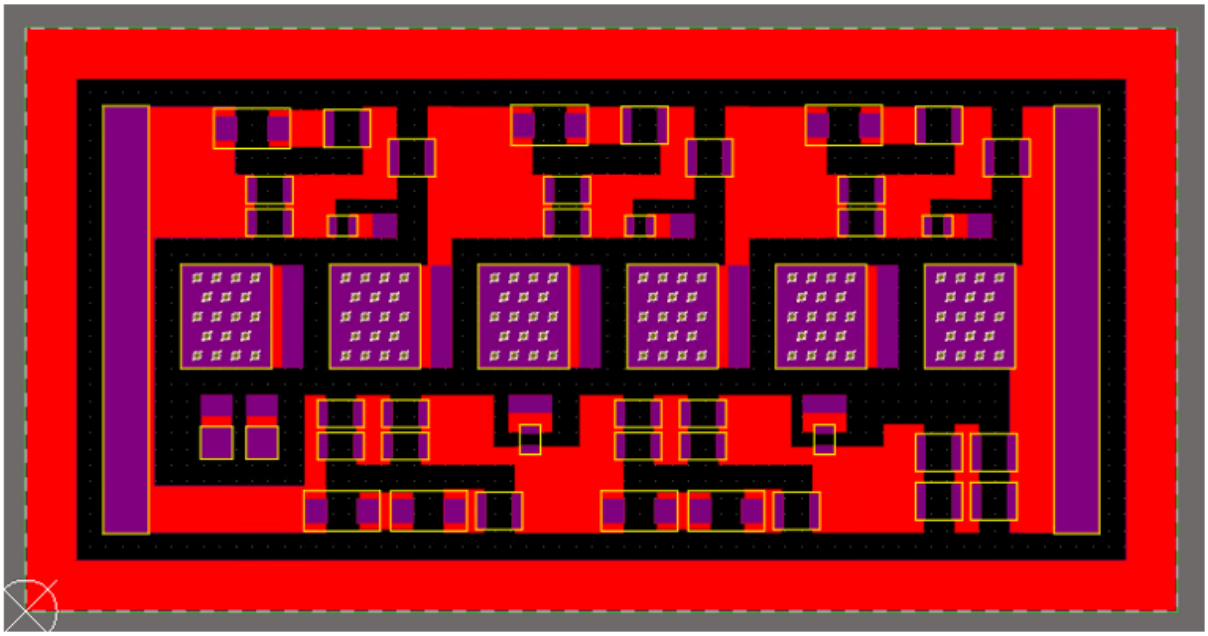


Fig. E-1: Top layer PCB design (Red: Copper masked, Purple: Exposed copper or Wire bondable area, Black: ERCD, Yellow: Solder Stops)

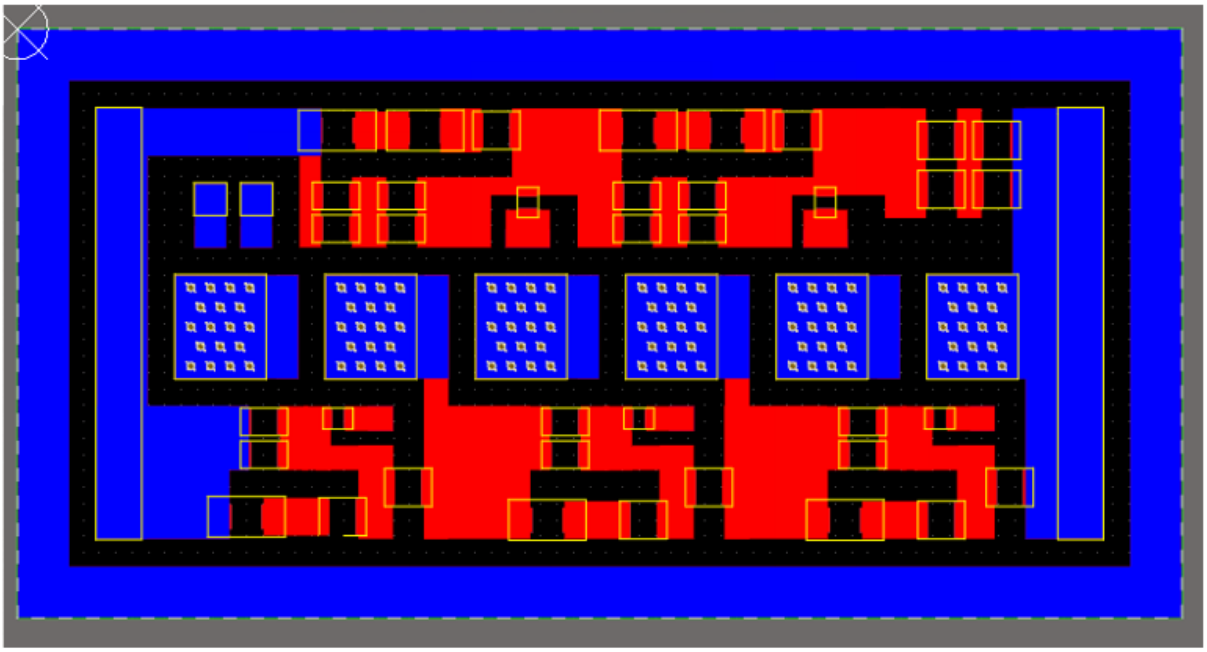


Fig. E-2: Bottom layer ERCD design (Blue: Copper masked, Purple: Exposed copper or Wirebondable area, Black: ERCD, Yellow : Solder Stops)

The SolidWorks CAD Models of the Housing and Lid design are shown in Fig. E-3 to E-8.

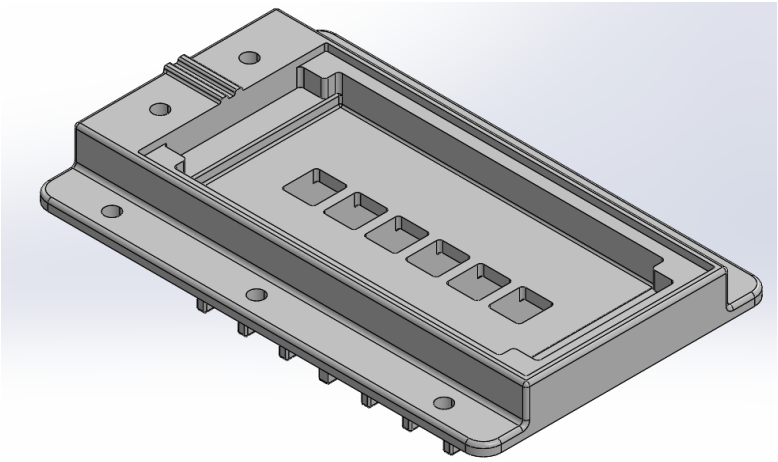


Fig. E-3: Isometric view of housing body

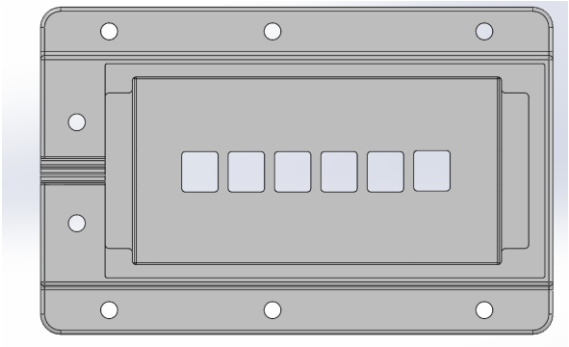


Fig. E-4: Top view of housing body

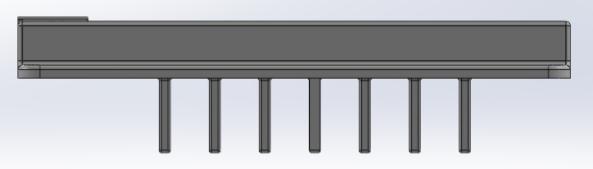


Fig. E-5: Side view of housing body

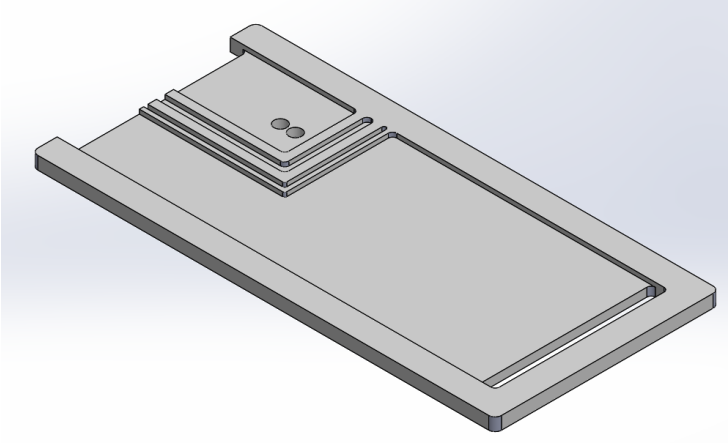


Fig. E-6: Isometric view of housing lid

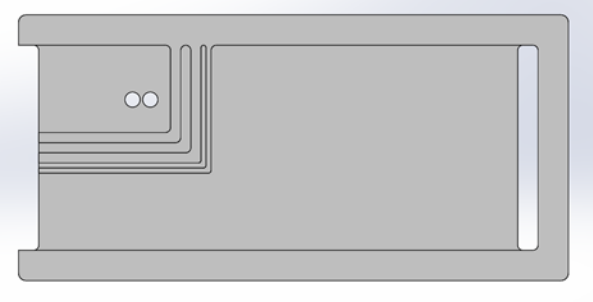


Fig. E-7: Top view of housing lid

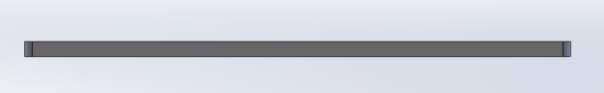


Fig. E-8: Side view of housing lid

2.1 Fabrication of 2S-3C Cascaded SuperCascode Power Switch (CSCPS)

This section describes the assembly process in fabricating the 2S-3C Cascaded SuperCascode Power module described above. The material list for the module is given in Table E.1 and shown in Fig. E-9 to E-12

Table E.1: 6.5kV/50A 2S-3C CSCPS module material list

Component	Material
Substrate	200/360/200 μm Cu/ERCD/Cu
SiC JFET Cascode	UnitedSiC – UF3S120009
SiC JFET	UnitedSiC – UF3N120008
Power device attach	Sn 5/Pb 95 83% T3 solder
Heat sink attach	Sn 63/Pb 37 85% T4 solder
Heat sink	Cool Innovations - 4-02027U
Power terminals	Customized with 0.75 mm thick Cu

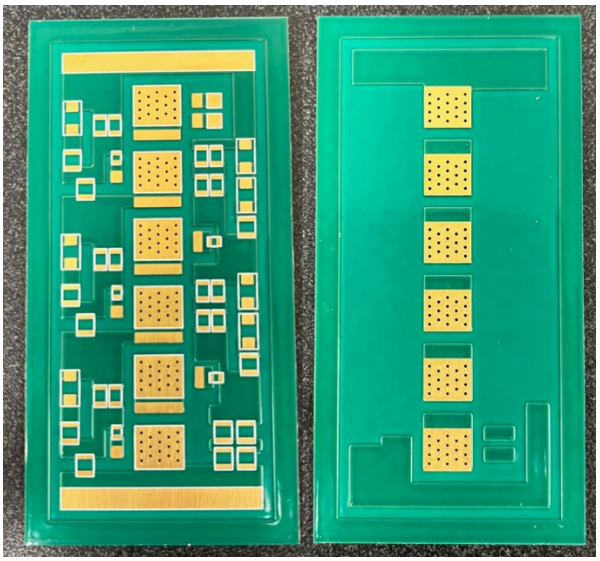


Fig. E-9: Top view of ERCD substrate

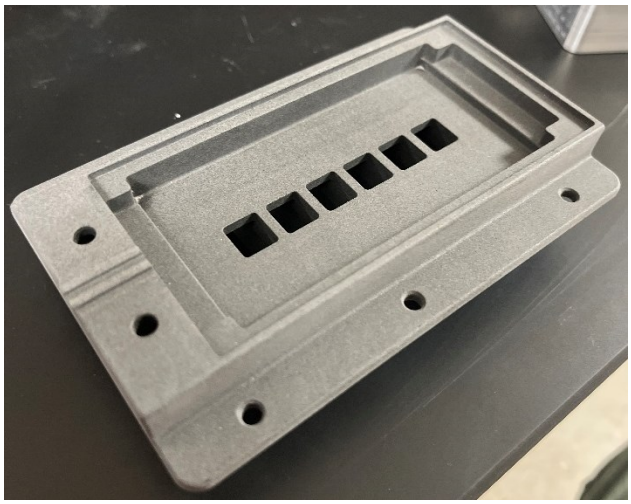


Fig. E-10: Isometric view of housing body

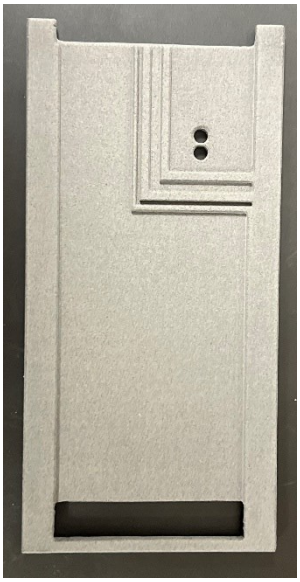


Fig. E-11: Top view of housing lid showing

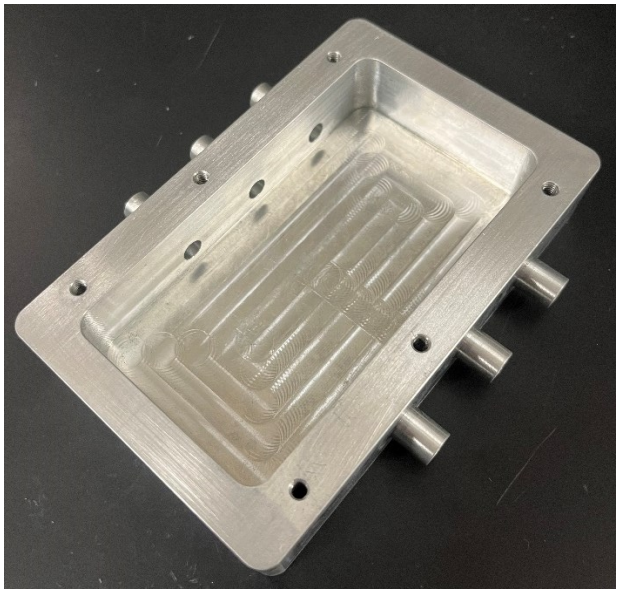


Fig. E-12: Isometric view of cooling chamber

A 200/360/200 µm ERCD substrate procurred from Brigitflex was selected for the power module. The exposed copper was electroless nickel-gold (ENIG) plated for better soldering and bonding performance. All non soldered and bondable area was solder masked (green) for

constraining the power, active and passive devices during reflow and for providing voltage isolation. The housing body was made with delerin for its ability to handle high continuous temperature and was CNC fabricated by PCBWAY, China. The overall dimensions of the power module is 127 x 81 x 12 mm. The power module package assembly steps is shown in Fig. E-13.

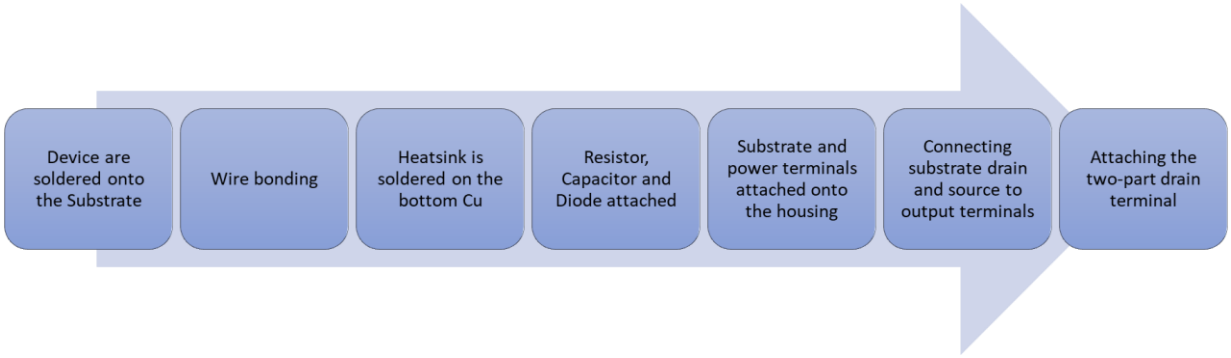


Fig. E-13: Fabrication process flow

First, all the power devices are attached with Sb5/Sn95 83% T3 solder dispensed in a cross pattern for 2.4 sec at 25psi and then reflowed in a Sikama Five stage reflow-oven. The temperature profile is 120/205/272/130 C wherein each zone is 3 mins 50 seconds, shown in Fig. E-14 calibrated for the substrate and thermal mass. The gates of the JFET and Cascode, gate of 1st JFET and source of MOSFET and kelvin connection from the MOSFET are wire bonded with a Hesse-Mechatronics BJ939 using 5 mil Al wire. The source of the JFETs are wire bonded to the adjacent JFET drain using 8 mil Al wire, wherein 10 wirebonds are parallelled and triple stick bonded per die to reduce contact resistance. All bond profiles were calibrated to form a low bonding profile (less than 2 mm) to meet the clearance standard IEC 60664-1 for a pollution level 2.

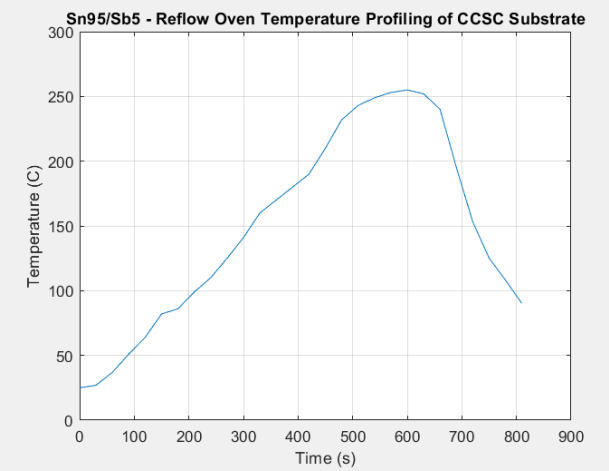


Fig. E-14: Reflow oven temperature profile for Sn95/Sb5 solder

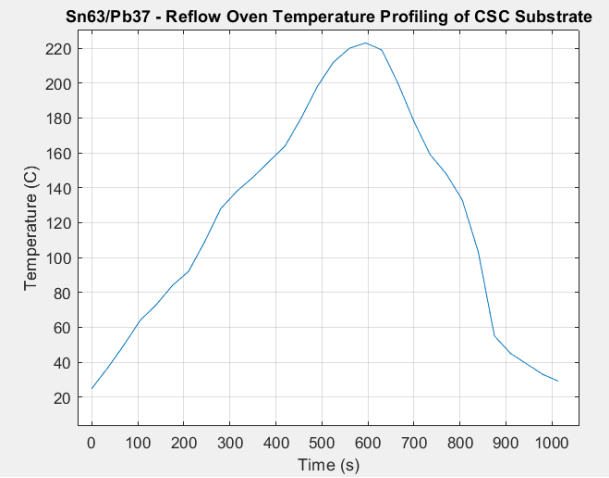


Fig. E-15: Reflow oven profile for Sn63/Pb37 solder

Next, the heat sink is attached to the bottom Cu using a solder hierachy. The heatsink is attached using Sn63/Pb37 85% T4 solder dispensed in a cross pattern for 2.5 sec at 25 psi and reflowed through the Sikama Five stage reflow-oven with a temperature profile is 120/195/240/150 C wherein each zone is 4 mins 15 sec, shown in Fig. E-15. Then the substrate and power terminals are attached onto the housing body with LOCTITE HY 4090 GY from Henkel. The copper strips are hand soldered to interconnect the substrate to the power terminals. Next, all other passive and active components including the resistors, capacitors and diodes are soldered onto the substrate.

Passivation, electrical isolation and encapsulation are provided by Risho High thermal conductivity encapsulation.The two part copper drain terminal is now solder attacher together completing the circuitry. Some fabrication photo's are shown in Fig. E-16 to Fig. E-21.

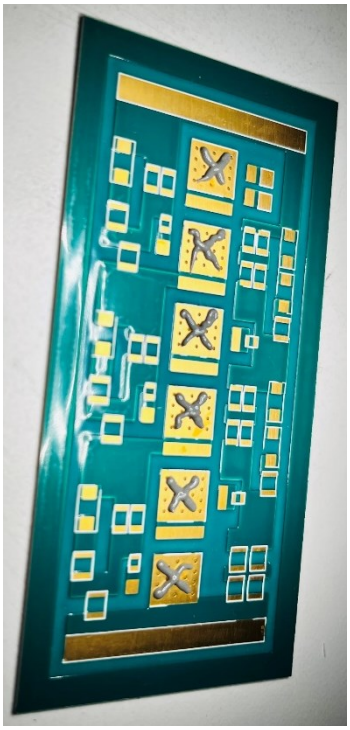


Fig. E-16: Solder dispense

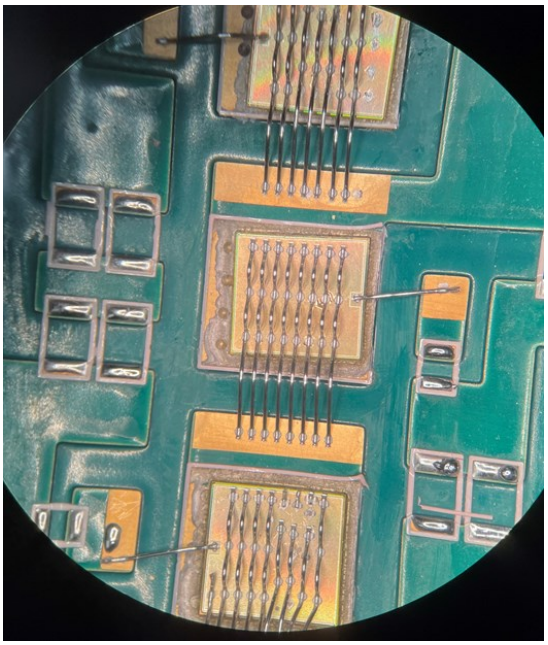


Fig. E-17: Wirebonding

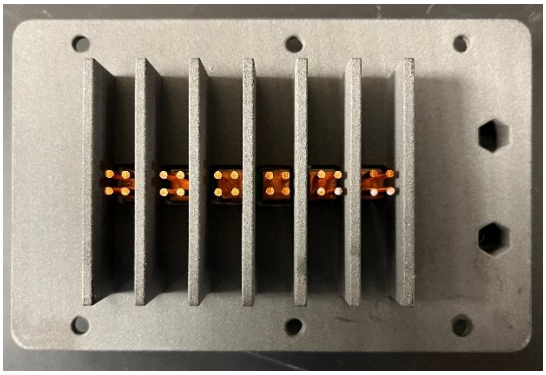


Fig. E-18: Bottom view of the power module (bottom view of module)

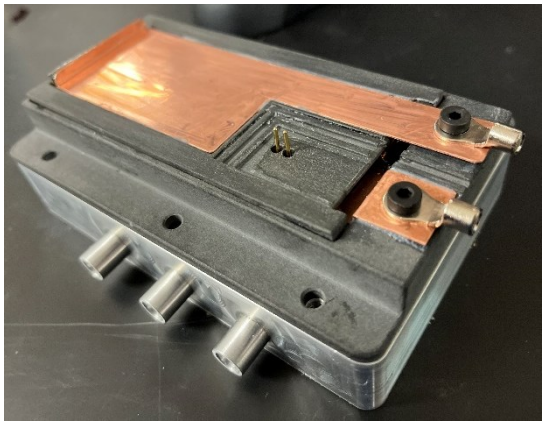


Fig. E-19: Overall power module

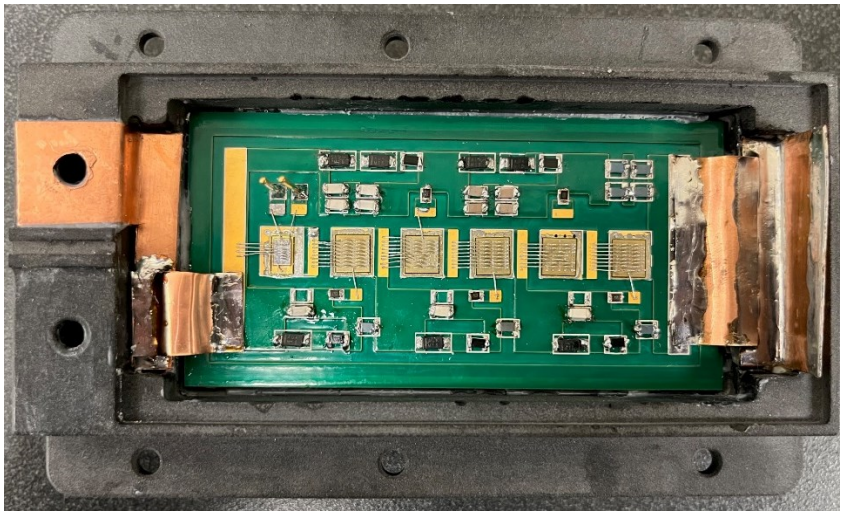
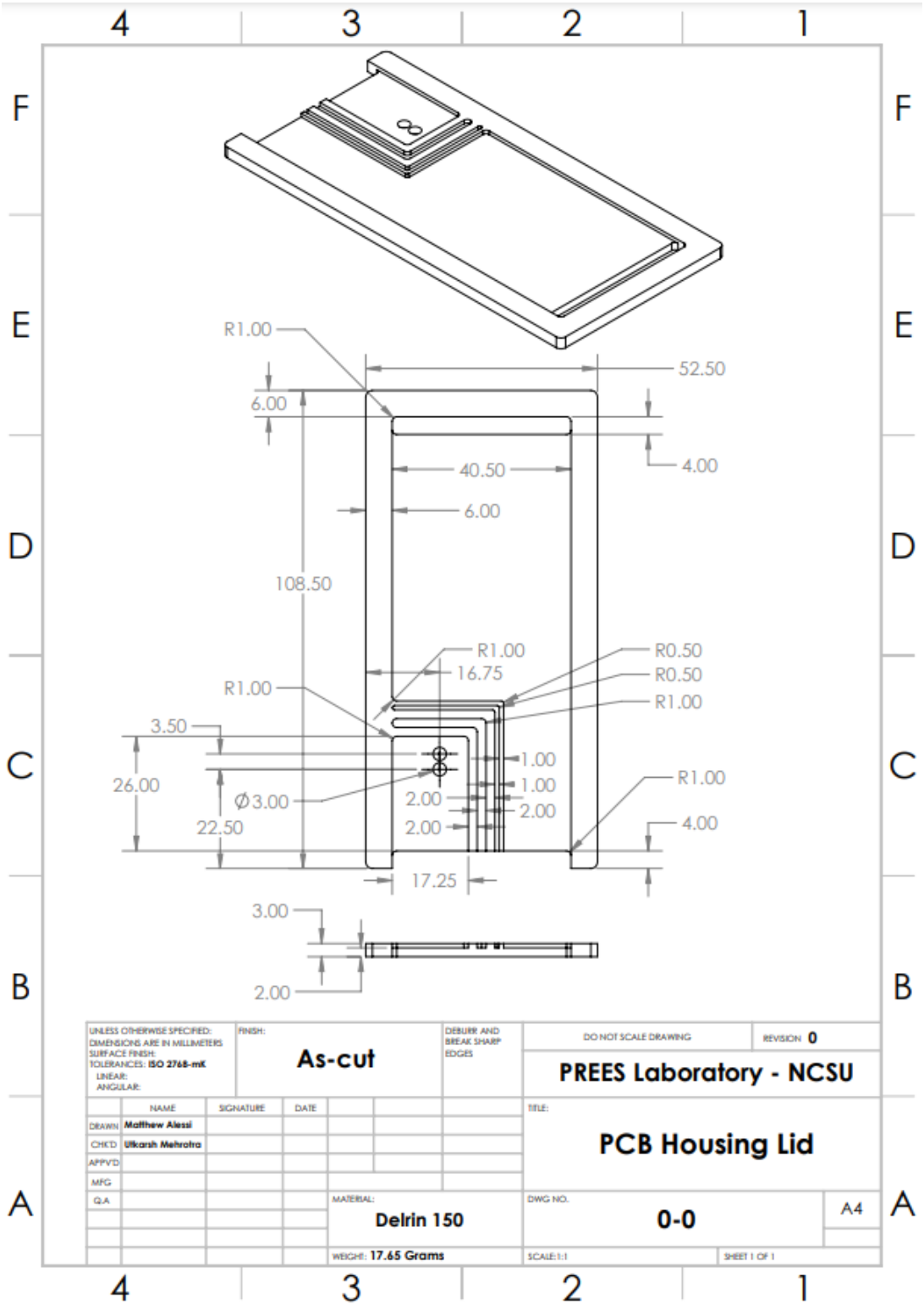
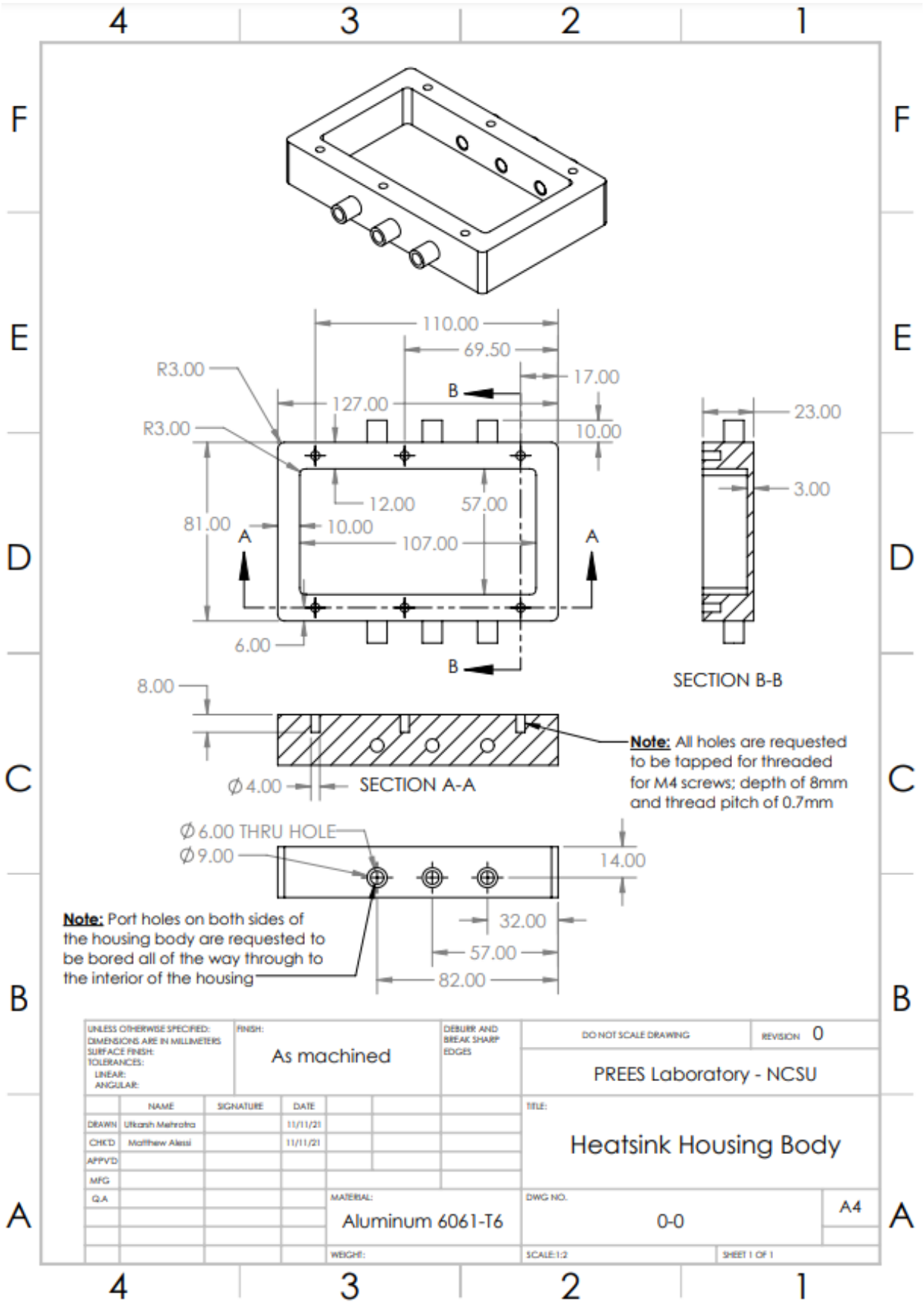
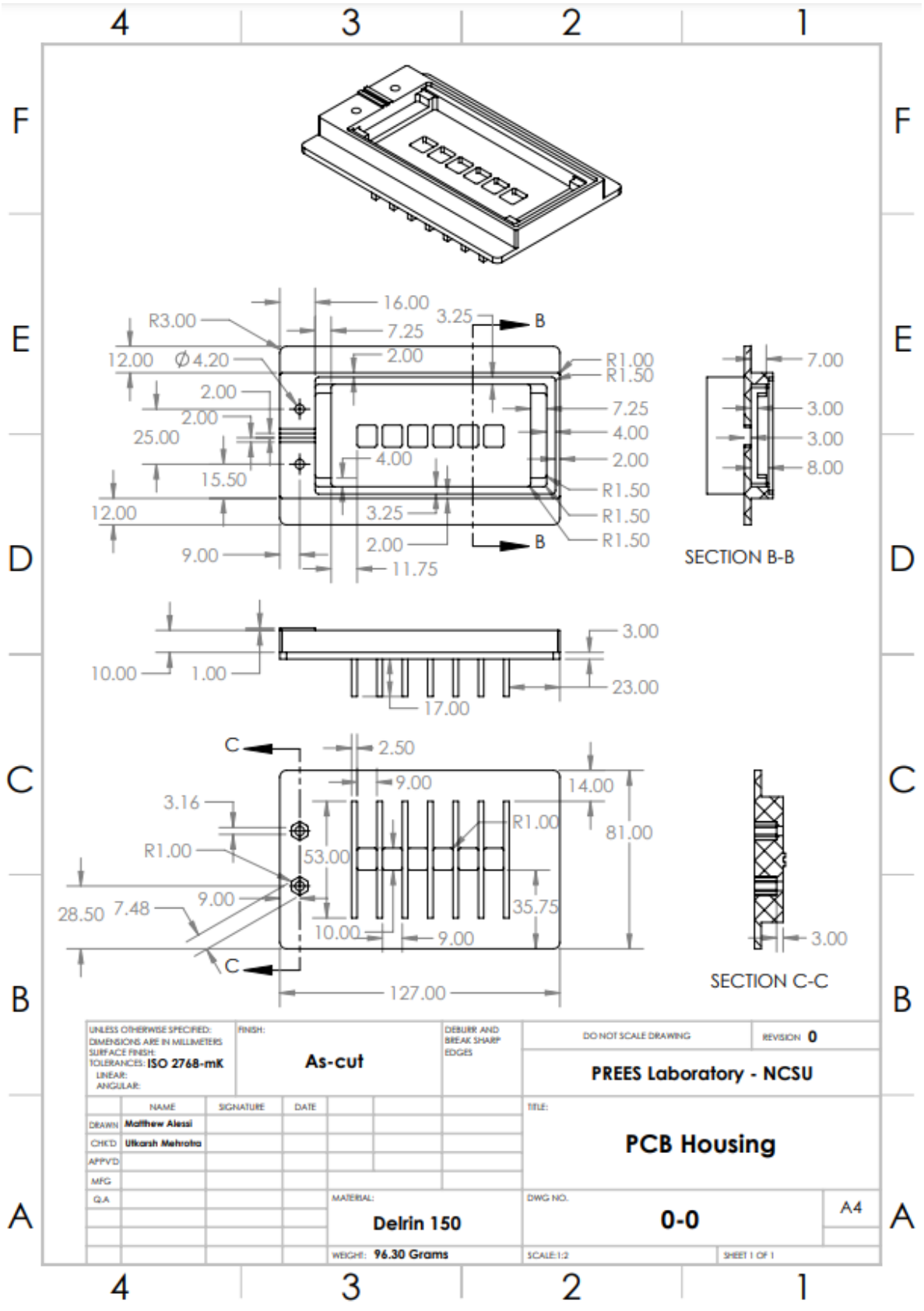


Fig. E-20: Populated open cavity 2S-3C CSCPM

Appendix F: CAD Drawing of power module




4
3
2
1
F
E
D
C
B
A
110.00
69.50
17.00
R3.00
127.00
B
R3.00
10.00
23.00
12.00
57.00
3.00
81.00
A
10.00
107.00
A
6.00
B
SECTION B-B
8.00
Note: All holes are requested to be tapped for threaded for M4 screws; depth of 8mm and thread pitch of 0.7mm
Ø4.00
SECTION A-A
Ø6.00 THRU HOLE
Ø9.00
14.00
32.00
57.00
82.00
Note: Port holes on both sides of the housing body are requested to be bored all of the way through to the interior of the housing
UNLESS OTHERWISE SPECIFIED:
DIMENSIONS ARE IN MILLIMETERS
SURFACE FINISH:
TOLERANCES:
LINEAR:
ANGULAR:
FINISH:
As machined
DEBURR AND BREAK SHARP EDGES
DO NOT SCALE DRAWING
REVISION 0
PREES Laboratory - NCSU
NAME
SIGNATURE
DATE
DRAWN
Utkarsh Mehrotra
11/11/21
CHK'D
Matthew Alessi
11/11/21
APPV'D
MFG
Q.A
TITLE:
Heatsink Housing Body
MATERIAL:
Aluminum 6061-T6
DWG NO.
0-0
A4
WEIGHT:
SCALE:1:2
SHEET 1 OF 1


4
3
2
1
F
E
D
C
B
A
16.00
7.25
3.25
B
R3.00
12.00
Ø4.20
2.00
2.00
25.00
15.50
12.00
9.00
4.00
3.25
2.00
11.75
R1.00
R1.50
7.25
4.00
2.00
R1.50
R1.50
R1.50
7.00
3.00
3.00
8.00
SECTION B-B
10.00
1.00
3.00
23.00
17.00
C
2.50
9.00
14.00
3.16
R1.00
81.00
R1.00
53.00
28.50
7.48
9.00
35.75
10.00
9.00
127.00
3.00
SECTION C-C
UNLESS OTHERWISE SPECIFIED:
DIMENSIONS ARE IN MILLIMETERS
SURFACE FINISH:
TOLERANCES: ISO 2768-mK
LINEAR:
ANGULAR:
FINISH:
As-cut
DEBURR AND BREAK SHARP EDGES
DO NOT SCALE DRAWING
REVISION 0
PREES Laboratory - NCSU
NAME
SIGNATURE
DATE
DRAWN Matthew Alessi
CHK'D Utkarsh Mehrotra
APPV'D
MFG
Q.A
TITLE:
PCB Housing
MATERIAL:
Delrin 150
DWG NO.
0-0
A4
WEIGHT: 96.30 Grams
SCALE:1:2
SHEET 1 OF 1

Appendix G: DPT Test code

The DPT controller was implemented with a PSoC 5LP MCU. To protect the operater, the DPT sequence is implemented througj USB communication and can be isolated with USB or wireless network. The system diagram consists of two major parts: USB communication and trigger button interface. The USB communication part exposes a USB serial port which can be accessed by the host computer through PuTTY (baud rate = 9600) or any serial port console. The source code for the main program is :

```
*/
#include "project.h"
#include "stdio.h"

#if defined (__GNUC__)
    /* Add an explicit reference to the floating point printf library */
    /* to allow usage of the floating point conversion specifiers. */
    /* This is not linked in by default with the newlib-nano library. */
    asm (".global _printf_float");
#endif

#define USBFS_DEVICE

/* The buffer size is equal to the maximum packet size of the IN and OUT bulk
* endpoints.
*/
#define USBUART_BUFFER_SIZE (64u)
#define LINE_STR_LENGTH     (20u)

char8* parity[] = {"None", "Odd", "Even", "Mark", "Space"};
char8* stop[]   = {"1", "1.5", "2"};

int main()
{
    int rxbuflen;
    int rxlen=0;
    int txlen;
    int i;
    char rxbuf[64];
    char rxstr[64];
```

```
char txbuf[64];
int crlf=0;
int value1, value2;
int pwmstart=0;
CyGlobalIntEnable;
/* Start USBFS operation with 5-V operation. */ /*This cannot operate at 3 V, 3.3 V or 5 V*/
  USBUART_Start(0,USBUART_5V_OPERATION); /*USBFS_DEVICE*/
    for(;;)
{
   /* Host can send double SET_INTERFACE request. */
   if (0u != USBUART_IsConfigurationChanged())
   {
      /* Initialize IN endpoints when device is configured. */
      if (0u != USBUART_GetConfiguration())
      {
         /* Enumeration is done, enable OUT endpoint to receive data
          * from host. */
         USBUART_CDC_Init();
      }
   }
   //
   if(!USBUART_GetConfiguration())
   {
      //Flush buffers
      rxbuflen=0;
      rxlen=0;
      txlen=0;
      crlf=0;
      continue;
   }
   //
   if(USBUART_DataIsReady())
   {
      //Read all data from buffer
      rxbuflen=USBUART_GetAll((uint8_t*)rxbuf);
      for(i=0;i<rxbuflen;i++)
      {
         //Find end of line
         if(rxbuf[i]=='\r' || rxbuf[i]=='\n')
         {
            //Do not respond to multiple CRLFs
            if(!crlf)
            {

               //Parse string
               rxstr[rxlen]='\0';
```

```
                if(strncmp(rxstr, "start", sizeof("start")-1)==0)
                {
                   PWM_Start();
                   LED_Write(1);
                   pwmstart=1;
                }
                if(strncmp(rxstr, "stop", sizeof("stop")-1)==0)
                {
                   PWM_Stop();
                   LED_Write(0);
                   pwmstart=0;
                }
                if(strncmp(rxstr, "set", sizeof("set")-1)==0)
                   if(sscanf(rxstr, "set %d %d", &value1, &value2)==1)
                      if(value1<=499 && value1>=49 && value2<=(value1>>2))
//Clock=50MHz, 49=500kHz, 499=50kHz, DT<=25%
                         if(pwmstart)
                         {
                            PWM_Stop();
                            PWM_WritePeriod(value1);
                            PWM_WriteCompare1(value1>>1);
                            PWM_WriteCompare2(value1>>1);
                            PWM_WriteDeadTime(value2);
                            PWM_Start();
                         }
                if(strncmp(rxstr, "status", sizeof("status"))-1==0)
                {
                   txlen=snprintf(txbuf, 64, "VIN %d, IIN %d, VOUT %d\r\n", 100, 200, 300);
                   USBUART_PutData((uint8_t*)txbuf, txlen);
                   if(txlen==64) USBUART_PutData(NULL, 0);
                }
                //Next command
                rxlen=0;
                crlf=1;
             }
          }
          else
          {
             //Add incoming character to string
             if(rxbuf[i]==0x08) //Backspace
                rxlen=rxlen>0?rxlen-1:0;
             else if(rxlen<63) //Buffer overrun protection
             {
                rxstr[rxlen++]=rxbuf[i];
                crlf=0;
             }
```

```
            }
        }
    }
    /*
    if (0u != USBUART_GetConfiguration())
    {
        if (0u != USBUART_DataIsReady())
        {
            count = USBUART_GetAll(buffer);

            if (0u != count)
            {
                while (0u == USBUART_CDCIsReady())
                {
                }

                USBUART_PutData(buffer, count);

                if (USBUART_BUFFER_SIZE == count)
                {
                    while (0u == USBUART_CDCIsReady())
                    {
                    }

                    USBUART_PutData(NULL, 0u);
                }
            }
        }
    }*/
  }
}
/* [] END OF FILE */
```