Propagation of High Speed
Digital Signals in Printed
Circuit Board Systems - Phase II

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C. Heyward Riedell and Glen Stewart

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August 23, 1988

CCSP-TR-22
Abstract

This technical report is a report on the second phase of a project entitled *Propagation of High Speed Digital Signals in Printed Circuit Board Systems* funded by Bell Northern Research as an enhancement project within the Center for Communications and Signal Processing in the Electrical and Computer Engineering Department at North Carolina State University. The report covers period July 1 1987 to June 30 1988. This phase was concerned with development of measurement techniques, design of test printed circuit boards, and development of a preliminary transmission line simulator program and associated circuit theory.
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NOTE: Sections are separated by colored paper.
INTRODUCTION

This is a report on an investigative project looking at digital signal propagation in systems incorporating printed circuit boards (PCBs). The project is concerned with reflection, cross-talk, and ground and supply noise phenomena in digital systems. In systems with digital devices that respond to fast rise- and fall-time signals, these phenomena can result in false responses and in some cases can render a system unusable. The project is concerned with establishing criteria, that minimize and control these effects, for the design of printed circuit boards and thus developing computer aided design tools to augment existing tools for their automated design.

The project is in three phases with the work progressing from literature and product review to development and integration of a computer aided design tool. Phase I lasted six months and involved a detailed literature and product search with the aims of identifying the problems to be addressed, those products which would assist in this program, requirements for integrating the results of this study with existing circuit board design systems, and outlining a work plan for the last two phases of the project. The second phase, reported on here, lasted one year and was concerned with development of measurement techniques, design of test printed circuit boards, and development of a preliminary transmission line simulator program and associated circuit theory.

The report is in two parts. The first documents the project review presented at Bell Northern Research, Research Triangle Park, in June 1988. The second part contains formal documents prepared during the project.
PART 1

PROJECT REVIEW PRESENTATIONS
OBJECTIVES OF THE PROJECT REVIEW

1) Explain BNRRTP's program
2) Determine areas of synergy
3) Commitment for collaboration

GOALS

1.1) Information Dump
1.2) Demo of Tool
2.1) Round Table Discussion
MANAGING TRANSMISSION LINE EFFECTS

1) Definition of the program

1.1 Objectives
1.2 Organization
1.3 Overview

2) Justification of work

3) Outline of basic approach
MANAGING TRANSMISSION LINE EFFECTS IN INTERCONNECT MEDIUMS

PROGRAM OBJECTIVE

Manage transmission line effects in interconnection media.

FOCUS ON: Board-to-board
           Chip-to-chip
DESIGN AND ANALYSIS OF PRINTED CIRCUIT BOARDS FOR HIGH SPEED PULSE PROPAGATION

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Research Triangle Park

Member of the Field Theory Committee of the Microwave Theory and Techniques Society of IEEE — Responsible for monitoring work on device-field interactions on Printed Circuit Boards.
Co-organizer of workshop on printed circuit board simulation, Microwave Theory and Techniques Symposium — June 1989, California.
OUTLINE

1. Issues being Addressed

2. Approach

3. Philosophy of Approach

4. Measurement Background

5. Alternative Approaches
Emphasis has been on development of a Post Layout Simulator

• As this is much cheaper and faster than building and debugging a prototype, and

• Because it is unlikely that a complete set of design guidelines could be developed or implemented.

We are beginning to address the development of design guidelines

• By formulating design practices currently being used

• Investigating the trade-off of PCB real estate (e.g. using extra buffers) and minimization of adverse transmission line effects.
ISSUES BEING ADDRESSED:

1. Design Guidelines (Real Pomerleau, Michael Steer, Dan Winklestein)

2. Macromodeling of Digital Devices (Cliff Barfield)

3. Analytic/Empirical Models (Glen Stewart)

4. Dielectric Measurement (Heyward Riedell)

5. Microwave Measurement (Jeff Kasten, Michael Kay)

6. Scaling and Table Look-up Techniques (so that field theoretic and measured results can be used in the simulator) (Mark Basel, Nan Liu)

7. Coupling (Michael Riddle, Ramin Nobaht)

8. Programming (Joseph Hall, Sasan Ardalan)
APPROACH ...

1. THE WORK IS AIMED AT THE EFFICIENT AND RELIABLE DESIGN OF HIGH SPEED PRINTED CIRCUIT BOARDS THROUGH

- Development of Design Guidelines
- Development of Post Layout Simulator

2. RELYING ON DESIGN GUIDELINES ALONE RESULTS IN A FAR TOO CONSERVATIVE A DESIGN. DESIGN GUIDELINES NEED TO CHANGE WITH DIFFERENT DIGITAL TECHNOLOGIES. THEY ARE LIKELY TO BE VERY DIFFICULT TO EXPRESS WHEN MIXED TECHNOLOGIES (E.G. TTL AND CMOS, TTL AND SURFACE MOUNT) ARE USED.

3. RELYING ON POST LAYOUT SIMULATION ALONE RESULTS IN TOO LONG A DESIGN CYCLE. HOWEVER THE POST LAYOUT SIMULATOR ENABLES THE PERFORMANCE OF THE BOARD WITH DIFFERENT TECHNOLOGIES TO BE INVESTIGATED.
4. SIMULATION CAN BE USED IN THREE WAYS

(a) AS AN AID IN DEVELOPMENT OF DESIGN GUIDELINES
    (QUICKEST DESIGN CYCLE)

(b) AS POST LAYOUT SIMULATOR TO FLAG PROBLEM AREAS
    (INTERMEDIATE DESIGN CYCLE)

(c) AS A CONCURRENT SIMULATOR AIDING A LAYOUT TOOL.
    (SLOWEST DESIGN CYCLE)

WE ARE FOCUSING ON POST LAYOUT SIMULATION AND DEVELOPMENT OF DESIGN GUIDELINES.
PHILOSOPHY OF APPROACH

1. Development of Simulator Core (CAPNET)
   Efficient Recursive Approach
   Signal Processing (e.g. eye diagrams).

2. Development of Analytic/Empirical Models and Table Based Models
   The tables could be developed from measurement or field theory analysis. We are emphasizing measurements.


4. Material Investigation
   — can we reduce our problems by using different materials and fabrication technologies.

5. Keep all of the investigations modular so that they can contribute to other efforts.
MEASUREMENT BACKGROUND

1. Analytic models do not match measurement results.

2. Effect of manufacturing variations can be significant with PCB’s.

3. These manufacturing variations are captured in measurements and incorporated in a simulation through table look-up techniques.

4. It would be difficult to model these manufacturing variations analytically.

Consider the following measured results and comparisons with calculations based on analytic models.
ALTERNATIVE APPROACH (1)

PRE-PROCESSOR
Express Models in S parameter Tables
Construct input to SUPERCOMPACT

SUPERCOMPACT

POST-PROCESSOR
Interpret Data Generated

1. ViABLE Approach
2. USEFUL FOR DEVELOPING Design Guidelines
3. NOT SUITABLE FOR USE AS POST LAYOUT SIMULATOR BECAUSE IT IS SLOW.
4. MOST MODELS FOR PCB structures ARE NOT AVAILABLE AND MUST BE EXTERNALLY GENERATED. HOWEVER MOST OF THE WORK IN THIS PROJECT CAN BE USED TOWARDS THIS APPROACH.
5. NONLINEAR analysis MUST BE HANDLED BY POST PROCESSOR
6. NOT Interactive.
ALTERNATIVE APPROACH (2)

TRANIENT SIMULATOR
WITH MODELS FOR PCB STRUCTURES
AND NONLINEAR ANALYSIS ROUTINES

1. Viable Approach

2. Useful for developing Design Guidelines and Post Lay-out Simulator.

3. Most of what we are doing could be used in such a simulator.

4. Suited to circuit level simulation.
Figure 1: Test setup for printed circuit board measurements, (a) test structure showing reference planes, (b) detail of adaptor mounting, and (c) detail of electrical contact to ground plane of printed circuit board.
8 mil Line on Solid Ground Plane

SET 3 5.13.87

EEsof - Touchstone - 01/04/80 - 16:13:10 - PCBC

CALCULATED

MEASURED
8 mil Line on Solid Ground Plane

SET 3 5.13.87
CHARACTERISTIC IMPEDENCE OF MICROSTRIP LINES

$Z_0$ (Ω) vs. WIDTH OF LINES (Ω)

- X: calculated
- ●: measured - solid ground plane
- □: measured - lattice
Printed Circuit Board Measurement Techniques

Jeffery S. Kasten
Master's Candidate
at
North Carolina State University

- Research Objectives
- Introduction to Measurement Techniques
- Concerns Unique to PCB Measurements
- New Two-Port Error Correction Techniques
- Conclusion
Goal:

To provide new error correction techniques that address the problems encountered with PCB transmission line measurements.

Objectives:

1. Focus on Two-Port error correction techniques.
2. Extend to Four-Port.
3. Extend to N-Port.
Introduction to Measurement Techniques

Why do we need PCB transmission line measurements?

- Provide data for simulators (empirical models)
- Verification of analytic models

Via

Bend

Tee

Coupling

etc.
Measurement System:

Measurements are done with a Vector Network Analyzer.

Structures are inserted in a fixture

Accurate measurements require some form of calibration.
Calibration: Removal of measurement errors.

Two-Tier process

1. Removal of system errors (coaxial)
2. Removal of fixture errors (microstrip)

De-embedding: Determination and removal of the fixture error.

- Apply coaxial techniques to microstrip i.e. Open-Short-Load (OSL)
- Use existing microstrip techniques i.e. Through-Short-Delay (TSD) Line-Reflect-Line (LRL)
- Develop new de-embedding techniques

WHY?
PCB Concerns

PCB De-embedding Standards

- Lack precision
- Need to be easily manufactured

PCB fixtures may not support conventional standards.
New Two-Port De-embedding Techniques

Three levels of fixture complexity

- Asymmetric
- Symmetric
- Identical

These are extendable to four-port and in general N-port extension will happen in the very near future.
Conclusion

PCB measurement techniques are a necessary part of any transmission line research.

This material has been accepted for presentation at RF Expo 88 East this fall.

The extention of the two-port results to four-port will give the most accurate measurements of PCB coupling to date.
Figure 6. Comparison of DUT scattering parameters with fixtures, DUT de-embedded using TSF, and direct VANA measurement.
Calculated $\text{Mag}[S_{21}]$ vs. Measured

Calculated $\text{Mag}[S_{11}]$ & $\text{Mag}[S_{22}]$ vs. Meas
MEASURING THE DIELECTRIC CONSTANT
OF PC BOARD LAMINATES

- Goals and Objectives

- Dielectric Measurement Techniques

- Preliminary Results

- Future Work
GOAL

The goal of this research is to expand the current understanding of PC Board laminates to improve the design process and the quality of the finished product.

OBJECTIVES

– Survey the current techniques of measuring the dielectric constant.

– Choose those methods applicable to PC Boards.

– Investigate dielectric variation due to
  1) anisotropic behavior
  2) frequency
  3) temperature

– Determine design sensitivity to variations in the dielectric constant.
A SURVEY OF TECHNIQUES

The various dielectric measurement techniques can be divided into four major categories:

1) Resonance
2) Reflection/Transmission
3) Time Domain Reflectometry
4) Length Comparison

RESONANCE

These techniques utilize the physical dimensions and measured resonant frequency to determine the complex permittivity. The best structures appear to be the metal-clad laminate and strip resonators.
REFLECTION/TRANSMISSION

These techniques require the insertion of a dielectric sample in the path of an electromagnetic wave propagating down a transmission line. The measured reflection (transmission) coefficients are used to obtain permittivity information. Difficulties encountered are sample preparation and frequent adjustment during testing.
TIME DOMAIN REFLECTOMETRY

Two types of TDR have been reported for determining the complex permittivity of dielectric materials. The first case uses only reflections from the front surface of a sample. The more complex case utilizes total reflection from the sample. The permittivity is found by converting the time domain signals to the frequency domain reflection coefficient and performing numerical analysis.
LENGTH COMPARISON

This method compares the difference in the physical length two strip transmission lines and the difference in the electrical length to determine the dielectric constant. The difference in two lines is suggested to remove the effect of connections to and from the test line. A single line can be used, if connector effect can be removed by other methods. One drawback of the method is the fact that the loss tangent cannot be determined.
**MANAGING TRANSMISSION LINE EFFECTS IN INTERCONNECT MEDIUMS**

**DIELECTRIC CONSTANT ($\varepsilon_r'$) vs. FREQUENCY AND TEMPERATURE**

E-GLASS REINFORCED EPOXY (G-12FR) LAMINATE (54 wt.% RESIN)

<table>
<thead>
<tr>
<th>FREQUENCY (MHz)</th>
<th>$\varepsilon_r'$</th>
<th>$\varepsilon_r''$</th>
<th>loss tan</th>
</tr>
</thead>
<tbody>
<tr>
<td>474.50</td>
<td>4.186</td>
<td>0.203</td>
<td>0.047</td>
</tr>
<tr>
<td>950.50</td>
<td>4.273</td>
<td>0.175</td>
<td>0.041</td>
</tr>
<tr>
<td>1432.50</td>
<td>4.233</td>
<td>0.168</td>
<td>0.040</td>
</tr>
<tr>
<td>2393.50</td>
<td>4.212</td>
<td>0.151</td>
<td>0.031</td>
</tr>
</tbody>
</table>

**STRIPLINE**
SUMMARY

COMPLETED

- Survey of measurement techniques (report available).
- Preliminary testing of resonant techniques.

CURRENTLY

- Improving accuracy of resonant technique.
- Reviewing alternate techniques.

PROJECTED

- Develop permittivity data base both as a function of frequency and temperature.
- Materials to be tested
  - FR-4
  - Cyanate Ester
  - MBT
  - Gore/FR-4
  - Gore/Cyanate Ester
- Investigate pulse propagation sensitivity to variation.
Cliff Barfield

BNR First Term Co-op

EE Masters Candidate at N.C. State University

Project Involvement: Macromodeling Digital Devices
MACROMODELING DIGITAL DEVICES

OUTLINE:

1) Objectives and Procedure

2) Discussion of Literature Review Report

3) Macromodel Example

4) Developing Macromodels from Measurement Techniques

5) Future Work
MACROMODELING DIGITAL DEVICES

Objectives:

1) Develop a complete macromodel for various digital devices. The macromodel should model the input and output characteristics as well as the internal characteristics of the device.

2) Develop a database library of the macromodels.

3) Incorporate the library of macromodels into a transmission line simulator.

Procedure:

1) Literature search and review.

2) Propose macromodel for device.

3) Conduct preliminary testing to ensure model validity.

4) Design test board to test devices.

5) Conduct measurements to develop macromodel of the device.

6) Verify macromodel with lab measurements.

7) Set up database library of device models.

8) Incorporate library of device models into simulator TRANSIM or SCAMPER.
MACROMODELING DIGITAL DEVICES

Literature review report:

1) General
   a) Definition
   b) Macromodel types

2) Macromodel Examples
   a) NAND gate
   b) Flip-flop

3) Developing Macromodels of Digital Devices
   a) Objectives
   b) Measurement techniques
      i) One-port models > input and output characteristics
      ii) Two-port models > internal characteristics

4) Extended Bibliography

NAND Gate Macromodel Example (Glesner):

Input stage:
   i) input characteristics

Middle stage:
   i) logic operation
      ii) transition times

Output stage:
   i) propagation delay
      ii) output characteristics

Figure 1.1: Two input TTL NAND gate macromodel
MACROMODELING DIGITAL DEVICES

Developing Macromodels from Measurement Techniques

1) One-port Measurements
   a) Macromodels presented in Figure 1.2.
   b) Measurement techniques:
      i) Nonlinear resistance from I-V curves.
      ii) Inductance and nonlinear capacitance from S-parameter measurements.
      iii) Current source from initial state of device.

   ![One-port macromodels of digital devices](image)

   a) Input characteristics                               b) Output characteristics

   Figure 1.2: One-port macromodels of digital devices

2) Two-port Measurements
   a) Capture internal characteristics of device.
      i) Logic operation
      ii) Transition times
      iii) Propagation delays
   b) Methods:
      i) Measurement techniques
         * Incorporate unit loads.
         * Use S-parameter measurements of device to determine internal characteristics.
         * Vary unit loads to determine if the input and output are coupled.
      ii) Use a technique similar to Glesner's NAND gate example.

   ![Two-port measurements of digital device](image)

   Figure 1.3: Two-port measurements of digital device
MACROMODELING DIGITAL DEVICES

Future Work:

1) Develop one-port models of devices.

2) Consider two-port models - preliminary testing.

3) Incorporate one-port models into transmission line simulators, such as TRANSIM and SCAMPER.

4) Eventually develop two-port models for use in transmission line simulators. Provide waveform analysis of entire circuit.

Figure 1.4: Example of digital circuit
Dan Winkelstein  
Bell Northern Research  
MSS Hardware Design

Presently responsible for:

- Developing a technique for simulating complex coupled transmission lines terminated with non-linear loads
- Developing a library of measure Scattering parameter for sub-structures of printed circuit boards
- Assist in efforts to develop macromodels of common digital devices
OUTLINE

• OBJECTIVES

• GENERAL METHOD FOR SOLVING COMPLEX COUPLED TRANSMISSION LINES TERMINATED WITH DIGITAL DEVICES

• RESULTS

• EXPERIMENTAL VERIFICATION

• LIBRARY OF SCATTERING PARAMETERS FOR PCB SUB-STRUCTURES

• FUTURE

• SPECIFICS ON TECHNIQUE
SIMULATION OF COMPLEX COUPLED TRANSMISSION LINE SYSTEMS WITH NON-LINEAR DIGITAL DEVICE TERMINATION

OBJECTIVES

1) Develop a numerical technique to solve for the transmission line effects of lossy/dispersive coupled transmission lines with discontinuities and terminated with digital devices.

2) Develop a library of measured Scattering Parameters for various PCB sub-structures.

3) Develop large signal macromodels for digital devices.

4) Prove a region of numerical convergence exists for an arbitrary systems of transmission lines terminated with digital devices. Investigate robustness of algorithm.

5) Compare theoretical results with actual measurements.
DESCRIPTION OF TRANSMISSION LINE SYSTEM

A complex coupled lossy transmission line system can be described using S-Parameters. The S-Parameters for a system can be found by cascading transmission parameters of each sub-structure.

DESCRIPTION OF DIGITAL DEVICE TERMINATION

The one-port termination impedance of any digital device can be modelled by a linear series inductor, non-linear shunt capacitor, non-linear series resistor and an EMF source.

SOLUTION TO COMPLEX COUPLED, LOSSY TRANSMISSION LINES TERMINATED WITH NON-LINEAR LOADS.

The node voltages and currents are determined using a numerical technique that solves the termination simultaneously with a set of convolution equations.
MANAGING TRANSMISSION LINE EFFECTS ON INTERCONNECT MEDIUMS

BASIC PROBLEM:

The solution for current through or voltage across a non-linear circuit elements must be solved in the time domain. The solution for lossy transmission lines should be solved in the frequency domain. However, by finding the time-domain Greene's function from measured S-Parameters a lossy transmission line can be solved in the time domain.

CONSIDER A SINGLE TRANSMISSION LINE WITH NON-LINEAR TERMINATION

Let's look just at the transmission line portion of this circuit with a network analyser.

If we are to place this transmission line back into our circuit with non-linear loads then we must remove the effects of the reference impedance.

Vin1 Zscr V1 S11 S12 S21 S22 Zload V2 Vin2

\[ G_{ij}(t) = F^{-1}(0.5S_{ij}(\omega)) \]
\[ G_{ii}(t) = F^{-1}(0.5(1+S_{ii}(\omega))) \]
\[ V_1(t) = V_1v(t)*G_{11}(t) + V_2v(t)*G_{21}(t) \]
\[ V_2(t) = V_1v(t)*G_{12}(t) + V_2v(t)*G_{22}(t) \]

Vin1 Zscr -Zref Zref V1 G_{11} G_{12} G_{21} G_{22} Zref -Zref Zload V2 Vin2

\[ V_1(t) = \text{SOURCE}(V_1,V_1v,Zscr,Zref) \]
\[ V_2(t) = \text{LOAD}(V_2,V_2v,Zload,Zref) \]
\[ V_1(t) = V_1v(t)*G_{11}(t) + V_2v(t)*G_{21}(t) \]
\[ V_2(t) = V_1v(t)*G_{12}(t) + V_2v(t)*G_{22}(t) \]
RESULTS

The following results capture the transmission line effects of two 12 inch coupled lossy lines terminated with FAST devices. A device at port one produces a 25ns pulse. The subsequent ringing and crosstalk are displayed.

Notice the ringing and cross-talk due to the HIGH-to-LOW transition is larger than the effect due to the LOW-to-HIGH transition. This is due to the fact that impedances are closely matched when devices are in the high state and grossly mismatched when devices are in the low state.
EXPERIMENTAL VERIFICATION

The following diagrams show the analytic results and actual experimental data for a 10Mhz clock waveform on the TOPS backplane. The two results match very closely. The difference in ringing at the logic state is due mostly to inductance in the measuring equipment.
STRUCTURE CHARACTERIZATION

To accurately and completely characterize the transmission line effects of a PC Board the transmission characteristics of the following sub-structures must be understood.

- Bends (45°, 90°)
- Multiple Bends
- Vias (25, 50, 75 mil)
- Line width changes
- Bends around a via
- Coupled bends (symmetric and asymmetric)
- Pads
- Jogs
- Via T's and X's
- Via T's with 45° lead-ins

We will use the network analyser to find the Scattering Parameters for each of these sub-structures, for frequency ranges from 0.3 MHz to 20 GHz.

Complex layouts can be fully characterized by cascading the T-parameters (cascadable S-parameters) associated with each sub-structure of a complex layout.

Complete boards can be simulated by finding the Greene's function for a complex layout from the S-parameters for the layout.
1) Verification of transmission line results.

2) Verification of device models.

3) Development of library of macromodels for digital devices.

4) Development of library of measured scattering parameters for each substructure found on a PCB. Scattering parameters should be measured up to 20 GHz for application with GaAs and other high speed logics.

5) Incorporate technique into a transmission line simulation tool.

6) Develop SCAMPER function to use this technique.
Mark S. Basel

Education

BSEE  Michigan State University
MSEE  North Carolina State University
Phd   NCSU (ongoing)

Background

Boeing Aerospace:  Systems Analyst, Seattle Washington
IBM Corporation:  High Speed Bipolar IC Test Equipment Designer
                 East Fishkill, NY.

Research Goals

Develop fast, efficient simulator for analysis of complex electronic interconnection systems using table based methods.
The Problem

>>> Complex transmission line problems affecting system function and performance.

>>> Zeroth order approximation

   >> Length as propagation delay time

   >> No reflections

   >> No coupling between lines

   >> Limited use of transmission line loading of output devices

>>> Problem, high speed circuits

   >> Must minimize propagation time, $T_p$

   >> Shorten line lengths, increase circuit density

      > Smaller line widths
      > More layers, more vias
      > Closer line spacings

   >> Switching delay time of circuits smaller

   >> Devices more sensitive to fast signals

   >> Smaller voltage swings of digital IC's

      > Schottky $TTL$, 0.5 to 2.4 = 1.9 V swing
      > ECL 10K -1.8 to -0.96 = 0.84 V swing
      > Proposed submicron MOS, $V_{dd}$ = 3.0 V
Current Methods

>>> Well documented, classical studies

>> 2D and 3D coupled lines

>> Discontinuities (Bends, Tee’s, etc)

>> Vias

>>> All well versed at handling SPECIFIC cases

>> Coupled lines (usual assumptions)

> Parallel, straight lines
> No random irregularities
> Isotropic, homogeneous constant permittivity
> Constant dielectric and metalization thickness

>> Discontinuities

> Limited bend angles (single bends)
> Tee’s (classic T)
> Limited shape library
> Usually lumped element model (SPICE)
> Multiple discontinuities ??

>> Vias

> Similar assumptions as for discontinuities
(See slide)
> Usually equal widths; line, pad, via

MSB
6/1/88
Complex transmission line system verses typical Via simplification
(From "Quasi-Static Analysis of a Microstrip Via Through a Hole in a Ground Plane", Wang,Harrington,Mautz, IEEE MTT vol 36, 1988)
Why Table Based Methods?

>>> Minimize assumptions about the system within the simulator

>>> Classical Methods

>> Traditional Fields approaches

>> By necessity must make "idealizations" of environment

> Quasi-static Analysis of a Via by Wang, Harrington and Mautz

> Neglects fabrication/process limitations

>> Technology moving toward multi-chip carriers

> Usually ceramic due to similar expansion coefficients with silicon

> Ceramic shrinks but metallization doesn't leading to "rippling" of lines

>>> Filling the Tables

>> Analytical methods (classical EM theory)

>> Measured data

>> Measurements as verification of analytical models

MSB
6/2/88
Table Based Methods

"Scaling" or interpolation in the Frequency Domain

Easiest way to handle microstrip lines
(Or Coax local area networks, etc)

"First pass" simulation using uncoupled lines

Start with frequency domain [S] parameters

Extract complex $Z_0$ and $\gamma$ (propagation constant)

Use standard transmission line equations

To find the voltage or current at any point

Find $Z_{in}$ at any node given the load impedance

Example:

$$Z_{in} = \frac{Z_L + \tanh(\gamma L)}{1 + Z_L \tanh(\gamma L)}$$

Where $Z_L = \frac{Z_L}{Z_0}$

MSB
6/2/88
One Form of Frequency Domain Scaling

>>> Extracting complex characteristic impedance $Z_0$ and propagation constant $\gamma$

>>> Impedance matrix representation of a uniform transmission line

\[
Z_{11} = \frac{Z_0}{\tanh(\gamma L)}
\]

\[
Z_{21} = \frac{Z_0}{\sinh(\gamma L)}
\]

\[
\frac{Z_{11}}{Z_{21}} = \cosh(\gamma L)
\]

>>> Impedance matrix representation from [S] representation

\[
Z_{11} = \frac{(1 + S_{11})(1 - S_{22}) + S_{12}S_{21}}{(1 - S_{11})(1 - S_{22}) - S_{12}S_{21}}
\]

\[
Z_{21} = \frac{2S_{21}}{(1 - S_{11})(1 - S_{22}) - S_{12}S_{21}}
\]

\[
\gamma L = \cosh^{-1}\left(\frac{Z_{11}}{Z_{21}}\right)
\]

\[
\gamma = \frac{1}{L} \ln \left[ \frac{(1 + S_{11})(1 - S_{22}) + S_{12}S_{21}}{2S_{21}} + \left( \frac{(1 + S_{11})(1 - S_{22}) + S_{12}S_{21}}{2S_{21}} - 1 \right)^{1/2} \right]
\]

MSB
6/2/88
Complex propagation constant $\gamma = \alpha + j\beta$ from [S] parameter data of four lossy microstrip transmission lines (from Touchstone data)
Complex characteristic impedance $Z_0$ of the same four lossy transmission lines.
Time Domain Scaling

What is Time Domain Scaling?

- From frequency domain \([S]\) data find the \(FFT^{-1}\)
- Window data to extract impulse response
  - Remove aliasing 'noise' due to bandlimited signal
  - Similar to convolution with finite rise time pulse (Well documented from Digital Signal Processing theory)
  - Minimize data storage
- Store pointer in table
- Use interpolation to determine intermediate responses
- Create linked list of elements making up the tree

Why Time Domain Scaling?

- Direct scaling of impulse response (transfer function)
- Nonlinear loads best handled in the time domain
- Reduction in data storage requirements
- Coupled lines handled similar to other structures
- Discontinuities handled the same as transmission lines

MSB
6/2/88
Simple example of the Time Domain table structure and scaling method for uncoupled microstrip transmission line.
Pulse response of a 377 mm long microstrip line along with the pulse response of a "scaled" line based on the time domain [S] parameters of a 100 mm line.
Future Research

>>> Refine Windowing and Interpolation Methods

    >> Determine the minimum impulse data necessary

    >> Improve interpolation of straight line method

>>> Extend T.D. Interpolation to Coupled Lines

>>> Obtain Measurements for Various Structures

>>> Refine Database Structure and Methodology

    >> Creation of linked lists

    >> Minimize redundancy  (L=200 & L=201 mm)

    >> Provide tools for easy additions of new structures

MSB
6/2/88
Modeling and Analysis of Complex Transmission Line Networks

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Generator connected to loaded transmission line

\[ v(x) = \frac{v_s z_0}{z_0 + z_s} \left[ e^{-\gamma x} + \Gamma_L e^{-\gamma(L-x)} + \Gamma_L \Gamma_s e^{-\gamma(2L+x)} + \frac{2}{\Gamma_L} \Gamma_s e^{-\gamma(3L-x)} + \frac{2}{\Gamma_L} \frac{2}{\Gamma_s} e^{-\gamma(3L+2x)} + \ldots \right] \]
Voltage at any point \( x \) on the line,

\[
v(x) = \frac{v_s z_0}{z_0 + z_s} e^{-\gamma x} \frac{1 + \Gamma_L e^{-2\gamma(L-x)}}{1 - \Gamma_s \Gamma_L e^{-2\gamma L}}
\]

Current at any point \( x \) on the line,

\[
i(x) = \frac{v_s}{z_0 + z_s} e^{-\gamma x} \frac{1 - \Gamma_L e^{-2\gamma(L-x)}}{1 - \Gamma_s \Gamma_L e^{-2\gamma L}}
\]

Reflection coefficient at the load,

\[
\Gamma_L = \frac{z_L - z_0}{z_L + z_0}
\]

Reflection coefficient at the source,

\[
\Gamma_s = \frac{z_s - z_0}{z_s + z_0}
\]

Propagation constant,

\[
\gamma = \sqrt{(r + j\omega)(g + j\omega)}
\]

Characteristic impedance,

\[
z_0 = \sqrt{\frac{r + j\omega}{g + j\omega}}
\]
Section of transmission line with boundary voltages and currents

Voltage transfer function,

\[
\frac{v(x)}{v(0)} = \frac{e^{-\gamma x} \frac{1 + \Gamma e^{-2\gamma L}}{1 + \Gamma e^{-2\gamma L}}}{1 + \Gamma e^{-2\gamma L}}
\]

Current transfer function,

\[
\frac{i(x)}{i(0)} = e^{-\gamma x} \frac{1 - \Gamma e^{-2\gamma L}}{1 - \Gamma e^{-2\gamma L}}
\]
Input impedance of loaded transmission line of length L

\[ Z_{\text{in}}(x) = \frac{1 + \Gamma_L e^{-2\gamma(Lx)}}{1 - \Gamma_L e^{-2\gamma(Lx)}} \]
Example transmission line network
Post-order traversing of tree for impedance calculations

Pre-order traversing of tree for current and voltage calculations
IMPULSE RESPONSE BRIDGED TAP

- Impulse Response

- Samples

- 1 Mile

- 2 Miles
Network to be Simulated
Computed impulse response between sending and receiving stations of test network
CONCLUSION

1) APPROACH

1.1) Frequency domain
1.2) Empirical solutions
1.3) Addressing overall interconnection hierarchy

2) STRENGTH

2.1) Measurement techniques
2.2) Design environment
   2.2.1) Ability to build models
   2.2.2) Insight on design criteria

3) WEAKNESS

3.1) CAD (Manpower)
3.2) Field theory methods
SCHEDULE

PHASE III

MATERIAL STUDY

Dielectric Measurements Results Sept 88
Tolerance Effect Nov 88

CIRCUIT BOARD CHARACTERIZATION

Library models (TxL, Bends, Vias, Etc) Sept 88
Macromodels Nov 88

TOOL DEVELOPMENT (TRAN–SIM)

Single Lines Ongoing
Coupled Lines Ongoing
Nonlinear Loads June 89

NON–LINEAR ANALYSIS

Completed
Single Line
Couple Line
Scamper Model July 88

DE–EMBEDDING TECHNIQUES

Completed
1 port July 88
2 ports Nov 88
N ports June 89

DESIGN GUIDELINES

Dec 88

TABLE BASED MODELLING

Ongoing
PART 2

REPORTS
De-embedding of Two-Port Networks With Symmetric Fixtures

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A straigh-forward procedure for the calibration of a measurement system with symmetric test fixturing is described and experimentally verified.

Introduction

At RF and microwave frequencies the calibration of both vector automatic network analyzers (VANA) and test fixturing is required to accurately determine the scattering parameters of a device under test (DUT). Calibration of a VANA is usually not a problem as it is generally fitted with precision coaxial connectors at the test ports, e.g. APC-3.5, and precisely defined reference standards are available. The conventional OSL (Open Short Load) calibration procedure can then be followed. In situations such as microstrip measurement where conventional standards are not readily available other calibration procedures have been developed. Many of these techniques use variations on the short open and matched load standards, e.g. TSD — Through Short Delay [1], TSO — Through Short Open [2], TRL — Through Reflect Line [3], and LRL — Line Reflect Line [4]. System calibration using most of these techniques is a two-tier method [2,5] whereby the VANA is first calibrated using OSL and precision standards, and a second calibration performed with the required test fixturing in place and using secondary standards. While relaxing the requirements on the reference standards, these techniques can still require calibra-
tion standards which may be difficult to construct. The TSD, TRL and LRL techniques require that the lines (or delays) introduce no discontinuity additional to a possible characteristic impedance discontinuity. Any additional discontinuity is absorbed in the error model developed for the test fixture [6] and is subtracted from the DUT on de-embedding. However, the discontinuity may be an intrinsic part of the DUT. As well, with the TRL and LRL methods the characteristic impedance of the transmission line becomes the reference and therefore must be known or assumed. These problems can be avoided when the test fixturing is symmetrical [7]. Here a straight-forward procedure for the calibration of a measurement system with symmetric test fixturing is described and experimentally verified. The only measurement configuration required is a through connection thus, in conformance with the practice of naming calibration procedures, we designate the new technique the TSF — for Through Symmetric Fixture — method.

Symmetric Fixture

When can test fixturing be treated as symmetric? The requirement for symmetric de-embedding as used here is that the test fixtures are identical and each fixture is symmetric. This holds at low frequencies when distributed effects are not significant or when the fixtures are electrically small. This also holds at higher frequencies with careful design of the test fixtures so that they are symmetrical. Ideally test fixtures introduce negligible discontinuity and so look like matched transmission lines.

Fixturing for two-port measurements is shown in the through configuration in Figure 1 along with signal flow graph representations of the through measurement and the second-tier error models that must be determined. If A and B are not identical then a conventional calibration scheme is required to determine the eight error terms, \( (e_{ija} \text{ and } e_{ijb}) \). Practically each fixture is reciprocal \( (e_{ij} = e_{ji}) \) and so there are only 6 unique error terms. In many situations the fixtures A and B are identical so that B is the port reverse, \( A^R \), of A, Figure 2. Now there are 3 unique error terms to be evaluated. If in addition each fixture
is symmetric, we have the through configuration and signal flow graph representations of Figure 3 where the scattering matrix of each fixture is

$$[S_e] = \begin{bmatrix} \alpha & \delta \\ \delta & \alpha \end{bmatrix}$$

(1)

. It is this structure that was addressed in [7] and is considered here.

Method

The determination of the error terms ($\alpha$ and $\delta$) is based upon signal flow graph theory. S-parameter measurements of the through connection yield two independent quantities, $S_{11}$ and $S_{21}$, as $S_{11} = S_{22}$ and $S_{12} = S_{21}$ because of symmetry and reciprocity. This is sufficient to determine $[S_e]$.

The signal flow graph provides two algebraic relationships for the known quantities as functions of the error terms:

$$S_{11} = \delta + \frac{\alpha^2 \delta}{1 - \delta^2}$$

(2)

$$S_{21} = \frac{\alpha^2}{1 - \delta^2}$$

(3)

Rearranging

$$\delta = \frac{S_{11}}{1 + S_{21}}$$

(4)

$$\alpha = \sqrt{S_{21} \frac{b^2 - S_{11}^2}{b^2}}$$

(5)

where

$$b = 1 + S_{21}$$

(6)

The square root gives two possible solutions and the root choice depends upon the electrical length ($L_e$) of the through connection. The positive root is valid when

$$n\lambda < L_e < \frac{(2n + 1)\lambda}{2}$$

(7)

where

$$n = 0, 1, 2, \cdots$$

(8)
otherwise the negative root is correct.

Equation (4) contains a singularity that can restrict the use of TSF. When the cascade $S_{21}$ is nearly equal to $-1$ equation (4) will return invalid results for $\delta$. This singularity can be avoided if the length of the cascade fixture is constructed such that it is not an integer half wavelength ($\frac{n\lambda}{2}$) long at any frequency in a desired measurement range.

**De-embedding**

The device under test (DUT) is inserted between the fixture halves and the embedded s-parameters are measured ($[S_{emb}]$) figure 5. The de-embedding is most easily carried out if cascadable s-parameters (t-parameters) are used. This requires conversion of all s-parameters to t-parameters with the standard s to t transform

$$\begin{bmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{bmatrix} = \frac{1}{S_{21}} \begin{bmatrix} 1 & -S_{22} \\ S_{11} & S_{12}S_{21} - S_{11}S_{22} \end{bmatrix}$$

so $[S_e]$ becomes $[T_e]$ and $[S_{emb}]$ corresponds to $[T_{emb}]$.

After conversion the embedded DUT is given by the following equation.

$$[T_{emb}] = [T_e][T_{DUT}][T_e]$$

Pre- and post-multiplication of this equation gives the t-parameters of the DUT

$$[T_{DUT}] = [T_e]^{-1}[T_{DUT}][T_e]^{-1}$$

and thus its s-parameters

$$\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} = \frac{1}{T_{11}} \begin{bmatrix} T_{21} & T_{11}T_{22} - T_{21}T_{12} \\ 1 & -T_{12} \end{bmatrix}$$

**Verification**

Verification requires comparison of a TSF error model with direct VANA (calibrator, using TSO) measurement of the test fixture. Increased confidence is obtained by comparing TSO and TSF calibrated measurements of a de-embedded DUT. These measurements
require that the same sexless connectors at the ports of the fixtures and the DUT. The calibration and measurement procedure is outlined in figure 4 where the DUT is a 500 MHz low pass filter and APC-7 connectors are used at the ports. The TSF fixture error model is compared to direct measurement in figure 5. We see that $S_{21} (\delta)$ and $S_{11} (\alpha)$ are tracked accurately. The final test, comparison of the TSF de-embedded DUT with direct VANA measurement is presented in figure 6. Again excellent agreement is obtained.

The fixtures we used were shunt inductors inserted between two APC-7 to SMA adapters. This choice of fixture was chosen for three reasons. First the inductive discontinuity introduced significant error which was then removed with TSF. Second the inductive element reduces the electrical length of the fixture thus forcing the $\frac{\lambda}{2}$ condition out of the frequency range that we were interested in. And third the lumped element was easily tuned to meet the fixture symmetry assumptions necessary for TSF. With the single calibration configuration, a simple through, TSF may be preferable to the more elaborate TSD, TRL and LRL techniques which require multiple disconnections and reconnections even at reasonably high frequencies when test fixture symmetry can be exploited.

Conclusion

We have presented a straight-forward technique, the TSF method, for determining the scattering parameters of a device measured with a symmetrical test fixture. The single calibration configuration is the through connection. TSF is the appropriate technique to use when the classical reference standards are not readily available, when test fixture symmetry can be exploited, or when measurements are required at frequencies low enough that asymmetrical fixture discontinuities can be neglected. The procedure follows directly from the application of signal flow graphs.

References


Figure 1. Through calibration with dissimilar fixtures, (a) configuration, (b) signal flow graph of through measurement, and (c) signal flow graph of error models.

Figure 2. Through calibration with identical fixtures, (a) configuration, (b) signal flow graph of through measurement, and (c) signal flow graph of error models.

Figure 3. Through calibration with symmetric and identical fixtures, (a) configuration, (b) signal flow graph of through measurement, and (c) signal flow graph of error models.

Figure 4. Configuration for measuring the DUT.
Figure 5. Comparison of error scattering parameters with direct VANA measurement.
Figure 5. Comparison of error scattering parameters with direct VANA measurement.
Figure 5. Comparison of error scattering parameters with direct VANA measurement.
Figure 6. Comparison of DUT scattering parameters with fixtures, DUT de-embedded using TSF, and direct VANA measurement.
Figure 6. Comparison of DUT de-embedded scattering parameters with direct VANA measurement.
Figure 6. Comparison of DUT scattering parameters with fixtures, DUT de-embedded using TSF, and direct VANA measurement.
Figure 6. Comparison of DUT scattering parameters with fixtures, DUT de-embedded using TSF, and direct VANA measurement.
Figure 6. Comparison of DUT de-embedded scattering parameters with direct VANA measurement.
A SURVEY OF TECHNIQUES TO
MEASURE THE DIELECTRIC
CONSTANT OF PC BOARDS

Submitted to BNR
as part of the
University Interaction Program
with
N. C. State University

C. Heyward Riedell
Dept. 3D21
BNR RTP
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This document is a review of current research into techniques for measuring the dielectric constant of PC Board laminates. Justification for high frequency (into the microwave region) study is given. Techniques that may be adapted from the present literature are discussed. For the methods chosen, analytic equations are given and design criteria are listed. Results from several measurements are discussed, and a comprehensive list of references is compiled for future interest in this subject.
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1. INTRODUCTION

1.1 Subject

The purpose of this paper is to discuss and compare current techniques of measuring the permittivity of dielectric materials. The focal point of this research will be to provide a recommendation of those techniques applicable to PCB (Printed Circuit Board) laminates.

1.2 Background

High speed digital signal propagation is limited by the quality of the PCB into which components are inserted. As clock speeds increase, circuit designers must be more aware of transmission problems caused by impedance mismatch, manufacturing tolerances, and discontinuities. In an effort to better understand these problems, this paper investigates current techniques to measure the dielectric constant—one of the physical parameters directly influencing impedance.

The impedance of a printed circuit track is a function of the dielectric constant of the insulating material separating a conductor from its ground plane(s). Unfortunately, PCB dielectrics are not always homogeneous materials described by a simple constant—especially at high frequencies (microwave). In fact, the effective dielectric constant seen by a transmission line can be a function of several variables (e.g., frequency, direction, temperature). Information resulting from dielectric constant measurement techniques will enable digital circuit designers to better understand impedance as a function of dielectric variation. This increased understanding will lead to tighter control of impedance variation and improved PCB quality.

1.3 Measuring The Dielectric Constant

The dielectric constant or complex permittivity can be separated into a real and an imaginary part. Figure 1.1 illustrates a generic material's frequency depend-

\[ \varepsilon_r = \varepsilon_r' - j\varepsilon_r'' \]

Figure 1.1) Frequency Dependent Permittivity. Permission to reprint [30].
ent permittivity. The real part of the permittivity directly influences the impedance of conductors, and the imaginary part influences the dielectric loss. A literature study on current research in this area revealed methods of measuring both parts of the permittivity; however, research specific to PCB’s is limited. Much of the literature focused on techniques to study the permittivity of MIC (Microwave Integrated Circuit) substrates. Some of these techniques, however, can be adapted directly to PCB’s.

The reason for emphasis in the literature on MIC substrate measurement techniques is linked to the frequency at which the permittivity is to be measured. Designs for MICs require values for the permittivity in the microwave region. Until recently there has been little interest in PCB properties at microwave frequencies, and lower frequency values of the permittivity have been used. Digital devices with fast rise times can generate pulses with frequency components extending into the gigahertz region. Figure 1.2 shows the even and odd components of the Fourier Transform of a fast pulse train. If the complex permittivity exhibits frequency dependence, these components will become distorted as they travel down a transmission line. Figure 1.3 shows one effect of distortion on a pulse propagating down a transmission line. Distortion can introduce transmission errors between devices and therefore must be controlled. Thus, improved characterization of PCB laminates through permittivity measurement deserves investigation.
1.4 Criteria For Consideration

Several items should be considered in choosing testing techniques for the complex permittivity:

(1) the possibility of anisotropic behavior,
(2) the frequency range,
(3) the measurement of both the real and imaginary parts of the permittivity, and
(4) the ease of implementation.

Since PCB laminates are fabricated with a resin/fiber combination, the effective dielectric constant seen by a transmission line may be a function of direction, with respect to some arbitrary coordinate system. Attention must be paid to the direction of the electric field during measurement to simulate the field configuration of a PCB track. A measurement of permittivity in which the fields propagate perpendicular to the PCB would likely be different to one taken in which the fields propagate in the plane of the board. The latter more closely resembles the field configuration of a PCB transmission line.

Frequency dependence should be quantified. If permittivity variation over a wide frequency range is minimal, an average value may be used in impedance calculations. If, however, the variation is extensive, its effect on signal propagation must be studied.

Determination of both parts of the complex permittivity is desirable. More comprehensive information about dielectric materials will improve the process of selecting laminates for high speed applications.

Finally, the difficulty of implementing the techniques should be addressed. Can test samples be easily fabricated? Does the technique require elaborate preparation, or can the test be done with relative ease?

2. CURRENT METHODS

The various dielectric measurement techniques can be divided into four major categories: (1) Resonance, (2) Reflection/Transmission, (3) Time Domain Reflectometry, and (4) Length Comparison.

2.1 Resonance Methods

Resonance methods yield information about the complex per-
mittivity at a specific resonant frequency for the structures involved. To characterize a PCB dielectric material at many frequencies, several structures designed to resonate at appropriate harmonics are needed. This multiplicity of test structures tends to complicate the characterization procedure. However, if the variation of the permittivity over a specified frequency range is expected to be minimal or monotonically changing, a spot check may be done with just a few structures. A discussion of four types of resonant systems follows.

2.1.1 Perturbation

Perturbation techniques are used frequently in electromagnetic theory to describe a system that deviates slightly from a 'known' system. A 'known' system is one that is well characterized theoretically. This system is perturbed slightly by changing some parameter, and the difference in response between the two systems is then expressed in terms of a modified solution to the 'known' system.

The Perturbation technique makes the assumption that a dielectric sample does not radically disturb the electromagnetic fields of a cavity in which it is inserted. Measurements are taken of the resonant frequency for a cavity without a sample to provide the 'known' response. The measurements are then repeated with a dielectric sample perturbing the cavity as shown by Figure 2.1. To calculate the real part of the permittivity, a formula can be derived that is dependent on the resonant frequency shift caused by perturbing the 'known' system [1]-[3].

The imaginary part of the permittivity is derived from the Q (Quality) factor of the cavity as determined by the 3dB bandwidth. The Q factor is measured both before and after dielectric perturbation of the cavity’s fields. As before the change or shift in the Q factor is used to calculate the imaginary part.

If dielectric loss is quite low, Q measurements may be er-
A technique to determine the conductivity that utilizes the coupling factor, frequency shift, and change in reflected power after dielectric insertion has been reported [1]. Alternatively, if the dielectric is rather lossy, it may be difficult to determine the exact location of the resonant and 3dB frequencies. A technique of increasing the Q factor during measurement called Q factor multiplication has been attempted with success [3].

With regard to the criteria listed in section 1.4, the perturbation method has some drawbacks. Anisotropic behavior of a dielectric material cannot be measured due to multi-dimensional resonance. If the cavity is made to resonate in one direction only (by dimensional adjustment) the dielectric sample is no longer a perturbation of an air cavity. It becomes a dielectrically loaded cavity, and the perturbation formulas no longer apply. Due to the dimensional constraints of a cavity, the perturbation method is suited to research at frequencies greater than about 1 GHz. However, if the frequency is too high the dimensions of a cavity become too small to treat a PCB laminate with perturbation theory.

### 2.1.2 Dielectric Resonators

Dielectric resonators have been used extensively in MIC circuitry. A novel technique has been developed for use in measuring the permittivity of MIC substrates [4]. Two cylindrical dielectric resonators are positioned above and below a planar dielectric sample as shown in Figure 2.2. They are loosely coupled by a magnetic field to microstrip input and output lines. The low coupling reduces Q factor loading. The real part of the permittivity of the substrate can be calculated from the measured resonant frequency, the dielectric resonator parameters (diameter, height, and dielectric constant), and the substrate thickness. In addition, the loss tangent is computed from the Q factor.

This method allows the determination of local permittivity (ie. at the point of component contact). Unfortunately, the substrate bulk per-
mittivity must be known in advance to yield accurate measurements. This technique is appropriate for finding local inhomogeneities in a presumed homogeneous substrate. Anisotropy cannot be investigated due to the cylindrical nature of the resonant system. The local permittivity calculated is an average value dependent on more than one direction. The operating frequency is on the order of 10 GHz or greater due to the size of the dielectric resonators. This limits the value of the technique, since the 100-10,000 MHz range is of more interest.

2.1.3 Coaxial Lines

An open circuited coaxial transmission line resonator has been proposed [5] for measuring the dielectric constant and loss tangent in homogeneous, rather lossy materials. The resonant structure consists of a transmission line with a capacitive coupling gap at one end and an open circuit at the other (See Figure 2.3). A parallel lumped circuit modelling the system incorporates a coupling capacitance for the gap, an LCG circuit for the resonant length of line, and a capacitance and conductance for the fringing field at the open end.

As in the perturbation methods, the shift in the measurement response due to the introduction of a dielectric into the resonant system is used to calculate the desired parameters. This method is recommended for frequencies up to about 4 GHz. An improvement in the lumped model to include radiation effects has been demonstrated that extends the frequency range into X band [6]. This technique incorporates a radiation conductance that is included with the fringing field terms in the lumped parallel circuit model.

To calculate the dielectric constant and the loss tangent, measurements are taken of the resonant frequency and the Q factor while allowing the electromagnetic fields at the open end to fringe into free space. The measurement is then repeated while the fields fringe into a sample of dielectric material that is placed against the open end of the transmission line. If a coaxial line is used, the field configuration is radially distributed with respect to...
the center conductor, and an average value of permittivity would then be measured as the field fringed into the dielectric. If a stripline were used instead, the field lines would be more appropriate for PCB laminates.

Anisotropic behavior may be studied by placing various surfaces of a laminate against the open end of the transmission line, but the uniformly distributed radial fields may introduce error since they are different from the field distributions of microstrip and stripline in PCBs. The frequency range is more favorable to PCB study than the previous two methods. Resonant lines can be fabricated for frequencies as low as 500 MHz and as high as 10 GHz. This technique may prove to be well suited to PCB laminate permittivity measurement. However, a problem may arise due to the thickness of a PCB dielectric sample. Fringing at the open end should occur only in the adjoining sample. Too thin a sample may cause fringing into free space simultaneously, thus changing the value of the permittivity calculated. Care must be taken in implementing this method.

2.1.4 Cavity Resonance

The literature available has many references to resonant cavity measurements. The geometry of the measurement structures usually corresponds to the intended use of the dielectric material. For example, a cylindrical structure is ideal for studying fiber optic cables. Other potential cavities include waveguides structures [7]-[8], metal-clad laminates [9]-[14] (a good candidate—refer to Figure 2.4), and other exotic cavities for specific applications such as the Fabry-Perot (open resonator) and reentrant cavities [15]-[17].

The real part of the permittivity can be determined by measuring the resonant frequency and the physical dimensions of the cavity. The imaginary part can be found from the Q factor of the resonator; however, the cavity must be relatively unaffected by the coupling mechanism (small loaded Q) and the losses in the metal must be accounted for.
The difference between this method and the methods of 2.1.1 and 2.1.3 is that only one measurement is taken to obtain results. A measurement with and without a dielectric is not needed.

The metal-clad laminate would be the most accurate resonant cavity for PCB materials. Measurement errors due to air gaps between the inserted sample and the cavity walls are eliminated. Fringing from the sides of the cavity can be reduced by coating the edge of the laminate with conductive material. The metal-clad laminate structure can be simplified to strip transmission line resonators by utilizing open (or short) circuited microstrip and stripline tracks [9],[18]–[21](refer to Figures 2.5 and 2.6). Previous work has been done utilizing the band-stop and bandpass fil-

![Figure 2.5) Microstrip 'Cavity' (a) Elevated View, (b) Cross Section](image)

![Figure 2.6) Stripline 'Cavity' (a) Elevated View (b) Cross Section](image)


ter configurations of MIC's. The preferred structure is the linear resonator which consists of an input and an output line coupling energy to and from a strip transmission line.

The cavity method appears to be the best of the resonant techniques. Anisotropy can be studied by fabricating resonators in the direction of interest on a PCB. The frequency range is as broad as the coaxial resonator. Sample preparation is quite simple. No cutting or shaping to fit a test structure is needed. The test structure can be included in the normal fabrication of a PCB. In addition, crude linear test resonators can be constructed from an existing PCB by cutting two gaps in microstrip or stripline tracks.
2.2 Reflection/Transmission Methods

Reflection/transmission methods yield information regarding the frequency dependence of permittivity at each frequency sampled. Consequently, less test structures are needed to obtain that information as compared to resonant methods. Three types of reflection/transmission methods are discussed below.

2.2.1 Transmission Line Dielectric Insertion

Transmission line insertion methods utilize a dielectric sample's reflection and transmission coefficients. These coefficients can be calculated from S-parameters measured by a network analyzer. From these coefficients the complex permittivity can be derived. The test structure consists of a transmission line with a dielectric sample inserted in the path of an electromagnetic wave. Two items of concern are the bandwidth of the measurement system and the ease of sample fabrication.

Three transmission line structures have been reported: a coaxial line, a waveguide, and a stripline [22],[23]. The Coax method (refer to Figure 2.7) has large bandwidth but is difficult to fabricate. A PC Board dielectric layer must be constructed to the thickness of a coaxial air lines' internal dimensions. Then the sample must be machined into a cylinder, including a drilled hole for the center conductor. Once inserted, the sample must surround the center conductor and mate with the outer shield while minimizing air gaps. (Air gaps alter the reflection and transmission coefficients measured.)

The Waveguide method has small bandwidth yet is relatively simple to fabricate compared to the coaxial structure. The waveguide configuration illustrated by Figure 2.8 (next page) requires a rectangular sample machined to the inner dimensions of the guide in use. Again, air gaps should be minimized to increase the accuracy of the reflection and transmission.
sion data. Unfortunately, the sample size is prohibitive for PCB's at the frequencies of interest. For example, the inner thickness for waveguide at 3 GHz is approximately 0.75 inches depending on the frequency band chosen. This dimension becomes ridiculous at lower frequencies. At 1.0 GHz the thickness approaches 4.5 inches. Obviously waveguide is only appropriate at much higher frequencies.

The Stripline method has a coax/stripline/coax structure (Figure 2.9) designed to allow two square dielectric slabs to be placed around the middle third of the stripline (The other two regions are free space). A ground plate is placed on either side of the dielectric, and the permittivity is determined from the reflection and transmission coefficients at the air/dielectric interfaces. Fabrication of the dielectric samples is not difficult. A hindrance, however, is the need for tuning the overall stripline impedance by inserting capacitive pins into the air regions. This tuning makes measurement tedious.

The field configurations of each of the above structures are acceptable for anisotropic study, since they propagate in the plane of the board, but again the uniformly distributed radial fields of the coaxial line may lead to some inaccuracy. The horizontal components are stronger in the coax than for the fields of the waveguide and stripline. Their fields are more concentrated in the vertical direction. The bandwidth of the coaxial line and the stripline are superior to the narrow bandwidth of waveguide. Sample preparation would be the most difficult for the coaxial structure and the least difficult for the stripline.
2.2.2 Coaxial Lumped Capacitance

The Coaxial Lumped Capacitance method has been investigated for lossy materials such as alcohols, thin semiconductor samples, small magnetic materials, and biological substances such as human epidermis [24]-[25]. The major drawback of this technique is the required dimension of the test structure. The method requires the fabrication of an extremely small dielectric sample with a diameter the same size as the inner conductor of a coaxial line. The longitudinal thickness must be smaller than the wavelength. These dimensions may prove to be unachievable considering that a PCB has a fiber/resin composition and may be difficult to machine.

Assuming that a sample is fabricated, it is inserted at either the end of a coaxial transmission line in a shunt connection or at some distance from the end of the line in a series connection as seen in Figure 2.10. The reflection coefficient is used to calculate the complex permittivity.

Theoretically, the fringing of fields can be neglected for parallel plate capacitors if the plate surface areas are large compared to the thickness of the dielectric. The lumped capacitance method does not have a large surface area to thickness ratio, however, and an extension of the method to include the fringing effect has been published [26]. A frequency range from 0.1-10 GHz can be obtained. Measurement of anisotropic behavior is complicated by the fringing fields and the small size of a test structure. One expects the results to be quite similar no matter how the sample is oriented.

2.2.3 Variable Impedance

This method requires a dielectric sample to be inserted into a transmission line and backed by an adjustable short circuit [27]. The phrase "variable impedance" refers to the impedance at the back of a test sample as the short circuit is adjusted. For the most accurate results at the frequency of interest, the short
circuit is positioned to produce a minimum reflection coefficient. The impedance at the input to the sample is determined from the reflection coefficient, and the propagation constant is found from the impedance. The permittivity is derived from the propagation constant.

The major hindrance to this method is the necessary tuning of the short circuit to produce a minimum reflection coefficient. This measurement interruption makes the investigation of many different frequencies as tedious as the tuning of the stripline method of section 2.2.1. Again, the permittivity as a function of direction can be studied by placing a dielectric sample in several different orientations in the transmission line. The frequency range is as broad as the transmission line used allows. Sample fabrication is simplest for a waveguide.

2.3 Time Domain Reflectometry (TDR)

TDR is a technique by which signal reflections measured in the time domain provide information about transmission lines, discontinuities, and loads. A comparison between a signal sent down a transmission line and the signal returned yields a quantity known as the reflection coefficient.

Two methods for TDR have been found in the literature [28]. In each case a dielectric sample is inserted into a measurement cell that connects to a coaxial line. The first reflection method only takes into account reflections from the front face of a sample. The second method terminates the sample with a load that matches the line, and the time window is set such that all reflections are taken into account.

Frequency domain information is obtained through Fourier Analysis. A Fourier Transform is performed on the signals reflected from a test sample and a reference structure. The frequency domain reflection coefficient is obtained by dividing the response due to the sample by that of the reference and multiplying by the reference signal's reflection coefficient. This reference is specific to the measurement system being used. The complex permittivity can be related to the frequency domain reflection coefficient and is found numerically.

This technique has been successful for a bandwidth of 2 MHz to 8 GHz. It has been used to study materials with fast relaxation phenomena and resonances due to ionic or molecular polarization.
This method may be applied to PCBs if a suitable test structure is devised. The variation of permittivity with respect to orientation may be studied by changing the surface of reflection for the sample. Again, if coaxial line is used, error may be introduced by the horizontal components of the fields reflected by the sample.

2.4 Length Comparison

The length comparison method utilizes the electrical and physical length differences of a pair of microstrip or striplines as seen in figure 2.11 [29]. The real part of the permittivity is related to the difference in the electrical lengths divided by the difference in the physical lengths. The imaginary part of the complex permittivity cannot be measured by this technique.

An advantage of this method over other methods is the direct cancellation of the effect of connectors on measurements. Their influence is simply subtracted out by taking the difference of measurements. Anisotropic behavior can be studied by placing the transmission lines in various orientations on a PCB. The frequency range is broad and the method should be accurate until the frequency is so high that connector error cannot be subtracted. Fabrication of a test structure merely requires obtaining a PCB with various length lines. The only drawback in relation to the other methods previously mentioned is the inability to determine the imaginary part of the complex permittivity.

3. CONSIDERATIONS

As previously stated in section 1.4 several items should be considered (refer to Figure 3.1 next page) in choosing testing techniques for the complex permittivity: (1) anisotropic behavior, (2) the frequency range, (3) measurement of both the real and imaginary parts of the permittivity, and (4) the ease of im-
plementation of the technique.

With respect to anisotropy, the Resonant Cavity method stands out from the others. Cavities can be designed to resonate in desired directions, thus providing information on the directional dependence of the permittivity. The various reflection methods yield directional information specific to the geometry of the structure at hand. Time Domain Reflectometry and Length Comparison may be acceptable methods of determining anisotropy.

The second item for consideration was the frequency range available for each test. Reflection/Transmission methods have a

<table>
<thead>
<tr>
<th>Methods</th>
<th>Measures Anisotropy</th>
<th>Frequency Range</th>
<th>Real and Imaginary</th>
<th>Ease of Implementation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Perturbation</td>
<td>Poor</td>
<td>&gt; 1 GHz</td>
<td>Yes</td>
<td>Simple</td>
</tr>
<tr>
<td>Dielectric Resonators</td>
<td>Poor</td>
<td>&gt; 10 GHz</td>
<td>Yes</td>
<td>Simple</td>
</tr>
<tr>
<td>Coaxial Lines</td>
<td>Fair</td>
<td>.5-10 GHz</td>
<td>Yes</td>
<td>Simple</td>
</tr>
<tr>
<td>Cavity Resonance</td>
<td>Good</td>
<td>.5-10 GHz</td>
<td>Yes</td>
<td>Simple</td>
</tr>
<tr>
<td>Coaxial</td>
<td>Fair</td>
<td>DC-10 GHz</td>
<td>Yes</td>
<td>Hard to Machine</td>
</tr>
<tr>
<td>Waveguide</td>
<td>Fair +</td>
<td>&gt; 1 GHz</td>
<td>Yes</td>
<td>Large Dimension</td>
</tr>
<tr>
<td>Stripline</td>
<td>Good</td>
<td>DC-10 GHz</td>
<td>Yes</td>
<td>Tuning</td>
</tr>
<tr>
<td>Coaxial Capac.</td>
<td>Fair</td>
<td>.1-10 GHz</td>
<td>Yes</td>
<td>Small Dimension</td>
</tr>
<tr>
<td>Variable Imp. Line Used</td>
<td>Depends on Line Used</td>
<td>Depends on Line Used</td>
<td>Yes</td>
<td>Tuning</td>
</tr>
<tr>
<td>TDR</td>
<td>Depends on Line Used</td>
<td>.2-8 GHz</td>
<td>Yes</td>
<td>Computer Processing</td>
</tr>
<tr>
<td>Length Comp.</td>
<td>Good</td>
<td>DC-10 GHz</td>
<td>No</td>
<td>Simple</td>
</tr>
</tbody>
</table>

Figure 3.1) Summary of Considerations
broader frequency range than Resonant methods. As previously stated, many resonant structures are needed to provide the same amount of information as one reflection/transmission test structure. The TDR and Length Comparison methods have wide frequency ranges also.

Another criterion was the ability to measure both parts of the complex permittivity. Each test method described above can measure both the real and imaginary parts except for the Length Comparison method. This method only measures the real portion.

The final consideration in choosing a test method was the ease of implementation. Several structures are not suitable for PCB study merely due to the size of the sample required. The Waveguide Insertion method needs very thick samples, and the Coaxial Capacitance method needs extremely small samples. The Stripline Insertion and the Variable Impedance methods seem impractical since many mechanical adjustments would be needed during the tests. These adjustments require interrupting the test, which leaves room for operator error and increases the testing time significantly. The problem of averaging the data over the volume of the sample or over the cross sectional distribution of the applied electromagnetic fields, should make one wary of the Perturbation method and any method relying on coaxial transmission lines. These methods are more appropriate for a homogeneous dielectric. Finally the Dielectric Resonator method should be eliminated since it is designed for finding local variations in a dielectric constant. The bulk permittivity must be known beforehand.

With these considerations in mind, the Resonant Cavity method was chosen as a point of initial inquiry for PCB study. Even though several structures will be needed to gather information about the permittivity at many frequencies, the question of anisotropic behavior can be easily determined. Both parts of the permittivity will be investigated, and the simplicity of the technique is appealing. After evaluation of the results of this method other techniques may be recommended.
4. THEORY-RESONANT CAVITY PERMITTIVITY DERIVATIONS

Beginning with Helmholtz's Equations, derive the resonant frequency for a general rectangular cavity seen in Figure 4.1 [31]

![General Rectangular Cavity](image)

Figure 4.1) General Rectangular Cavity

\[ \nabla^2 E + K_0^2 E = 0 \]  
\[ \nabla^2 H + K_0^2 H = 0 \]

Solve for the Hz component of the H field by using the transverse and longitudinal del notation and separation of variables. Since \( E_{\text{tan}} \) and \( H_{\text{norm}} \) go to zero at the walls of a waveguide, Hz can be found

\[ Hz = A \cos \left( \frac{m \pi}{a} \right) \cos \left( \frac{n \pi}{b} \right) \]  

along with the cutoff wavenumber, \( K_c \), and the propagation constant, \( \beta \).

\[ K_c^2 = K_x^2 + K_y^2 \]  
\[ B^2 = K_0^2 - K_c^2 = \frac{2\pi f}{c} \]

where \( K_x = \frac{m \pi}{a} \)  
and \( K_y = \frac{n \pi}{b} \)
By closing the ends of the waveguide with shorting plates a standing wave is set up due to the new boundary. These boundary conditions yield the \( H_z \) component

\[
H_z = -2jH \cos \left( \frac{m \pi}{a} \right) \cos \left( \frac{n \pi}{b} \right) \sin B_d
\]  

(9)

with

\[
B = \frac{1}{d} \pi
\]

(10)

Now, using Equations 5, 6, 7, 8 and 10 solve for \( f \), the resonant frequency.

\[
f = c \sqrt{\left( \frac{1}{2d} \right)^2 + \left( \frac{m}{2a} \right)^2 + \left( \frac{n}{2b} \right)^2}
\]

(11)

Noting that the above was derived for free space, the speed of propagation, \( C \), can be replaced by \( V \), the velocity in a dielectric medium

\[
V = \frac{C}{\sqrt{\varepsilon_r}}
\]

(12)

and the real part of the complex permittivity can be found.

\[
\varepsilon_r' = \left( \frac{c}{f} \right)^2 \left[ \left( \frac{1}{2d} \right)^2 + \left( \frac{m}{2a} \right)^2 + \left( \frac{n}{2b} \right)^2 \right]
\]

(13)

For the case in which resonance is allowed only in the longitudinal direction, Equation 13 reduces to

\[
\varepsilon_r' = \left( \frac{c}{f} \right)^2 \left( \frac{1}{2d} \right)^2 = \left( \frac{c}{2fd} \right)^2
\]

(14)
The imaginary part of the complex permittivity is found from the Q factor of the cavity, assuming wall losses are negligible

\[ Q_d = \frac{\varepsilon_r'}{\varepsilon_r''} \]  

If wall or radiation losses are significant, then the total Q would be comprised of the three terms \( Q_d, Q_w, \) and \( Q_r \).

\[ Q = \left( \frac{1}{Q_d} + \frac{1}{Q_w} + \frac{1}{Q_r} \right)^{-1} \]  

The terms \( Q_w \) and \( Q_r \) can be removed from a Q measurement to yield the desired \( Q_d \) and hence the loss tangent.

5. DESIGN

Three types of resonant cavities will be investigated. The first two cavities are actually microstrip and stripline transmission line resonators, but they may be considered to be derivatives of the cavity concept. The same formulas apply. The cavity most resembling the theoretical treatment of section 4, however, is the metal-clad laminate.

5.1 Microstrip

The microstrip structure, as depicted in Figure 2.5, was simulated using the software program Super Compact. The program was used to look at the effect of gap distance variation. It was seen that coupling across the gap was maximized at a distance between 3 and 7 mils. Since this approaches the limits of PCB fabrication technology, the gap distance was then set to 5 mils. Anisotropic study requires the separation of resonant modes by dimensional restriction. In addition, multiple structures would be needed to study a wide frequency range. Concerns arose as to the effect of linewidth on the accuracy of measurements, and the potential problem of crowding resonances as frequency is increased.
To study these questions the following conditions were imposed.

1) Resonance was restricted to one direction only.

2) The resonant structures were duplicated with one set lying in a direction perpendicular to the other set.

3) 3 linewidths were chosen to be 25, 50, and 100 mils. The 25 mils line was designed for 50 ohms.

4) Dominant mode resonance for the six frequencies of 0.5, 0.75, 1.0, 5.0, 7.5, and 10.0 GHz was designated by appropriately choosing six different line lengths.

5.2 Stripline

The stripline structure, shown in Figure 2.6, was to be simulated on Super Compact also, but an error in the version used produced gain (the structure is passive). A technical representative from the software company offered to run the simulations on the latest version. The results were similar to the microstrip simulation, so the same dimensions were used. Hence, the only difference between the microstrip and stripline test boards is the cross section of the transmission lines.

5.3 Metal-Clad Laminate

The metal-clad laminate resonators, illustrated in Figure 2.4, were deemed to be the most accurate cavity, since the sidewalls are metallized and fringing is eliminated. Design criteria were as follows.

1) Resonance was to occur in the longitudinal direction.

2) End launch connectors were to excite the cavity.

3) Dominant mode frequencies were chosen to be 0.5, 0.75, 1.0, 5.0, 7.5 and 10.0 GHz to compare with the microstrip and stripline boards.

6. MEASUREMENTS

The measurements section is divided into two main components. Section 6.1 highlights information obtained from raw data. Section 6.2 relates insight gained from the results of the Resonant Cavity
6.1 PRELIMINARY RESULTS

The preliminary results for resonant cavity measurements presented in this section provide a nominal value of complex permittivity and indicate the trend in permittivity variation as a function of frequency and orientation. Results are based on microstrip and stripline measurements. Measurements of a metal-clad laminate are not yet available.

6.1.1 Nominal Values

To calculate a nominal value of the real part of the complex permittivity for the laminate tested (FR4), a crude parallel plate capacitor was fashioned from some scrap PCB laminate. A capacitance meter was used to determine the capacitance of the structure. Utilizing the formula for a parallel plate capacitor \( C = \varepsilon_0 A / T \), a relative value of 3.9 was calculated. A nominal value for the imaginary part of the complex permittivity was inferred from the loss tangent of a resin at 100 MHz of 0.0264. These values compare favorably to values calculated from resonant cavity measurements.

6.1.2 Frequency Trend

Shown below in Figure 6.1 is the general trend of permittivity versus frequency. The real part appears to decrease, but not severely. The imaginary part also appears to decrease with frequency. These calculations were made using raw S-parameter data (internally corrected with respect to an open, short and load) from a network analyzer for a 100 mils wide stripline resonator.

<table>
<thead>
<tr>
<th>F (MHz)</th>
<th>( \varepsilon_r' )</th>
<th>( \varepsilon_r'' )</th>
<th>loss tan</th>
</tr>
</thead>
<tbody>
<tr>
<td>474.50</td>
<td>4.286</td>
<td>0.203</td>
<td>0.047</td>
</tr>
<tr>
<td>950.50</td>
<td>4.273</td>
<td>0.175</td>
<td>0.041</td>
</tr>
<tr>
<td>1432.50</td>
<td>4.233</td>
<td>0.168</td>
<td>0.040</td>
</tr>
<tr>
<td>2393.50</td>
<td>4.212</td>
<td>0.151</td>
<td>0.031</td>
</tr>
</tbody>
</table>

Figure 6.1) General Frequency Trend
### 6.1.3 Anisotropic Behavior

Having established the general trend of the permittivity variation with frequency, attention was turned to permittivity variation with orientation. Figures 6.2a and 6.2b present a listing of permittivity calculated with respect to two directions, x and y, that are perpendicular to one another. Four sets of data were compiled corresponding to two boards (microstrip and stripline) in both the x and y directions. The resonant lines are again 100 mils wide.

#### X MICROSTRIP

<table>
<thead>
<tr>
<th>F (MHz)</th>
<th>$\varepsilon_{\text{reff}}$'</th>
<th>$\varepsilon_\prime$''</th>
<th>loss tan</th>
</tr>
</thead>
<tbody>
<tr>
<td>504.50</td>
<td>3.792</td>
<td>0.169</td>
<td>0.045</td>
</tr>
<tr>
<td>1013.50</td>
<td>3.759</td>
<td>0.142</td>
<td>0.038</td>
</tr>
<tr>
<td>1527.00</td>
<td>3.725</td>
<td>0.130</td>
<td>0.035</td>
</tr>
<tr>
<td>2029.25</td>
<td>3.750</td>
<td>0.157</td>
<td>0.042</td>
</tr>
<tr>
<td>2551.00</td>
<td>3.708</td>
<td>0.179</td>
<td>0.048</td>
</tr>
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</table>

#### Y MICROSTRIP

<table>
<thead>
<tr>
<th>F (MHz)</th>
<th>$\varepsilon_{\text{reff}}$'</th>
<th>$\varepsilon_\prime$''</th>
<th>loss tan</th>
</tr>
</thead>
<tbody>
<tr>
<td>503.75</td>
<td>3.803</td>
<td>0.193</td>
<td>0.050</td>
</tr>
<tr>
<td>1006.00</td>
<td>3.815</td>
<td>0.142</td>
<td>0.037</td>
</tr>
<tr>
<td>1519.50</td>
<td>3.762</td>
<td>0.145</td>
<td>0.039</td>
</tr>
<tr>
<td>2027.75</td>
<td>3.756</td>
<td>0.153</td>
<td>0.041</td>
</tr>
<tr>
<td>2536.75</td>
<td>3.750</td>
<td>0.163</td>
<td>0.043</td>
</tr>
</tbody>
</table>

*Figure 6.2a) Microstrip Anisotropic Data*
### X STRIPLINE

<table>
<thead>
<tr>
<th>F (MHz)</th>
<th>$E_r'$</th>
<th>$E_r''$</th>
<th>loss tan</th>
</tr>
</thead>
<tbody>
<tr>
<td>474.50</td>
<td>4.287</td>
<td>0.203</td>
<td>0.047</td>
</tr>
<tr>
<td>950.50</td>
<td>4.273</td>
<td>0.179</td>
<td>0.038</td>
</tr>
<tr>
<td>1432.50</td>
<td>4.233</td>
<td>0.182</td>
<td>0.043</td>
</tr>
<tr>
<td>1907.75</td>
<td>4.243</td>
<td>0.168</td>
<td>0.040</td>
</tr>
<tr>
<td>2393.50</td>
<td>4.212</td>
<td>0.161</td>
<td>0.038</td>
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</table>

### Y STRIPLINE

<table>
<thead>
<tr>
<th>F (MHz)</th>
<th>$E_r'$</th>
<th>$E_r''$</th>
<th>loss tan</th>
</tr>
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<tbody>
<tr>
<td>473.75</td>
<td>4.300</td>
<td>0.204</td>
<td>0.047</td>
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<tr>
<td>950.50</td>
<td>4.273</td>
<td>0.182</td>
<td>0.043</td>
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<tr>
<td>1434.00</td>
<td>4.224</td>
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<tr>
<td>1911.50</td>
<td>4.226</td>
<td>0.159</td>
<td>0.038</td>
</tr>
<tr>
<td>2392.75</td>
<td>4.215</td>
<td>0.160</td>
<td>0.038</td>
</tr>
</tbody>
</table>

Figure 6.2b) Stripline Anisotropic Data

The data presented indicates that a directional dependence with respect to an x or y direction in the plane of the board is negligible at these frequencies. At much higher frequencies this type of dependence may have more of an effect.

### 6.2 INSIGHT INTO THE METHOD

Further insight is given into the application of the Resonant Cavity method. The importance of the manner of data acquisition is investigated. Also, the separation of loss terms is addressed.

### 6.2.1 Data Acquisition

S-parameter data taken by a network analyzer can be output raw or corrected. Methods of improving raw data output include reducing the IF (intermediate frequency) bandwidth, averaging over several frequency sweeps, or smoothing over a frequency window (a percentage of the sweep). The data in Figure 6.3 illustrates the effect of these data improvement techniques on final permittivity calculations. A reference calculation is made on a microstrip board for a 100 mils line with an IF bandwidth of 3000 Hz.
Since the data above does not vary for at least two significant digits, the calculations from raw data for the permittivity in sections 6.1.2 and 6.1.3 appear to be reasonable. While the accuracy of the Resonant Cavity method in general is still to be quantified, the transition from data acquisition to permittivity calculations does not seem to introduce a major source of error.

### 6.2.2 Q Factor and Loss

The loss tangent for transmission line resonators has been related (see section 4) to three components $Q_r$ (radiation), $Q_d$ (dielectric), and $Q_c$ (conductor). In an effort to separate these components, measurements were taken from three structures. Two stripline resonators of different lengths were compared to determine conductor loss. Loss due to radiation should be nonexistent due to the shielding ground planes inherent in stripline. Then a microstrip line and a stripline of the same length were compared to locate any radiation loss in the microstrip. Here conductor loss is held constant. Figure 6.4 presents the results.
The data indicates that the radiative loss for microstrip can be neglected. Additionally, the conductive loss can be neglected for both microstrip and stripline loss tangent calculations. An important conclusion that can be drawn from this data is that the measured Q factor of these resonators is dominated by the loss due to the dielectric material. In other words, the calculated loss tangent of the resonant system is the loss tangent of the PCB dielectric.

7. CONCLUSIONS

This document reviews current techniques for measuring the complex permittivity of PCB laminates at high (rf and microwave) frequencies. A brief summary is given in section 7.1. Section 7.2 concludes with recommendations.

7.1 Summary

Four major categories of techniques were presented. These methods included Resonant techniques, Reflection/Transmission methods, TDR, and Length Comparison. Of the various methods described, the Resonant Cavity was chosen as a point of initial inquiry. It was appealing for its simplicity. It was one of the best methods suited for measuring anisotropic effects. The Resonant Cavity method would provide information concerning both parts of the complex permittivity, and a reasonable frequency range could be covered with six test structures.

Upon choosing the Resonant Cavity technique, general equations were derived relating the real and imaginary parts of the complex permittivity to physical parameters and the resonant frequency. Test boards were designed and several measurements were taken.

7.2 Discussion

The Resonant Cavity method was a good choice to begin dielectric study. It was discovered that FR4 (the laminate used for these preliminary results) can be considered isotropic in the plane of the laminate over the frequencies .5 to 2.5 GHz. The effective dielectric constant was determined to be approximately 3.8 for microstrip (Er for stripline was 4.2). Variation with frequency is detectable, but is not drastic. The loss tangent was calculated to be about 0.04. Surprisingly, the Q factor was dominated by Qd. Overall the measured values are reasonably close to the expected values discussed in section 6.1.
Having obtained this information, it is recommended that alternate methods be tested for verification of this data. The Metal-Clad Laminate test would be the best indicator of the accuracy of the microstrip and stripline results. Additionally, the Coaxial Resonator method should be tested to investigate the effect of the horizontal radial components of the fringing field on permittivity. If there is no significant effect, this method may be used in place of the Resonant Cavity method.

Finally, the TDR and Length Comparison methods should be investigated. The TDR method provides wide bandwidth permittivity data with very few measurements. A measurement cell must be designed for a PCB sample, and some software must be written to solve transcendental equations. The Length Comparison method is so simple, it too deserves investigation.

8. REFERENCES

Perturbation


Dielectric Resonators


Coax Resonance


Waveguide


Metal Clad Laminates


**General Cavities**


**Strip Structures**


Transmission Line


Coaxial Lumped Capacitance


Variable Impedance


Time Domain Reflectometry


Electrical and Physical Length


ABSTRACT

This paper presents methods of modeling digital devices using macromodels. The paper presents macromodel examples and introduces development of one-port and two-port macromodels using measurement techniques. This paper is a product of the project entitled "Propagation of High Speed Digital Signals in Printed Circuit Board Systems" funded by Bell Northern Research through the University Interactions Program with North Carolina State University.
INTRODUCTION

As the demand for higher clock frequencies in digital systems increases, the correct design of printed circuit boards (PCBs) becomes a crucial step in overall system performance. Impedance mismatches on transmission lines cause ringing and propagation delays, which deteriorates overall PCB performance. Consequently, if the interconnections of a PCB could be modeled, then overall performance could be estimated and improved. One step in the modeling process is determining how digital devices behave when interconnected on a PCB. The input and output characteristics of the digital device determine the termination characteristics.

One goal of this project is to develop a macromodel of digital devices. The macromodel should characterize the input and output characteristics, as well as the delay and switching characteristics of the device. Because a digital device is nonlinear, the model for the input and output characteristics should consist of nonlinear circuit elements.

This paper presents methods of modeling digital devices by using macromodels. It also introduces approaches for incorporating these macromodels into a computer simulation program to simulate overall PCB performance.
I. GENERAL

A macromodel is a simplified model representing the internal and external characteristics of a complex system or device. The macromodel consists of simplified equations and/or an equivalent component level model which describes the static and dynamic characteristics to the same degree of accuracy as the original system or device [1]. Macromodeling is a technique to develop a macromodel based on analytical formulation of the input and output characteristics of a system or device [2].

Hsieh and Rabbat define five types of macromodels [9]:

1) Circuit Reduction Macromodel

The circuit reduction macromodel consists of a circuit which is simpler than the original circuit. This macromodel can be obtained in two ways:

a) Replacing the original circuit components one at a time with short or open circuits until the input and output characteristics of the original circuit deviates more than the error limits.

b) Using the sensitivity approach. The dominant components for the original circuit are found using sensitivities of the original circuit. These dominant components are used to develop the macromodel. The number of components used depends on the accuracy required.

2) Circuit Behavior Macromodel

The circuit behavior macromodel represents the external characteristics of the original circuit. The macromodel is characterized by input and output impedance, delays, and terminal circuit properties. Internal elements of the macromodel may not resemble the original circuit or may have little physical significance.

3) Table Behavior Macromodel

The table behavior macromodel uses a numerical table to represent the original
circuit. A table stores all the circuit input and output characteristics for various input and loading conditions. The numeric entries are either derived from data or from actual hardware measurements. In table look-up form, the macromodel is easily automated for computer simulation.

4) **Mathematical Macromodel**

The mathematical macromodel consists of using various mathematical techniques to represent the circuit components. For example, differential equations or polynomials may represent a controlled source or a nonlinear element. A probability density function may simulate the input/output propagation delays on various voltage levels. Developing macromodels using this technique requires intimate knowledge of the system's behavior.

5) **Symbolic Macromodel**

The symbolic macromodel is obtained by symbolic manipulations of the original subnetwork. Examples of symbolic elimination are matrix formulation and ordering, Gaussian elimination, and forward substitution. An example of a symbolic macromodel is the function-oriented symbolic macromodel (FOSM).

6) **Combination of Macromodel Types**

In general a macromodel may consist of several different model types. For example, a digital logic circuit can be represented by two macromodel types:

a) a table macromodel to represent the input and output characteristics of the device, and

b) a function symbolic macromodel to represent the remaining components in the device.

Keeping the macromodel as general as possible results in a savings in computer storage and computational time.

In summary, Ruehli, Rabbat, and Hsieh present several macromodeling approaches, techniques, and means of analysis in Figure 1.1 on page 5.
Frolkin, Tikhomirova, and Moshnyaga define five levels of accuracy which describes the dynamic process in developing macromodels for digital devices [9]:

1) Modeling the mean propagation delay.
2) Modeling the switch-on and switch-off delays.
3) Modeling the dependence of the propagation delay and switch-on and switch-off delays in relation to the loads on each output and the duration of the transients at the input.
4) Modeling the duration of the fall and rise of the output signal.
5) Modeling the complete initial circuit of the device.

II. MACROMODELING EXAMPLES

A. TTL NAND Gate

This section presents three examples of NAND gate models. The NAND gates are two input, positive logic devices. The macromodels model the input, output, and internal characteristics of the gate.
The Bakhov model is shown in Figure 2.1. The model consists of three stages:

1) Input stage
   Logic operation, input characteristics

2) Middle stage
   Propagation delay, transition times

3) Output stage
   Output characteristics

Nonlinear current sources $J_A$ and $J_B$ and capacitances $C_A$ and $C_B$ model the input characteristics of the device. The AND function is performed by taking the minimum of the input signals. This allows expansion of the macromodel into multiple inputs.

The voltage source $V_{MIN}$, resistance $R_1$, and macrocapacitance $W_1$ model the propagation delay of the gate. The macrocapacitance $W_1$ is defined as follows:

$$C_w = \begin{cases} f_1(V) & \text{for } dV/dt < 0 \\ f_2(V) & \text{for } dV/dt > 0 \end{cases}$$

where: $V$ is the voltage across the macrocapacitance, which is a controlled voltage source $E(V)$. Assuming the delay in switching from logic 0 to logic 1 and logic 1 to logic 0 are equivalent, a macrocapacitance $W_1$ is used, which depends on the derivative of the voltage with respect to time.

The voltage source $E_2$, resistance $R_2$, and macrocapacitance $W_2$ model the transfer characteristic and the transition times of the gate. The macrocapacitance $W_2$ models the different values of the output signal edges when switching from logic 0 to
logic 1 and from logic 1 to logic 0.

The voltage source $E_z$, resistance $R_z$, capacitance $C_z$, and nonlinear current source $J_z$ model the output characteristics of the device. The voltage source $E_z$, which is a function of $W_z$, decouples the input from the output of the macromodel.

To increase the accuracy of the model, Bakhov suggests incorporating nonlinear capacitances and nonlinear current sources, controlled by two voltages, at the input and output of the model.

ii) Greenbaum Model [5]

The Greenbaum model along with its computer program listing is shown in Figure 2.2 on page 8. The computer program listing is written in SCEPTRE and CIRCUS-2 languages. The model consists of three stages:

1) Input stage
   Input characteristics

2) Middle stage
   Logic state, propagation delay

3) Output stage
   Transfer characteristics, output characteristics

Input stage:

Current sources $J_a$ and $J_b$ model the input characteristics of the gate. The current sources are zero-valued, which implies an infinite input impedance. This is a good first-order approximation, since the input impedance for a NAND gate is in the kilo-ohm region. For increased accuracy, Greenbaum suggests modeling current sources $J_a$ and $J_b$ in diode-equation format or as tables of current as a function of applied voltage.

Middle stage:

Dependent voltage source $E_z$ establishes the logic state of the gate. If either of the input signals is less than or equal to 0.8 V (maximum logic 0 input voltage), then $E_z$ is set to 3.1 V (maximum logic 1 output voltage). If both input signals are equal to or
FOR SCEPTRE: \(E_1 = f(FN2), C_1 = f(FCAP1), E_2 = f(VC1)\)
FOR CIRCUS-2: \(V_1 = f(FN2), R_1 = f(RR72), V_2 = f(VC1)\)

**SCEPTRE DESCRIPTION**

**MODEL LOO (A-B-OUT-GND)**

2 INPUT NAND GATE

\[ \begin{align*}
A &= \text{INPUT A} \\
B &= \text{INPUT B} \\
E_1, \text{GND-1} &= Q_4(V_{JA}, V_{JB}, 0.8, 3.1, 1.9, 0.3) \\
R_1, 1-2 &= 100 \\
C_1, 2-\text{GND} &= Q_2(E_1, E_2, 550.5 \cdot 10^{-12}, 300.5 \cdot 10^{-12}) \\
E_2, \text{GND-3} &= X_1(VC_1) \\
R_2, 3-\text{OUT} &= 30 \\
\text{FUNCTIONS} \\
Q_2(A, B, C, D) &= (FCAP1 (A, B, C, D)) \\
Q_4(A, B, C, D, E, F) &= (FN2 (A, B, C, D, E, F)) \\
\text{OUTPUTS} \\
V_{JA} (A \text{ IN}), V_{JB} (B \text{ IN}), V_{JO} (\text{OUTPUT}), PLOT
\end{align*} \]

**CIRCUS-2 DESCRIPTION**

**MODELS**

**MODEL NAME = NAND GATE**

**EXTERNAL NODES = (A, B, OUT, GND)_**

**TOPOLOGY**

\[ \begin{align*}
JA, A, \text{GND} &= 0 \\
JB, B, \text{GND} &= 0 \\
JO, \text{OUT-GND} &= 0 \\
E_1, \text{GND-1} &= Q_4(V_{JA}, V_{JB}, 0.8, 3.1, 1.9, 0.3) \\
R_1, 1-2 &= 100 \\
C_1, 2-\text{GND} &= Q_2(E_1, E_2, 550.5 \cdot 10^{-12}, 300.5 \cdot 10^{-12}) \\
E_2, \text{GND-3} &= X_1(VC_1) \\
R_2, 3-\text{OUT} &= 30 \\
\text{FUNCTIONS} \\
Q_2(A, B, C, D) &= (FCAP1 (A, B, C, D)) \\
Q_4(A, B, C, D, E, F) &= (FN2 (A, B, C, D, E, F)) \\
\text{OUTPUTS} \\
V_{JA} (A \text{ IN}), V_{JB} (B \text{ IN}), V_{JO} (\text{OUTPUT}), PLOT
\end{align*} \]

**DEVICE NAME = LOO, MODEL NAME = NAND GATE**

**SINGLE VALUED PARAMETERS**

\[ \begin{align*}
C_1 &= 100E-12, A1 = 550, A2 = 300, A3 = 0.8, A4 = 3.1 \\
A5 &= 1.9, A6 = 0.3, JA = 0, JB = 0, JO = 0, R2 = 30
\end{align*} \]

**MODEL SUBROUTINES**

1. CFN2 QUAD 2 INPUT NAND GATE LEVEL SELECT
2. CFN2 FOR USE WITH 2 INPUT NAND GATE
3. CFN2 FUNCTION FN2(A, B, C, D, E, F)
4. CFN2 A = VJA B = VJB C = 0.8
5. CFN2 D = 3.1 E = 1.9 F = 0.3
6. IF (A .LE. B .OR. B .LE. C) GO TO 4
7. IF (A .GE. B .AND. B .GE. C) GO TO 5
8. FN2 = D - AMIN1(A, B)
9. RETURN
10. 4 FN2 = D
11. RETURN
12. 5 FN2 = F
13. RETURN
14. END

1. CFCAPI DIGITAL IC CAPACITOR SELECT
2. CFCAPI FUNCTION FCAP1(A, B, C, D)
3. CFCAPI TO ESTABLISH CAPACITOR VALUE OF IC
4. FCAP1 = C
5. IF (A .GE. B) FCAP1 = D
6. RETURN
7. END

**Figure 2.2:** Two input NAND gate model with computer simulation programs (After [5])
greater than 1.9 V (minimum logic 1 input voltage), then $E_1$ is set to 0.3 V (maximum logic 0 output). If neither of these conditions exist, for example, if the input is in a transition state, then $E_1$ is set to 3.1 V minus the absolute value of the smaller of the two input signals. The subroutine FN2 calculates the value of $E_1$.

The resistor, $R_1$, and capacitor, $C_1$, model the propagation delays of the gate. The subroutine FCAP1 determines the value of capacitor $C_1$. $C_1$ is set at 550 pF, except when voltage $E_1$ is less than voltage $E_2$, then $C_1$ is set to 300 pF. With $C_1$ set at 550 pF and 300 pF, the propagation delays are 55 ns and 30 ns, respectively. In most cases the two propagation delays, low to high and high to low transitions, are not equal. Therefore, if alternate propagation delays are needed, then $C_1$ can be adjusted accordingly.

**Output stage:**

Voltage source $E_2$ establishes the transfer characteristics, i.e., the relationship between the input and output signals, of the gate. $E_2$ is a function of the voltage across capacitor $C_1$, which is a function of $E_1$. Therefore, $E_1$ and $E_2$ are related, and a relationship between the input and the output signals exists.

The resistor $R_2$ models the output characteristics of the device. $R_2$ is fixed at 30 ohms. This does not model the output characteristics accurately for all input and load conditions, but it does provide a first-order approximation for the output signal level. The zero-valued current source $J_0$ is a reference component which serves to monitor the output signal under various input and load conditions.

Greenbaum presents results showing agreement of the gate model with the actual gate response.

**iii) Glesner Model [8]**

The Glesner model is shown in Figure 2.3 on page 10. The model consists of three stages:

1) Input stage
   Input characteristics, logic operation
2) Middle stage
   Voltage transfer characteristics, transition times

3) Output stage
   Propagation delay, output characteristics

**Input stage:**

The current sources $J_A$ and $J_B$ model the input characteristics of the device. The current sources are nonlinear and depend on their respective input voltages. Glesner uses a table of values to represent each current source. The table of values can be implemented in a simulation program.

The input stage also models the logic operation of the device. Glesner defines a logic state parameter, PL, which performs the AND operation on the input signals:

$$PL = \text{MIN}(V_{JA}, V_{JB}).$$

The AND operation is equivalent to taking the minimum of all input signals. The logic state parameter simply allows expansion of the macromodel into multiple inputs by evaluating the MIN function on all input voltages.

**Middle stage:**

The voltage source $E_1$, resistor $R_1$, and capacitor $C_1$ model the transition times of the device. Glesner uses the voltage transfer characteristic of the gate to perform an inversion of the input signal. A table stores the voltage transfer characteristics of the gate. The table of values is assigned to the voltage source $E_1$. Thus, given an input
voltage, the corresponding voltage at $E$, represents a NAND function. The resistor $R$, and capacitor $C$, provide a low pass network, which simulates the transition times of the gate. The transition times are simulated in the model by assigning capacitor $C$, two capacitor values, one corresponding to the rising edge and one corresponding to the falling edge of the output signal.

The current source $J_o$ serves as a reference component for the dc analysis and transfers the output voltage of the low pass network to the output stage.

**Output stage:**

The voltage source $E_o$ models the average propagation delay of the gate. $E_o$ is a function of $V_{in}$, which is the voltage across current source $J_i$. The variable PDT represents the average of the two propagation delay times, $t_{PH}$ (low to high propagation delay) and $t_{HL}$ (high to low propagation delay). A FORTRAN subroutine simulates the delay function in the time domain. Values of $V_{in}$ are stored in a delay table at time $t_k$ ($t_k$ = time point of the $k$ integration step) and read out at time $t_k + PDT$.

The resistance $R_o$, capacitance $C_i$, and current source $J_o$ model the output characteristics of the device. Glesner uses a linearized version of the output characteristics simulated using SPICE. From the output characteristics, an output resistance $R_o$ and a positive and negative limitation PSP and PSN are computed. $R_o$, PSP, and PSN are all a function of the logic state parameter PL. The values of $R_o(PL)$, PSP(PL), and PSN(PL) are read from the simulated linearized characteristics and stored into three tables. The current $I_o$ through the output resistance $R_o$ controls the current generator $J_o$. If $I_o$ exceeds the current limitations PSP or PSN, then the current source $J_o$ increases or decreases linearly to hold the output current constant. $C_o$, which models the constant output capacitance of the gate, is fixed at 15 pF.

Glesner uses a three stage ring oscillator to test the transient response of the macromodel. The macromodel simulation and actual device measurements agree within five percent. Glesner also uses the macromodel to study the propagation of
digital signals on transmission lines. The test circuit consists of two NAND gates interconnected by a coaxial cable. To demonstrate the effects of ringing, two different characteristic impedances of the coaxial cable, 50 ohms and 240 ohms, are used in the simulation. The results agree well with laboratory measurements.

B. TTL Flip-Flop

Greenbaum and Miller present a macromodel of a TTL D-type flip-flop shown in Figure 2.4 on page 13. Program listings in SCEPTR and CIRCUS-2 languages are included with the model. The model consists of three stages:

1) Input stage
   Input characteristics

2) Middle stage
   Logic state, propagation delay

3) Output stage
   Transfer characteristics, output characteristics

Input stage:

Current sources \( J_o, J_{ns}, J_s, \) and \( J_{ck} \) model the input characteristics of the device. The current sources are zero-valued, which implies an infinite input impedance. As with the NAND gate, this also provides a good first-order approximation, since the input impedance for a flip-flop device is in the kilo-ohm region. For increased accuracy, Greenbaum and Miller suggest modeling current sources \( J_o, J_{ns}, J_s, \) and \( J_{ck} \) in diode-equation format or as tables relating current to applied voltage.

Middle stage:

Dependent voltage sources \( E_1 \) establishes the logic state of the device for output \( Q \). There are two conditions for establishing the voltage for source \( E_1 \):

1) Set or reset inputs are logic 0.
2) Set or reset inputs are logic 1.

If either the set or reset input signals are logic 0, then \( E_1 \) is set to logic 1. If either the
CIRCUS-2 DESCRIPTION

MODEL 9774 (CK-D-SET-RS-Q-QB-GND)
D FLIP FLOP

ELEMENTS
JCK, CK-GND = 0
JS, SET-GND = 0
JRS, RS-GND = 0
JD, D-GND = 0
JO, Q-GND = 0
JQB, QB-GND = 0
E1, GND-1 = Q1(VJS,VJRS,VJCK,VJD,TIME)
R1, 1-2 = 100
C1, 2-GND = Q2(E1,VC1,250,E-12,300,E-12)
E2, GND-3 = X1(3.1-E1)
R2, 3-4 = 100
C2, 4-GND = Q2(E2,VC2,250,E-12,300,E-12)
E3, GND-5 = X2(VC1)
R3, 5-Q = 100
E4, GND-6 = X3(VC2)
R4, 6-QB = 100
FUNCTIONS
Q1(A,B,C,D,E) = (FEI(A,B,C,D,E))
Q2(A,B,C,D) = (FCAP1(A,B,C,D))

OUTPUTS
VJO, VJOB, PLOT

MODEL SUBROUTINES

1 CFCEI D FLIP FLOP
2 FUNCTION FEID(VSET,VRESET,VCLOCK,VDRIVE,TIME)
3 C
4 C FOR USE WITH D FLIP FLOP
5 C VSET = VOLTAGE AT SET INPUT
6 C VRESET = VOLTAGE AT RESET INPUT
7 C VCLOCK = VOLTAGE AT CLOCK INPUT
8 C VDRIVE = VOLTAGE AT D-INPUT
9 C XCLOCK = VOLTAGE AT CLOCK INPUT DURING LAST COMP.
10 C XGEN = VOLTAGE AT GATE(E1) DURING LAST COMP.
11 C
12 IF(TIME.LE.0) XCLOCK = VCLOCK
13 IF(TIME.LE.0) XGEN = 3.0
14 IF(VSET.LE.1.2) GO TO 1
15 IF(VRESET.LE.1.2) GO TO 2
16 GO TO 3
17 3 IF(TIME.LE.0) XGEN = 3.0
18 IF(VCLOCK.LE.XCLOCK) GO TO 9
19 IF(VCLOCK.GE.0.8.AND.VCLOCK.LE.2.0) GO TO 4
20 9 FEI = XGEN
21 GO TO 10
22 4 IF(VDRIVE.GE.1.5) FEI = 3.0
23 IF(VDRIVE.LT.1.5) FEI = 0.1
24 GO TO 10
25 1 FEI = 3.0
26 GO TO 10
27 2 FEI = 0.1
28 10 XCLOCK = VCLOCK
29 XGEN = FEI
30 RETURN
31 END

1 CFCAP1 DIG IC CAP SELECT
2 FUNCTION FCAP1(A,B,C,D)
3 CFCAP1 TO ESTABLISH CAP VALUE FOR IC
4 FCAP1 = 0
5 IF(A.GE.0) FCAP1 = D
6 RETURN
7 END

Figure 2.4: TTL D-type Flip-Flop with computer simulation program (After [6])
set or reset is logic 1, then the subroutine FE1 controls the logic state.

The subroutine FE1 monitors the clock signal voltage to assure that the flip-flop triggers on the positive-going edge of the clock pulse, and that the clock signal voltage is in the correct range. Once these conditions are met, the subroutine FE1 assigns a voltage to source E, given an input signal at D. If the input signal at D is logic 1, then source E, is set to 3.0 V (logic 1). Likewise, if the input signal at D is logic 0, then source E, is set to 0.1 V (logic 0).

Dependent voltage source E, establishes the logic state of the device for output Q. Q, is the complement of output Q, therefore voltage source E, is calculated as 3.1 V minus the voltage of E,. For example, when E, is 3.0 V (logic 1), E, is 0.1 V (logic 0), and when E, is 0.1 V (logic 0), E, is 3.0 V (logic 1).

The resistor-capacitor combinations, R1-C1 and R2-C2, model the propagation delays of the respective outputs, Q and Q, of the device. Since the propagation delays for an increase and decrease in the output signal levels are not equivalent, the capacitors C1 and C2 are adjusted. The subroutine FCAP1 determines the capacitors C1 and C2. If voltage source E, or E, is greater than or equal to its respective output signal voltage Q or Q, then C1 and/or C2 are set to 300 pF. Otherwise, if E, or E, is less than its respective output signal voltage Q or Q, then capacitor C1 and/or C2 are set to 250 pF.

Voltage sources E3 and E4 establish the transfer characteristics for the respective outputs of the device. The voltage source E3 determines the voltage across capacitor C1. Voltage source E4, which is a function of the voltage across capacitor C2, determines the output at Q. Likewise, voltage source E5, which is a function of the voltage across capacitor C2, determines the output at Q, Therefore, a direct relationship between the input and output signals exist.

Output stage:

Resistors R3 and R4 model the output characteristics for the respective outputs, Q
and $Q_3$, of the device. $R_3$ and $R_4$ are fixed at 100 ohms. This does not model the output characteristics accurately for all input and load conditions, but it does provide a first-order approximation for the output signal level. The zero-valued current sources $J_e$ and $J_o$ are reference components which serve to monitor the output signal under various input and load conditions.

C. SUMMARY

The macromodel examples model the following characteristics:

1) The input and output characteristics of the device
2) The logic operation of the device
3) The propagation delay of the device
4) The transition times of the device

A comparison of the macromodel examples in relation to the four characteristics follows.

Nonlinear components provide an accurate model of the input characteristics of the device. The nonlinear current source in Glesner's model satisfactorily models the input characteristics. Although, Bakhov's model with a nonlinear current source and a shunt nonlinear capacitance more accurately models the input characteristics.

Nonlinear components should also model the output characteristics. Bakhov suggests a series resistance with a shunt nonlinear current source and a shunt nonlinear capacitance. Glesner suggests a series nonlinear resistance with a shunt nonlinear current source and a shunt capacitance. Either output structure would provide reasonable accuracy. A combination of both output structures, a series nonlinear resistance with a shunt nonlinear current source and a shunt nonlinear capacitance, would provide even better accuracy.

Either the voltage transfer characteristics or a subroutine can model the logic operation of the device. Using the voltage transfer characteristics of the device to model the logic operation provides an accurate method of modeling the NAND gate. For the flip-flop, Greenbaum and Miller use a subroutine to compute the logic operation of the
device. Incorporating the voltage transfer characteristics into the subroutine would provide a more accurate model of the logic operation of the flip-flop.

A voltage source, resistor, and capacitor network model the transition times of the devices. A subroutine can vary either the resistance or the capacitance to simulate the different transition times. Greenbaum does not model the transition times for the NAND gate or the flip-flop.

Either a resistor, capacitor network or a delay subroutine can model the propagation delay of the devices. Glesner's delay subroutine may provide more accuracy than a resistor, capacitor network.

With a slight modification of the input and output structures, Glesner's macromodel best simulates the NAND gate. His techniques can be expanded to model other devices as well.

III. DEVELOPING MACROMODELS OF DIGITAL DEVICES

The objectives of this project are as follows:

1) Develop complete macromodels for various digital devices.

2) Develop a database library of the macromodels.

3) Incorporate the library of macromodels into a transmission line simulator.

One-port Models:

The first step is to develop macromodels of digital devices using measurement techniques. One-port measurements yield the input and output characteristics of the device. Possible one-port macromodels are shown in Figure 3.1 on page 17. A series inductor with a nonlinear shunt capacitor, nonlinear shunt resistor, and shunt current source model the input and output characteristics of the device. The inductor represents the lead inductance of the device package. These macromodels of the input and output characteristics are similar to the macromodel examples presented
Measurement techniques can be used to calculate the individual components of the macromodel. The nonlinear resistance is calculated from the I-V curves of the device. The inductance and nonlinear capacitance are calculated from frequency measurements using a network analyzer. The current source is calculated from the initial state of the device.

![Diagram of one-port macromodels](image)

**Figure 3.1:** One-port macromodels of digital devices

**Two-port Models:**

Two port measurements yield the internal characteristics of the device, such as transition times and propagation delays. A model incorporating Glesner's techniques could be used to model the internal characteristics of the device. A possible two-port model is shown in Figure 3.2.

![Diagram of two-port macromodels](image)

**Figure 3.2:** Two-port macromodels of digital devices

After developing the macromodel, a library database stores the models in the form of look-up tables. The libraries can be implemented in a transmission line simulator to model the effects of high speed digital signals on printed circuit boards.
CONCLUSION

This paper presented several macromodeling examples and discussed a procedure for developing macromodels of digital devices using measurement techniques. The macromodel examples provided techniques to model the input and output characteristics and the internal characteristics of devices. The macromodels are easily simulated using circuit simulation programs such as SPICE or SCAMPER. Examples of simulation were presented in Greenbaum's models of a NAND gate and a D-type flip-flop. The examples have proved helpful in developing macromodels of digital devices, and future work will be based on the ideas presented here.
BIBLIOGRAPHY


Guidelines for Developing Macromodels of Digital Devices Using Measurement Techniques

Approach:
In order to develop a complete macromodel, two measurement techniques are needed:

1) One-port measurements
   * Input and output characteristics of the device

2) Two-port measurements
   * Internal characteristics of the device
     > Logic operation
     > Transition times
     > Propagation delay

The one-port macromodels are shown in Figure 1.1. The inductor represents the lead inductance of the device packaging. The nonlinear resistor can be calculated from the I-V curves of the device. The inductor and nonlinear capacitor can be calculated from S-parameter measurements using a network analyzer.

![Figure 1.2: One-port macromodels of digital devices](image)

One possible approach in developing a macromodel of the internal characteristics of the device is the use of a unit load representation. This approach is shown in Figure 1.2 on page 2. The unit loads are adjusted to provide different loads at the input and output of the device. To determine if the input and output of the device is coupled, S-
parameter measurements are taken for the various loads. The two-port characteristics of the device are determined by de-embedding the unit loads from the S-parameter measurements.

Another approach at developing a macromodel of the internal characteristics of the device is to use the techniques presented by Glesner for his NAND gate macromodel. Although, the accuracy of this model under all input and load conditions is questionable.

Theories to be tested:

1) Impedance characteristics of input and output ports
2) Coupling from the input to the output
3) Effects of various packaging on one-port models
4) Effect of noise reduction techniques on one and two port models

Theories not to be tested:

1) Crosstalk between inputs
2) Temperature effects
3) Hysteresis of devices

Test board setup:

1) Devices to be tested
   a) Buffer/Drivers
      * Standard
      * Tri-state
b) Inverters
c) Multiple input NAND gates
d) Flip-flops

2) Device technologies
   a) AS TTL
   b) ALS TTL
c) FAST TTL
d) S TTL
e) AC
f) HC
g) ECL
h) GaAs

3) Packaging
   a) Surface mount
   b) Dual in line (DIP)
c) Zig-zag in line (ZIP)

4) Noise considerations
   a) Ferrite beads
      * Used to reduce noise on power supply line.
b) Decoupling capacitors
      * Used to reduce noise to power supply and provide on demand current for device.
      * Capacitors can be placed either horizontally or vertically on board.
c) Unused inputs
      * Test devices with unused inputs terminated (ground or load).
      * Test devices with unused inputs floating.
5) Two-port measurements
   a) Effect of unit load on device characteristics.
   b) Develop technique to remove unit load from S-parameter measurements.

Procedure for test board design:

1) Identify all components.
2) Use IEDB to locate components with their codes.
3) Use FUNDES to capture design.
4) Conduct design review.
5) Incorporate changes from design review.
6) Schedule board kickoff meeting.
7) Review layout, send board to be manufactured.

Device Testing:

After completion of the test board, device testing can begin. Developing one-port macromodels will be the primary concern. The one-port macromodels can be used in a transmission line simulator such as TRANSIM or SCAMPER. After developing and testing one-port macromodels, ideas for two-port macromodels can be tested.
Simulation of Complex Coupled Transmission Line Systems with Non-Linear Digital Device Termination

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ABSTRACT

A numerical method for determining the transient response of arbitrarily complex transmission line systems is presented. The technique convolves a time domain Green's function with the voltage/current characteristics of experimentally developed macromodels of terminating digital devices. This paper compares experimental results to analytical results and discusses the problems of stability, convergence, and numerical calculus.

MAJOR CONTRIBUTIONS

1) Arbitrarily complex topology of coupled transmission line systems (not just uniformly coupled lines).

2) Large signal macro-models of digital devices as sources and loads.

3) Lossy and coupled transmission lines.

4) Development of time domain Green's function approach.

5) Numerical stability and accuracy are discussed.
INTRODUCTION

Performance of digital printed circuit boards (PCB) systems are currently limited by transmission line effects such as delay, coupling, dispersion, losses, and impedance mismatch. Numerical simulation as an aid in design requires efficient simulation of transmission lines coupled with analysis of non-linear device terminations.

The basic simulation problem of transmission lines terminated by non-linear devices is that transmission line effects are best solved in the frequency domain, while voltage and current through a non-linear device can only be solved in the time domain. This problem is addressed in this paper by presenting a numerical technique that convolves the time domain Green's function with the voltage/current characteristics of experimentally developed macromodels of digital devices.

The time domain Green's function is a matrix function with each element being the impulse response of the system at one node. The impulse response is derived from experimentally determined frequency domain scattering parameters.

This method has been implemented on a computer and the analytical results are compared against experimental results.

BACKGROUND

Other papers have addressed various aspects of the problem of solving the complex transmission line systems and solving transmission lines terminated with non-linear loads.

Gupta, Garg, and Bahl[1] provided an analytical solutions for microstrips and coupled microstrips, but his work stopped short of providing an analytical solution for vias or coupled lines with discontinuities. While, Gupta's work addressed the solution to the physical characteristics of microstrips, it was not intended to provide a solution of signal propagation in these complex networks.

Schutt-Aine and Mittra[2] provided a time domain solution to a single conductor terminated with digital devices. This work is based on a scattering parameter approach and thus is applicable to uncoupled lines with complex discontinuities. Furthermore, this work uses a simplistic model for digital devices.

Djordjevic, Sarkar, and Harrington[3] developed a technique based on the Green's function for multi-conductor lines. The technique developed by Djordjevic is extended in this paper. Djordjevic's paper is limited because it did not address termination of transmission lines with reactive devices. Both Djordjevic and Schutt-Aine's work did not address the problems of numerical convergence or of numerical calculus.
METHOD

The method of simulating transmission lines with nonlinear termination utilizes non-linear macromodels of digital devices and a time domain green's function description of the transmission lines as shown in figure 1.

![Figure 1 Complex transmission line system terminated with digital devices](image)

MACROMODELS OF DIGITAL DEVICES

In general, the termination of digital devices may be modeled as shown in figure 2.

![Figure 2: Model of digital device](image)

The symbol $R[\ ]$ indicates that the current through the resistive element is a non-linear function of the applied voltage. For resistive elements the following constitutive relationship is used[4].

(1) \[ R_i[V_{i1}-V_{A_i},J_{R_i}]=0 \]

Here $R[\ ]$ is a monotonic, continuous, and differentiable function of current in terms of voltage.

The symbol $C[\ ]$ indicates that the charge of the capacitive element is a non-linear function of the applied voltage. For capacitive elements it is best to introduce charge as an additional variable to separate the constitutive relationship from the differential equation. Thus:

(2a) \[ C_i[V_{A_i},Q_{C}]=0 \]
Here $C(\cdot)$ is a monotonic, continuous, and differentiable function of charge in terms of voltage.

The inductor is linear for digital devices. Thus:

$$I_L = \frac{1}{L_i} \int_0^t (V_{ai} - V_i) dt$$

### DEVELOPMENT OF TIME DOMAIN GREENS FUNCTION

The solution to the system shown in figure 1 is the solution to the node voltages $(V_1, V_2, V_3, ..., V_N)$ for arbitrary inputs $(V_{i1}, V_{i2}, V_{i3}, ..., V_{iN})$.

In order to incorporate arbitrarily complex transmission lines, this paper proposes the development of a library of measured scattering parameters for PCB sub-structures (lines, bends, vias, coupled lines, etc.). To find the frequency domain behavior of a complex system, the scattering parameters of each sub-structure are transformed into $T$-parameters, cascaded, and transformed back to $S$-parameters.

For a transmission line system in a linear media, a frequency domain Green's function can be defined in terms of the Scattering parameters. The Green's function is the response at each node $j$ to a unit impulse excitation at node $i$.

$$G_{ij}(\omega) = \begin{cases} 
0.5(1 + S_{ij}(\omega)) / \Delta & \text{for } i=j \\
0.5S_{ij}(\omega) / \Delta & \text{for } i \neq j 
\end{cases}$$

where $\Delta t$ is the time step used in the numerical convolution.

The time domain Green's function can be found by taking the inverse Fourier transform of the frequency domain Greens function. The general response of a transmission line system with arbitrary source and a known reference impedance, as shown in figure 3, can be found.

![Figure 3: N-port transmission line system with reference termination](image-url)
The solution at each port is the summation of the convolution of the Green's function an EMF source

\[
V_1(t) = G_{11}(t)\cdot V_{i1}(t) + G_{21}(t)\cdot V_{i2}(t) + \ldots + G_{N1}(t)\cdot V_{iN}(t)
\]
\[
V_2(t) = G_{12}(t)\cdot V_{i1}(t) + G_{22}(t)\cdot V_{i2}(t) + \ldots + G_{N2}(t)\cdot V_{iN}(t)
\]
\[
V_3(t) = G_{13}(t)\cdot V_{i1}(t) + G_{23}(t)\cdot V_{i2}(t) + \ldots + G_{N3}(t)\cdot V_{iN}(t)
\]
\[
\vdots
\]
\[
V_N(t) = G_{1N}(t)\cdot V_{i1}(t) + G_{2N}(t)\cdot V_{i2}(t) + \ldots + G_{NN}(t)\cdot V_{iN}(t)
\]

(5)

Development of System of Equations

To remove the reference impedance from the system a negative reference impedance can be placed in series between the non-linear device and the reference impedance. This creates a virtual short circuit between the load and the transmission network as shown in figure 4.

By using the compensation theorem, the circuit shown in figure 4 can be separated, as shown in figure 5, into a linear convolution equation and a set of non-linear termination equations.
The system can be represented by the following set of equations for each port:

(6a) \[ R \left[ V_{n_i} - V_{A_i}, I_{R_i} \right] = 0 \]
(6b) \[ C \left[ V_{i}, Q_{c} \right] = 0 \]
(6c) \[ I_{c_i} = \frac{dQ_{c}}{dt} \]
(6d) \[ k_i \cdot I_{C_i} \cdot \frac{1}{I_i} \int_{0}^{t} (V_{A_i} - V) dt = 0 \]
(6e) \[ \frac{1}{L_i} \int_{0}^{t} (V_{A_i} - V) dt + \frac{1}{Z_{ref}} (V_i - V_{V_i}) = 0 \]
(6f) \[ V_i - \sum_{j=0}^{N} G_{ji} V_{v_j} = 0 \]

Equation 6a can be estimated from the I/V diagrams in the data books for the digital device of interest. In general the input to a digital device has a single I/V curve, while the output of a digital device will have a separate curve for the logic 1 and logic 0 states.

Equation 6b can be estimated from the charge associated with a reverse biased diode with gradient diffusion.

The derivative of equation 6c can be estimated using a finite difference method,

(7) \[ \frac{dQ_c}{dt} = \frac{Q_c(t) - Q_c(t-1)}{\Delta t} \]

The integration of equation 6d and 6e can be estimated by using the trapezoidal rule.
\[
\int_0^t [V_{A_i}(t) - V_{i(t)}] dt = \frac{1}{2} \Delta t \sum_{p=0}^q \left[ X_i(p) - X_i(p+1) - Y(p) + Y(p+1) \right]
\]

And finally, the convolution of equation 6f can be estimated using Simpson's rule:

\[
G_{ji} \ast V_{vj} = \int_0^t G_{ji}(t-\tau)V_{vj}(\tau) d\tau = \sum_{p=0}^q G_{ji}(q-p)V_{vj}(p) \Delta t
\]

The system of equations can be solved using a Newton-Raphson method expanded to multi-dimensions. The Jacobian matrix used in this method is generally sparse. An iterative solution to the Jacobian matrix produces the next iteration faster than a direct method (such as Gaussian elimination and backward substitution) for systems of six or more ports.
RESULTS

A coupled transmission line structure terminated with FAST devices was simulated. Figure 6 illustrates the analytic results obtained for a 10 MHz clock. Experimental measurements are currently being performed and will be included in the full manuscript.

![Figure 6: Analytic Results](image)

CONVERGENCE, STABILITY, ACCURACY

Provided the step size ($\Delta t$) is chosen small enough, the solution will generally converge. The point were the solution may not converge is around the point where the cut-off diode of the input devices becomes forward biased. A further reduction of the step size generally improves convergence around this point. However, there are problems associated with a small values of $\Delta t$ which include:

- Use of double precision numbers for calculations
- Long execution time
- Round off errors due to very small numbers
- Large memory requirements
- Increased cumulative errors

In general the derivative in equation 7 is the most error prone portion of the numerical method. Reducing the value of $\Delta t$ generally improves the accuracy of the derivative but may reduce the accuracy of the overall solution.

Finally, the inverse Fourier transform required to produce the time domain Green's function generally introduces aliasing errors due to finite bandwidth of the
S-parameters. The larger the bandwidth, the smaller the aliasing errors. The aliasing errors can also be reduced by windowing the Green's function in the time domain. Windowing involves setting the Green's function to zero at all known zero points.

CONCLUSION

A numerical technique to solve arbitrarily complex transmission line system terminated with digital devices is presented. This technique convolves the time domain Green's function with the voltage/current characteristics of macromodels of digital devices. The time domain Green's function is derived from measured Scattering parameters. The macromodels of digital devices is derived from measured data. Good agreement was obtained between simulated and preliminary experimental results.
REFERENCES


This is a report on the state-of-the-art of table look-up techniques. The report covers table-based modeling of MOSFETs in detail as the most sophisticated modeling of this type has been in this area. However many of the concerns and solutions are also applicable to table-based modeling of distributed structures found on printed circuit boards.
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1 Introduction

Circuit simulation techniques, which are marked "third generation" in that they go beyond time integration approach, have rejected one or more of those principal features in their quest for size and speed capabilities commensurate with the requirements of the VLSI era. Circuit simulator, which matured in 1970's, has established itself as a significant design aid and a significant cost item as well, in most large integrated circuit (IC) design houses [25].

Computer design tools and methodologies have become an important part of integrated circuit design. Advances in simulation technology now allow the design of complex integrated circuits containing hundreds of thousands of transistors. As a result, IC designers face a major obstacle posed not by technological limitations, but by the tremendous time and effort required to fully utilize these technologies. Computer design tools along with improved modeling capability can provide the design average necessary to reduce design time and improve the probability of successful first-silicon.

Much effort has been devoted to developing design methods for analog and digital VLSI, resulting in methodologies such as analytical and numerical analysis. The common theme is that the systems being designed take too much CPU time and/or too much storage for economically realistic simulation support for the design effect. As a result, the search is on for alternatives to circuit simulations that were once considered revolutionary, but are now regarded as "standard".

Table look-up techniques have been employed in computer aided circuit analysis, offering certain advantages over analytical models to implement VLSI simulation analysis. In comparison, table look-up methodology is just beginning to be developed. Although it is advantageous to use analytical approach in many design, table look-up technique will fill an important need in IC design.

This paper attempts to describe mainly the table look-up techniques for MOSFET nonlinear models. The modeling techniques proposed in this paper puts emphasis on computation efficiency and accuracy in a simulation application.

Section 2 briefly reviews some advantages employed table look-up techniques in VLSI design. Section 3 discusses mainly the general idea of the table look-up techniques, its approaches and interpolation and extrapolation implementation. Section 4 establishes three different dimensional models used in table look-up techniques. The different results come from section 4 are compared in section 5 and give some conclusion in section 6.
2 Motivation

2.1 Look-up table techniques in VLSI design

As MOSFET devices, which are used for VLSI circuits, have shrunk into the submicron range, models based on one-dimensional analysis have become inappropriate. Therefore, the results from two- or three-dimensional numerical solutions for MOSFET devices become of interest in research for implementing new phenomena in an analytical model. However, the model complexity causes higher computation cost, especially in fine line device evaluation.

In addition, conventional analytical methods offer empiricall adjustable constants for many different MOSFET categories, such as complementary, E/D, and SOS, to maintain good accuracy [8].

The table, which is able to deal with future submicron devices, is constructed with a few thousand work memory capacity requirement by suppressing data redundancy. Sufficiently high accuracy, with less than point several percent error, is achieved by using a special interpolation, which is called curve shape fitting technique [1]. Computational time to perform the interpolation from the table is much less than for the analytical model.

A common implementation approach in this novel CAD method is based on storing the analytical functions in look-up tables. Hardware savings can be achieved if some of the operands are fixed. Most of the reported procedures, performance evaluation, and analysis of look-up table implementation approaches assume that commercially available memory packages are used.
2.2 Look-up table applications in other fields

Modern GaAs MMIC technology also makes use of look-up table techniques in microwave circuit design and analysis. A novel CAD concept is used. The Field-theoretical package described has been structured to serve as a CAD kernel component in the frame of a hybrid and monolithic MIC design program [34].

Accurate computer-aided design of GaAs MMICs is complicated by the multiplayer situation. The analytical CAD models available for passive MIC structures are restricted to the conventional microstrip circuit environment. They consider only two dielectric media, the substrate and the air-filled space. The numerical CAD tools based on a rigorous frequency-dependent field-theoretical formulation are capable of handling multiplayer configurations in principle. These tools are much too time consuming for direct use in CAD, even for the elementary transmission line structures. Table look-up technique as an efficient field-theoretical tool application to a broad class of passive circuit structures has been developed as a CAD kernel component for multiplayer GaAs MMIC design. It is based on a new enhanced spectral domain technique (ESDT) which results in a reduction of CPU-times by one or two orders of magnitude compared to the conventional spectral domain approach. The field-theoretical package can be used to generate multidimensional look-up tables in the frame of a general purpose linear CAD program.

The computation times can be further reduced depending on the number of conductors considered. Together with the associated CAD concept and interpolation technique, the new tool constitutes a shift away from analytical models obtaining improvements with respect to generality, reliability of prediction, accuracy and even efficiency.

The extended multidimensional look-up tables, which are under the control MIC design program, are also applicable to hybrid-made printed circuit problems in general and could become a standard procedure.

The principle of the interpolation technique used in the CAD concept uses necessary data cubes generated by the field-theoretical tool at the beginning of a design task under control of the general purpose CAD program. The final stage, the new concept allows further increased precision by contraction of the data cubes around the accepted, near optimum parameters.

LINMIC is a CAD package for the layout-oriented design of single- and multi-layer MICs/MMICs up to mm-wave frequencies. Its description is based on a fast, enhanced spected design data in the form of multi-dimensional look-up tables under the control of LINMIC. Its input and output parameters are the geometrical data (lengths, widths, radii angles) of the geometrical planar MIC structures as well as the nominal resistance and capacitance values of hybrid chip components. In analysis and optimization, these tables
are used together with a fast interpolation method [34].

Researchers working in the field of telecommunication also employ look-up table techniques to analyze the Residue Number System (RNS) in current high-speed digital signal-processing (DSP) architectures [32]. RNS implementations have a highly modular structure, and are not dependent upon large binary arithmetic elements. With the advantages offered by look-up table techniques, RNS implementations become more attractive.

M. A. Bayoumi [32] has developed a look-up table layout model, which is used to derive relationships between the size of each modulus and both chip area times, this model supports all types of moduli. The procedure of selecting the most efficient layout is according to the design requirements and allows the designers to control the area time or the configuration of the memory module required for implementing a modulo look-up table. The multi-look-up table modules can be used to build block units for implementing digital signal-processing architectures.
3 Look-up table in MOSFET modeling

3.1 Look-up table techniques

This section describes general look-up table techniques for precise circuit simulation, which is based on four Japanese research work in 1982 [1]. To get table structure it is necessary to review device characteristics.

A basic MOSFET is such a device that it has four external terminals. Among the equivalent circuit parameters its drain current is most interested, which is determined by three bias voltages, \( V_{ds}, V_{ge}, \) and \( V_{bs} \). We are also noted that the drain current is a very smooth function of three bias voltages. The information contained in the curvature of the device characteristics itself is provided for reducing the table memory capacity requirement.

For an n-channel MOSFET, the following analytical equations give us the drain current expressions in different operation region.

- Linear region:
  \[
  I_{ds} = \beta \{(V_{gs} - V_t)V_{ds} - \frac{1}{2} V_{ds}^2 - \frac{2}{3} k[(V_{ds} - V_{bs} + 2\phi_f)^{\frac{3}{2}} - (2\phi_f - V_{bs})^{\frac{3}{2}}]\}
  \]

- Saturation region:
  \[
  I_{ds} = \beta \{(V_{gs} - V_t)V_{ds(sat)} - \frac{1}{2} V_{ds(sat)}^2 - \frac{2}{3} k[(V_{ds(sat)} - V_{bs} + 2\phi_f)^{\frac{3}{2}} - (2\phi_f - V_{bs})^{\frac{3}{2}}]\}
  \]

where

\[
\beta = \mu L W \frac{C_0}{2},
\]

\[
k = \frac{\sqrt{2eN_{o}K_i}}{C_0}
\]

Let \( I_{ds} \) be the drain current interpolated linearly. Then the following equations [22] give the resulting errors from the interpolation:

\[
E_i(V_j, V_k) = |[I_{ds}(V_j, V_k) - I_{ds}(V_j, V_k)]|
\]
\[
\leq \frac{\Delta_i^2}{8} \prod_{i=\text{MAX}(V_j, V_k)} \left| \frac{\partial^2}{\partial V_i^2} I_{ds}(V_j, V_k) \right|
\]
\[ i, j, k = d, g, b, \ i \neq j, i \neq k, j \neq k \]

where \( E_i(V_j, V_k) \) is the error evaluation for suffix \( i \) with \( V_j \) and \( V_k \) keep constant, and \( \Delta_i \) is the data points' interval along \( V_i \) axis, say, \( V_{ds}, V_{gs}, \) and \( V_{bs}. \) \( \Delta_d, \Delta_g, \) and \( \Delta_b \) are those to be dependent on in constructing the three-dimensional table structure, their relation is prescribed by the following equation:

\[
\frac{1}{\Delta_d} : \frac{1}{\Delta_g} : \frac{1}{\Delta_b} = \sqrt{1 + \frac{k}{2}(2\phi_f)^{-\frac{1}{2}}} : \sqrt{\frac{k}{2}(2\phi_f)^{-\frac{1}{2}}}
\]

It is noticed that

\[
\frac{1}{\Delta_d}, \frac{1}{\Delta_g} \gg \frac{1}{\Delta_b}
\]

It is obvious that the bulk bias effects are small enough to reduce the table data points because of similar current characteristics with different bulk bias conditions. Thus, it becomes possible to reduce data points corresponding to \( V_b \) and save table memory.

The following simplified equation is used to model weak inversion effect.

\[
I_{ds} = I'_0 e^{\frac{V_s - V_t}{kT}}
\]

where \( I'_0 = f[V_{ds}, (V_{gs} - V_i)_{min}, V_{bs}] \)

Note that \( (V_{gs} - V_i)_{min} \) refers to the table minimum gate to source bias voltage, which is near threshold condition. And \( I'_0 \) is reconstructed from the lower boundary value of the table. Therefore, we can easily extrapolate the weak inversion effect if the coefficient \( (q/\alpha KT) \) is known.

Now we can turn our concentration to the issue of table structure. As we have been noticed that circuit simulation program should meet following conditions.

1. Current continuity
2. Computation time saving
3. Small memory capacity requirement
4. Accuracy

1) and 2) are realized by applying simple interpolation, 3) and 4) are achieved as discussed above.

In general, a three-dimensional table consists of several two-dimensional tables, each for a constant bulk bias. Bulk bias effect is reducible without losing accuracy. Therefore the table derived into two parts. One of them is called a main-table, which expresses fine characteristics $I_{ds}$ as the function of $V_{ds}$ and $V_{gs}$ with zero bulk bias, has much precise data. Others are subtables, which has different threshold voltages defined by transformation formula, $V_{gs} - V_{t}$, expresses only derivations from the main-table.

Generally, almost the same characteristics as those in the main-table can be obtained at a subtable if the threshold voltage bulk bias dependence is embedded in the table structure (see Fig.1). That is, the $I_{ds} - V_{gs}$ characteristics are almost the same under different bulk bias conditions.

Gate voltage difference between two of the curves will remain the same at either high or low levels. So, if the origins of the subtables are shifted along with $V_{gs}$ due to the change of the threshold voltages, only small changes are needed to modify the characteristics in the subtables. The amount of data in the subtables is thus reduced by this configuration.

The following steps show how to generate subtables.

1. Using $V_{gs(min)}(V_{bs})$ array, the threshold bias dependency with the specified bulk bias is determined. Generally, the depletion layer growth bulk bias dependency has square root characteristics. Thus, a second-order polynomial approximation is adopted for calculating the threshold voltage precisely.

2. Get three dimensional vector $V_{ds}$, $V_{gs} - V_{t}$ and $V_{bs}$.

3. Choose two of the subtables according to the specified bulk bias. Intervals between subtable entries coincide with that in the main-table. There are usually eight generating points to construct a three-dimensional cell. DC operating point then moves from one cell to another. Note that careful attention must be paid for ensuring current continuity and avoiding convergency problems.

4. The generated eight cell points are multiplied by the main-table current data. This is called the "curve shape fitting" method.

5. Two points on each of the two subtables are calculated with the specified $V_{ds}$ and $(V_{gs} - V_{t})$ bias condition. DC operating current with respect to the designated $V_{bs}$ is interpolated from these two values.
3.2 Interpolation and extrapolation

In order to find intermediate current values, linear interpolation can be used down along $V_{ds}$.

The interpolation and extrapolation methods are central to the accuracy of the table model. The selection of interpolation and extrapolation techniques can be based upon the physics of the MOSFET in each region of its operation. Sufficient points must be included with in the table to reduce the error to an acceptable minimum. Typically, 20–50 points result in good accuracy.

Interpolation based on the

$$V_t = V_{t0} + k[\sqrt{2\phi_f - V_{bs}} - \sqrt{2\phi_f}]$$

formula, with $k$ and $\phi_f$ as fitted variables, is done to calculate $V_t$ for a given $V_{bs}$. Though $k$ and $\phi_f$ are expected to be nearly constant for a large device, their variations in case of a small device result in an accurate $V_t$.

Take an example. Let $A, B, C$ and $D$ denote 4 nearest grid points which enclose the point $P$, see Fig.2. Define normalized variables $\alpha$ and $\beta$ along $V_{gse}$ and $V_{ds}$ axes, respectively, as

$$\alpha = \frac{(V_{gse} - V_{gse1})}{(V_{gse2} - V_{gse1})}$$

$$\beta = \frac{(V_{ds} - V_{ds1})}{(V_{ds2} - V_{ds1})}$$

where $V_{gse} = V_{gs} - V_t$

$P$ is then computed as

$$P = A + (B - A)\alpha + (C - A)\beta + (D + A - B - C)\alpha\beta$$

Note that if $I_{ds}$ is chosen as a well continuous function, interpolated points can be guaranteed to be continuous through the $V_{gse}$-$V_{ds}$ plane.
In order to determine the value outside the table range, extrapolation is employed. As seen in 3.1 the value, which is in \([±V_{ds(max)}, ±∞]_{V_{ds}}\) and \([±V_{gs(min)}(V_{bs}), ±∞]_{V_{gs}}\), is extrapolated by using a boundary value and boundary conductance. Whereas the value in \([±∞, ±V_{bs(min)}]_{V_{gs}}\) and \([±V_{bs(\text{offset})}, ±∞]_{V_{gs}}\) is fixed to the boundary value, due to avoiding reverse current.

There are many different methods used for interpolating or approximating MOSFET device characteristics. For example,

- The polynomial approximation
- The piecewise polynomial approximation
- MOSFET analytical model parameter matching

Each method has its own individual advantages and disadvantages [6] [15] [21] [29] [31].
4 Table look-up MOSFET models

4.1 Three-dimensional table look-up MOSFET model

The novel concept for the 3-dimensional $I_{ds}(V_{ds}, V_{gs}, V_{bs})$ table model has been proposed in section 3. Here, a simplified accurate three-dimensional table look-up model has been developed, which is expected to be successfully applied to circuit simulation of MOS VLSI having submicron device dimension [10]. Recently, in the design of VLSI memories such as 1M bit DRAM, a very accurate circuit simulation is required since miniaturized size of MOSFETs gives rise to strong influence on their electrical characteristics through three-dimensional geometrical effects.

This subsection takes a gate-offset-voltage table and a stabilized current-correction table as an example to propose a short-channel effect and basic characteristics of a small geometrical device.

Based on the concept introduced in 3.1, we get three-dimensional table consists of three tables, which are current tables, gate-offset-table and current-correction table.

1. Current Table

The data of the 2-D current $I_{ds}(V_{ds}, V_{gs})$ table are measured by altering $V_{gs}$ to $V_{gs}$. $V_{gs}$ varies with $V_{ds}$ and $V_{gs}$ in order to take the back-gate-bias effect and short-channel-effect on the threshold voltage into account with the 2-D $I_{ds}(V_{ds}, V_{gs})$ table.

2. Gate-OFFSET-Voltage Table

The gate-offset-voltage $V_{gs}$ is defined at a given drain current $I_{d}$ and it is rather different from the threshold voltage because $I_{d}$ is freely selected in accordance with the type and size of MOSFETs. In measuring the current table $I_{ds}(V_{ds}, V_{gs})$, $I_{ds}$ becomes the measured drain current datum, so $I_{d}$ should be selected as an adequate value for the precise circuit simulation.

3. Current-Correction Table

In order to realize the much more accurate table model, the concept of current-correction table is introduced, and which is combined with the above two 2-D tables, $I_{ds}$, and $V_{gs}$. The current-correction table consists of several subtables where each of them has a constant bulk-bias. Koji Sakui et al have given out the experimental and simulated results [10].

System performance is regarded as the implemented interpolationability. The 3-D
interpolation is accomplished by fixing one variable and by using successively applied 2-D interpolations.
4.2 Two-dimensional table look-up MOSFET model

A key ingredient in the successful simulation of integrated circuits lies dramatically in developing an efficient means of modeling transistors. As MOSFET's in VLSI's are being shrunk down to and near submicron dimension to satisfy the ever-increasing need for higher speed and larger packing density, 2-dimensional numerical device models are becoming indispensable for an accurate electrical characterization of these small size devices. The reason for this is that the numerical approach is readily applicable to any 2-D problems such as short channel effect or narrow width effect. The major motivation in this subsection is how to reduce the number of table data.

As we have seen in 4.1, for a 3-D model, if \( N \) points per dimension are required for adequate accuracy, the two arrays of this 3-dimensional model together must contain \( 2N^3 \) entries. A large amount of storage is therefore needed unless \( N \) is small. Even if the storage is reduced through creative model design, the 3-D approach still requires on the order of \( 10^3 \) memory locations. In the following discussion, two table look-up models which have substantially better storage characteristics than the 3-D table model approach.

- Model description and circuit calculation

R. S. Muller [23] indicates that MOSFET is a square-law device in the triode region, and a perfect current source in the saturation region. The storage requirement can be reduced with respect to the 3-dimensional model by exploiting these basic physical characteristics of the MOSFET device. Most of the information regarding the drain current as a function of the bias voltages lies within the triode region. The bulk of the storage is thus reasonably dedicated to this region. The output characteristic curves are stored for the triode region in a 2-dimensional array, which range is bounded by an \( I(\text{sat}), V(\text{sat}) \) characteristic separating the triode region from the saturation region.

\[ V(\text{sat}) = V_{ds} = V_{gs} - V_t \]

\( V_{ds} \) and \( V_{gsc} \) (\( V_{gsc} = V_{gs} - V_t \)) are parameters in 2-dimensional array. Since the data is stored only up to the saturation voltage, \( V(\text{sat}) \), the total number of elements in the array is less than \( N^2 \) if \( N \) points per dimension are included for the entire desired voltage range. The actual number of points depends on the shape of the \( I(\text{sat}), V(\text{sat}) \) characteristic.

Since the bulk-source potential, \( V_{bs} \), affects the device characteristics primarily through the threshold voltage, its effect on the drain characteristics is incorporated through the
introduction of a 1-dimensional array, which expresses the change in threshold voltage as a function of $V_{ds}$.

In saturation, MOSFET drain current is not constant for a given gate bias, but instead varies approximately linearly with $V_{ds}$ for simple theory. It is due to channel length modulation and electrostatic feedback from the drain. Following is the analytic representation model which is linear in $V_{ds}$.

$$I_d = I_{(sat)}(1 + \lambda V_{ds})$$

It is generally appended to the triode region current equation to ensure current continuity between the triode and saturation regions. If operation in either the triode region or the saturation region, the current is multiplied by $(1 + \lambda V_{ds})$. For long-channel devices, one $\lambda$ value is adequate. For short-channel devices, the saturation-region output conductance increases with increasing $V_{gse}$. The 2-dimensional model uses a 1-dimensional array for this variation.

Paper[2] indicates that the computational cost of the device simulator is drastically reduced by a proposed monotonic piecewise cubic interpolation technique. With this technique, the device simulator needs to calculate only 100–200 points to make up an accurate 3-D table look-up model. The computational time necessary for the interpolation is only about one third of the time for calculating one current point by the device simulator.
4.3 One-dimensional table look-up MOSFET model

The 2-dimensional table look-up model requires fewer memory locations than the simple 3-dimensional model described above. If a further level of approximation is made, a further reduction in storage is possible such that only 1-dimensional arrays are needed.

A. R. Newton has developed 1-D model [8]. Interpolation routines dealing with 1-D model also have been added.

Drain current in the triode region is given by the Shichman-Hodges model [24].

\[ I_{ds} = K(V_{gse(max)} - \frac{V_{ds} + \Delta V}{2})(V_{ds} + \Delta V) - K(V_{gse(max)} - \frac{\Delta V}{2})\Delta V \]

where

\[ \Delta V = V_{(sat)(max)} - V_{gse} \]

\[ V_{gse} = V_g - V_i \]

For this model, a single triode region characteristics is stored for \( V_{gse} = V_{gse(max)} \) and \( V_{gse(max)} \) is the largest possible \( V_{gse} \) in the circuit. Given a operating point, the current is computed by twice shifting the origin of the characteristics, then performing a subtraction. This is adequate for long-channel devices. For short-channel devices, it is necessary to redefine

\[ \Delta V = V_{(sat)(max)} - V(V_{gse}) \]

to account for the nonquadratic relationship between \( I_{(sat)} \) and \( V_{(sat)} \) and a 1-D array is introduced.

If \( N \) points per dimension are needed for adequate accuracy, then only \( 4N \) total points are required for this model. This saves \( N(N^2 - 4) \) points compared to the 3-D method.
5 Comparison of three models

From section 2, we can find out that a typical $E$ type $T_r (N = 0.2^{15} cm^{-3}, C_0 = 5.83^{-8} F/cm^2)$ in a three-dimension table is \\
\[
\frac{1}{\Delta_d} : \frac{1}{\Delta_g} : \frac{1}{\Delta_b} \approx 1 : 1 : 0.3
\]

This shows that the number of data points in the subtable can be reduced to 0.09, in comparison with the number of data points in the main-table.

The three-dimensional table look-up model is shown to be applicable to precise circuit simulation. This model is independent of the circuit simulator. The model can be generated easily, not only by direct device measurements, but also by theoretical computations. Following is some results.

- High accuracy (error $\leq 0.3$ percent)
- Memory capacity requirement is $2 \sim 3K$ points per model.
- Save at least half simulation time compared with the original SPICE MOSFET model [20].
- Capacity of handling short channel device.

Conceptually 3-D tables, requiring a large memory, are needed to accurately simulate an MOSFET. 3-D table look-up model in which the current table uses 3000 points. The model was shown to be about 2 times faster than the original SPICE model. Attempts were made to reduce the memory requirements, at the expense of some accuracy, by constructing 2-D tables. The table is constructed with less than 1000 points.

Following is some results we've got.

1. Accuracy vs. Storage and Interpolation Method

The results show the performance of the table models in terms of accuracy as a function of the number of points stored and the method of interpolation. For either the $V_{ds}$ or the $V_{gss}$ quadratic interpolation replaced a linear interpolation in the 2-D model, large errors result for small value of voltage. In particular, for approximately
400 points in the current array, the 2-D model had a maximum error of 109% for $V_{gs}$ interpolated linearly in the saturation region. The 1-D model showed a maximum error of 9.6% for 160 points in the array when interpolated linearly.

These results suggest that linear interpolation is unacceptable in the table models unless a very large set data is stored.

2. Body Bias Affect

The body bias table's impact on the accuracy of the table models has been examined. It is necessary to consider this source of error, because the body bias table is interpolated using a nonideal linear function for simplicity instead of a more physically meaningful half-power law. The 1-D and 2-D table models behave identically with respect to this effect, because the body bias term is computed in the same way in both models. It is shown that the output characteristic curves from the table model have been compared to the exact curves for a body bias of 2.5V. The curves are compared as a function of $V_{ds}$ for $V_g$, values of 1, 3, and 5V. The data shows that 20–50 points are needed for sufficient accuracy.

3. Speed of Evaluation

Total run times for the simulator do not greatly differ for the various models. This is because the model evaluation time is a small fraction of the total simulation time for this particular simulation program. The iteration count varies somewhat with the choice of model also.
6 Conclusion

Table models cannot be used directly to predict the behavior of hypothetical devices. However, table models have several advantages over analytic models. For instance, the task of obtaining a set of data for a table model is simpler than obtaining parameter values for a complex analytic model. Table models do not require revision for process changes. Also, evaluation of table models can be faster than evaluation of analytic models of equal accuracy.

Evaluation of MOSFET models in circuit and timing simulation for VLSI circuits accounts for 70% to 80% of the total analysis time. With the use of the proposed table model, the modeling time reduces to about 30% to 40% of the overall analysis time.

The result described in 4.1 provides an accurate three-D table look-up model without increasing computational time and data storage requirement. The three-dimensional table points becomes practical in size with less than 3000 points. Computational efficiency is improved by simple interpolation. The table model is at least two times faster than conventional analytical models [20]. This model is independent of a circuit simulation program. In the present system, table data are generated by measuring equipment of six different MOSFET analytical models [4].

It can be shown that under the appropriate interpolation, the look-up table models matchs exactly an ideal Shichman-Hogges transistor, excepting for the body bias effect.

However, the idea of using table look-up has been limited to the calculation of transport current. No table formulation exists in the literature for evaluating device capacitances. Narendra K. Jain et al [17] developed two 2-dimensional tables: the transport current and total gate-change tables. The device internodal capacitances, junction capacitors and junction diodes are then evaluated.

D. Divekar gives [26] a generalized table model for MOSFET transistors which models the variation of drain current with respect to both, the terminal voltages and the device geometry and is implemented in the circuit simulation program PowerSPICE. The model complexity can be chosen according to the desired accuracy and computation speed requirements. A variety of interfaces is provided to generate the required tables.

Up to now, the table look-up model has been considered applicable to accurate MOSFET device modeling, if the massive storage capacity is adequate for multi-dimensional table structure. It also can adopted timing simulator programs like MOTIS [18] and MOTIS-C [19].
System design in the VLSI medium becomes a challenge which requires new types of design methodologies to manage the complexity level. These design methods require coordination between the functional definition, the architectural description, the circuit design, and the physical layout implementation.
7 Acknowledgement

I am very grateful to Dr. M. B. Steer for his encouragement and overall guidance throughout the course. I would also thank Dr. R. S. Gyurcsik for his helpful suggestion.
References


and

\[ V_{\text{gsmin}} (V_{\text{bs}}) \]

**Fig. 1** Table Structure
Fig. 2 Interpolation Scheme
High-Speed Printed Circuit Board Analysis and Simulation in a Workstation Environment

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Abstract

Performance of digital systems on printed circuit boards (PCBs) is currently limited by transmission line effects and not by the technology of digital devices. CAPNET, an interactive, user-friendly graphical tool for the simulation and analysis of complex transmission line systems, is used to investigate high-speed pulse transmission on PCBs. CAPNET supports both experimental and analytic models of microstrips and most PCB structures, such as bends, tees and vias. In this paper an overview of CAPNET and examples illustrating propagation effects on printed circuit boards will be presented.
1. Introduction

Traditional computer aided design of printed circuit boards (PCBs) begins with a functional schematic from which components are manually or automatically placed and routed on a multi-layer substrate. The automatic routing routines work well for clock speeds up to 20 or 30 MHz by using a set of design rules that include limiting the maximum conductor length, establishing trace widths, and maintaining a minimum separation of traces. These design rules control many of the transmission line effects of importance by determining the relative amplitudes of forward and backward traveling wave components of a signal. The initial forward traveling wave is generated by the line driver and backward waves result from reflections at mismatched transmission line/device interfaces. Subsequently the backward waves also reflect resulting in additional forward traveling wave component. Generally drivers can not establish the required voltage levels with the initial forward traveling wave (especially when the characteristic impedance of a line is low enough that reflections at the driver interface are minimized) and so backward traveling wave components are essential in developing the correct operating voltage on the line.

Understanding the presence of forward and backward traveling waves is essential in analyzing transmission line effects and in establishing design guidelines.

We can now refer back to the design guidelines and discuss them in the context of wave components. Limiting conductor length limits the maximum delay of the forward and backward wave components. Fixing the width of traces determines the characteristic impedance of the line (if the dielectric properties are set) and, because of transmission line/device mismatch, determines the relative amplitudes of the forward and backward traveling components and thus the number of reflections required to establish voltage levels on
the transmission line. Thus limiting conductor lengths and fixing the width of traces determines the maximum signal propagation delay. The third design guideline --- minimum trace spacing --- limits crosstalk between adjacent traces.

Design of PCBs with circuits operating at clock speeds above 30 MHz or so requires more sophisticated design guidelines as well as post layout simulation. Only simulation of the transmission line networks will provide the required confidence in design. This is a significant departure from lower frequency design where it is usually sufficient to treat a transmission lines as a lumped capacitance or perhaps by a delay, if the transmission lines need be considered at all. Simulation of transmission line structures can be achieved by

1. using linear RF/microwave techniques with linear approximations of digital devices,

2. by modeling the transmission line as a lossless bidirectional delay line and using a circuit level simulator like SPICE,

3. by modeling the line as a set of lumped element subcircuits and again using a program like SPICE,

4. or through convolution techniques using the impulse response of the transmission line network obtained as the Fourier transform of its frequency domain characteristic. This has also been implemented in a circuit level simulator.

The first approach is available with commercial RF and microwave simulation packages but is restricted to linear approximations of digital devices --- a serious limitation. As the last three techniques can be incorporated in circuit level simulation packages, the actual nonlinear characteristics of digital devices can be incorporated. These latter techniques all yield useful design information but are prohibitively slow when analyzing large portions of the transmission line network on a PCB. This slow simulation speed results from the
use of matrix techniques and the treatment of all digital devices as though they were instantaneously coupled. However on a PCB a transmission line network is arranged as a tree and digital devices are not instantaneously coupled because of the finite delay along interconnecting transmission lines.

Transmission line networks on a PCB form a tree rather than a mesh and considerable simulation efficiency can be achieved by avoiding the matrix techniques required to handle a mesh (as implemented in circuit level simulators). The technique we present in this paper achieves simulation efficiency through recursive analysis of a transmission line tree.

The paper is organized as follows. First a review of transmission line theory is presented. Next, a technique for recursively solving transmission line networks is described [5]. A recursive tree data structure and algorithms are then presented. Finally, a review of CAPNET, the CAD tool for complex transmission line networks is presented along with example sessions on a DEC workstation.
2. Theory

In this section we review relevant transmission line theory and introduce a recursive algorithm for solving transmission line networks. The method has the advantage that the solution to all nodes in the system is simultaneously obtained.

2.1 Transmission Line Networks

Consider the basic problem of simulating pulse transmission through a loaded transmission line. Assuming that the pulse is bandlimited with a cutoff frequency of $f_c$, we can obtain the pulse response by computing the inverse FFT of the complex multiplication of the frequency response of the pulse and the transmission line network. Therefore, as a first step in calculating the frequency response of the network, we analyze the network response to a single sinusoid of frequency $f_0$. Consider the loaded transmission line connected to the generator $E_g$ through a source impedance $Z_s$ as shown in Fig. 1.

![Figure 1. Generator connected to loaded transmission line](image)

The voltage and current at any point on the transmission line can be obtained from the following expressions [2]:
In the above expressions

\[ \gamma = \sqrt{(r + j\omega)(g + j\omega)} \]  

(3)

is the propagation constant and

\[ z_0 = \sqrt{r + j\omega \over g + j\omega} \]  

(4)

is the characteristic impedance of the transmission line. The expressions for the source and load reflection coefficients are,

\[ \Gamma_L = -{z_L - z_0 \over z_L + z_0} \]  

(5)

\[ \Gamma_s = -{z_s - z_0 \over z_s + z_0} \]  

(6)

The expression for \( v(x) \) includes the superposition of all waves reflecting from the source and load mismatches. This can be seen by a Taylor series expansion of (1)

\[ v(x) = {v_s z_0 \over z_0 + z_s} \left[ e^{-\gamma x} + \Gamma_L e^{-\gamma(L-x)} + \Gamma_L \Gamma_s e^{-\gamma(2L-x)} + \Gamma_L^2 \Gamma_s^2 e^{-\gamma(3L-x)} + \ldots \right] \]  

(7)
To obtain the shape of the pulse at the load we evaluate $v(L)$ at frequencies from $f=0$ to $f=f_c$ in discrete steps where $f_c$ is the cutoff frequency of the bandlimited pulse. The number of points must be a power of 2 such that the inverse FFT may be used to obtain the sampled pulse response at the load.

Consider now the case where the boundary voltage and current are known on a section of transmission line. See Fig. 2. Evaluate $v(0)$ in (4) and then compute.

$$\frac{v(x)}{v(0)} = \frac{e^{-\gamma_1} + \Gamma L e^{-2\gamma(L-x)}}{1 + \Gamma L e^{-2\gamma L}} \tag{8}$$

Also

$$\frac{i(x)}{i(0)} = \frac{e^{-\gamma_1} - \Gamma L e^{-2\gamma(L-x)}}{1 - \Gamma L e^{-2\gamma L}} \tag{9}$$

Thus using (8) and (9) the voltage and current can be evaluated at any point on the transmission line given the boundary voltage and current.

Figure 2. Section of transmission line with boundary voltages and currents.
With the above preliminaries, we will examine the simple network in Fig. 3 and present a methodology for its solution. In Fig. 3, the nodes have been labeled $n_1$ through $n_5$. To solve this network, that is to obtain the voltage and current at each node and at any location within the network, consider equation (1). This equation suggests that if the impedance at node $n_1$ was known then the voltage and current at node $n_1$ can be calculated from the generator and source impedance. Thus the first step is to obtain the impedance at $n_1$. This impedance is seen to consist of the parallel combination of the impedance looking into $n_5$ and $n_2$ from $n_1$.

![Figure 3. Example transmission line network](image)

These impedances can be obtained by noting that (Fig. 4),

$$Z_{in}(x) = \frac{1 + \Gamma L e^{-2\gamma(L-x)}}{1 - \Gamma L e^{-2\gamma(L-x)}} Z_0$$

(10)
Thus, the first step is to calculate the impedances looking into \( n_3 \) and \( n_4 \) from \( n_2 \). The parallel combination forms the impedance at \( n_2 \). The impedance at \( n_1 \) is thus calculated by the parallel combination of the impedances looking into \( n_2 \) and \( n_5 \).

Therefore, the following methodology is suggested for solving the network. In the first pass, starting from the three loaded end nodes, the impedances are calculated and the parallel combination of these impedances at the parent node forms the parent node impedance. Working backward in this manner, the impedance at the root node (\( n_1 \), in the example) is calculated. Using (1) the voltage and current at the root node \( n_1 \) is calculated. Using (8) and (9) and the boundary voltages and currents, which were calculated at the parent node, the voltage and current at each node in the network can be calculated. Note that the current at each node is split into two currents flowing into each node.

In the next section, a computer program will be introduced which uses recursion and recursive data structures available in C to solve complex transmission line networks.
2.2. Recursive Programming and Data Structures

To introduce the algorithm for solving a complex transmission line network, we first consider the case where the network is limited to the binary tree structure shown in Fig. 5. In the figure, the generator is connected to the root of the tree through a source impedance $Z_s$. The tree consists of nodes which are either parents or leaves. A leaf is a node which is terminated on a load. For example, $n_3$, $n_4$, $n_6$, $n_7$, $n_9$, $n_{11}$, and $n_{12}$. Parent nodes have two branches. A left branch and a right branch. Nodes $n_1$, $n_2$, $n_5$, $n_8$, and $n_{10}$ are parent nodes.

In general each branch represents a transmission line with different characteristics and lengths. Each section of transmission line is associated with the node on which it terminates. Thus the section of transmission line from the generator to the root node $n_1$ is described in the data structure pointed to by $n_1$. This concept is described below.

Figure 5. Transmission line network as a tree structure
Each node has an associated data structure which occupies memory locations. A pointer can be defined which points to the data structure in memory. As nodes are added to the tree, memory is dynamically allocated for the data structure and a pointer is defined. Thus, for the nodes of the network in Fig. 5 the following data structure can be defined in C.

```c
struct node {
    struct node *left;
    struct node *right;
    struct node *parent;
    char name [16];
    float r,l,c,g;
    float length
    complex Z_Left;
    complex Z_Right;
    complex Z_L;
    complex node_voltage;
    complex left_current;
    complex right_current;
    complex input_current;
    complex Z_0;
    complex gamma;
}
```

Within the data structure definition are three pointers to data structures of the same type. Thus the data structure is recursive. Two pointers point to the left and right nodes while the third pointer points to the parent node. Three cases are immediately evident. If the node is a leaf then the left and right node pointers are NULL. Otherwise, they will point to the left and right child nodes attached to the node. If the node is the root node, then the pointer to the parent will be NULL.
The other data types within the structure represent data necessary to describe the node. These can be classified into two groups. One group defines the name of the node and the characteristics of the transmission line (e.g., r,l,c,g and $Z_0$ and $\gamma$). The other group represents data which are calculated and depend on the network. These include the voltage at the node, the current flowing into the right and left nodes, and the impedances looking into the nodes.

It is very convenient to access data in a data structure using pointers to data structures. For example, to assign the variable $Z$ the value of the characteristic impedance at the node pointed to by $np$ we write,

$$Z = np -> Z_0$$

To access the characteristic impedance of the left child node of the node pointed to by $np$ we write,

$$Z = np -> left -> Z_0$$

At this stage, we will describe recursive functions which are used to compute the impedances, voltage and currents at each node. First we introduce two methods for traversing tree data structures.

### 2.3. Traversing Trees

There are general methods for traversing trees [3]. We will apply two of these methods to solve the tree network.

**Postorder Listing**

Postorder traversing of trees is illustrated in Fig. 6. This method is useful in the first pass needed prior to solving for the voltages and currents of the network. As pointed out earlier the impedances at each node must be computed. Thus in Fig. 6, the impedance at 3 is the parallel combination of the impedances of the loaded transmission lines 1 and 2. Similarly, the impedance at 6 is
computed from 4 and 5. Once the impedance of 3 and 6 are computed, the impedance at 7 can be calculated and so on. Careful study of the figure will show that the numbering schemes correspond to the order in which the impedance calculations must be carried out. This order of traversing the tree is termed postorder listing. The method is summarized below [3]:

(1) If a tree is composed of only a single node, the post order listing consists of just that single node.
(2) If a tree consists of more than one node, the postorder listing consists of the postorder listing of each subtree, in left-to-right order, followed by the root.

Figure 6. Post-order traversing of tree for impedance calculations

Preorder Listing

This method is used in the calculation of the voltages and currents at each node once the impedances have been determined. Preorder listing is illustrated in Fig. 7. Thus, once the boundary voltage at node 1 is known, the voltage at node 2 can be computed (since the
impedance at 2 is also known from the first postorder traversing in computing the impedance. From 2, the voltage at 3 and 6 can be computed and so on. The preorder listing method is summarized below [3]:

1. If a tree is composed of a single node, the preorder listing consists of just that single node.
2. If a tree consists of more than one node, the preorder listing consists of the root, followed by the preorder listing of each sub tree in left-to-right order.

![Figure 7 Pre-order traversing of tree for current and voltage calculations](image)

Figure 7 Pre-order traversing of tree for current and voltage calculations

The technique for solving complex transmission line networks outlined above has been incorporated in a CAD tool called CAPNET. CAPNET is described in the next section.
3. An Overview of CAPNET Design

CAPNET (CAPture NETwork) is a physical-level transmission line network analysis tool with a user-friendly graphical interface. The current implementation allows user to model both local-area networks and printed circuit boards; the analysis technique used can easily be expanded to model other types of transmission line networks as well.

CAPNET supports both analytical and empirical (table-based) models of transmission lines and junctions. It is designed so that new models for lines and junctions can be coded and incorporated into the program with a minimum of difficulty, specifically, without modification to the "high-level" simulator and editor.

The program provides a graphical display of the "captured" network. It also provides a variety of output data and plots, including impulse and frequency responses, characteristic impedance and other line parameters, conductor voltage and current distributions, pulse responses, and eye diagrams.

CAPNET currently comprises about 12,500 lines of C code, split about equally between the graphical interface and the actual simulator. It requires a VAXstation running VMS, and currently uses the GKS graphics interface[4]. We will also have CAPNET running on X-Windows in the near future.

Future development will include models for multi-conductor (three or more) lines, inter- and intra-conductor coupling, and non-linear loads.

3.1. How CAPNET Represents a Network Topology
Visually, CAPNET represents a network topology as a multiway tree, consisting of "nodes" connected by "edges." A root or "source" node represents the signal input. Other nodes represent either junctions between conductors or conductor terminations. Conductors themselves are represented as edges.

A consequence of this is that networks represented by the present implementation of CAPNET must be free of loops. Many topologies containing internal loops can, however, be reduced to simplified cases without such loops, and we may investigate how to incorporate this process into CAPNET in the future.

At the lowest level, CAPNET topologies are represented by a binary tree structure. This is most satisfactory in the cases where nodes connect at most three edges. Instances of nodes connecting four or more edges are infrequent enough (in our experience) that we have opted to use a modified binary tree representation of the network rather than a generalized multiway tree representation. The structure of the binary tree is both easier to comprehend and manipulate, and our implementation has no difficulty dealing with cases where more than three edges connect at a node.

### 3.2 Creating and Editing a Network Topology

CAPNET topologies are created and edited graphically in most cases. Topology data is stored in a simple ASCII (text) file, however, and it is possible to create networks without using the graphical editor. We have already seen one application that converts the output of a PCB layout program to a CAPNET-readable form; other programs of this nature should not be too difficult to write.

Users of CAPNET typically define (that is, draw) the topology of a new network before defining the network's specific line and junction types. We found this method to be considerably faster than the
alternative, in which a user has to pause to enter data after adding each line segment to the graph. A user could expect to enter a complete network of ten to twenty lines in under five minutes, and in less if he is familiar with the system.

Users can edit a network at any stage during or after its creation. The editor allows users to delete single line segments and subtrees, insert new line segments, divide existing line segments, relocate the source node, and reorient individual line segments or subtrees. Users can also modify line and junction characteristics at any time.

3.3 Analysis Options

The CAPNET simulator produces a variety of output, all of which can be redirected to plotting devices or files. CAPNET can display voltage and current distributions across any line at a chosen analysis frequency. It can display the characteristic impedance and other calculated parameters of the junction and transmission line at that frequency, including the subtree load impedance and nodal currents and voltages.

In addition, CAPNET can display the frequency and impulse response at any node in the network. Impulse responses can be convolved with individual pulses or pulse trains to produce pulse responses and eye diagrams.

The analysis technique used makes it possible to solve for the frequency response of many nodes simultaneously without a significant increase in the calculation time. This is convenient when the network being analyzed is very large.

3.4 CAPNET Example

An analysis of pulse propagation in a printed circuit board is provided below. In Figure 8, a PC board trace is shown with bends,
vias, and tees. The length of each trace is also shown in meters. The menu in Figure 8 shows the editing features available in CAPNET. These extensive features make graphical capture or modification of large networks very easy.

In Figure 9, the analysis window is shown. Note that for the selected segment, the line length is 2 cm of 8-mil trace. The load is also shown as a parallel resistance (280 Ohms) and capacitance (10.0 pf). The flag for calculating the impulse response for this node has been set.
In this case, when the network is solved, the impulse response for this node will be stored in a dynamically allocated array. (The user can flag those nodes for which an impulse response is desired prior to calculation).

From Fig. 9 note the analysis options for node n12 which include:

- **Seg. Info.** (Voltage and current distribution at a fixed frequency, node information such as characteristic impedance and propagation constant among other parameters).

- **Pulse Param.** This is used to set pulse width, rise and fall times and pulse repetition rate.

- **Eye Diag. Param.** This is used to set the eye diagram parameters such as number of samples per baud, phase etc.

- **Eye Diagram.** This calculated and plots the eye diagram.

- **Sample Parameters.** This option is used to set the sampling rate and the number of samples to compute the impulse response.

- **Freq. Response.** The frequency and phase response are plotted.

- **Imp. Response.** The impulse response is computed and plotted.

- **Pulse Response.** The pulse response based on convolving the impulse response with the pulse sequence determined by the pulse parameters option is computed and displayed.
Figure 9. Analysis Options.

Figure 10 shows the impulse response for Schottky TTL loads. The pulse response to a 5 ns wide pulse is shown in Figure 11. The eye diagram is shown in Figure 12.
Figure 10.
Pulse Response

Figure 11.
Choose output device type from the menu.

Figure 12.
Figure 13.
The loads were changed to TTL and the eye diagram was obtained and is displayed in Figure 13. Note the severe degradation associated with the slower speed technology on this trace compared to Figure 12.

Also shown in Figure 12 is the hardcopy options. A hardcopy of any plot can be obtained on the devices shown in the menu.

The example presented above illustrates the power of this CAD tool in analyzing the performance of high speed technologies in printed circuit boards and other complex transmission line networks. Using the tool, the lines, loading impedances, distances and other circuit parameters can be modified so that acceptable high speed operation is obtained.

4. References


Abstract

A data structure and algorithm for representing, and simultaneously solving for all nodes within complex transmission line systems is presented. The method is based on representing the network as a recursive tree structure and solving for the voltage, current, and impedance at each node using recursive programming techniques. First, all frequency dependent parameters within the tree structure are updated, then in a post-order traversing of the tree, the impedances at each node are computed followed by a pre-order traversing of the tree to compute node voltages and currents. The technique is useful in networks with many branches and mixed transmission line characteristics. Applications include the modeling and simulation of pulse propagation in distribution line carrier networks, local area networks, and the digital subscriber loop with bridged taps.
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I. Introduction

In many digital communication systems, complex transmission line networks are encountered which contain mixed transmission lines with different characteristics and many branches. Examples include the distribution line carrier network, the digital subscriber loop with bridge taps, and certain local area network configurations. The transmission line network usually introduces severe magnitude and phase distortion resulting in the degradation of bit error rate performance in digital transmission systems.

In this paper we present a program for computer modeling and simulation of complex transmission line networks. The network is represented in the computer by a recursive binary tree data structure. Using recursive programming techniques, the node voltage current, and impedance at each node within the tree structure is computed. In this manner the frequency response of the network, from the source node to the receiving node is computed. The impulse response or the pulse response of the network is then calculated from the frequency response using Fast Fourier Transforms.

Computer programs for modeling transmission line networks have been written using ABCD parameters [1]. In this paper a new technique in which the frequency response at all nodes within the network are obtained simultaneously is presented. The technique is also suitable for the computer aided design and modeling of digital communication systems, with complex transmission line networks. A CAD tool is currently being developed for this purpose and a technical report describing the graphical capture, editing, and analysis of networks is available by in [5]. The interactive graphics is based on the graphical kernel system (GKS) [4]

II. Transmission Line Networks

Consider the basic problem of simulating pulse transmission through a loaded transmission line. Assuming that the pulse is bandlimited with a cutoff frequency of $f_c$, we can obtain the pulse response by computing the inverse FFT of the complex multiplication of the frequency response of the pulse and the transmission line network. Therefore, as a first step in calculating the frequency response of the network, we analyze the network response to a
single sinusoid of frequency $f_0$. Consider the loaded transmission line connected to the generator $E_g$ through a source impedance $Z_s$ as shown in Fig. 1 [2].

$$\text{Figure 1. Generator connected to loaded transmission line}$$

The voltage and current at any point on the transmission line can be obtained from the following expressions:

$$v(x) = \frac{v_s z_0}{z_0 + z_s} e^{-\gamma x} \frac{1 + \Gamma L e^{-2\gamma x}}{1 - \Gamma s L e^{-2\gamma x}}$$  \hspace{1cm} (1)$$

$$i(x) = \frac{v_s z_0}{z_0 + z_s} e^{-\gamma x} \frac{1 - \Gamma L e^{-2\gamma x}}{1 - \Gamma s L e^{-2\gamma x}}$$  \hspace{1cm} (2)$$

In the above expressions

$$\gamma = \sqrt{(r + j\omega)(g + j\omega)}$$  \hspace{1cm} (3)$$

is the propagation constant and

$$z_0 = \sqrt{\frac{r + j\omega}{g + j\omega}}$$ \hspace{1cm} (4)$$

is the characteristic impedance of the transmission line. The expressions for the source and load reflection coefficients are,
The expression for $v(x)$ includes the superposition of all waves reflecting from the source and load mismatches. This can be seen by a Taylor series expansion of (1)

$$v(x) = \frac{v_s z_0}{z_0 + z_s} \left[ e^{-\gamma x} + \Gamma_L e^{-\gamma (L + x)} + \Gamma_L e^{-\gamma (2L + x)} + \Gamma_L^2 \Gamma_s e^{-\gamma (3L + x)} + ... \right]$$

To obtain the shape of the pulse at the load we evaluate $v(L)$ at frequencies from $f=0$ to $f=f_c$ in discrete steps where $f_c$ is the cutoff frequency of the bandlimited pulse. The number of points must be a power of 2 such that the inverse FFT may be used to obtain the sampled pulse response at the load.

Consider now the case where the boundary voltage and current are known on a section of transmission line. See Fig. 2. Evaluate $v(0)$ in (4) and then compute.

$$\frac{v(x)}{v(0)} = \frac{e^{-\gamma x} 1 + \Gamma_L e^{-\gamma (L + x)}}{1 + \Gamma_L e^{-\gamma L}}$$

Also

$$\frac{i(x)}{i(0)} = \frac{e^{-\gamma x} 1 - \Gamma_L e^{-\gamma (L + x)}}{1 - \Gamma_L e^{-\gamma L}}$$

Thus using (8) and (9) the voltage and current can be evaluated at any point on the transmission line given the boundary voltage and current.
With the above preliminaries, we will examine the simple network in Fig. 3 and present a methodology for its solution. In Fig. 3, the nodes have been labeled $n_1$ through $n_5$. To solve this network, that is to obtain the voltage and current at each node and at any location within the network, consider equation (1). This equation suggests that if the impedance at node $n_1$ was known then the voltage and current at node $n_1$ can be calculated from the generator and source impedance. Thus the first step is to obtain the impedance at $n_1$. This impedance is seen to consist of the parallel combination of the impedance looking into $n_5$ and $n_2$ from $n_1$. 

Figure 2. Section of transmission line with boundary voltages and currents

Figure 3. Example transmission line network
Thus, the first step is to calculate the impedances looking into n3 and na from n2. The parallel combination forms the impedance at n2. The impedance at n1 is thus calculated by the parallel combination of the impedances looking into n2 and ny.

Therefore, the following methodology is suggested for solving the network. In the first pass, starting from the three loaded end nodes, the impedances are calculated and the parallel combination of these impedances at the parent node forms the parent node impedance. Working backward in this manner, the impedance at the root node (n1 in the example) is calculated. Using (1) the voltage and current at the root node n1 is calculated. Using (8) and (9) and the boundary voltages and currents, calculated at the parent node, the voltage and current at each node in the network can be calculated. Note that the current at each node is split into two currents flowing into each node.

In the next section, a computer program will be introduced which uses recursion and recursive data structures available in C to solve complex transmission line networks.
III. Recursive Programming and Data Structures

To introduce the algorithm for solving a complex transmission line network, we first consider the case where the network is limited to the binary tree structure shown in Fig. 5. In the figure, the generator is connected to the root of the tree through a source impedance $Z_s$. The tree consists of nodes which are either parents or leaves. A leaf is a node which is terminated on a load. For example, $n_3, n_4, n_6, n_7, n_9, n_{11},$ and $n_{12}$. Parent nodes have two branches. A left branch and a right branch. Nodes $n_1, n_2, n_5, n_8,$ and $n_{10}$ are parent nodes.

![Figure 5. Transmission line network as a tree structure](image)

In general each branch represents a transmission line with different characteristics and lengths. Each section of transmission line is associated with the node on which it terminates. Thus the section of transmission line from the generator to the root node $n_1$ is described in the data structure pointed to by $n_1$. This concept is described below.

Each node has an associated data structure which occupies memory locations. A pointer can be defined which points to the data structure in memory. As nodes are added to the tree, memory is
dynamically allocated for the data structure and a pointer is defined. Thus, for the nodes of the network in Fig. 5 the following data structure can be defined in C.

```c
struct node {
    struct node *left;
    struct node *right;
    struct node *parent;
    char name [16];
    float r,l,c,g;
    float length;
    complex Z_Left;
    complex Z_Right;
    complex ZL;
    complex node_voltage;
    complex left_current;
    complex right_current;
    complex input_current;
    complex Z0;
    complex gamma;
}
```

Within the data structure definition are three pointers to data structures of the same type. Thus the data structure is recursive. Two pointers point to the left and right nodes while the third pointer points to the parent node. Three cases are immediately evident. If the node is a leaf then the left and right node pointers are NULL. Otherwise, they will point to the left and right child nodes attached to the node. If the node is the root node, then the pointer to the parent will be NULL.

The other data types within the structure represent data necessary to describe the node. These can be classified into two groups. One group defines the name of the node and the characteristics of the transmission line (e.g., r,l,c,g and Z₀ and γ). The other group represents data which are calculated and depend on the network. These include the voltage at the node, the current flowing into the right and left nodes, and the impedances looking into the nodes.

It is very convenient to access data in a data structure using pointers to data structures. For example, to assign the variable Z the value of the characteristic impedance at the node pointed to by np we write,
\[ Z = np \to Z_0 \]

To access the characteristic impedance of the left child node of the node pointed to by \( np \) we write,

\[ Z = np \to \text{left} \to Z_0 \]

At this stage, we will describe recursive functions which are used to compute the impedances, voltage and currents at each node. First we introduce two methods for traversing tree data structures.

IV. Traversing Trees

There are general methods for traversing trees [3]. We will apply two of these methods to solve the tree network.

Postorder Listing

Postorder traversing of trees is illustrated in Fig. 6. This method is useful in the first pass needed prior to solving for the voltages and currents of the network. As pointed out earlier the impedances at each node must be computed. Thus in Fig. 6, the impedance at 3 is the parallel combination of the impedances of the loaded transmission lines 1 and 2. Similarly, the impedance at 6 is computed from 4 and 5. Once the impedance of 3 and 6 are computed, the impedance at 7 can be calculated and so on. Careful study of the figure will show that the numbering schemes corresponds to the order in which the impedance calculations must be carried out. This order of traversing the tree is termed postorder listing. The method is summarized below [3]:

1. If a tree is composed of only a single node, the post order listing consists of just that single node.
2. If a tree consists of more than one node, the postorder listing consists of the postorder listing of each subtree, in left-to-right order, followed by the root.
Figure 6. Post-order traversing of tree for impedance calculations

**Preorder Listing**

This method is used in the calculation of the voltages and currents at each node once the impedances have been determined. Preorder listing is illustrated in Fig. 7. Thus, once the boundary voltage at node 1 is known, the voltage at node 2 can be computed (since the impedance at 2 is also known from the first postorder traversing in computing the impedance). From 2, the voltage at 3 and 6 can be computed and so on. The preorder listing method is summarized below [3]:

1. If a tree is composed of a single node, the preorder listing consists of just that single node.
2. If a tree consists of more than one node, the preorder listing consists of the root, followed by the preorder listing of each sub tree in left-to-right order.
V. Recursive Calculation of Network Impedances

The following C code presents a recursive function that calculates the impedance at each node using a post order traversing of the tree structure.

1. `Complex calculate_impedance (root)`
   ```c
   struct node * root;
   {
   ```

2. `(2) if ((root-> left == NULL) && (root -> right == NULL)) {
   ```
        /*
        * we are at a leaf
        * calculate impedance a distance root -> length away from
        * the load, root -> Z_L
        * calculate reflection coefficient at load
        */
        rcl = calc_rcl (root-> Z_L ,root -> Z_0);
        return (line_impedance (rcl, root -> Z_0,
             root -> gamma,root -> length));
   }

3. `root -> left_impedance = calculate_impedance (root -> left);
   root -> right_impedance = calculate_impedance (root -> right);`
/*
* calculate parallel combination of left and right
* impedance
*/

(4) root ->Z_L = Z_impedance_parallel (root -> left_impedance,
    root-> right_impedance);
    rcl = calc_rcl (root ->Z_L, root -> Z_0);
(5) return ((line_impedance(rcl, root ->Z_0 , root -> gamma,
    root-> length));
} 

Function explanation:

(1) The function argument, root, is a pointer to a node within the tree. The function returns the impedance "looking into a node," and it is complex.

(2) The function checks to see if the node is a leaf. If it is, then it calculates and returns the impedance looking into the leaf node. This is one of the terminating conditions of the recursive function. In other words, once a leaf node is reached, the function returns. The function line_impedance() calculates the impedance based on equation (10)

(3) If the node is not a leaf, then the function recursively calls itself by passing the left branch node pointer. After returning the impedance looking into the left node, the function is recursively called to calculate the right branch node impedance

(4) Once the left and right impedances at the node are known, the parallel combination is computed. This produces the total node impedance.

(5) At this point the impedance looking into the node is computed and returned by the function. This is also another terminating condition.

After this function is called, the impedances at all nodes are stored in the data structures pointed to by each node within the network.

VI. Recursive Calculation of Node Currents and Voltage.

After the function calculate_impedance (root) is called, each node contains the terminating or left and right branch impedance. The next recursive function, calculates the total current flowing into each
node including the left and right branch currents. The function makes use of equation (9) to compute the node current $I(L)$ based on knowledge of the boundary current $I(0)$. The function performs a pre-order traversing of the tree network.

(1) \texttt{calc\_current (root, i\_input)}
\begin{verbatim}
    struct node * root;
    complex i_input;
    {
        complex line\_current();
        /*
        * evaluates boundary current based on Eq. (9)
        */
        complex calc\_left\_current ();
        complex calc\_right\_current ();
        /*
        * calculate the total node current based on equation (9)
        * i\_input is the boundary current corresponding to I(0) in 
        * the equation
        */
        (3) root->input\_current = line\_current (root, i\_input, root->ZL, root->length);
        (4) if (root->left != (struct node *)NULL) {
            root->left\_current = calc\_left\_current (root->left\_impedance, root->right\_impedance, root->input\_current);
            calc\_current (root->left, root->left\_current);
        }
        if (root->right != (struct node *)NULL) {
            root->right\_current = calc\_right\_current (root->left\_impulse, root->right\_impulse, root->input\_current);
            calc\_current (root->right, root->right\_current);
        }
    }
\end{verbatim}

Explanation:

(1) The \texttt{root} argument is a pointer to the current node, \texttt{i\_input} is the complex boundary current corresponding to $I(0)$ in equation (9). That is, it is the total current flowing into the transmission line associated with the node.

(2) The function \texttt{line\_current()} computes the current $I(L)$ in equation (9). The functions \texttt{calc\_left\_current()} and \texttt{calc\_right\_current()}, calculate the currents flowing into the left and right branches.
This operation calculates $I(L)$ and stores it in the data structure of the node. Note that since this is a recursive procedure for traversing all the nodes of the tree, this operation will occur for each node.

If the left branch is not a termination, then recursively call the function by moving to the node attached to the current node, root. However, first compute the boundary current $I(0)$ flowing into the node, in this case $left\_current$.

The same as in step 4 but for the right branch.

After this procedure is called, all node data structures will contain the total current, and the left and right currents. Note that when the procedure is first called, $i\_input$ is the total current flowing from the generator into the network. It is computed based on equation (2).

VII. Computer Simulation Results

In the previous sections, we showed how the voltage and currents at each node can be computed. In general, for bandlimited digital transmission over a complex transmission line network, the frequency response of the network and the input impedance looking into the network over a frequency range is required to completely model the network. Thus, the response of the network to a generator with arbitrary source impedance may be computed.

Fig. 8 shows a test network consisting of coaxial cable transmission lines with different characteristics. We are interested in obtaining the impulse response from the sending station to the receiving station.
The computer program computed the voltage at the receiving station at discrete frequency intervals up to 100 MHz. The program then performed a 1024 point inverse FFT to produce the impulse response at a sampling rate of $f_s = 200$ MHz. Due to skin effect at higher frequencies the frequency response of the network is effectively bandlimited. The computed impulse response at node $n_6$ is displayed in Fig. 9.

**Impulse Response**

![Impulse Response Graph](image-url)
Notice the pure delay corresponding to traveling a distance of 180 m from the sending station to the receiving station. Also, immediately following the main impulse, a large second impulse appears with a delay corresponding to traveling a distance of 40 m. This second impulse is due to reflections from the two open circuit transmission lines of 20 m length each (RG 58/U) which constructively add and propagate to the receiving station.

The response of the test network to a series of three pulses, shown in Figure 10, is given in Figure 11. The pulse widths are 1 μs. The rise and fall times are 100 ns and the period is 4 μs.

![Unwindowed Pulse](image)

Figure 11. Sequence of pulses.
Pulse Response

The eye diagram corresponding to exciting the network with a pseudo random sequence of pulses with 1 μs pulse widths, 100 ns rise and fall times and pulse separation of 1.5 μs is shown in Figure 12. It is interesting to compare the eye diagram with the pulse response of Figure 10. The eye diagram gives very useful information about the performance of the network for pulse propagation.
An interesting phenomenon associated with complex transmission line systems is that while reliable communication to one node is possible, another node may exhibit significantly lower reliability within the same network. This can be seen by examining Figure 13 through Figure 16. In these figures the eye diagram at various nodes is displayed. Obviously some nodes will behave better than others in terms of error rate performance.
Figure 13. Eye diagram at node n2

Figure 14. Eye diagram at node n4
Figure 15. Eye diagram at node n6

Figure 16. Eye diagram at node n7
The results presented above were obtained from the program CAPNET written by Joseph Hall [5] which solves complex transmission line networks based on the technique presented in this paper. Using CAPNET a complicated network is graphically captured using flexible graphical editing capabilities. The program also models junctions such as bends, "tees", and transitions between different types of transmission lines. The plots presented in this paper are from sessions in CAPNET in which the user can change parameters, plot the results, and obtain hard copies of the plots without leaving the program. CAPNET uses GKS for its interactive graphics and workstation independent capabilities.

Finally in Fig. 17, the voltage distribution along the 50 m cable connecting the receiving station to the main RG 8/U coaxial cable transmission line is shown at a frequency of 10 MHz. Note the standing wave pattern and loss associated with skin effect in the cable. The source was 5 volts.

Figure 17. Voltage distribution along a transmission line segment n6.
VIII. Conclusions

In this technical report, a computer program is described which simultaneously solves for all nodes within complex networks of transmission lines. A tree data structure was introduced for representing the network in the computer. Recursive procedures were presented for traversing the tree data structure to compute the impedance, voltage and current at each node within the network. Simulation results were then presented in which the impulse response of a test network composed of transmission lines of various characteristics and lengths was computed. The impulse response was then related to the network in terms of the predicted reflections and delays.

The program efficiently solves complex transmission line networks and has applications in the area of Computer Aided Design (CAD) of digital communication networks. Specific applications include the Distribution Line Carrier Network, the digital subscriber loop, and Local Area Networks.

IX. References.


MULTICONDUCTOR COMPUTER AIDED ANALYSIS
AND DESIGN PROGRAM

A USERS GUIDE

By

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August 10, 1988

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GENERAL NOTES

(1) The directory contains all the source files, header files, libraries and special files for the creation of the program MCCAD.

(2) This program uses interactive graphics to setup the coupling geometry and circuit components of a system of four conductor transmission lines with arbitrary source and load terminations.

(3) The program computes and plots the frequency response and the voltage and current distribution along the conductors.

(4) The frequency response can be stored so that the impulse response at each conductor can be calculated.

(5) A program to calculate the impulse response from the frequency responses is available and is called FRIMP.

(6) The program uses GKS level 2b for its interactive graphics capabilities. It can be run on VT125, a VT240, VT330/340 or VAX Station GPX.

(7) The circuit and conductors can appear anywhere on the screen. The base coordinates are specified in the *.pic files. Also text size, color, and font including line width and color are also specified in these files.

(8) The *.pic files are read by MCCAD during initialization. More information on how to change the placement and graphic attributes by modifying these files will be provided later.
OPERATION NOTES

(1) To run the program make sure that you have set the right workstation type by typing:

$define gks$wstype 41

In this case a VAX Station GPX is specified. Look at the GKS manual for appropriate numbers for the workstation type. (vt125 = 11, vt240 = 13)

(2) Run MCCAD. The program will draw a four conductor transmission line circuit with arbitrary source and load networks. A menu will appear with a choice of either parallel lines above a ground plane or circular shielded system.

Circuit Drawn on Workstation
(3) After selecting the appropriate coupling system a menu will appear with options to:

- Load a File
- Update a File
- Store
- Edit
- analyze
- Hardcopy
- Information
- Exit

(4) Choose Edit. This will allow you to pick (using a mouse or cursor keys) a conductor, shield, source/load admittance, circuit length, source voltages or other circuit elements.

(5) Once an item is picked, the current value (values) associated with the item will be displayed. You can change the value or hit <return> to accept the displayed value.

(6) If a conductor in the coupling geometry (circular shield or ground plane) is picked, you can move the conductor to a desired position.

Circular Shield Configuration
(7) After the desired position is selected, the surface is updated. You are asked whether you want to modify any parameters or accept the default values.

(8) It is important to initially modify all values. The values are the conductor polar coordinates for circular shield and x and y coordinates for the ground plane. The conductor wire radius must also be specified especially since they are initially set to zero. Note that no check is made to see if the conductors are within the shield. This is up to you!

(9) If the circular shield is picked, you will be prompted for the shield radius and the dielectric constant.

(10) If the ground plane is selected, you will be prompted for a relative length. This length is used for scaling. If a large value is selected the conductors are zoomed in. If a small value is chosen, a zoom out effect occurs. The value of this length has no effect on the physical length of the conductors in meters. However, since the conductor heights could be large (power lines) or small (PC boards for example) this length is used for display purposes after the actual coordinates of the conductors are entered. A little experimentation may be necessary. If the conductors disappear off the screen select a large value to zoom them in to select them.
(11) Important: to get back to the main menu click on an empty region on the screen.

(12) Selecting the "Information" option will display all circuit component values and the coupling geometry including wire radius.

(13) Selecting "Hardcopy" will allow you to obtain a hardcopy of the circuit and coupling geometry including the "information box" on a variety of plotting devices. Choose the appropriate device from the menu. Then enter a file name to store the hardcopy. Later you can print the file on the hardcopy device.

(14) To analyze the circuit choose "Analyze". This will allow you to obtain the frequency response at any point along the transmission line for any conductor. You can plot the results for all three conductors using linear, log x, and y in dB's or other combinations.

(15) If you intend to store the frequency response to obtain the impulse response, then start at a minimum frequency of zero.

(16) The prompts are such that for quick analysis where you don't want to store the results you can just type return to ignore them.

(16) You are also given the option of calculating and plotting the voltage and current distributions at a fixed frequency as a function of length along the transmission line system.

(17) You can store the circuit and coupling geometry in an ASCII file by selecting "Store". You can then load it in later using "Load". Note that you can always edit the ASCII file directly. Its format is given below.

(18) Good luck and have fun!
MAKING THE PROGRAMS

(1) A makefile is provided to make both MCCAD and FRIMP. Simply type
$make mccad
or
$make frimp
See the appendix for the make file.

FORMAT OF STORED ASCII FILE FOR COUPLING SYSTEM

The circuit parameters are stored and read from ASCII files based on the
following format:

**Ground Plane:**

Dielectric Constant
Reference length
Cond #1 Height, Horizontal Distance, Wire Radius
Cond #2 Height, Horizontal Distance, Wire Radius
Cond #3 Height, Horizontal Distance, Wire Radius
Circuit Length
Source Voltage #1
Source Voltage #2
Source Voltage #3
Source Y_{11} Y_{12}
Source Y_{22} Y_{23}
Source Y_{33} Y_{13}
Load Y_{11} Y_{12}
Load Y_{22} Y_{23}
Load Y_{33} Y_{13}
Circular Shield:

Dielectric Constant
Reference length
Cond #1 Polar Radius, Polar Angle, Wire Radius
Cond #2 Polar Radius, Polar Angle, Wire Radius
Cond #3 Polar Radius, Polar Angle, Wire Radius
Circuit Length
Source Voltage #1
Source Voltage #2
Source Voltage #3
Source $Y_{11}$ $Y_{12}$
Source $Y_{22}$ $Y_{23}$
Source $Y_{33}$ $Y_{13}$
Load $Y_{11}$ $Y_{12}$
Load $Y_{22}$ $Y_{23}$
Load $Y_{33}$ $Y_{13}$
FILES ASSOCIATED WITH DRAWING THE CIRCUIT AND GEOMETRY

There are four files with the .PIC attribute. These files are read by MCCAD during initialization and are used to draw the circuit, and coupling geometry. Each file has an x and y coordinate used to place the drawing on the workstation surface. Thus, the circular shield can be placed at the bottom and the circuit at the top. The "information box" can also be placed any where on the surface.

Circuit Geom.pic:

This file is used to draw the circuit. The data is as follows:

Line 1: int TextFont, int TextPrec, int TextColor, float TextHeight
Line 2: int LineColor, float LineWidth
Line 3: xBase yBase

See the GKS manuals for values and definitions for the text attributes. The text attributes control the conductor numbers. See GKS manuals for workstation dependent line colors. The LineWidth controls the thickness of the line.

xBase and yBase are the absolute coordinates of the lower left hand coordinate of the circuit to be drawn on the screen. These coordinates are in normalized device coordinates (0 <= x <= 1.0, 0 <= y <= 1.0).

Parall Geom.pic:

This file contains data to draw the ground plane and three conductors on the screen. The first line contains xBase and yBase which are the lower left coordinates of the ground plane drawing.

Shield Geom.pic:
This file contains data to draw the circular shield and three conductors on the screen. The first line contains xBase and yBase which are the lower left coordinates of the circular shield drawing.

**Text.pic:**

This file controls the placement and text attributes of the information box.

Line 1: `int TextFont, int TextPrec, int TextColor, float TextHeight`
Line 2: `int LineColor, float LineWidth (for the box)`
Line 3: `xBase yBase`
Line 4: `xi yi`
Line 5: `xWidth yWidth`
Line 6: `inFact, outFact`

`xBase` and `yBase` are the coordinates of the upper left corner of the box. `yi` is the increment towards the bottom of the screen as each line is printed. `xi` is ignored. `xWidth` determines the width of the Box `yWidth` is ignored since it is determined by how many lines are written. `inFact` and `outFact` control the shape of the Box (the inner and outer box)
Appendix

# Makefile for MCCAD and FreqImp
#
# written by Sasan Ardalan
# Center for Communications and Signal Processing
# Dept. of Electrical and Computer Engineering
# North Carolina State University
# Raleigh, NC 27695-7914
#
#
# set up some symbols
#
MULTIC = mc_matrix3.obj mc_calc3.obj
MULTLNK = mc_matrix3, mc_calc3
LIBLINK = imslmatx/lib

# Make file for CCAD.EXE

mccad.obj: mccad.c mc.h mccad.h
    cc/noopt mccad

mc_file.obj: mc_file.c mc.h mccad.h
    cc/noopt mc_file

mc_edit.obj: mc_edit.c mc.h mccad.h
    cc/noopt mc_edit

mc_draw.obj: mc_draw.c mc.h mccad.h
    cc/noopt mc_draw

mc_analysis.obj: mc_analysis.c mc.h mc_analysis.h
    cc/noopt mc_analysis

mc_menus.obj: mc_menus.c mc.h
    cc/noopt mc_menus.c
mc_init.obj: mc_init.c mc.h mc_init.h
   cc/noopt mc_init.c

mc_close.obj: mc_close.c mc_init.h
   cc/noopt mc_close.c

mc_hardcopy.obj: mc_hardcopy.c mc.h mc_hardcopy.h
   cc/noopt mc_hardcopy.c

Gkt_descrip.obj: Gkt_descrip.c Gkt_global.h
   cc/noopt Gkt_descrip.c

mc_matrix.obj: mc_matrix.c
   cc/noopt mc_matrix

mc_multicon.obj: mc_multicon.for
   for/noopt/check mc_multicon

mc_matrix3.obj: mc_matrix3.for
   for/noopt/check mc_matrix3

mc_calc3.obj: mc_calc3.for
   for/noopt/check mc_calc3

tr_param.obj: tr_param.c
   cc/noopt tr_param

tr_bessel.obj: tr_bessel.c
   cc/noopt tr_bessel

mc_mp.obj: mc_mp.c
   cc/noopt mc_mp

#
# Object files for freqimp.exe
#

mc_freqimp.obj : mc_freqimp.c
   cc/noopt mc_freqimp

mc_fft.obj : mc_fft.c
   cc/noopt mc_fft
# show how executables depend on objects & libs
#

mccad.exe : mccad.obj mc_file.obj mc_edit.obj mc_analysis.obj mc_draw.obj \
   mc_menus.obj mc_hardcopy.obj mc_init.obj mc_close.obj
Gkt_descrip.obj \\n   mc_multicon.obj mc_matrix.obj tr_param.obj tr_bessel.obj
mc_mp.obj  \$
   {MULTIC}
   write sys$output "linking"
   link mccad,mc_analysis,mc_draw,mc_edit,mc_file,mc_hardcopy,-
   tr_param, tr_bessel, mc_matrix, Gkt_descrip, -
   Gkt_input, mc_menus, mc_init, mc_close, -
   mc_mp, dr/lib,-
   dua0:[sys0.syslib]vaxcrtl/lib, -
   dua1:[users.ccsp.ardalan.multic]mc_multicon, -
   dua1:[users.ccsp.ardalan.multic]mc_matrix3, -
   dua1:[users.ccsp.ardalan.multic]mc_calc3, -
   dua1:[users.ccsp.ardalan.multic]imslmatx/LIB
   dua1:[users.ccsp.ardalan.graphics]GKSTOOLS/LIB

mccad : mccad.exe

frimp.exe: mc_freqimp.obj mc_fft.obj mc_mp.obj
   link/exe=frimp mc_freqimp.obj, mc_fft.obj, mc_mp, dr/lib

frimp: frimp.exe
Dielectric Constant = 1.000000
Radius = 0.005000
Position Radius, Angle, Wire Radius
1 0.003478 183.433594 4.0000000e-04
2 0.001772 92.245735 4.0000000e-04
3 0.003068 50.194424 4.0000000e-04
Circuit Length = 1000.000000
Source Voltages:
1 = 5.000000
2 = 0.000000
3 = 0.000000
Source Admittances
1 Y11 = 0.020000 Y12 = 0.000000
2 Y22 = 0.001000 Y23 = 0.000000
3 Y33 = 0.001000 Y13 = 0.000000
Load Admittances
1 Y11 = 0.020000 Y12 = 0.000000
2 Y22 = 0.001000 Y23 = 0.000000
3 Y33 = 0.001000 Y13 = 0.000000
Pour Conductor Coupling Voltages, Volta...
Welcome to Multiconductor CAD

Dielectric Constant 1.000000
Reference length = 0.250000
Height, Horizontal Distance, Wire Radius
#1 0.020000, 0.040000, 1.000000e-03
#2 0.020000, 0.051823, 4.000000e-04
#3 0.020000, 0.061979, 4.000000e-04
Circuit Length = 10.000000
Source Voltages:
#1 = 1.000000
#2 = 0.000000
#3 = 0.000000
Source Admittances
#1 Y11=0.010000 Y12=0.000000
#2 Y22=1000.000000 Y23=0.000000
#3 Y33=0.010000 Y13=0.000000
Load Admittances
#1 Y11=0.010000 Y12=0.000000
#2 Y22=1000.000000 Y23=0.000000
#3 Y33=0.010000 Y13=0.000000
Pour Conductor Coupling Voltages
An Overview of CAPNET Design

by

Joseph Hall

August 10, 1988

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An Overview of CAPNET Design

CAPNET (CAPture NETwork) is a physical-level transmission line network analysis tool with a user-friendly graphical interface. The current implementation allows user to model both local-area networks and printed circuit boards; the analysis technique used can easily be expanded to model other types of transmission line networks as well.

CAPNET supports both analytical and empirical (table-based) models of transmission lines and junctions. It is designed so that new models for lines and junctions can be coded and incorporated into the program with a minimum of difficulty, specifically, without modification to the "high-level" simulator and editor.

The program provides a graphical display of the "captured" network. It also provides a variety of output data and plots, including impulse and frequency responses, characteristic impedance and other line parameters, conductor voltage and current distributions, pulse responses, and eye diagrams.

CAPNET currently comprises about 12,500 lines of C code, split about equally between the graphical interface and the actual simulator. It requires a VAXstation running VMS, and currently uses the GKS graphics interface. We will also have CAPNET running on X-Windows in the near future.

Future development will include models for multi-conductor (three or more) lines, inter- and intra-conductor coupling, and non-linear loads.
How CAPNET Represents a Network Topology

Visually, CAPNET represents a network topology as a multiway tree, consisting of "nodes" connected by "edges." A root or "source" node represents the signal input. Other nodes represent either junctions between conductors or conductor terminations. Conductors themselves are represented as edges.

A consequence of this is that networks represented by the present implementation of CAPNET must be free of loops. Many topologies containing internal loops can, however, be reduced to simplified cases without such loops, and we may investigate how to incorporate this process into CAPNET in the future.

At the lowest level, CAPNET topologies are represented by a binary tree structure. This is most satisfactory in the cases where nodes connect at most three edges. Instances of nodes connecting four or more edges are infrequent enough (in our experience) that we have opted to use a modified binary tree representation of the network rather than a generalized multiway tree representation. The structure of the binary tree is both easier to comprehend and manipulate, and our implementation has no difficulty dealing with cases where more than three edges connect at a node.

Creating and Editing a Network Topology

CAPNET topologies are created and edited graphically in most cases. Topology data is stored in a simple ASCII (text) file, however, and it is possible to create networks without using the graphical editor. We have already seen one application that converts the output of a PCB layout program to a CAPNET-readable form; other programs of this nature should not be too difficult to write.
Users of CAPNET typically define (that is, draw) the topology of a new network before defining the network's specific line and junction types. We found this method to be considerably faster than the alternative, in which a user has to pause to enter data after adding each line segment to the graph. A user could expect to enter a complete network of ten to twenty lines in under five minutes, and in less if he is familiar with the system.

Users can edit a network at any stage during or after its creation. The editor allows users to delete single line segments and subtrees, insert new line segments, divide existing line segments, relocate the source node, and reorient individual line segments or subtrees. Users can also modify line and junction characteristics at any time.

Analysis Options

The CAPNET simulator produces a variety of output, all of which can be redirected to plotting devices or files. CAPNET can display voltage and current distributions across any line at a chosen analysis frequency. It can display the characteristic impedance and other calculated parameters of the junction and transmission line at that frequency, including the subtree load impedance and nodal currents and voltages.

In addition, CAPNET can display the frequency and impulse response at any node in the network. Impulse responses can be convolved with individual pulses or pulse trains to produce pulse responses and eye diagrams.

The analysis technique used makes it possible to solve for the frequency response of many nodes simultaneously without a significant increase in the calculation time. This is convenient when the network being analyzed is very large.
CAPNET Example

An analysis of pulse propagation in a printed circuit board is provided below. In Figure 1, a PC board trace is shown with bends, vias, and T's. The length of each trace is also shown in meters. The menu in Figure 1 shows the editing features available in CAPNET. These extensive features make graphical capture or modification of large networks very easy.

Figure 1. Editing Options.
In Figure 2, the analysis window is shown. Note that for the selected segment, the line length is 2 cm of 8-mil trace. The load is also shown as a parallel resistance (280. Ohms) and capacitance (10.0 pf). The flag for calculating the impulse response for this node has been set. In this case, when the network is solved, the impulse response for this node will be stored in a dynamically allocated array. (The user can flag those nodes for which an impulse response is desired prior to calculation).

Note the analysis options for node n12 which include:

- **Seg. Info.** (Voltage and Current Distribution at a fixed frequency, Node information such as characteristic impedance and propagation constant among other parameters).

- **Pulse Param.** This is used to set pulse width, rise and fall times and pulse repetition rate.

- **Eye Diag. Param.** This is used to set the eye diagram parameters such as number of samples per baud, phase etc.

- **Eye Diagram.** This calculated and plots the eye diagram.

- **Sample Parameters.** This option is used to set the sampling rate and the number of samples to compute the impulse response.

- **Freq. Response.** The frequency and phase response are plotted.

- **Imp. Response.** The impulse response is computed and plotted.

- **Pulse Response.** The pulse response based on convolving the impulse response with the pulse sequence determined by the pulse parameters option is computed and displayed.
Figure 2. Analysis Options.

Figure 3 shows the impulse response for Schottky TTL loads. The pulse response to a 5 ns wide pulse is shown in Figure 4. The eye diagram is shown in Figure 5.
Impulse Response

Figure 3.
Figure 4.
Eye Diagram

Amplitude (volts)

Relative t (sec)

Choose output device type from the menu.

Figure 5.
Figure 6.

The loads were changed to TTL and the eye diagram was obtained and is displayed in Figure 6. Note the severe degradation associated with the slower speed technology on this trace compared to Figure 5.

Also shown in Figure 5 is the hardcopy options. A hardcopy of any plot can be obtained on the devices shown in the menu.
The example presented above illustrates the power of this CAD tool in analyzing the performance of high speed technologies in printed circuit boards and other complex transmission line networks. Using the tool, the lines, loading impedances, distances and other circuit parameters can be modified so that acceptable high speed operation is obtained.
Derivation of
Voltage and Current Transfer Functions for
Multiconductor Transmission Lines

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Abstract

A set of new and compact equations are derived for solving a system of multiconductor transmission lines with arbitrary source and load termination networks. The derivations are based on defining the reflection coefficient matrix for multiconductor transmission lines. Expressions for the voltage and current transfer functions are derived. For the two conductor case, the equations reduce to well known results. The expressions are very suitable for straightforward coding on a computer. The validity of the derived equations is checked with published experimental and computer models for three and four conductor transmission line systems.
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1. Introduction

The study of coupling between wires in multiconductor systems is important in many communication systems. These include near-end and far-end crosstalk in the subscriber loop in telephone networks, coupling to and from twisted wire pairs in high speed Local Area Networks (LANs), the prediction of voltage distribution in poly-phase distribution line systems in power line communications, and the prediction of crosstalk noise due to high speed switching in printed circuit boards [6-17].

Previously expressions have been derived for solving multiconductor transmission line systems, for example in [3] and [4]. These expressions are not compact nor do they easily reduce directly to familiar two conductor equations [1]. In this paper a set of compact equations are derived for solving a system of multiconductor transmission lines with arbitrary source and load terminations. Also expressions for the voltage and current transfer functions in terms of the reflection coefficient at the load are derived. In the derivation, the reflection coefficient matrix is defined and the voltage and current vectors and input impedance matrix are derived in terms of the reflection coefficient matrix at the load.

The equations derived in this paper were coded in a computer program and used to solve a number of multiconductor transmission line systems. Published experimental and computer model predictions for these systems were available in the excellent work in [5] and [6].

Further comparisons between the derived multiconductor equations and measurements from poly-phase power distribution lines, under a variety of loading conditions, is presented in [16] and [17].

2. Derivation of Multiconductor Transfer Functions

Consider a transmission line system of n+1 conductors driven by an arbitrary source network and terminated by an arbitrary load network as shown in Figure 1.
Figure 1. Multiconductor Transmission Line Configuration

We can collect the conductor voltages and currents at any point along the line, \( x \), in vectors as follows,

\[
\mathbf{V}(x) = [v_1(x), v_2(x), \ldots, v_n(x)]^T \tag{1}
\]

\[
\mathbf{I}(x) = [i_1(x), i_2(x), \ldots, i_n(x)]^T \tag{2}
\]

Under suitable conditions, a transmission line system can be characterized by its per-unit parameters. Consider the three conductor case shown in Figure 2.
Figure 2. Three conductor per unit parameters.

We define the impedance per unit length matrix as,

\[
Z = \begin{bmatrix}
  z_{11} & z_{12} \\
  z_{12} & z_{22}
\end{bmatrix}
\]  \hspace{1cm} (3)

and the admittance per unit length matrix as,

\[
Y = \begin{bmatrix}
  y_{11} + y_{12} & -y_{12} \\
  -y_{12} & y_{22} + y_{12}
\end{bmatrix}
\]  \hspace{1cm} (4)

For general \( n+1 \) conductors,

\[
Z = \begin{bmatrix}
  z_{11} & z_{12} & \cdots & z_{1n} \\
  z_{12} & z_{22} & \cdots & z_{2n} \\
  \vdots & \vdots & \ddots & \vdots \\
  z_{1n} & \cdots & \cdots & z_{nn}
\end{bmatrix}
\]  \hspace{1cm} (5)
and,

\[
Y = \begin{bmatrix}
y_{11} + y_{12} + \cdots + y_{1n} & -y_{12} & \cdots & -y_{1n} \\
-y_{12} & y_{22} + y_{12} + \cdots + y_{2n} & \cdots & -y_{2n} \\
\vdots & \vdots & \ddots & \vdots \\
y_{1n} & \cdots & -y_{(n-1)n} & y_{nn} + y_{1n} + \cdots + y_{(n-1)n}
\end{bmatrix}
\]  \hspace{1cm} (6)

The vector differential equations for the general multiconductor transmission line can be written \[1,2,3\],

\[
\frac{\partial V(x)}{\partial x} = -Z I(x)
\]  \hspace{1cm} (7)

\[
\frac{\partial I(x)}{\partial x} = -Y V(x)
\]  \hspace{1cm} (8)

Solutions to the differential equations are \[1,2,3\],

\[
V(x) = e^{-\gamma x} V_w^+ + e^{+\gamma x} V_w^-
\]  \hspace{1cm} (9)

and

\[
I(x) = e^{-\gamma x} I_w^+ - e^{+\gamma x} I_w^-
\]  \hspace{1cm} (10)

In the above equations we have defined the propagation matrix \(\gamma = ZY\) \hspace{1cm} (11)
In (9) $V_w^+$ is the incident vector voltage at $x=0$, or at the source boundary
$V_w^-$ is the reflected vector voltage at the source boundary. Similarly for $I_w^+$
and $I_w^-$. Now, define the reflection coefficient at any point $x$, $\Gamma(x)$,

$$V_w^-(x) = \Gamma(x)V_w^+(x) \quad (12a)$$

$$\Gamma(x)e^{-\gamma x}V_w^+=e^{\gamma x}V_w^- \quad (12b)$$

Or,

$$V_w^- = e^{-\gamma x}\Gamma(x)e^{-\gamma x}V_w^+ \quad (13)$$

Clearly,

$$V_w^- = \Gamma(0) V_w^+ \quad (14)$$

where $\Gamma(0)$ is the reflection coefficient at the source boundary.

In deriving (9), a solution for the differential equations was,

$$V_w^+(x) = e^{-\gamma x}V_w^+ \quad (15)$$

By taking the derivative of (15) with respect to $x$ an using (7) we can
relate the forward travelling voltage vector and current,

$$I_w^+(x) = Y_0 e^{-\gamma x}V_w^+ \quad (16)$$

where we have defined the characteristic admittance matrix,
Define the input impedance at any point $x$,

$$V(x) = Z_{\text{in}}(x)I(x)$$  \hspace{1cm} (18)

Now, substitute for $V(x)$ and $I(x)$ based on (9) and (10) into (18). Next, eliminate $I^+_w$ and $I^-_w$ to obtain the following expression:

$$V^-_w = e^{-\gamma x} [Z_{\text{in}}(x)Y_0 + I]^{-1} [Z_{\text{in}}(x)Y_0 - I] e^{-\gamma x} V^+_w$$  \hspace{1cm} (19)

Compare (19) and (13) to obtain an expression for the reflection coefficient matrix,

$$\Gamma(x) = [Z_{\text{in}}(x)Y_0 + I]^{-1} [Z_{\text{in}}(x)Y_0 - I]$$  \hspace{1cm} (20)

Similarly the input impedance at any point can be written in terms of the reflection coefficient,

$$Z_{\text{in}}(x) = [I + \Gamma(x)] [I - \Gamma(x)]^{-1} Y_0^{-1}$$  \hspace{1cm} (21)

The reflection coefficient matrix at the load is,

$$\Gamma_L = \Gamma(L) = [Z_L Y_0 + I]^{-1} [Z_L Y_0 - I]$$  \hspace{1cm} (22)

The boundary condition at the source is [3],...
\[ \text{V}(0) = \text{V}_s - Z_s \text{I}(0) \]  
\[ (23) \]

Hence,
\[ \text{V}(0) = Z_{\text{in}}(0)[Z_s + Z_{\text{in}}(0)]^{-1} \text{V}_s \]  
\[ (24) \]

Write \( \text{V}(x) \) in terms of the incident voltage vector,
\[ \text{V}(x) = \left[ 1 + e^{-\gamma x} \right] e^{-\gamma x} \text{V}_w^+ \]  
\[ (25) \]

Let \( x=0 \) in (25),
\[ \text{V}_w^+ = \left[ 1 + \Gamma(0) \right]^{-1} \text{V}(0) \]  
\[ (26) \]

To obtain an expression for \( \text{V}(x) \) only in terms of the source voltage \( \text{V}_s \) and source and load impedances, eliminate \( \text{V}_w^+ \) between (25) and (26). Next substitute for \( \text{V}(0) \) from (24). After further substitutions as appropriate and some algebra we obtain,
\[ \text{V}(x) = \left[ 1 + e^{\gamma (x-1)} C_1 e^{\gamma(x-1)} \right] e^{-\gamma x} \left[ 1 - e^{-\gamma L} C_1 e^{-\gamma L} \right]^{-1} Z_0 \]
\[ Z_s + \left[ 1 + e^{-\gamma L} C_1 e^{-\gamma L} \right] \left[ 1 - e^{-\gamma L} C_1 e^{-\gamma L} \right]^{-1} Z_0 \] \( -1 \text{V}_s \)  
\[ (27) \]

Following the same procedure an expression for \( \text{I}(x) \) is found.
\[ \text{I}(x) = Y_0 \left[ 1 - e^{\gamma (x-1)} C_1 e^{\gamma(x-1)} \right] e^{-\gamma x} \left[ 1 - e^{-\gamma L} C_1 e^{-\gamma L} \right]^{-1} Z_0 \]
\[ Z_s + \left[ 1 + e^{-\gamma L} C_1 e^{-\gamma L} \right] \left[ 1 - e^{-\gamma L} C_1 e^{-\gamma L} \right]^{-1} Z_0 \] \( -1 \text{V}_s \)  
\[ (28) \]
An expression for the input impedance at any point $x$ along the transmission line system can be obtained in terms of the reflection coefficient at the load.

$$Z_{in}(x) = [1 + e^{\gamma(x-L)} Y_0]^{-1} Y_0 - e^{-\gamma x}[1 - e^{-\gamma L} Y_0]^{-1} Y_0$$  \hspace{1cm} (29)

By evaluating (27) and (28) at $x=0$, we can obtain the voltage vector and current vector transfer functions for the transmission line system:

$$V(x) = [1 + e^{\gamma(x-L)} Y_0]^{-1} Y_0 - e^{-\gamma x}[1 - e^{-\gamma L} Y_0]^{-1} V(0)$$  \hspace{1cm} (30)

$$I(x) = Y_0 [1 - e^{\gamma(x-L)} Y_0]^{-1} Y_0 - e^{-yL} [1 - e^{-\gamma L} Y_0]^{-1} Z_0 I(0)$$  \hspace{1cm} (31)

3. Two Conductor Transmission Line System

For two conductor transmission line systems the $n \times n$ matrices in the above equations are scalars. In this case equations (27) and (28) reduce to the two conductor forms [1],

$$v(x) = \frac{v_s z_0}{z_0 + z_s} \frac{e^{-\gamma x}(1 + \Gamma_L e^{-\gamma L x})}{1 - \Gamma_s \Gamma_L e^{-2\gamma L}}$$  \hspace{1cm} (32)

and

$$i(x) = \frac{v_s}{z_0 + z_s} \frac{e^{-\gamma x}(1 - \Gamma_L e^{-\gamma L x})}{1 - \Gamma_s \Gamma_L e^{-2\gamma L}}$$  \hspace{1cm} (33)

In the above expressions the source and load reflection coefficients are,

$$\Gamma_L = \frac{z_L - j}{z_0 \cdot z_L}$$  \hspace{1cm} (34)
and

\[ \Gamma_s = \frac{z_s - z_0}{z_s + z_0} \]  \hspace{1cm} (35)

The input impedance also reduces to,

\[ Z_{in}(x) = \frac{1 + \Gamma_l e^{-2\gamma L_x}}{1 - \Gamma_l e^{-2\gamma L_x}} Z_0 \]  \hspace{1cm} (36)
4. Summary of Derived Results

The equations necessary to solve a system of multiconductor transmission lines with arbitrary source and load termination networks derived in this paper are summarized in the Tables below. In the tables, \( x \) is the distance from the source toward the load along the transmission lines. The length of the transmission line system is \( L \).

<table>
<thead>
<tr>
<th>Table I.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Summary of equations to solve a multiconductor transmission line system with arbitrary source and load termination networks.</td>
</tr>
</tbody>
</table>

**Voltage vector**

\[
V(x) = [v_1(x), v_2(x), \ldots, v_n(x)]^T
\]

**Current vector**

\[
I(x) = [i_1(x), i_2(x), \ldots, i_n(x)]^T
\]

**Propagation matrix**

\[
\gamma = ZY
\]

**Characteristic admittance**

\[
Y_0 = Z^{-1} \gamma
\]

**Reflection Coefficient at the Load**

\[
\Gamma_L = \Gamma(L) = [Z_L Y_0 + I]^{-1} [Z_L Y_0 - I]
\]

**Conductor voltage at point \( x \) along conductor**

\[
V(x) = [I + e^{\chi x - L} \Gamma_L e^{\chi x - L}] e^{-\chi x} [I - e^{-\gamma L} \Gamma_L e^{-\gamma L}]^{-1} Z_0 \\
[Z_s + [I + e^{-\gamma L} \Gamma_L e^{-\gamma L}] [I - e^{-\gamma L} \Gamma_L e^{-\gamma L}]^{-1} Z_0]^{-1} V_s
\]

**Conductor current at point \( x \) along conductor**

\[
I(x) = Y_0 [I - e^{\chi x - L} \Gamma_L e^{\chi x - L}] e^{-\chi x} [I - e^{-\gamma L} \Gamma_L e^{-\gamma L}]^{-1} Z_0 \\
[Z_s + [I + e^{-\gamma L} \Gamma_L e^{-\gamma L}] [I - e^{-\gamma L} \Gamma_L e^{-\gamma L}]^{-1} Z_0]^{-1} V_s
\]

**Input Impedance at distance \( x \) looking towards load**

\[
Z_{in}(x) = [I + e^{\chi x - L} \Gamma_L e^{\chi x - L}] [I - e^{\chi x - L} \Gamma_L e^{\chi x - L}]^{-1} Y_0^{-1}
\]
Table II.

<table>
<thead>
<tr>
<th>Voltage transfer function</th>
</tr>
</thead>
<tbody>
<tr>
<td>[ V(x) = [I + e^{\gamma x - L} e^{\gamma x - L}] e^{-\gamma x} \left[ I - e^{-\gamma L} \Gamma e^{-\gamma L} \right]^{-1} V(0) ]</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Current transfer function</th>
</tr>
</thead>
<tbody>
<tr>
<td>[ I(x) = Y_0 \left[ I - e^{\gamma x - L} \Gamma e^{\gamma x - L} \right] e^{-\gamma x} \left[ I - e^{-\gamma L} \Gamma e^{-\gamma L} \right]^{-1} Z_0 I(0) ]</td>
</tr>
</tbody>
</table>

5. Comparison with Published Experimental and Computer Results

In this section the expressions derived in the paper will be verified and checked with published experimental and computer models for three and four conductor coupled transmission line systems.

5.1 Reduction of Inductive Coupling by Reducing Cross-section

In Figure 3 we show a three conductor system consisting of two parallel wires above a ground plane. Consider the coupling from the generator wire 1 to the receptor wire 2. The per-unit-length mutual inductance between the generator circuit and the receptor circuit is related to the cross-sectional area between the receptor wire and the ground plane. This is because the generator circuit produces a magnetic flux, and the mutual inductance is directly related to the portion of this flux which penetrates the area between the receptor wire and the ground plane shown in the shaded region in Figure 3 [5].
Figure 3 Three conductor system

Now, consider Figure 4 in which a third wire 3 has been added on the receptor side. This wire reduces the cross-section shown in the shaded region which in turn reduces the mutual inductive coupling. Thus, under certain conditions this configuration will result in less coupling than the configuration in Figure 3. Inductive coupling is dominant when the current is large, in other words, when heavy loads are used. Otherwise, capacitive coupling will dominate and the configuration in Figure 4 has no advantage over Figure 3 in terms of reducing coupling. These issues will be investigated using computer programs which calculate the coupled voltage and currents based on the equations derived in this paper.

Figure 4. Four conductor system
5.2 Four Conductor Transmission Line System

The multiconductor transmission line system to be investigated is shown in Figure 5. In this configuration the coupling between the two straight wires 2 and 3 onto the single wire 1 is of interest. In the following we let,

\[ Z_{S11} = 0; \quad Z_{S23} = Z_{L11} = Z_{L23} = R. \]

We are interested in the amount of far-end coupling (voltage across \( Z_{L11} \)) as the value of \( R \) is changed from 1 Ohm, to 50 Ohms and 1000 Ohms.

![Figure 5. Multiconductor transmission line circuit configuration](image)

The coupling geometry is shown in Figure 6. In the results to follow,

- \( h = 2 \) cm
- \( \Delta h = 0.00166 \) mm (66 mils)
- \( d = 2 \) cm
- \( L = 4.572 \) m (15 ft)
- \( r_{w1} = r_{w2} = r_{w3} = 0.406 \) mm (16 mils).

In the above, \( r_{wi}, i=1,3 \) is the radius of the conductor. The circuit configuration in Figure 5 and the coupling geometry are the same as those in [5] for the case of Straight Wire Pair (SWP) experiments and computer models (the only difference is the length which was 15 ft and 5 1/4 inch
The per unit inductance and capacitance matrix are calculated based on [7]. Losses are taken into account, using a quasi TEM mode approximation.

![Figure 6. Four conductor coupling geometry](image)

The results of the computer program which evaluates equations (27) for the various values of R is shown in Figure 7. In the Figure, the far-end crosstalk (voltage across $Z_{L11}$) is plotted against frequency.

![Two Wire Pair Coupling on Single Wire](image)

**Figure 8. Far-end crosstalk for various loads**

An examination of Figure 8 reveals that as the load is increased ($R$ decreases) the coupling is significantly reduced. This verifies the fact that
the two-wire configuration reduces coupling due to inductive coupling (high currents). As the load is decreased (R = 1000 Ohms) the coupling increases. With this load, the coupling is mainly capacitive and the two-wire configuration has no significant effect in reducing coupling. The results in Figure 8 agree very closely with the experimental and computer models in [5].

5.3 Three Conductor Coupling

In the following, a three conductor transmission line system is analyzed. The system consists of two parallel wires above a ground plane. The separation between the wires is 2 cm. Each wire is 2 cm above the ground plane. The wire radius was 0.406 mm (16 mils) for each conductor. The circuit configurations are exactly those of [6]. Specifically, Figure 9 corresponds to example 1, Figure 10 to example 2, and finally Figure 11 to example 3 in [6]. In [6] experimental and theoretical results are presented. The results presented here based on the multiconductor transmission line equations derived in [20] and presented in this paper agree exceptionally well with the experimental results of [6].
Near End Crosstalk Three Conductor System

Frequency, Hz

Near End Crosstalk, dB

Figure 9 (b).

Figure 9(a).
Figure 10(b).

Figure 10(a).
Near End Cross Talk Three Conductor System

Figure 11 (b).

Figure 11(a).
6. Conclusions

In this technical report we have presented a derivation of the voltage and current transfer functions of a system of multiconductor transmission lines. The new equations are very compact and suitable for computer modeling of multiconductor transmission line systems with arbitrary loads and sources.

The validity of the derived expressions was verified by comparing results predicted using these equations and published experimental and computer models.

7. References


