ZSIM: A NONLINEAR Z-DOMAIN SIMULATOR FOR DELTA-SIGMA MODULATORS

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ABSTRACT

In this report we present ZSIM, a nonlinear Z-domain SIMulator for sampled data systems, specifically for delta-sigma modulators. ZSIM integrates analytic tools, a difference equation simulator, a novel table-based nonlinear Z-domain simulator, and digital signal processing into a workstation environment. The primary goal of ZSIM is development of a fast and accurate simulator for delta-sigma modulators. The use of table-based simulation allows for simulation of circuit nonidealities including clock feed-through, nonlinearities, and hysteresis. We present high-level and low-level comparisons of difference-equation simulations and circuit-level simulations to verify the table-based ZSIM simulator. Simulations are presented for delta-sigma modulators used in voice-band CODECs and in the U-interface of an ISDN network terminator.

I. INTRODUCTION

We present a new simulator termed ZSIM for nonlinear Z-domain SIMulator for the fast and accurate simulation of sampled data systems. Speed and accuracy are achieved using tables to characterize each subsystem of a circuit, with the tables developed using circuit-level simulation provided by an external routine such as SPICE [1] and CAzM (Circuit Analyzer with Macromodeling) [2]. Here we apply ZSIM to the simulation and computer aided analysis and design (CAD) of delta-sigma modulators. ZSIM represents an extension of a difference equation simulation technique with multi-dimensional tables used to describe complex circuit interactions which cannot be captured by difference equations. ZSIM is the last component of a CAD tool for delta-sigma modulator design currently under development at North Carolina State University. The system integrates analytic tools [3, 4, 5] a difference equation simulator [3, 4], a table look-up simulator, and includes decimation and baseband filtering, and post-processing for the oversampled delta-sigma modulator.

Delta-sigma is one of a class of systems which use oversampling and 1-bit quantization to achieve high resolution A/D conversion. Recently they have received increased attention for use in voice-band CODECs [6] and for the U-interface of an Integrated Services Digital Network (ISDN) [7] as an alternative to conventional A/D converters. This is because they have looser tolerance requirements and can be fabricated using conventional digital MOS IC technology [8], thus dramaticly reducing costs. However, the implementation and wide-spread use of delta-sigma modulators is partly limited by the inadequacy of analytic and simulation tools since they contain a mix of continuous analog and sampled digital signals, as well as strong nonlinearities.

Until now numerical simulation of delta-sigma modulators has been restricted to the use of time-consuming circuit-level simulators (e.g. SPICE), and efficient though less accurate difference equation simulators [9]. The speed of simulation is of overwhelming importance as the circuit must be simulated for a large number of clock cycles, often tens of thousands. While being rapid, difference equation simulations cannot easily include component effects such as slew-rate limiting, noise, hysteresis, clock feed-through, and the nonlinearity associated with some types of comparators.

In the following sections, the concept of table simulation for delta-sigma modulators is detailed and benchmark comparisons of table-based simulations and difference equation simulations is presented. Timing comparisons for system-level simulation and circuit-level simulation are also presented.

II. CAD OF DELTA-SIGMA MODULATORS

The approach taken to integrating analytical, difference equation and circuit derived table-based difference equation simulators, and postprocessing is illustrated in Figure 1. Using the analytical tools developed in [3, 4, 5. 10, 11], the parameters of a candidate delta-sigma modulator are derived for desired system performance such as signal-to-distortion ratio. These parameters include the oversampling ratio, the order of the modulator (first, second, or third order), the gains for stable operation, the required length of

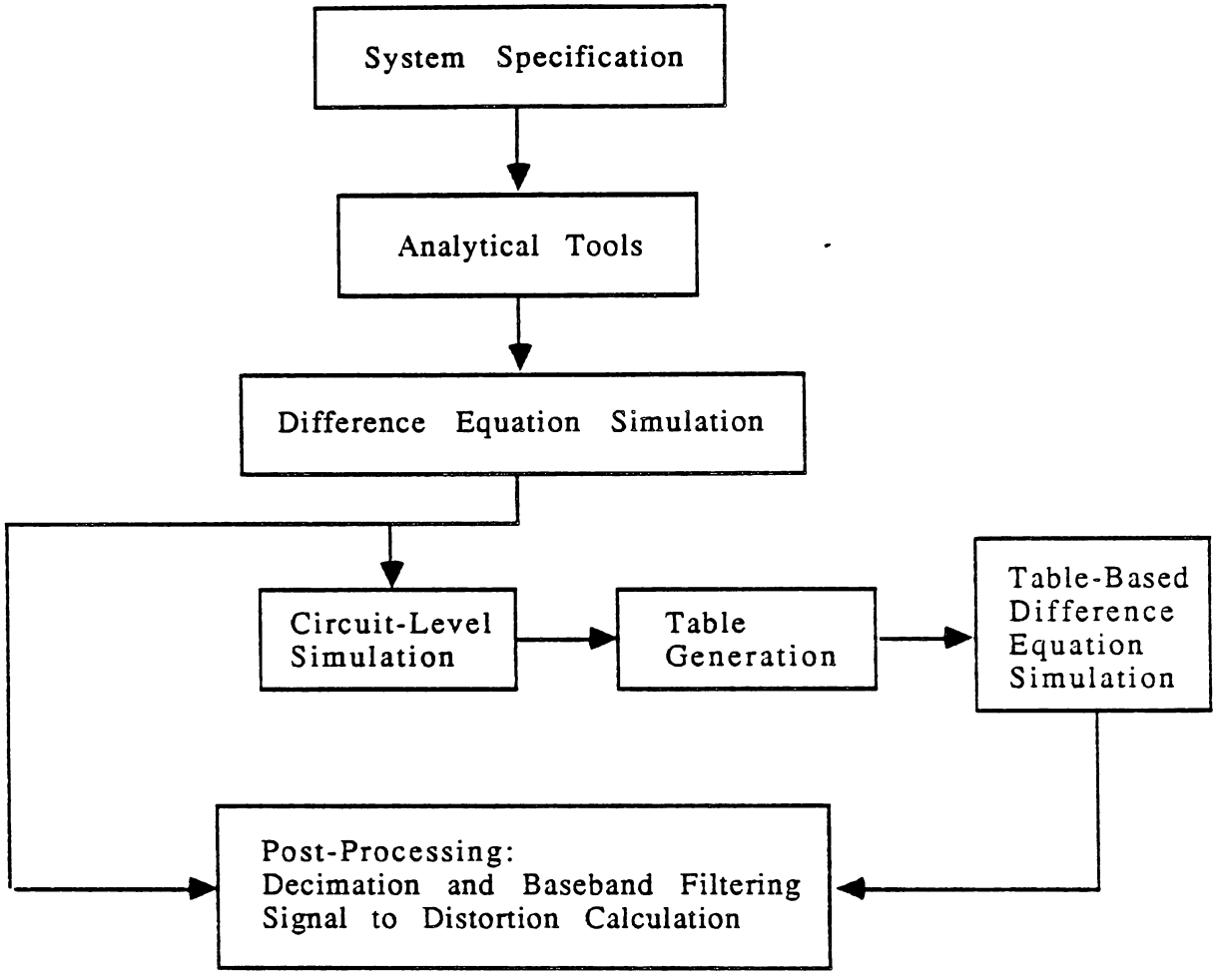

Figure 1: Flowchart of CAD tool for delta-sigma modulation

the decimation filter, the decimation weighting (uniform, triangular, or parabolic), and other parameters.

Difference equation simulations along with decimation, baseband filtering and post processing are performed to verify the performance of the modulator. At this stage, circuit-level implementations are considered in which, using circuit-level simulators such as SPICE, tables are generated for the subsystems that make up the modulator. Using these tables, ZSIM captures circuit-level nonidealities yet achieves rapid simulation as only subsystems are modeled.

During each stage of the design and simulation process the designer can iterate between the simulation systems and analytical tools to determine the circuit which is most appropriate in terms of complexity, technology, and other constraints.

III. DEVELOPMENT

As delta-sigma modulators are sampled data systems it is possible to model the performance of individual subsystems of the modulator at the sampling intervals. Continuous-time information, such as the circuit waveform between sampling intervals, and the circuit state at internal subsystem nodes are not required for accurate system-level simulation. Thus it is possible to use a z-domain description of the system. The utility of difference equation simulators is that they operate in the linear z-domain and so computations are kept to a minimum. Often, however, it is not possible to develop sufficiently accurate difference equations for practical delta-sigma modulators because of complex dependencies on circuit nonlinearity, hysteresis, clock feed-through, and slew-rate limiting of the subsystems. ZSIM, using table look-up techniques, is a natural extension of difference equation simulators and enables such effects to be modeled using a multi-dimensional table.

The implementation of ZSIM is analogous to that of the difference equation method. With the addition of fictitious sample and holds, a delta-sigma circuit can be represented in the z-domain as in Figure 2. This representation enables the subsystems to be considered individually by a table developed with the input and output loading on the subcircuits unchanged. Since practical monolithic implementation of delta-sigma modulators use sampled data circuits and/or switched-capacitor circuits, the addition of fictitious

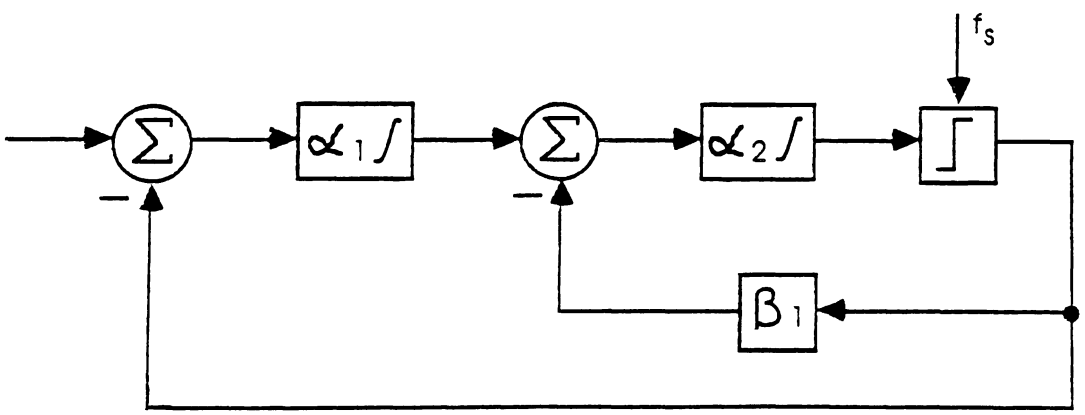

Figure 2: Block diagram of z-domain 2^{nd}-order delta-sigma modulator

sample and holds, if placed appropriately, has no effect on circuit performance.

ZSIM consists of three modules - a Table Generator Module, a Simulator Module, and a Post-Processor Module. The Table Generator Module develops the tables that describe the input-output characteristics of each subsystem. At present table generation has not been automated completely. In this work the table for a subsystem was developed using SPICE and CAzM simulations of the subcircuit for a number of cycles with a different set of initial conditions at each external node of the subsystem at each cycle. The feedback loops were cut but otherwise the connectivity of the circuit was not altered.

The Simulator Module implements simulation of the entire system using the table description of individual subsystems while difference equation simulation is available for rapid circuit investigations. Each table represents the response of a subsystem for discrete values of the inputs to the subsystem at, usually, the previous cycle and the current cycle. For intermediate values the table was linearly interpolated to determine the desired output. Note that the accuracy of the interpolation will improve as more table points are introduced into the table for a nonlinear region of operation, yet, the table method interpolates to the exact value in the linear regions of subcircuit operation. The Post-Processor Module implements decimation and baseband filtering and calculates system performance characteristics such as signal-to-distortion ratios.

IV. TABLES AND INTERPOLATION

In order to ensure that a table look-up simulation of a delta-sigma circuit is accurate, it must first be shown that the table look-up simulation produces the same results as the difference equation simulation. For this reason a table was generated for each integrator in the modulator shown in Figure 2. The difference equation of an ideal differential integrator is given by,

$$y[k] = y[k-1] + \alpha\,(\,x[k] - p[k]\,). \tag{1}$$

It is observed that the output of the integrator depends on three variables, denoted $T(x,y,p)$: the input signal $x[k]$ at the k^{th} clock cycle, the integrator output $y[k-1]$ at the previous cycle, and the current comparator output $p[k]$. Since $p[k]$, in this example, is the output of a binary comparator, it can assume only two values. The signals $x[k]$ and $y[k-1]$,however, range from each power rail, although $y[k]$ is limited by op-amp saturation. Thus, if N discrete values at equal intervals are selected for $x[k]$ and M discrete values for $y[k-1]$, a 2xNxM dimensional table will describe the operation of the integrator. Therefore, the table is essentially divided into two smaller tables, each representing one of the two possible values for $p[k]$, and reducing the dimensionality of each table to two.

After a comparator decision during circuit simulation, an integrator output becomes a function of two variables, $T(x,y)$. The input, $x[k]$, falls between two of the N discrete data points; the previous output, $y[k-1]$, falls between two of the M discrete data points. Thus, four $y[k]$'s are selected from the table: $T(x_1,y_1)$, $T(x_2,y_1)$, $T(x_1,y_2)$, $T(x_2,y_2)$. Using the actual $x[k]$ value, linear interpolation between $T(x_1,y_1)$ and $T(x_2,y_1)$ produces

$T(y_1)$, and interpolation between $T(x_1,y_2)$ and $T(x_2,y_2)$ yields $T(y_2)$. Then linear interpolation of $T(y_1)$ and $T(y_2)$ with $y[k-1]$ leads to the desired approximate of $y[k]$. A small error variance will occur at the output in the nonlinear regions of integrator operation due to the present choice of linear interpolation. With more elaborate interpolation routines and nonuniform interval tables, a more accurate model of the linear and nonlinear regions will be obtained with fewer table points. For the benchmark simulations to be presented, a 2x10x8 table for each integrator was generated.

V. SIMULATION RESULTS

High-Level Benchmark: Table vs. Difference Equation

A complete delta-sigma modulator system for a voiceband CODEC application is simulated using ZSIM's table simulator and difference equation simulator. A second order delta-sigma modulator was used with integrator gains $\alpha_1 = 0.1$ and $\alpha_2 = 0.5$, sampling frequency $f_s = 1.024$ MHz, and a 1 kHz input sinewave. The power supplies are $\pm$ 2.5 V. The digital output of the modulator is fed into a smoothing FIR decimation filter using parabolic weighting with 128 taps to provide the necessary out of band noise rejection [5, 12]. The sampling rate is reduced by a factor of 32 and the samples are then filtered using an IIR baseband (voice-band) filter to further attenuate and shape the frequency response. After baseband filtering, the sampling rate is reduced from 32 kHz to 8 kHz.

The gain of each integrator is chosen to ensure that saturation does not occur. Thus, modulator operates in the linear region of the integrators, so linear interpolation of the table points closely tracts the output value of the difference equation modeled.

Low-Level Benchmark: SPICE & CAzM Tables vs. Difference Equation

A delta-sigma modulator circuit was simulated using ZSIM to demonstrate the process of table generation and to show some real results. In a digital subscriber loop (ISDN) application, a baseband sampling frequency of 160 kHz was required with a resolution of 12 bits. A second-order delta-sigma modulator was used with a sampling rate of 5.12 MHz, integrator gains of $\alpha_1 = 0.1$ and $\alpha_2 = 0.5$, and an ideal comparator. The circuit topology is shown in Figure 3. Figure 4 shows the operational amplifier used for each integrator. A Class AB topology is used to insure fast operation, i.e., no slew-rate limiting will occur. The modulator requires only an FIR decimation filter, as used for the CODEC application.

ZSIM table simulations were performed for two sets of tables. One set was generated by SPICE simulations and one set was generated by CAzM simulations. The purpose of two table sets is to compare the end results of ZSIM with respect to different types of circuit-level simulators. Specifically, CAzM used charge-based device models which will show better performance for switched-capacitor circuit simulations. A series of individual transient circuit simulations were performed to build up the tables one point at a time. A SPICE table and a CAzM table was constructed for each integrator. Figure 5 shows the

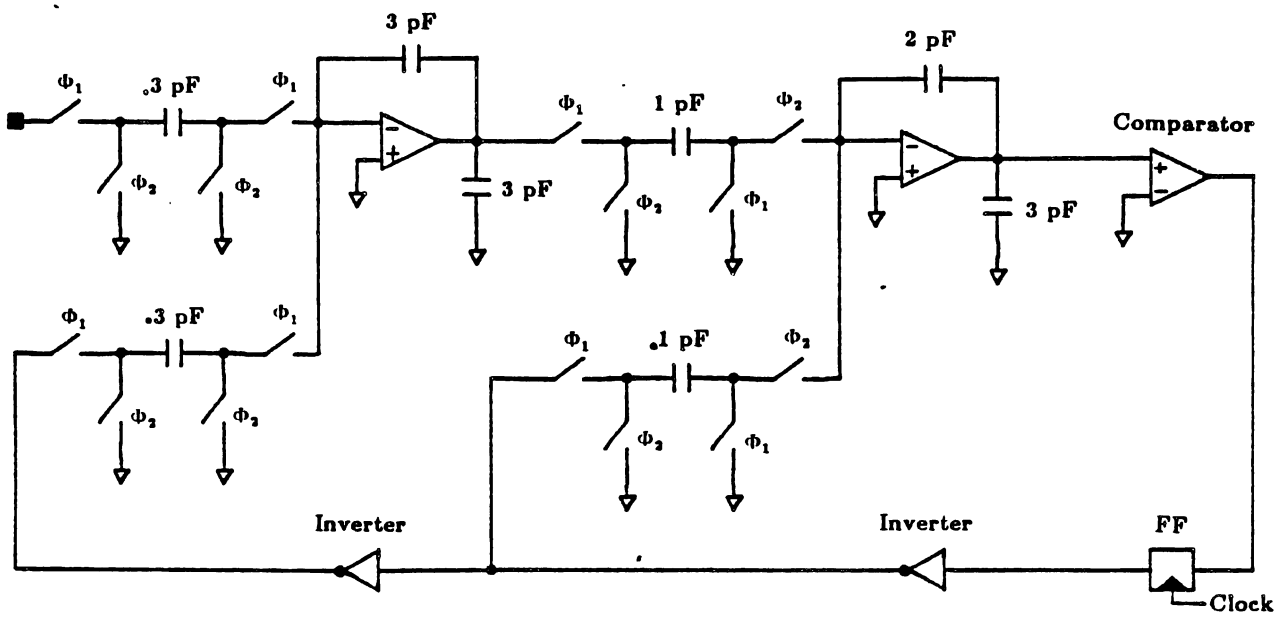

Figure 3: 2^{nd}-order delta-sigma switched-capacitor circuit

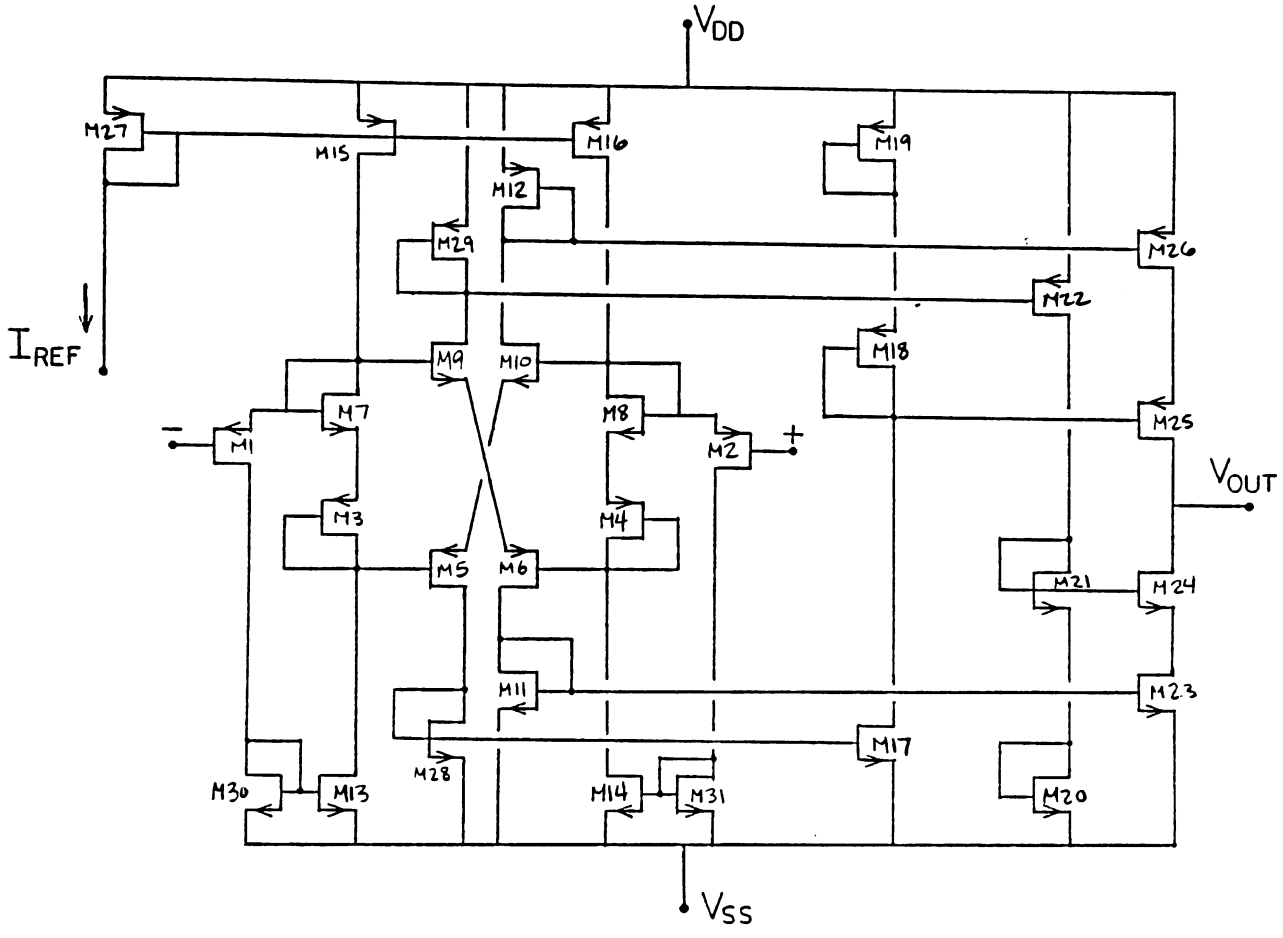

Figure 4: Class AB CMOS operational amplifier

graphical representation of the first integrator table generated by SPICE simulations. Figure 6 show SPICE's second integrator table. The tables generated by CAzM are similar and need not be shown here. However, the CAzM tables closer represent the ideal tables than the SPICE tables do. Both SPICE integrators exhibit differences in output of up to 20 mV, in some cases, when compared to the ideal difference equation solution, whereas CAzM showed differences of up to 4 mV. To compare SPICE and CAzM overall performance, a sample of data points was chosen from the tables representing the first integrator. The data point set represents all points for which $x[k] = -1.0$ V. The differential error is calculated for each data point as compared to the ideal difference equation solution for each input combination of $x[k]$, $y[k-1]$, and $p[k]$. The results are depicted in Figure 7. One should expect ZSIM simulations to show better performance when using CAzM tables rather than SPICE tables.

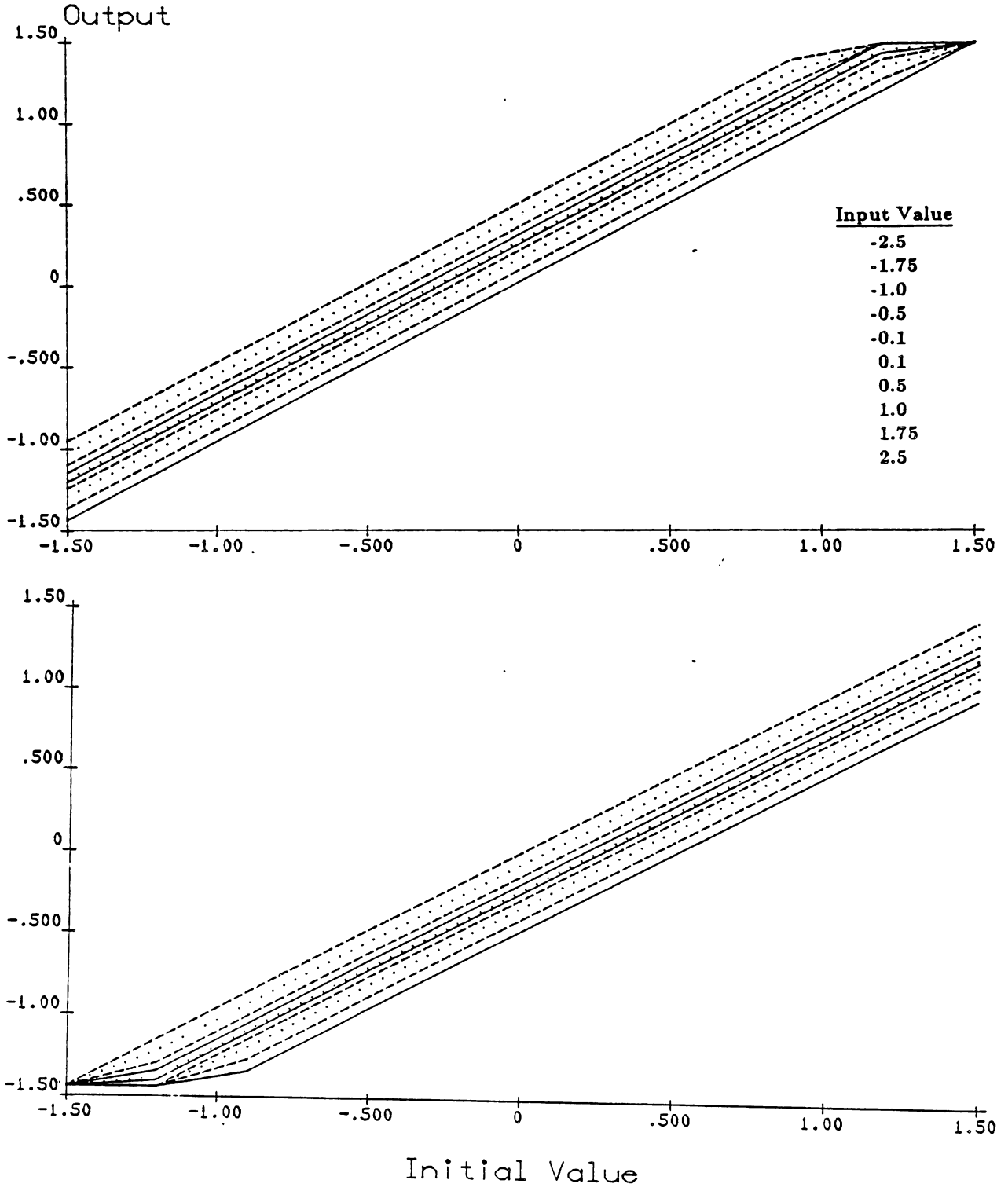

Figure 5: SPICE integrator #1 table for (a) $p[k] = -1$, (b) $p[k] = 1$

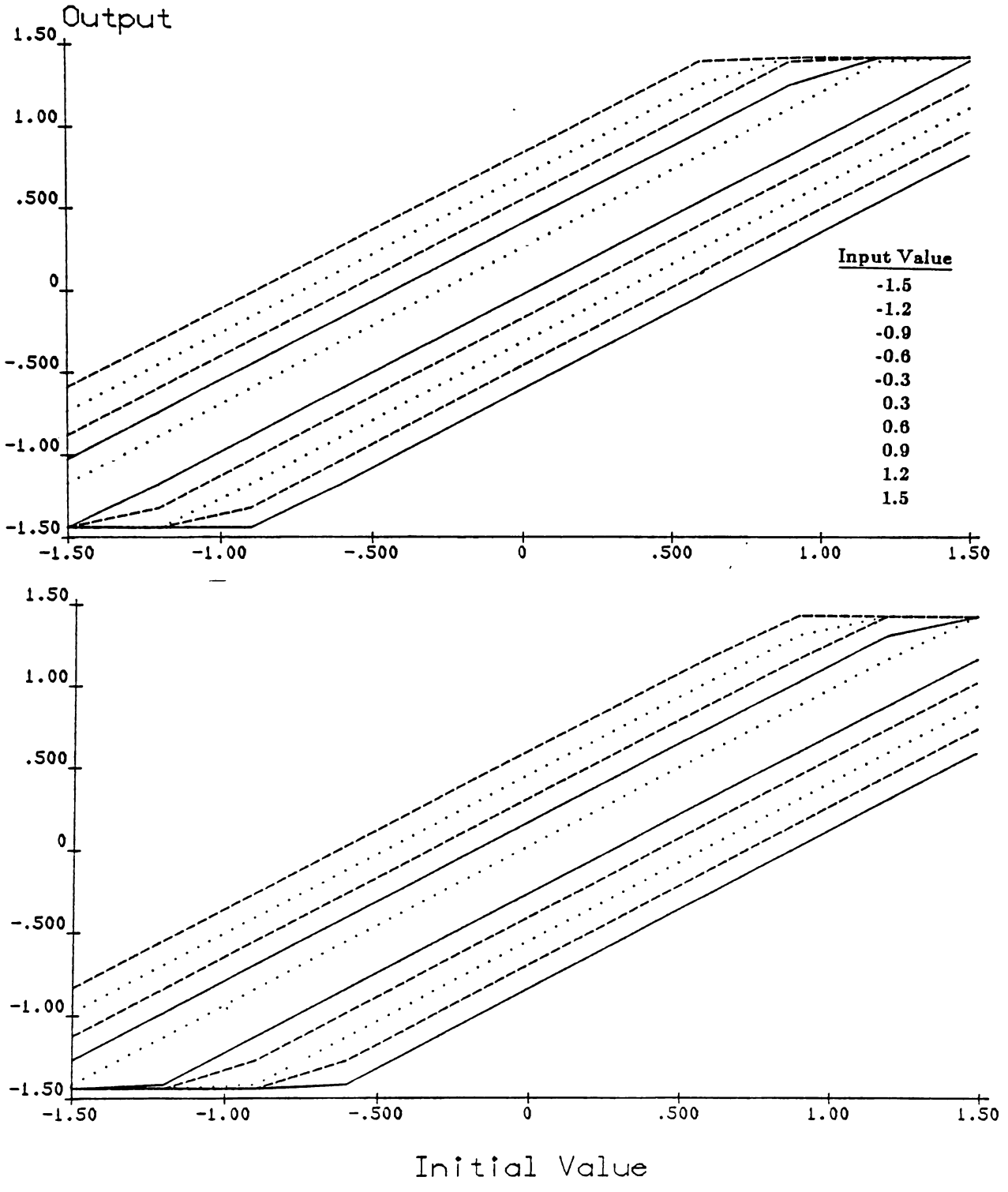

Figure 6: SPICE integrator #2 table for (a) $p[k] = -1$, (b) $p[k] = 1$

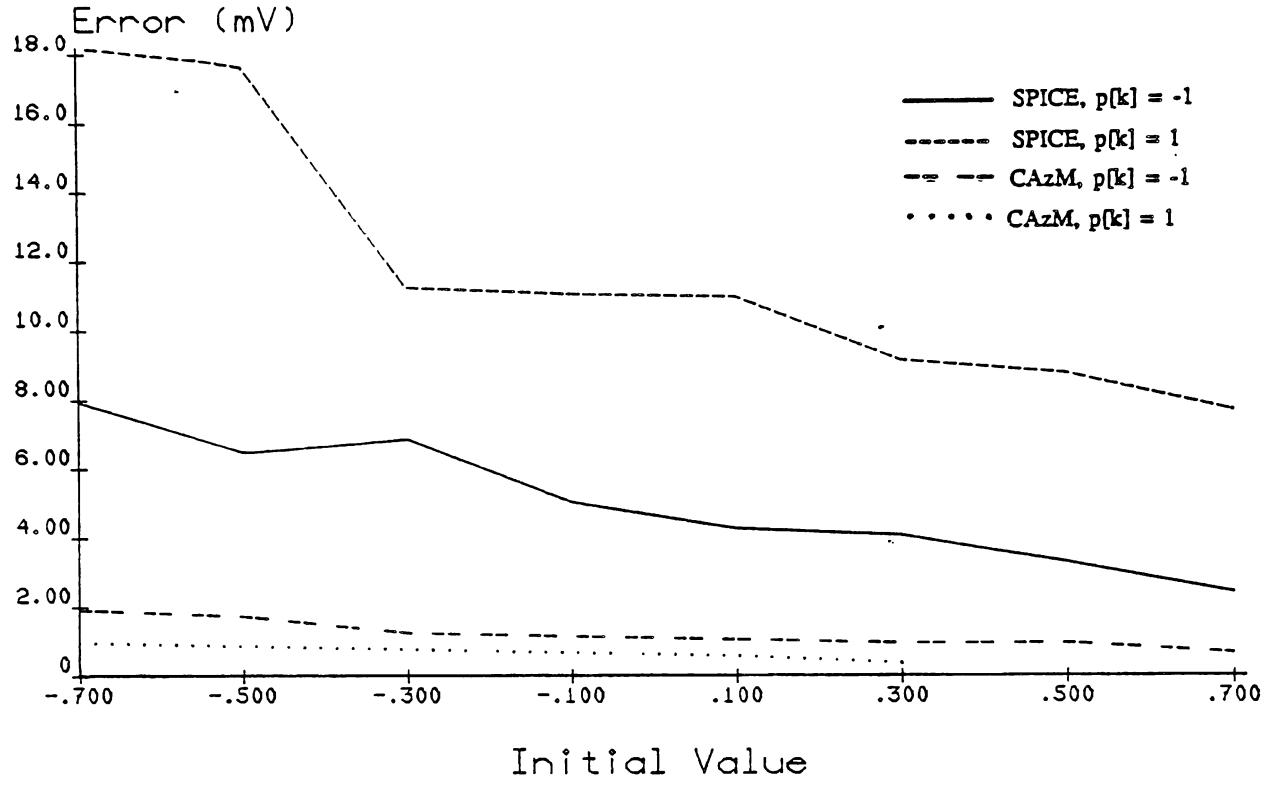

Figure 7: Circuit errors for SPICE and CAzM tables

ZSIM simulations were performed for the ISDN circuit using difference equations, SPICE tables, and CAzM tables. The purpose of these tests is to show that circuit nonlinearities are inherently modeled by the tables and therefore produce a degradation in overall system performance by introduction of noise into the simulation. Figure 8 shows the signal-to-distortion ratio for an input signal frequency of 32 kHz over a range of input signal levels, for each type of simulation. Notice that the SPICE table simulation exhibits a degradation is SDR performance over the entire input range when compared with its ideal counterpart. Notice that the performance of the circuit improves when using CAzM tables rather than SPICE tables. This result suggests that CAzM may have less numerical noise than SPICE or, more likely, that CAzM is free of charge conservation problems present in SPICE.

Further investigation of system performance shows an increase in circuit noise for frequencies less than the signal frequency when using SPICE tables rather than CAzM tables. This result can be seen in the baseband frequency spectra of Figure 9. The limited accuracy of the tables may possibly be the cause of the additional low frequency noise. Other nonlinearities captured by the circuit-level simulations include clock feedthrough, saturation, and finite slewing. However, most of the SDR degradation for the SPICE simulation is determined to be numerical noise, finite precision, and charge

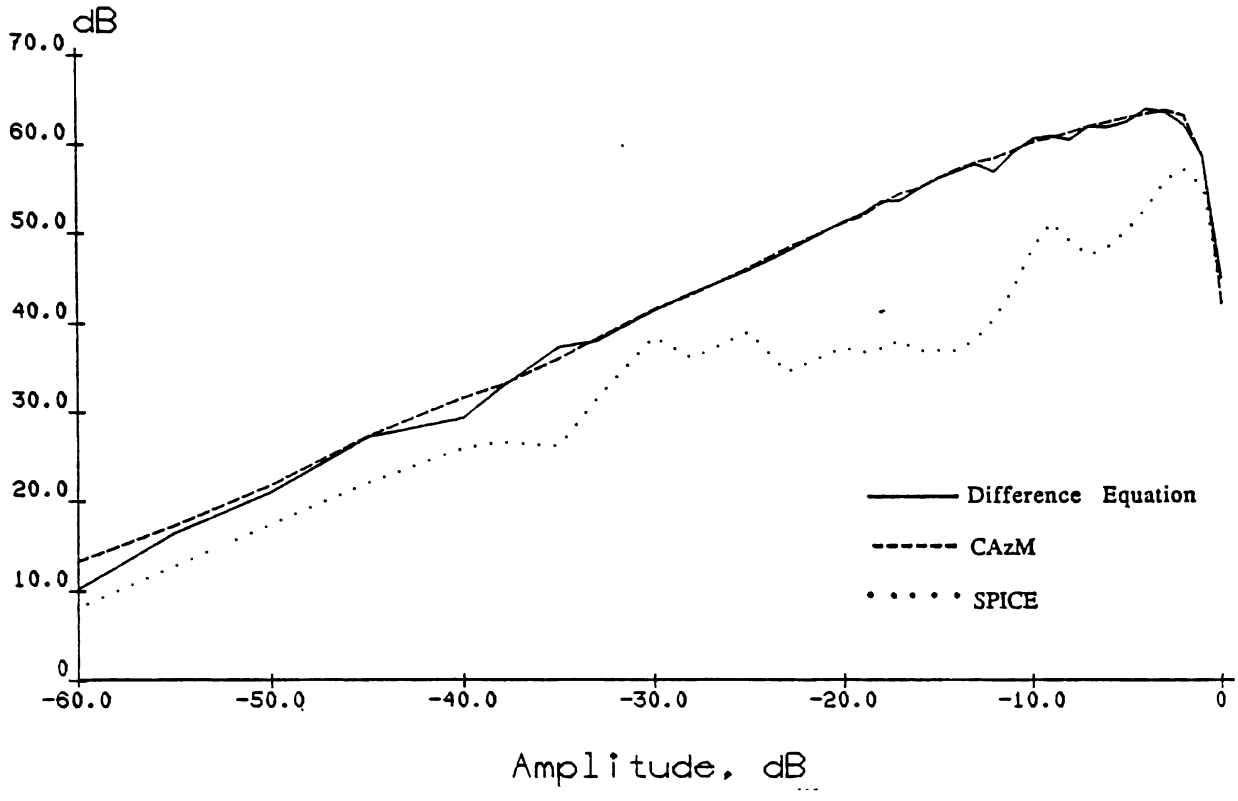

Figure 8: Signal-to-distortion ratio versus signal level

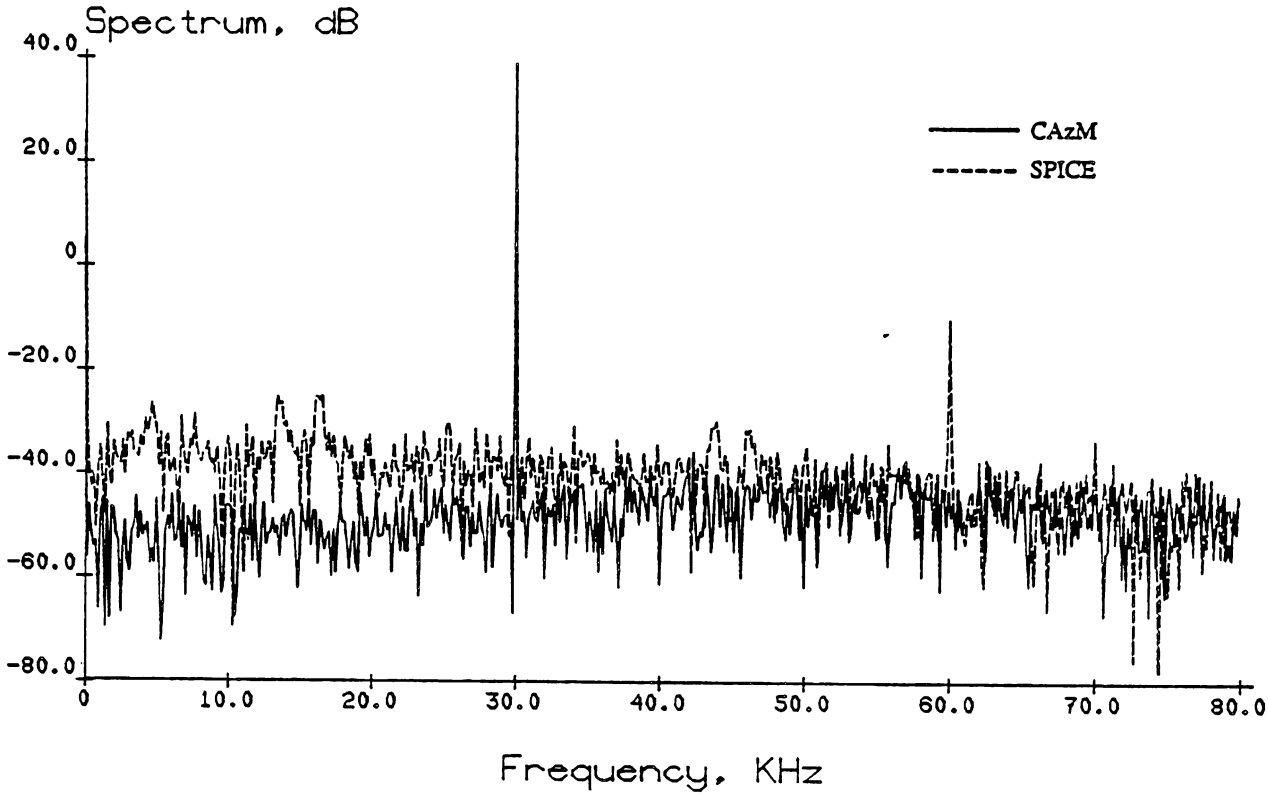

Figure 9: Baseband spectra for input = -10 dB

conservation problems. The spectrum for difference equation simulations has been excluded from Figure 9 since it is essentially the same as the CAzM result. Overall, CAzM has given better ZSIM results than SPICE, which can be attributed to CAzM's use of charge-based models. Clearly, the choice of a "good" circuit-level simulator is essential to creating table points that suppress numerical errors.

VI. COMPUTATION TIME COMPARISON

The primary goal of ZSIM is the fast simulation of delta-sigma modulators. Thus, the idea of table-based simulation is directed toward sampled-data systems that require a large number of clock cycles for circuit evaluation. In this section, simulation speed of ZSIM is compared to other simulation techniques (for a DEC MICROVAX II system).

Table 1 presents a timing comparison between ZSIM and SPICE for a signal-to-distortion ratio calculation of a first-order delta-sigma modulator with an ideal quantizer. Simulation is for one input signal level and 2^{16} clock cycles. First notice that the total simulation time, when ZSIM reads a table from memory, is only twice as long as the difference equation time. This factor is not a disadvantage since the table simulation is more accurate and includes all circuit nonlinearities.

Table 1. Run time comparison of difference equation, table, and SPICE simulation

	ZSIM			SPICE
	Table look-up simulation		Difference equation simulation	Circuit-level simulation
	first run	other runs		
generate table SPICE	1430 min	–	–	–
read table	–	1 min	–	–
simulation	3 min	3 min	1 min	780,970 min
digital signal processing	2 min	2 min	2 min	2 min
TOTAL TIME	1435 min	6 min	3 min	780,972 min

A 120 point table (2x6x10) is assumed for the integrator. Using the integrator discussed later in Chapter 4, a SPICE simulation for one clock period takes 715 seconds. For 120 individual simulations, 1430 CPU minutes are required to generate a complete set of table values. ZSIM table simulation takes only 3 minutes and the SDR calculation takes only 2 minutes. Total time for a first-run ZSIM evaluation is then 1435 minutes (approximately 1 day). The estimated SPICE time is a prediction based on 715 seconds per clock cycle multiplied by the number of clock cycles (2^{16}), or 780,790 minutes (approximately 1.5 years). This estimated time does not included the extra time required to simulate a complete circuit which includes the comparator and the feedback path. Therefore, the ZSIM simulation shows approximately 550 times speed-up over SPICE. Note that once a table for a specific integrator is generated and stored in memory, additional simulations take only 6 minutes to evaluate the system. However, for each additional SPICE simulation, another 1.5 years is needed. Therefore, each subsequent run using ZSIM results in a 200,000 times speed-up over SPICE.

VII. CONCLUSIONS

In this paper the development of a CAD tool for delta-sigma modulation was described which incorporates analytical tools, difference equation simulation, and circuit-level simulation through the use of a novel table-based nonlinear z-domain simulator. The tool includes various post processing functions such as decimation and baseband filtering, and signal-to-distortion ratio calculations. Simulations comparing the direct difference equation and table-based nonlinear z-domain simulator were presented for an ISDN network terminator in which the baseband frequency spectrum and the signal-to-distortion ratio as a function of input signal amplitude for both cases agreed closely. It is

shown that table simulation maintains circuit-level simulation accuracy and increases simulation speed up to 5 orders of magnitude.

VIII. REFERENCES

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