CMOS Implementation of Image Deconvolution and Mean Field Annealing

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Abstract

We report the physical implementation of a small deconvolution circuit in discrete CMOS ICs on a printed circuit board as well as spice simulation results of several other image processing circuits. The circuit design for the actual implementation in CMOS ICs on PCB solves the deconvolution problem in the vector space of the estimated signal and therefore is well suited to regularization. For simplicity, the implemented blurring kernel was chosen small enough to obtain a stable circuit without regularization. Spice simulations of mean field annealing with piecewise constant Bayesian prior probability subcircuits for regularization are reported along with simulations of the simplest spatial inverse filters for deconvolution using inverters for gain and level 2 models of 2μ CMOS transistors extracted from MOSIS fabrication runs.

1 Image Formation Model

Images degraded by imperfect sensors or transmission can be modeled usefully[6] as the sum of random noise image and a convolution of the true image with a point spread function or blurring kernel. We will write

$$g = h * f + n, \tag{1}$$

for the degraded image and restrict ourselves to one dimensional discrete images so that g_i for $i = 1, 2, ..., L$ is the i^{th} pixel of L pixels in image g. Blurring is represented by the convolution of kernel h with the true signal f by the $*$ operator, defined by the relation

$$(h * f)_i = \sum_j h_{i-j} f_j \tag{2}$$

so that the i^{th} pixel of the convolved image $h * f$ is a weighted sum of pixels of f. Here we restrict ourselves to the case of a symmetric blur $h_{-i} = h_i$. Additive noise is effectively an image of random variables n_i where $i = 1, 2, ..., L$ are collected in n.

2 Image Restoration

The simplest approach to estimating f given the blurred image g and the blurring kernel h is to attempt to ignore the noise n and solve

$$g = h * f \tag{3}$$

in the Fourier domain. The resulting inverse filter is unstable[6]. The Weiner filter is stable but cannot adequately recover sharp edges[6]. Edges can be preserved by nonlinear Bayesian techniques, but these require global optimization such as simulated annealing[4] or mean field annealing[2, 5] The potential for implementing mean field annealing as a neural network in analog integrated circuits has been recognized previously[1].

Piecewise smooth *maximum a posteriori* or MAP restorations produce high quality results when implemented as numerical algorithms on general purpose digital computers. But even efficient serial implementations require several seconds to process a frame of video and therefore cannot be implemented in real time. Parallel implementations require perhaps two orders of magnitude less time[3] but this is still less than frame rate. Analog VSLI may allow real time implementation of mean field annealing of video images.

3 Deconvolution Circuit Simulation

The simplest deconvolution method is the spatial domain analog of inverse filter which attempts to solve $g = h * f$ for f at each pixel. The simplest circuit to implement this method is to put a resistive network model of the convolution in the negative feedback path of a differential amplifier whose noninverting input is the blurred image.

This input can be deconvolved by the following circuit which is implemented using only simple inverter as in digital applications.

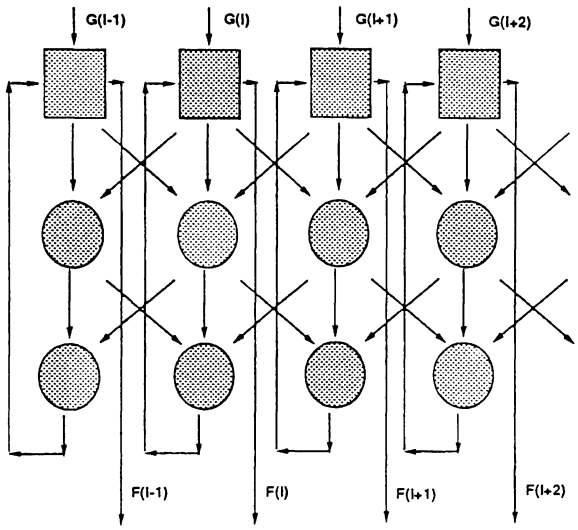

Figure 1: Neural network architecture for piecewise constant image restoration using mean field annealing previously reported[1].

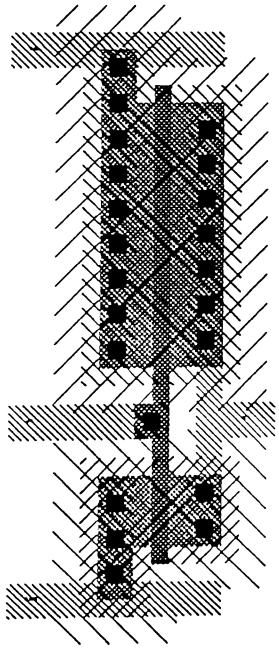

Figure 2: Magic layout of the simple inverting amplifier used in the circuit simulations.

```
*DECONVOLUTION NETWORK
x103 101 102 103 104 403 404 10 40 dcell
x203 201 202 203 204 103 104 10 40 dcell
x303 301 302 303 304 203 204 10 40 dcell
x403 401 402 403 404 303 304 10 40 dcell

*DECONVOLUTION CELL
.subckt dcell 1 2  3   4  5   6   10  40
r12 1 2 15k
x23 2 3 10 40 inv
r42 4 2 20k
r34 3 4 10k
r36 3 6 30k
r54 5 4 30k
.ends
```

This Deconvolution network uses a (usually digital) inverter as an analog inverting amplier. The spice description for this simple amplifier is shown below.

```
*INVERTER
.subckt inv   2   3  10  40
m1 10   2  3 10 CMOSP L=4.0U W=200U
m2  3   2 40 40 CMOSN L=4.0U W=51.0U
.ends
```

The MAGIC layout for the simple amplifier is shown in Figure 2. The Spice description as well as the Magic layout show that the PMOS width is about 4 times larger than the NMOS device as is required for matching the realistic models of transistors with the following level 2 CMOS parameters extracted from MOSIS fabrication runs.

```
*  These SCN-2.0um parameters taken from MOSIS
.MODEL CMOSN NMOS LEVEL=2 LD=0.250000U TOX=408.000001E-10
+ NSUB=6.264661E+15 VTO=0.77527 KP=5.518000E-05 GAMMA=0.5388
+ PHI=0.6 UO=652 UEXP=0.100942 UCRIT=93790.5
+ DELTA=1.000000E-06 VMAX=100000 XJ=0.250000U LAMBDA=2.752568E-03
+ NFS=2.06E+11 NEFF=1 NSS=1.000000E+10 TPG=1.000000
+ RSH=31.020000 CGDO=3.173845E-10 CGSO=3.173845E-10 CGBO=4.260832E-10
+ CJ=1.038500E-04 MJ=0.649379 CJSW=4.743300E-10 MJSW=0.326991 PB=0.800000
.MODEL CMOSP PMOS LEVEL=2 LD=0.213695U TOX=408.000001E-10
+ NSUB=5.574486E+15 VTO=-0.77048 KP=2.226000E-05 GAMMA=0.5083
+ PHI=0.6 UO=263.253 UEXP=0.169026 UCRIT=23491.2
+ DELTA=7.31456 VMAX=17079.4 XJ=0.250000U LAMBDA=1.427309E-02
+ NFS=2.77E+11 NEFF=1.001 NSS=1.000000E+10 TPG=-1.000000
+ RSH=88.940000 CGDO=2.712940E-10 CGSO=2.712940E-10 CGBO=3.651103E-10
+ CJ=2.375000E-04 MJ=0.532556 CJSW=2.707600E-10 MJSW=0.252466 PB=0.800000
```

For input,

```
v(101) = -5.99999e-01
v(201) = -2.00000e-01
v(301) = 0.000000e+00
v(401) = -2.00000e-01
```

which represents the negative of the image of an impulse blurred with kernel $h = [.2, .6, .2]^T$, the output from the deconvolution

```
v(103) = 1.139140e+00
v(203) = 1.010371e-02
v(303) = -2.31055e-01
v(403) = 1.010371e-02
```

```
v2 2 0 dc 0.8
v3 3 0 dc 0.9
v4 4 0 dc 1.0
v5 5 0 dc 1.1
v6 6 0 dc 1.9
v7 7 0 dc 2.0
v8 8 0 dc 2.1
v9 9 0 dc 2.2
```

Table 1: List of input voltages for MFA circuit simulation in Figure4.

shows that the signal to noise has been raised enough to reduce the tails of the estimated f by about over one order of magnitude. This circuit does not correct for overall magnitude.

Deconvolution by inversion is not stable, whether in the frequency domain or the space domain. Stability can be improved by regularization, which is equivalent to a Bayesian estimate. Regularization terms that result in linear problems cannot completely distinguish between high frequency edge features and noise. When the true signal is known to be piecewise smooth, a better regularization term is the sum of Gaussians of differences of adjacent pixels. The excellent quality results of such formulations are compromised only by the high numerical complexity of solving the resulting global optimization problem which we propose to to implement in silicon neural networks.

In this approach the optimal estimate is the image that minimizes

$$H[f] = |g - h * f|^2 + R[f] \tag{4}$$

where R is some regularization term. The gradient

$$\frac{\partial H}{\partial f} = h * (g - h * f) + \frac{\partial R}{\partial f}. \tag{5}$$

4 Deconvolution Circuit Implementation

Figure 3 shows a physical implementation of a Neural Net implementation using Equation 5 for the simplest case with $R = 0$ for 6 pixels. This circuit, like Figure 1, uses two layers of convolution: the first $h * f$ to estimate the error $g - h * f$, and the second to transform the error to the coordinate syste of the estimate f to which a term like $\frac{\partial R}{\partial f}$ can be added.

In Figure 3, the inputs are controlled by potentiometers and determine the brightness of LEDs at the bottom of the picture. The output is read from corresponding LEDs at the top of the picture. This circuit implements the kernel $h = [.1, .8, .1]^T$ and the picture shows the potentiometers adjusted to present $g = [0, 0, .1, .8, .1, 0]^T$ so that the proper output is $f = [0, 0, 0, 1, 0, 0]^T$ as is observed.

5 MFA Circuit Simulation

For all but the simplest functions R in Equation 5, a Neural Net implementation based on Equation 5 has many stable operating points and cannot be used without forcing the circuit to terminate in the optimal state. This can be done by introducing a temperature into the R and annealing[1]. Such a circuit has been designed and simulated in Spice with the results shown in Figure 4. This has no blur but does have significant additive noise and prior probability function very similar to the summed Gaussian of the first differences previously reported[1]. The input is a constant degraded by adding a small ramp signal, visible at low reciprocal temperature on the left and in the following Spice table of input voltages. As the control voltage corresponding to temperature is reduced, the input splits to become piecewise smooth. It appears possible to implement this circuit in analog VLSI for operation at video frame rate.

References

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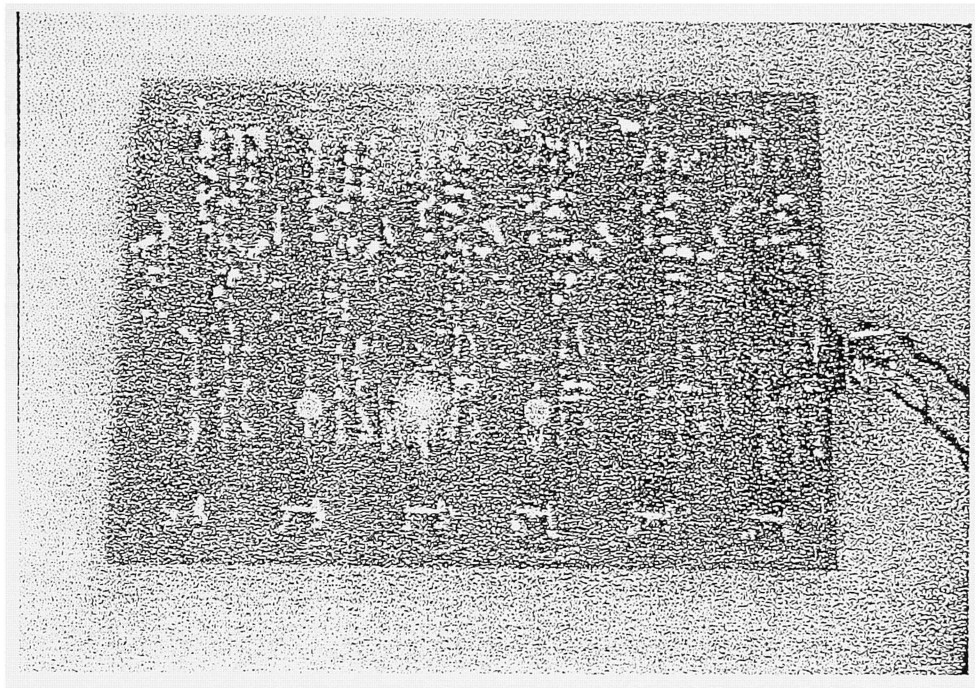
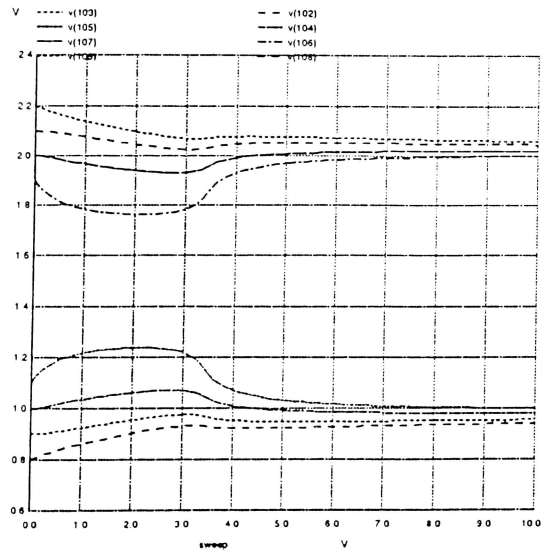
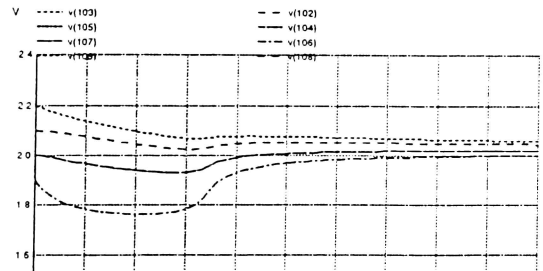


Figure 3: Implementation of a 6 pixel deconvolution using Equation 5 with $R = 0$.





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