Design-Time Yield Optimization for GaAs MESFET Fabrication

Griff L. Bilbro
David E. Stoneking
Robert J. Trew

Center for Communications and Signal Processing
Department Electrical and Computer Engineering
North Carolina State University

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G. L. Bilbro, D. E. Stoneking, and R. J. Trew
Department of Electrical and Computer Engineering
North Carolina State University
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Abstract

We have constructed a next-generation design tool for gallium arsenide transistors. Gallium arsenide transistors are fast, but their commercial development is impeded by low production yields. Our code predicts and optimizes production yield, and is in the final stages of computational verification to make it industrially useful.

1 Problem Description

Existing design tools for gallium arsenide (GaAs) transistors cannot predict yield because they do not model variations in physical parameters that are unavoidable in actual fabrication. These variations result in devices that deviate from specification. Devices that deviate too far from specification must be discarded. The fraction of acceptable devices is called the yield. GaAs devices typically have low yields which are costly and commercially unattractive.

We have developed code that predicts fabrication yield at design time, *before* prototyping the fabrication line. Moreover our code can adjust the initial design to optimize that yield. We are now conducting the computer experimentation to document the reliability of our predictions in the high dimensional design space of interest to industry.

The development of this process yield model is significant and is supported by a grant from the U. S. Government under the MIMIC program for Computer-Aided Design. We are cooperating with several industries now, including **GE, Hughes, ITT, Texas Instruments**, and **Raytheon**.

2 Objectives

Our objective is to predict fabrication statistics of GaAs MESFETs and to improve them at design time. The resulting code will facilitate the fabrication of next-generation high-speed transistors. It will shorten the design and development phases of a product life cycle by getting fabrication right the first time. We will publish our algorithm, our experimental evidence, our code, and the documentation for using the code.

3 Technical Approach

The yield of a specified nominal design can be estimated by combining a simulation of the device physics with a statistical simulation of fabrication disturbances. The KT model of the GaAs MESFET uses physics to predict electrical operating characteristics in terms of physical device parameters such as channel doping and gate geometry[3]. GaAs fabrication is imprecise enough that physical parameters of actual devices deviate considerably from nominal design values. The resulting deviations in device operation are too complex to model directly but the variations in physical parameters are simple and generic: they can be modeled by a multivariate Gaussian probability density with a mean at the nominal design and with a covariance that is independent of the nominal design.

Computation of yield is dominated by numerical analytic operations such as fast Fourier transforms and matrix manipulations. This numerical analysis is used to generate and evaluate a collection of devices stochastically sampled from the probability density of physical parameters. The yield optimizer iteratively improves an initial yield estimate.

4 Preliminary Results

The KT model was developed at NCSU in 1988 to understand MESFET operation in terms of the physics of electric fields and charge carrier density fields[3]. The model has been verified against MESFETs with various doping profiles from several manufacturers including GE, Hughes, ITT, Texas Instruments, and Raytheon. In addition to its practical utility, it provides a theoretical tool to develop and evaluate other models[2].

TEFLON was first applied to the problem of yield shortly after it was written[5, 4]. Those early yield studies confined themselves to variations in one parameter at a time and did not address yield optimization at all. However those studies resulted in the first estimates of relative sensitivity of yield to variations in different parameters, *e.g.* peak doping *verus* straggle.

Our current yield estimation code *does* treat correlations between the parameters and *does* adjust design parameters to optimize yield. It also supports a rich set of acceptability criteria involving any of 17 figures of merit including small signal gain, power added efficiency, and power at 1dB gain compression. Our current code has been accelerated by the introduction of several heuristics, including a high dimensional model of the objective[1].

Current yield estimates are consistent with earlier results when restricted to variations in a single parameter. In the multivariate case, the results are plausible and consistent with experience. The yield optimization code also performs as expected.

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