US006388286B1

(12) **United States Patent**
Baliga

(10) **Patent No.: US 6,388,286 B1**
(45) **Date of Patent: *May 14, 2002**

(54) **POWER SEMICONDUCTOR DEVICES HAVING TRENCH-BASED GATE ELECTRODES AND FIELD PLATES**

(75) Inventor: **Bantval Jayant Baliga**, Raleigh, NC (US)

(73) Assignee: **North Carolina State University**, Raleigh, NC (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **09/377,006**

(22) Filed: **Aug. 18, 1999**

Related U.S. Application Data

(63) Continuation-in-part of application No. 09/178,845, filed on Oct. 26, 1998, now Pat. No. 5,998,833.

(51) **Int. Cl.**[7] **H01L 29/76**; H01L 29/94; H01L 31/062; H01L 31/113; H01L 23/58

(52) **U.S. Cl.** **257/330**; 257/329; 257/331; 257/339; 257/488

(58) **Field of Search** 257/329, 330, 257/331, 332, 333, 334, 339, 488, 471, 476

(56) **References Cited**

U.S. PATENT DOCUMENTS

3,849,789	A	11/1974	Cordes et al.	357/15
4,646,115	A	2/1987	Shannon et al.	357/15
4,941,026	A	7/1990	Temple	357/23.4

(List continued on next page.)

FOREIGN PATENT DOCUMENTS

EP	0 580 452 A1	1/1994	257/330
JP	63-296282	2/1988	257/329
WO	WO 97/43789	11/1997	257/475

OTHER PUBLICATIONS

U.S. application No. 09/167,298, Filed Oct. 6, 1998, now abandoned.

Primary Examiner—Steven Loke
(74) *Attorney, Agent, or Firm*—Myers Bigel Sibley & Sajovec

(57) **ABSTRACT**

Integrated power semiconductor devices having improved high frequency switching performance, improved edge termination characteristics and reduced on-state resistance include GD-UMOSFET unit cells with upper trench-based gate electrodes and lower trench-based source electrodes. The use of the trench-based source electrode instead of a larger gate electrode reduces the gate-to-drain capacitance (C_{GD}) of the UMOSFET and improves switching speed by reducing the amount of gate charging and discharging current that is needed during high frequency operation. Methods according to the present invention also include the steps of forming a trench in a semiconductor substrate and then forming an insulated source electrode in and adjacent a bottom of the trench by forming a first electrically insulating layer on a bottom and sidewall of the trench, then forming a first electrically conductive layer on the first electrically insulating layer and then forming a second electrically insulating layer on the first electrically conductive layer using a thermal oxidation technique, for example. An insulated gate electrode is then formed in and adjacent a top of trench. Steps are also provided to form a source region of first conductivity type in the semiconductor substrate and form a second source electrode electrically connected to the source region and the insulated source electrode.

11 Claims, 10 Drawing Sheets