The Performance and Reliability of PMOSFET's with Ultrathin Silicon Nitride/Oxide Stacked Gate Dielectrics with Nitrided Si-SiO$_2$ Interfaces Prepared by Remote Plasma Enhanced CVD and Post-Deposition Rapid Thermal Annealing

Yider Wu, *Member, IEEE*, Gerald Lucovsky, *Member, IEEE*, and Yi-Mu Lee

***Abstract*—Ultrathin (∼1.9 nm) nitride/oxide (N/O) dual layer gate dielectrics have been prepared by the remote plasma enhanced chemical vapor deposition (RPECVD) of Si_3N_4 onto oxides. Compared to PMOSFET's with heavily doped p^+-poly-Si gates and oxide dielectrics, devices incorporating the RPECVD stacked nitrides display reduced tunneling current, effectively no boron penetration and improved interface characteristics. By preventing boron penetration into the bulk oxide and channel region, gate dielectric reliability and short channel effects are significantly improved. The hole mobility in devices with N/O dielectrics with equivalent oxide thickness between 1.8 nm and 3.0 nm is not significantly degraded. Because nitrogen is transported to the substrate/dielectric interface during post-deposition annealing, degradation of mobility during hot carrier stressing is significantly reduced for N/O devices. Compared with oxide, the tunneling current for N/O films with ∼1.9 nm equivalent oxide thickness is lower by about an order of magnitude due to the larger physical thickness. Suppression of boron transport in nitride layers is explained by a percolation model in which boron transport is blocked in sufficiently thick nitrides, and is proportional to the oxide fraction in oxynitride alloys.**

***Index Terms*—Boron penetration, gate dielectrics, nitride, N/O, oxide.**

I. Introduction

THE aggressive scaling of CMOS gate oxide thickness to below 2.0 nm for sub-0.25 μm technology is necessary to increase MOSFET drive currents and improve short channel behavior. Although the improvement in device performance is appreciable, boron penetration and direct tunneling current through the ultrathin gate oxides become severe issues for gate dielectric integrity. Tradeoff between boron penetration and polydepletion has been a critical issue in device engineering of PMOSFET's with p^+poly-Si gate electrodes. Numerous studies have attempted to reduce the boron diffusivity and increase resistance to hot carrier stress degradation by incorporating silicon oxynitride alloys formed by annealing thermal oxides in ammonia, or by alloy film growth in nitrous oxide [1]–[4]. However, using these techniques, high temperature processing is required to incorporate a sufficient amount of nitrogen at the Si-dielectric interface; the high process temperatures become even more critical as scaling continues. However, whereas the presence of nitrogen at the Si-dielectric interface was reported to suppress boron penetration into the Si substrate, it was also associated with a degradation of the peak hole channel mobility in PMOSFET's [5]. In addition, because peak nitrogen concentration is at substrate Si-dielectric interface for the high temperature nitridation processes, boron accumulates in the bulk of the oxide, resulting in increased concentrations of electron traps that degrade the oxide reliability [6], [7].

Direct tunneling introduces another major limitation on the scaling of gate dielectrics. Lo *et al.* claimed 2.0 nm to be the scaling limit of oxide, based on the tolerable standby power consideration; this is referenced to a 100 mW/chip for a power supply of 1 V [8]. However, the National Technology Roadmap for Semiconductors (NTRS) requires 1.5–2 nm to be the equivalent oxide thickness for FET's with 100 nm gate lengths, and 1.5 nm for 70 nm gate lengths. Therefore, alternative dielectrics with higher dielectric constants (so called high-k dielectrics) must be incorporated into the gate stack to suppress tunneling currents. Compared with oxides, high-k materials, such as Si_3N_4 and Ta_2O_5, allow the use of physically thicker films while maintaining the same dielectric capacitance. However, during the deposition and post-deposition annealing of many of these materials in an oxygen ambient, a thin layer of SiO_2 is formed between the high-k material and Si substrate [9]. This interfacial oxide reduces the expected capacitance from the high-k films to be less than what can be obtained from SiO_2 and the benefit of high-k dielectrics is reduced. In addition, many high-k dielectrics show a thermodynamic stability problem when contacting silicon, which results in the necessity of a top buffer layer and/or a metal gate, thereby increasing process complexity [10]. Finally, another tradeoff between barrier height and dielectric constant exists because the band gap, and therefore the barrier heights at conduction

Manuscript received December 16, 1998. This work was supported by the National Science Foundation, Office of Naval Research, and Semiconductor Research Center. The review of this paper was arranged by C. Y. Yang.

Y. Wu and Y. M. Lee are with the Department of Electrical and Computer Engineering, North Carolina State University, Raleigh, NC 27695-8202 USA (e-mail: wu@ncsu.edu).

G. Lucovsky is with the Department of Electrical and Computer Engineering and the Department of Physics, North Carolina State University, Raleigh, NC 27695-8202 USA.

Publisher Item Identifier S 0018-9383(00)05193-5.

0018–9383/00$10.00 © 2000 IEEE

and valence band edges, tends to decrease with increasing the dielectric constant [11].

Silicon nitride is a viable candidate for replacing silicon oxide because its dielectric constant is double that of oxide while demonstrating a conduction band and valence band off-set energies of $\sim$2 eV, and a dielectric strength of at least 10 MV/cm [12]. Additionally, the excellent thermal stability of silicon nitride makes it relatively easy to integrate nitride layers into gate stack processing, with minimum modification of current process technology. The drawback of nitrides to date has been in bulk defects, which degrade both performance and reliability. However, nitride films deposited by remote plasma enhanced chemical vapor deposition (RPECVD) at 300 °C and annealed at 900 °C have sufficient bonded hydrogen to reduce defect and defect-precursor concentrations to acceptable levels [13]–[15]. For example, compared with oxides of the same equivalent thickness, nitride/oxide dual layer gate dielectrics made with oxides and nitrides, both deposited by RPECVD, and in the 1.9 nm range have been reported to 1) yield comparable current drive to oxides, 2) reduce the tunneling current by about an order of magnitude, and 3) improve reliability for NMOSFET's devices [15]. In a previous publication, we have discussed preliminary results for PMOSFET's with dielectric equivalent thickness $>$3 nm [14]. In this paper, we report the integration of ultrathin ($<$2.0 nm) nitride/oxide stack gate dielectrics in PMOSFET's. Nitride layers were prepared by low-temperature RPECVD and a low-thermal-budget rapid thermal anneal (RTA) for 30 s at 900 °C was performed for structural and chemical relaxation [13]. This annealing also drives nitrogen atoms to the oxide/silicon interface to form a high quality interface, thereby creating an N/O/N device structure, in which the O and N layers in the bulk thin films with thicknesses of at least several molecular layers, i.e., $>$0.5 nm, while the interface nitrogen concentration is in the monolayer regime [14]. The effectiveness of these top nitride films in stopping boron penetration was studied with PMOS capacitors by monitoring flat band voltage shifts and poly-Si depletion. It has been shown that 0.8 nm of nitride effectively suppresses boron transport out of p^+ poly gates even with a high thermal budget dopant activation condition. Since the boron diffusion barrier is located at the polysilicon/nitride interface, the N/O dual layer dielectrics with nitrided Si-dielectric interfaces show improved dielectric reliability compared with oxides by preventing boron accumulation in the oxide bulk and at the Si-dielectric interface [7]. Compared with SiO_2, the tunneling current through these N/O/N gate stacks is lower by about an order of magnitude and the breakdown field is improved. Boron transport in silicon nitride and silicon oxynitride was also studied in order to identify the microscopic origin of the improved PMOSFET performance. A thickness of 0.8 nm of nitride has been found to block boron diffusion for annealing up to 4 min at 1000 °C. By maintaining a fixed barrier layer thickness and substituting RPECVD oxynitrides for the RPECVD nitride layers, it is demonstrated that the boron transport in silicon oxynitride films proceeds via hopping between oxygen atoms in a percolation-like process. To confirm this model, boron diffusion in oxynitride alloys was also studied for a fixed nitrogen areal density with increasing oxynitride alloy thickness [16]. With areal density of nitrogen equal to that of a 0.8 nm nitride, but with increased thickness of 1.1 nm, no boron penetration was observed for a lightly-diluted oxynitride alloy, $(SiO_2)_{0.3}(Si_3N_4)_{0.7}$, whereas boron penetration was observed for a more heavily diluted alloy, $(SiO_2)_{0.7}(Si_3N_4)_{0.3}$, even though the thickness was significantly increased to 2.7 nm. These experiments are consistent with a *site percolation* mechanism for boron transport in oxynitride alloys. Finally, we suggest a microscopic mechanism for the site percolation that additionally explains the blocking power of nitrogen atoms in the oxynitride alloys, as well as in bulk nitrides.

II. Experimental

The p-channel MOS devices with p^+-poly-Si gate electrodes were fabricated on n-type Si(100) substrates. RCA clean followed by diluted HF dip was used to clean wafers before field and gate oxidation. Some wafers were implanted with phosphorous to increase the channel doping for these PMOSFET's. Bottom oxides were grown by either 1) thermal oxidation in oxygen with 4.5% HCl at 800 °C for thicknesses of 1.5 nm to 4.0 nm, or 2) remote plasma oxidation in N_2O at 300 °C for an approximately 0.6 nm thickness. The low-temperature plasma oxidation process provides improved thickness control with respect to furnace oxidation process for oxides in sub-1.0 nm range. This was followed by the RPECVD nitride depositions in a range for $\sim$0.2 to $\sim$2.4 nm [13]. In the RPECVD process, active nitrogen species, e.g., N-atoms, metastables and ions, form a remotely excited He/N_2 mixture are combined with downstream-injected SiH_4 to deposit heavily hydrogenated nitride films ([H] $\sim$ 20–25 %). The substrate temperature is 300 °C, and the process pressure is 0.2 torr. The top nitride layer thickness was measured by Auger electron spectroscopy [17] and confirmed by spectroscopic ellipsometry. Post-deposition annealing of the N/O stacked dielectrics were performed in He at 900°C for 30 s [13], [16]. This annealing does several things. It drives nitrogen to oxide/substrate interface to form the bottom nitride layer of the resulting N/O/N stack; it reduces the hydrogen concentration by about a factor of two [16]; and it minimizes bonding defects in the top nitride layer by forming additional Si-N bonds, from sites that have lost H atoms during the 900 °C anneal [18]. Boron implantion at a level of 5×10^{15}/cm^2, and implant energy of 20 KeV, was used to implant 0.2 μm thick poly-silicon for the p^+ gate electrode. It was followed by the deposition of 200 nm LTO onto polysilicon layer to prevent boron out-diffusion during dopant activation anneals, ranging from 950 °C to 1000 °C for 1 min. After deposition and patterning of Al for gate, source and drain contacts, a conventional post metallization anneal (PMA) in forming gas (N_2/H_2) at 400 °C was performed for 30 min. The equivalent oxide electrical thickness ($T_{\text{ox-eq}}$) was determined by capacitance–voltage (*C*–*V*) measurement with capacitors biased in the accumulation region using a quantum mechanical correction [19]. PMOSFET's with thermal oxides were fabricated as control devices. Because the bottom oxide thickness is measured by ellipsometry, some uncertainty might be introduced to the N/O thickness ratio for the ultrathin dielectrics.

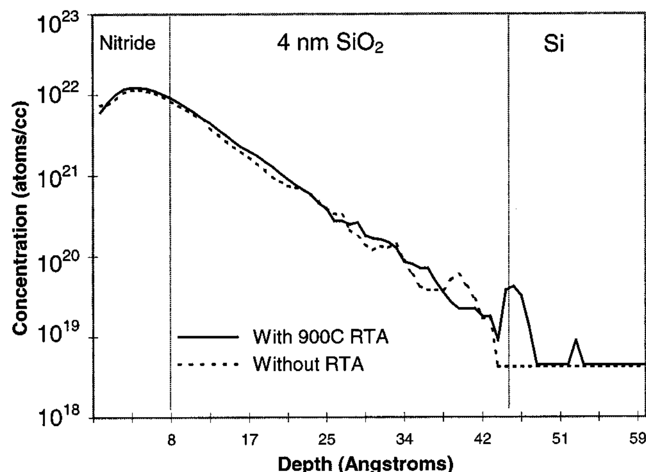
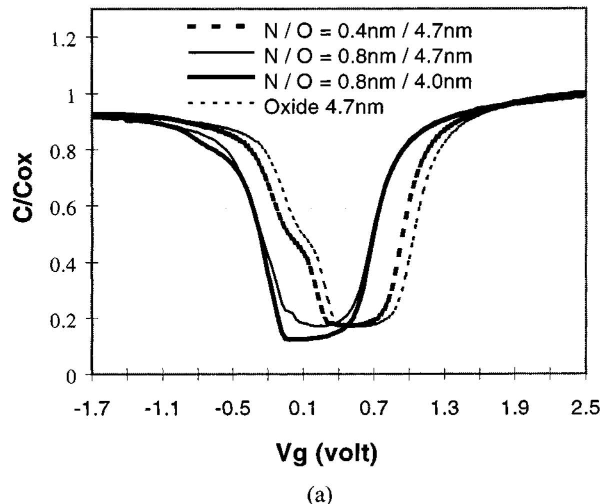


Fig. 1. Nitrogen profile determined by SIMS analysis for a nitride/oxide (∼0.8 nm/4.0 nm) dual layer gate dielectrics before and after a 900 °C post-deposition RTA.



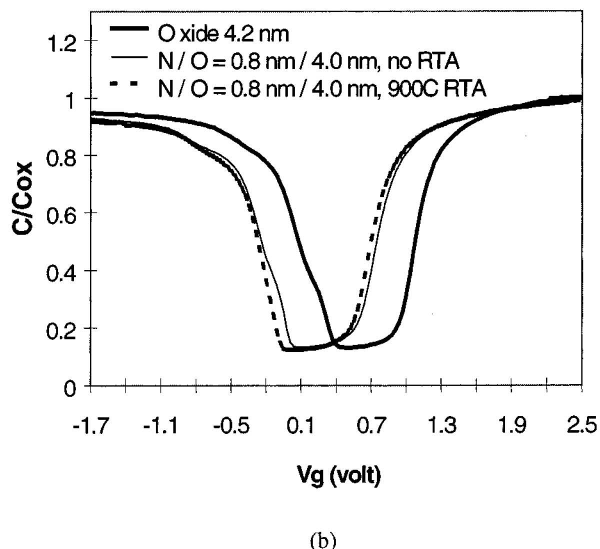


Fig. 2. Normalized quasistatic C–V curves for (a) MOS capacitors with oxide and oxide/nitride dielectrics with 0.4 nm and 0.8 nm top nitride films deposited by remote PECVD. (b) Demonstrates the effects of post-nitride-deposition annealing effect on boron penetration for devices with these N/O films.

III. Results and Discussion

A. Boron Diffusion Barrier

SIMS analysis of a nitride/oxide ∼ 0.8 nm/4.0 nm dual layer structure was performed as shown in Fig. 1. The *trailing* of the nitrogen signal into the oxide is an artifact of the SIMS analysis method. After annealing at 900 °C for 30 s, a distinct nitrogen peak appears at the oxide/silicon interface, showing that N-atoms diffuse into, and pile up at the oxide/silicon interface during the anneal. The Si-N bonds at the interface replace Si-O bonds, relieving interface strain due to the smaller effective size of the nitrogen atoms, thereby providing a physically smoother interface with less suboxide bonding in the oxide [20]. This enhanced smoothness of the oxide/silicon interface also contributes to the increased high field mobility reported for electrons in nitrided oxide [5].

With a 0.8 nm ultrathin nitride layer on the top of oxide, the N/O PMOS capacitor with the nitrided interface shows a significant improvement on the suppression of boron penetration to the Si-SiO_2 interface compared to thermal oxide PMOS devices, in which boron atoms are transported into the Si substrate. Fig. 2(a) contains the superposition of normalized quasistatic C–V curves for capacitors with the control oxide, and N/O/N stacked dielectrics in which the deposited nitride layers are either ∼0.4 nm or ∼0.8 nm thick. The C–V curve for control oxide is shifted to the more positive voltage, approximately +0.5 V with respect to the capacitor with 0.8 nm top nitride. Based on the anticipated value of flatband voltage as determined from the substrate and gate electrode doping, the large shift of the reference oxide flat-band voltage indicates significant boron penetration to the substrate [21]. The flatband voltage shift of capacitor with 0.4 nm top nitride film is intermediate, which indicates that the amount of boron diffusion can be controlled for a fixed thermal budget by simply changing the top nitride layer thickness.

Additionally, an enhanced boron blocking capability associated with post-nitride-deposition annealing is observed by monitoring the C–V curve shift in Fig. 2(b). The annealing of RPECVD nitride film at 900 °C for 30 s prior to the poly-Si deposition, implantation and activation anneal, drives out excess hydrogen, densifies the film, and minimizes bonding defects in the nitride layer, therefore further retards the diffusion of boron through the top nitride during the activation anneal. As displayed in Fig. 2(b), the C–V curve for N/O film without annealing shows a small shift to the positive voltage with respect to N/O film with the post-deposition RTA. This indicates a small amount of boron migrates through the nonannealed nitride films into the substrate. Additionally, the C–V exhibits curve distortion at the onset of inversion region for the nonannealed N/O film.

For the high substrate doping devices with the ultrathin oxide layers, <3 nm, the conventional C–V technique is no longer effective on extracting D_{it} because of the large ΔD_{it} uncertainties associated with poly-depletion, quantum effects in the

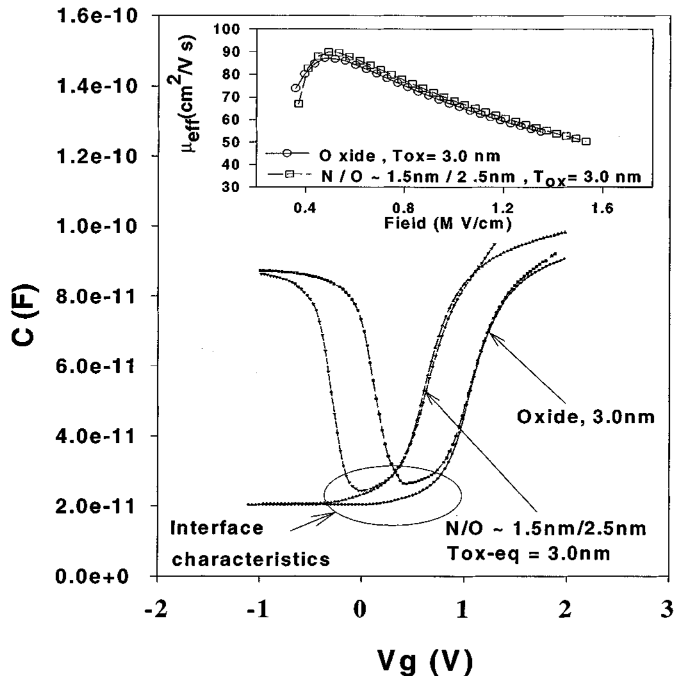


Fig. 3. Devices with N/O dielectrics and nitrided interfaces display low interface defect densities as indicated by comparing the separation between of high frequency and quasistatic *C–V* curves at the onset of inversion. The insert shows the effective mobility for these devices with N/O and oxide dielectrics with $T_{\text{ox-eq}}$ = 3.0 nm.

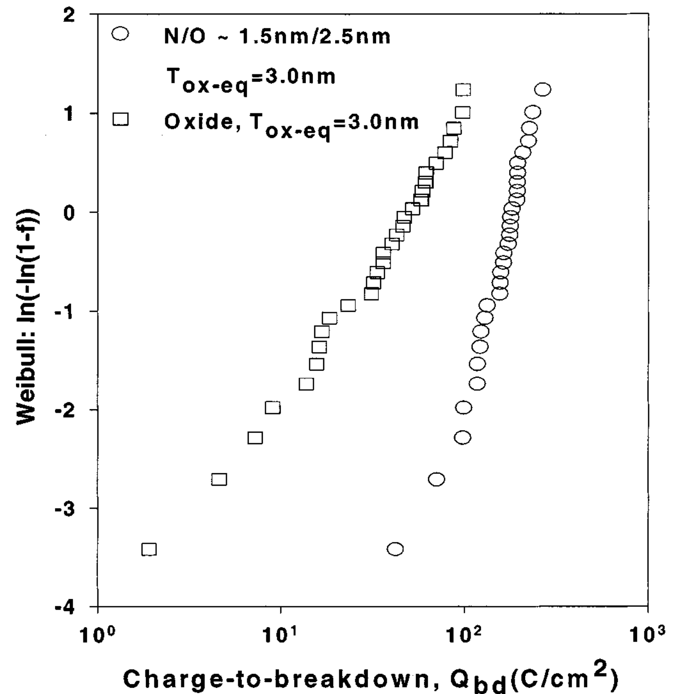


Fig. 4. Weibull plots of Q_{bd} as shown for capacitors with 3.0 nm N/O and oxide dielectrics under a constant substrate injection current stressing at a current density of 500 mA/cm^2.

channel region, and nonuniform substrate doping. However, because the interface state density determines the deviation of high-low frequency *C–V* curves at the onset of inversion region, this deviation can still be used to compare the oxide interface quality. Interface quality for devices with N/O gate stacks with nitrided interfaces, and oxide devices, each with an equivalent oxide thickness ~3.0 nm are compared in Fig. 3. It is clear that the deviation between the high frequency and quasistatic *C–V* curves at the onset of inversion is reduced for the device with the N/O dielectric, indicating a reduced interface defect state density. This is at least in part attributed to the incorporation of nitrogen at oxide/substrate interface during the post-nitride-deposition annealing. Additionally, it has been observed that the field dependence of the hole channel mobility in the PMOSFET device with the stacked N/O/N gate dielectric is essentially identical to that of device with the oxide dielectric; this indicates the advantage of the low temperature RPECVD process in maintaining the oxide/substrate interface integrity with bottom oxide thickness at the range of 2.5 nm.

Locating the nitrogen peak on the top of oxide as a diffusion barrier is another advantage of the N/O dual layer structure for boron doped p-poly PMOS devices. Previous studies have shown that the nitrogen concentration peaks are at the bottom of nitrided oxides grown by oxidation in NO or N_2O. Since boron transport is stopped at the Si-SiO_2 interface, this nitridation approach allows an accumulation of boron in the oxide bulk, degrading the dielectric reliability compared to oxides grown in O_2 without nitrogen incorporation [6]. However, by preventing boron from diffusing into the oxide bulk by the top nitride layer, the N/O dual layer dielectric reliability is improved significantly compared to the devices with O_2 oxide. Fig. 4 shows Weibull plots for gate dielectrics with $T_{\text{ox-eq}}$ ~3.0 nm under a substrate injection stress of 500 mA/cm^2. The charge to breakdown is improved by about an order of magnitude in N/O devices. The improved reliability for the N/O dual layer dielectrics is attributed to the reduction of boron associated defects in the oxide bulk and near the Si-SiO_2 interface, which cause the reliability degradation for the NO, N_2O, and O_2 oxide devices.

B. PMOSFET's with p^+ Poly-Si Gate Electrodes

It is well-established that PMOSFET's with p^+ poly-Si gate electrodes and oxide gate dielectrics suffer from the boron penetration into channel region, which results in the flatband voltage shifts and enhanced short channel effects [2], [3]. In marked contrast, PMOSFET's with p^+ poly-Si gate electrodes and N/O stacked gate dielectrics with nitrided Si-SiO_2 interfaces display improved short channel effects because of the excellent boron blocking capability of the top nitride layer. Fig. 5 shows the threshold voltage dependence on the effective channel length for PMOSFET's with oxide and N/O dielectrics. The threshold voltage is determined by the extrapolation of the linear I_{ds}-V_{gs} slope at the maximum transconductance on the V_{gs} axis, with a drain bias of −0.05 V. While the devices with stacked N/O dielectrics maintain essentially the same threshold voltage (~ −0.6 V) down to 0.5 μm effective channel length, the devices with oxide gate dielectrics show threshold voltage roll-off for devices with channel lengths shorter than $L_{\text{eff}} \sim 0.7$ μm, due to an enhanced short channel effect resulting from the boron penetration [22]. Fig. 6 shows the I_d-V_d characteristics with an effective channel length ~0.5 μm for PMOSFET devices with p^+ poly-Si gates with both stacked N/O and homogeneous

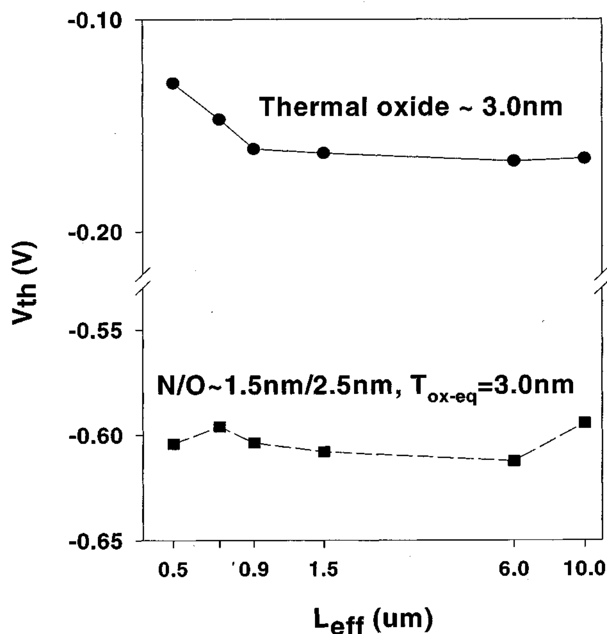


Fig. 5. Variation of threshold voltage vs. $L_{\rm eff}$ for PMOSFET's with N/O and oxide dielectrics. The threshold voltage roll-off is observed for oxide device starting from 0.7 μm.

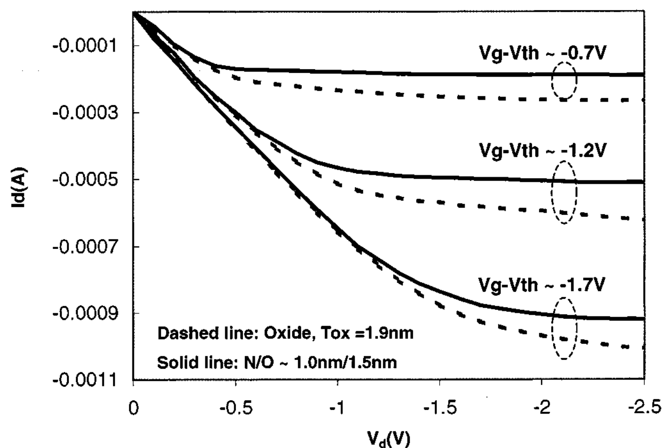


Fig. 6. I_d–V_d characteristics for PMOSFET's with p$^+$-poly Si gates and 1.9 nm N/O dual layer (solid line) and oxide (dashed line) dielectrics. The effective channel length is 0.5 μm.

oxide gate dielectrics with the same oxide equivalent thickness of approximately 1.9 nm. The device with the stacked N/O dielectric shows improved saturation characteristics with respect to the device with homogeneous oxide dielectric. The reduced trend to saturation on the I_d-V_d curves for the device with the oxide dielectric is another possible indicative of an enhanced short channel effect associated with boron penetration into the channel region [2]. For the devices with oxide dielectric, the resultant peaked boron concentration at the oxide/substrate interface moves the channel away from the interface, and therefore results in poorer gate electrode control of the channel potential profile.

I_d–V_g characteristics for PMOSFET's with channel lengths of 0.8 μm and an oxide equivalent thickness of ~1.9 nm are shown in Fig. 7. By preventing boron from entering the channel region, the subthreshold slope is improved from 99 mV/decade for the device with the oxide dielectric to 82 mV/decade for the device with the N/O dielectrics. In addition, the impact of a reduced tunneling current in the sub-2.0 nm region is reflected in an improved transistor off-state characteristic. In Fig. 7, the device with the N/O dielectric shows a good turn off characteristic, with the off-state leakage current coming mostly from junction leakage. However, the device with the oxide dielectric shows a significantly increased off-state leakage current by an order of magnitude for a 0.5 volt gate bias range. This rapid increase in leakage current is due to the large direct gate tunneling current through the oxide. This can result in a high standby power dissipation and limit the use of sub-2.0 nm devices with homogeneous oxide gate dielectrics.

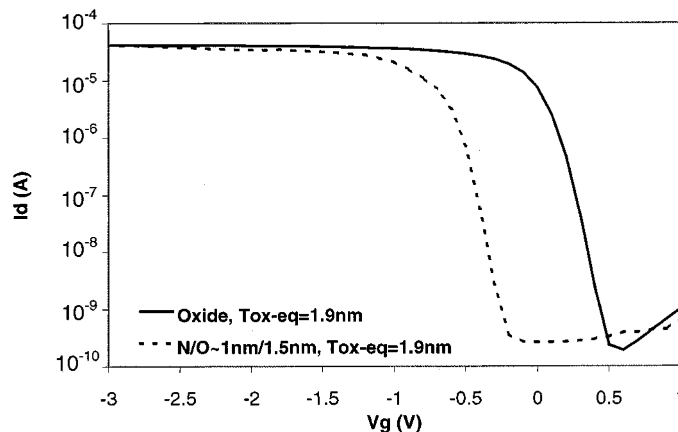


Fig. 7. I_d–V_g characteristics for PMOSFET's (L/W = 0.8 μm/20 μm) with oxide and N/O dielectrics for $T_{\rm ox\text{-}eq}$ = 1.9 nm. The increased off-state leakage current for oxide device is indicative of a larger tunneling current.

The effective mobility of devices with N/O and oxide were extracted from I_d-V_g curves in the linear region in the conventional way with $V_d = -0.05$ V. Large dimension transistors (W/L = 100 μm/100 μm for $T_{\rm ox\text{-}eq}$ ~ 3.0 nm, 20 μm/20 μm for $T_{\rm ox\text{-}eq}$ ~ 2.0 nm) are used to avoid the uncertainties from the source/drain series resistance and lithography. It has been shown in the insert in Fig. 3 that almost identical effective channel hole mobilities were obtained for PMOSFET's with N/O and oxide dielectrics for oxide equivalent thickness in the 3-nm range. The bottom oxide had a thickness of ~2.5 nm for the device with the N/O stacked dielectric. Fig. 8(a) and (b) show the mobilities for devices with stacked N/O dielectrics for scaling the effective oxide thickness down to 1.9–nm range. Devices with two different bottom oxides, ~1.5 nm and ~0.6 nm, were used to monitor the effect of oxide thickness on the channel mobility. As shown in Fig. 8(a), the N/O device with a bottom oxide thickness of 1.5 nm displayed a field dependent channel mobility essentially equal to that of the device with the oxide dielectric. Furthermore, the N/O device shows an improvement on the high field mobility due to the incorporation of nitrogen at the interface during the post-nitride-deposition annealing. However, when the bottom oxide thickness was reduced to ~0.6 nm, as shown in Fig. 8(b) we observed about a 10% mobility degradation for device with the N/O dielectric as compared to the device with the oxide device. Since the decrease in hole mobility is essentially independent of electric field, this effect is not due

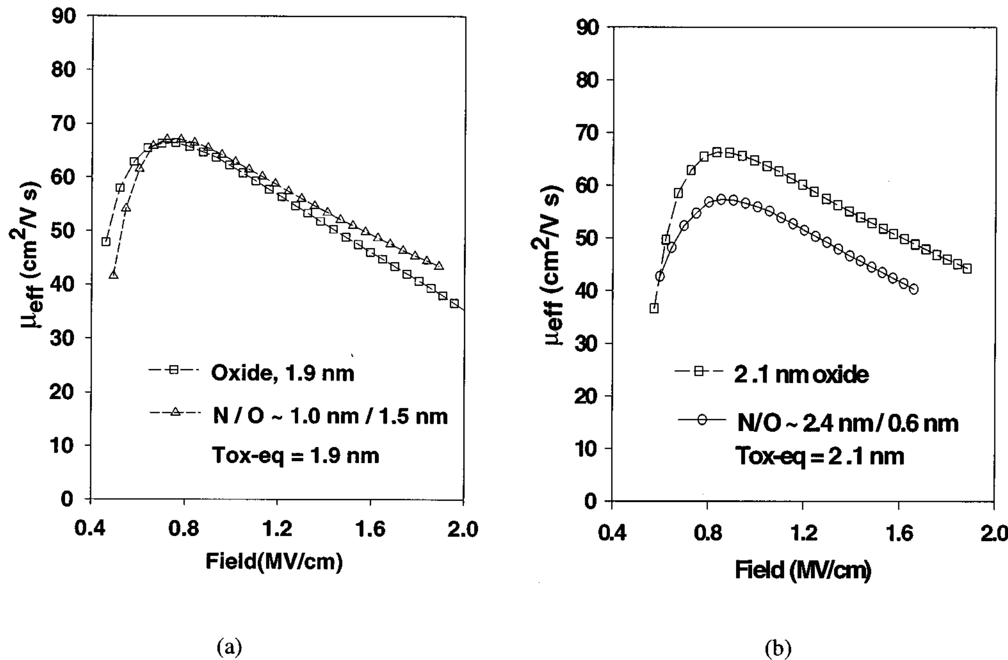


Fig. 8. Effective hole mobility verses effective normal field of PMOSFET's for oxide and N/O dual layer gate dielectrics with $T_{\text{ox-eq}} \sim 2.0$ nm. (a) is a device with an N/O dielectric with a bottom oxide thickness of 1.5 nm, and (b) an N/O device with 0.6 nm thick bottom oxide. The substrate doping is $1.1 \times 10^{18}/\text{cm}^3$.

to increased surface roughness. This aspect of the mobility-field relationship is consistent with other studies that incorporation of nitride at the interface leads to the improved high field mobilities in NMOSFET's [23]. As noted above, the 0.6 nm bottom oxide in Fig. 8(b) is grown by the N_2O remote plasma oxidation process because it is difficult to control the thickness below 1.0 nm by conventional thermal oxidation process. Previous studies [24], [25] have shown that oxidation in N_2O leads to monolayer interface nitridation, paralleling the effects of nitrogen transport to the Si-SiO_2 interface as shown in Fig. 1. A shift of peak mobility for device with the 0.6 nm bottom oxide to higher gate voltages, as indicated in Fig. 8, is due mostly to a higher substrate doping density, $\sim 5 \times 10^{17}$ cm^{-3} for the device with the N/O 1.0 nm/1.5 nm stack, and $\sim 1.1 \times 10^{18}$ cm^{-3} for the device with the 2.4 nm/0.6 nm stack.

In contrast, in PMOSFET's with oxynitride gate dielectrics formed by low-pressure rapid thermal chemical vapor deposition (RTCVD) with SiH_4, N_2O and NH_3 as the reactive gases, it has been reported that the hole mobility is degraded at all electric fields by increasing the nitrogen concentration [5]. Since increased nitrogen concentrations in oxynitride alloys leads to reduction of boron penetration [26] and higher dielectric constants, the mobility reduction in devices using these alloys identifies a trade-off in performance. The PMOSFET's of this paper with stacked N/O gate dielectrics and nitrided interfaces displays advantages of increased nitrogen concentrations leading to improvements in boron penetration resistance and dielectric constant without any significant reductions in the hole channel mobilities.

The direct substitution of Si_3N_4 for SiO_2 would yield a higher effective dielectric constant than for stacked N/O dielectrics. However, it is not possible due to the increased intrinsic defect density at Si-Si_3N_4 interfaces relative to Si-SiO_2. As shown in Fig. 9 when a nitride layer is substituted for the N/O stacked with the monolayer nitrided interface, the nitride I_d-V_g curve is shifted in the negative voltage direction by approximately 1 V and the drive current is degraded by about two orders of magnitude. The soft turn on of this device indicates a high density of interface traps, and the threshold voltage shift indicates a large amount of fixed charge, of the order of $10^{13}/\text{cm}^2$. Other aspects of device performance are discussed in detail in Misra *et al.* [27]. On the other hand, Fig. 9 also shows that, when $\sim$0.6 nm of oxide is inserted between the Si substrate and nitride layer, the drive current is improved significantly and is comparable to that of devices with an oxide dielectric. For example, PMOSFET's with N/O and oxide dielectrics with $T_{\text{ox-eq}} \sim 1.9$ nm show comparable drive current demonstrating the importance of the buffer oxide layer. If the thickness of the buffer oxide layer can be further reduced into the 0.3 nm range, this would lead to further reductions of the oxide equivalent oxide thickness.

Differences in the behavior of interface defects at monolayer nitrided Si-SiO_2 interfaces and Si-Si_3N_4 interfaces have been discussed in the context of constraints imposed by bonding coordination differences between SiO_2 and Si_3N_4. For example in bulk glasses and thin films, it has been shown that low defect densities in SiO_2 bulk result from an average bonding per atom of 2.7 [28]. This is sufficiently low to match the number of bonding constraints per atom to the degrees of freedom to form low-defect density films [28], [29]. A value of average bonding per atom $\sim$3 marks a criteria between device quality and highly defective thin films [28]. The bonding coordination of 3.43 in Si_3N_4 is too high and significant hydrogen incorporation is required to reduce bulk defect densities. A model has been developed for extending constraint theory to interfaces between crystalline Si and gate dielectric materials, which also shows that an average bonding per atom of $\sim$3 also marks a demarcation be-

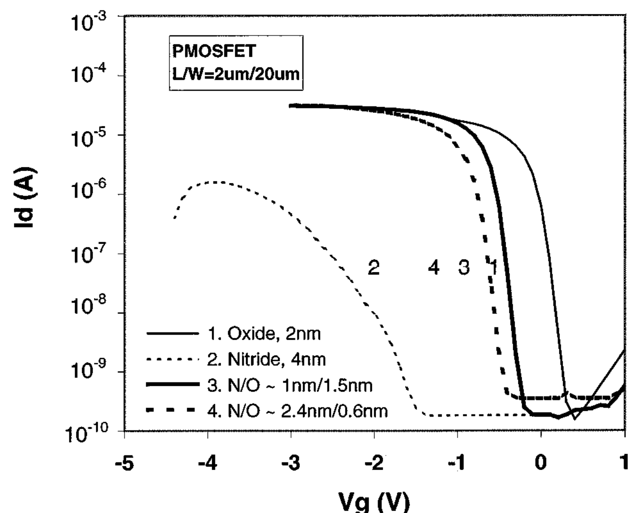


Fig. 9. I_d–V_g characteristics for oxide, N/O dual layer, and nitride devices with $T_{ox} \sim 2.0$ nm, indicating the effects of different effects of nitride and oxide interface regions.

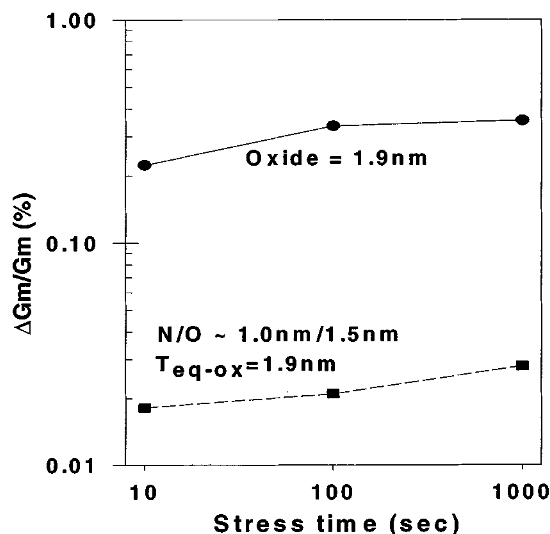


Fig. 10. Hot carrier stressing for PMOSFET's with N/O and oxide dielectrics. The device with the N/O dielectric displays increased immunity to hot hole stressing. (V_g-V_{th} = −1.7 V, V_d = −5 V).

tween low defect density and highly defective interfaces [30]. This model provides an explanation for the behavior shown in Fig. 9; in particular it demonstates that insertion of an oxide layer ~0.6-nm thick is sufficient to reduce the average number of bonds per atom at the interface from ~3.5 for a Si-Si_3N_4 interface to ~3 for the Si-SiO_2-Si_3N_4 interface of the aggressively scaled device of Fig. 9.

Fig. 10 shows the peak-transconductance degradation under channel hot-carrier injection for PMOSFET's devices with $L_{\text{eff}} = 0.5$ μm, and with 1.9-nm thick N/O dual layer dielectrics and oxide dielectrics. The devices were stressed at the peak substrate current for worst case degradation, with a high drain bias at −5 V. Compared with the control oxide, the PMOSFET with the N/O dielectric shows less transconductance degradation during hot carrier injection, implying a more robust silicon/dielectric interface. This improved interface immunity against hot carrier stressing is believed to be due to the interfacial strain relaxation by the nitrogen incorporation at oxide/substrate interface during the post-deposition annealing. Although the channel hot-carrier generation is localized primarily at the drain edge, the improvement of device reliability due to nitrogen incorporation is significant.

As oxide thickness is reduced sub-2.0 nm region, the rapid increase of direct tunneling current becomes a major obstacle for the device scaling. Fig. 11 shows the comparison of tunneling current through 100 μm × 100 μm capacitors with a 1.9 nm oxide and with N/O ~1.0 nm/1.5 nm and 2.4 nm/0.6 nm that correspond to approximately the same oxide equivalent thickness. The gate current for N/O devices is about an order of magnitude lower at a bias voltage of 1 V. In addition, because the physical thickness of N/O films is greater than that of oxide with the same $T_{\text{ox-eq}}$, the equivalent breakdown electrical field is increased from ~13.5 MV/cm for oxide to ~16 MV/cm for N/O ~1.0 nm/1.5 nm. Since the physical thicknesses of the two devices with N/O stacked dielectrics are significantly different, 2.5 for the 1.0 nm/1.5 nm dielectric and 3.0 nm for the 2.4 nm/0.6 nm, it is not obvious why the tunneling current has

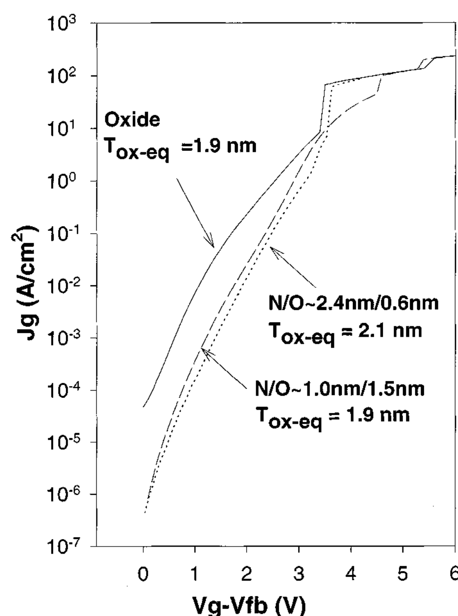


Fig. 11. I_g-V_g curves for capacitors with N/O and oxide dielectrics in the $T_{\text{ox-eq}} \sim 2.0$ nm range. The tunneling current for devices with N/O dielectrics is reduced with respect to the device with the oxide dielectric.

not decreased significantly with the N/O thickness ratio and associated increased physical thickness. Model tunneling calculations anticipate decreases in tunneling current for fixed $T_{\text{ox-eq}}$ with an increasing N/O thickness ratio [31]. Experiments with homogeneous oxide dielectrics with monolayer nitrided interfaces suggests that the reductions in tunneling current shown in Fig. 11 may result primarily from interface nitridation and not from increases in combined physical thickness [23]. If this were indeed the case, this would place a serious limitation of aggressive scaling limits using N/O gate dielectrics. In addition, as suggested by the data in Fig. 8, increasing the N/O ratio can also lead to reductions in the hole channel mobility, so that more research is clearly needed.

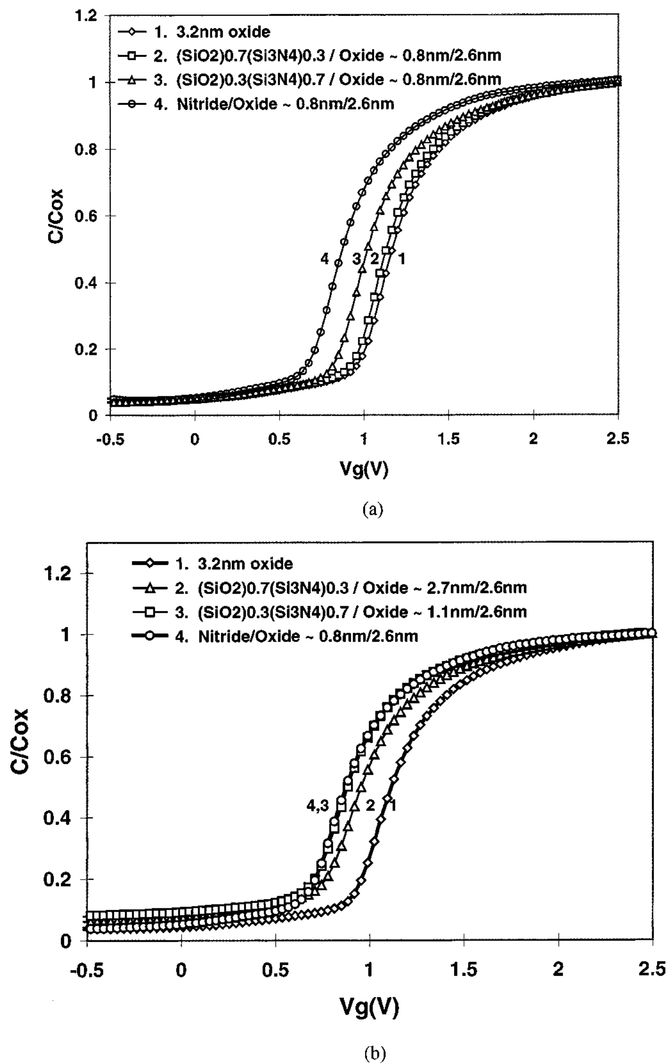


Fig. 12. Effectiveness of $(SiO_2)_x(Si_3N_4)_{1-x}$ alloy diffusion barriers in (a) dielectrics in which the barrier layer thickness is fixed at ~0.8 nm and the oxide fraction increased, and (b) in which the areal density of nitrogen atoms is fixed, and the barrier layer is increased proportionally.

C. Boron Diffusion in $(SiO_2)_x(Si_3N_4)_{1-x}$ Alloys

The 0.8-nm top nitride has been demonstrated to be able to stop boron penetration even with a thermal budget as high as 1000 °C for 4 min [7]. However, as shown in Fig. 2, boron penetration is observed when the top nitride thickness is reduced to 0.4 nm. It is difficult to explain the strong thickness dependence on the boron transport through the nitride layer by the conventional diffusion theory. A percolation model has been developed to account for boron transport in nitride and silicon oxynitride films [32]. The model is supported by the experimental results of Fig. 12. Boron penetration to the Si-SiO_2 interface has been studied by changes in flatband voltage for two different types of oxynitride deposited onto a 2.5 nm oxide. The $(SiO_2)_x(Si_3N_4)_{1-x}$ alloys were formed by an RPECVD technique described in [16]. The SiO_2 fraction, x, in the $(SiO_2)_x(Si_3N_4)_{1-x}$ alloys were 0, 0.3, 0.7, and 1. In the first set of experiments, the thickness of the oxynitride alloy is fixed at ~0.8 nm and the nitrogen concentration was reduced by alloying; i.e., by increasing x. In the second set of experiments. The areal density of nitrogen atoms is fixed at $\sim 4.5 \times 10^{15}$ cm^{-2} (as in a 0.8 Si_3N_4 film) and film oxynitride thickness is increased as the oxide fraction is increased. Fig. 12(a) shows the effectiveness of boron diffusion barrier formed by 0.8 nm $(SiO_2)_x(Si_3N_4)_{1-x}$, with the series of alloys with increasing SiO_2 fraction nitrogen. The extent of boron penetration can be compared by studying the flatband voltage shift from the theoretical value determined solely by the work function difference between gate and substrate. In Fig. 12(a), the 0.8 nm top nitride device shows no flatband voltage shift, which implies no boron penetration through this 0.8 nm nitride film, confirming the results shown in Figs. 2 and 3. By reducing the nitrogen areal density by substituting $(SiO_2)_x(Si_3N_4)_{1-x}$ alloys for the nitride layer, the flatband voltage is shifted to more positive voltages indicating increased boron penetration. Similar results apply for the second set of experiments in which the nitrogen areal density is fixed by increasing the thickness of the $(SiO_2)_x(Si_3N_4)_{1-x}$ alloy films. The reduced penetration of boron through the this second set of films supports a model in which boron transport proceeds through a percolation process involving the connectivity of the oxygen atom pathways through the oxynitride alloys. This model is qualitatively different from the model for boron transport through oxides as proposed by Fair [26], and will be discussed in more detail in a later publication [32].

IV. Conclusions

N/O dual layer gate dielectrics prepared by a combined RPECVD/oxidation process with equivalent oxide thickness of 1.9 nm have been fabricated for p^+-poly PMOSFET's. Post-deposition annealing drives nitrogen into the interface and results in a low defect density and robust interface against hot carrier stressing. The top nitride layer effectively suppresses boron penetration into the oxide and channel region, thereby eliminating threshold voltage shifts, short channel effects, while improving the gate dielectric reliability. While nitrided oxides show degraded mobility behavior for all fields, the N/O films of this paper display a comparable effective mobility with thermal oxides down to sub-2.0 nm thickness region. Along with the reduced tunneling current, these N/O dual layer gate dielectrics show excellent promise for the sub-0.25 μm dual-gate CMOS technology. The N/O interface engineering of this paper can provide a bridge to the future high-k/oxide dielectrics for the 1.0 nm $T_{\text{ox-eq}}$ CMOS technology. This paper has also addressed two other issues relevant to the performance of PMOSFET's with stacked N/O gate dielectrics with mono-layer scale interface nitridation: 1) the effectiveness of ultrathin interfacial oxide layers in reducing defect concentrations below those of Si-Si_3N_4 interfaces, and 2) mechanistic aspects of boron transport in oxynitride alloys.

References

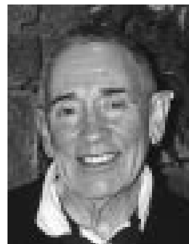
[1] G. Hu and R. Bruce, "Design tradeoffs between surface and buried-channel FETs," *IEEE Trans. Electron Devices*, vol. ED-32, p. 584, 1985.
[2] S. Wolf, *Silicon Procession for the VLSI Era*. Sunset Beach, CA: Lattice, 1995, vol. 3, p. 311.
[3] J. Pfiester and F. Baker, "Physical model for boron penetration through thin gate oxides from p^+ polysilicon gates," *IEEE Electron Device Lett.*, vol. 11, p. 247, 1990.

[4] T. Mogami, L. Johansson, I. Sakai, and M. Fukuma, "Hot-carrier effects in surface-channel PMOSFET with BF2- or boron-implanted gates," in *IEDM Tech. Dig.*, 1991, p. 533.
[5] E. Vogel, P. McLarty, and J. Wortman, "Mobility behavior of n-channel and p-channel MOSFET's with oxynitride gate dielectrics formed by LP rapid thermal chemical vapor deposition," *IEEE Trans. Electron Devices*, vol. 43, p. 753, 1996.
[6] D. Wristers, L. Han, and D. Kwong, "Degradation of oxynitride gate dielectric reliability due to boron diffusion," *Appl. Phys. Lett.*, vol. 68, p. 2094, 1996.
[7] Y. Wu and G. Lucovsky, "Improvement of gate dielectric reliability for p^+ poly MOS devices using remote PECVD top nitride deposition on thin gate oxides," in *IEEE Int. Reliability Physics Symp.*, 1998, p. 70.
[8] S. Lo, D. Buchanan, Y. Taur, and W. Wang, "Quantum-mechanical modeling of electron tunneling current from inversion layer of ultra-thin-oxide nMOSFET's," *IEEE Electron Device Lett.*, vol. 18, p. 209, 1997.
[9] G. Alers, D. Werder, and Y. Chabal, "Intermixing at the tantalum oxide/silicon interface in gate dielectric structures," *Appl. Phys. Lett.*, vol. 73, p. 1517, 1998.
[10] K. Hubbard and D. Schlom, "Thermodynamic stability of binary oxides in contact with silicon," *J. Mater. Res.*, vol. 11, p. 2757, 1996.
[11] S. Campbell *et al.*, "MOSFET transistors fabricated with high permittivity TiO_2 dielectrics," *IEEE Trans. Electron Devices*, vol. 44, p. 104, Jan. 1997.
[12] S. Sze, *Physics of Semiconductor Devices*, 2nd ed, New York: Wiley, 1981, p. 852.
[13] Y. Ma, T. Yasuda, and G. Lucovsky, "Ultrathin device quality oxide-nitride-oxide heterostructure formed by remote plasma enhanced chemical vapor deposition," *Appl. Phys. Lett.*, vol. 64, p. 2226, 1994.
[14] Y. Wu and G. Lucovsky, "Ultrathin nitride/oxide (N/O) gate dielectrics for p^+- polyslicon gated PMOSFET's prepared by a combined remote plasma enhanced CVD/thermal oxidation process," *IEEE Electron Device Lett.*, vol. 19, p. 367, 1998.
[15] Y. Wu, Y. Lee, and G. Lucovsky, "1.6 nm oxide equivalent gate dielectrics usng nitride/oxide composites prepared by RPECVD process," *IEEE Electron Device Lett.*, vol. 21, p. 116, Mar. 2000.
[16] S. V. Hattangady, H. Niimi, and G. Lucovsky, "Integrated processing of silicon oxynitride films by combined plasma and rapid thermal processing," *J. Vac. Sci. Technol. A*, vol. 14, p. 3017, 1996.
[17] C. C. Chang, "General formalism for quantitative Auger analysis," *Surf. Sci.*, vol. 48, p. 9, 1975.
[18] Z. Lu *et al.*, "Fourier transform infrared study of rapid thermal annealing of a0Si:N:H(D) films prepared by remote plasma-enhanced chemical vapor deposition," *J. Vac. Sci. Technol. A*, vol. 13, p. 607, 1995.
[19] S. Lo, D. Buchanan, Y. Taur, L. Han, and E. Wu, "Modeling and characterization of n^+ and p^+-polysilicon-gated ultra thin oxides (21–26 A)," in *Proc. Symp. VLSI Technology*, 1997, p. 149.
[20] M. L. Green *et al.*, "Rapid thermal oxidation of silicon in N_2O between 800 and 1200°C: Incorporated nitrogen and interfacial roughness," *Appl. Phys. Lett.*, vol. 65, p. 848, 1994.
[21] L. Han *et al.*, "Highly suppressed boron penetration in NO-nitrided SiO_2 for p^+-polysilicon gated MOS device application," *IEEE Electron Device Lett.*, vol. 16, p. 319, 1995.
[22] B. Maiti *et al.*, "High performance 20 A NO oxynitride for gate dielectric in deep sub-quarter micron CMOS technology," in *IEDM Tech. Dig.*, 1997, p. 651.
[23] H. Niimi, H. Yang, and G. Lucovsky, "A new low thermal budget approach to interface nitridation for ultra-thin silicon dioxide gate dielectrics by combined plasma-assisted and rapid thermal processing," in *Proc. Int. Conf. Characterization and Metrology for ULSI Technology*, 1998.
[24] D. Lee, C. Parker, J. Hauser, and G. Lucovsky, "Reliability of nitrided Si-SiO2 interfaces formed by a new, low-temperature, remote-plasma process," *J. Vac. Sci. Technol. B*, vol. 13, p. 1788, 1995.
[25] D. Lee and G. Lucovsky, "Nitrogen-atom incorporation at Si-SiO2 interfaces by a low-temperature (300-degree-C), pre-deposition, remote-plasma oxidation using N_2O," *J. Vac. Sci. Technol. A*, vol. 13, p. 1671, 1995.
[26] R. Fair, "Modeling boron diffusion in ultra-thin nitrided oxide p^+ Si gate technology," *IEEE Electron Device Lett.*, vol. 18, p. 244, 1997.
[27] Z. Misra *et al.*, "Interfacial properties of ultra-thin pure silicon nitride formed by remote plasma enhanced CVD," *IEEE Trans. Electron Devices*.
[28] G. Lucovsky and J. Philips, "Minimization of dangling bond defects in hydrogenated silicon nitride dielectrics for thin film transistors (TFT's)," *J. Non-Cryst. Solids*, vol. 227, p. 1221, 1998.
[29] G. Lucovsky *et al.*, "Bonding constraint-induced defect formation at Si-dielectric interfaces," in *Proc. IEEE Semiconductor Interface Specialist Conf.*, San Diego, 1998.
[30] ——, "Bonding constraint-induced defect formation at Si-dielectric interface and internal interfaces in dual-layer gate dielectrics," *Appl. Phys. Lett.*.
[31] H. Yang, H. Niimi, and G. Lucovsky, "Tunneling currents through ultrathin oxide/nitride dual layer gate dielectrics for advanced microelectronic devices," *J. Vac. Sci. Technol. B.*, vol. 17, p. 1806, 1999.
[32] Y. Wu *et al.*, "Microscopic model for boron-atom penetration through silicon dioxide and suppression of boron transport through silicon nitride," in *Proc. Conf. Physics and Chemistry of Semiconductor Interfaces*, San Diego, CA, 1999.

Yider Wu (S'96–M'99) received the B.S. degree in physics from National Tsing Hua University, Taiwan, R.O.C., in 1990, and the M.S. degree in applied physics from University of Massachuestts, Lowell, in 1994. He received the Ph.D. degree in electrical and computer engineering from North Carolina State University (NCSU), Raleigh, in 1999, with a dissertation on remote PECVD ultrathin nitride/oxide dual layer gate dielectrics. His Ph.D. research involved nitride/oxide gate dielectrics formation, interface nitridation, ultrathin oxide reliability and breakdown mechanism, dopant diffusion in dielectrics, quantum mechanical modeling, and remote PECVD techniques.

From 1995 to 1999, he was a Research Assistant in the Advanced Electronic Materials Processing Center, NCSU. After a summer internship in the Strategic Technology Group at Advanced Micro Devices, Sunnyvale, CA, where he studied time dependent dielectric wearout of ultrathin gate dielectric, he returned to Advanced Micro Devices in July 1999 as a Permanent Member. He is currently engaged in the process integration of next-generation flash memory technology within the Nonvolatile Memory Technology Directorate.

Dr. Wu is a member of the Electrochemical Society.



Gerald Lucovsky (M'99) received the B.S. and M.A. degrees in physics from the University of Rochester, Rochester, NY, in 1956, and 1958, respectively, and the Ph.D. degree in physics from Temple University, Philadelphia, PA, in 1960.

From 1958 to 1965, he was with Philco Corporation, Blue Bell, PA, and from 1965 to 1980, with Xerox Corporation at the research centers in Webster, NY, and in Palo Alto, CA (PARC), where he was a Senior Research Fellow and Manager of the General Sciences Laboratory. In 1980, he joined the Department of Physics, North Carolina State University (NCSU), Raleigh, as a University Professor of Physics. He is also a member of the Departments of Materials Science and Engineering and Electrical and Computer Engineering. His research activities at NCSU span a broad range from basic studies of electronic materials to the application of plasma processing in the fabrication of electronic devices. The focus of his present research is on alternative gate dielectrics for aggressively-scaled CMOS devices. Materials being researched include Si nitride and oxynitride alloys, and high-k oxides and silicate alloys.

Yi-Mu Lee was born in Kaohsiung, Taiwan, R.O.C., 1970. He received the B.S. degree in chemical engineering from National Cheng Kung University, Taiwan, in 1993, and M.S. degree from University of Missouri, Columbia, in 1998, respectively. He is currently pursuing the Ph.D. degree in electrical engineering at North Carolina State University, Raleigh.

His research interests include the RPECVD thin film technology, advanced gate dielectric, MOS transistor, and associated processing.