ABSTRACT

Bhate Kaustubh, Ramesh. Design and Fabrication of a MEMS Pressure Sensor and Developing a Release Protocol for MEMS (Under the guidance of Dr. Paul Franzon and Dr. Christine Grant)

This presents the design and fabrication of a MEMS Pressure Sensor for application in the Textile Industry. The transducer element in the sensor is a piezoresistive device. The Pressure Sensor layout is made in Cadence-Virtuoso and a 3-D Model is simulated in MEMCAD. Calculated and simulated results are compared. Processing steps are carried out in the NCSU Cleanroom to fabricate the device. A part of this thesis also attempts to develop a Release Protocol for MEMS devices made in the SUMMIT process. SUMMIT chips are released by wet etching in HF followed by rinsing in Methanol. The released device is then observed under Optical Microscope for results. Cantilever beams are also designed in SUMMIT process to be tested electrically when they come back after being fabricated at Sandia National Laboratories.

Design and Fabrication of a MEMS Pressure Sensor and Developing a Release Protocol for MEMS.

by
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Biography

Kaustubh Bhate was born in Thane, India in 1979. He graduated from the Government College of Engineering, Pune, University of Pune with a Bachelor's Degree in Instrumentation and Control in 2000. He worked as a Trainee Engineer at Tata-Honeywell, Pune between June 2000-July 2000, before joining the Master's Program of Electrical Engineering at North Carolina State University in August 2000. He worked on his MS thesis under the guidance of Dr. Paul Franzon and Dr. Christine Grant from May 2001 to August 2002.

Acknowledgements

I am grateful to my advisors Dr. Paul Franzon and Dr. Christine Grant for the opportunity to work in the field of MEMS, which is a fast growing area and for guiding my research through the course of my Master's Program. Many thanks to my thesis committee member Dr. Griff Bilbro for his encouragement and reviewing my thesis. I would like to thank Dr. Jacqueline Krim for her support during the course of the project. I would also like to thank all my colleagues at Riddick Laboratories as well as at EGRC for making them wonderful places to work in.

Lastly my deepest regards and thanks to my father and mother.

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Chapter 1

Introduction

1.1 Introduction to Micromachined Devices

The acronym MEMS stands for "*Microelectromechanical Systems*". These systems consist of microfabricated sensors, actuators and other structures that have become increasingly popular in many areas of science and engineering. The field of MEMS has evolved because of the fact that silicon and other semiconductors can be used to fabricate not only integrated electronic circuits, but also transducers and other devices by the use of similar lithographic and other microfabrication techniques. These techniques that are used to carry out fabrication of MEMS devices are referred to as "*micromachining*".

Numerous Micromachined Sensors have been developed so far and this has been possible mainly because of the fact that silicon possesses remarkable mechanical properties. These sensors have a wide range of applications: pressure measurement, optical interconnects in VLSI technology, microfluidic systems, inertial sensing and RF devices. A market study by System Planning Corporation (SPC (1999)) indicates that Pressure Sensors dominate over other MEMS applications [1].

This thesis aims at designing, simulating and fabricating a MEMS Pressure sensor to be used in the Textile Industry. The sensor has been designed for the specific application of measurement of tension in a thread that is being woven around a yarn.

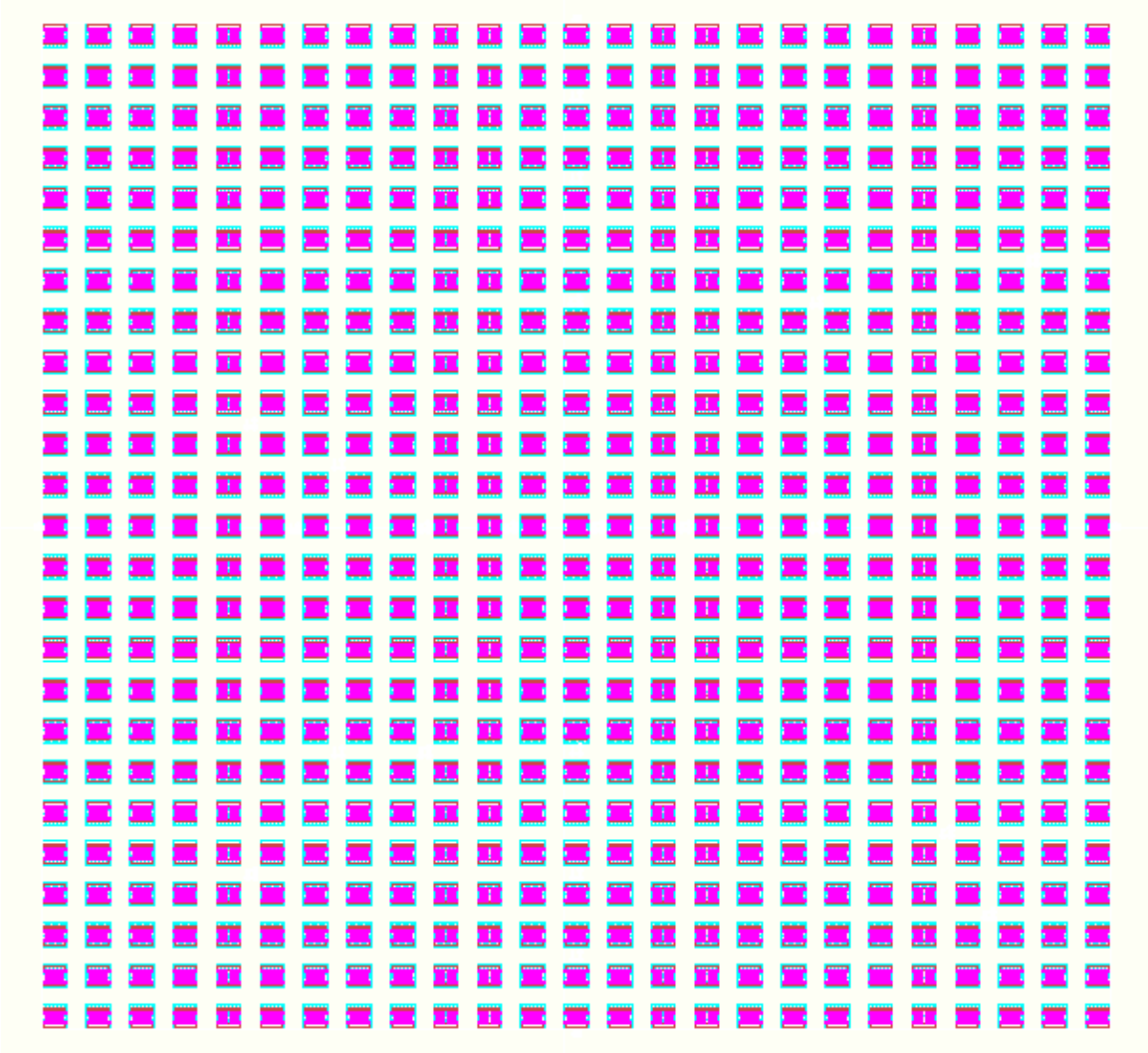
The transducing element in the sensor is a piezoresistive device fabricated on a silicon diaphragm that senses pressure in terms of change in resistance. The sensor will be placed beneath the thread and the tension/stress in the thread will exert a pressure on the piezoresistive element. This pressure displaces the diaphragm and this in turn causes a

stress in the piezoresistive element changing the value of its original resistance. If the sensor is calibrated then, the stress in the thread can be measured in terms of change of resistance of the piezoresistive element.

The main contribution of this thesis is in the design, simulation and in-house fabrication of the pressure sensor. For static simulation of the device, MEMCAD tool from Microcosm has been used. The design for the pressure sensor starts with a 2D layout in Cadence-Virtuoso, followed by a 3D model in MEMCAD. The tool MEMMech within MEMCAD is used to carry out simulations of the effect of various values of diaphragm thicknesses on the piezoresistive element. This analysis gives an idea of how the actual device will behave after fabrication.

After performing the above simulations, the layout of the sensor array is sent out for making hard masks to be used in fabrication of the device. These masks have been used in the various lithographic steps carried out in the fabrication of the sensors. Pre-thinned 4-inch wafers of (100), p-type silicon have been used for the fabrication of the pressure sensor. These wafers are 100um and 200um thick and polished on both sides. The wafers are bulk etched from one side to create a diaphragm type structure and the piezoresistive element is fabricated on the other side of wafer. The wafers have a 25X25 array of the pressure sensor. Fig 1.1 shows the array of structures on the wafers.

The last section of the thesis Chapter 6 highlights the conclusions and the future work that can be done in this area. It highlights various issues faced during the fabrication of the pressure sensor and recommends ways to address these issues.



1.1: Layout of the 25 X 25 array of the pressure sensor.

1.2 Issues in MEMS

Microelectromechanical Systems (MEMS) is an emerging, cutting-edge technology that relies on the microfabrication of small-scale mechanical components like actuators, sensors and mirrors and the integration of these components with on-board electronic processing.

Currently, three fabrication techniques are used to design MEMS structures viz. Surface micromachining, Bulk micromachining and the LIGA process. In surface micromachining, structures are built on top of the silicon wafer using thin films deposited through various standard methods similar to IC fabrication. Bulk micromachining involves etching away selected portions of the substrate to produce overhanging movable structures on top of silicon wafer. Some of the standardized processes that cater to the fabrication needs of all MEMS devices are MUMPS and SUMMIT. Multi-User MEMS Process (MUMPS) renders cost effective surface micromachining fabrication and is provided by MCNC (Microelectronics Center of North Carolina) in RTP, North Carolina. It is a three-layer polysilicon surface micromachining process involving polysilicon, metal and PSG sacrificial layers. The SUMMIT (Sandia's Ultra-planar Multi-level MEMS Technology) process is provided by Sandia National Laboratories. This is a five-layer surface micromachining process. The LIGA (Lithographic, Galvanoformung, Abformung) is a micromachining process that makes plastic and metal parts with high accuracy.

A well-known problem in the fabrication of MEMS devices from surface micromachining is stiction, which occurs when surface adhesion forces are higher than the mechanical restoring force of the microstructure. When a device is removed from the aqueous solution after wet etching of an underlying sacrificial layer, the liquid meniscus formed on hydrophilic surfaces pulls the microstructure towards the substrate and stiction occurs. A more difficult problem is in-use stiction that occurs during operation when microstructures come into contact.

One attractive approach to tackle the stiction problem is to provide low-energy surface coating in the form of an organic passivation layer on the inorganic surface. Another approach to eliminate in-use stiction is the formation of siloxane self assembled monolayers (SAMs) on the oxide terminated surface.

This thesis aims at developing a release protocol that will release MEMS devices made in the SUMMIT process. These devices can then be coated with low energy surface coatings

or self assembled monolayers to eliminate stiction. The main contribution of this thesis has been the use of wet etching techniques for the release of complex MEMS structures made in the SUMMIT process, as so far SUMMIT devices have been released using supercritical CO_2. This release process can be standardized to release other MEMS devices made in the SUMMIT process.

As a continuing part of this research work, cantilever beams have been designed in the SUMMIT process and sent to Sandia National Laboratories for fabrication. These beams have varying length, width and mass and can be used to detect the presence of stiction during release. These structures can also be used to deposit low-energy surface coatings or self assembled monolayers (SAMs) to study and characterize stiction.

The last section of the thesis Chapter 6 highlights the conclusions and the future work that can be done in this area. It highlights various issues faced during the release of MEMS devices and recommends ways to address these issues.

Chapter 2

Background and Literature Survey

In this chapter, a brief review of the existing work and literature in the filed of Pressure sensors is presented.

Pressure sensors represent a fairly mature and commercially viable area for micromachined mechanical sensors. There is an enormous range of applications for sensing pressure in liquids and gases. Examples include automotive manifold air pressure systems, aerospace systems, medical and many other. Micromachining technology has been able to make large inroads into this area due to improved performance, reduced size and reduced cost.

2.1 Pressure Sensor Designs

Most pressure sensor today use sealed gas or vacuum filled cavities. The basic operation of such a sensor is to couple the pressure to be measured to one surface of a membrane and to measure its deflection. To measure the displacement, any suitable sensing technique can be used, including strain gauges, capacitance, piezoelectric, optical and any other.

The Fig. 2.1 [2] shows the different type of pressure sensor designs commonly implemented in micromachined form. Pressure sensors can be built to measure pressure relative to a sealed reference cavity or differentially using two input ports. For sealed cavity designs a vacuum is preferred since there will be no temperature dependent pressure changes in the reference pressure.

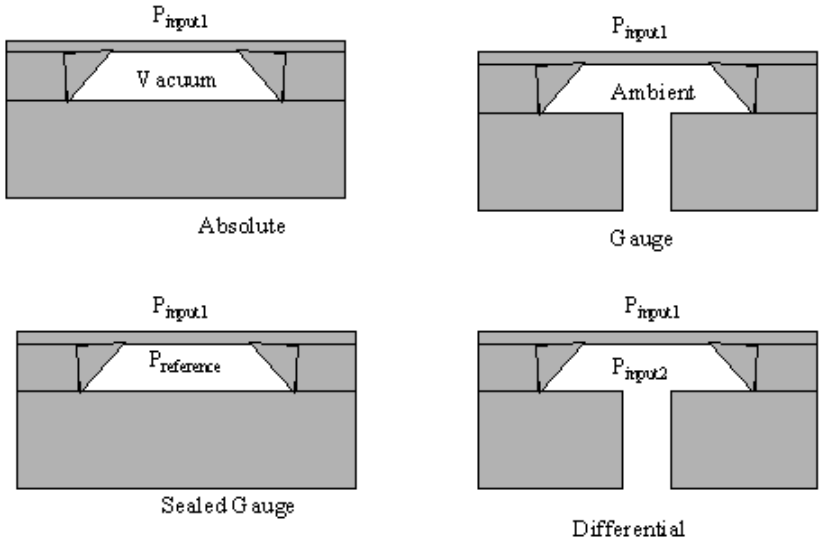


Fig 2.1 Pressure sensor designs [1]

For a circular clamped membrane, the deflection of the center can be related to pressure by

$$\frac{P*r^4}{E*h^4} = \frac{16}{3(1-v^2)}\left[\frac{y}{h}\right] + \frac{7-v}{3(1-v)}\left[\frac{y}{h}\right]^3 \qquad \text{……..(2.1)}$$

where,

P = applied pressure, in Pa

R = diaphragm radius, in m

E = young's modulus, in Pa

h = diaphragm thickness, in m

v = Poisson's ratio

y = deflection at the diaphragm's center, in m.

For small signal operation (y<h/2), the linear term of the above equation approximates the behavior of the diaphragm.

2.2 Capacitive Pressure Sensors

Capacitive sensing mechanisms can readily be employed to realize pressure sensors, despite the fact that this mechanism is inherently non-linear (because capacitance is inversely proportional to gap width).

Since the membranes employed are typically clamped at all edges, the capacitance of such membrane structures is not given simply by the parallel-plate capacitor equation, but it can be used as a crude starting point,

$$C = \frac{\in_0 * A}{D} \qquad \text{…….(2.2)}$$

which gives a $\triangle C$ in terms of change in gap width, δd, of,

$$\triangle C = - \frac{\in_0 * A * \delta d}{d^2} \qquad \text{……...(2.3)}$$

An interesting example of a micromachined capacitive pressure sensor is an acutely implantable blood pressure sensor developed at the University of Michigan [3]. They fabricated pressure transducer membranes using boron-selective EDP etching of structures that were anodically bonded to a glass substrate pre-etched to form cavities for lead attachment and metallized to form the lower capacitor plate and interconnections to a separate CMOS processor chip.

As shown in the Fig 2.2, the membrane formation process was carried out by pre-etching depressions into a silicon wafer, oxidizing and patterning the oxide, and performing a deep boron diffusion to define the membrane frame. This was followed by a shallower boron diffusion to form the membrane and the deposition of a silicon dioxide/silicon

nitride electrical insulating layer on the surface of the diaphragm. The silicon wafer was anodically bonded to a metallized glass wafer containing the opposite capacitor plates,

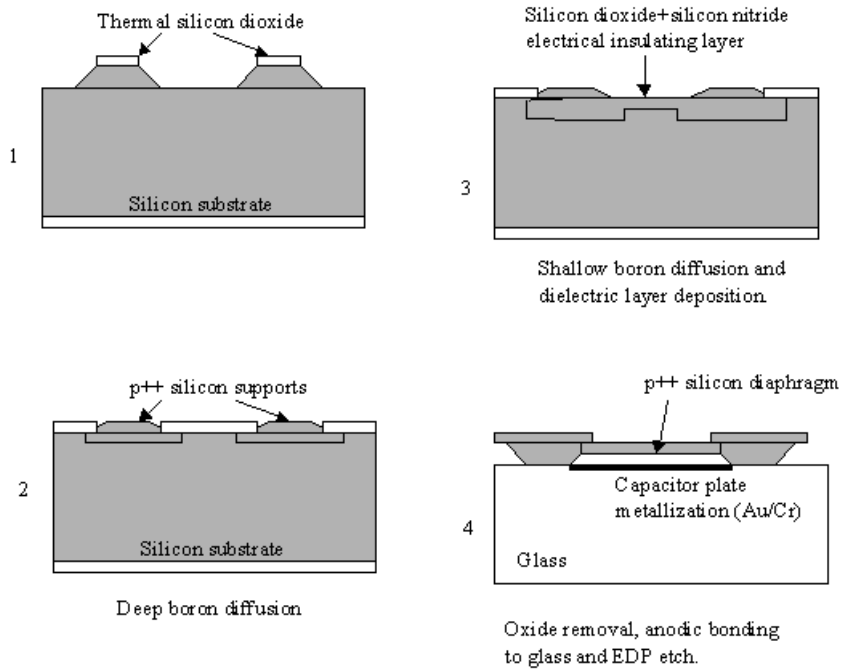


Fig 2.2 Capacitive membrane pressure sensor [3]

bond pads and etched grooves to accept interconnect wires. The silicon wafer was then etched away in EDP, leaving behind the membranes.

2.3 Resonant Pressure Sensor

Resonating structures make use of the fact that measurement of frequency is one of the most robust and high precision methods available, and also that their resonant frequency is generally not a function of the imperfections of electronics.

Petersen, et al (1991), [4], fabricated a very high precision resonant beam pressure sensor using silicon fusion bonding. Shallow pits were etched into n-type substrates, and p-type deflection electrodes were diffused in and above the pits, followed by fusion bonding of a second wafer above the first. The top wafer was then grounded and polished down to

6um thickness. A passivation layer was then formed on the top wafer and the sensing piezoresistors were formed using ion implantation, after which contact holes for metallization to connect to the diffused deflection electrodes were etched. Bond pads and interconnect metallization were then deposited and patterned, followed by etching of the diaphragm from the back of the wafer. Finally, two slots were etched next to the beam to release it over the buried cavity.

The beam was resonated by applying signals as small as a few millivolts between the beam and the deflection electrode and providing feedback from the piezoresistors in the beam. Pressure applied to the underlying wafer's diaphragm increases the tension on the resonating beam, increasing its resonant frequency.

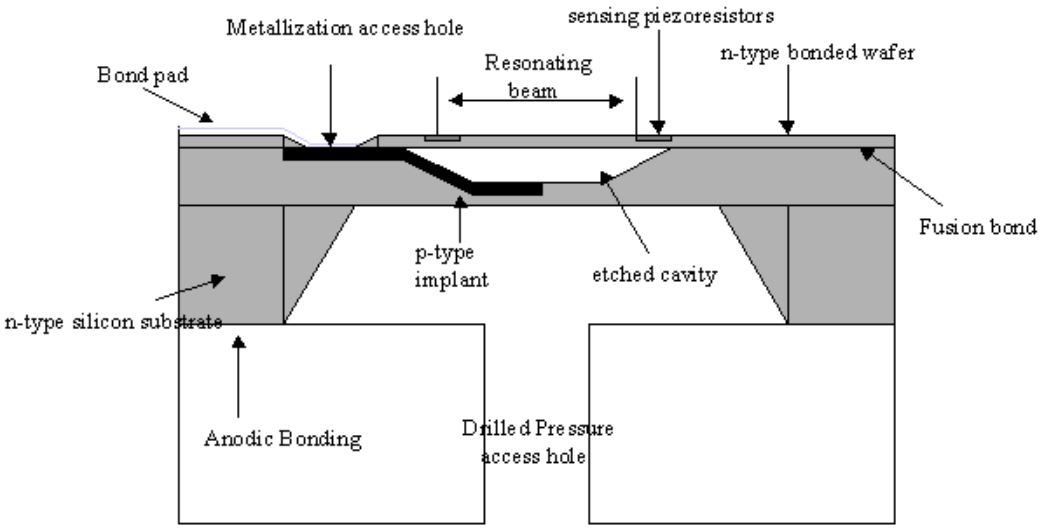


Fig 2.3 Cross-section of the resonant pressure sensor [4]

2.4 Planar Surface Micromachined Pressure Sensor

Planar, surface micromachined pressure sensors have been fabricated by Eaton and Smith [22], at the Sandia National Laboratories, by an extension of chemical-mechanical

polishing (CMP) process. CMP eliminates many of the fabrication problems associated with photolithography, dry etch, and metallization of nonplanar devices and adds design flexibility.

The fabrication process is shown in Fig. 2.4. In the first step, two separate trenches are etched into the silicon substrate (Fig. 2.4a). The first trench is shallow (0.3um) while the second trench is deeper (2 um). The shallow trench serves as a narrow etch port, which can be easily sealed at a later point in the process. Once the trenches are etched a silicon nitride liner is deposited (0.3um). The trenches are then filled with CVD oxides (Fig. 2.4b). The borophosphosilicate glass is used to shorten the release etch times. For polysilicon diaphragms, 2.4 um oxide film is used. Then, the wafers are polished using a colloidal fumed silica slurry and a polyurethane pad (Fig. 2.3c). Then diaphragm material (low stress silicon nitride or fine-grained polysilicon) is deposited and patterned for etch ports. (Fig. 2.4d). The release etch is than performed and the wafers are rinsed, dried and sealed. (Fig. 2.4e). The diaphragms are sealed by a 0.3μm low stress nitride deposition. Since deposition is done in LPCVD system, near vacuum persists in the cavity after sealing and serves as a reference pressure. Processing continues with the deposition and ion implantation of polysilicon piezoresistors. After implant polysilicon is patterned followed by aluminum deposition and pattern (Fig. 2.4f), and the device is ready to be tested.

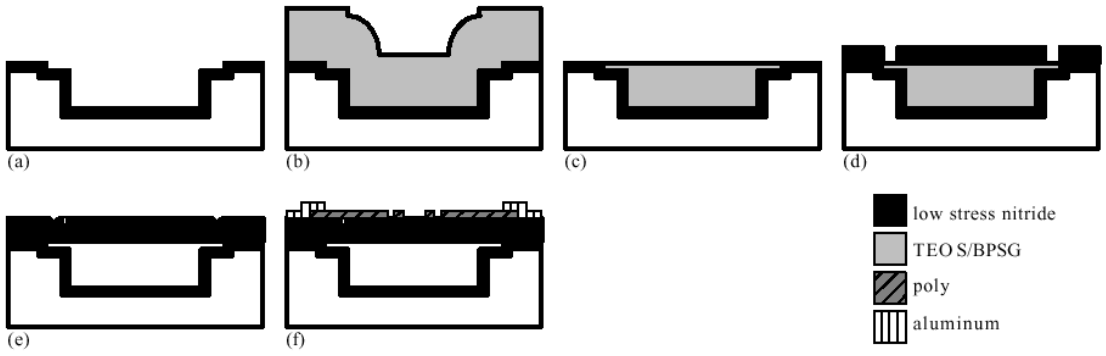


Fig 2.4 Schematic Fabrication process for nitride diaphragm sensor [22]

2.5 Piezoresistive Pressure Sensors

Silicon has the property of piezoresistance, a change in resistance with stress (or strain). An indirect way to sense pressure is to measure the bending strain in a diaphragm. Silicon is a material that is ideally suited for this type of a device and hence micromachined piezoresistive pressure sensors are very popular. Also these devices offer advantages such as accuracies of the order of 1%, minimum temperature dependence and linear operating range and hence they are widely used.

Chapter 3

Piezoresistive Pressure Sensor for the Textile Industry.

As suggested in the introduction this thesis aims at developing a MEMS pressure sensor for the specific application in the Textile industry. The choice of the piezoresistive transducer element is purely guided by the specific application needs. The sensor needs to withstand the pressure that it will measure and at the same time provide an accurate value of the pressure. Also the pressure sensor needed to be fabricated in-house thus limiting the different processing steps that could be performed in the device fabrication.

3.1 Application of the Pressure Sensor

The textile industry needs a sensor to detect the tension that a thread is undergoing as it is being spun around a yarn in order to prevent it from breaking. This can be achieved by placing the piezoresistive pressure sensor beneath the thread such that the thread remains in contact with the sensor as it moves while being spun. The tension in the thread will exert a force onto the piezoresistive element of the sensor that will change the resistance of the element and after calibration the pressure can be measured in terms of change in resistance.

3.2 Piezoresistivity

Piezoresistivity is a widely used physical effect that has its name derived from the Greek word “piezen”, meaning to apply pressure [5]. It is a phenomenon by which an electrical resistance changes in response to mechanical stress.

Piezoresistivity arises from the deformation of the energy bands as a result of applied stress. In turn, the deformed bands affect the effective mass and mobility of electrons and holes, hence modifying resistivity.

3.2.1 Longitudinal and Transverse Piezoresistance

If a relatively long, relatively narrow resistor is defined in a planar structure then the primary current density and electric field are both along the long axis of the resistor. This axis need not coincide with the cubic crystal axes [6]. Therefore it is necessary to know how to transform the peizoresistive equations to an arbitrary coordinate system. The structures are typically designed so that one of the axes of principal in-plane stress is also along the resistor axis. This permits a simplification of the piezoresistive formulation to the form shown in equation 3.1.l

$$\delta R/R = \pi_p \sigma_p + \pi_t \sigma_t \qquad \text{.....(3.1)}$$

where R is the resistance of the resistor and the proportionality constants, π_p and π_t are called the parallel and perpendicular piezoresistive coefficients, respectively, and are related to the gauge factor by the Young’s modulus of the material.

The general expressions for π_p and π_t are given by:

$$\pi_p = \pi_{11} - 2 (\pi_{11} - \pi_{12} - \pi_{44}) (l_1^2 m_1^2 + l_1^2 n_1^2 + m_1^2 n_1^2) \qquad \text{.....(3.2)}$$

and

$$\pi_t = \pi_{12} + 2 (\pi_{11} - \pi_{12} - \pi_{44}) (l_1^2 l_2^2 + m_1^2 m_2^2 + n_1^2 n_2^2) \qquad \text{.....(3.3)}$$

where (l_1, m_1, n_1) and (l_2,m_2,n_2) are directional cosines between the longitudinal resistor direction (subscript 1) and the crystal axis, and between the transverse resistor direction (subscript 2) and the crystal axis. In many silicon micromachined devices, resistors are oriented along [110] directions in (100) wafers. The longitudinal cosines are ($1/\sqrt{2}$, $1/\sqrt{2}$,0) and the transverse direction cosines are ($-1/\sqrt{2}$, $1/\sqrt{2}$,0). This results in:

$$\pi_{p,110} = \tfrac{1}{2} (\pi_{11} + \pi_{12} + \pi_{44}) \quad \text{.....(3.4)}$$

and

$$\pi_{t,110} = \tfrac{1}{2} (\pi_{11} + \pi_{12} - \pi_{44}) \quad \text{.....(3.5)}$$

3.2.2 Piezoresistive Coefficients of Silicon

The piezoresistive coefficients are dependent on crystal orientation and can change significantly from one direction to another [6]. They also depend on dopant type (n-type vs. p-type) and concentration. These coefficients are a weak function of doping level for doping below about 10^{19} cm^{-3} but then decrease markedly for high doping. The coefficients decrease with increasing temperature, dropping to about 0.7 of their room temperature value at 150°C. The temperature dependence is nonlinear which aggravates the problem of compensating for temperature dependence. An important fact is that at higher doping levels, the temperature dependence of piezoresistive coefficients becomes small.

3.3 Resistor Orientation

The wafers used in the fabrication on the Pressure Sensor are (100), p-type. In order to make diffused resistors in these wafers, n-type (phosphorus) doping impurity is used to achieve junction isolation.

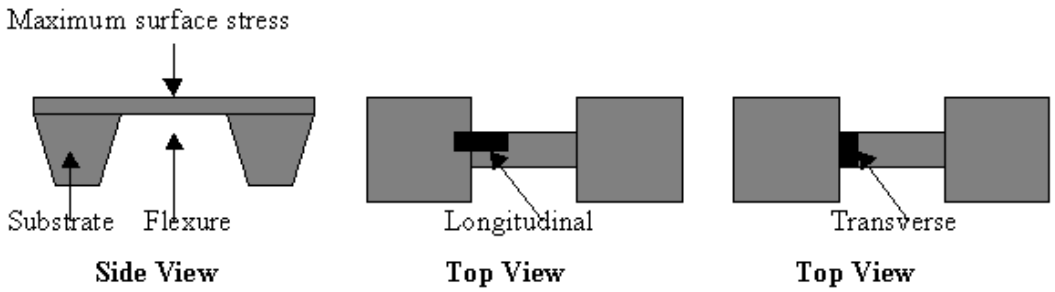


Fig 3.1 Lateral and transverse piezoresistor placements. [6]

When the actual size of the resistor is taken into account, the transverse resistor orientation has the potential for the largest response, because if it can be placed at exactly the right point, the entire resistor will experience the maximum bending stress [6]. However, this orientation is very susceptible to manufacturing variations that can arise from small lithographic alignment errors. The longitudinal resistor, on the other hand, must extend over some finite length along the cantilever and, for alignment reasons, may also extend onto the support. Therefore not every part of the resistor experiences the maximum stress, and some loss of sensitivity results. However, small misalignments or placement errors will have a less severe effect than for the transverse orientation. Hence to address these issues a resistor placement is used that is reasonably insensitive to alignment tolerances. The resistor is divided into two sections and spans over the entire area of the diaphragm for maximum sensitivity.

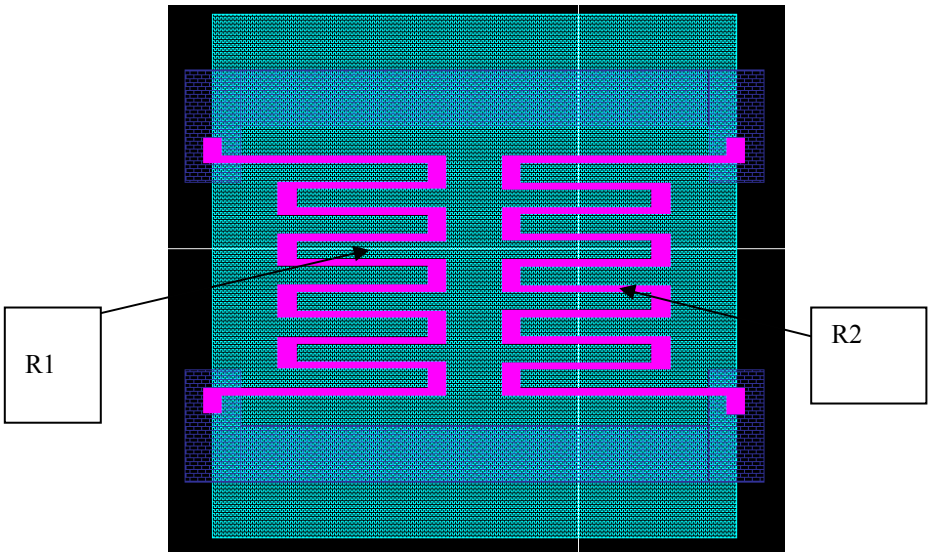


Fig 3.2 Layout of the sensor in Cadence-Virtuoso

The structure shown in the above figure is bulk micromachined and hence all resistor axes are along the <110> directions and are aligned along an axis of principal stress at the edge of the plate. Further, as these resistors are on a plate rather than a cantilever, each resistor experiences both a longitudinal stress and transverse stress. For example, if the resistor R1 experiences a longitudinal stress σ_l, then it must simultaneously experience a transverse stress $\nu\sigma_t$, where ν is the Poisson's ratio. Otherwise it would shrink in the transverse direction, which is not allowed in a plate. As a result, the total change in resistance for R1, assuming uniform stress over the entire resistor would be

$$\delta R_1/R_1 = (\pi_l + \nu\pi_l)\,\sigma_l \qquad \ldots\ldots\ldots\ldots (3.6)$$

The Poisson ratio happens to have a minimum in the [110] direction of a (100) plane, with a value of 0.064. Assuming resistor orientation along [110] direction, π_l for a n-type piezoresistor is $-31.2*10^{-11}$ Pa and equation 3.6 becomes

$$\delta R_1/R_1 = (-33.19*10^{-11})\,\sigma_l \qquad \ldots\ldots\ldots\ldots (3.7)$$

3.4 Modeling the Sensor

The diaphragm is modeled as a square plate under stress. An energy-method analysis [6] gives the load-deflection equation of the form

$$P = \left\{C_r[\sigma_0*H/L^2] + C_b[E*H^3/(1-\nu^2)*L^4]\right\} c_1 + C_s*f_s[E*H/(1-\nu)*L^4]c_1^3 \quad \ldots\ldots (3.8)$$

where C_r is the coefficient of the residual stress term, C_b is the coefficient of the plate bending term, and C_s is the coefficient of the large-amplitude-in-plane stretching term. For our analysis C_r is zero because the diaphragm is bulk micromachined. For small

amplitude loading C_s is ignored. The value of C_b from variational analysis is $\pi^4/6$. Thus the energy method solution has pressure-deflection relation

$$P = [\pi^4/6*(E* H^3)* c_1]/(1-\nu^2)*L^4 \qquad \text{……..(3.9)}$$

where L = edge length of the diaphragm, c_1 = displacement at the center of the diaphragm, E = Young's Modulus, H = the diaphragm thickness and ν = Poisson's ratio.

The magnitude of the x-directed surface stress at the middle of the diaphragm edge is

$$\sigma_x = E*H/ 2\rho_x \qquad \text{……(3.10)}$$

where the x-directed radius of curvature is given by

$$1/\rho_x = (2\pi/L)^2 \ *c_1/2 \qquad \text{……..(3.11)}$$

Thus σ_x can be expressed as

$$\sigma_x = 1/\pi^2(1-\nu^2)*(L/H)^2 * P \qquad \text{…….(3.12)}$$

and because we are dealing with a plate, the y-directed stress at the center of the edge is

$$\sigma_y = \nu\sigma_x \qquad \text{……(3.13)}$$

where ν= 0.06 for a [110] direction in a (100) plane.

Chapter 4

Design, Simulation and Fabrication of the Pressure sensor.

As mentioned in the introduction, this thesis aims at developing a pressure sensor that can be used in the Textile industry to measure the stress in the yarn while it is being woven. This chapter discusses the various issues faced during the different stages of the making of this sensor. This chapter will give an overview of the design of the pressure sensor, its simulation using the software tool MEMCAD and finally the various issues faced while attempting the fabrication of the pressure sensor.

4.1 Design of the MEMS Pressure Sensor

The first issue in the design of this pressure sensor was the choice of the transducer element in the sensor. The application required that sensor be placed beneath the thread and remain in constant contact with it. This required that the sensor design be robust as well as sensitive to the tension in the thread. Also the sensor needed to be fabricated in the EGRC cleanroom limiting the kind of process steps that could be incorporated in the fabrication process. The sensor area also needed to be fairly large so as to cover the entire diameter of the thread about 1mm. One option considered was a capacitive pressure sensor with an enclosed capsule to measure pressure relative to a sealed reference cavity, but the process complexity involved in its fabrication turned out to be a major drawback for the design. Hence after much deliberation, a piezoresistive element was chosen as the transducer element in the sensor.

4.1.1 Mask Layout

The current design for MEMS starts from drawing the mask layout of different layers involved in the fabrication process by using a layout editor. This procedure is the same as generating the layout of a VLSI circuit. Cadence Virtuoso layout editor was used for this purpose. The mask layout information was drawn by this layout editor. It saves the MEMS structures in CIF (Caltech Interchange format) or GDS-II format which is then sent over for fabrication. Since the sensor was going to be fabricated in-house no particular design rules were considered. The layout of the pressure sensor is shown in the Fig. 4.1 [7].

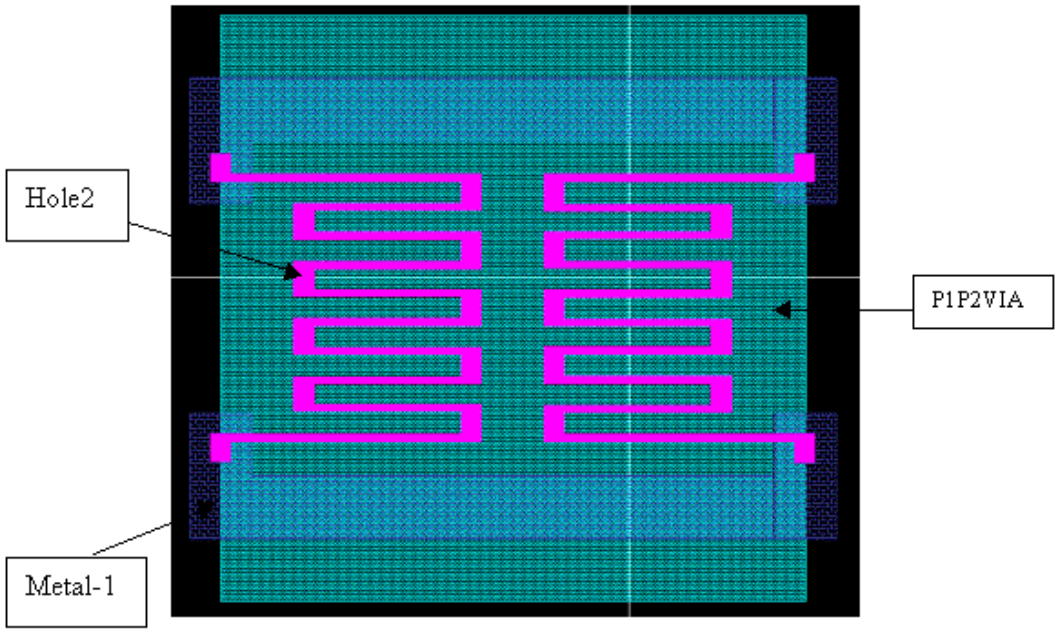


Fig 4.1 Masks of the sensor

The area of the complete layout is 1400um X 1400um. This large area of the layout is attributed to the fact that it should be able to extend beyond the entire diameter of the thread. The P1P2VIA mask is a backside mask. This mask will be used to bulk etch the wafer from the backside to create a diaphragm like structure. The actual area of the diaphragm after fabrication will be is 1145um X 1145 um. This area is less than the area

of the mask that was designed for it as can be seen from the Fig.4.2.

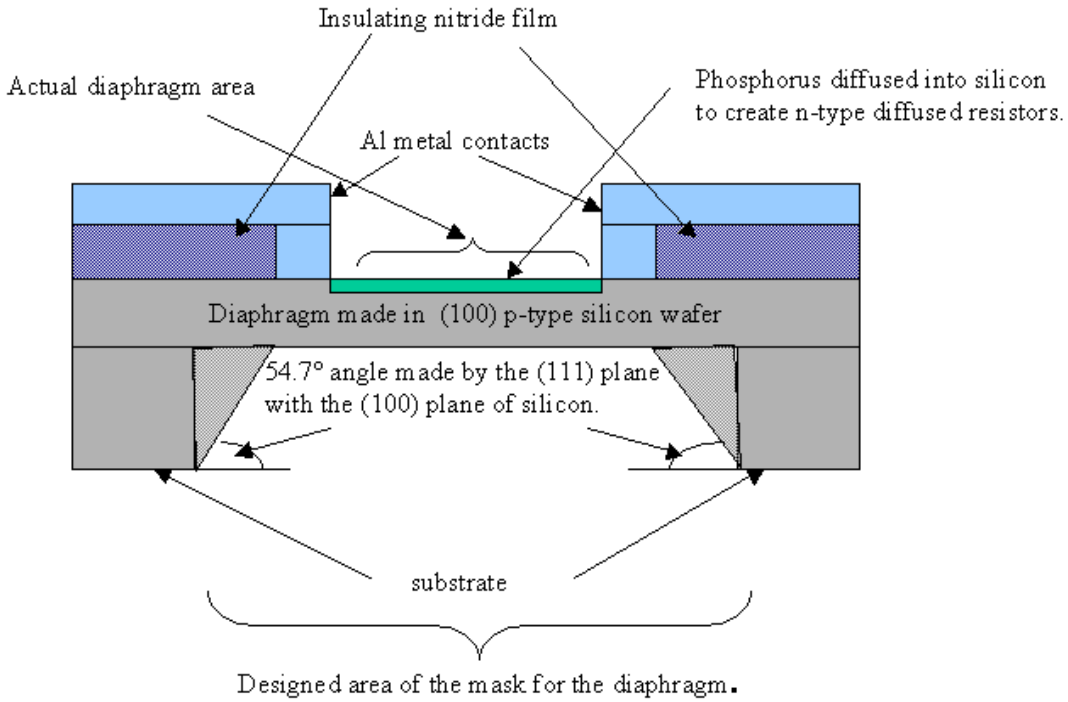


Fig 4.2 Cross-section of the pressure sensor.

This is because the (100) wafers that are being used for the fabrication process etch along the (111) plane that makes an angle of 54.7 degrees with (100) plane and hence the final diaphragm area is less than the designed mask area. The HOLE2 mask defines the shape of the piezoresistive element. This mask will be used to cut the nitride layer on the wafer to enable diffusion that will form diffused resistors in the silicon wafer above the diaphragm. The structure is defined such that it lies completely on the diaphragm for maximum sensitivity. When the diaphragm stretches due to pressure from the thread the resistance of the piezoresistive element comes under stress and it's resistance changes. The METAL mask defines the metal contact area to the piezoresistive element. The metal can also be used as a probing pad to probe the structure for measurements when the device is tested after fabrication. The proposed metal to be used in fabrication is Aluminium.

4.1.2 Alignment Marks

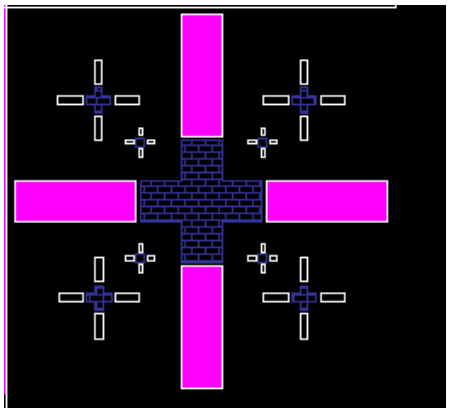


Fig 4.3 Alignment marks on the masks

The alignment marks shown in Fig 4.3 are designed to align the METAL1 layer to the HOLE2 layer during lithography. These alignment marks are placed on either side of the 25 X 25 array of sensors to minimize alignment errors.

4.2 Simulation of the Pressure Sensor

4.2.1 Process Definition

The process definition input to the MEMCAD tool from Microcosm is the information of the process steps that are involved in the MEMS fabrication process [8]. Differences among fabrication processes involve parameters such as the number and sequences of mask steps, materials used, material thickness and types of deposition and etch techniques. Four different types of techniques of deposition can be modeled by MEMCAD viz. conformal, planar, stacked and via. The conformal deposit confirms to the profile of the surface and flows over the uneven levels of the materials already present. Planar deposits fill in any uneven areas and result in a uniform deposition over the top of the surface. Stacked deposits are more rigid depositions that lay on top of any irregularities in the surface but, which do not fill in any of the areas. Via deposits are used as plugs to fill in any holes on the surface. Etching can be positive or negative

depending upon how the etch masks have been defined. Modeling the process steps by MEMCAD involves specifying a series of deposit and etch steps depending on the fabrication process. It describes the type of deposited film and it's thickness, the name of the mask from the layout editor used to etch off the layer and also the angle and offset which can be specified to take care of fabrication faults.

The nitride film deposited on the wafer is described as planar. The masks P1P2VIA and HOLE2 are described as having negative polarities as they are used to etch away the nitride layer on the frontside and the backside of the wafer respectively. The METAL1 mask is defined as positive as it indicates areas on the wafers where metal should remain.

4.2.2 Generation of 3D Model

From the 2D-mask layout information and the elevation information from the process definition, a 3D model of the MEMS structure is generated. The generated CIF file of the layout is first exported from Cadence Virtuoso and then imported by the layout editor Catapult in MEMCAD. MEMCAD uses a 3D-model generator from SDRC, "I-DEAS" to do it. The 3D model generator builds up the model in steps, by getting the height and depth information from the process file, at every deposit and etch step, along with the 2D geometry of the concerned mask layer from the CIF file. The 3D model generated by MEMCAD is shown in Fig 4.4.

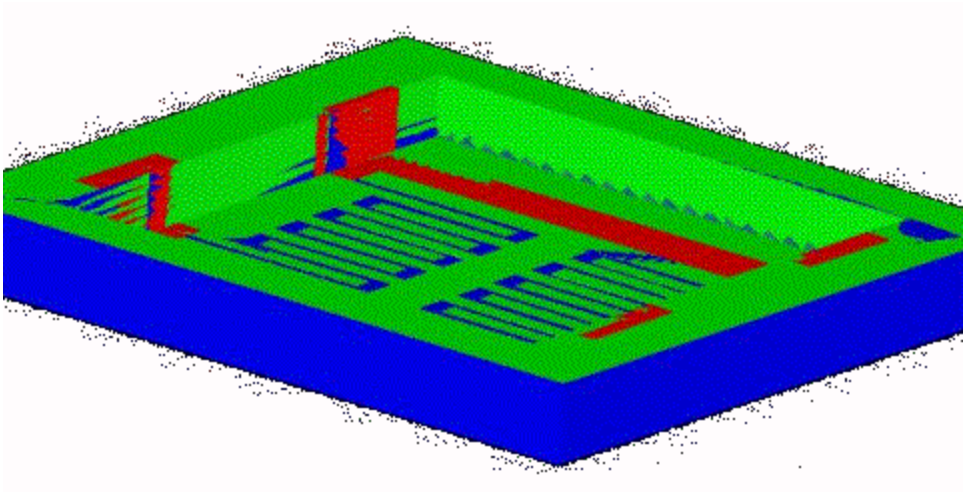


Fig 4.4 3-D Model in MEMCAD.

4.2.3 Meshing of the 3D model

Complicated geometries arise in various applications like thermodynamics, structural analysis, electromagnetics and acoustics. In each of these areas, a partial differentiation equation or a series of partial differential equations are needed to be solved on a geometric region. A method of choice here is finite element analysis, which has meshing as the first step of operation. Meshing or mesh generation involves breaking down the solid structure into small subparts, and the differential equations are solved on each subpart [8]. The meshes created have a tremendous impact on the solution of the numerical model; both with respect to accuracy and the extent of computational resources they demand. To get the best possible solution while still maintaining minimum computational leads, the following criterion should be met:

- Keep the number of nodes to a minimum to save computational resources.
- Have sufficient number of nodes especially on the corners where high gradients of the function solved are encountered, where the domain boundaries need to be specified in detail.

The final meshed structure for the Pressure Sensor is shown in Fig 4.5.

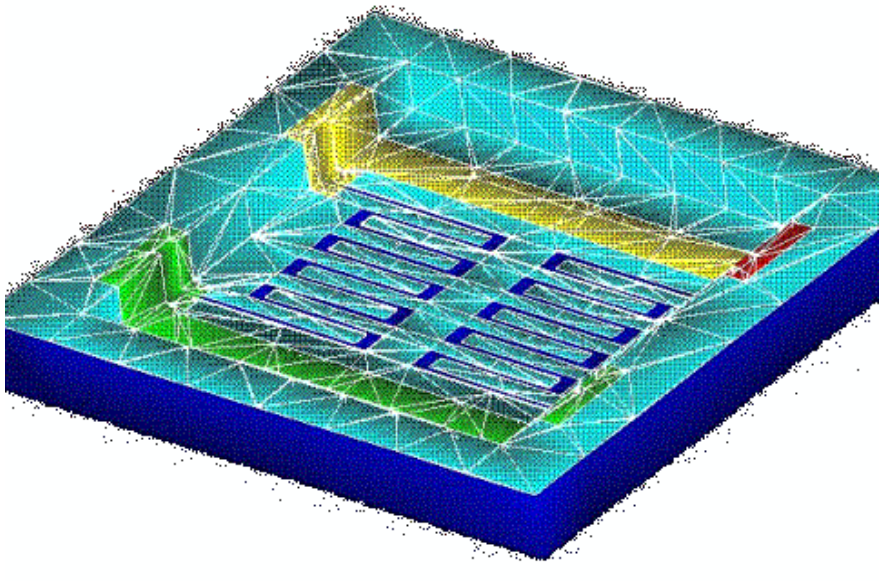


Fig 4.5 Meshed 3-D model in MEMCAD

4.3 Fabrication of the Pressure Sensor

The Fig. 4.6 shows a bird's eye view of the process flow for the pressure sensor.

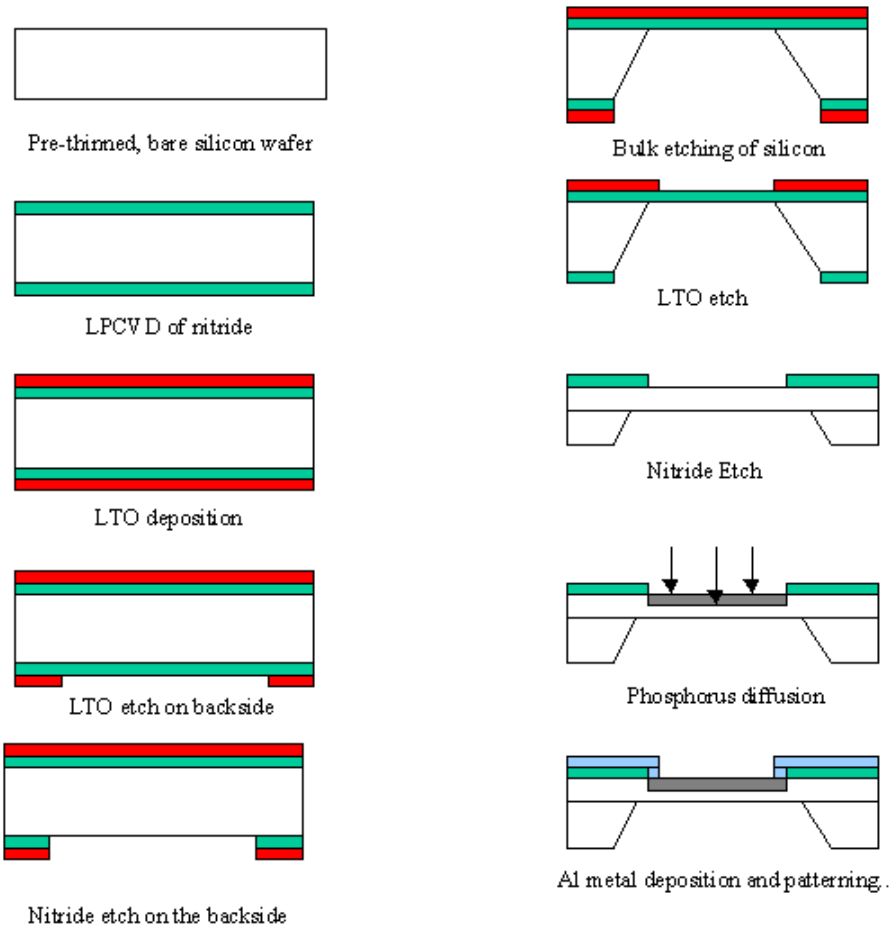


Fig 4.6 Process flow for the fabrication of the pressure sensor.

Before starting the actual fabrication process in the cleanroom a "Traveler" was created based on the above process flow. The "Traveler" is a document that lists sequentially all the different process that will be carried out in the fabrication of the sensor. It also

includes the documentation of the different process conditions for the various processing steps that will be carried out.

4.3.1 Choice of Pre-thinned wafers

Based on the design of the process flow for the sensor it is clear that the wafers, on which the device will be fabricated, will need to be bulk etched. There are two types of chemicals to do bulk etching of silicon viz. isotropic etchants and anisotropic etchants. Isotropic etchants like HNA (mixture of hydrofluoric acid, nitric acid and acetic acid) will etch silicon at the same rate in all the directions whereas anisotropic etchants like TMAH (tetramethyl ammonium hydroxide) and KOH (potassium hydroxide) etch silicon much faster in the (100) direction than in the (111) direction. Based on the geometry of the structure that is required to create the diaphragm it was decided to use an anisotropic etchant to do the bulk etch of silicon.

Potassium being a contaminant for CMOS processes, KOH cannot be used in the cleanroom to etch silicon and hence TMAH was the likely choice. Literature predicts that the most optimistic etch-rate of silicon by TMAH is 1um/min which means that in order to etch a regular 500+/-25 um thick wafer to create a diaphragm of 20μm, the etch time would be around 500 minutes (more than 8 hours of continuous etch). This is very difficult to achieve with a continuous uniform etch rate and hence it was decided that in order to reduce the etch time of silicon and maintain a uniformity in the etch rate, pre-thinned wafers would be used. These wafers are available in 100 μm and 200 μm thicknesses and would take a maximum of about 3 hours of bulk-etch time based on the literature data available.

4.3.2 Handling Pre-thinned wafers

These wafers being so thin are very difficult to handle especially when doing wet chemical processing. The wafers need to be picked up very gently and care should be taken that they do not break while loading or unloading them from the furnace boats or

wet etch boats. Both surfaces of these wafers are polished and it is not possible to write a name on these wafers using a scribe. These wafers cannot be dried using the regular spin dryer, as there is every possibility that they may break during this operation. Hence they need to be dried by a nitrogen gun (blow dryer) which also again needs to be done very carefully. Wet chemical processing is especially difficult because when picking up the wet wafers by a tweezer, the surface tension of the water between the wafer-tweezer contact causes the wafer to stick to the tweezer and it becomes extremely difficult to get the wafer off the tweezer without breaking it. The vacuum-operated holder also cannot be used to pick the wafers because the vacuum sucks the thin wafer at the contact, causing a pit to appear on the other side.

In order to make the wafers more robust in handling, during some of the processing steps, it was decided to bond a thin wafer to a normal substrate by means of glue. To serve this purpose, Crystalbond^{TM} 509 (glue) is used. It comes in the form of small candle-size sticks and is very easy to use [9].

The substrate wafer is placed on a hot plate and heated to about 110° C. The glue-stick is then moved along the edge of this wafer, causing the glue to melt on the surface of the wafer. The hot plate is then turned off and the wafer is allowed to cool to room temperature. The thin wafer is then placed on top of this substrate-wafer that has solidified glue on it. The thin wafer is aligned so that it is exactly on top of the substrate and then the hot plate is turned on again with the set point at 110° C. At this temperature the glue sandwiched between the two wafers melts again and serves to bond the two wafers together. This sandwiched assembly can then be used directly for processing in certain process steps like spinning photoresist (PR) and wet etching.

The wafers can be easily de-glued again by placing the assembly on hot plate and heating it to a temperature above 121° C, at which point the adhesive disintegrates and vaporizes and the two wafers come off easily. Any remaining residue on the wafers can be cleaned by putting the wafers in an Acetone bath. Acetone dissolves any residue of the adhesive

and cleans the wafers, which can then even be put in the furnace to do any other processing step.

4.3.3 Nitride deposition

A nitride film is deposited on the silicon wafers to act as an insulating layer. Silicon nitride is highly suitable for this purpose because it behaves as a nearly impervious barrier to diffusion [10]. The film is deposited by a method called Low Pressure Chemical Vapor Deposition (LPCVD). Since this process is carried out in very low pressures it is surface reaction limited and the transportation of chemicals is not important allowing the wafers to be stacked in the furnace. The method also provides a higher throughput if the temperatures are lowered. However as the temperature is lowered, the deposition rate can decrease significantly and the film quality may suffer.

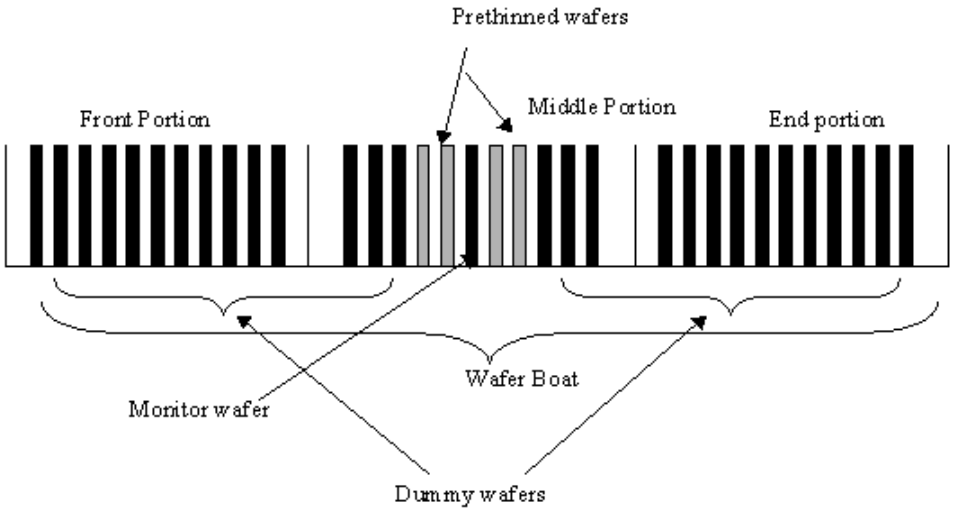


Fig 4.7 Arrangement of wafers for LPCVD runs [10]

The nitride film was deposited at temperatures of 800°C, 775°C, 775°C for the front, middle and the end portion of the furnace. The pressure during the deposition time was 300 mTorr. The wafers were put in the furnace with their major flats at the top. The pre-thinned wafers are polished on both sides so it is difficult to determine which face of the wafer was facing the gases flowing through the furnace and which face was in the

opposite directions. A monitor wafer is put in the furnace in the middle of the thin wafers so that the measurements (Table 2 and Table 3 in Appendix) of the monitor are an average indication of the film thickness on the first and the last pre-thinned wafer in the stack.

After the nitride film has been deposited, its' thickness is measured using Ellipsometry at different points on the wafer. From these results the average film thickness and the deposition rate of nitride is calculated.

This deposited nitride film will act as a mask to protect the rest of the silicon wafer when it's desired part is being bulk etched in TMAH. This film also serves as a mask to prevent the diffusion of phosphorus atoms into the silicon wafers in areas other than where the piezoresistors have been defined. A wafer with known nitride film thickness is put in TMAH solution at 90°C and a procedure identical to that used in bulk etching silicon is followed. The wafer is etched for 50 minutes and then the nitride film thickness is measured again (Table 1 in Appendix). It is found that the nitride film is almost untouched by the TMAH solution, thus proving that it is the right choice as a mask for the wafer.

4.3.4 LTO Deposition

When non-plasma silane deposition of oxygen is done at temperature less than 500°C, it is commonly referred to as Low-temperature oxide, or LTO deposition [10]. Because a nitride film has been deposited on the wafers and the fact that oxide can be grown thermally only at the silicon oxide interface, it is difficult to thermally grow oxide on these wafers. Hence oxide is deposited on top of the nitride film by LPCVD. The LTO film deposited is usually very porous and can also exhibit inadequate step coverage or filling. Because of it's porous nature the LTO film etches much faster in HF than thermally grown oxide.

The purpose of the LTO film here is to act as a mask to protect the nitride film from being etched away except from the area where the piezoresistors are fabricated. Nitride film is etched in a solution called the trans-N etch at 180°C. To calculate the desired LTO film thickness on nitride, the etch rate of trans-N on LTO is calculated. A dummy wafer with known LTO film thickness on it, is put in the etch solution for 8 minutes and then the film thickness is measured again using Ellipsometer. It is observed that the etch rate of trans-N on LTO is about 30A°/min at 180°C (Table 7 in Appendix). Similarly, the etch rate of trans-N on nitride is calculated and from the data now available the thickness of the LTO film to be deposited on nitride is obtained.

For LTO deposition the wafers are loaded with their major flats at the top. A bare silicon monitor wafer is also included in the stack of wafers because LTO thickness on nitride cannot be measured. The monitor wafer is placed in the middle of the thin wafers so that its thickness is the average thickness of LTO on the first and the last of the wafers. The slot numbers of the boat, in which the wafers are loaded, are also noted. The LTO deposition is carried out at about 410°C with pressure of 660 mTorr. The gas flow of the gases in the furnace is also noted.

After the deposition-run the LTO thickness is measured on the monitor wafer (Table4 and Table 5 in Appendix). The deposition rate and average thickness is also calculated. The values obtained from these calculations are used as benchmark to estimate the LTO thickness on the other wafers. From the readings obtained it is found that the LTO thickness is more near the wafer flat that was at the top and less at the bottom of the wafer. This is attributed to the fact that there is a better circulation of the furnace gasses at the top than at the bottom of the wafers leading to a faster reaction at the top and hence more LTO thickness. Also from the previous runs of the furnace it is observed that the film thickness is more on wafers at the front and decreases towards the wafers at the end.

4.3.5 Photolithography

After LTO depositions the wafers are taken for lithography. The photoresist Shipley1813 is spun on the wafers at 4000 rpm for 40 seconds. The Shipley1813 is a positive photoresist i.e. the photoresist will dissolve in the developer solution wherever it has been exposed. Before spinning the PR the wafers are coated with a primer that provides a better contact between the PR and the wafer.

After spinning PR on the wafers they are then exposed to UV light through the mask under consideration (P1P2VIA, HOLE2 and/or METAL1). The expose time is set to 8 seconds.

The wafers are then developed in the Developer solution by immersing them in its bath. The develop time varies from 1.5 to 2 minutes. The wafer-boat is continuously pulled out of the bath to see if the features are visible. Once the features can be seen, the wafers are developed for a few more seconds and then pulled out.

After developing the wafers, they are then hard baked for 1 minute. This hardens the resist and improves it's ability to act as an etch mask. The photoresist is then used as a mask to etch away the LTO in HF bath.

4.3.6 LTO Etch

LTO is etched away in a solution called "Buffered oxide etch" (BOE) which contains HF. Because LTO is porous and has a lesser density as compared to thermally grown oxide it's etch rate in HF is much faster (about 1800A°/min) than that of the latter. During the etch step a monitor wafer is also put in the BOE bath to help determine the endpoint of the etch.

The boat is continuously agitated up and down when put in the BOE solution to give a clear view of the monitor wafer. When all the oxide is etched away the BOE solution no

longer clings to the wafer and the wafer become “de-wet”. Once the monitor wafer become “de-wet”, an overetch is done for about 5 sec and the boat is then removed from the solution.

4.3.7 Strip Photoresist

The photoresist is removed by putting the wafers in a solution called Nanostrip. Nanostrip consists of sulfuric acid that dissolves the photoresist on the wafers. The wafers are kept in the “Nanostrip” bath for as long as all the photoresist is not removed. The end point is indicated by clear solution dripping from the wafers when pulled out of the bath rather than dark thick liquid containing photoresist. Sulfuric acid does not affect silicon wafers so the time for which the wafers are kept in the “Nanostrip” bath is not critical. In general it takes about ten minutes to completely strip the photoresist of the wafers.

4.3.8 Nitride Etch

Nitride is etched using a solution called “trans-N” that contains phosphoric acid. The reaction is carried out at 180°C. The LTO layer serves as a mask for the nitride etch. From the available data the etch rate of LTO by “trans-N” is about 30A°/min, while that for nitride varies with the number of wafers in the bath. It is 68A°/min with one wafer in the bath and drops to about 62A°/min with four wafers in the bath. This is attributed to the fact that the solution in-between the wafers does not have a continuos circulation and so after sometime the etch rate begins to fall which is ultimately evident in the form of a decrease in the overall etch rate over the period of time.

A monitor wafer is used during the etching of nitride on the wafers (Table 6 in Appendix). The measurements on the monitor wafer by Ellipsometer indicate whether all the nitride has been etched away. An overetch of about one minute is done to ensure that the nitride is completely etched away.

4.3.9 Bulk Etch of Silicon

Silicon is bulk etched using TMAH (tetramethyl ammonium hydroxide). The reaction is carrried out by heating the TMAH solution in a petridish, on a hot plate to about 91°C, and then putting one wafer into it [11].

TMAH is present in all cleanrooms since it is used in developing positive photoresists. A potential trade-off with use of TMAH is that the surface morphology tends to be rough.

An elaborate procedure has been developed to carry out this bulk etch step in order to achieve a uniform etch rate. A known quantity of TMAH is begun to heat. As the TMAH temperature rises it begins to evaporate and the quantity of the solution in the dish begins to change. To prevent this the dish is covered when being heated to minimize the evaporation. The temperature of the TMAH solution is indicated by using a thermocouple. The etch rate of silicon depends on the temperature as well as the volume of the TMAH in the dish and hence these two parameters need to be controlled as accurately as possible. To reduce the effects of TMAH evaporation the solution in the dish is replenished from time to time to keep the volume of the solution in the dish a constant. When the solution temperature reaches 91°C, a wafer is put in the dish to start the bulk etching.

Silicon begins to get etched where it is exposed. As more and more silicon is etched, the concentration of silicon in the TMAH solution and the rate of TMAH evaporation also increases, reducing the etch rate. To minimize these effect, the dish is kept covered throughout the etch period and the solution in the dish is replenished frequently.

Literature [11] predicts an etch rate of 1um/min for silicon by TMAH. However the initial obtained etch rate is much less than that. The measurements indicate that the etch rate is about 0.3μm/min. Also it is observed that for long etch time (more than 30 minutes), apart from replenishing the solution from time to time, if the whole solution is changed after a fixed interval of time (viz. every 30 minutes), the etch rate is much faster.

In order to get a better etch rate, the wafer is glued to another wafer that is coated with a thick (>2000A°) nitride film, which acts as an excellent mask to protect silicon from being etched. As a result of this, now only one face of the wafer is exposed to TMAH during the entire etch cycle. Using this method, an etch rate as high as 43 μm/hr was obtained, following the same procedure as before.

4.3.10 Diffusion

Phosphorus was diffused into the p-type wafers to create diffused resistors in the wafers. Phosphorus was chosen as the dopant, instead of Boron, because the wafers being p-type and phosphorus being a n-type impurity, there is an isolation between the two.

The wafers were diffused with Phosphorus using phosphorus-disks. The diffusion was carried out for 70 minutes at 950°C. This long time and high temperature is because of the fact that the resistance of the piezoresistor need to be reasonably small, below I KΩ. Phosphorus pentoxide is formed on the wafer surface (Table 8 in Appendix), from which the phosphorus then diffuses, into the wafer. The wafers are placed in the following order in the furnace: p-disk, wafer, wafer, p-disk. The wafer pair is placed back-to-back, to prevent the back-side doping of the wafers.

A bare silicon monitor wafer was also put in the furnace to measure the sheet resistance of the wafer after diffusion. Measurements indicate that the sheet resistance in 5.78Ω/□, while the oxide thickness measurements are indicated in Table 8 in the Appendix. Both the measurement results are in accordance with the calibration data sheet of the phosphorus-disks [12].

4.3.11 P-Deglaze

Following diffusion, the oxide formed on the wafers was etched by putting the wafers in a solution called P-deglaze, which is diluted BOE (buffered oxide etch) solution. The

ratio of BOE and water is 1:4. This diluted solution is used to etch the oxide because the P_2O_5 glass is easy to etch. The "de-wetting" of the monitor wafer was used as an end-point in determining the complete removal of the oxide. The recommended time is 30 seconds but the wafers were etched for 40 seconds to make sure that the oxide had been etched from all the wafers, completely.

4.3.12 Aluminum Deposition and Etching

Aluminum was deposited to make contact with the diffused resistors. The metal pads can be used to probe the structure when the fabrication is complete. The metal thickness is chosen to be 2000 A°.

After metal deposition, it was patterned using the METAL1 mask and then the wafers were etched to remove unwanted Aluminum. The aluminum etch is done in a solution composed of: phosphoric acid (80%), nitric acid (5%), $C_2H_4O_2$ (5%) and distilled water. The endpoint for aluminum etch is detected by a rapid change of color on the wafer. The shiny metal look on the wafer is completely taken off.

Chapter 5

Developing a Release Protocol for MEMS Devices

There have been many exciting predictions that the future of micromachines or MEMS is just “around the corner”, but this future has proven to be slow in coming. Despite the demonstration of numerous MEMS devices and product concepts (Analog Devices, ADXL-50, Capacitive Accelerometer) each year, a very small number have actually succeeded in the market. The most critical impediment to the fabrication and operation of many MEMS devices has been the difficulty in controlling surface forces during processing and operation.

Several interesting processes have been demonstrated that rely on “sacrificial” materials that are used as “forms” or “spacers” to make desired shapes and are latter removed. Phosphosilicate glass (PSG) etches much faster in HF than thermally grown or undoped oxides, making it an attractive sacrificial layer for undercutting polysilicon structures [1]. A large number of sacrificial processes have been demonstrated, using both dry and wet etching, and the technique can be readily extended to form multiple levels of interconnected, released structures.

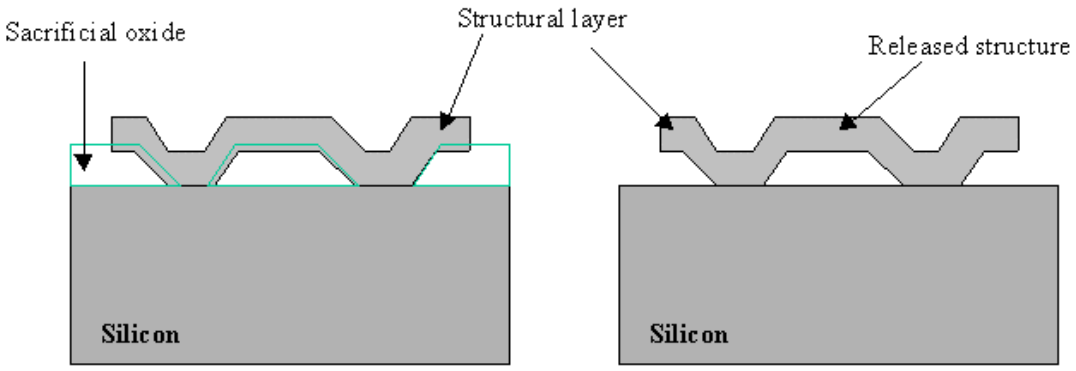


Fig. 5.1 Illustration of the use of sacrificial layer [1]

5.1 Sticking Problems during Wet Release

Attractive capillary forces can be a real problem with wet released microstructures because the drying fluid tends to pull deformable microstructures into contact with the substrate and/or each other. Once deflected, van der Waals forces are responsible for stiction of hydrophobic surfaces and hydrogen bonding is the dominant adhesion mechanism for hydrophilic surfaces [13]. Thus the total forces acting on a structure during release can be summed as

$$U_{total} = U_{bending} + U_{stretching} + U_{surface\ tension} \quad \text{.....(5.1)}$$

Hydrogen bonding can occur when there are hydrogen atoms bonded to nitrogen, oxygen or fluorine. This is a fairly common situation with compounds used in micromachining [13]. For example, hydrophilic silicon has a large number of surface –OH groups. The use of less polar solvents than water, such as methanol and ethanol greatly reduces this effect.

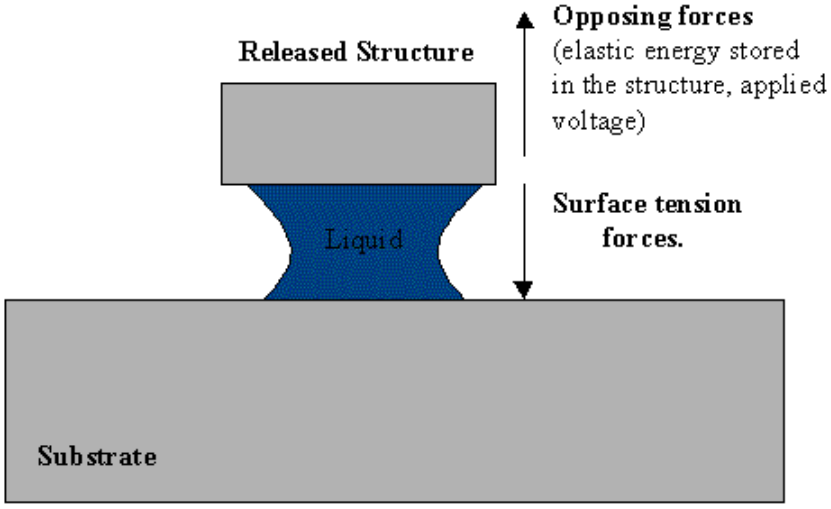


Fig. 5.2 Illustration of different forces during release [1]

5.1.1 Stiction

A well-known problem in the fabrication of MEMS devices from surface micromachining is stiction. Stiction occurs when surface adhesion forces are higher than the mechanical restoring force for the microstructure. When a device is removed from the aqueous solution after wet etching of an underlying sacrificial layer, the liquid meniscus formed on hydrophilic surface pulls the microstructure towards the substrate and stiction occurs.

5.2 Stiction Reduction during Release

A wide variety of stiction-minimizing process approaches have been developed for surface micromachining applications some of which are described in this section.

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5.2.1 Vapor-phase Sacrificial Layer Etch

Vapor-phase etching of sacrificial oxides can be accomplished using HF and methanol with negligible stiction problem and greatly simplified overall release procedure. By

etching the sacrificial silicon dioxide with hydrofluoric acid vapor instead of conventional aqueous HF solution, the need for subsequent rinsing and elaborate drying procedure is eliminated [14]. Condensation of water on the etch surfaces can prevent the success of HF vapor release but the use of anhydrous HF gas and methanol mixture under low pressures solves this problem.

Using this method etch rates of 10 to 15 μm/hr on silicon dioxide for partial pressures of 15 and 4.5 torr for HF and methanol, respectively, were obtained.

However the disadvantage of this method is that, etching in vapor phase is much slower than that in aqueous solution. The speed of etching is a concern when the width of the microstructures is large and when more layers of sacrificial oxide are involved.

5.2.2 Geometry/Process Specific Release Methods

A less general approach to reducing sticking following wet etch release is the use of methods specific to given geometries or processes. Abe, et al [15], studied the drying of post release singly and doubly clamped beams. For singly clamped cantilevers, they observed that for the shorter structures, drying occurred from tip uniformly back to the base, while for longer cantilevers, the fluid dried in the opposite direction, causing stiction problems. By adding small, narrower width protrusions, from the ends of the long cantilevers, sticking was considerably reduced.

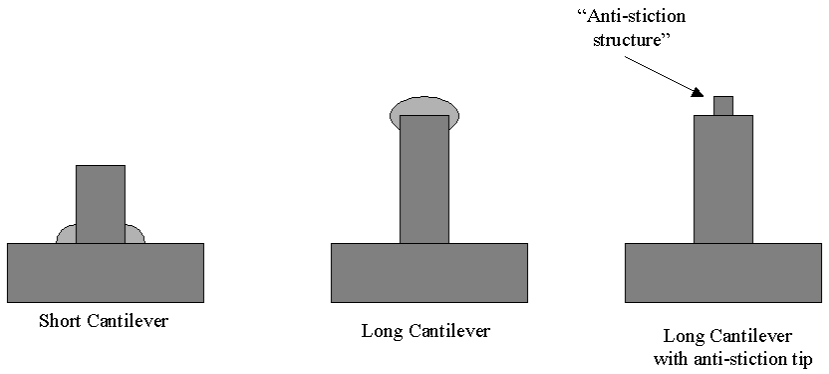

Fig 5.3 Anti-stiction structure improving release yield [15].

5.2.3 Supercritical Drying

The most common method of preventing stiction in MEMS devices during their release is supercritical drying.

Supercritical fluids are compounds heated and pressurized above their critical pressure and temperature, at which point liquid and vapor states become indistinguishable and become a fourth, supercritical state. Supercritical fluid has the attractive property of absence of surface tension due to the coexistence of liquid and vapor states [16].

The basic idea is to take advantage of the fact that, under the correct i.e. (supercritical) conditions, the liquid and vapor phases cease to exist as distinct states as indicated in Fig 5.4. When this occurs the interface between them is eliminated and, after transitioning directly to the gas phase, the gas can be gently vented without disturbing the structures.

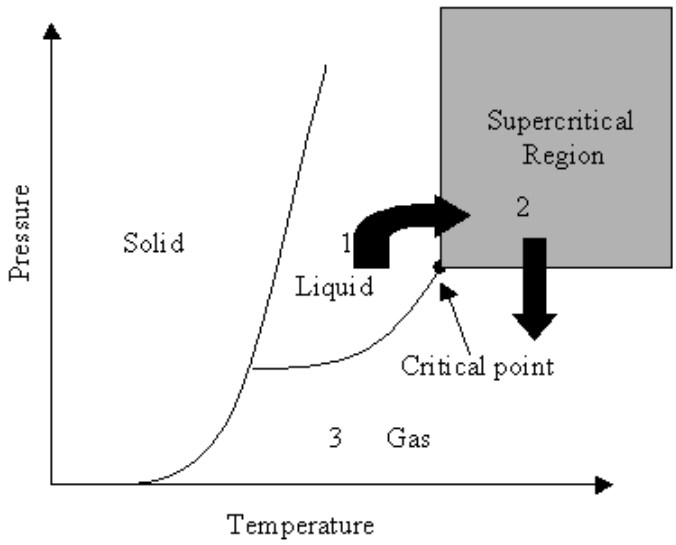

Fig 5.4 Phase relationships in critical point drying [1]

A possible choice for use in micromachining is water because it is used in rinsing. However the critical point for water is 228.5 bar and 374°C that would normally destroy the substrate. Another possible choice is methanol but this also has high critical point as well (240°C, 79.9 bar). A material with low critical pressure and temperature is carbon dioxide (31°C, 73.8 bar), but it is only a liquid at pressures greater than 900 psi. However methanol is completely miscible with liquid carbon dioxide and this provides a good method for using carbon dioxide as drying fluid. Liquid carbon dioxide is used to replace liquid methanol at room temperature and elevated pressure, and then the supercritical transition of carbon dioxide is used to dry the devices.

The Critical Point Drying method is expensive because it requires the use of Critical Point Dryers that have a very high cost. Their cost varies from 8000$ to 13,500$ [17] depending on the manufacturer and the different features available in a particular model. Also, these machines have to be used carefully with proper safety measures because of the high pressures involved.

5.3 Anti-Stiction Coatings

An alternative to Critical Point Drying method is to provide low-energy surface coating in the form of an organic passivation layer on the inorganic surface [18]. Such a coating can not only eliminate or reduce capillary forces and direct chemical bonding, but also reduce electrostatic forces. This occurs if the thin organic layer is directly applied to the semiconducting substrate, without the intervening oxide layer. Texas Instruments uses a fluorinated fatty acid self assembled monolayer (SAM) on the aluminum oxide surface in their DMD (Digital micro-mirror device), while Analog Devices coats the surfaces of their inertial sensors using thermal evaporation of silicone polymeric materials at the packaging stage after the device is completely released. Another much advocated approach is the formation of siloxane self –assembled monolayers (SAMs) on the oxide terminated surface, but the difficulty of this chemistry and the poor reproducibility puts significant limitations on it’s practical usage.

A part of this thesis aims at developing a release protocol for MEMS devices made in the SUMMIT^{TM} process which can then be treated with organic monolayers to eliminate release-related stiction. SUMMIT devices are normally released using the Supercritical CO_2 drying but this thesis attempts to show that they can be released using a wet etch step in HF followed by a rinse in methanol. The resulting devices are shown (Appendix C) to be released completely with the total removal of the sacrificial oxide layer. This protocol can be used for the release of any MEMS device made in the SUMMIT process. Once this part of the release process has been standardized, the surface-active agents selected for surface modification can be studied for their effect on release-related stiction.

5.4 Release of MEMS Devices Made in SUMMIT Process

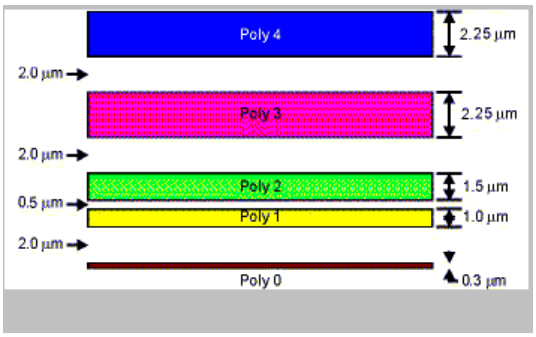

Fig. 5.5 Stack-up of layers in SUMMIT [19].

The Fig 5.5 shows the stack-up of the different layers involved in the SUMMIT process [19]. It can be seen that there are four layers of sacrificial oxide sandwiched between five layers of poylisilicon. Because of this nine layer stackup (as compared to the three polysilicon and two oxide layers resulting in a total of five layers involved in the MUMPS^{TM} process of Cronos, Inc,) the rate at which the sacrificial oxide can be etched away is slower as compared to that in the MUMPS process. In addition, more complex designs can be made in the SUMMIT process than in the MUMPS process, which can also affect the release rate of the sacrificial oxide. This is because structures with very reduced feature sizes or those which are made of more number of polysilicon layers, consequently involving more number of sacrificial oxide layers to be released. The

resulting reduction in the HF solution in contact with the oxide, requires longer release times.

5.4.1 Release Procedure

Literature [20] tells us that in order to release a MEMS device made in the MUMPS^{TM} process, it is etched in 49% HF for 2.5 minutes, before introducing the sample in DI water for rinsing.

In order to release a chip made in the SUMMIT process we have modified the above recommendation because of the difference in the two fabrication processes. The chip is first put in a 49% HF solution for fifteen minutes. Small fragments are seen being released from the chip, while it is in HF. This is attributed to the fact that HF attacks the oxide present on the chip causing it to dissolve. In addition to this, as HF etches the sacrificial oxide layer, micro-bubbles are observed on the chip surface, indicating a reaction. Following this step, the chip is rinsed with methanol in three steps, each time immersing the chip in fresh methanol solution for ten minutes. The chip has to be handled carefully when moving from one solution to another, in order to avoid mechanical damage to the chip. Also, the transfer from one solution to another should be aimed at minimizing the exposure of the chip to atmosphere. The sample is then placed on a hot plate at 115°C for approximately 20 minutes. The resulting sample is then taken for observation under an optical microscope to study the results of the reaction.

5.4.2 Observations

The above procedure was carried out in the NCSU cleanroom and initial runs were conducted by a trial and error method with the time of HF etch being varied incrementally in fixed steps of two minutes, starting with a time of five minutes of HF etch. It was observed under the optical microscope that for times less than fifteen minutes, the sacrificial oxide is not completely etched away. The regions of oxide that are

deep inside the chip take a longer time to be etched away and the oxide if present, can be seen under the optical microscope.

In general, after MEMS devices are released, a few of the structures can be seen to be floating on the chip (Appendix C). These are structures that have been completely freed because of an overetch of the underlying sacrificial oxide layer. This was used as a guideline while observing the released chips under the optical microscope, to determine whether the chip was being released.

DI water, instead of methanol, was also initially used to rinse the chips after the HF etch, but the results were not satisfactory. The DI water leaves behind a stain/residue on the chip that can be seen under the optical microscope (Appendix C). As a result, it is difficult to tell whether the chip has been released completely under the stain because looking for oxide on the chip becomes difficult.

5.4.3 Testing the Released Chips

The SUMMIT chips that were used to test the release protocol have RF switches, capacitors and transmission lines on them. These structures are not the ideal test benches to detect stiction as they are usually tested by using complex instruments like the HP8510 that uses the microwave theory concept of s-parameters. Also, these structures do not move or displace over a large distance, which is usually a criterion in studying stiction in MEMS devices. The few movable structures that are there on the chip move in the vertical direction, instead of lateral, making it difficult to detect and analyze these movements. The complex nature of the components on the chip also make it difficult to conclude whether a particular released device failed in its operation because of stiction or charge build-up or mechanical damage to the structure during release.

5.5 Design of Cantilever Beams to Characterize Stiction

Cantilever beams are the simplest of all MEMS strutures for design, fabrication as well as testing. Their layout is very easy to design and the calculations involved in the analysis and testing of these structures are also not complex.

If sticking forces present during release are more than the opposing forces (elastic energy stored in the beam, applied voltage to the beam), they pull the beam down towards the substrate. This can be detected very easily by simple observation under an optical microscope. The pulled down portion of the beam appears of a different color than the portion of the beam near the clamp because of difference in the topography. The effect of stiction on a cantilever beam during release is indicated in Fig 5.6a and Fig. 5.6b.

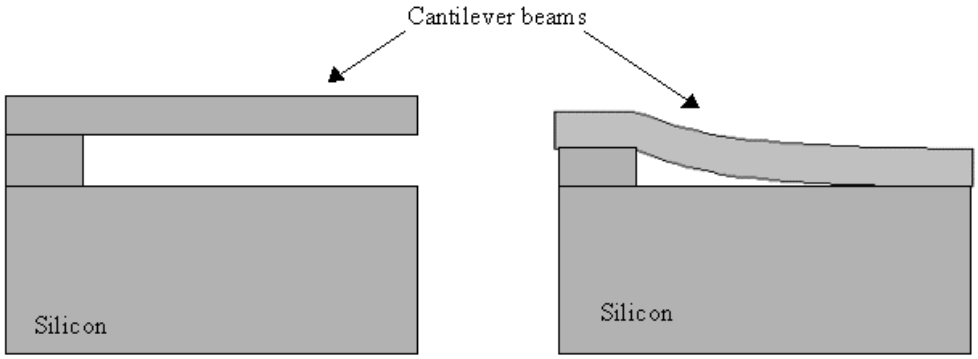

Fig. 5.6a No stiction after release

Fig. 5.6b Effect of stiction after release

The maximum detachment length decreases as the width of the cantilever beam increases. This phenomenon indicates that for long and flexible structures, as rinsing liquid starts to evaporate the liquid bridge splits and moves toward the flexible tip as seen in Fig 5.7 d and Fig 5.7e. Fig 5.7e shows the final liquid drop below the tip. This liquid creates an initial pull-down force through capillary action. The maximum detachment length depends upon the pull-down force and thus the area of this liquid drop. Due to the

tendency of the drop to be circular (to minimize the free surface area), the final liquid area should be proportional to approximately square of the beam width if the gap is much smaller than the beam width

The cantilever beam will spring back and become a free standing structure i.e. (released) if the elastic energy stored in the pull-down beam is larger than the capillary pull-down energy. For a given beam length, elastic energy is proportional to beam width [21]:

$$F=ky=\frac{w*h^3*E*y}{4*l^3} \qquad \text{……..(5.2)}$$

where w= beam-width, h =beam thickness, E = Young's modulus, y = vertical displacement at the end and l = length. The capillary pull-down energy that causes surface contact is proportional to the square of the width as explained above [20]. Thus the liquid pull-down energy increases at a greater rate than beam elastic energy as width increases and so the maximum detachment length for evaporation drying decreases with increasing width.

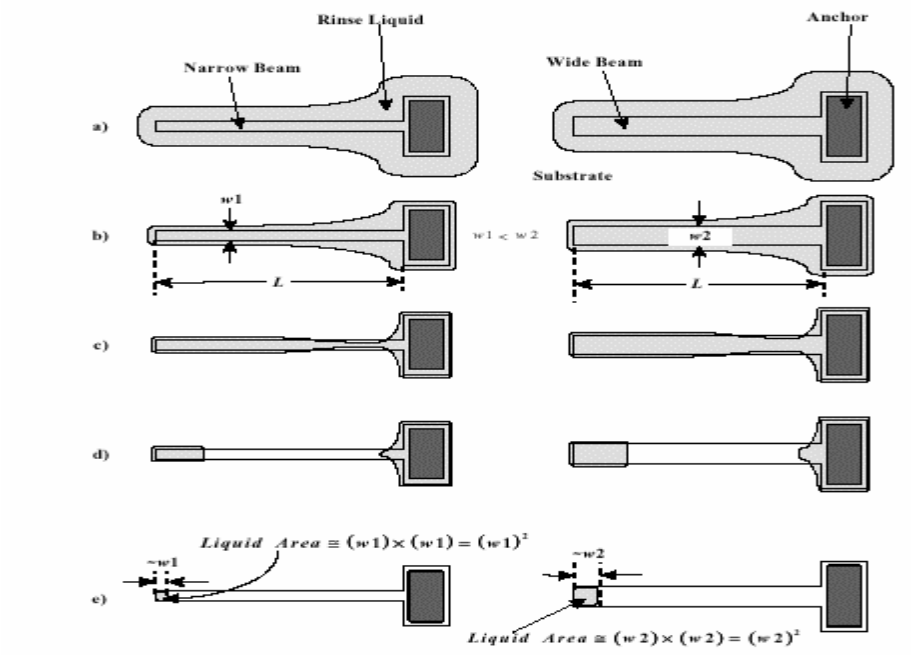

Fig. 5.7 Projected drying steps for evaporation release of two cantilever beams with different width [21].

5.5.1 Application and Testing of the Cantilever Beams.

The Fig. 5.8 shows the CAD plot of an array of cantilever beams that have been designed in the SUMMIT process to help in our studies related to stiction. These beams can be used to study release related stiction as well as in-use stiction. These beams can also be probed and tested if required. The probe station, here at NCSU-EGRC-301, can be used for this purpose. Small microprobes hooked onto an oscilloscope and function generator can be used to excite the beams and observe their deflection. Using the microprobes, DC voltage as well as an AC signal can be applied to the beams and their resultant behavior can be studied under the optical microscope.

The beams have been design based on the aforementioned relations between the beam length, beam width and stiction. An array of beams has been created with varying lengths and widths (lengths varying from 150μm to 500μm and widths varying from 3μm to 50μm). Also, the beams have been made in different polysilicon layers to study the effect of the mass of the beam on release-related stiction.

These structures have been sent to Sandia National Laboratories for fabrication and, are expected to be back by September/October. These beams can be used to study their behavior during the release process and also study the effects of release-related stiction with the varying beam dimensions.

The entire array of beams shown in the Fig 5.8 has a Poly0 ground plane underneath it. To test these beams a voltage needs to be applied onto the beam support through a

microprobe. The beam support (Fig. 5.9) has been made sufficiently large (40μm X 40μm) to act as a probe pad.

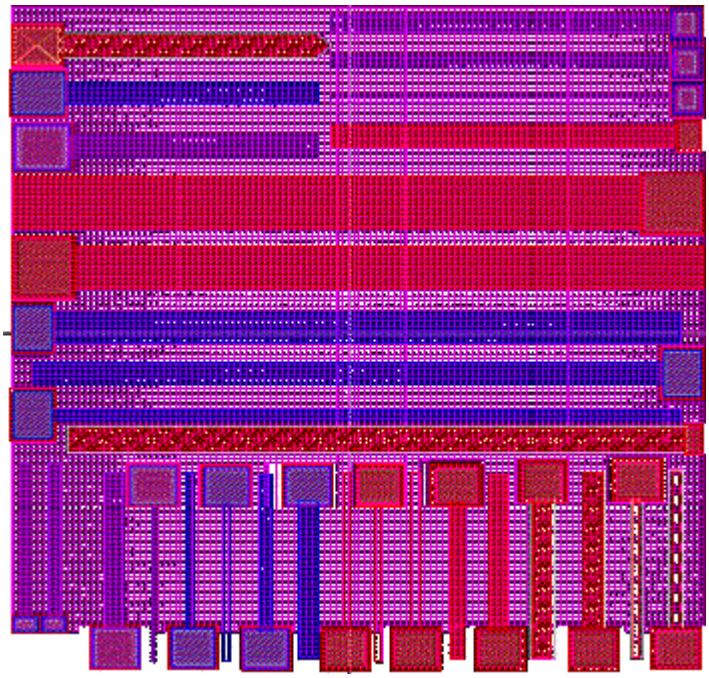

Fig. 5.8 Layout of cantilever beams in Cadence-Virtuoso

Fig 5.9 shows some of the individual beam structures enlarged.

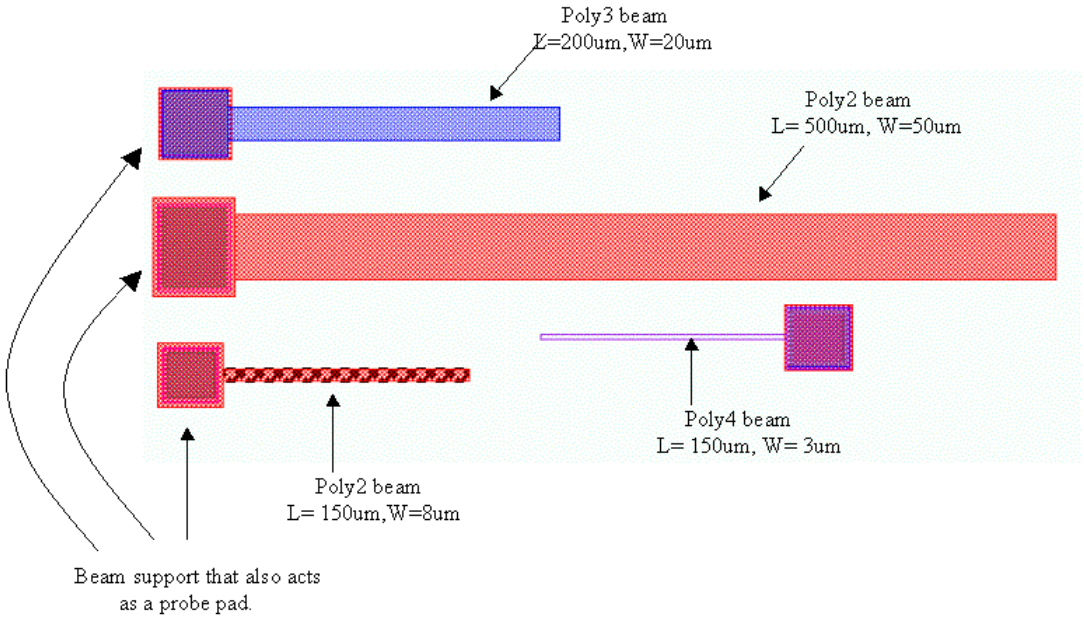

Fig. 5.9 Individual beam structures

Chapter 6

Conclusion and Future Work

6.1 Textiles Pressure Sensor

In this thesis an approach has been made in the design and fabrication of a Piezoresistive Pressure Sensor that can be used in Textile Industry. The designed sensor was simulated and analyzed in MEMCAD and then it was attempted to fabricate in the cleanroom at NC State University.

A process flow was designed for fabricating the sensor and a Traveler document was generated in this regard. During the course of Processing it has been found that the chief hurdle in the completion of the sensor fabrication is the "Back-side alignment". As, in case of many MEMS devices, the fabrication of this Pressure Sensor involves processing of the wafer on both sides. There is front-side processing that involves the fabrication of diffused resistors to act as piezoresistive elements and the back-side processing that involves Bulk etching of the wafer to create a diaphragm underneath the resistors. The Karl Suss MA6 aligner, in the NC State Cleanroom, does not have the provision to do backside alignment and hence the issue arises.

There are a couple of alternatives to overcome this problem. The first is to use an infrared source for alignment [23]. In this method an infrared (IR) light source is placed on one side of the wafer-mask pair and the optical objective is on the other side. Since silicon is transparent in the IR spectrum, the wafer and the mask can be aligned to each other. For optimum results the silicon wafers should be double side polished, which is the case for the pre-thinned wafers, and hence this option is viable.

Another approach is to use "through wafer via holes". By etching via holes in the wafer through the entire wafer, the alignment marks on the mask may then be used as reference to do the front and backside alignment. However this approach is tricky because handling pre-thinned wafers will become very difficult once they have etch holes in them all the way through and hence should be used with caution.

During the fabrication process it is found that, creating an array of diaphragms of 20 um thickness on pre-thinned wafers is very difficult using wet etch techniques like TMAH. The diaphragm breaks either when the wafer is being pulled out of the viscous TMAH solution because of the surface tension of the liquid or when the wafer is being blow-dried by a nitrogen-gun. Although, etch depths upto 80 μm have been measured, on a 200 μm thick wafer, using the Profilometer, further measurements have not been possible as the diaphragm breaks down. This problem can be solved by doing a partial wet etch initially as it is faster, and then doing a (dry etch) Reactive Ion Etch (RIE).

Future work will involve working on the backside alignment problem and testing the final pressure sensor device. Once the backside alignment issue is tackled, it will be possible to do the bulk etching step as the last in the fabrication process flow and this will also reduce the handling issues of the pre-thinned wafers post "bulk-etching".

6.2 Release Protocol for MEMS Devices

A part of this thesis aims at developing a Release Protocol for MEMS devices made in the SUMMIT^{TM} Process. The procedure involves a wet HF etch of the chips made in SUMMIT^{TM} process, followed by drying them and observing and testing them to confirm that the devices on the chip have been released.

The chips were etched and dried and observed under an optical microscope for the presence of oxide. These observations indicate that the chips do seem to have been released; however, in order to confirm this, the devices on these chips need to be electrically tested. The chips that were available for doing the release had an inherent

design flaw, in that, the POLY 3 and POLY2 layers were not connected together by means of via holes. Hence the devices could not be tested for their motion by electrical actuation. Further, these devices are RF components like transmission lines and RF switches, which have their own testing issues, and do not have a significant lateral or vertical movement that can indicate that the devices have been released, upon electrical activation.

To circumvent this problem, cantilever beams have been designed in the SUMMIT^{TM} process, and sent to Sandia National Labs for fabrication. Upon, their arrival these devices can be released using the same protocol as above and then electrically tested to observe their motion and confirm the release. Testing of cantilever beams is fairly simple. The entire array of beams has a ground plane, which can be hooked up, as circuit ground. The beam supports (clamps) have been designed to be sufficiently large so as to serve as a landing pad for a test probe or to wire-bond it onto a chip. On applying a suitable activation voltage to the beam and grounding the ground plane, the beam will be attracted towards the substrate and will bend downwards. This motion will vary from 2 um to 10.25 um depending on whether the beam is made of POLY1 or POLY4 layers respectively.

Future work would involve trying out the release protocol on the Cantilever beams and electrical testing of the Cantilever beams to verify that they have been released. These structures can further be used for studying Release-related stiction.

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Appendix A

Processing Measurements

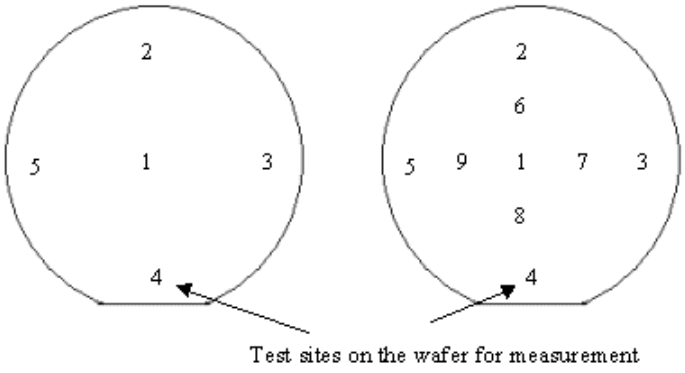

Fig. 1 Wafer map (points indicate measurement sites)

• Table 1 indicates the results of measurement of nitride film thickness after it was put in TMAH for 50 minutes at 91°C. The results indicate the etch rate of nitride by TMAH.

Table 1

	Nitride thickness measurements before TMAH etch (in A°)	Nitride thickness measurements after TMAH etch (in A°)
1	2534	2534
2	2649	2645
3	2616	2616
4	2650	2647
5	2555	2529
Avg.	2600.8	2594.2

Avg. Etch rate = (2600.8-2594.2)/50 = 0.132A°/min.

•Table 2 indicates the thickness measurement of nitride film on the first batch of wafers.

Table 2

Nitride thickness measurements on first batch of wafers.

	Wafer#1 (A°)	Wafer#2 (A°)	Wafer#3 (A°)
1	588	584	587
2	601	599	589
3	578	575	570
4	595	592	598
5	616	610	611
6	589	588	583
7	580	578	572
8	586	585	582
9	594	598	592
Avg.	591.8	589.8	587.1

•Table 3 indicates the nitride thickness measurements on the monitor wafer used in the second batch of wafers.

Table 3 Nitride thickness (A°)	
1	190
2	184
3	191
4	198
5	192
Avg.	191

• Table 4 indicates the LTO thickness measurements for the first batch of wafers, on the monitor wafers.

Table 4 LTO thickness measurement on monitor.		
	Wafer#1 (A°)	Wafer#2 (A°)
1	341	351
2	340	346
3	323	330
4	329	325
5	329	334
Avg.	332.4	337.2

• Table 5 indicates the thickness measurement of LTO on nitride for the second batch of wafers.

Table 5 LTO thickness measurements(A°)	
	Monitor Wafer
1	811
2	647
3	858
4	1129
5	820
Avg.	853

• Table 6 indicates the data to calculate the etch rate of "trans-N" solution on nitride. Two wafers coated with nitride were put in the solution for 8 minutes.

Table 6 Etch rate of "trans-N" on nitride				
	Wafer#1 (before etch A°)	Wafer#1 (after etch A°)	Wafer#2 (before etch A°)	Wafer#2 (after etch A°)
1	2549	1990	2573	2016
2	2521	2031	2521	2040
3	2577	2045	2599	2069
4	2626	2035	2638	2060
5	2585	1996	2593	2010
Avg.	2571.6	2019.4	2584.8	2039

The amount of nitride etched for wafer#1 is 552.2 A° and for wafer#2 is 545.8 A°. The average etch rate for the two wafers is [(552.2+545.8)/2]/8 = 68.6 A°/min.

• Table 7 the data to calculate etch rate of "trans-N" on LTO. Wafers with LTO on them were put in a "trans-N" solution for 8 minutes at 180°C.

Table 7
Etch rate of "trans-N" on LTO.

	Wafer#1 (before etch A°)	Wafer#1 (after etch A°)	Wafer #2 (before etch A°)	Wafer#2 (after etch A°)
1	829	588	721	481
2	772	551	698	487
3	816	578	728	490
4	839	586	741	487
5	835	582	735	480
Avg.	818.2	577	724.6	485

The amount of LTO etched from wafer#1 is 241.2 A° and that from wafer#2 is 239.6 A°. Hence the average rate of LTO etch using "trans-N" is [(241.2+239.6)/2]/8 = 30 A°/min.

- Table 8 indicates the thickness of oxide formed on the monitor wafer during diffusion.

Table 8 PDS oxide thickness measurement on monitor wafer (A°)	
1	1142
2	1117
3	1117
4	1124
5	1125
Avg.	1125

Appendix B

MEMCAD Simulation Analysis

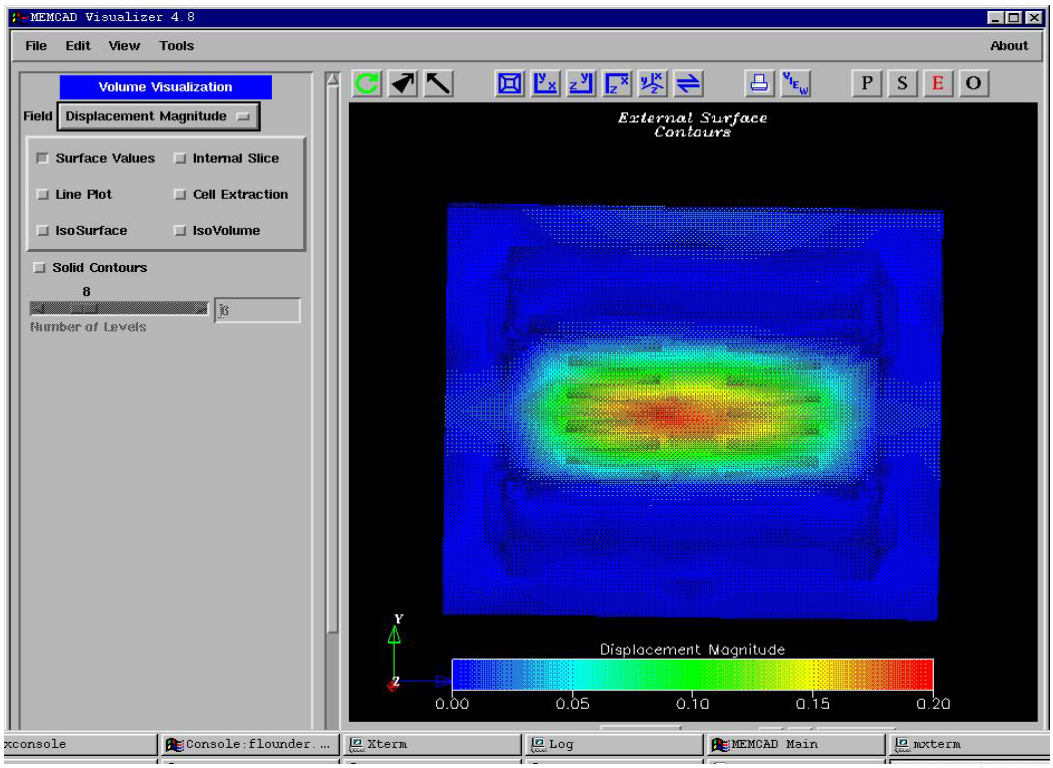

Fig. 1 Result from MEMCAD Simulation showing the Displacement magnitude across the diaphragm.

For a 50µm thick diaphragm, with a Pressure of 1MPa MEMCAD gives a displacement of 0.2µm at the center of the diaphragm.

Calculations

$$P = [\pi^4/6*(E* H^3)* c_1]/(1-\nu^2)*L^4 \qquad \text{……..(7.1)}$$

where E = Young's Modulus of silicon = 190 GPa

H = diaphragm thickness = 50μm

P= applied pressure = 1MPa

c_1= displacement at the center of the diaphragm.

ν = Poisson's ratio in [110] direction of a (100) plane = 0.06

L = diaphragm length = 1145μm.

Resulting calculations indicate that **"c_1" = 4um.** This result is about an order more than the value indicated by MEMCAD simulations. This can be attributed to the fact that equation 7.1 is a highly simplified expression modeling the diaphragm behavior.

Also, the longitudinal surface stress on the diaphragm is given by

$$\sigma_x = 0.606*(L/H)^2 * P \qquad \text{……..(7.2)}$$

Substituting the known values of L, H and P we have σ_x **= 317 MPa**.

And the resultant change in resistance in resistance is given by

$$\delta R_1/R_1 = (-33.19*10^{-11})\ \sigma_x \qquad \text{……..(7.3)}$$

which gives $\triangle R_1/R_1$**= 0.105,** i.e. a 10.5 % change in resistance.

Appendix C

Release Protocol for MEMS

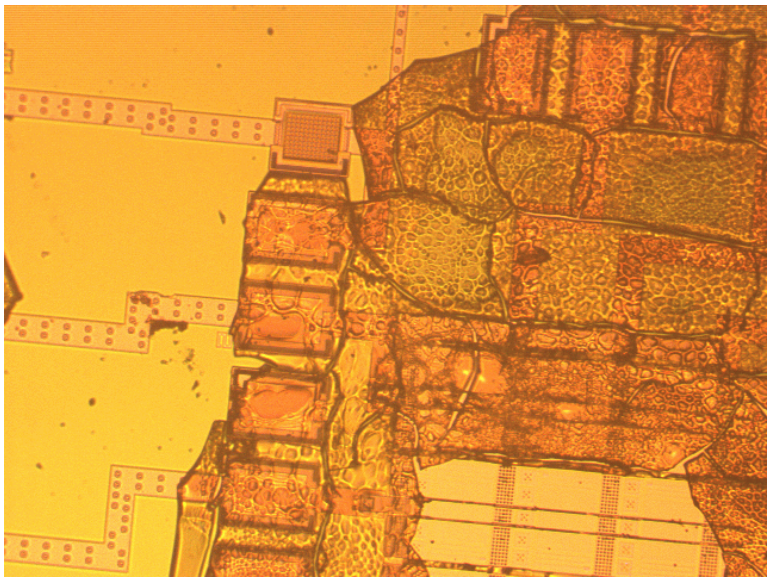

Fig. 1 Observation with water as a rinsing solution after release.

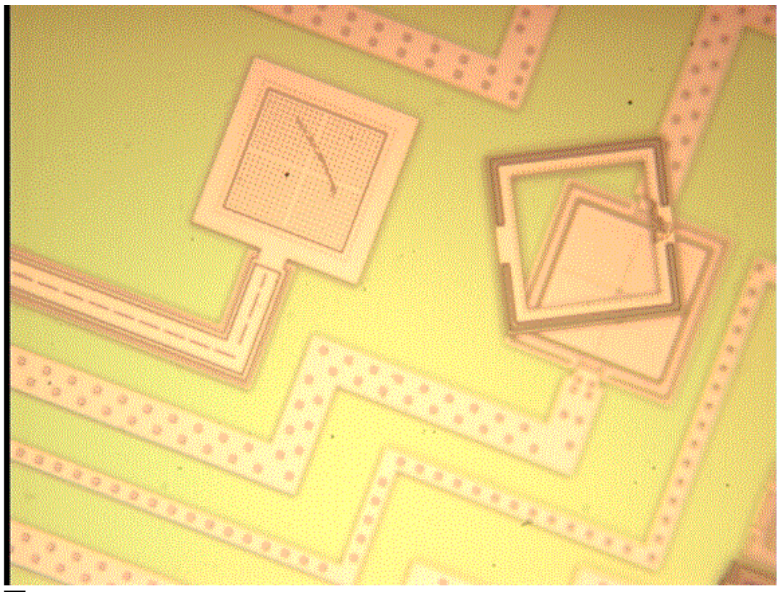

Fig 2 Observation after rinsing the released chip with Methanol.

The floating structure seen in the picture indicates that the chip has been released.

Appendix D

Traveler

1) Trial run with nitride coated wafers to determine etch rate of TMAH on nitride.
   Time = 50 min, temperature = 91°C.
2) Ellipsometry to determine nitride thickness after TMAH etch.
3) JTB clean
   Time = 10 min.
4) Wash and blow-dry
5) Nitride Deposition
   Time = 15 min, target thickness = 500 A°, temperature = 800°C, 775°C, 775°C. Pressure = 300mTorr, monitor wafer used.
6) Ellipsometry
   Nitride thickness measurements.
7) LTO Deposition
   Time = 20 min, target thickness = 600 A°, Pressure = 660 mTorr, Temperature = 410 °C, gas flow: oxygen = 30%, 300 sccm; LTO = 30%, 151 sccm, monitor wafer used.
8) Elipsometery to measure LTO thickness on monitor wafer.
9) Bond wafers to a substrate using adhesive.
   Temperature = 110°C, adhesive = Crystalbond 509, use hot plate.
10) Spin Photoresist.
    Spin time = 40 sec, rpm = 4000, PR used = S1813.
11) Expose wafers using mask HOLE2
    Time = 8 sec, Power of Aligner = 361 W.
12) Develop PR.
    Time = 1min 30 sec, endpoint detection: visibility of structures, 10 sec overdevelop.
13) Wash and blow-dry wafers.

14) Hard bake wafers for 1 min, enhances PR performance as a mask during etch.

15) LTO etch

Time = 40 sec, endpoint detected by “de-wet” of the monitor wafer, PR acts as mask for LTO etch.

16) Wash and blow-dry wafers.

17) Strip PR

Strip time = 12 minutes, endpoint detected by the color of the dripping solution form the wafers, solution turns from dark brown to colorless.

18) Wash and blow-dry wafers.

19) Nitride Etch

Time = 10 minutes, timed etch, etch rate of “trans-N” is first determined, both on LTO as well as Nitride.

20) Wash and blow-dry.

21) De-bond wafers.

Time = 10 min, temperature = 121°C, use hot plate.

22) Wash wafers in Acetone to remove residual adhesive on the wafer.

23) Wash and blow-dry the wafers.

24) Diffusion

Time = 70 min, temperature = 943°C, nitrogen flow = 3976 sccm, monitor wafer used for oxide thickness measurement, sheet resistance = 5.78Ω/□, avg. oxide thickness = 1125 A°, junction depth = 1.5um.

25) Ellipsometery to determine oxide thickness on monitor wafer.

26) P-Deglaze to remove P_2O_5.

Time = 30 sec, end point determined by de-wet of the monitor wafer.

27) Wash and blow-dry wafers.

28) Aluminum Deposition

Time = 2.47 minutes, thickness = 2000 A°, E- beam evaporation.

29) Aluminum thickness measurement on Dektak-II profilometer

30) Bond wafers using Crystalbond 509.

31) Spin PR.

Time = 40sec, rpm = 4000, PR used = S1813.

32) Expose wafers, using mask METAL1.

Time = 8 sec, Aligner power = 361W.

33) Develop PR.

Time = 1 min.

34) Aluminum etch

Time = 2 minutes, endpoint is the loss of shiny metal appearance on wafer face.

35) Strip PR

Strip time = 12 minutes, endpoint detected by the color of the dripping solution form the wafers, solution turns from dark brown to colorless.

36) Batch I wafers, Nitride deposition.

Time = 25 minutes, target thickness = 500A°, temperature = 800°C, 775°C, 775°C, Pressure = 300mTorr.

37) Ellipsometry to measure nitride film thickness.

38) LTO deposition

Time = 10 min, target thickness = 300 A°, Pressure = 660 mTorr, Temperature = 410 °C, gas flow: oxygen = 30%, 300 sccm; LTO = 30%, 151 sccm, monitor wafer used.

37) Ellipsometry on monitor wafer to determine LTO thickness.

38) Bond wafers using adhesive.

Temperature = 110°C, adhesive = Crystalbond 509, use hot plate.

39) Spin PR.

Time = 40sec, rpm = 4000, PR used = S1813.

40) Expose PR using mask P1P2VIA.

Time = 8 sec, Aligner power = 371W.

41) Develop PR.

Time = 1min 30 sec, endpoint detection: visibility of structures, 10 sec overdevelop.

42) Wash and blow-dry.

43) Hard bake wafers for 1 min.

44) LTO etch.

Time = 25 sec, endpoint detected by “de-wet” of the monitor wafer, PR acts as mask for LTO etch.

45) Strip PR.

Strip time = 12 minutes, endpoint detected by the color of the dripping solution form the wafers, solution turns from dark brown to colorless.

46) Wash and blow-dry.

47) Nitride Etch

Time = 10 minutes, timed etch, etch rate of "trans-N" is first determined, both on LTO as well as Nitride.

48) Wash and blow-dry.

49) De-bond wafers.

Time = 10 min, temperature = 121°C, use hot plate.

50) Bond wafers to substrate coated with Nitride, using Crystalbond 509.

51) TMAH Etch

Temperature = 91°C, time = batch of 30 minutes each for about 3 hrs, prevent evaporation of TMAH by covering dish, replenish solution from time-to-time.

52) Etch Depth measurement using Profilometer.