ABSTRACT

SHAH, CHINTAN HEMENDRA. Inductively Coupled Interconnect for Chip to Chip Communication over Transmission Line. (Under the direction of Dr. Paul Franzon).

As data frequency increases beyond several Gbps range, low power chip to chip communication becomes more critical. The concept researched in this thesis is inductively coupled interconnect (LCI) over short length transmission line. The data will be transmitted across a 10 cm differential microstrip line on FR-4 material with a transformer on each side of the line. The transmitter and receiver circuits are designed in TSMC 0.18μm process technology and can operate at 2.5 Gbps. The power consumption of the design is 5.53 mW at 2.5 Gbps which yields around 2.21 $mW.Gb^{-1}.s^{-1}$. This design can achieve BER of less than 10^{-12}. The inductive coupling will reduce DC power because the low frequency DC component of the signal will be blocked by coupling inductors. The power consumed by this design is lower than most of the conventional I/Os that use physical contact interconnects. An H-bridge current steering driver is used at the transmitter and a differential amplifier and Sense-amp Flip flop is used at the receiver.

Inductively Coupled Interconnect for Chip to Chip Communication over Transmission Line

by
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BIOGRAPHY

Chintan Shah was born in Ahmedabad, India in 1984. He moved to United States in 1996 at age 11. He graduated with an undergraduate degree in Electrical and Computer Engineering from NC State University in 2006. During undergraduate he did an internship at IBM in RTP, NC working on board design in their server division. After completing his bachelor's degree he pursued master's degree in Electrical Engineering at NC State University. He worked on his thesis under the guidance of Dr. Paul Franzon from January 2008 to March 2009. He worked as an intern in Qualcomm for their circuit design group in Raleigh, NC during 2008. After completing his master's requirement he joined Qualcomm as a circuit design engineer on their next generation processor team at Raleigh location.

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1

Introduction

1.1 Motivation

As the technology scales and the bandwidth increases beyond several Gbps, the power consumption between a chip-to-chip communication increases significantly. Data transmission between a processor and a memory or a processor and a graphics card requires transmission rate of over 1 Gbps. Chip I/Os has generally been the bottleneck of the chip performance. This research presents a new way of minimizing the I/O power and as well as improving the bandwidth.

In today's technology, a short length chip-to-chip communication consumes power in the order of 20 $mW.Gb^{-1}.s^{-1}$ [1]. In a conventional interconnect, the signal pins from a chip are connected physically to the board which reduces the bandwidth and increases DC power. In a digital transmission, the data information is only contained within the transition edges and thus the DC component of the signal is not required. The DC power is high in a conventional interconnect because transition edges as well as the DC component of the digital signal are being transmitted.

To eliminate the low frequency and DC component of the signal, the AC coupling technique can be utilized. This research focuses on reducing the chip-to-chip I/O power during high speed data transmission using the AC coupled interconnect (ACCI) technique. ACCI relies on non-contacting passive coupling device to transmit data. In an ACCI system, data is only transmitted on transition edges of the signal. ACCI uses passive device such as a coupling capacitor in capacitive coupling interconnect (CCI) or a pair of spiral inductors acting as a transformer in inductively coupling interconnect (LCI). The capacitor in CCI and a transformer in LCI would filter out the low frequency and DC component of the signal, vastly reducing the DC power [3].

The technique explored in this thesis is inductive coupling interconnect specifically over a short length transmission line. The application of this technique can be in high speed communication line between processor and a memory on the same circuit board. In LCI, two spiral inductors are stacked on top of each other with limited spacing between the inductors. The transformer works on the principle of applying current through the primary inductor, which would generate a differential voltage pulse on the secondary inductor. The challenge is in producing large enough output voltage pulse to be detectable by the receiver after going through a lossy transmission line and a second transformer without sacrificing power. The size of the voltage pulse depends on the coupling coefficient of the transformer and the rate of change in current being applied at the transmitter.

The bandwidth of an LCI system can be extended to beyond 2 Gbps for the TSMC 0.18μm technology. The circuits are designed specifically to reduce power. Various power efficient designs of transmitter and receiver were explored in this thesis. The output of the

transformer is differential and differential signaling is preferred to reduce noise. The signal is transmitted over a 10 cm long microstip line to the receiver. A transformer is used at the transmitter and the receiver end. The transformer is modeled and simulated using E-M tools HFSS and Q3D. The design works successfully at 2.5 Gbps and could be extended to 3 Gbps.

1.2 Organization

Chapter 2 focuses on the Transformer design and transmission line. A RLC equivalent model of the transformer and spice model extraction are also given. Chapter 3 overviews the transceiver circuits design. The operations of the transmitter and the receiver are discussed with some power reduction technique. The simulation results are recorded in the Chapter 4. It shows the simulation over varying process corners and temperature. It discusses the power improvements over other conventional chip-to-chip communications. The predicted BER is also calculated statistically. Chapter 5 discusses the conclusion of the thesis and the future work that needs to be looked at.

2

LCI Overview

In inductively coupled interconnect (LCI) the coupled spiral inductor will act as an interconnect between the chip and the board. Inductive coupling replaces the physical contact between a chip and a board. Jian Xu in his Ph.D dissertation describes inductively coupled interconnect circuits for 3-D ICs where a receiver is placed at the output of first transformer [3]. This work extends that concept by using multiple transformers over a transmission line. A transformer is placed at each end of the transmission line to connect to transmitter and receiver. Figure 2.1 shows the overview of the system design in this thesis.

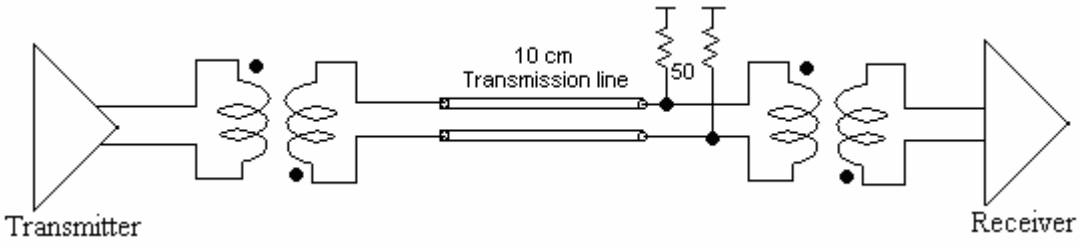

Figure 2.1 LCI Transceiver

2.1 Transformer Overview

The two coupled inductor would form a transformer. The current passed in the first inductor would generate a magnetic flux around the inductor which would penetrate into the second inductor [4]. The amount of flux absorbed by the second inductor is measured by the

coupling coefficient (k). Thus the coupling coefficient is dependent on the strength of the magnetic flux and the spacing between the two inductors. The inductance of the inductor is related to the size of the spiral inductor and the number of turns. Figure 2.2 shows the 3-D view of the inductor. The "w" is the width of the metal, "s" is the spacing between each line, "t" is the metal thickness and "d" is the distance between two inductors. The 2-D model of the transformer was designed in Cadence Virtuoso, and converted to Visual Basic Script (VBScript) using Perl script provided by Evan Erickson. The Visual Basic Script is executed in Ansoft HFSS to create 3-D model of the transformer. The 3D model was simulated in High Frequency Structure Simulator (HFSS). HFSS is software for 3D electromagnetic simulation of high-frequency components [19].

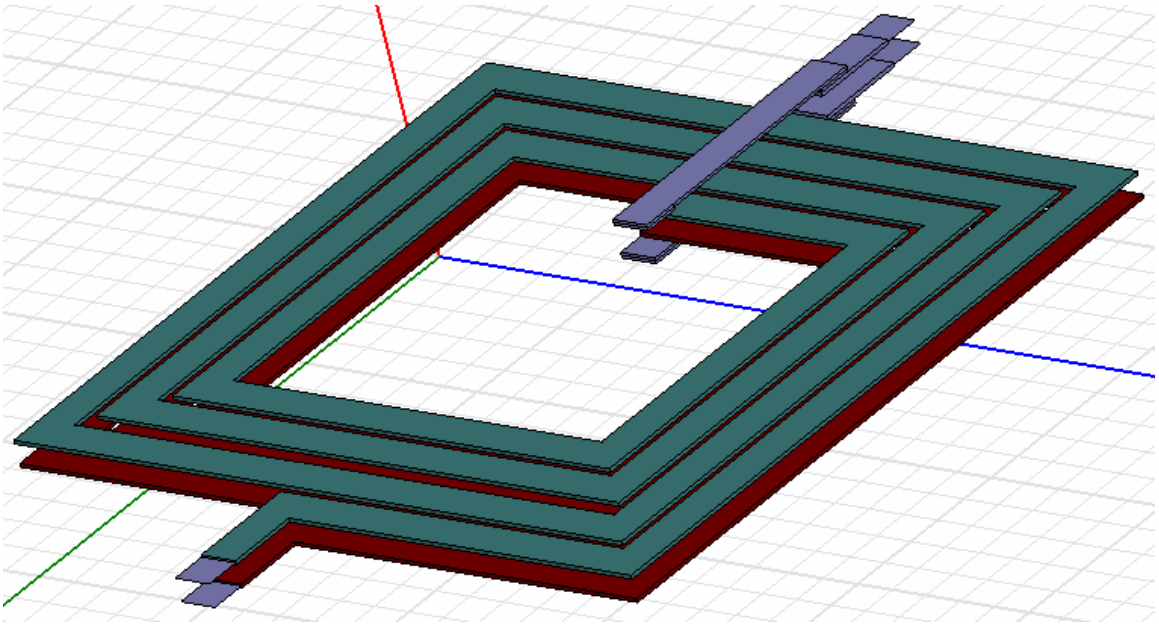

Figure 2.2 – 3-D Transformer model in HFSS

The achieved signal at the output of the transformer is based on the inductance of the inductor and the mutual inductance between the two. Ideally the signal strength will increase

with increased inductance and increased coupling coefficient. But since the transformer in this research is not ideal, the signal strength will also be dictated by the parasitic capacitance and resistance. In this design, a transmitted signal will pass through two transformers before it reaches the receiver. Thus it is important for the transformer to have high coupling coefficient in the range of 0.6 to 0.8 to get detectable signal at the receiver. Jian in his Ph.D dissertation designed a 400x400 μm^2 transformer with 25 μm line width and spacing which had coupling coefficient of 0.58 [3]. The transformer used in this thesis is optimized to have even higher coupling coefficient. The size is reduced to 380x380 μm^2, with 20 μm line width and 5 μm spacing. Reducing the line spacing increases coupling coefficient. The inductor dimensions and the generated self inductance designed in this thesis are shown in Table 2.1. The spacing between two inductors is 10μm.

Table 2.1 – Inductor dimensions and inductance

Width (w)	**Spacing (s)**	**Thickness (t)**	**Diameter**	**L1**	**L2**	**k**
20μm	5μm	2μm	380μm	6.63nH	6.63nH	0.662

Scattering parameter of each port is shown in figure 2.3. From the magnitude plots in figure 2.3, the power of the received signal on output ports 3 and 4 is in the range of -6dB to -8dB at around 5 GHz. Majority of the signal component is roughly around 5 GHz. Signals at port 3 and 4 are differential and thus maintain 180° phase difference for all frequencies.

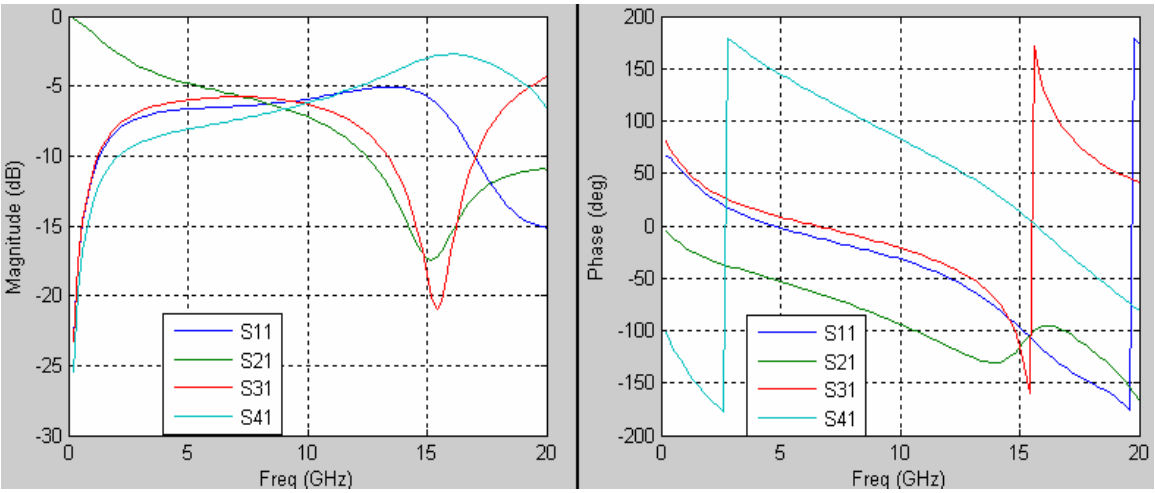

Figure 2.3 – S-parameter of the Transformer

The transformer was designed and simulated in HFSS. The inductors are built on a Benzocyclobutene (BCB) substrate with air between the inductors. The equivalent low bandwidth RLC circuit was extracted from the HFSS run. The RLC model is shown in figure 2.4. L1 and L2 are the inductors and k is the coupling coefficient between L1 and L2. Cm1 through Cm4 are the mutual capacitance between the two inductors. C1 through C4 are parasitic capacitors between the inductor and the substrate. R1 through R4 are very small resistance in the value of μΩ and can be treated as a short. Capacitors Resistors R2, R7, R8 and R9 are resistive losses of the inductor. For detailed view with all the values of the RLC components please refer to figure A.13 in Appendix A.

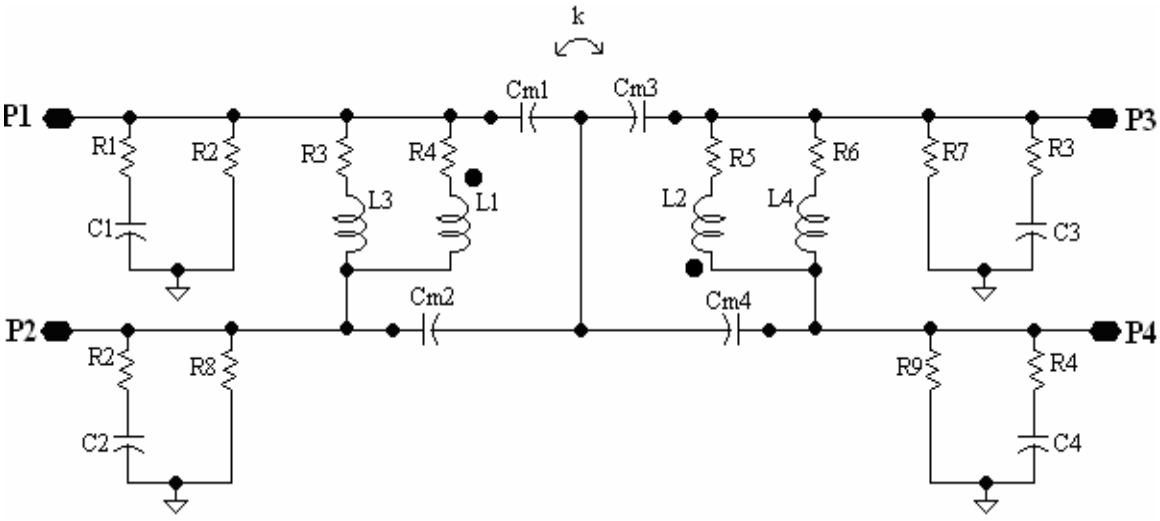

Figure 2.4 – RLC equivalent model of Transformer

2.1.1 Crosstalk

Crosstalk noise at the victim transformer is generated by the surrounding transformers. The spacing between adjacent transformers contributes significantly to the crosstalk noise at the victim. The unwanted coupling capacitance and inductance between the adjacent transformers is observed to determine the minimum spacing required to maintain constant BER.

The coupling capacitance and inductance were calculated using Ansoft Q3D extractor. Q3D is a 3D parasitic extraction software that can extract RLC models to be used in SPICE simulation. The coupling capacitance and inductuctance are extracted from Q3D and used with the original model generated by HFSS. In Q3D, two different extraction are simulated; one in horizontal direction and other in vertical direction. In vertical direction shown in figure 2.6, the sides with I/O ports of inductor are side by side with the adjacent

inductor's I/O port. In horizontal direction shown in figure 2.5, the other two sides are side by side. All the inductors are on the same plane with similar geometry.

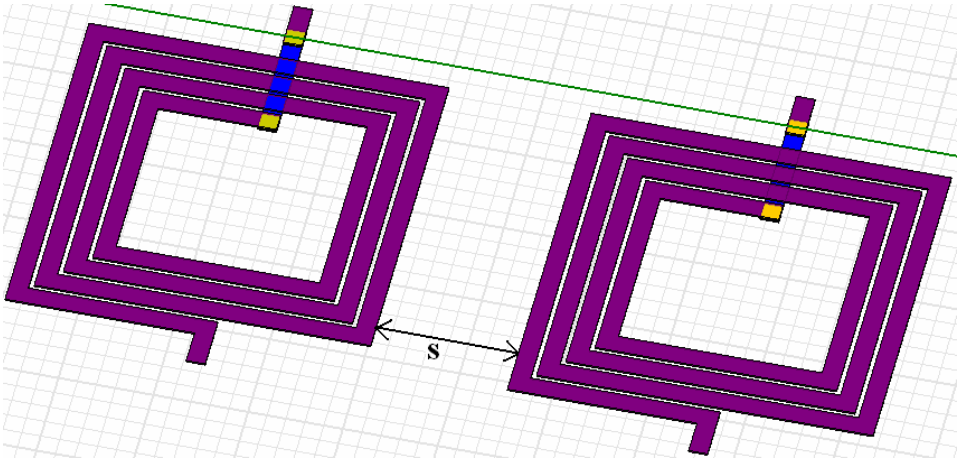

Figure 2.5 – Horizontal arrangement of adjacent Transformer

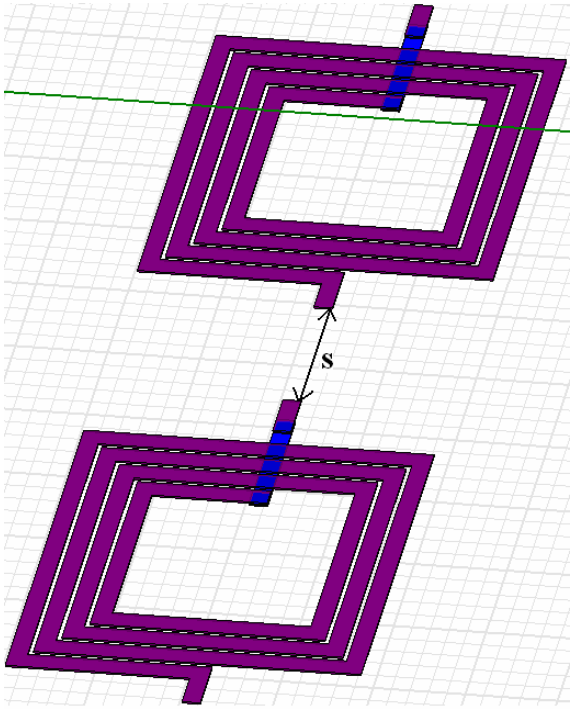

Figure 2.6 – Vertical arrangement of adjacent Transformer

The mutual capacitance (Cm) and coupling coefficient (k) between two inductors have been calculated and recorded in Table 2.2. Increasing the spacing decreases the parasitic

capacitance and inductance. The mutual capacitance has much higher impact on the victim than mutual inductance. The coupling coefficient is very low and can be negligible even for shorter distance. The maximum spacing is 380 μm which is the diameter of the inductor. The impact of crosstalk noise on the amplitude of the signal is discussed in Chapter 4.

Table 2.2 – Mutual Capacitance and Inductance for adjacent inductors

	Vertical		**Horizontal**	
Spacing (s)	**Cm**	**k**	**Cm**	**k**
100 μm	65 fF	-0.0002	74.36 fF	-0.008
150 μm	61.3 fF	0.008	68 fF	-0.004
200 μm	56.3 fF	0.00095	62 fF	0.002
380 μm	49 Ff	0.006	52 fF	0.01

2.1.2 Transformer Packaging

The transformer designed in this thesis only has a gap spacing of 10 μm between the two inductors. Current technology of placing solder bumps on surface of the PCB would be inadequate in providing such small spacing. The technique of buried solder bump for AC coupled interconnects developed by Franzon et al. can be used to achieve spacing in the range of 10 μm [16]. Mick in his Ph.D dissertation gives a graphical view of how the solder bumps are buried into trenches to decrease the gap spacing between coupling elements [4]. Figure 2.7 shows the cross-section view of the buried solder bumps as shown by Mick. These solder bumps are the power and ground connections which needs to be physically connected. Buried solder bump also provides a good way to self-align the chip and the PCB with minimal coupling spacing.

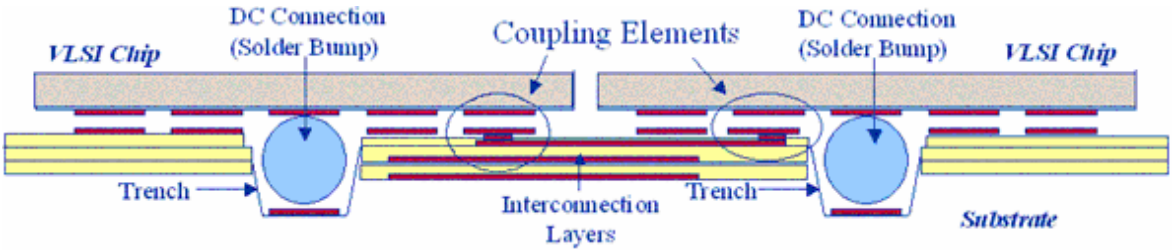

Figure 2.7 – Buried solder Bump technique for LCI

2.2 Transmission Line

The transmission line used in this thesis is a coupled microstip line. It is simulated using 2-D Hspice simulator [11]. The width (W) of the metal is 101.4 µm, thickness (T) is 17.5 µm, and spacing (S) is 101.4 µm. The length (L) of line is 10 cm. The metal to ground spacing (H) is 25.4 µm or 1 mil. The cross-section of the line with the corresponding labels is shown in figure 2.8. The line is constructed on FR-4 material with dielectric constant of 4.4 and loss tangent of 0.02. The dimensions simulated in this research are the minimum dimension that can be fabricated by Suwa Precision Engineering Component Manufacturers who specializes in PCB fabrication [10]. Spiral transformers are connected at both ends of the line as shown in figure 2.1. Hspice generates a w-element model of the transmission line. The RLGC matrix of this model is shown in Table 2.3.

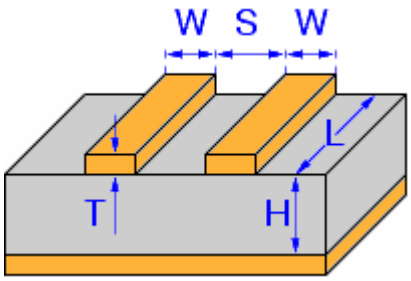

Figure 2.8 – Transmission line cross-section

Table 2.3 – RLGC Matrix of Transmission line

		Self Line 1	**Mutual**	**Self Line 2**
DC Inductance	L (H/m)	1.75e-7	1.027e-8	1.75e-7
DC Capacitance	C (F/m)	2.137e-10	-2.996e-12	2.137e-10
DC Resistance	Ro (Ω/m)	9.532	0	9.532
DC Shunt conductance	Go (S/m)	0	0	0
Skin Effect Resistance	Rs (Ω/(m*sqrt(Hz))	1.526e-3	9.269e-5	1.526e-3
Dielectric Loss conductance	Gd (S/(m*Hz))	1.343e-11	-1.882e-13	1.343e-11

The dimensions of the transmission line are critical in matching with the transformer. Increasing the width of the line, will increase the self capacitance of the line causing mismatch. The self capacitance of the line for width 101.4um is 2.137e-10 F/m. These value increases to 2.533e-10 F/m for width of 127.4um. This reduces the eye opening at the output of the transmission line. The eye diagram will be discussed more in details in Chapter 4.

3

Transceiver Design

The transceiver designed in this thesis has to operate at over 2 Gbps transmitting over a transmission line. The transmitter and receiver are connected to a transformer. The transceiver is designed in TSMC 0.18μm CMOS technology and verified using hspice simulation. The transmitter will apply a current at the primary inductor which will generate a voltage pulse on the secondary inductor. This pulse will be transmitted across transmission line and feed into the primary inductor on the receiver side. This would generate an even smaller pulse on the second inductor connected to the receiver. The receiver will consist of sensing stage, an amplifier and a Flip flop to detect the received data. The received signal after going through two transformers and a transmission line will be reduced to around 50mV peak to peak differential at the receiver.

3.1 Transmitter

The schematic of the transmitter is shown in figure 3.1. The transmitter is an H-bridge current steering circuit which steers the current in either direction of primary inductor. In the schematic pins p1 and p2 are connected to the primary inductor. The current is steered using large driving inverters. This driver design is adapted from Jian's work in his Ph.D

dissertation [3]. Jian uses two large inverters to induce current through the inductor. The inputs to these inverters are differential, such that during transmission only opposite NMOS and PMOS are turned on. The size of pulse on the secondary inductor is dependent on the rate of change in current in the primary inductor. Equation 3.1 shows the voltage and current relationship for an inductor. Thus it is necessary to have very fast changing current.

$$V = L * {}^{dI}/_{dt} \qquad [3.1]$$

In LCI data is only transmitted on the transition edge of the signal. Thus after the transition, it would be ideal to turn off the current through the primary inductor after the transmission to prevent any wastage power. This could be achieved by using a small pulse of only the fraction of the unit interval for the transmitting. Pulse signaling in LCI system was first introduced by Kuroda et al [5, 6]. The circuit presented by Kuroda's group is shown in figure 3.2. They use a clock pulse to determine the amount of time the current will flow for one data transmission. In this design, I use the pulse generator concept from Kuroda's work and adapt it with driver from Jian's work. In reference [5], they use a digitally controlled precise pulse shaping technique to reduce the pulse size. Reducing the pulse size by a half reduces the driver power by a quarter because shorter pulses will double the current slew rate. For double slew rate, the current only needs to reach half the maximum current to produce the similar voltage pulses at the transformer output. Such technique was not used in this research because driver transistors are very large to drive large inductor load. The width of driving transistors is around 15μm, which would make very difficult to reduce the pulse.

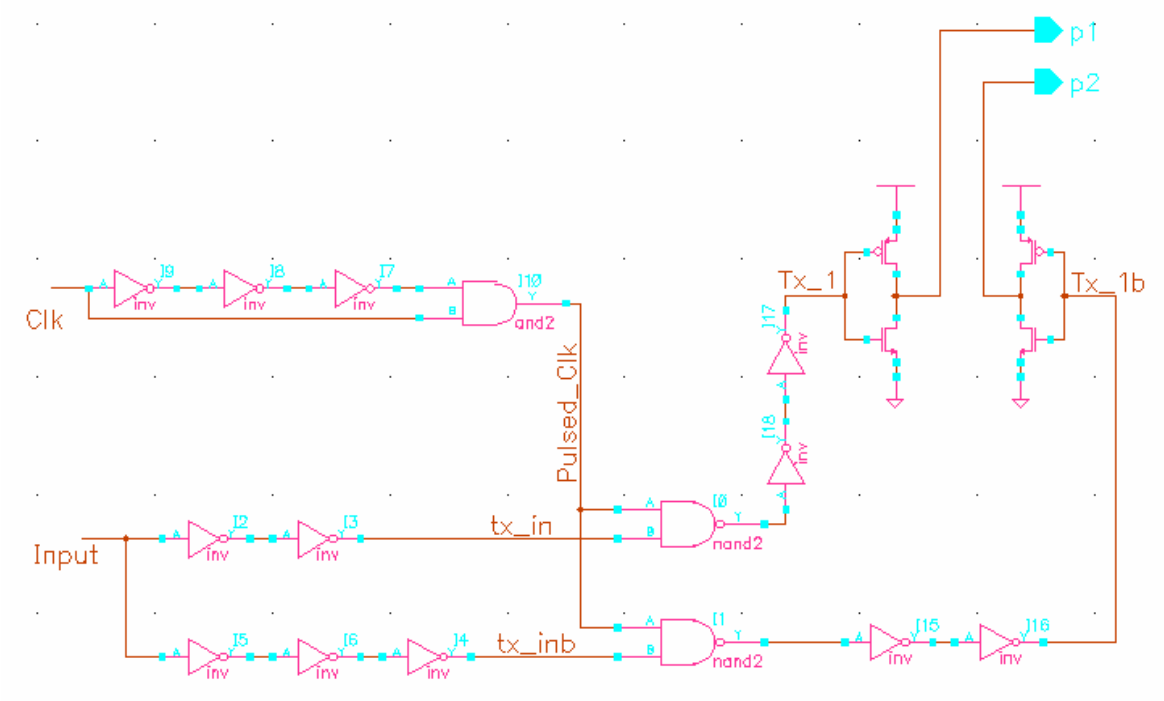

Figure 3.1 – Transmitter Schematic

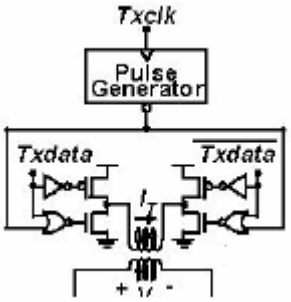

Figure 3.2 – Transmitter from Kuroda's work

Using pulse signaling prevents any wastage power after the data bit has been transmitted. The power reduction is discussed more in Chapter 4. The detailed schematics of the transmitter can be found in Appendix A. The size of the entire transmitter is 513μm^2. The layout of the transmitter can be found in figure A.14 in Appendix A.

3.1.1 Transmitter Operation

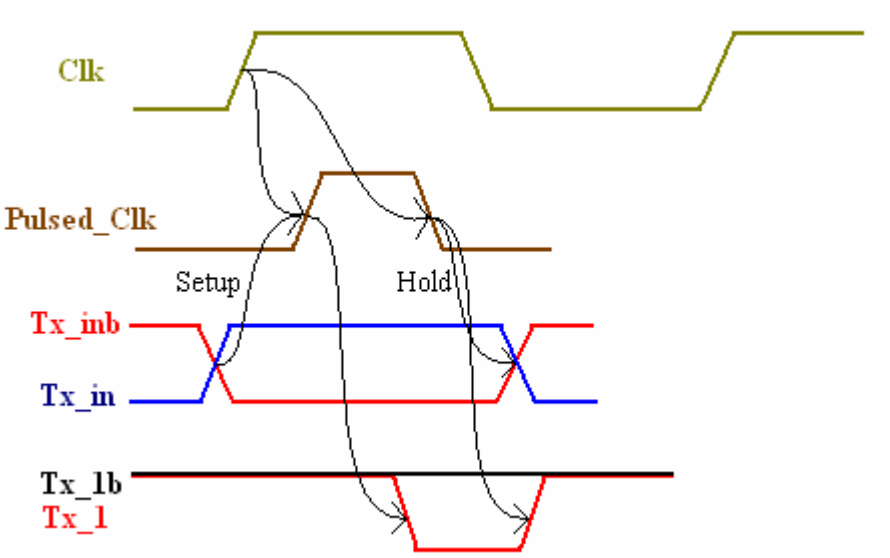

Figure 3.3 – Transmitter waveforms

Signal names in figure 3.3 correspond to the names in schematic in figure 3.1. The arrows drawn in the figure are the data and clock dependencies. When clock goes high it generates a pulse on the net Pulsed_clk. Tx_in and Tx_inb are the differential inputs. The setup of the Tx_in and Tx_inb is to the rising edge of the Pulsed_clk and hold is to the falling edge of the Pulsed_clk. This is a clock gater circuit. The setup and hold margins of the clock gater circuit are discussed in Chapter 4. When the Pulsed_Clk goes high, it pulls down either Tx_1 or Tx_1b depending on if you are transmitting a 0 or 1. This is the time where the transmission occurs. The Tx_1 and Tx_1b will be pulled high as soon as Pulsed_clk is pulled low. This allows the driver to turn off after data transmission to save power.

Figure 3.4 shows the current in the primary inductor and the voltage at the output of the secondary inductor. The current through the primary inductor is represented by I and p3 and p4 are the output ports for the transformer. When the current through the primary

inductor begins to change, a magnetic flux is generated which creates the first pulse at the output. Immediately after current reaches 4 mA, current begins to reduce back to 0; a magnetic flux in opposite direction is generated which results in the second pulse in the opposite direction. Thus second pulse is only seen when cutting off the current through a pulse. Data information is only in the first pulse and second pulse will be ignored at the receiver.

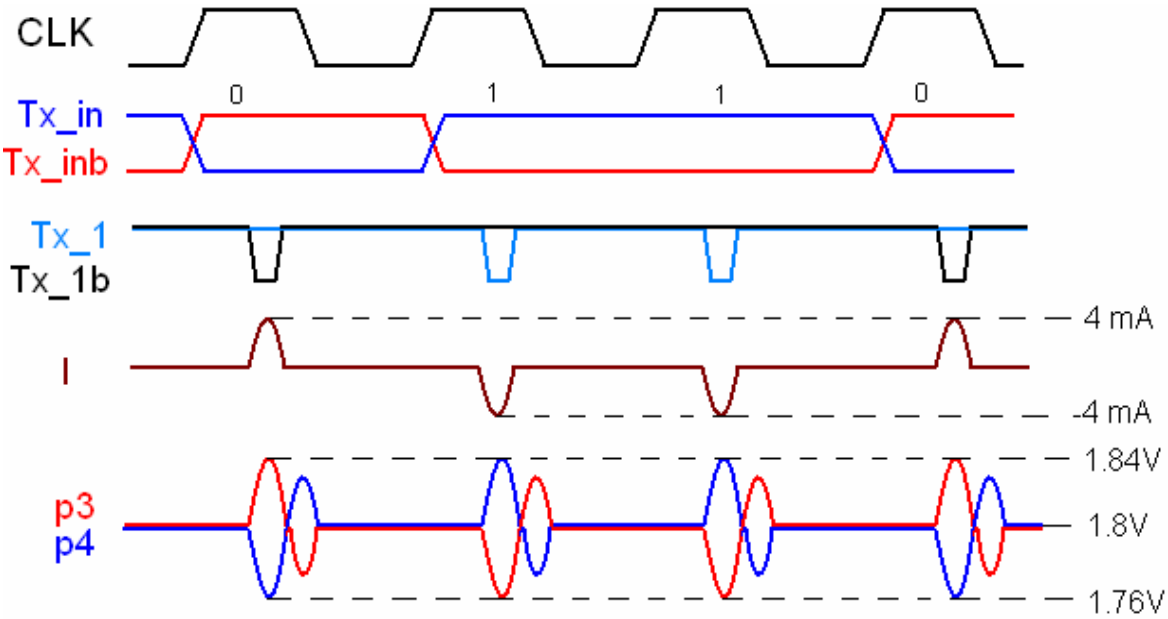

Figure 3.4 – Waveform at transmitter output

3.2 Receiver

The receiver receives the signal from the secondary inductor on the receiver side. The receiver consists of a sensing stage, amplifier stage and a flip-flop. The schematic of the receiver is shown in figure 3.5. The inputs to the receiver are pins in1 and in2. The output of the sensing stage amp_in1 and amp_in2 are amplified using a fully differential cascode amplifier. Since the incoming signal is not a NRZ signal, a Sense-amp Flip flop (SAFF) is

required to correctly detect the incoming data. Two buffers are used for the clock signal. First buffer is used to adjust the clock skew for varying process corners. The clock would arrive at earlier time during the FF corner and later during the SS corner. The second buffer is used to strengthen the clock signal going into large load in SAFF. The size of the entire receiver circuit is 620μm^2. The layout of the receiver can be found in figure A.15 in Appendix A.

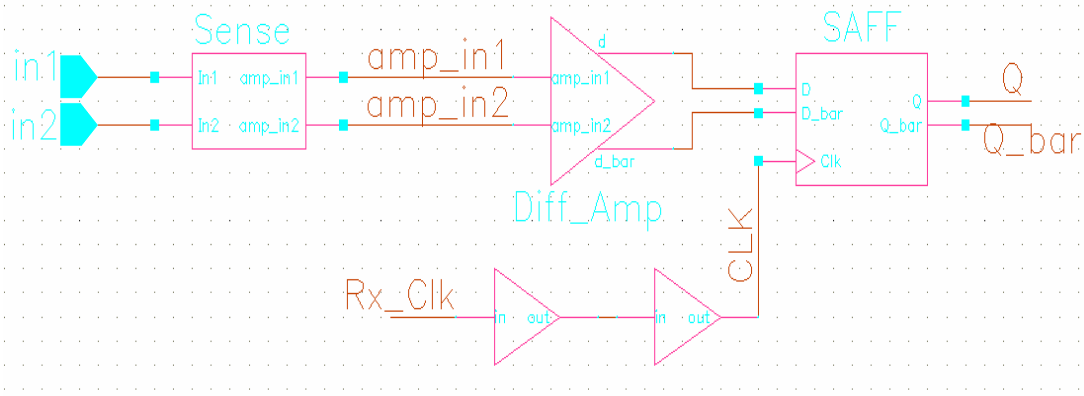

Figure 3.5 – Receiver Schematic

3.2.1 Sensing Stage

In the sensing stage shown in figure 3.6, inputs in1 and in2 are coupled with on-chip capacitors to block any DC components from the line. After coupling, these signals are adjusted to common mode voltage needed by the amplifier. The common mode voltage for the amplifier needs to be between 0.65V to 0.75V across all corners. The termination resistor is 50 Ohms and was designed in the layout. The signal v_pmos in figure 3.4 is the biasing PMOS voltage generated by the biasing circuit.

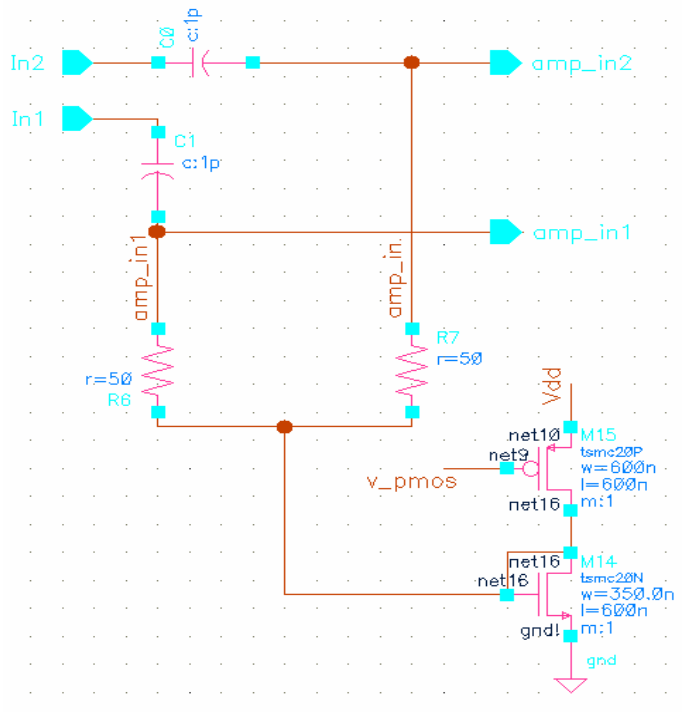

Figure 3.6 – Sensing Stage of the receiver

3.2.2 Differential Amplifier

The amplifier used for the receiver is a fully differential cascode amplifier. The schematic of the amplifier is shown in Figure 3.7. For detailed schematic refer to figure A.6 in Appendix A. This amplifier has been adopted from wideband CMOS transimpedance amplifier design which uses inductive peaking to extend the bandwidth and gain but the inductor is not needed in this amplifier because such high gain at high frequency was not needed [7]. Also the inductor is very spacious and would double the size of the amplifier. The reason for using a cascode design is to increase the bandwidth. The cascode transistor isolates the input output feedback resulting in increased bandwidth [8]. The resistors R1 and R2 are the load resistors. The transistors M5 and M6 connected in parallel with the load resistors act as a current bleeder to reduce the voltage drop across the load resistors [7]. The

common mode output needs to be at around 0.9V or higher for the next stage. Thus using a current bleeder would allow a high gain at a higher output voltage. The performance of the amplifier is discussed in details in Chapter 4.

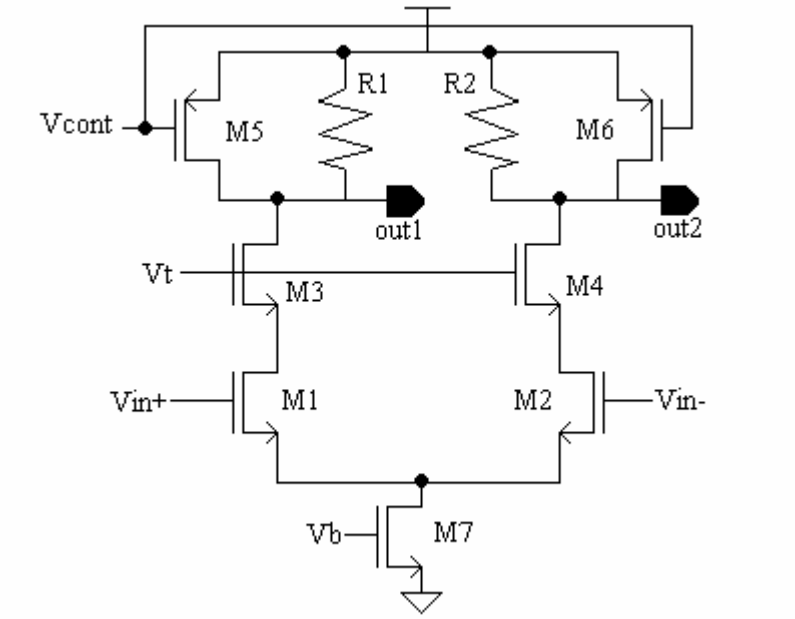

Figure 3.7 – Fully Differential Cascode Amplifier

3.2.3 Voltage Biasing

There are several bias voltages required for the amplifier and the sensing. The schematic used for the biasing is shown in figure 3.8 [8]. This is a self-biasing circuit. The output v_nmos and v_pmos are the biasing voltage for NMOS and PMOS respectively. The challenge in designing the bias circuit is to minimize the current through each line while maintaining the proper voltages.

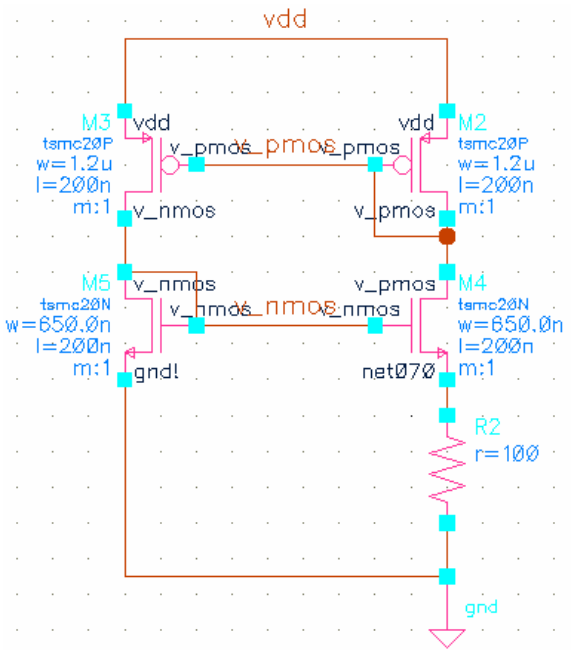

Figure 3.8 – Biasing Circuit

3.2.4 Sense-Amp Flip Flop

Incoming signal from the amplifier would have the magnitude of 200mV peak to peak differential. Thus a SAFF would be ideal to further amplify the signal in order to detect successfully. The schematic of the SAFF is shown in figure 3.9. The detailed schematic can be referred on figure A.7 in Appendix A. The first part of SAFF is the sense amplifier and the second is the R-S latch [9]. The incoming signal will have the common mode voltage of 0.9 or higher. This is required because a small change in input voltage has to be enough to trigger the change at output. Due to such high common mode voltage, transistor M7 and M8 needs to be strong enough to pull the R and S net high during precharge. Above 2 Gbps, there is less than 200ps that the circuit will be in evaluate phase. Thus it is necessary to pull the R or S net low as soon as clock goes high. It requires that the input change synchronizes with the

clock going high. The tail transistor M9 has to be large enough to boost the current through the line.

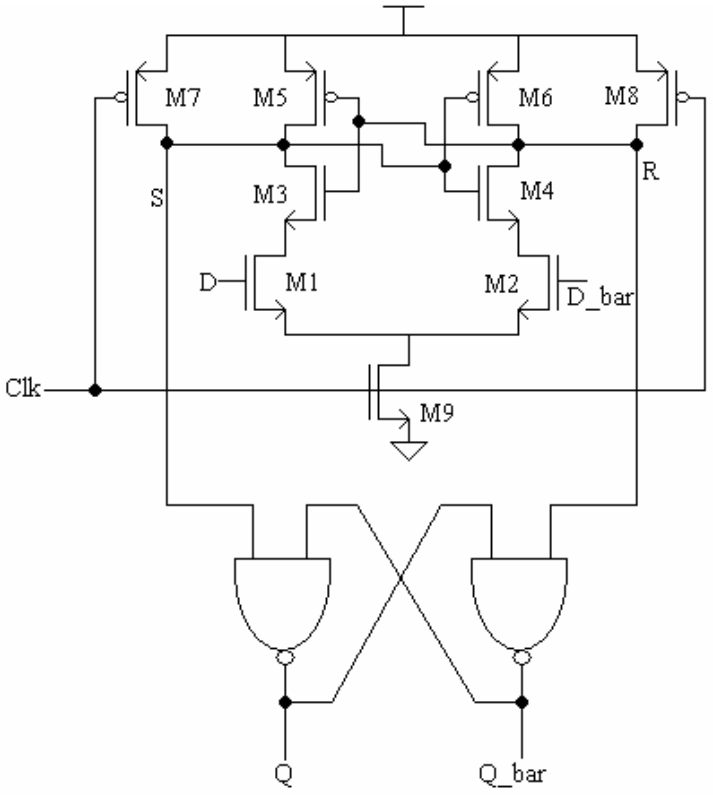

Figure 3.9 – SAFF schematic

3.2.5 Receiver Operations

The waveforms for the receiver operations are shown in figure 3.10. The net names correspond to the receiver schematic in figure 3.3. The signal amp_in1 and amp_in2 are the amplifier inputs. The input signal will contain multiple voltage pulses for a single data bit after going through two transformers. The amplitude of the first pulse is around 50mV to 60mV differential. The D and D_bar are the output of the amplifier that goes into the Sense-amp Flip-flop.

The first pulse of the data has to synchronize with the rising edge of the receiver clock that is connected to the SAFF. There is only a small time window that the first pulse of the input can occur for the receiver to detect the correct signal. If the first pulse changes before the valid window, then the output will change according to the second pulse. If the first pulse changes after the valid window, the input is too late causing the output to change for the tail of the previous bit. Either way, incorrect signal is detected. The valid clock skew that the receiver can operate over any condition is measured in the Chapter 4.

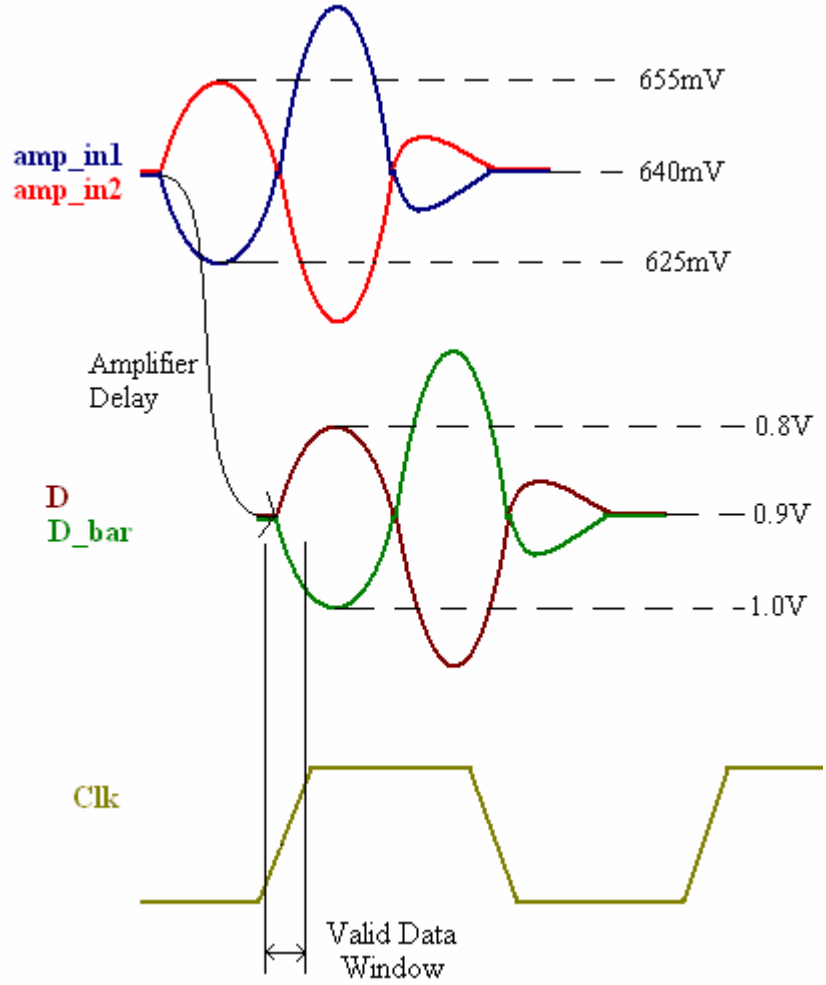

Figure 3.10 – Receiver waveforms

The use of SAFF can ignore the second and third pulses. During the first pulse in evaluate phase, the R or S nets of SAFF will be pulled low depending upon the input. When one of the nets is pulled low, it will not set again until the precharge phase which is at the rising edge of the next clock cycle. Thus when either R or S is pulled low, the second and third pulse has no effect on the output. It is very important to properly synchronize the clock with the first pulse.

4

Simulations

The circuit simulations were performed in Hspice and the transistor technology used in this thesis is the TSMC 0.18μm technology. The transformer simulation was done in HFSS and the RLC spice model was extracted and used in Hspice. The design is fully functional for all the process corners and the temperature variations from 0°C to 90°C. The power number and the projected BER are also presented in this chapter.

4.1 Transmitter

The transmitter was simulated at 2.5 Gbps for the worst case, slow-slow (SS) process corner at 90°C. The simulation was performed on the fully extracted model from the layout. Figure 4.1 shows the input clock at 2.5 GHz and the generated pulse. The maximum clock to Pulsed_Clk delay is 139ps. The worst case pulse width of the Pulsed_Clk is 128ps.

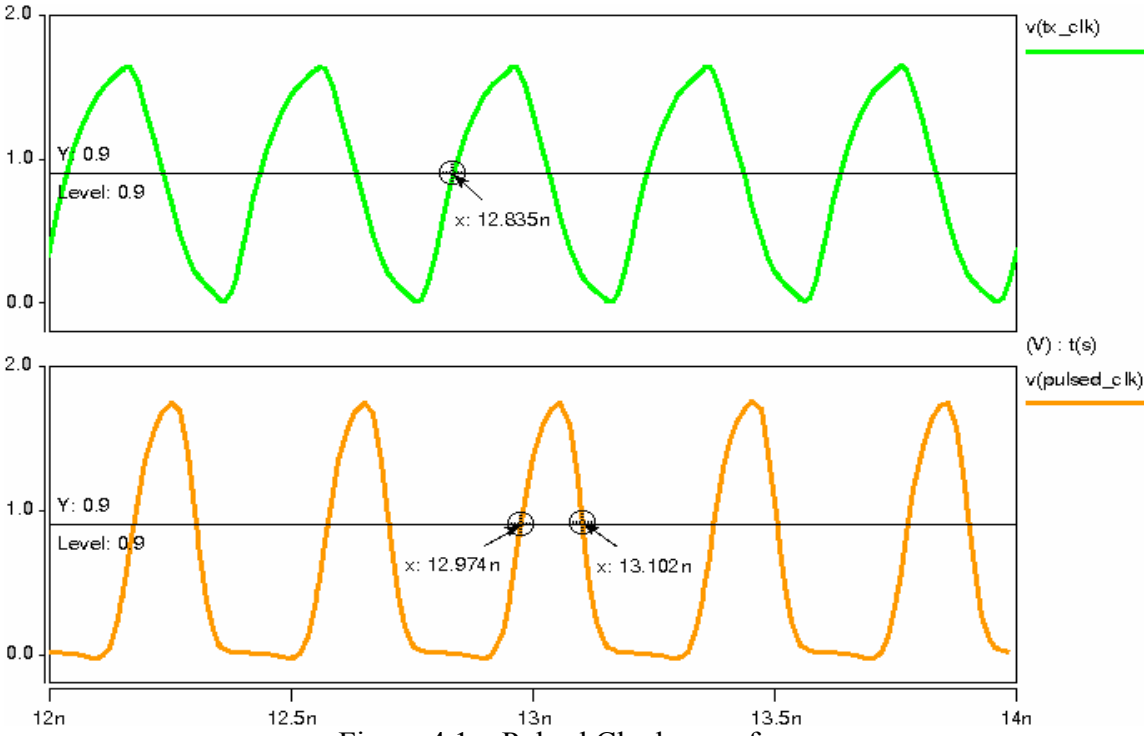

Figure 4.1 – Pulsed Clock waveform

The setup and hold time calculations for the inputs tx_in and tx_inb to the Pulsed_clk are shown in figure 4.2 and 4.3 respectively. The setup time is the latest time that the tx_in or tx_inb signal can change before the Pulsed_clk goes high. Adequate setup time is required to ensure a large enough current is induced in the primary inductor to produce a voltage pulse large enough to correctly detect the incoming signal. The setup time for the worst case operation is 19ps. The input data needs to hold past the falling edge of Pulsed_clk to prevent shorter pulses from transmitting. The hold time for the best case operation is 27.4ps.

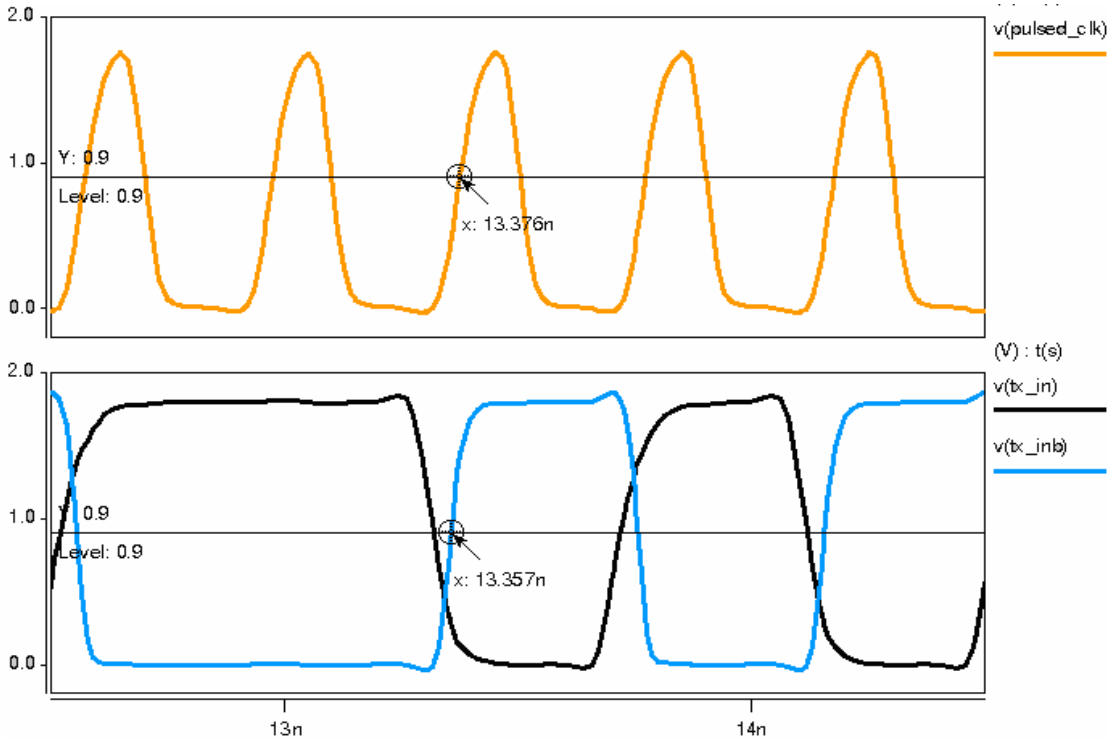

Figure 4.2 – Setup Time

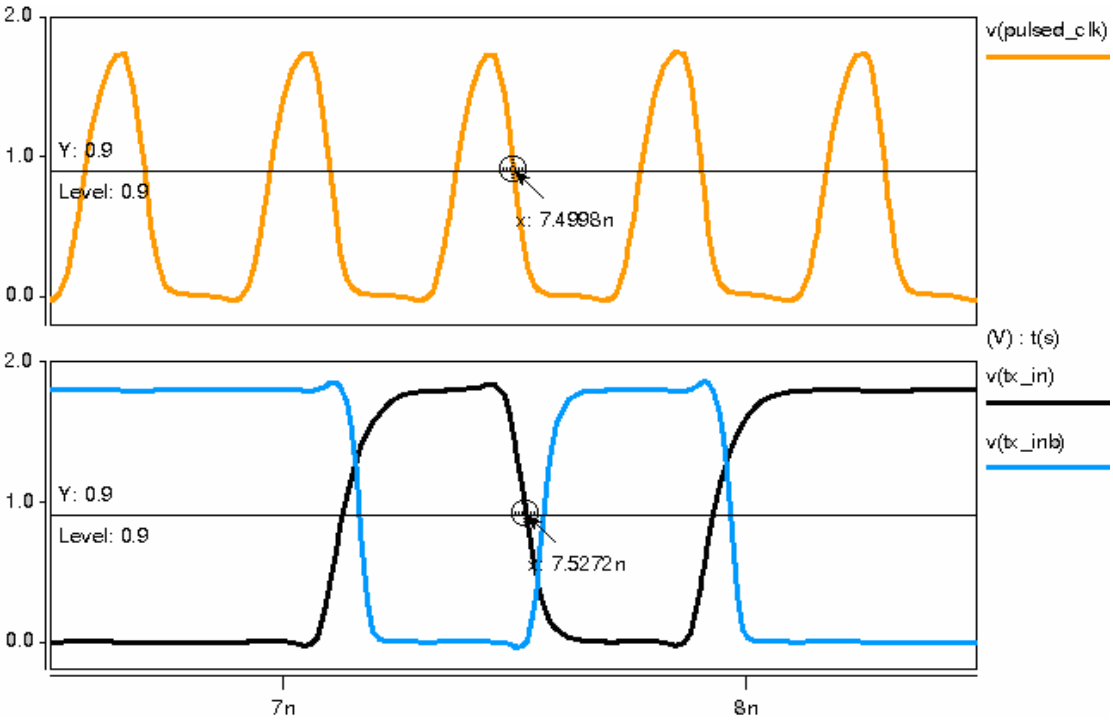

Figure 4.3 – Hold Time

The signal at the driver transistor of the transmitter is shown in figure 4.4. To transmit data bit 1, tx_1 net is pulled low while tx_1b remains high. This enables the current to flow in one direction. Inversely, to transmit 0, tx_1b is pulled low while tx_1 remains high to drive current in other direction. The current through the primary inductor is shown in figure 4.5. The current rises to about 2mA and shuts down immediately. Without using pulse, the power consumed by just the driver will exceed 3.6 mW, but when using pulse signaling driver only consumes around 0.8 mW.

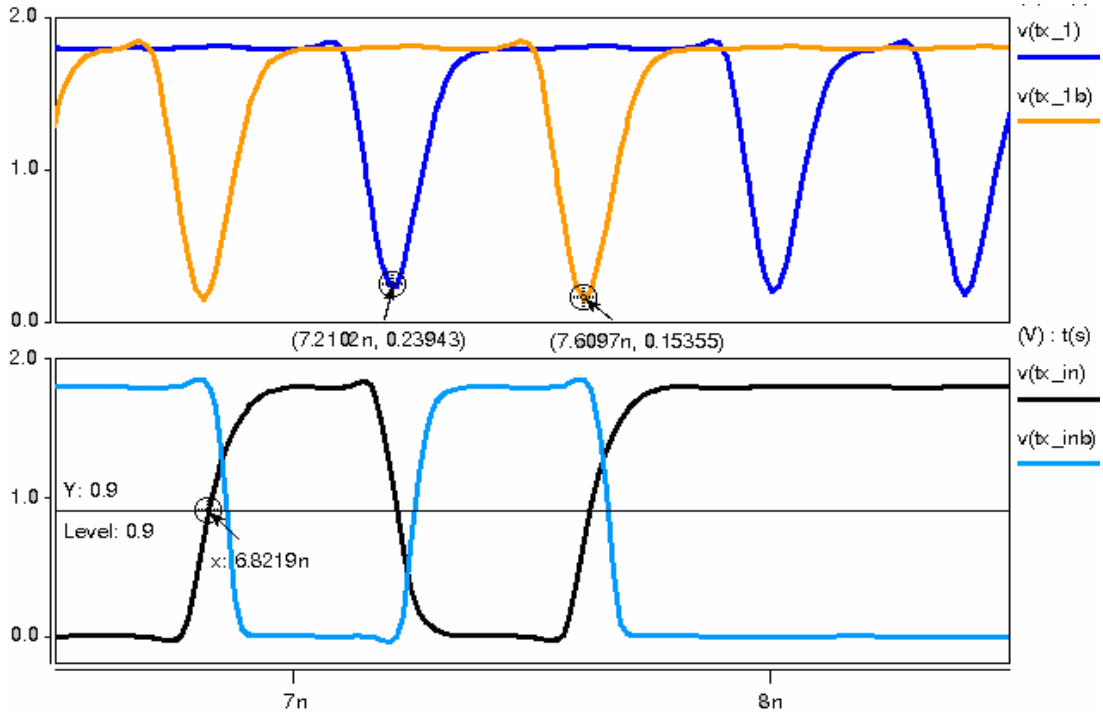

Figure 4.4 – Signal level at the driver

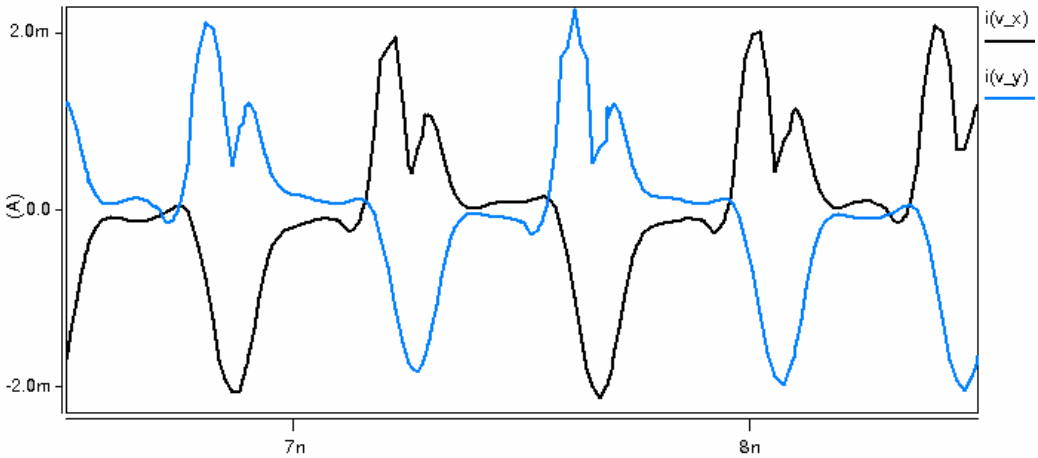

Figure 4.5 – Current in primary Inductor

4.2 Transformer

Figure 4.6 shows the signal on the transmission channel. Signal p3 and p4 are the output of the first transformer connected to the transmission line. Signal rx1 and rx2 are the signal at the end of the line connecting to the input of the receiving transformer and amp_in1 and amp_in2 are the inputs to the amplifier of the receiver. These signals are for SS corner at 90°C. The line is terminated to 1.8V Vdd with a 50Ohm load.

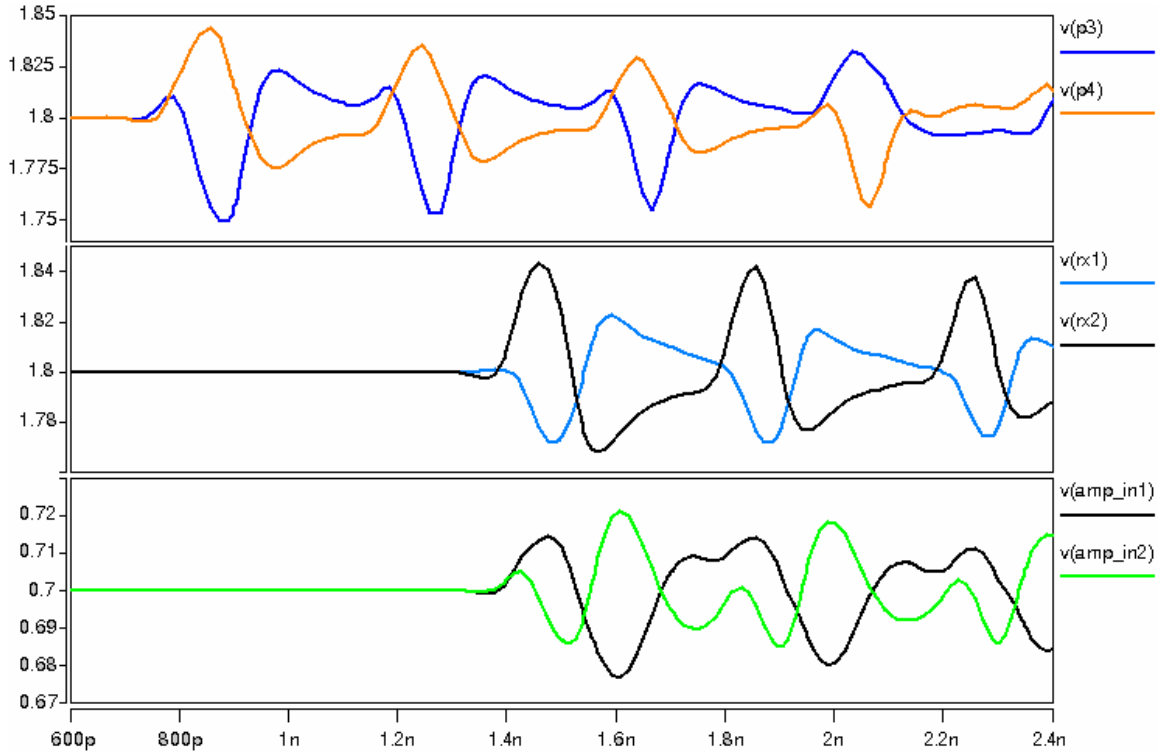

Figure 4.6 – Signal level on the channel

The differential eye diagrams for the SS corner at 90°C of these signals are shown in figure 4.7, 4.8, and 4.9. Figure 4.7 shows the eye diagram at the output of first transformer, 4.8 shows the eye diagram at the output of the transmission line and figure 4.9 shows the eye diagram at the amplifier input. The eye diagrams are generated for 2,500 pseudo-random data bits sequence using a vector file in Hspice. Maximum number of consecutive 0s or 1s is 7. The input vectors and clock signal are passed through minimum size buffer to make the data and clock non-ideal. The eye diagrams are measured by subtracting the two differential voltages at each point. Since there is no noise in the simulation, the eye diagram only contains deterministic jitter due to ISI and no random jitter. The horizontal and vertical eye openings of the first pulse are also shown in the figure. The signal at the input of amplifier of the receiver in figure 4.9 goes through two transformers resulting in three or more pulses.

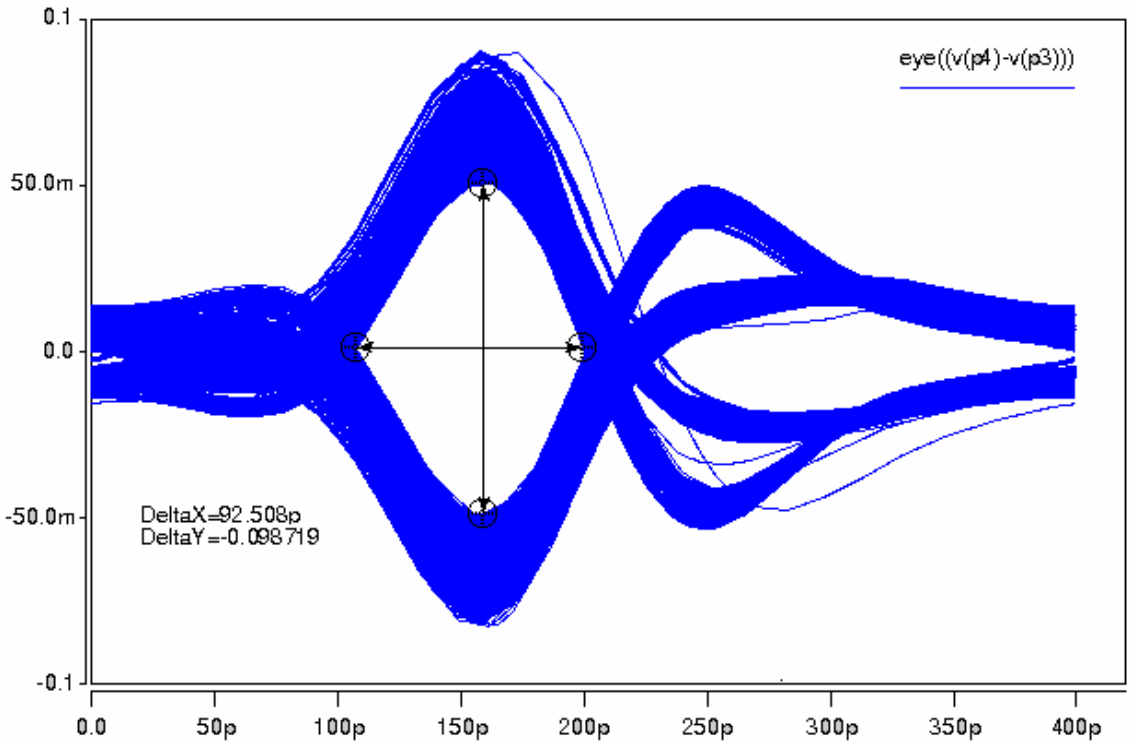

Figure 4.7 – Eye Diagram at output of first Transformer

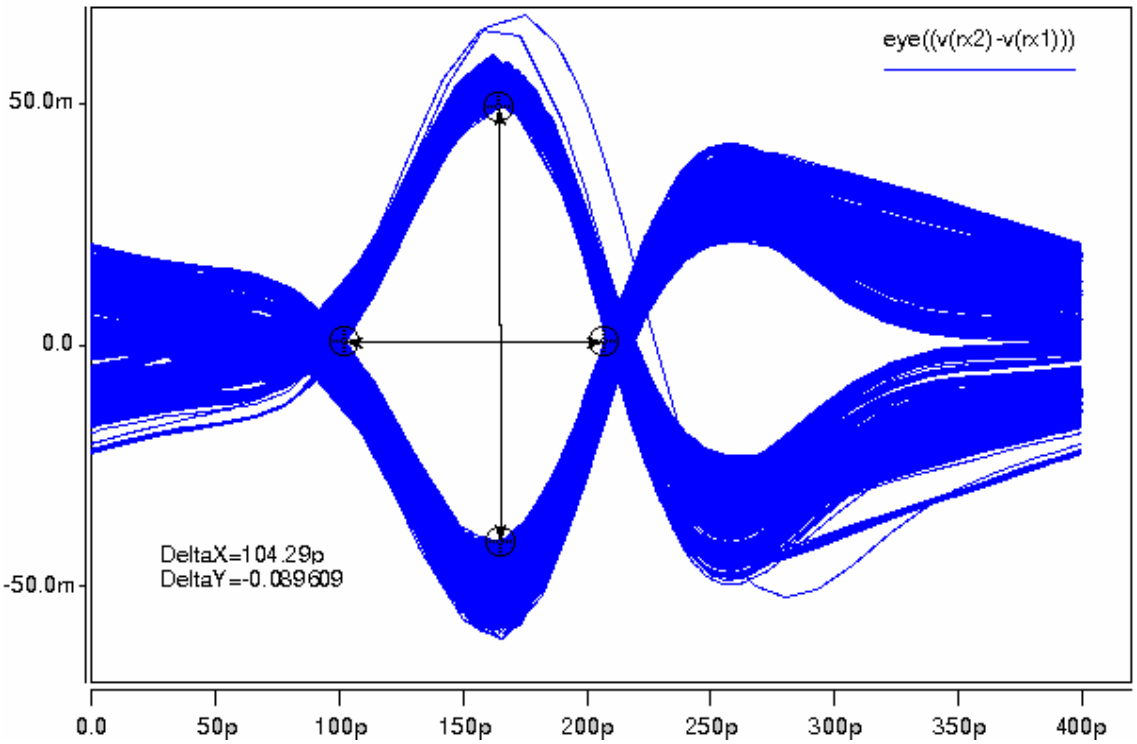

Figure 4.8 – Eye Diagram at output of Transmission line

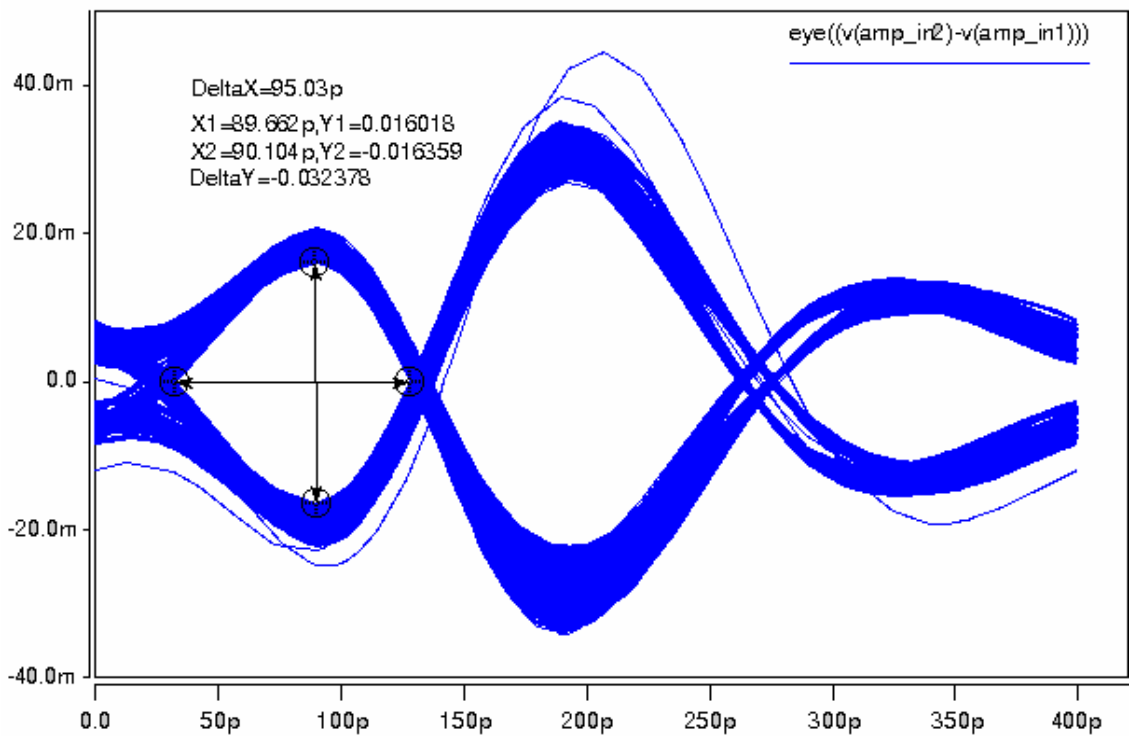

Figure 4.9 – Eye Diagram at the Receiver for SS corner

The eye opening at the amplifier input is 32.4mV peak to peak differential for the slow-slow corner at 90°C as seen in figure 4.9. Figure 4.10 shows the eye diagram at the input of the receiver for the nominal case at 25°C. This diagram is also generated using the same pattern. The eye opening for nominal case is 58mV peak to peak differential.

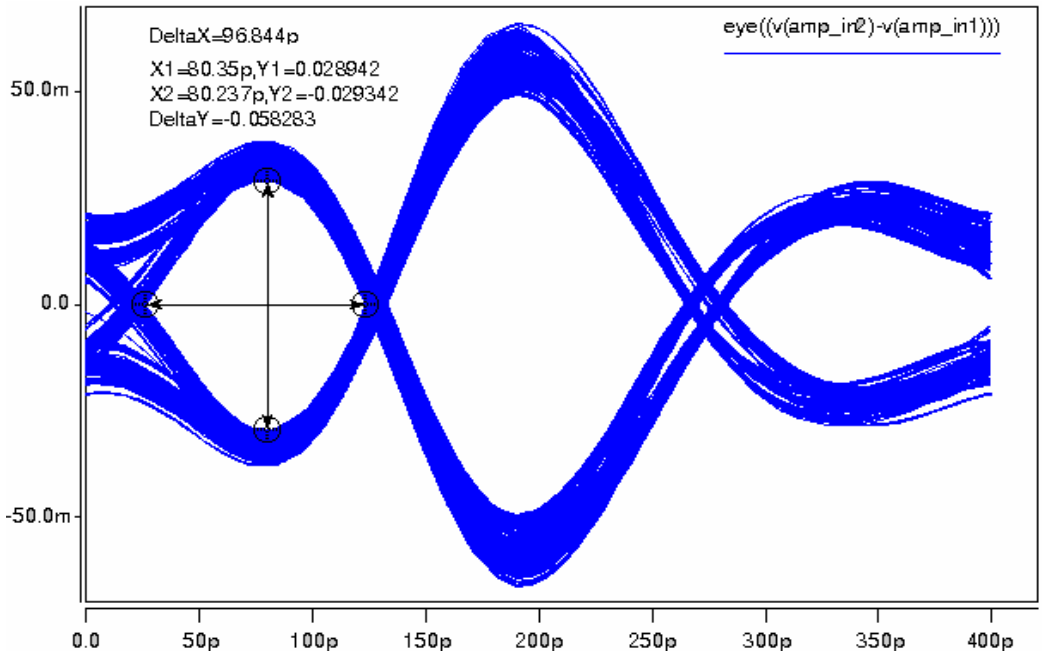

Figure 4.10 – Eye Diagram at Receiver for Nominal case

4.2.1 Transformer Crosstalk

The crosstalk noise on the victim transformer significantly reduces the amplitude of the signal. The effect of crosstalk was accounted for four surrounding transformer. Mutual capacitance and inductance are used from the values obtained from Q3D extractor. Figure 4.11 shows the inductor arrangement used in Hspice simulation. Cm1 is the mutual capacitance on the horizontal side and Cm2 is the mutual capacitance on the vertical side.

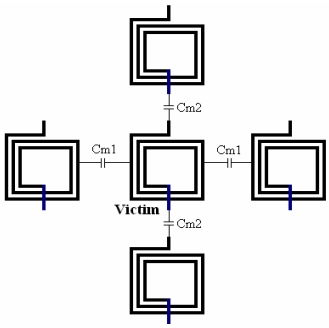

Figure 4.11 – Transformer crosstalk arrangement

The crosstalk noise is analyzed for the inductor spacing of 380µm in horizontal and vertical direction. Figure 4.12 shows the eye diagram at the output of first transformer going into the transmission line. The black trace is without any crosstalk and blue trace is with crosstalk. The eye opening reduces from 153mV to 117mV. The eye diagram at the input of the amplifier on receiver is shown in figure 4.13. At receiver, eye opening reduces from 59.5mV to 45.6mV. The impact of reduce eye on the receiver BER is discussed in the later section. These eye diagrams are generated for only 250 pseudo-random data bits.

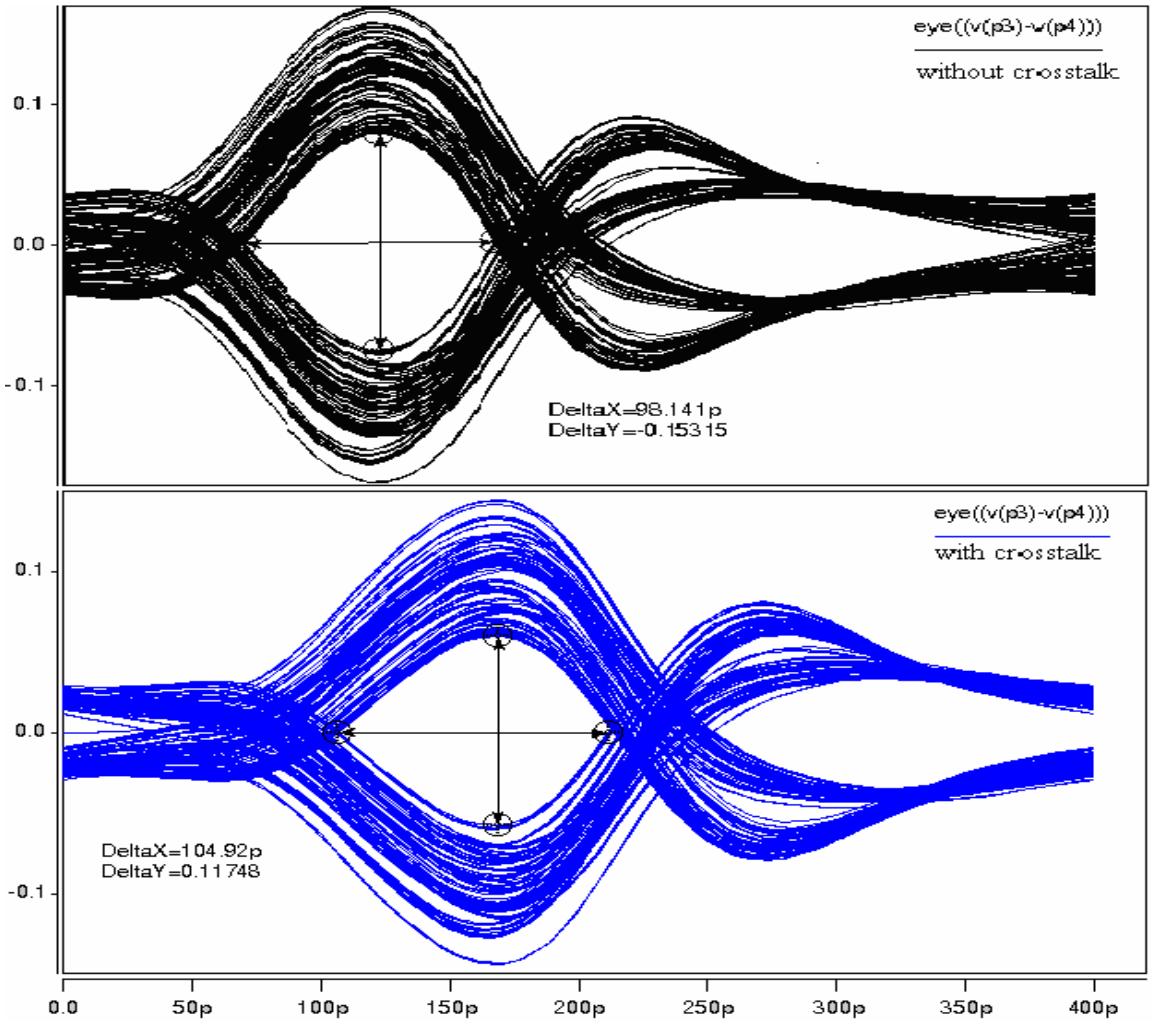

Figure 4.12 – Eye Diagram at output of first Transformer with crosstalk

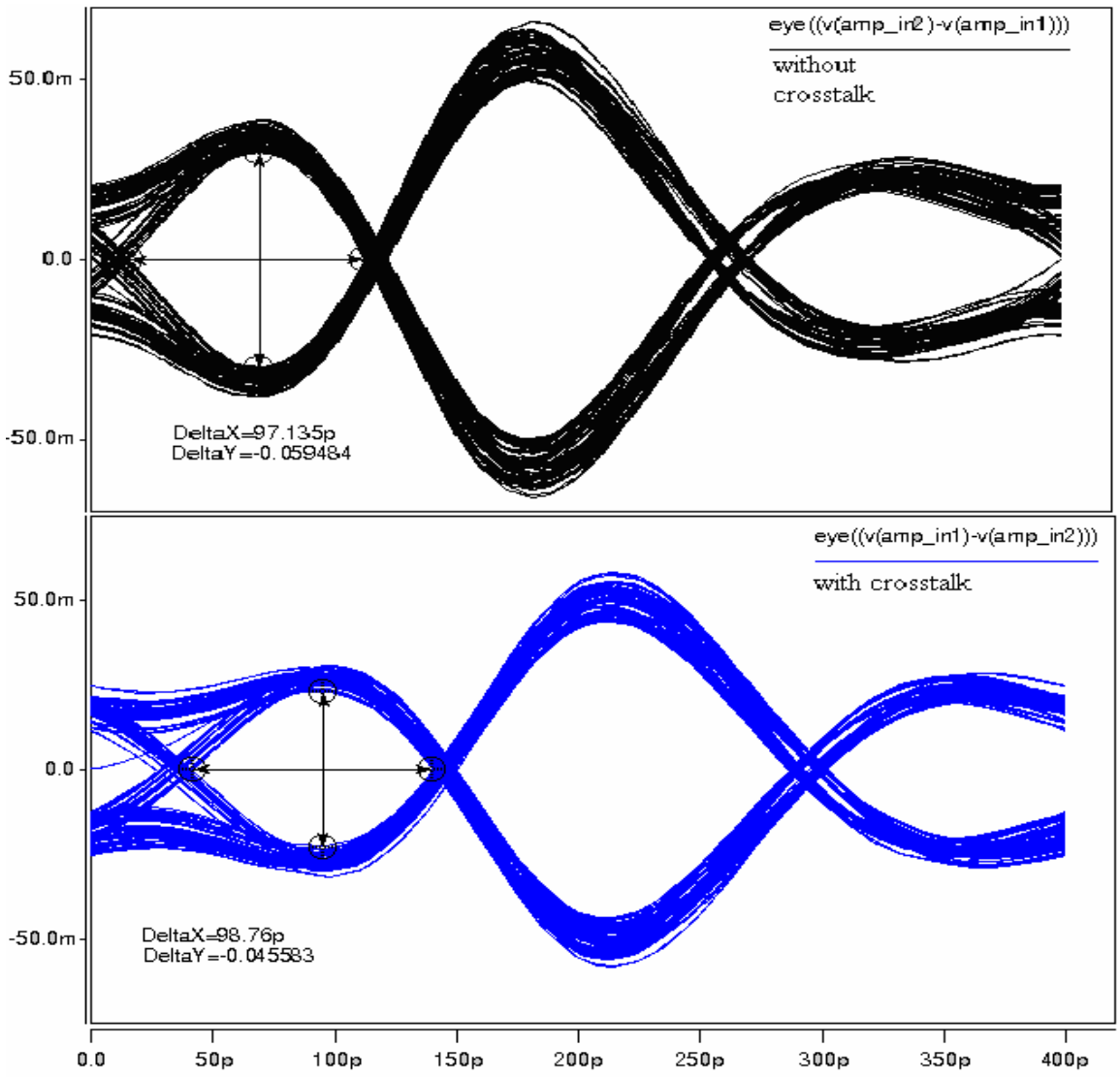

Figure 4.13 – Eye Diagram at input of Receiver

Figure 4.14 shows the response on a quiet victim line by keeping the middle transformer quiet and transmitting data on all four surrounding transformers. The top eye diagram in figure 4.14 is at the output of first transformer and bottom eye diagram is at the input of the amplifier. The maximum swing of the first pulse at the amplifier input is around 18mV peak to peak differential. The first pulse changes later in time as compare to figure 4.13 when transmitting data. Thus the output at the receiver will not change for such small

input swing. The minimum inductor distance required to keep victim line from changing is 380µm in both directions.

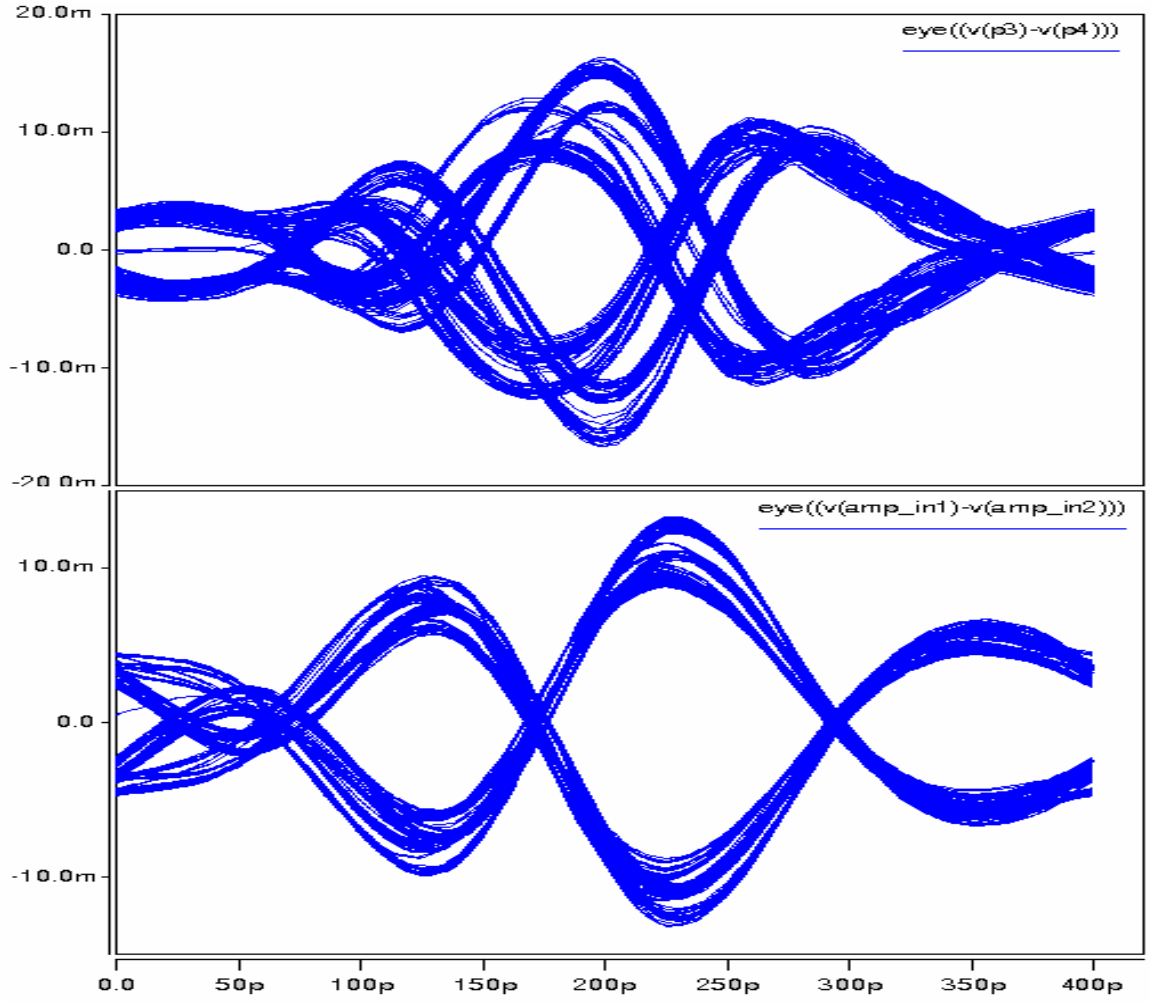

Figure 4.14 – Eye Diagram on quiet victim line

4.3 Receiver

4.3.1 Amplifier

Figure 4.15 shows the AC response of the amplifier with Sense-Amp Flip flop as the load. The low frequency gain on the line is 17.56 dB. The 3dB bandwidth of the amplifier is 1.7 GHz. Majority of the receiver input signal is between 2 GHz and 5 GHz. The gain at this

frequency is between 9dB and 13dB on each line. This limited gain is enough to correctly detect the signal by the SAFF. The transient response of the input and output signal of the amplifier is shown in figure 4.16. The input to the amplifier is amp_in1 and amp_in2 from the sensing stage and the output is the input to the SAFF. Since this is a negative gain amplifier, d is amp_in1 amplified and d_bar is amp_in2 amplified. Signals d and d_bar needs to have a high common mode voltage to trigger SAFF with very small change. The amplifier delay is around 120ps. The distortion in the d and d_bar signal is caused by the changing clock signal on the SAFF. This specifically occurs when the clock transitions from 0 to 1.

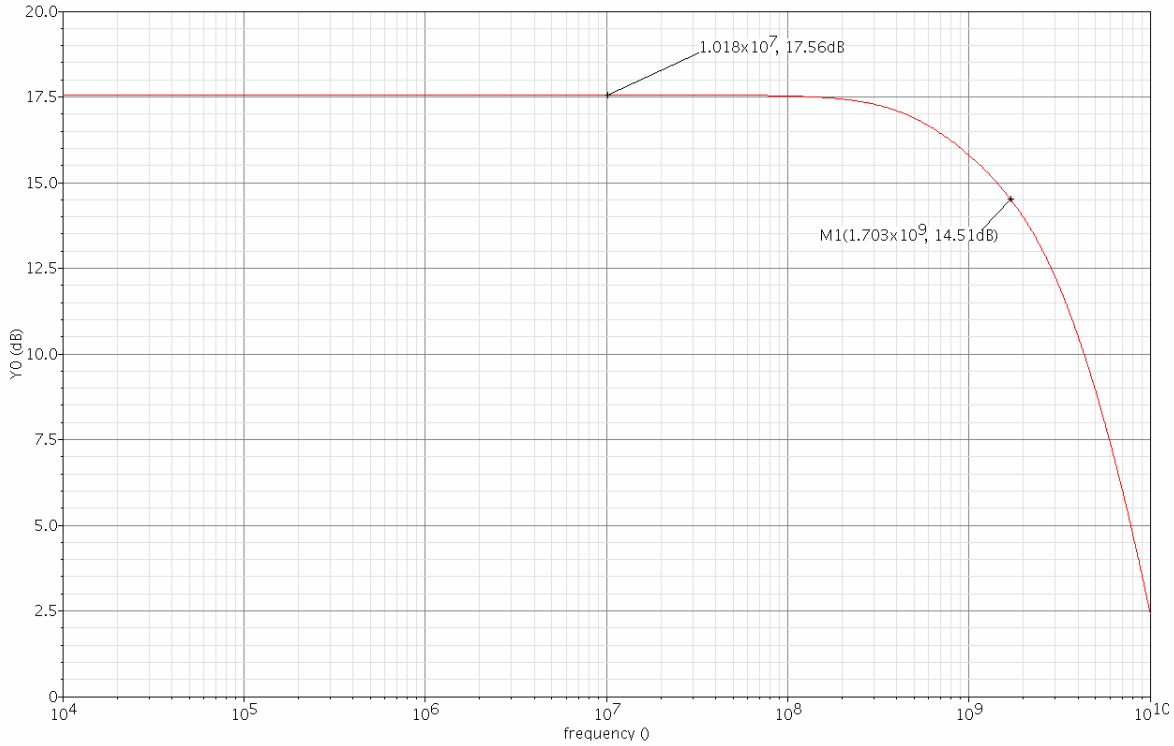

Figure 4.15 – AC response of the Differential amplifier

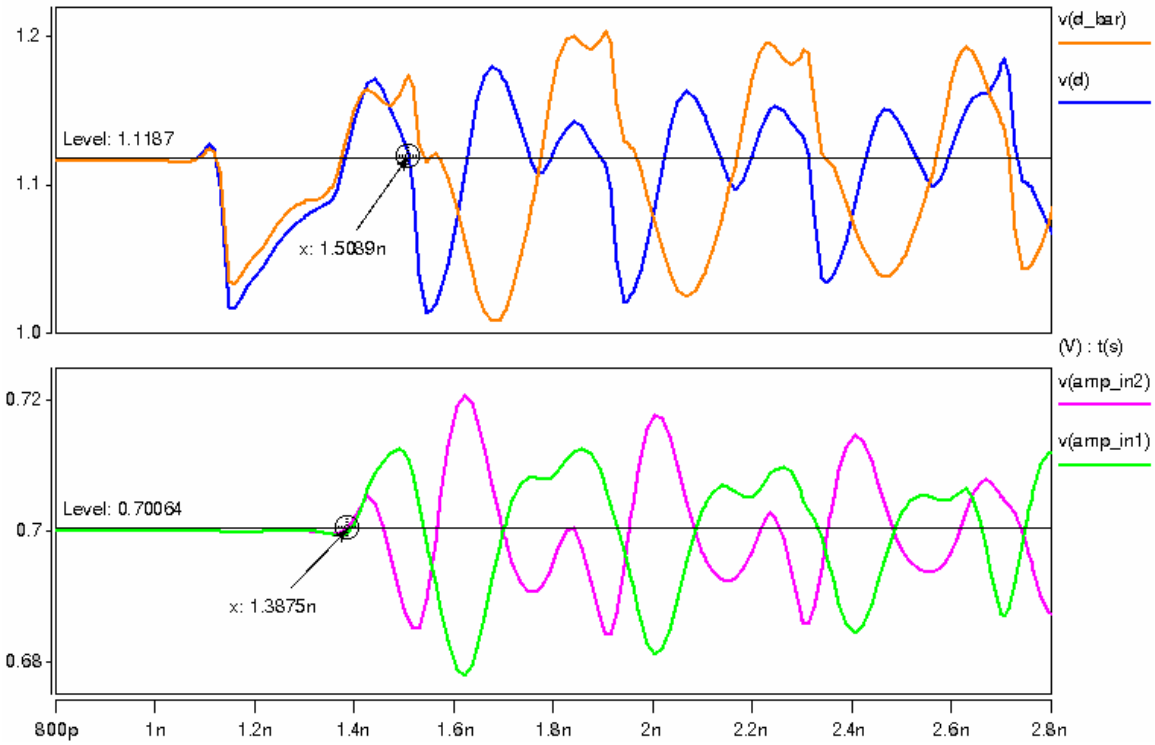

Figure 4.16 – Transient response of the amplifier

4.3.2 SAFF

The input data to the SAFF should change only when the clock is transitioning from 0 to 1. There is a limited time window in clock that would allow the input data to be correctly detected. Data coming earlier or later in the clock will not be correctly detected. The maximum clock jitter that the SAFF can handle in ensuring the correct data is 28ps for all corner cases. For each individual corner the valid window is much larger but when factoring in FF and SS corner, window size shrinks to 28ps. This is also valid for all temperature less than 90°C. Figure 4.17 shows the valid clock window that the receiver can handle. Q and Q_bar are the output and d and d_bar are the inputs of the SAFF. The outputs Q and Q_bar are loaded with a minimum sized inverter load. The skew at the output is only 18ps to 22ps

because the output is dependent on the clock and input and input arrives at the same time for both simulations. Figure 4.18 shows the eye diagram of output Q for the slow-slow corner at 90°C. Figure 4.19 shows the eye diagram for the nominal case at 25°C.

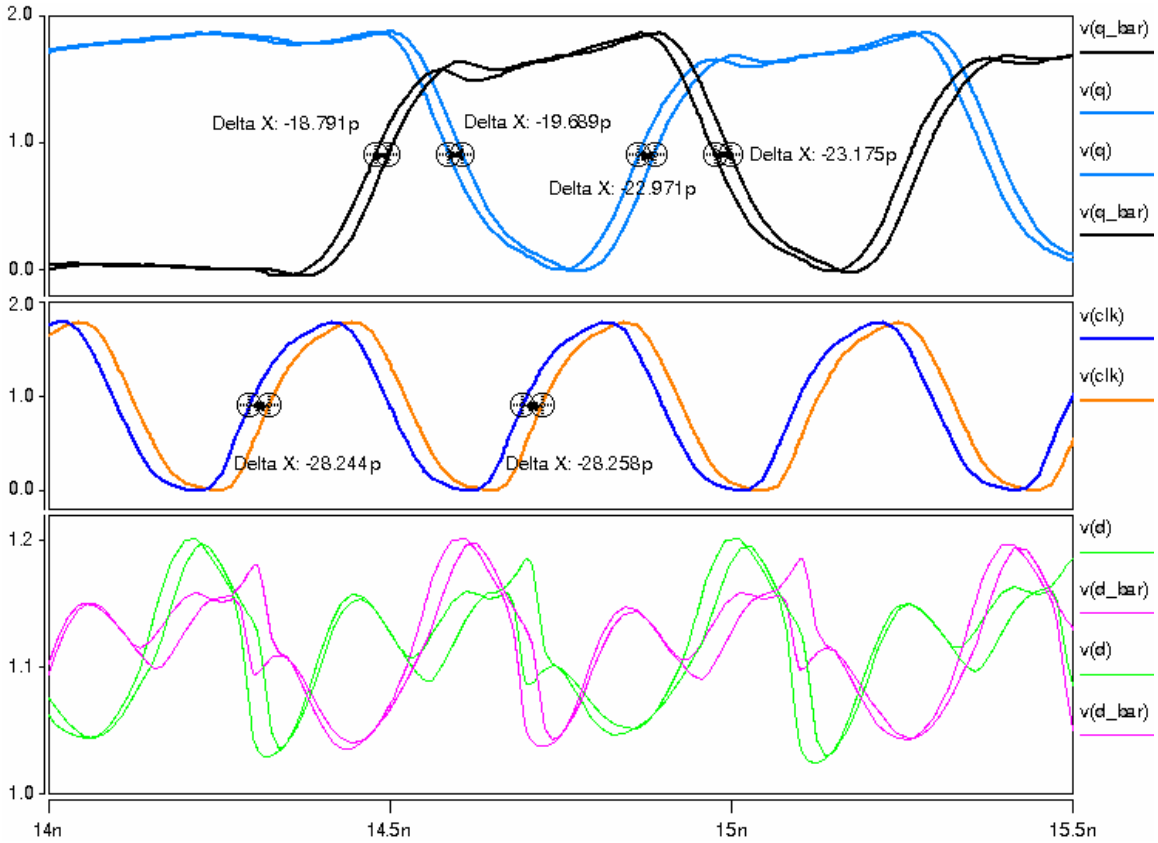

Figure 4.17 – Valid Clock window at receiver

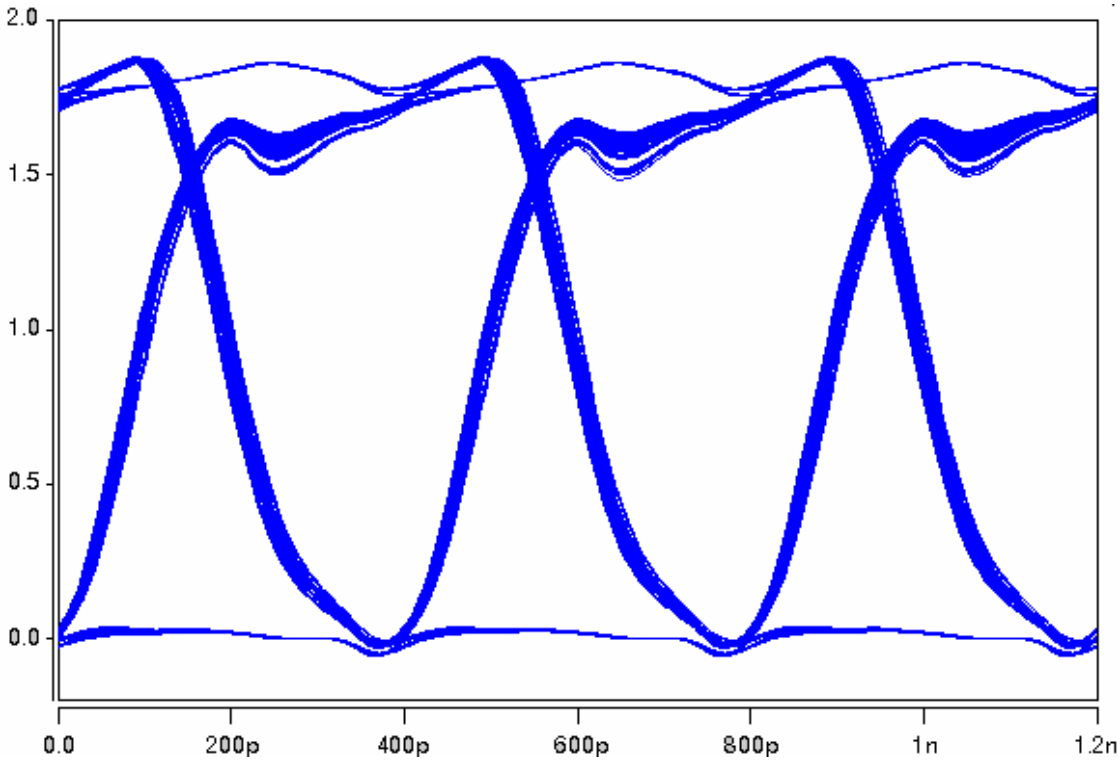

Figure 4.18 – Eye Diagram at the output for SS corner at 90°C

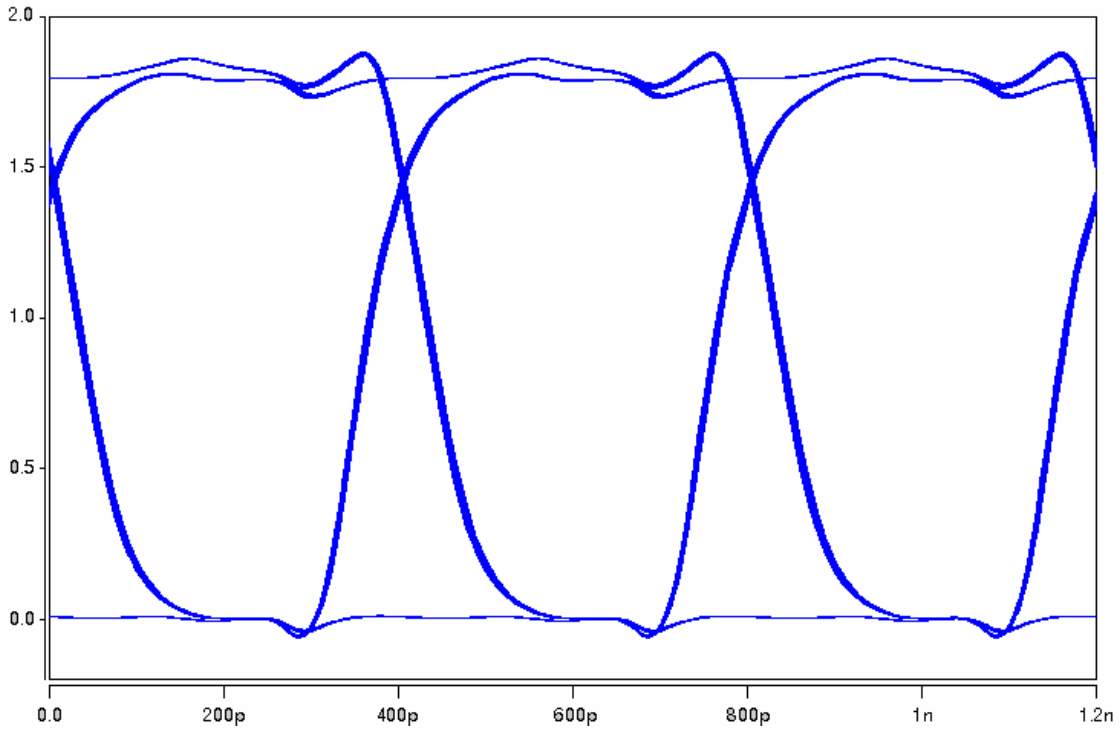

Figure 4.19 – Eye Diagram at the output for Nominal case

4.4 Power

One of the major goals of this research is to minimize power for high speed data transmission over other conventional designs. Using Inductively coupled interconnect blocks the unwanted DC power being transmitted. The power bandwidth of this work is around 2.21 $mW.Gb^{-1}.s^{-1}$. The transmitter only allows current flow during the short pulse. The pulse technique is very power efficient. In one of the previous work [12], the current flow through the primary inductor was for the entire duration of the bit, and the power consumption was 47.6 mW for 2.8Gbps data rate, which is around 17 $mW.Gb^{-1}.s^{-1}$. Table 4.1 shows the maximum power consumption for all the possible cases.

Table 4.1 – Power across corners and temperature

	0°C	**25°C**	**90°C**
Nominal (TT)	5.483 mW	5.526 mW	5.519 mW
Slow-slow (SS)	4.788 mW	4.694 mW	4.111 mW
Fast-fast (FF)	6.053 mW	6.167 mW	6.401 mW
Slow-fast (SF)	5.689 mW	5.718 mW	5.672 mW
Fast-slow (FS)	5.302 mW	5.353 mW	5.362 mW

For nominal case at 25°C the power consumption at 2.5Gbps is 5.526 mW. The transmitter power is 4.03 mW and the receiver power is 1.495 mW. Around 30-35% of the transmitter power is used by the driver current through the primary inductor.

Inductively coupled interconnect technique compares favorably over other designs in terms of power efficiency. Table 4.2 shows the comparison of this design versus capacitive coupled interconnect (CCI) [18] and other conventional design using physical connections [17]. The comparisons are in terms of power, bandwidth and technology. Both techniques in the comparison deals with chip-to-chip communications. The work in [1, 17] has comparable

power efficiency of this work but allows higher bandwidth. This can be due to using 90nm technology as compare to 180nm in this work. Transmitter power can easily be reduced by one half or more by scaling the technology. Smaller technology will shrink the current pulse width which reduces the time that the current flows through the inductor. In addition, the maximum current can also be reduce from 4 mA, because the current slew rate will be faster. This is because the voltage amplitude at the secondary inductor is dependent on rate of change in current through the inductor.

Table 4.2 – Power Comparison vs. other technique

	This work	**Ref [17]**	**Ref [18]**
Power bandwidth	2.21 $mW.Gb^{-1}.s^{-1}$	2.25 $mW.Gb^{-1}.s^{-1}$	5 $mW.Gb^{-1}.s^{-1}$
Bandwidth	2.5 Gbps	6.25 Gbps	3 Gbps
Process	0.18µm CMOS	90nm CMOS	0.18µm CMOS
Line Length	10 cm	9.5 cm	15 cm

Table 4.3 shows the comparison between this research and older inductively coupled interconnect work. The published result is only used for inter-chip communication such as in 3D-IC and does not transmit over transmission line [6]. The power bandwidth achieved in this research is lower and the bandwidth is higher. Both designs in the comparison use the pulse signaling to transmit data for only the fraction of unit interval. The inductor size used in this thesis is about a magnitude larger than the one used in [6]. This is due to maintaining a detectable signal level at the receiver after passing through two transformers and a transmission line. In another work [5], the power bandwidth is reduced to 0.14 $mW.Gb^{-1}.s^{-1}$ using precise pulse shaping. That technique was done in smaller technology and smaller pulses can be difficult with large inductor sizes

Table 4.3 – Power Comparison vs. older LCI technique.

	This work	Ref [6]
Power bandwidth	2.21 $mW.Gb^{-1}.s^{-1}$	3 $mW.Gb^{-1}.s^{-1}$
Bandwidth	2.5 Gbps	1 Gbps
Process	0.18µm CMOS	0.18µm CMOS

Figure 4.20 [1], shows the current trend in power consumption of a chip-to-chip communication line. Chip-to-chip power is reducing at the rate of 20% per year. In 2007, most of the system consumed 10 $mW.Gb^{-1}.s^{-1}$ to 20 $mW.Gb^{-1}.s^{-1}$ of power. Inductively coupling interconnect presented in this thesis requires around 2.21 $mW.Gb^{-1}.s^{-1}$.

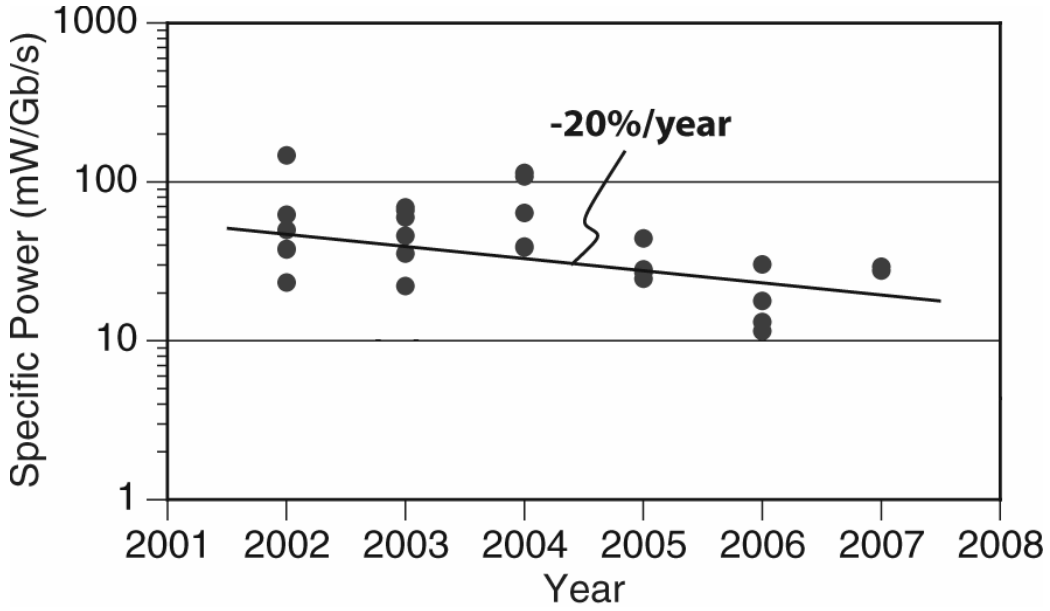

Figure 4.20 [1] – Current Trends in Transceiver power

4.5 BER calculations

The bit error rate of the system has to be calculated statistically from the channel response. The deterministic jitter (DJ) is primarily caused by the ISI of the data which can be determined from the simulation. Random jitter (RJ) is unbounded and can be represented by a Gaussian distribution function. Thus the total jitter (TJ) on a line is shown in equation 4.1.

$$TJ = DJ + RJ \quad [4.1]$$

The probability distribution function (PDF) of random jitter can be mathematically represented as given in equation 4.2 [13].

$$PDF_{random}(\Delta t) = \frac{1}{\sigma\sqrt{2\pi}} exp(-\frac{\Delta t^2}{2\sigma^2}) \quad [4.2]$$

In the equation above, σ represents the standard deviation of the distribution. The distribution of random jitter based on determinisitic jitter is shown in figure 4.21. A bell shaped curve is drawn at the end of negative and positive jitter. The standard deviation of random jitter in time domain is used to determine the BER.

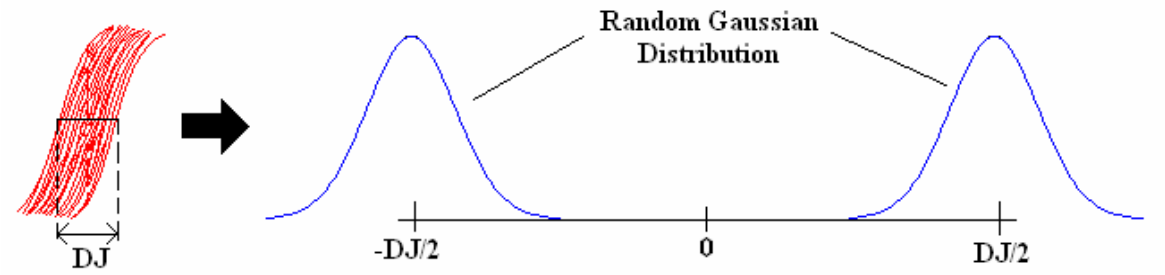

Figure 4.21 – Random Gaussian Distribution

For a given BER, to calculate the amount of random jitter, equation 4.3 is used [15]. The Q calculated is in relationship with standard deviation of random jitter. Table 4.4 shows some common BER values and the Q. To calculate BER of the system, minimum eye opening is calculated that is sufficient for the receiver to detect the correct output. After finding the minimum opening, you find the time difference between the minimum boundary edge and the edges of the deterministic jitter. Dividing this time by the standard deviation of random jitter will result in the Q in terms of standard deviation. To estimate BER, compare Q

with some common BER given in Table 4.4. Random jitter will also close the vertical opening of the eye, so that also needs to be monitored.

$$Q = \sqrt{2} * erf^{-1}(2 * (1 - BER) - 1) \quad [4.3]$$

Table 4.4 – BER versus Q

BER	Q
1e-11	6.7060σ
1e-12	7.0345σ
1e-13	7.3487σ
1e-14	7.6511σ
1e-15	7.9419σ

Calculating the BER for this system is little different than the conventional system. The data transmitted is not typical NRZ signal but multiple voltage pulses. Only the first pulse is required to detect the signal, and thus only eye of first pulse is required. Figure 4.22 shows the eye diagram at the end of the transmission line before the receiver transformer. The small triangle within the eye shows the minimum opening that the receiver can successfully detect the output. The minimum eye opening required by the receiver is 38ps by 68mV. The dimensions and the skew of the minimum opening triangle are derived by inputting set of pulses in the shape of ideal triangle at the receiver transformer and observing if the output at the SAFF of the receiver changed accordingly. Determining the exact size was done by trial and error before finding the minimum dimensions that will trigger the output. This can be verified by checking the output eye diagram with the added random jitter.

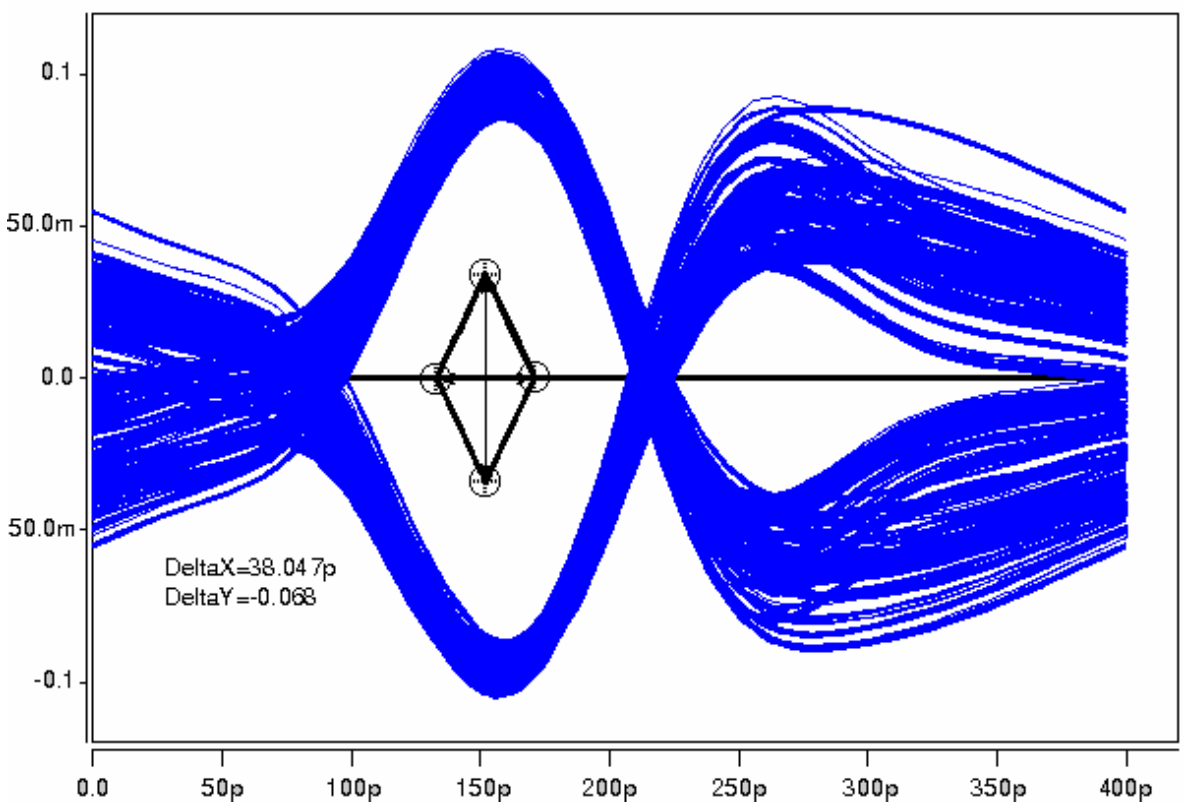

Figure 4.22 – Eye Diagram at the output of the Transmission line

Using the standard deviation of random jitter and knowing the amount of skew it will generate for a given BER, an eye diagram with the same skew is generated. Figure 4.23 shows the eye diagram with projected BER of 10^{-12} with 4.5ps of random jitter standard deviation. This plot was generated by manually inserting the skew into hspice simulator due to random jitter. The dark blue trace is the original eye without any random jitter and orange trace is the skew generated due to random jitter. The eye diagram passes the required minimum eye opening for the receiver. This system has BER of less than 10^{-12}. Additional random jitter would cause it to violate the minimum eye opening requirement.

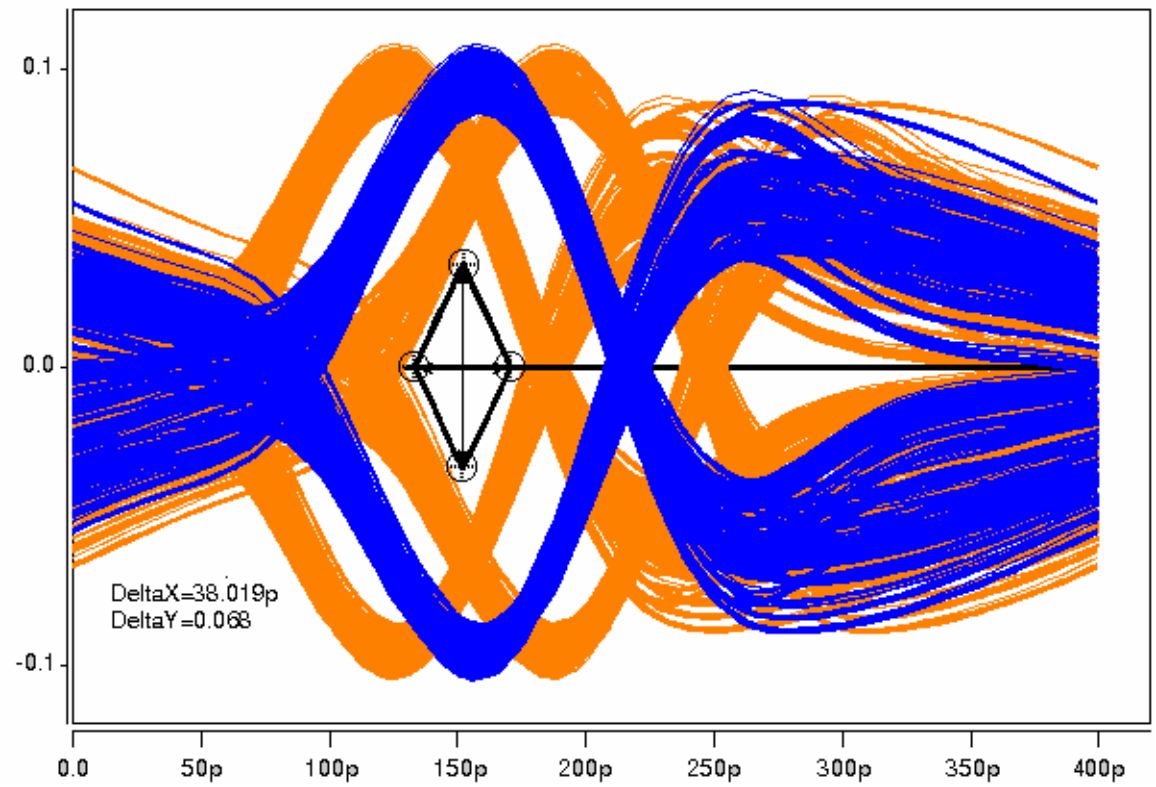

Figure 4.23 – Eye Diagram with projected random jitter

The bathtub plot of the system using the 4.5ps standard deviation of random jitter is shown in figure 4.24. The bathtub plot is generated in Matlab using the deterministic and random jitter. An estimate of deterministic jitter was extrapolated from the eye diagram and used in Matlab. The bathtub plot only considers the first pulse of signal. For BER of 10^{-12}, the bathtub opening is around 46ps. Comparing this with the eye opening in figure 4.23 shows roughly the same opening. For BER less than 10^{-12}, the margins would shrink and violate the minimum opening requirement. For Matlab code refer to Appendix B.

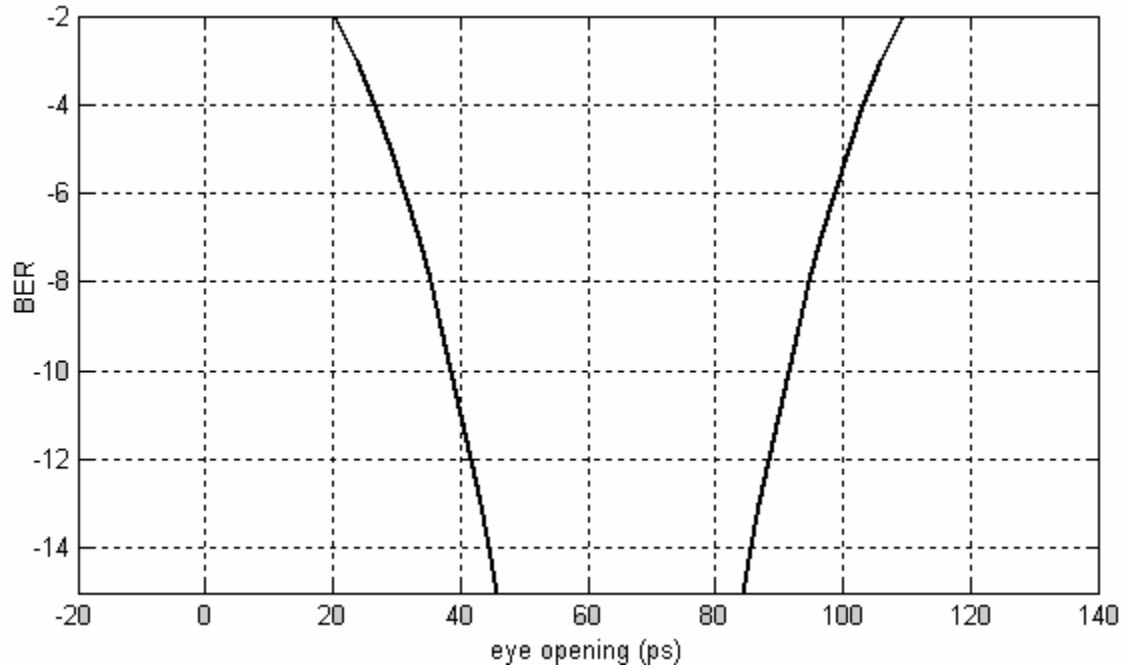

Figure 4.24 – Bathtub curve

The BER calculated in figure 4.22 is for nominal condition. For worst condition, with SS corner and temperature at 90°C, the BER increased to around 10^{-8}. The random jitter standard deviation remained the same for this simulation. Figure 4.25 shows the eye diagram at the end of the transmission line before the second transformer. The amplitude has shrunk increasing the BER. Figure 4.26 shows the eye diagram at the output. The blue trace is without any random jitter and green trace is due to random jitter. Added noise for the worst case will introduce some glitch at the output.

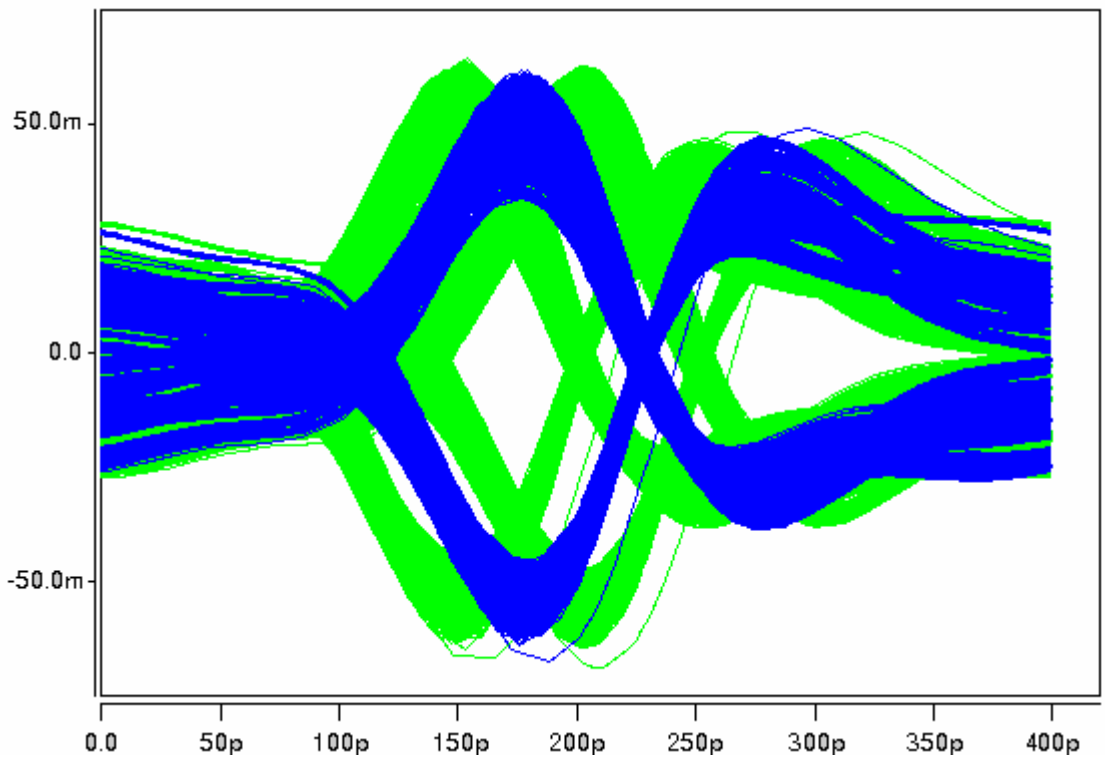

Figure 4.25 – Eye diagram for worst case

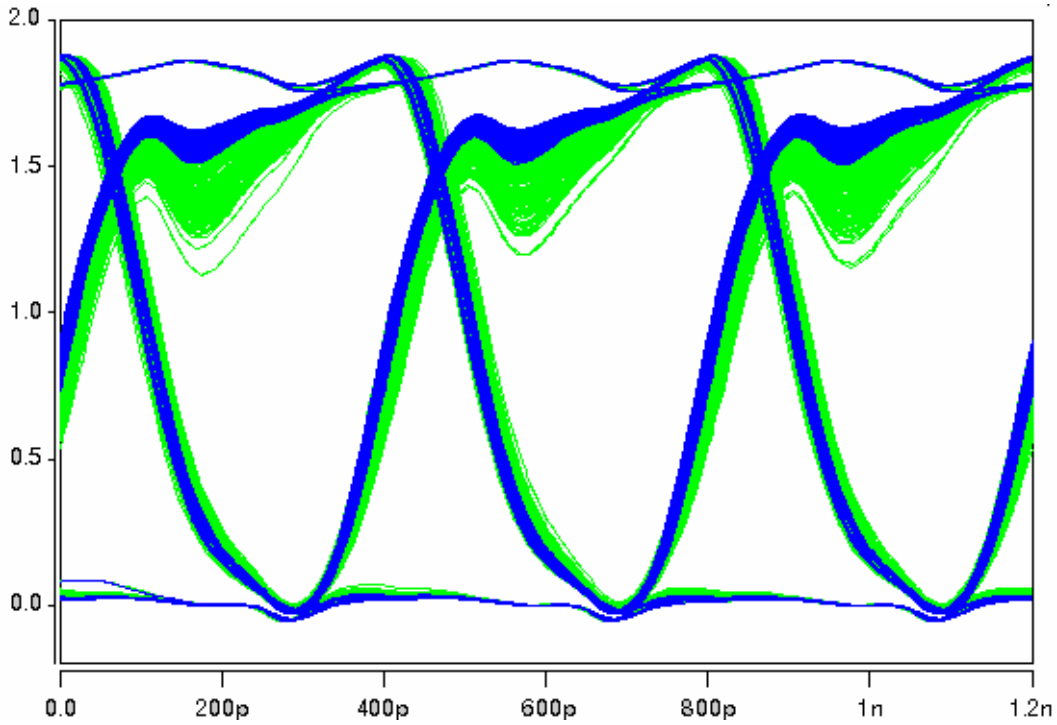

Figure 4.26 – Output Eye Diagram for worst case

4.5.1 BER with crosstalk

With reduce amplitude at the output of the transformer due to crosstalk, it is necessary to find the minimum inductor spacing that will maintain the BER of less than 10^{-12}. Using the transformer arrangement as shown earlier in figure 4.11, it is found that the minimum inductor spacing on either side needs to be a minimum of 380μm to maintain BER of less than 10^{-12}. Figure 4.27 shows the eye diagram generated in Hspice by inserting random jitter manually. The entire eye clears the minimum required area. Comparing this eye diagram with the one in figure 4.23 without any crosstalk noise shows a decrease in amplitude. Blue trace is the without any added random jitter and green trace is skew due to random jitter. The output eye diagram is shown in figure 4.28. The output skew is 63ps. This eye diagram is generated for 250 pseudo-random data bits.

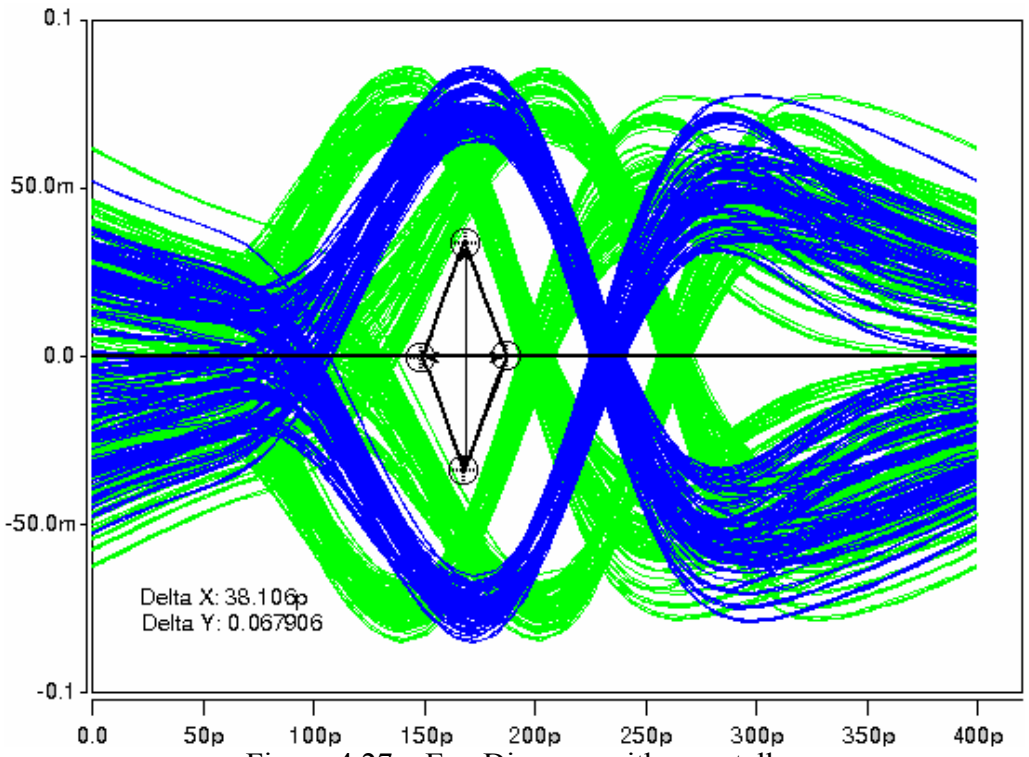

Figure 4.27 – Eye Diagram with crosstalk

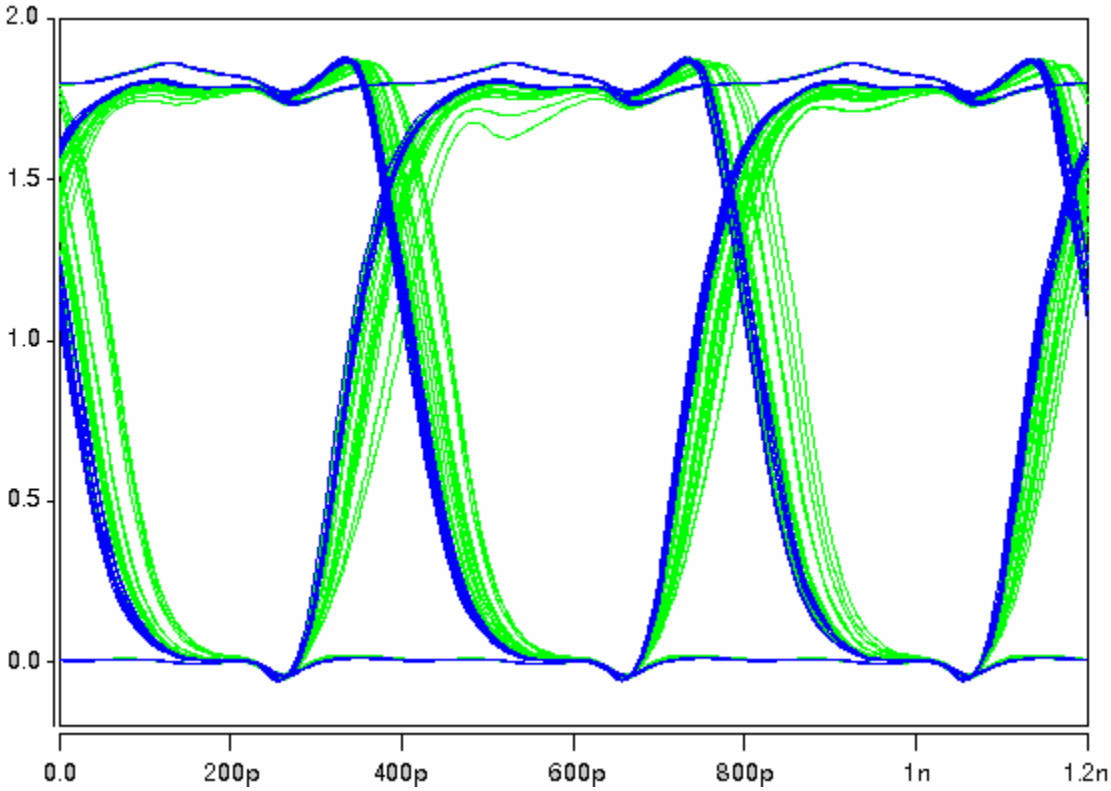

Figure 4.25 – Eye Diagram at the output

5

Conclusion and Future Work

This thesis presents a technique of using inductive coupling interconnect for chip to chip communication over transmission line. Most of the transceiver design has been adapted from previous works but is implemented to work over a transmission line. The major benefit of using inductive coupling over physically connected system is reduced power which is proved in the simulation chapter. This design achieved the power bandwidth of 2.21 $mW.Gb^{-1}.s^{-1}$ for a 2.5Gbps data rate on a 0.18μm TSMC technology, which is better than other inductively coupled interconnect circuits. Most of the previous LCI designs have only worked where the data has to go through only one transformer where as in this design the data could be transmitted across multiple transformers and a transmission line. The transmitter and receiver can be designed without increasing much circuit complexity. The projected BER is less than 10^{-12} which is in line with most of the digital systems. Similar BER can also be achieved when there are multiple transformers in the vicinity transmitting simultaneously. The circuit meets all the industry standard corners and temperatures.

5.1 Future Work

As all the work done in this thesis is simulation based, next step would be to put this transceiver on an actual chip and compare it with simulation results. The chip and the board will also need inductors to form the transformer.

This design works flawlessly for 2.5Gbps for all corners and temperature. This work could be extended to operate beyond 3Gbps using smaller CMOS technology. Another problem beyond 3.5Gbps is the increased ISI from multiple pulses due to shortened unit interval. Some circuit technique needs to be researched that will remove multiple pulses after the first pulse, since data information is only in the first pulse.

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APPENDIX

APPENDIX A

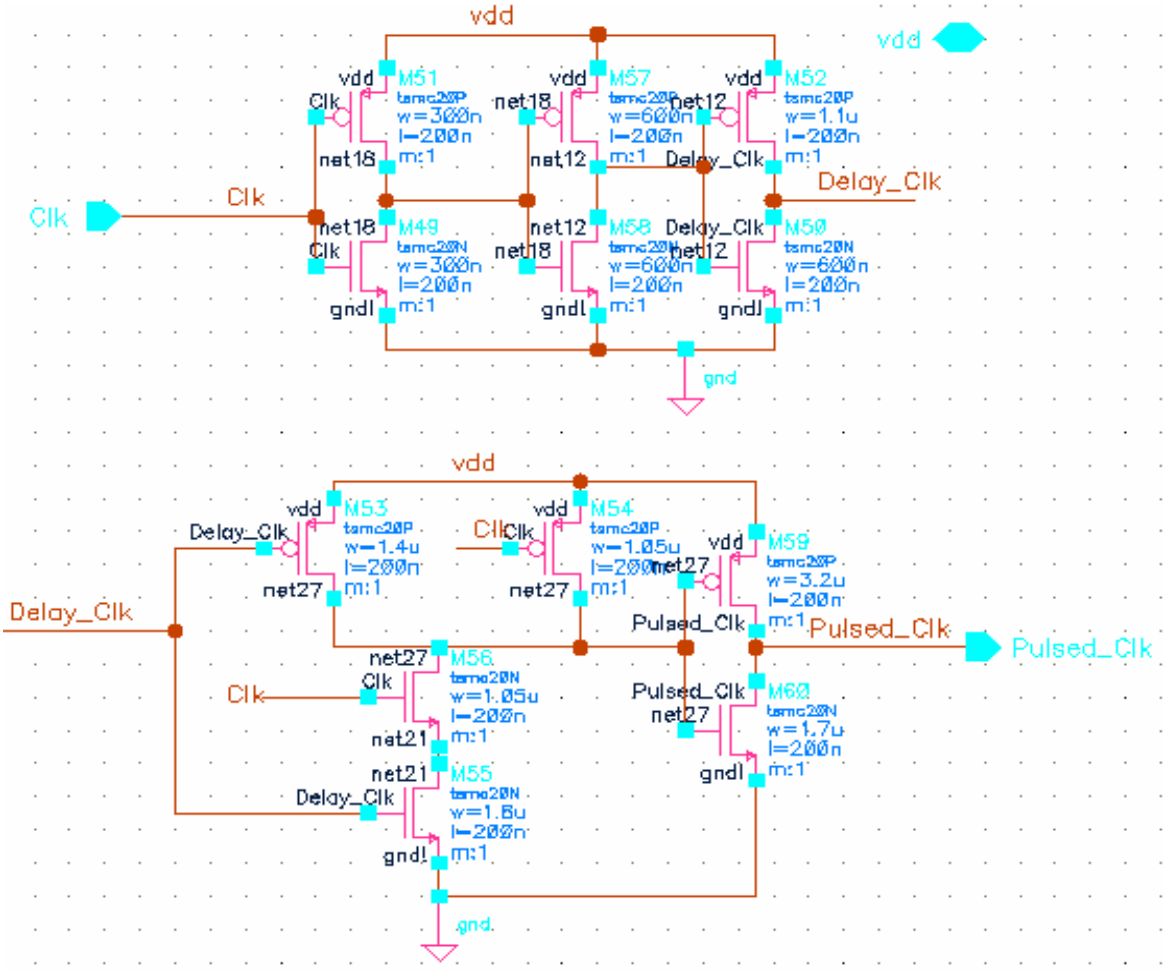

Figure A.1 – Pulse Generator Schematic

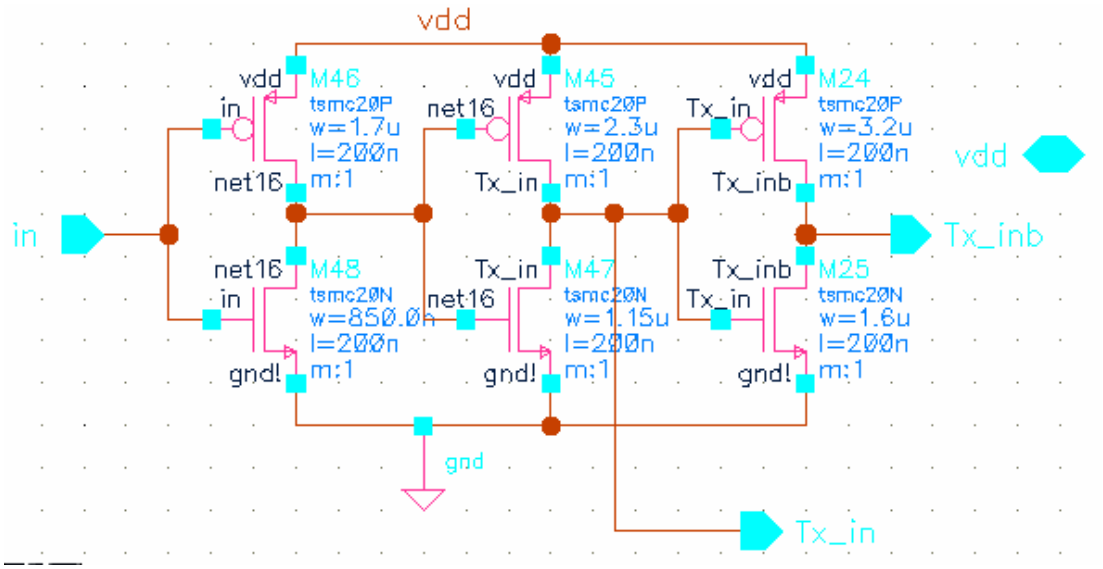

Figure A.2 – Schematic of Input Buffer

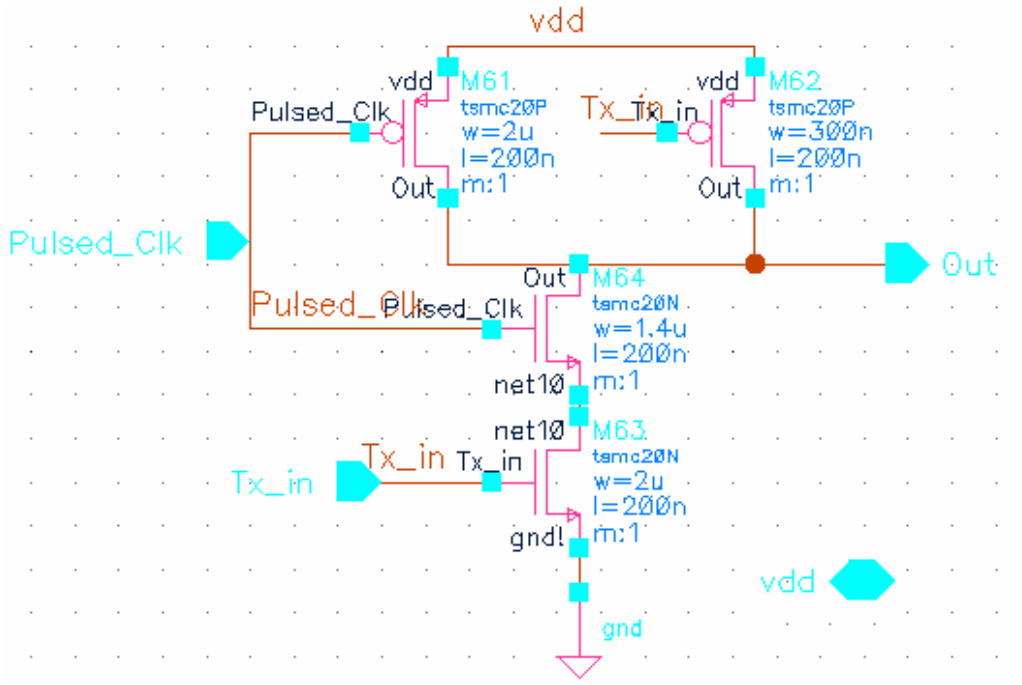

Figure A.3 – Schematic of NAND gate

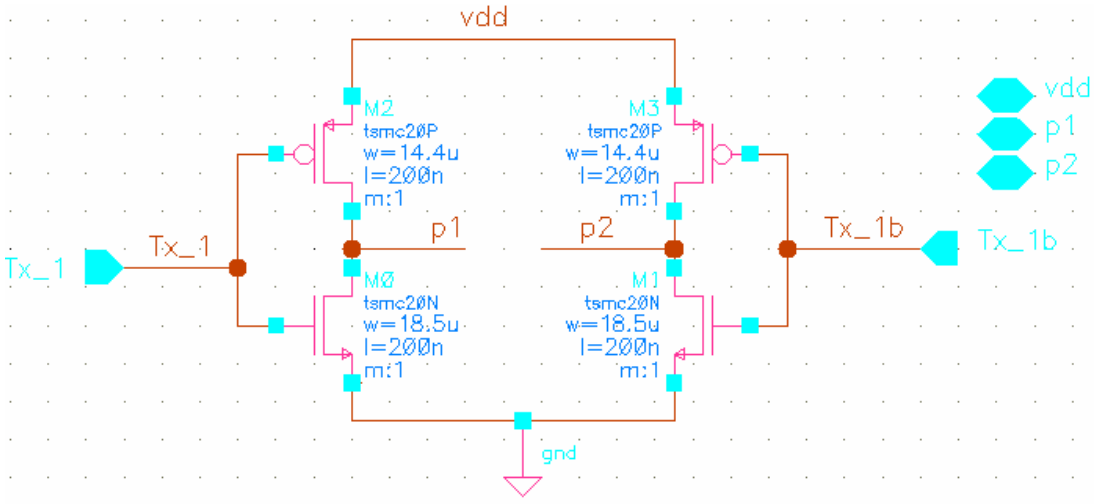

Figure A.4 – Schematic of Driver

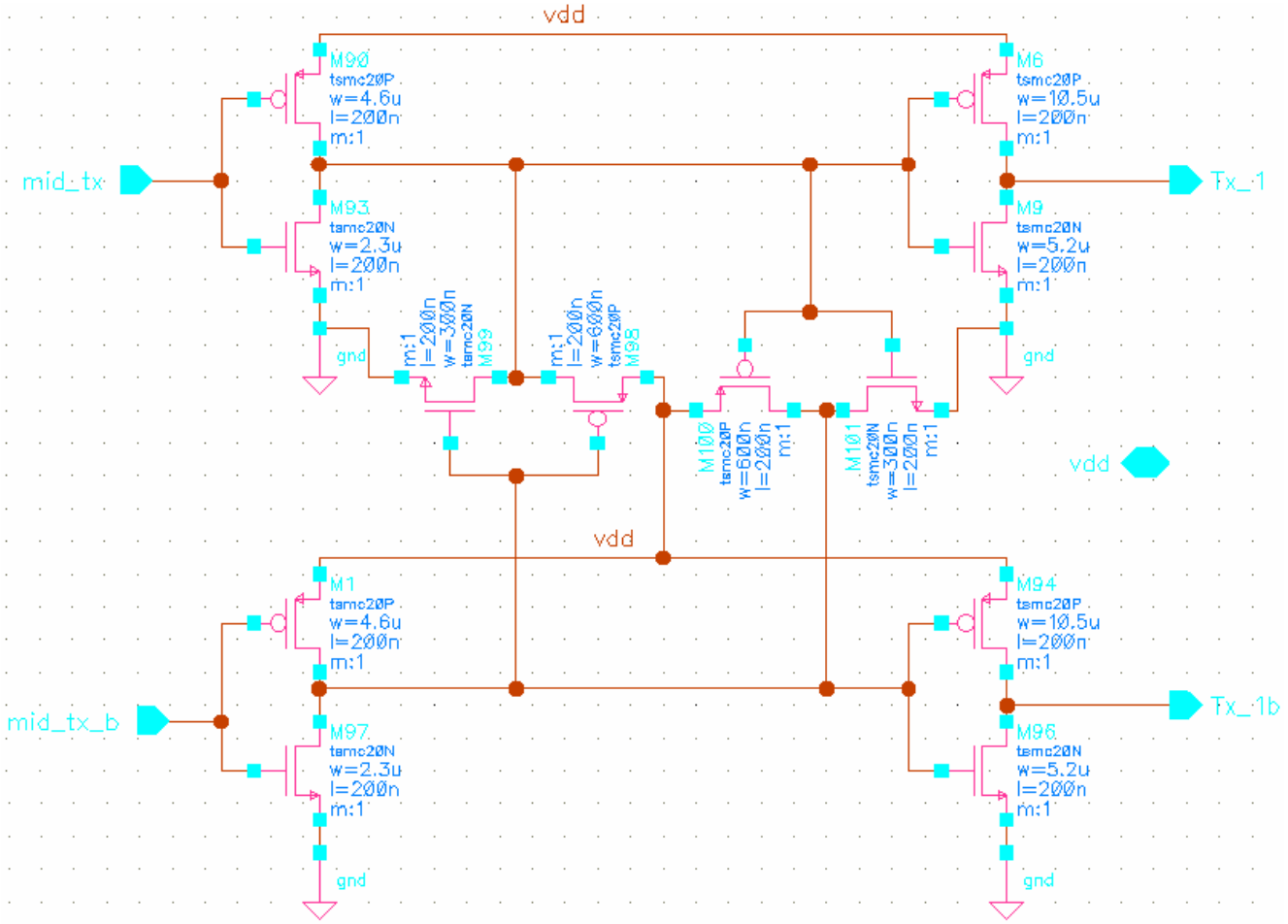

Figure A.5 – Schematic of Transmit Buffer

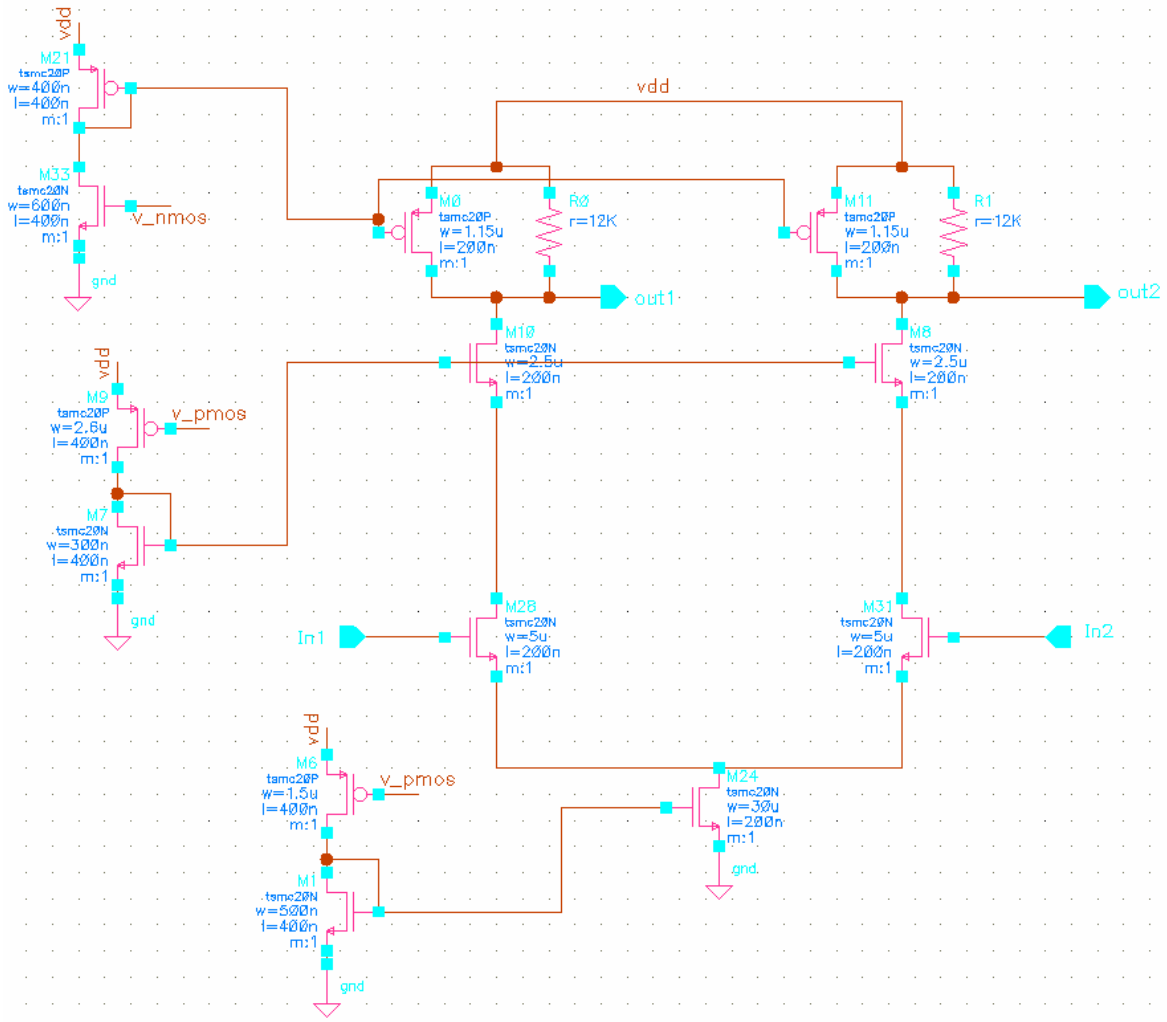

Figure A.6 – Schematic of Differential Amplifier

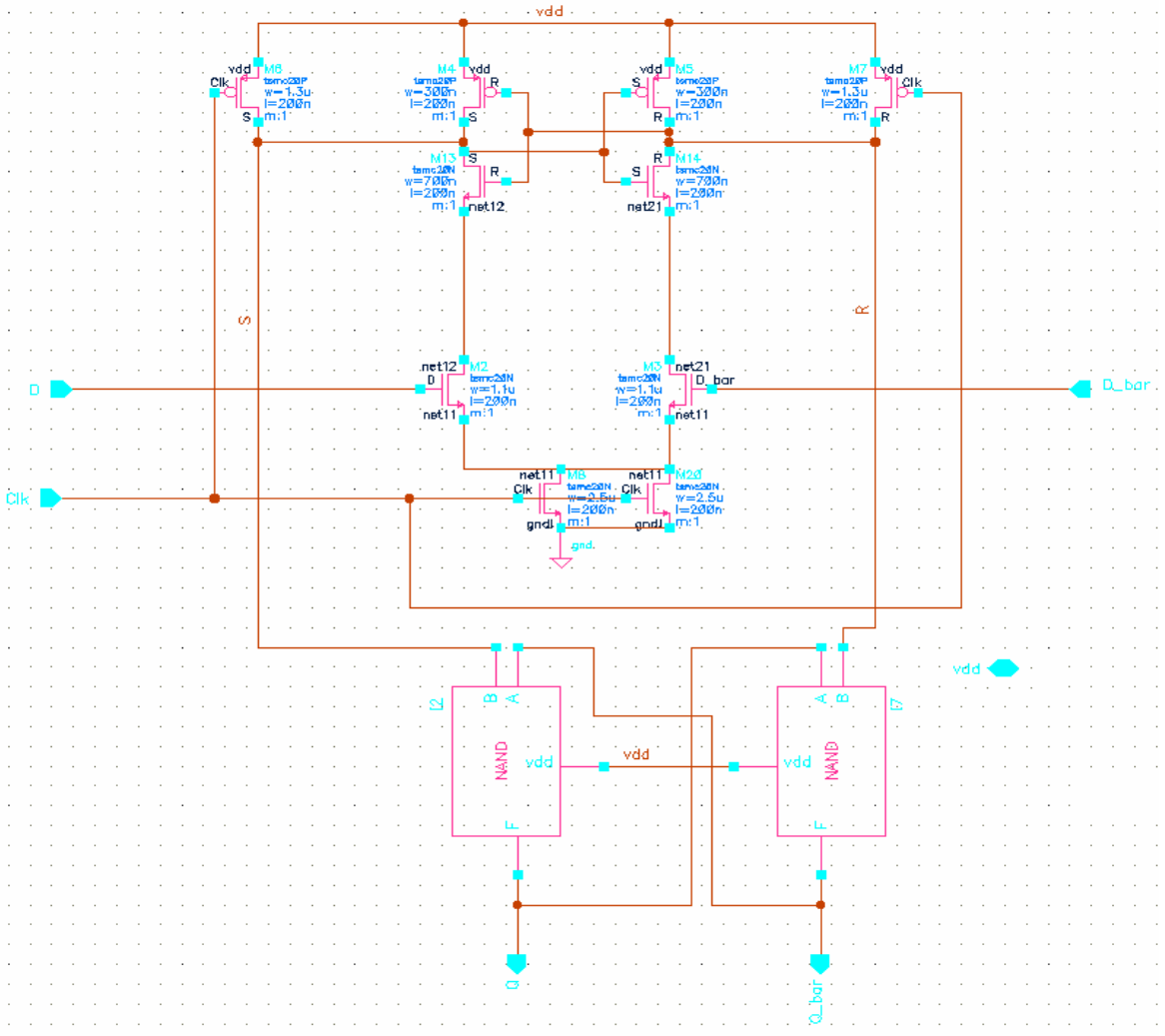

Figure A.7 – Schematic of Sense-amp Flip-flop

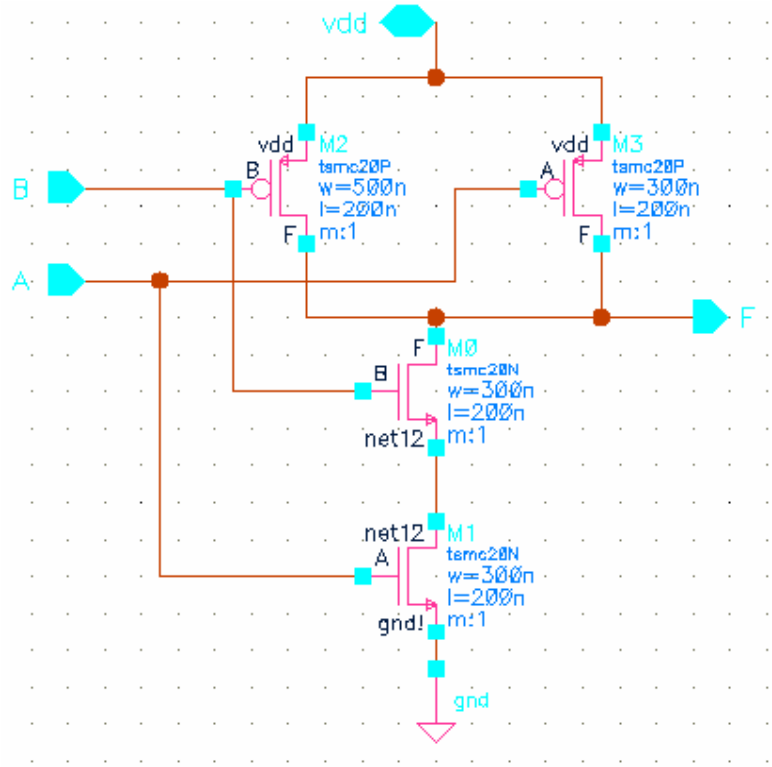

Figure A.8 – Schematic of NAND gate of SAFF

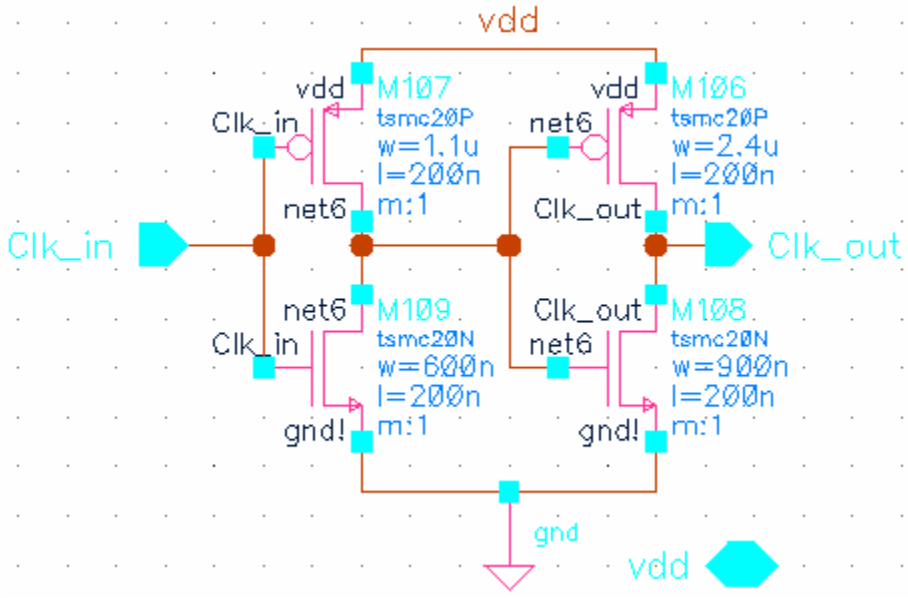

Figure A.9 – Schematic of Receiver Clk Buffer

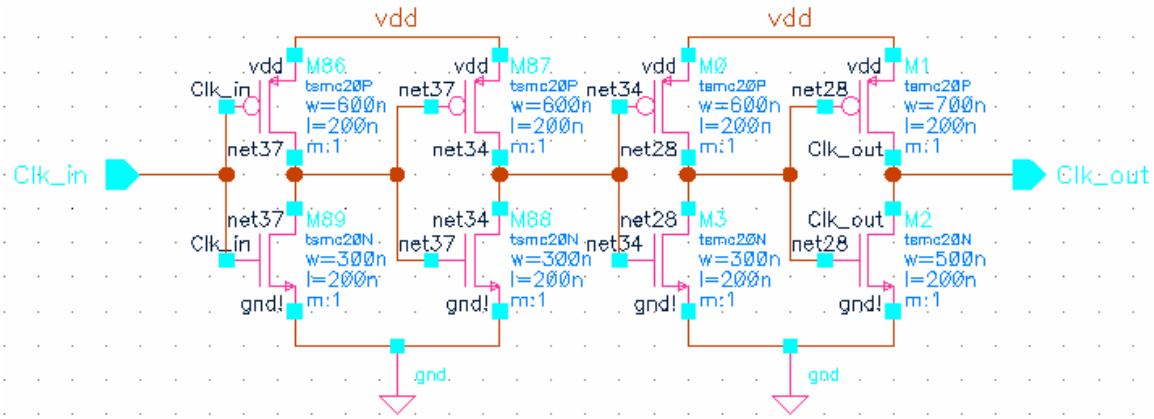

Figure A.10 – Schematic of Receiver Clk Delay Buffer

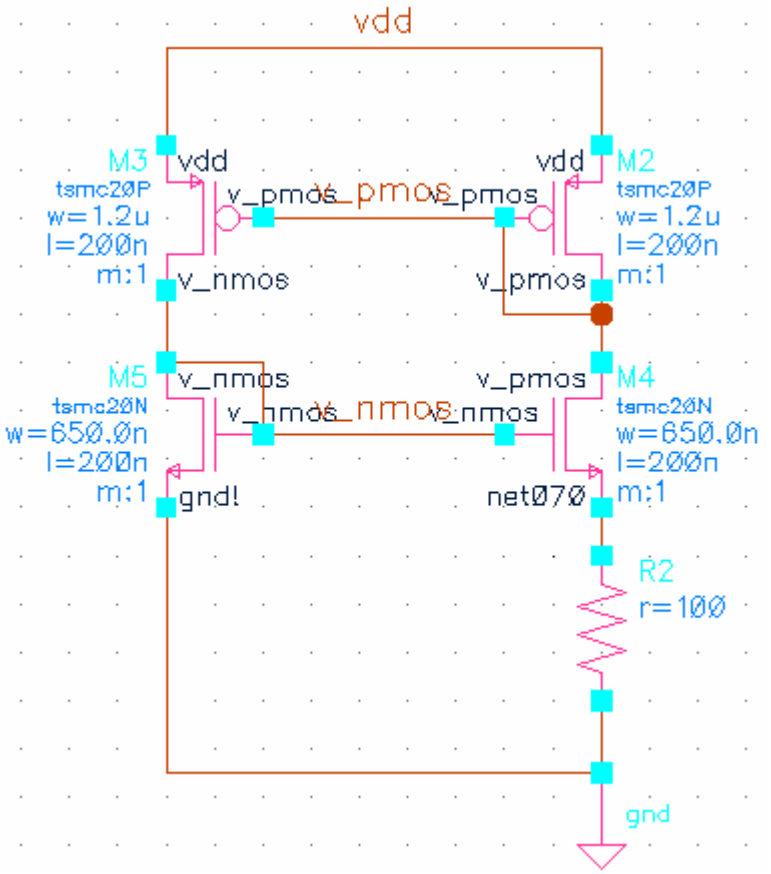

Figure A.11 – Schematic of Biasing Circuit

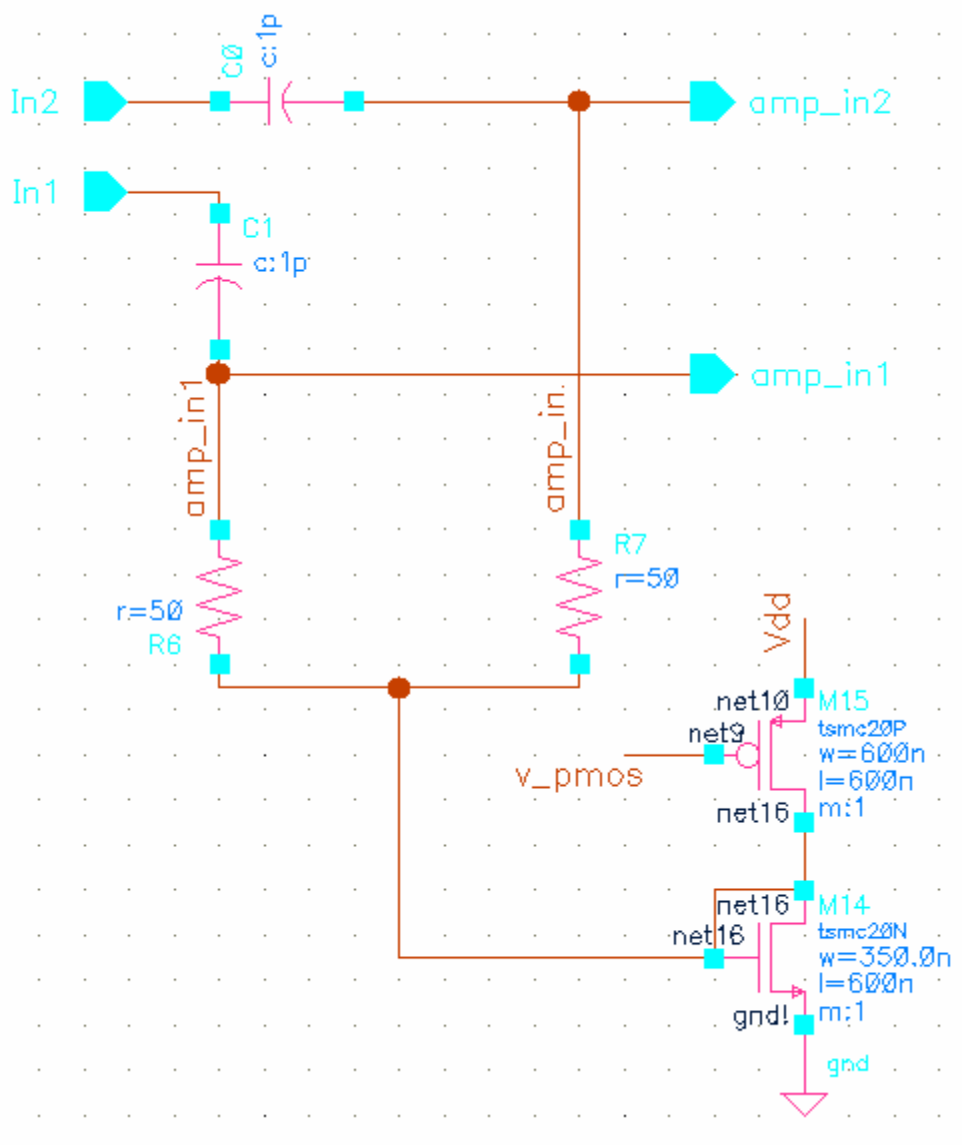

Figure A.12 – Schematic of Receiver Input and termination

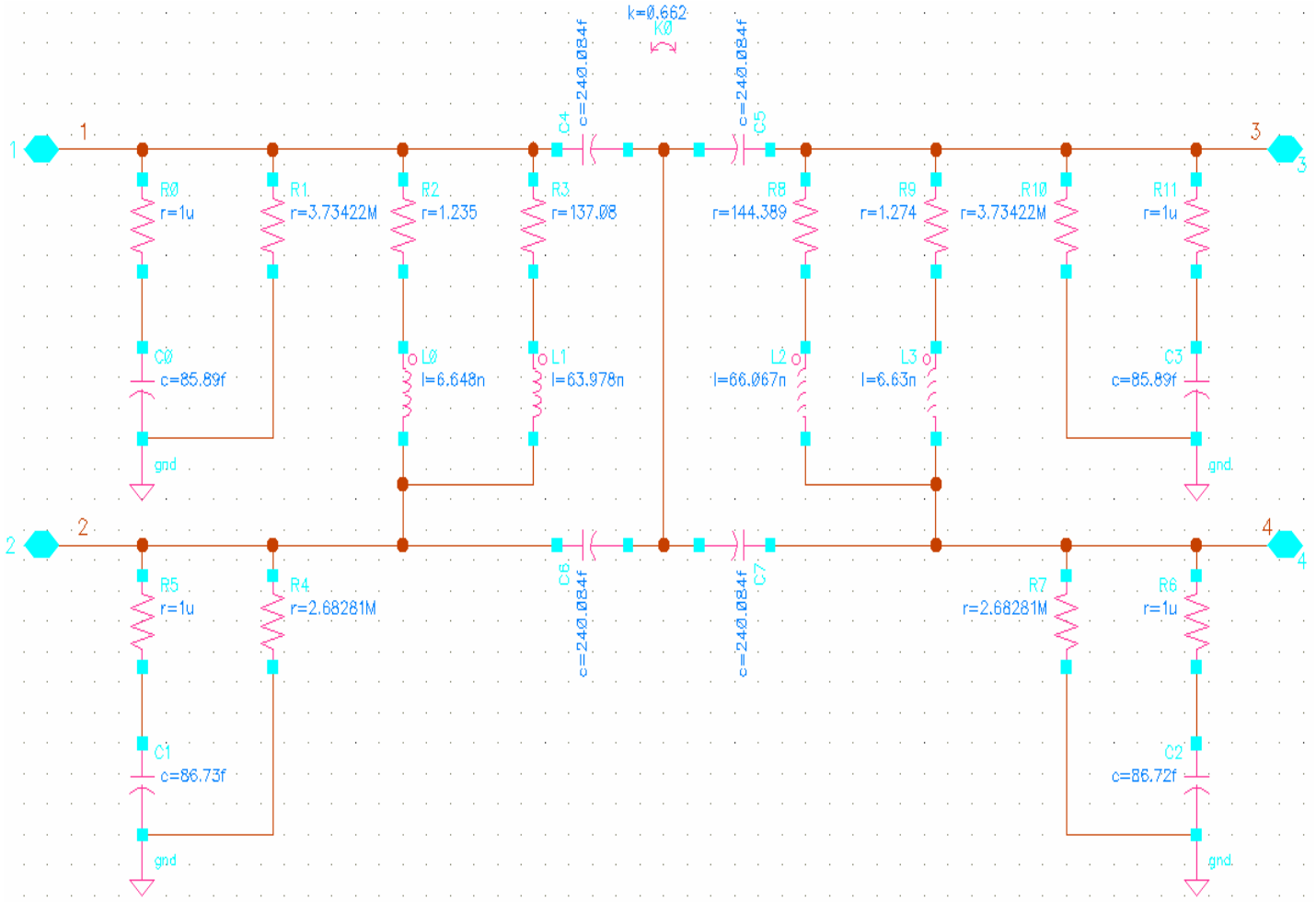

Figure A.13 – RLC equivalent model of Transformer

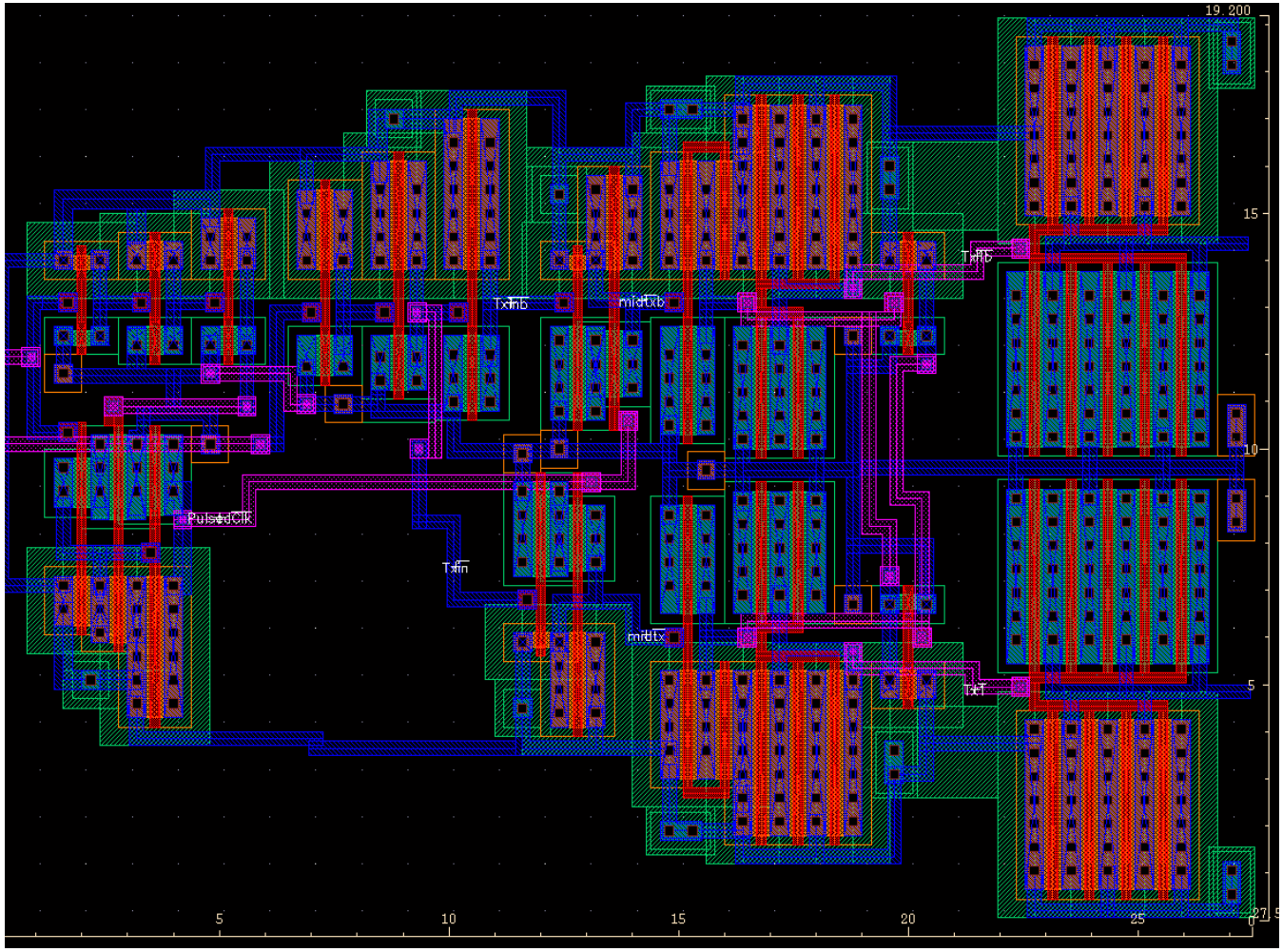

Figure A.15 – Layout of Transmitter

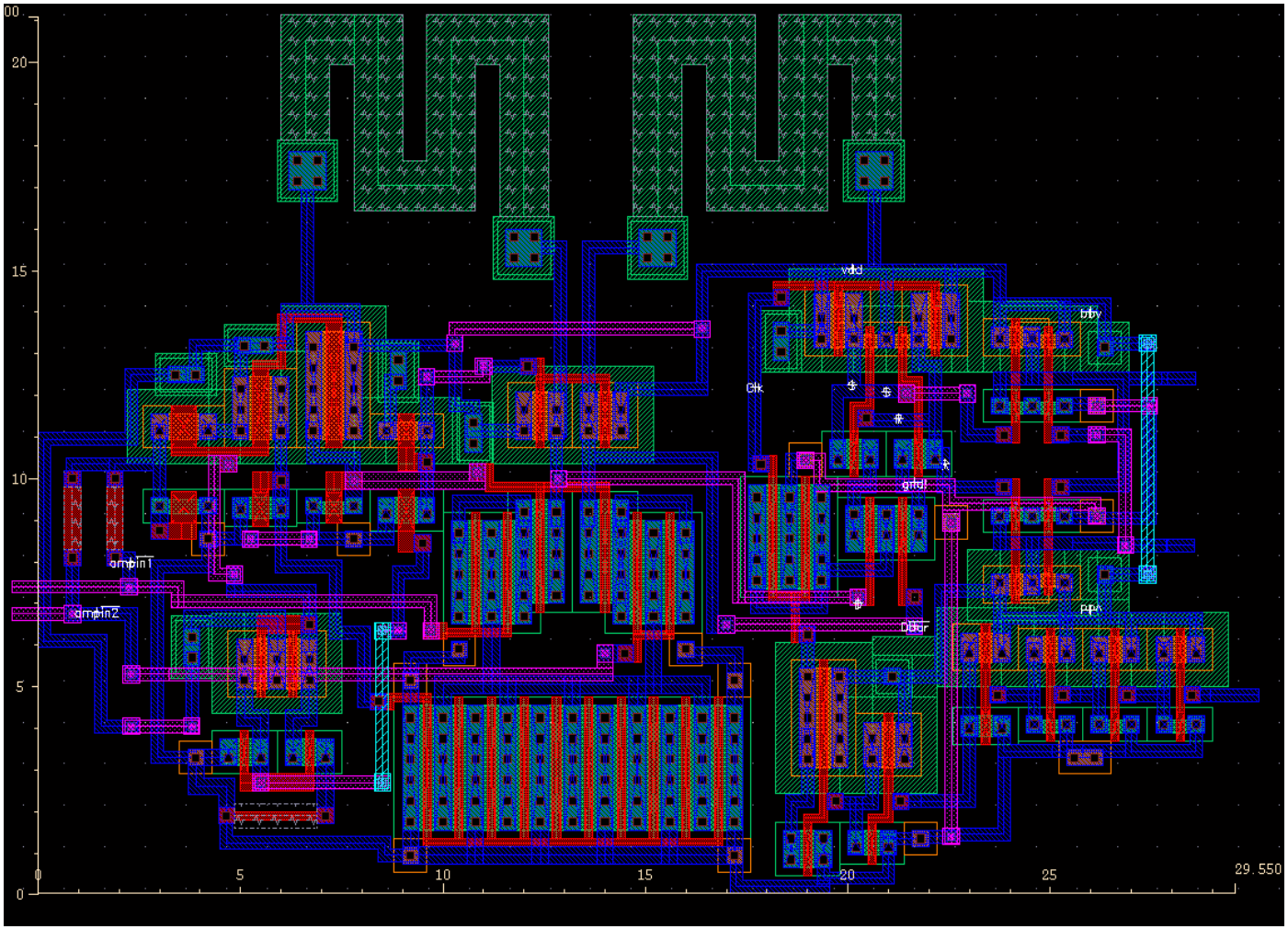

Figure A.15 – Layout of Receiver

APPENDIX B

Matlab Code to generate Bathtub curve

```
clear all

x = 0:5:125;
min_x = 10:5:120;
max_x = -10:5:125;
req_x = 48:19:86;
req_y = [0 0.034 0];
neg_req_y = req_y*-1;
max_y = [
    0.0224
    0.024
    0.0278
    0.0329
    0.0381
    0.0448
    0.0523
    0.0599
    0.0674
    0.0758
    0.0831
    0.09
    0.096
    0.1006
    0.1045
    0.1062
    0.1065
    0.1058
    0.1027
    0.0993
    0.0927
    0.086
    0.0765
    0.0667
    0.0557
    0.0437
    0.0318
    0.0205
];
min_y = [
    0
```

```
    0.0081
    0.01719
    0.0266
    0.0359
    0.0452
    0.054
    0.0616
    0.0692
    0.0754
    0.0805
    0.0841
    0.0848
    0.0843
    0.0812
    0.0771
    0.0702
    0.0618
    0.0516
    0.0403
    0.0286
    0.0154
    0
];
neg_min_y = min_y*-1;
neg_max_y = max_y*-1;

sigma_random = 4.5;
x1 = min_x+7.04*sigma_random;
x2 = min_x-7.04*sigma_random;
x3 = max_x+7.04*sigma_random;
x4 = max_x-7.04*sigma_random;

n=1;
for I=-2:-1:-15
    BER(n) = 10.^I;
    Q(n) = sqrt(2)*erfinv(2*(1-BER(n))-1);
    n=n+1;
end

for J=1:1:14
    temp_x1 = min_x+Q(J)*sigma_random;
    temp_x2 = min_x-Q(J)*sigma_random;
    low_opening(J) = temp_x1(1);
    high_opening(J) = temp_x2(23);
end
```

```
opp_Q = fliplr(Q);
opp_BER = fliplr(BER);
value = -2:-1:-15;
opp_value = -15:1:-2;


plot(high_opening, value, 'k', low_opening, value, 'k',
'LineWidth', 2)
ylabel('BER')
xlabel('eye opening (ps)')
title('Bathtub Curve')
AXIS([-20 140 -15 -2])
grid on
```