ABSTRACT

KIM, JINWOO. Characterization of Hf Si Oxynitride Pseudo-ternary Gate Dielectrics for the Application of Ge MOSFETs. (Under the direction of Gerald Lucovsky.)

The major contribution of this dissertation is to provide a possible engineering solution pathway for the elimination of slow trap density (negative and positive trap charges) and achievement of low interface trap density for the application of high-k dielectrics for high performance Ge MOSFETs. To demonstrate the effect of surface passivation treatment on germanium, four types of surface passivation have been investigated: (1) 1nm of Si + RPAN (15 sec.), (2) 0.6nm of Si + RPAN (50 sec.), (3) 0.6 nm of Si + RPAN (15 sec.), and (4) RPAN (90 sec.). Dramatic improvements such as the extreme reduction of slow trap density (or negative trap charges) and low interface trap density were achieved by thermally stable pseudo ternary HfSiON with pseudomorphic 1 nm of Si passivation with nitridation (1).
As-deposited HfSiON Ge PMOS with this passivation layer yielded a maximum hysteresis of 16 mV corresponding to a slow trap density of 7×10^{10} cm^2, a fixed oxide charge density of 2.2×10^{11} cm^2, and a D_{it} of $7 \times 10^{11} cm^{-2}$ eV^{-1} resulting from the suppression of slow interface states near the valence band for p-Ge.

Thermal stability of 2 nm HfSiON Ge PMOS was successfully demonstrated. It is remarkable that no hysteresis was found across the entire frequency range, indicating that “zero” slow trap density, low D_{it} of $3 \times 10^{11} cm^{-2}$ eV^{-1} and EOT of 0.86 nm were achieved after a 600 °C anneal. In addition, suppression of interface states near E_c by the pseudomorphic Si layer for a HfSiON MOS capacitor was successfully demonstrated by DLTS data. Thermal stability of the pseudomorphic Si layer at a 700 °C anneal was clearly observed.

Furthermore, with this passivation excellent electrical properties of HfSiON NMOS were obtained. Unprecedented C-V curves for HfSiON on p-Ge with this passivation demonstrated the effective suppression of interface states near the conduction band edge (E_c). A N_f value of -5.15×10^{11} cm^{-2}, a slow trap density of 5.21×10^{10} cm^{-2} and a D_{it} of 3.2×10^{11} cm^{-2} eV^{-1} were achieved for HfSiON Ge NMOS. Interface states near E_c have been reported as a major factor to degrade Ge *n*-channel MOSFET performances because it causes weak Fermi level pinning at the conduction band. Therefore, pseudo-ternary HfiSiON with a 1nm pseudomorphic Si passivation layer grown by RPECVD can be novel structure to solve the asymmetric electron and hole mobility degradation in Ge for high performance Ge n-channel MOSFETs.

The successful application of TiO_2 with a pseudomorphic Si layer has been successfully demonstrated. The C-V curve of TiO_2 with a pseudomorphic Si layer also showed well behaved curves such as no kink in depletion and negligible stretch out. It is remarkable that extremely low (~5mV) hysteresis corresponding to a slow trap density of 1.13×10^{10} cm^{-2} and a 0.431 nm of EOT were achieved through a pseudomorphic Si layer with nitridation (process 1) because this passivation yielded large a conduction-band offset energy (CBOE) and also a large valence-band offset energy (VBOE) to Ge. This passivation meets the requirements for high-*k* gate dielectrics with CBOE larger than 1 eV to the semiconductor channel, provides excellent interface quality, and good thermal stability. Therefore, this passivation layer can provide a pathway for the Titanium based Ge-MOSFETs.

Characterization of Hf Si Oxynitride Pseudo-ternary Gate Dielectrics for the Application of Ge MOSFETs

by
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DEDICATION

With love to my parents and my wife's devotion

BIOGRAPHY

Jinwoo Kim obtained his B.S. degree in Materials Science and Engineering, Hanyang University, Seoul, South Korea in 2000. After graduation, he was a member of research staff, Memory R&D Division, Hynix Inc., and focused on Dual oxide and Dual gate electrode formation for sub-0.10μm CMOS device and technical strategy planning for 1G DRAM from 2000 to 2002. He continued to study for M.S. degree in Semiconductor Materials Laboratory, Hanyang Univ. and obtained M.S. degree in Materials Science and Engineering in 2005. While pursuing M.S. degree, he received BK 21 national scholarship of the Ministry of Science and Technology and took responsibility for research projects of the National Program for Tera-level Nano-devices from the Ministry of Science and Technology as one of the 21st century Frontier Programs. He focused his research on physical, chemical, and electrical characteristics of High-k gate dielectrics grown by remote-plasma and direct-plasma ALD. After his graduate study, he worked as researcher in Research Institute of Industrial Science in Hanyang University from 2005 to 2006. He was a visiting researcher of the National Institute of Standards and Technology (NIST), Gaithersburg, MD, US and continued research projects of the NIST about the Advanced MOS Device Reliability and Characterization from 2007 to 2008. From 2008, he enrolled in the Ph.D. program in Dept. of Materials Science and Engineering at NC State University, Raleigh. He joined as research assistant in Prof. Lucovsky's lab and mainly focused on the investigation of high-k gate dielectrics and interface passivation for the application of Ge MOSFETs.

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1 INTROUDCTION

1.1 Need of High-k Dielectrics in Scaled Down CMOS and Memory

Since the first experimental demonstration in 1960, Si-based the Metal-Oxide-Semiconductor-Field-Effect-Transistor (MOSFET) has become the driving force for the semiconductor industry over several decades [1]. Since the 1970s, the transistor density has doubled every 18 months following Moore`s Law. The exponential decrease in transistor dimensions has resulted in increase in microprocessor performance such as higher switching speed or less delay time, less power consumption over technology generations [2-4]. The relationship between transistor performance (transient response time of transistor switching, τ, and oxide capacitance, $C_{ox,}$ and saturation drain current, $I_{D,sat}$) scaling factors are given by the following Eq.:

$$\tau = \frac{C_{load} \cdot V_{DD}}{I_{D,sat}} \tag{1.1}$$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \tag{1.2}$$

$$I_{D,sat} = \left(\frac{W}{2L}\right)\mu_{eff} C_{ox} (V_{gs} - V_T)^2 \tag{1.3}$$

where, C_{load} is the load capacitor of transistor, V_{dd} is the supply voltage, ε_{ox} is the dielectric constant of the gate dielectric, t_{ox} is the thickness of the gate dielectric, W is the channel width, L is the gate length, μ_{eff} is the effective mobility of charge carrier, V_{gs} is the gate-source bias, and V_T is the threshold voltage. Since the transient response time of a

switching transistor is proportional to decreased switching charges in the channel can provide reduced gate thickness and delay time. However, it leads to increased gate-leakage current with thin dielectric layers [5]. Advanced MOSFET processing technology requires gate oxide thicknesses less than 1.5 nm and extending below 1 nm [6]. However, SiO_2 based gate dielectric has been supposed to reach a physical limit beyond 45 nm gate length MOSFET technology [7]. Ultra thin SiO_2/SiON suffers from direct tunneling through gate stacks. Around 1.5 nm SiON has a direct tunneling current of greater than 10^3 A/cm^2 for high-performance logic chips and 0.1 A/cm^2 for low power chips [3].

As scaling reached the sub-100nm regime, more non-silicon elements were introduced to Si technology (Figure 1.1). Currently, alternative gate dielectrics with high dielectric constants have been widely studied because the aggressive scaling of Si MOSFET limits the use of SiO_2 as a gate dielectric insulator. A high-k gate dielectric has the possibility of giving the same capacitance but with a physically thicker dielectric so that leakage current is less (potentially). High-k dielectrics should meet the material requirements *ideally* similar to SiO_2, which has been a perfect match with the substrate; 1) low leakage current level, 2) band gap and band offset more than around 1 eV with substrate for the properties of an insulator, 3) thermodynamic stability against crystallization and phase separation, 4) high interface quality to form a good electrical interface with the substrate, 5) thermally stable in contact with the gate electrode, and 5) minimal bulk electrically active defects-intrinsic defects [8,9]. However, numerous studies for alternative gate dielectrics comparable to thermally grown SiO_2 have been widely investigated, but the superior position of Si-SiO_2 system in the MOS technology has never been replaced. Major problems for the integration of high-k dielectrics

to MOSFETs are listed as (i) leakage current levels that are not solely dependent on physical oxide thickness, (ii) surface dipoles or defects present close to the interface of poly-Si gate/high-k gate dielectrics invoking Fermi level pinning, (iii) lowered channel mobility compared to the universal mobility, and finally (iv) fast charge trapping and trap creation resulting in threshold hysteresis and threshold voltage instability. The presence of defects in high-k gate dielectrics has been considered to be very closely related to these problems.

1.2 The advantages of Germanium

As shown in Table 1.1, Ge provides superior bulk hole (approximately 4 times higher) and electron mobility (approximately 2.5 times higher) than those of Si. To date, several research groups have successfully demonstrated high mobility Ge PMOSFET. Xu. *et. al.* reported that Ge p-MOSFET with HfO_2/TaON offered 1.7-fold hole-mobility enhancement as compared with conventional Si p-MOSFETs (Figure 1.2 (a)) [10]. In addition, PMOS inversion mobility, measured on HfO_2 Ge PMOS fabricated using surface passivation, has 82% higher hole mobility than universal Si mobility (Figure 1.2 (b)) [11]. Moreover, Ge has practical advantages compared to III-V semiconductors. Ge is an elemental semiconductor and has also the advantage of process compatibility, and is easily integrated with Si. Both Ge and Si are using similar dopants and dopant activation techniques and enable self-aligned device as well. Ge has been considered as a promising candidate channel material for future technology nodes because of its attractive fundamental advantages. However, Ge has some critical issues for integration of CMOS technology. In the next section, detailed critical challenges of Ge will be addressed.

1.3 The disadvantages and challenges of Germanium

1.3.1 Interface of gate dielectrics and germanium

Germanium oxide does not offer high quality and stable passivation on Ge, unlike SiO_2 on Si. Germanium oxide exists in various Ge suboxide (GeO_x) states during oxidation and various crystal structures such as amorphous, tetragonal, and hexagonal depending on deposition process [12, 13]. Germanium oxide has a mixture of various oxidation states and transition is available depending on deposition processing, such as pressure and temperature, because surface bonding are affected by these conditions [13,14]. Tetragonal germanium oxide is not water soluble whereas hexagonal and amorphous structures are water soluble. The control of the early stages of oxidation is challenging because of lack of stability of GeO_x. A few angstrom (A) layer of GeO_x usually exists on the germanium surface prior to gate dielectric deposition because of difficulty of passivation of germanium surface against oxidation (Figure 1.3) [15].

GeO_x can be formed after oxide deposition or device processing, even if there is absence of oxide on initial germanium surface. Therefore, the gate dielectrics and germanium interface are the most critical issues for Ge device engineering. Various surface passivation techniques have been widely examined to suppress GeO_x formation during deposition and stabilize or reduce the GeO_x. Therefore, surface passivation between high-k gate dielectrics and Ge has been considered as the most promising approach for the high quality Ge and gate dielectrics interface.

1.3.2 Surface Nitridation

Surface nitridation (GeO_xN_y) using thermal or plasma has been commonly used to passivate germanium surfaces [16-19]. In the case of GeON, nitridation of Ge surfaces provided an improvement of chemical and thermal stability [16]. However, as shown in Figure 1.4 (a) many research groups reported that surface nitridation is creating new slow-interface traps deep in the band gap because nitrided samples show a significant dispersion in the inversion region as the frequency is reduced, indicating the presence of slow-interface states [20]. As shown in Figure 1.4 (b), Dimoulas *et al.* also reported a similar dispersion in the inversion region on p-type substrate after Ge surface was treated with O and N beams due to an increase in minority carrier generation due to diffusion of impurities from the dielectric into the substrate or to the interaction of interface slow states [21]. We also observed large hysteresis in bidirectional C-V caused by slow trap density and large negative flat band voltage shift (V_{fb}) due to large amount of positive fixed charge density with N_2 plasma nitridation on Ge. In addition, Ge MOS device with GeON interfacial layers showed a lack of thermal stability and large gate leakage after 500 C annealing [22]. This can be critical problems for Ge n-MOSFET due to n-MOSFET required above 500 °C for the n-type dopant activation. Moreover, GeON layers showed the lack of effectiveness to prevent interfacial GeO_x formation after dielectrics deposition [22].

1.3.3 Si-Passivation

To solve the problems associated with dielectric and Ge interfaces, Si-passivation has been investigated as an alternative way of forming a high quality passivation on Ge [23-28].

A thin silicon layer grown by epitaxial growth fully passivates with covalent bonds and should not create any states in the band gap. As shown in Figure 1.5 (a) and (b), Si interfacial layer grown by SiH_4+N_2 ambient at 400 °C and by solid source molecular beam epitaxy (SS-MBE) were fully oxidized after dielectric deposition [29, 30]. Those interfaces could reach again the Ge substrate and result in the formation of GeO_x or other oxidation states. In addition, electrical properties of Si passivation devices showed kinks near the inversion regime indicating slow interface states near the valence band (E_V) for n-Ge and slow interface states near the conduction band (E_c) for p-Ge substrates (Figure 1.6 (a) and (b)) [30,31]. Therefore, alternative passivation techniques should be explored to achieve a stable silicon passivation layer during dielectric deposition and further device processing.

1.3.4 Direct deposition of High-k dielectrics on Ge

Research groups reported that high-k dielectrics such as HfO_2 and ZrO_2 were deposited directly on Ge substrate after removing native Ge oxide by thermal or chemical cleaning [32, 33]. High-k dielectrics should be deposited directly on Ge to reduce the interfacial layer; however, intrinsic GeOx layers should be created because of incomplete native oxide removal, oxidation after cleaning, and growth during deposition. High-k dielectrics deposited directly on Ge have presented interfaces with very poor electric properties such as mobility degradation, large frequency dispersion and hysteresis [33, 34]. Figure 1.7 shows, C-V and transmission electron microscope (TEM) results of HfO_2 deposited by PVD with molecular beam deposition at 225 °C from Hf and O atomic beams. In the case of no interfacial layer, TEM shows a very smooth and straight interface between polycrystalline HfO_2 and Ge.

However, the good TEM images in terms of surface roughness between HfO_2 and Ge do not translate into the electrical quality of the interface. C-V measurements of HfO_2 gate stacks straight on Ge invariably show a flat line such as in Figure 1.7, indicating strong Fermi level pinning, and high leakage current level [35]. In addition, large hysteresis due to slow (or border) traps has been also observed in directly deposited HfO_2 films on Ge [36,37]. The problem is probably caused by interdiffusion of Ge into the dielectric, as HfO_2 is highly reactive with Ge [38]. Furthermore, Ge MOSFETs with high-k dielectric directly deposited on Ge exhibits even lower mobility than Si MOSFETs. Currently, surface passivation between high-k gate dielectrics and Ge has been considered as the most promising approach for the high quality Ge and gate dielectrics interface.

1.3.5 Fluorine passivation

One of the alternative passivation of dangling bonds of Ge, Fluorine plasma treatment, has been proposed because the higher bonding energy of the Ge-F bond (5.04 eV) than of the Ge-H bond (<3.34 eV) [39, 40]. The effect of Fluorine which is effectively incorporated in the GeO_x/HfO_2 interface, is shown in Figure 1.8 (a) MOS capacitor with F plasma treatment results showed small kinks and negligible V_{fb} shifts and less stretch-out behaviors [41]. P-MOSFET with F plasma exhibited around 12%~17% higher hole mobility than without F plasma MOSFET (Figure 1.8 (b)) [41].

1.3.6 Slow traps density

As shown in Figure 1.9, slow traps can be broadly present at the interfacial layer and

high-k or at the bulk of high-k dielectric. The time constants of slow traps are so large that they depend on the DC voltage sweeping rate rather than the frequency of AC signal. Trapping properties of MOS dielectric layers are most often evaluated via simple capacitance–voltage (C–V) and current–voltage (I –V) techniques [42].

To date, one of the most critical challenges is large density of slow traps for the application of high-k dielectric on Ge [43]. Large hysteresis due to slow (or border) traps has been commonly observed in directly deposited HfO_2 films, HfO_2 on thermally grown GeO_2, and ZrO_2 on SiO_2/GeO_2 bilayer, HfO_2/Dy_2O_3 gate stack on Ge [43-45]. These problems are probably caused by inter-diffusion of Ge into the dielectric, as HfO_2 is highly reactive with Ge. In addition, large hysteresis of the flat band voltage (ΔV_{FB}) of the GeO_x/Al_2O_3 (~200 mV) and GeO_x /HfO_2 stacks (~900 mV) were observed even though these showed very low the density of interface states (~$3x10^{11}$ cm^{-2} eV^{-1}), approaching state-of-the-art Si/SiO_x /HfO_2 /metal gate stacks [45]. Therefore, the interlayer or passiviation layer should;

1) Be stable after oxide deposition to prevent reaction and interdiffusion at dielectrics and Ge
2) Suppress GeO_x or other oxidation states formation
3) Reduce interface state density
4) Have thermal stability to mitigate problems associated with GeO_x formation and interdiffusion

1.4 Apparatus [46, 47]

The implementation of remote plasma processing chambers into multichamber cluster

systems has made it possible to interrupt plasma assisted oxidation, nitridation, pseudomorphic silicon deposition, and/or film deposition and then, without removing the sample from an ultrahigh vacuum (UHV) compatible environment, perform on-line chemical analysis by Auger electron spectroscopy (AES). This research-level cluster tool consists of three chambers: i) a load-lock chamber for sample introduction, ii) a remote plasma processing chamber (RPP) for (a) interface and/or top surface oxidation/nitridation and (b) film depositions, iii) a surface analysis chamber with AES. Figure 1.9 shows a cross sectional view of the remote plasma processing chamber. The system configuration includes three components: i) a quartz tube which connects to an RF generator to produce localized plasma, ii) two Hafnium and Titanium sources injectors and iii) a heater stage to heat the wafer to temperatures up to 300 ^{o}C. The wafer is isolated from the plasma excitation region and grounded.

The main differences for remote plasma processing from conventional or direct plasma processing are that i) source and carrier gases are selectively excited and ii) deposition substrate is outside of the plasma glow region. The advantages for the remote plasma processing are i) low temperature process, ii) low plasma damage and iii) restricted or controlled chemical pathways. In RPECVD, a high density of reactant species is created by impact ionization in the plasma region of the reactor structure. One important characteristic of RPECVD is that all reactant gases such as N_2O, N_2, and O_2 diluted with He, are directly injected into the plasma tube, or upstream, except SiH_4 used for deposition of pseudo-ternary high-k dielectrics, pseudomorphic Si layer, nitrides and oxynitrides. The downstream SiH_4 injection prevents SiH_4 fragmentation into SiH_x species, which are precursors to

uncontrolled hydrogen incorporation in the deposited dielectric films. The substrate is neutral with respect to the plasma and is located outside of the plasma generation region. This prevents plasma damage to the wafer surface and the deposited film from ion bombardment generated by the plasma [47].

1.5 Electrical techniques: Current-Voltage (I-V) and Capacitance-Voltage (C-V)

For electrical measurements, metal-electrode capacitors were fabricated using shadow masks on mid 10^{17} to low 10^{18} cm^{-2} n- and p-type Si and Ge substrate. Capacitors were prepared in a class-100 cleanroom located at North Carolina State University (NCSU). The overall process steps include surface cleaning, sacrificial thermal oxide and high-k oxide growth, post deposition rapid thermal anneal (RTA), and dot metal electrode (Al) formation using evaporation. The process included forming gas anneal (FGA) for 30 minutes in a mixture of 10% H_2 in N_2 at 400°C used to minimize D_{it}. This step was done before metallization in order to prevent reactions between the Al gate metal and the dielectric films.

Electrical measurements of Si- and Ge-capacitor devices were performed on a Material Development Corporation system. An HP 4284A LCR meter with a frequency range of 10 kHz to 1 MHz was used to perform capacitance-voltage measurements for capacitance dispersion. Current-voltage measurements were done on an HP 4140B voltage source with a pico-ammeter. Voltage-ramp rates were varied from dV/dt = 0.001 V/sec to dV/dt = 0.05 V/sec. A slower ramp rate is preferred to reduce the displacement current, ensuring that the current measured is actually tunneling current. The temperature of the sample was maintained at 25°C and all measurements were performed in a light-tight box. Capacitance-

voltage data was analyzed using NCSU-CVC Version 7 which extracts parameters from measured capacitance voltage traces. As for ultrathin gate oxides, quantum mechanical effects near the surface, specifically increased band bending due to localized energy levels, and the charge centroid being located further from the surface than classically predicted, lead to incorrect C-V parameter extraction in classical analysis. NCSU-CVC Version 7 (Hauser's program) corrects for these-quantum mechanical effects and uses the non linear least squares fitting technique, allowing a more accurate analysis of the data.

1.6 Deep level transient spectroscopy (DLTS)

Deep level transient spectroscopy (DLTS) is a technique used to measure the concentration and identify recombination centers at a certain energy level in the band gap of materials. This technique has been used extensively since its introduction by Lang (1974) to characterize non-radioactive deep traps present in semiconductors. The fabrication of Schottky diodes or p-n junction is necessary to perform DLTS measurements. During measurements, a diode is held at a constant reverse bias and pulsed with a reduced bias. When the diode is held at reverse bias, the space charge region is depleted of majority carriers. The majority carriers move to the depletion region filling deep energy levels along the way during a pulse. Finally, the carriers move out of the region by reverse bias. The capacitance decay by this emission is monitored during DLTS measurement. The discrete energy level, density and capture cross section of specific deep level impurity can be determined by the DLTS data collected over a range of temperatures.

In contrast of conventional DLTS system, the interface trapped charge DLTS

measurement can determine not only interface traps continuously distributed in energy through the energy band gap, but bulk traps which have discrete energy levels. The interface qualities of different interfacial transition regions (ITRs) can be examined by the plot of interface trap densities (D_{it}) versus energy levels (in case of P-MOS, E_c-E_t) converted from DLTS spectra. The separation of interface states and bulk traps can be possible with various pulse voltages. Putting it differently, the peak of interface state changes with various pulse voltages, on the other hand, the peak of bulk trap shift. This method for distinction of interface states and bulk traps is useful to determine the effect of D_{it} on C-V measurements.

1.7 Overview of dissertation

As investigated by previous researches, remarkable progress has been achieved on Ge MOSFETs, especially p-MOSFETs. However, surface passivation of high-k and germanium interface has been considered to be a serious challenge and asymmetric electron and hole mobility degradation has not been solved. Furthermore, thermal stability of passivation layer has remained a serious challenge for the application of conventional CMOS process. In this study, pseudo-ternary Hf Si oxynitride (HfSiON) and HfO2 on Si and Ge are demonstrated. Pseudomorphic silicon layer following nitridation deposited by remote plasma enhanced chemical vapor deposition (RPECVD) are also focused on this study; However, GeOxNy passivation layer is also investigated. The specific goals of this dissertation are as following:

1) Investigation of properties of HfSiON gate dielectrics

2) Development and optimization and investigation of pseudomorphic silicon layer following nitridation

3) P- and N- MOS Device performance of HfSiON with Si passivation and GeOxNy

4) Investigation of thermal stability of pseudomorphic silicon layer on Ge

This dissertation is organized into six chapters. Chapter Two addresses the properties of HfSiON ($(HfO_2)_{0.3}(SiO_2)_{0.3}(Si_3N_4)_{0.4}$) deposited by RPECVD on Si to demonstrate the intrinsic properties of HfSiON gate dielectric. Electrical properties of HfSiON on Ge with surface nitridation and the effects of annealing on those devices will be investigated.

Chapter Three discusses development, optimization and investigation of pseudomorphic silicon layer following nitridation using in-situ AES analysis and XPS. Four types of surface passivation are employed to investigate the effect of surface passivation treatment on Ge: (1) 1nm of Si + RPAN (15 sec.), (2) 0.6nm of Si + RPAN (50 sec.), (3) 0.6 nm of Si + RPAN (15 sec.), and (4) RPAN (90 sec.). As-deposited HfSiON Ge MOS devices with four types of surface passivation will be estimated.

Chapter Four presents an investigation of the thermal stability of pseudomorphic silicon layers on Ge and the effects of annealing on HfSiON Ge MOS devices to achieve below EOT 1nm. The energy distribution of interface states is studied by DLTS. Electrical properties of TiO_2 (4nm) on n-Ge with same passivation layer will be addressed for the application of Ge MOSFETs.

Chapter Five investigates the electrical properties of HfSiON with same passivation on p-type Ge to demonstrate the suppression of interface states near the conduction band edge (E_c) by passivation layer. .

Chapter Six concludes the dissertation with a summary and suggestions for future work in these research areas.

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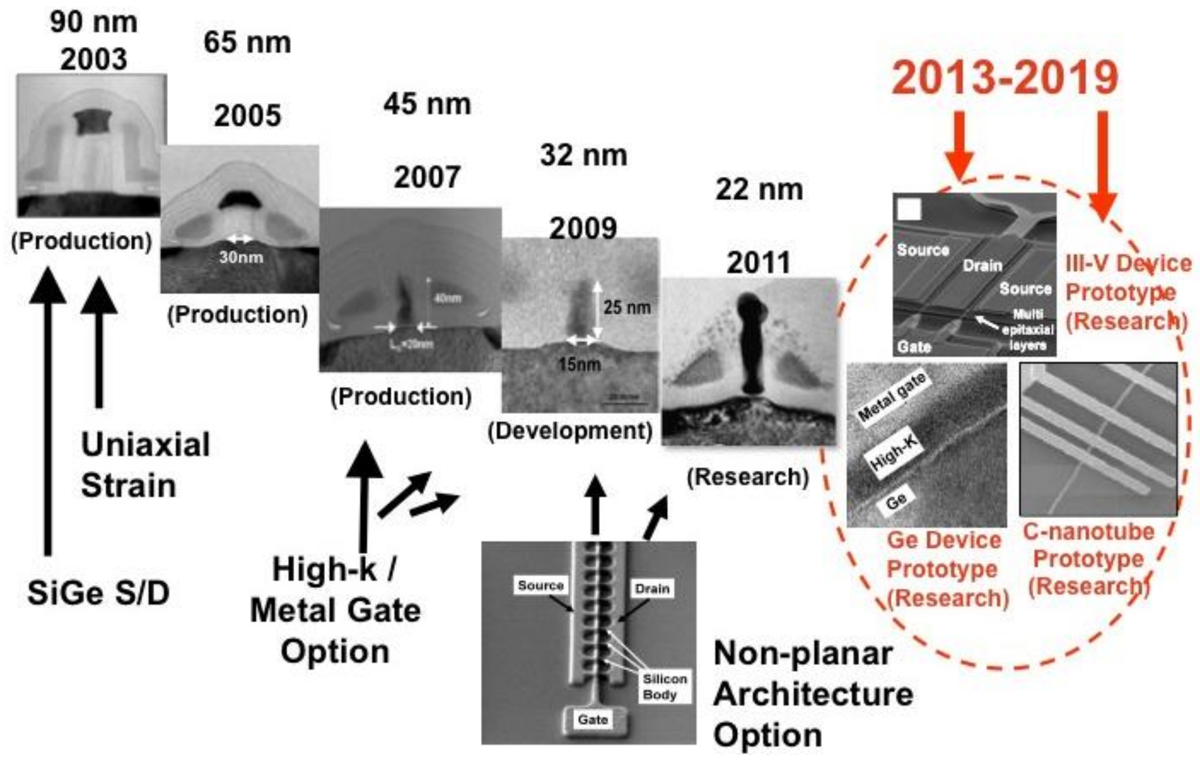
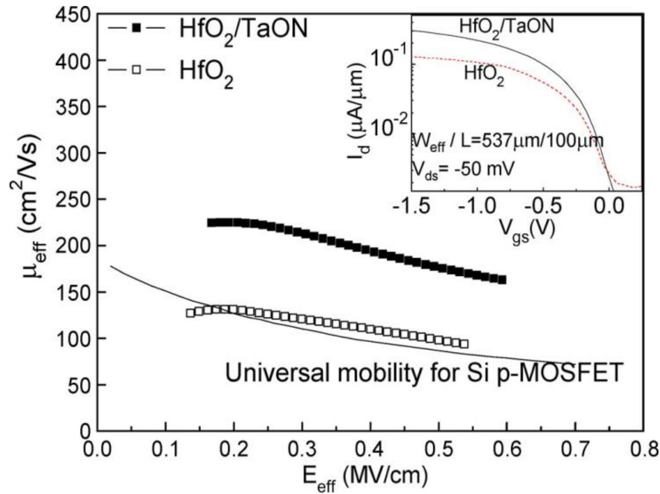


Figure 1.1. Sub-100 nm CMOS technology scaling (Intel Corp)

(a)



(b)

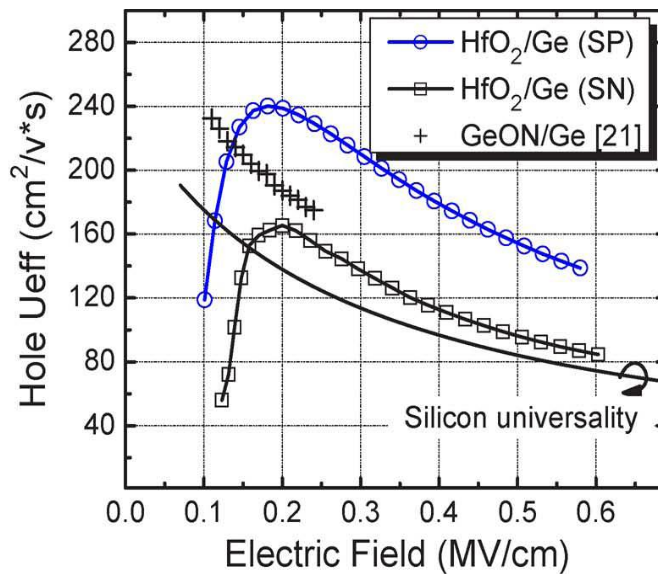


Figure 1.2 (a) Effective hole mobility of the two Ge p-MOSFETs and (solid line) the universal hole mobility for conventional Si p-MOSFETs. The inset is their transfer characteristics. (b) Extracted effective hole mobility of the p-FET. The SP process results in much improved mobility over other technologies involving nitrogen.

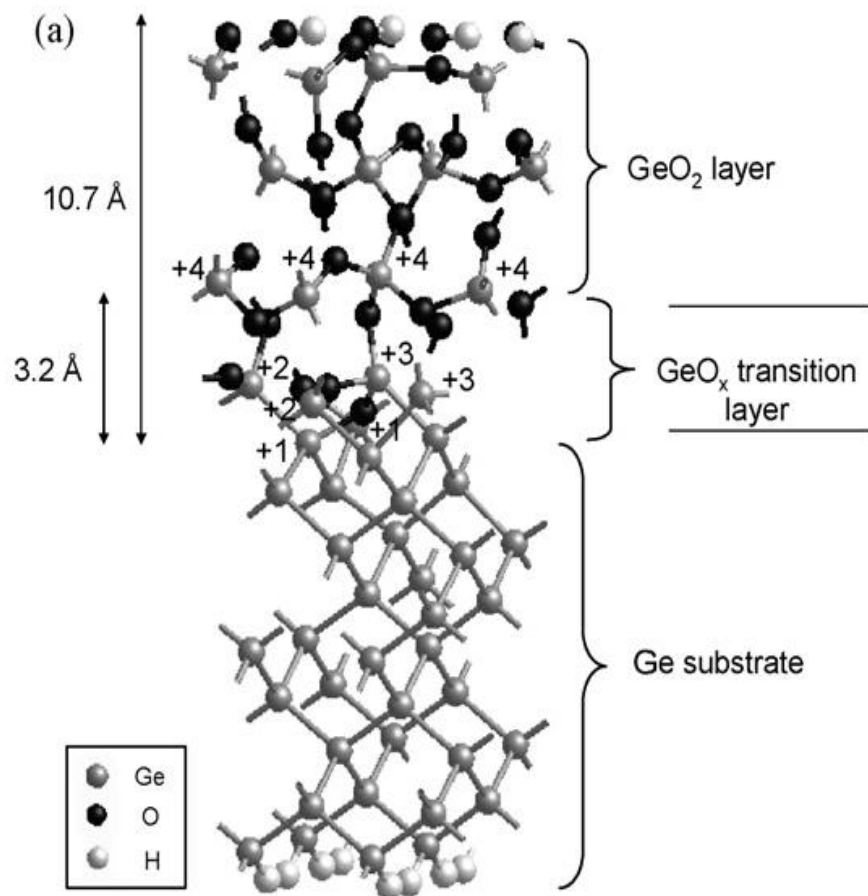
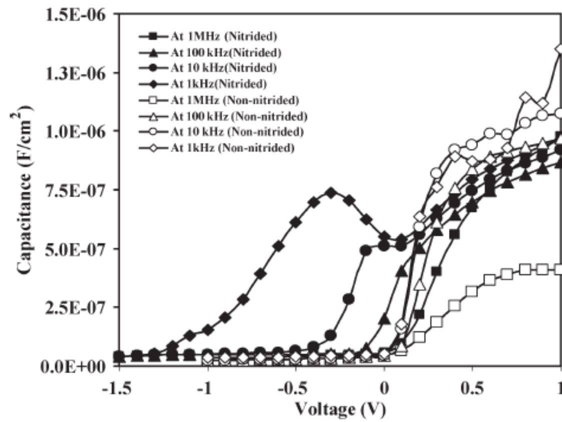


Figure 1.3 GeO_x suboxide layer between Ge substrate and GeO_2 layer

(a)



(b)

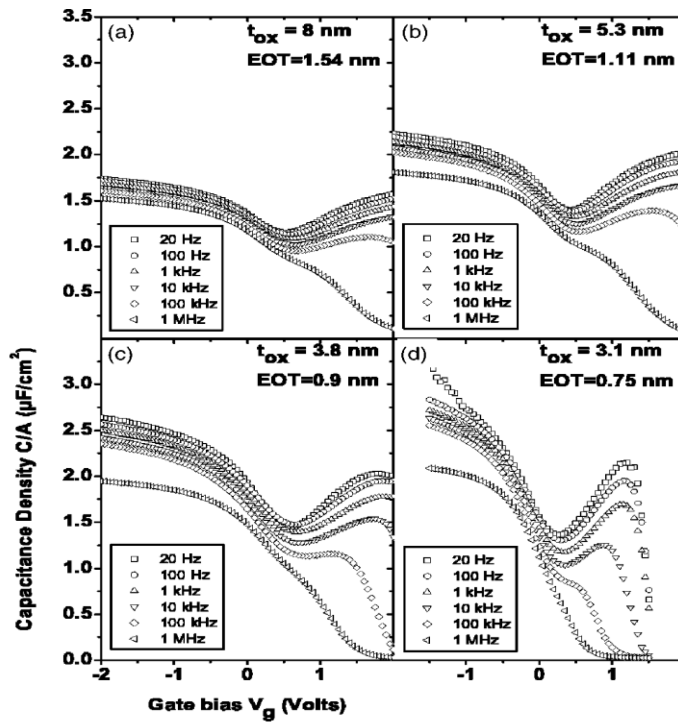
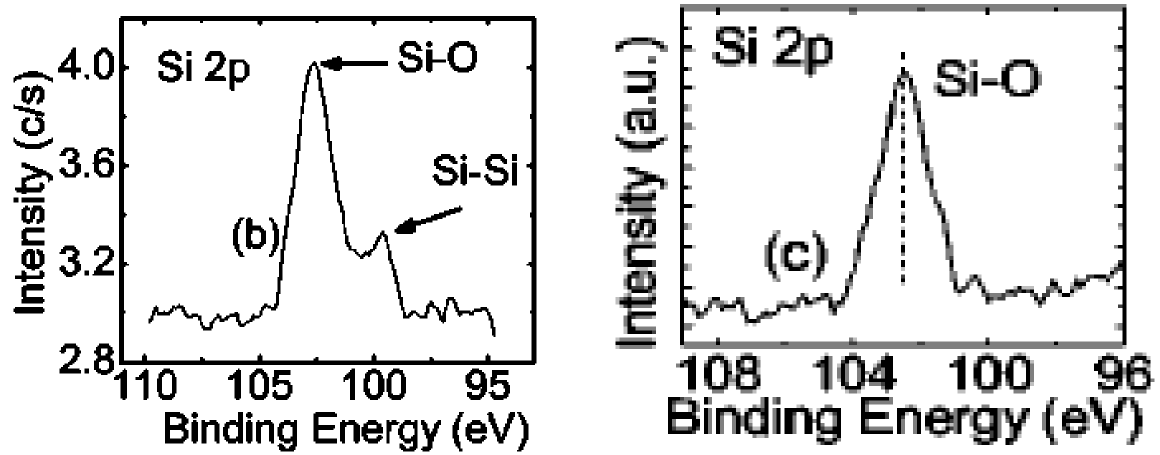


Figure 1.4 (a) C–V characteristics of nitrided and nonnitrided Ge/HfO_2/Al MOS capacitors at different frequencies ranging from 1 kHz to 1 MHz. (b) Frequency dependence of C-V curves for as-deposited p-type MIS capacitors. The scale and axes labels in (a), (b), and (d) are the same as the ones shown with the graph in (c).

(a)



(b)

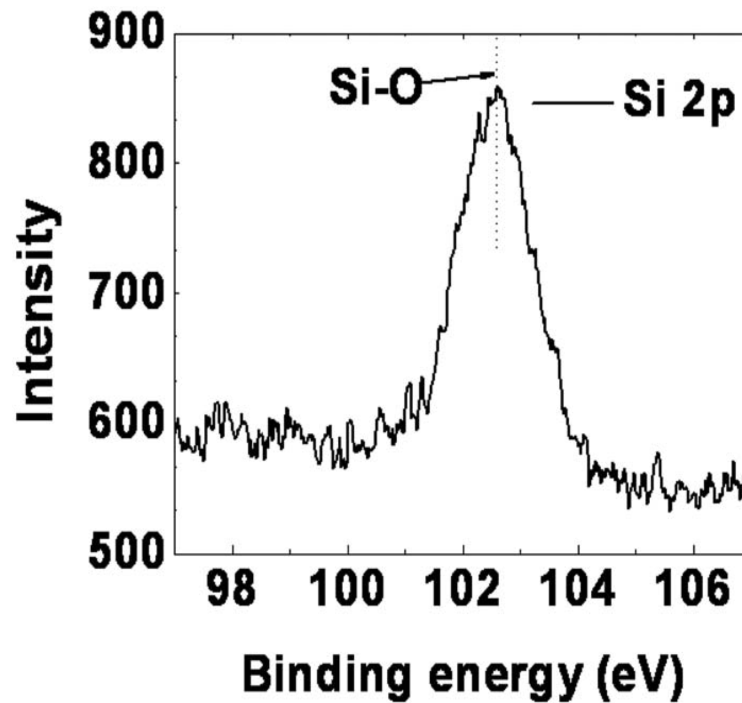
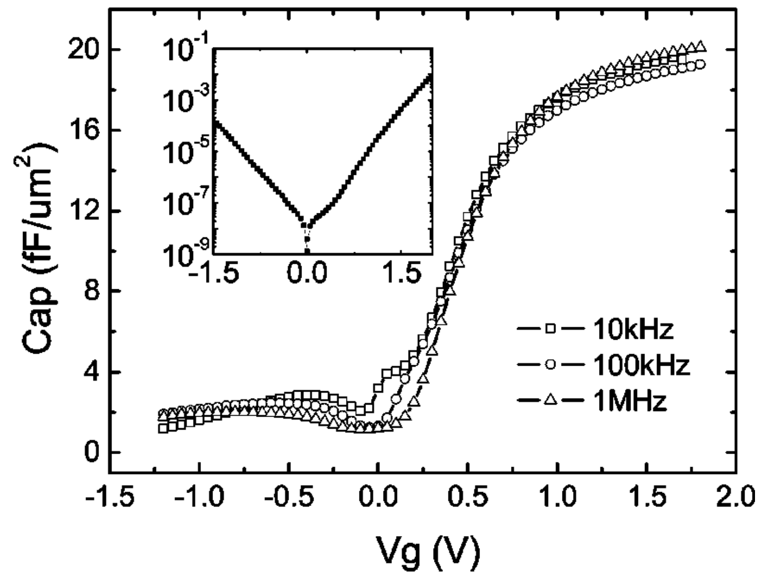


Figure 1.5 (a) The Si 2p spectra of the samples after SiH4 passivation (left) and after HfO_2 MOCVD.(right).(b) Core level Si 2p x-ray photoemission spectra of the Al_2O_3 /4 MLSi/Ge sample, showing the Si–O peak at 102.6 eV

(a)



(b)

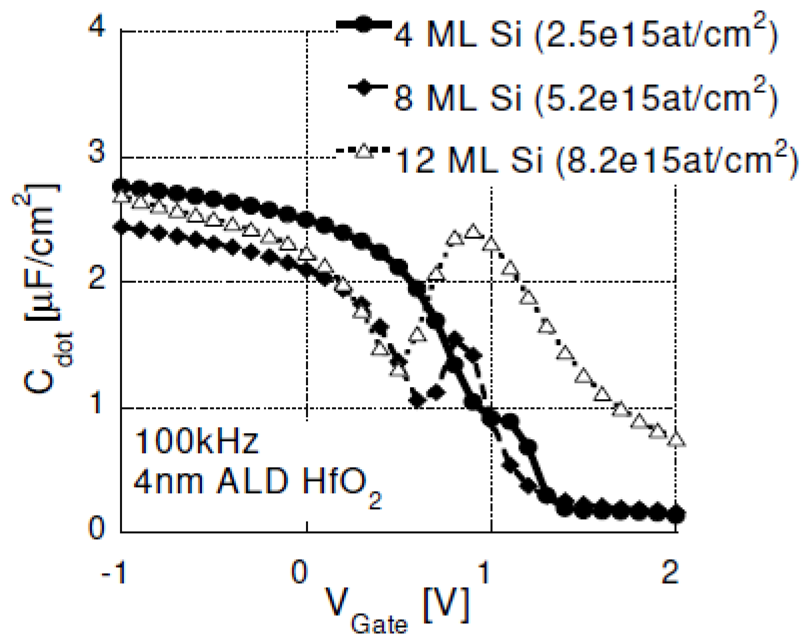


Figure 1.6 (a) Electrical characteristics of the TaN/HfO_2 /Ge MOS capacitor with SiH_4 surface passivation. (b) CV characteristics in the capacitor experiment with 4, 8 and 12 monolayers (ML) of Si

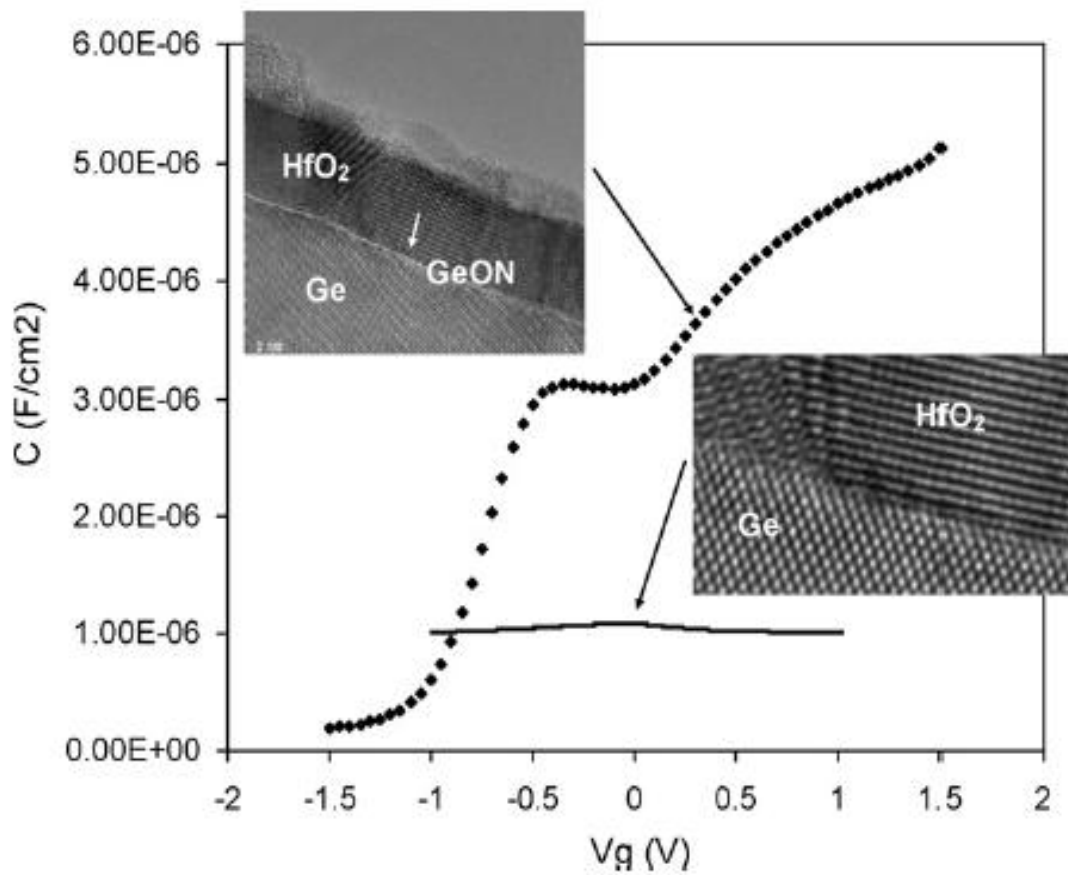
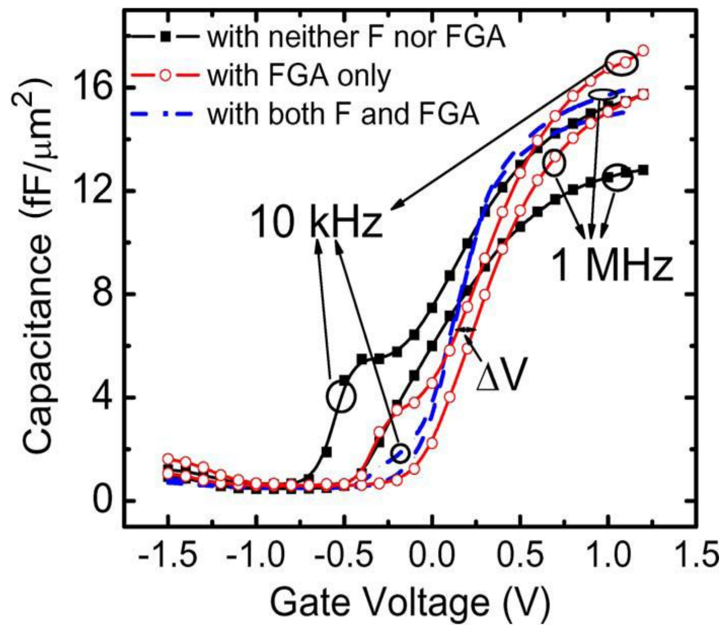


Figure 1.7. C–V curves of TiN metal dot capacitors on MBD-grown 4.5 nm HfO_2 on either a GeON layer (upper curve) or on HF dipped Ge (lower curve). The insets show x-TEM images of the interface between HfO_2 and Ge with pre-deposited GeON interfacial layer (0.5–1.5 nm) and without.

(a)



(b)

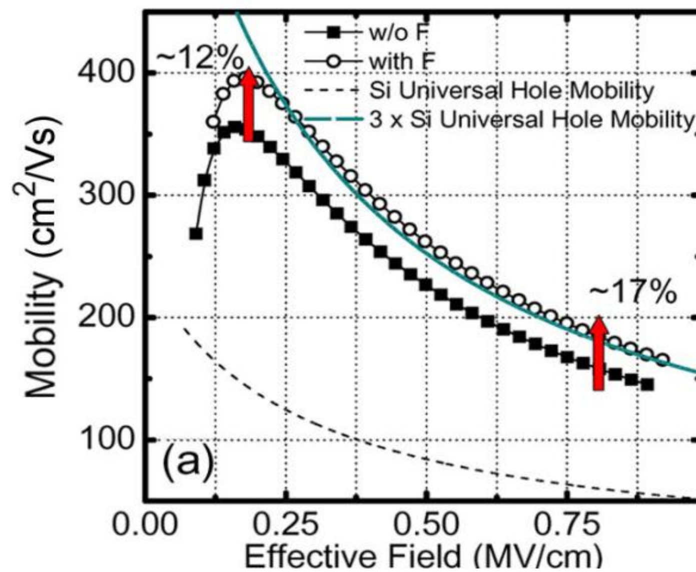


Figure 1.8 (a) C–V characteristics for TaN/HfO_2/GeOx/Ge MOS capacitors without any postgate treatment, with FGA, or with both F incorporation and FGA. (b) Hole mobility as a function of vertical effective field for pMOSFETs with and without F incorporation.

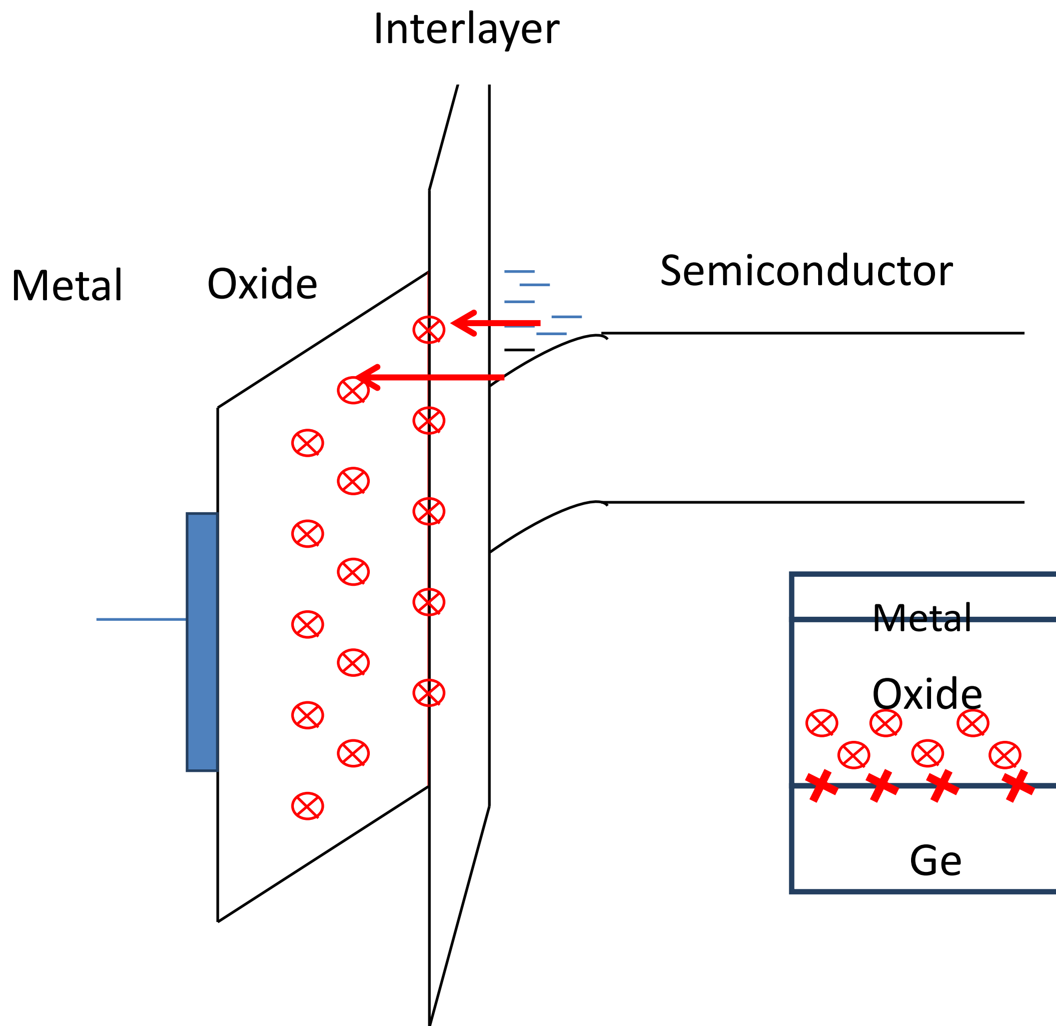


Figure 1.9 Schematic illustration of the slow traps existed at the interfacial layer/high-k dielectrics and in the bulk of high-k dielectric. Inset of Figure shows schematic illustration of defects in MOS oxides. Shown are border traps in oxide and interface traps.

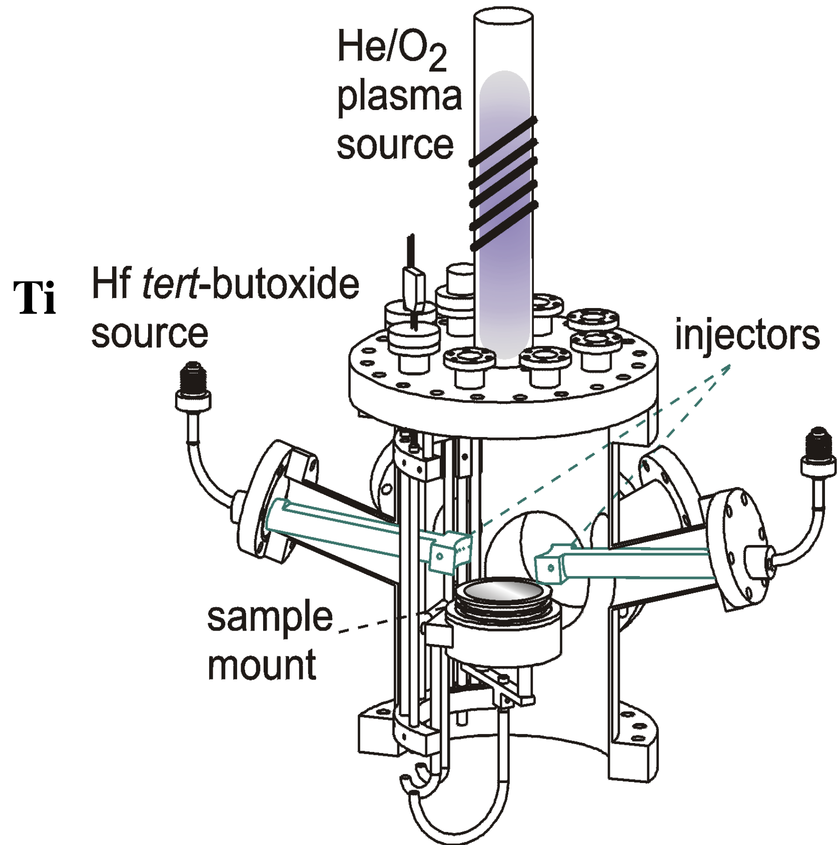


Figure 1.10 Cross sectional view of remote plasma processing system.

2 Investigation of properties of pseudo-ternary HfSiON on Si and nitride Ge

Abstract

Investigation of HfSiON ($(HfO_2)_{0.3}(SiO_2)_{0.3}(Si_3N_4)_{0.4}$) deposited by RPECVD on Si and nitrided Ge substrate are reported in this chapter. The results of HfSiON on Si have been briefly introduced to demonstrate intrinsic properties of HfSiON for applying to Ge with surface nitridation by remote plasma. As-deposited HfSiON MOS devices show excellent C-V curves such as negligible frequency dispersion and hysteresis, absence of bumps at any regime, and minimal stretch out which correspond to interface trap states. Electrical properties of HfSiON Si-MOS device are approaching state-of-the-art Si/SiO_2/metal gate stacks such as slow trap density of 1.24×10^{10} cm^{-2}, D_{it} of 5.7×10^{10} $eV^{-1}cm^{-2}$, fixed oxide charge density of 4.67×10^{11} cm^{-2}, and very low leakage current level (5.2×10^{-8} A/cm^{-2}). Those excellent properties of HfSiON on Si do not transfer to apply to Ge substrate. HfSiON Ge-MOS device shows inferior electrical properties such as large hysteresis, severe stretch out, bumps near depletion regime, and severe frequency dispersion due to incorporation of Ge into gate dielectrics. For 650 °C we obtain devices with improved interface quality such as minimum slow trap density and D_{it}, However, D_{it} in the lower half of the band gap will still lead to bumps where the sizes are frequency dependent. Therefore, alternative passivation technique should be explored to achieve improved performance for Ge MOSFETs.

2.1 Introduction

There has been considerable interest in Ge for applications in scaled complementary metal-oxide semiconductor (CMOS) devices due to several attractive properties of Ge including higher carrier mobility for larger drive current, smaller mobility band gap for supply voltage scaling, and smaller optical band gap to broaden the absorption wavelength spectrum [1,2].

However, because of many difficulties related with different physical and chemical properties of Ge, Ge based CMOS technology has not been achieved. One of the most critical issues is to obtain superior interface properties for a Ge metal–oxide-semiconductor (MOS) capacitor, leading to conducting numerous studies on alternative passivation technology for interface between gate dielectric film and Ge substrate. GeO_2, Ge_3N_4, and GeO_xN_y, on Ge surface have been widely attempted for the high quality of interface [3-6]. However, many research groups reported that surface nitridation is creating new slow-interface traps deep in the band gap because nitrided samples show a significant dispersion in the inversion region as the frequency is reduced, indicating the presence of slow-interface states [7].

In this chapter, HfSiON ($(HfO_2)_{0.3}(SiO_2)_{0.3}(Si_3N_4)_{0.4}$) deposited by RPECVD on Si has been briefly introduced to demonstrate intrinsic properties of HfSiON for applying to Ge with surface nitridation by remote plasma. In addition, electrical properties of Al/HfSiON/nitridation/n-Ge MOS capacitors with rapid thermal anneal (RTA) will be investigated to demonstrate the quality of nitride passivation layer and HfSiON gate dielectrics.

2.2 Experimental Procedures

2.2.1 Pseudo-ternary HfSiON ($(HfO_2)_{0.3}(SiO_2)_{0.3}(Si_3N_4)_{0.4}$) on Si and Ge

After HF cleaning of n-Si wafers, 5 nm of pseudo-ternary HfSiON($(HfO_2)_{0.3}(SiO_2)_{0.3}(Si_3N_4)_{0.4}$) gate dielectrics were deposited by remote plasma-enhanced metal organic chemical vapor deposition (RPECVD) onto n-Si substrates with 0.6–0.8 nm thick SiON interfacial layers. The Si and Hf source gases, 2% SiH_4 in He, and Hf (IV) t-butoxide respectively, were delivered directly into the substrate region of a remote plasma reactor through two different injectors. An N_2/N_2O/He mixture was subjected to remote plasma excitation at 30 W and 13.56 MHz and was employed to initiate RPECVD process. The processing chamber pressure and substrate temperature were 30 mTorr and 300 °C for all depositions, including interfacial oxidation and nitridation.

To compare, the same dielectrics deposited onto remote plasma nitrided n-Ge substrates. Prior to plasma processing native oxides were removed by wet chemistry techniques that have been optimized for Ge substrates using visible/vacuum ultraviolet spectroscopic ellipsometry, and are qualitatively different than conventional wet chemical processing for Si substrates; i.e., they are generally less acidic in nature [1]. Detailed NH_4OH based cleaning procedure will be introduced in chapter three.

2.2.2 Fabrication of HfSiON PMOS capacitors

For the fabrication of HfSiON MOS devices and electrical characterization studies, A 500 nm Al layer was evaporated and defined by shadow mask. Forming gas anneal (FGA) for 30 minutes in a mixture of 10% H_2 in N_2 at 400°C was used to minimize D_{it}. This step was done

before metallization in order to prevent reactions between the Al gate and the dielectric films. Electrical measurements were performed on a Material Development Corporation system. An HP 4284A LCR meter with a frequency range of 1 kHz to 1 MHz was used to perform capacitance-voltage measurements for capacitance dispersion. Current-voltage measurements were done on an HP 4140B voltage source with a pico-ammeter. Voltage-ramp rates were varied from dV/dt = 0.001V/sec to dV/dt = 0.05 V/sec. A slower ramp rate is preferred to reduce the displacement current, ensuring that the current measured is actually tunneling current. All electrical measurements were performed in the dark room and at room temperature.

2.3 Results and Discussion

2.3.1 Properties of HfSiON gate stack on Si

Figure 2.1 (a) shows the frequency dependence of C-V characteristics of as-deposited Al/HfSiON (5nm)/RPN+RPO/n-Si PMOS capacitors. The capacitance was measured at various frequencies as a function of gate voltage and the capacitor was swept from inversion to accumulation at room temperature in the dark room. The C-V curve of the as-deposited device shows excellent behavior curves such as negligible frequency dispersion, absence of bumps at any regime, and minimal stretch out which correspond to interface trap states. As shown in inset of Figure 2.1, the retrace on the 1 MHz curve of this device shows about 12mV of hysteresis corresponding to a slow trap density of 1.24 x 10^{10} cm^{-2}. Around 10 ~12 mV of hysteresis was found across the entire frequency range. Figure 2.1 (b) shows measured and calculated C-V curves of a HfSiON Si PMOS capacitor. The C-V curve was

measured at 1 MHz and 25 ^{o}C in the dark. The gate voltage was swept from negative to positive voltage (or from depletion to accumulation). Superior agreement between measured HFCV and simulated LFCV is observed for the sample, suggesting excellent quality of interface. V_{fb} and N_f values calculated form $V_{fb, ideal}$, net donor concentration, and EOT extract by NCSU-CVC version 7 were -0.082V, 4.67 x 10^{11} cm^{-2}, 1.5 x 10^{18} cm^{-3} and 1.954 nm, respectively.

Figure 2.2 (a) shows interface trap density (D_{it}) as a function of gate bias for Al/HfSiON (5nm)/RPN+RPO/n-Si PMOS capacitors. Using the conductance technique interface state densities could easily be extracted using following Eq. (2.1). Furthermore, in a plot of G_p/ω versus log-*f*, a maximum is observed at 10 kHz, therefore 10 kHz was chosen as the measurement frequency.

$$D_{it} = \frac{0.4(G_p / \omega)}{qA} \tag{2.1}$$

where, G_p is the peak conductance [8].

The determined D_{it} of MOS capacitor is ~5.7 x 10^{10} $eV^{-1}cm^{-2}$.

Figure 2.2 (b) shows leakage current density of HfSiON MOS capacitor. As can be expected, very low leakage current level, 5.2 x 10^{-8} A/cm^{-2} at V_g-V_{fb}=1 V, is achieved for HfSiON MOS capacitor.

Figure 2.3 shows HRTEM result of HfSiON (4nm)/RPN+RPO/n-Si gate stack. As can be measured, the HfSiON dielectric layer has a thickness of around 4.9 nm including

amorphous interlayer has a thickness of 0.9 nm. All these layers have almost atomic flat interfaces and amorphous structure.

2.3.2 Electrical properties of HfSiON gate stack on Ge

Inspired by the excellent properties of HfSiON on Si, we have investigated the possibility of applying HfSiON to Ge with surface nitridation by remote plasma technique.

Figure 2.4 (a) shows the frequency dependence of C-V characteristics of as-deposited HfSiON/nitridation/n-Ge PMOS capacitors. Unfortunately, the excellent properties of HfSiON on Si do not transfer to apply to Ge substrate. Ge MOS device showed severe stretch out and bumps near depletion regime, and severe frequency dispersion. The bumps near the inversion regime increase with decreasing measurement frequency implying that there exist some slow surface states near the valence band (E_v) for n-Ge.

As displayed in Figure 2.4 (b), after scanning from inversion to the accumulation condition, the C–V curve shifted along the positive axis during reverse scan as a consequence of electron trapping from the *n*-type Ge substrate injection. Very large hysteresis (around 0.64V at 1 MHz) indicating large amount of slow (or border) trap density was observed. The hysteresis occurs due to the gate bias at which electrons fill the traps being different from the point at which the electrons leave the trap and/or due to the difference between the capture and emission times of the border traps [9]. Previously reported studies from our group have suggested that the increased levels of trapping at Ge substrates which are negatively biased results from an interfacial gate stack alignment in which the conduction band offset energy between the Ge substrate and a native Ge

dielectric ITR is less than that of the conduction band offset energy (CBOE) between a Hf- or Zr-based high-*K* dielectric and the Ge substrate. This arrangement can lead to the formation of a potential well that localizes and confines electrons at the interface, and thereby accounts for high interfacial densities of negative trapped charge [10,11]. The density of these traps can be estimated by following equation,

$$Q_{ot} = \frac{C_{ox}\Delta V_{hyst}}{qA} \tag{2.2}$$

where ΔV_{hyst} is the magnitude of the hysteresis in the flat band condition. The determined Q_{ot} was ~2 x $10^{12}cm^{-2}$. The determined D_{it} of each Ge MOS capacitor was ~2.2 x 10^{12} $eV^{-1}cm^{-2}$ using the conductance technique. V_{fb}, V_{th}, net donor concentration, and EOT extract by NCSU-CVC version 7 were -0.603V, -1.766, 7.2 x 10^{17} cm^{-3} and 2.151 nm, respectively.

Figure 2.5 (a), (b), and (c) showed multi frequency C-V characteristics of Al/ HfSiON/nitridation/n-Ge PMOS capacitors as a function of annealing temperatures. The capacitance was measured at 1MHz and 100 kHz as a function of gate voltage and the capacitor was swept from inversion to accumulation at room temperature in the dark room. Regardless of annealing temperature, all of C-V curves shifted along the positive axis during reverse scan indicating electron trapping were observed. As can be seen in Figure 2.5 (b) and (c), hysteresis were reduced to 0.25V after 625 °C anneal, and clearly achieves a minimum value (0.12V) after 650 °C anneal. This reduction in hysteresis indicates improvement in gate dielectric characteristics as annealing temperature increased. The

determined Q_{ot} were 1.46 x 10^{12} cm^{-2} for 625 °C and 7.11 x 10^{11} cm^{-2} for 650 °C anneal respectively and they demonstrated minimum values at temperatures of 650 °C anneal. However, the opposite effect was observed after 700°C anneal (Figure 2.5 (c)). Hysteresis increased rapidly as the temperature increases above 700°C due to possible interaction of interfacial GeON with the HfSiON film at higher temperature annealing. Deteriorated electron trapping after high temperature annealing was attributed to Hf^{3+} states arising from oxygen divacancies clustered at grain boundaries and to Hf^{3+} and Ge^{3+} states caused by the interdiffusion of Ge into the films. The determined Q_{ot} was 3.2 x $10^{12}$$cm^{-2}$ for 700 °C anneal. For the high-*k* films fabricated by conventional processes, high-temperature PDA for as-deposited films is inevitable process to improve their electrical properties. However, it is well known that high-temperature process is very critical for the Ge MIS structures in respect to degradation of interfacial electrical properties [12]. The calculated slow trap density as a function of annealing temperature is graphically shown in Figure 2.6 (a). Thus, it is an important guide line for the selection of PDA range for the both low slow trap density and D_{it} for improved Ge based MOS device.

Using the conductance technique, the determined D_{it} of each Ge MOS capacitor as a function of annealing temperature were ~2.1 x 10^{12}, 7.1 x 10^{11}, 6.1 x 10^{11}, and 7.0 x 10^{11} $eV^{-1}cm^{-2}$ for as-deposited, 625 °C, 650 °C and 700°C respectively and graphically shown in Figure 2.6 (b).

For direct comparison, Figure 2.7 showed 1 MHz C-V curves for as-deposited and 650 °C annealed Ge MOS capacitors. Minimal stretch out and lowest hysteresis were obtained for 650 °C annealed device. It is found that the Ge nitride/Ge interface with 650 °C

annealing indicates significant reduction of slow trap density, while there is no significant improvement for reducing D_{it} between 625 °C, 650 °C and 700°C annealed devices. Furthermore, all of devices showed the kinks near the inversion regime reduce with increasing measurement frequency implying that there exist some "slow" surface states near the valence band (E_v) for n-Ge even though 650 °C annealed device showed significant reduction of slow trap density. Previously our group reported that the reactions between the Ge substrate and deposited high-*k* dielectrics, as-deposited and after annealing to 600–800 °C, Ge–O bonding into the high-*k* gate stacks which result in increased levels of conduction band edge defect states that incorporate these Ge atoms [10]. Therefore, it is clear that deteriorated electron trapping for 700 °C device as attributed to Ge incorporation into high-k dielectrics after 700 °C annealing. V_{fb}, and slow trap density and interface trap density as a function of annealing temperature were summarized in Table 2.1. Therefore, surface nitridation could not adequately enhance the Ge MOS performance even though significant improvement after 650 °C annealing; thus, alternative passivation technique, which can significantly reduce the interface traps and slow trap density, should be explored to achieve improved performance for Ge *n*-MOSFETs.

2.4 Summary

HfSiON ($(HfO_2)_{0.3}(SiO_2)_{0.3}(Si_3N_4)_{0.4}$) on Si has been investigated to demonstrate intrinsic properties of HfSiON for applying to Ge with surface nitridation by remote plasma. Electrical properties of HfSiON Si-MOS device are approaching state-of-the-art Si/SiO_2/metal gate stacks such as slow trap density of 1.24×10^{10} cm^{-2}, D_{it} of 5.7×10^{10} eV^{-1}cm^{-2}, fixed oxide

charge density of 4.67×10^{11} cm^{-2}, and very low leakage current level (5.2×10^{-8} A/cm^{-2}). Those excellent properties of HfSiON on Si do not transfer to apply to Ge substrate. HfSiON Ge-MOS device shows inferior electrical properties such as large hysteresis, severe stretch out, bumps near depletion regime, and severe frequency dispersion due to incorporation of Ge into gate dielectrics. All of devices showed the kinks near the inversion regime reduce with increasing measurement frequency implying that there exist some “slow” surface states near the valence band (E_v) for n-Ge even though 650 °C annealed device showed significant reduction of slow trap density. Therefore, alternative passivation technique should be explored to achieve improved performance for Ge MOSFETs.

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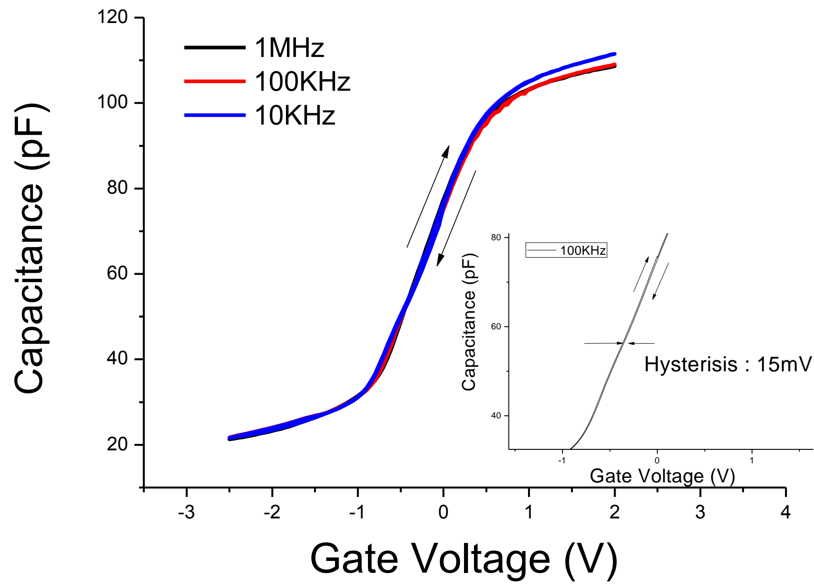
(a)



(b)

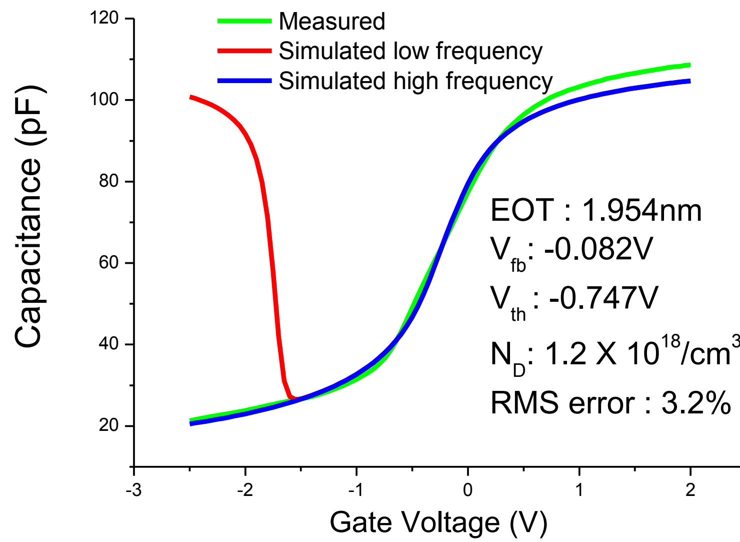
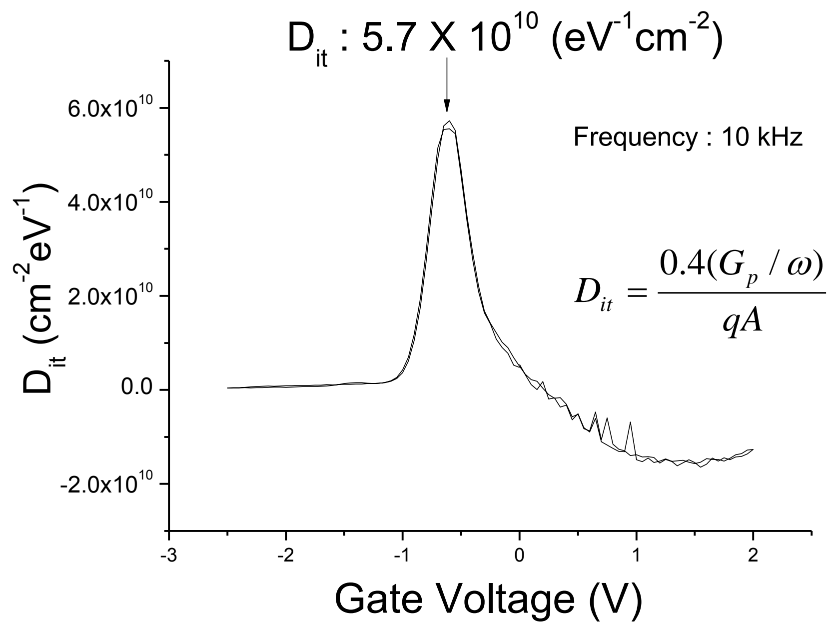


Figure 2.1 (a) the frequency dependence of C-V characteristics of as-deposited Al/HfSiON/RPN+RPO/n-Si PMOS capacitors. (b) Measured and calculated C-V curve of Al/HfSiON/RPN+RPO/n-Si PMOS capacitors.

(a)



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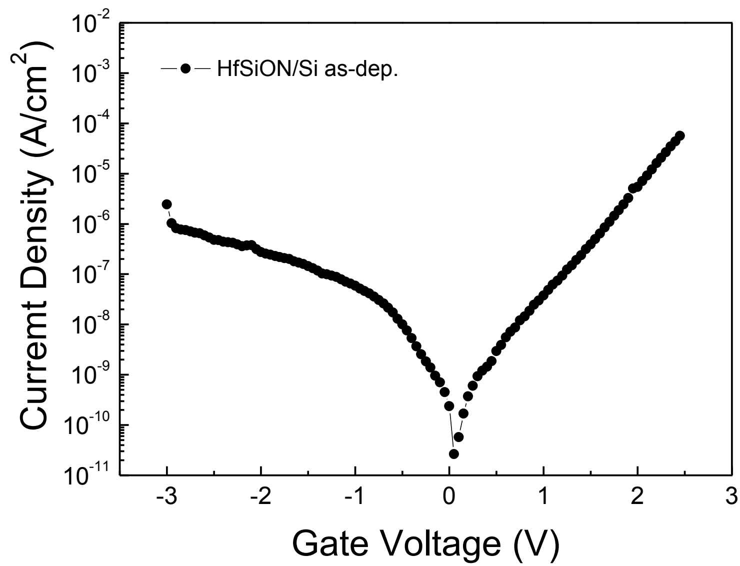


Figure 2.2 (a) interface trap density (D_{it}) as a function of gate bias for Al/HfSiON(5nm)/RPN+RPO/n-Si PMOS capacitors. (b) leakage current density of HfSiON PMOS capacitor.

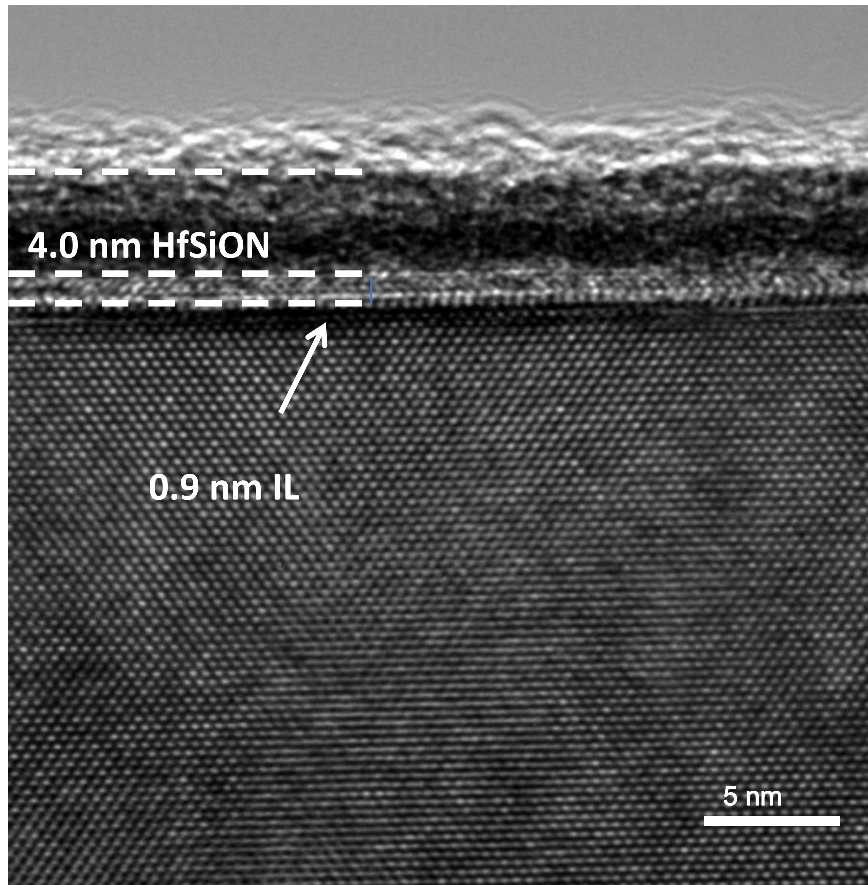
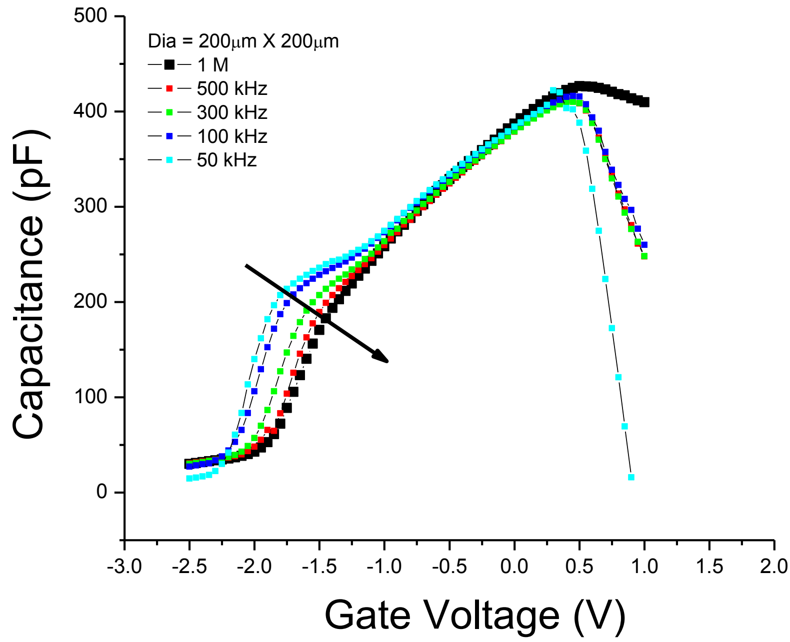


Figure 2.3 HRTEM result of HfSiON(4nm)/RPN+RPO/n-Si gate stack.

(a)



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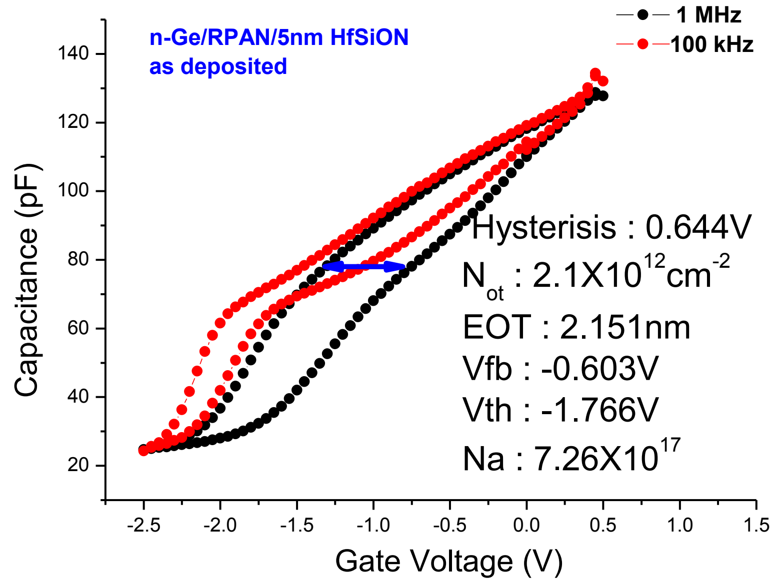
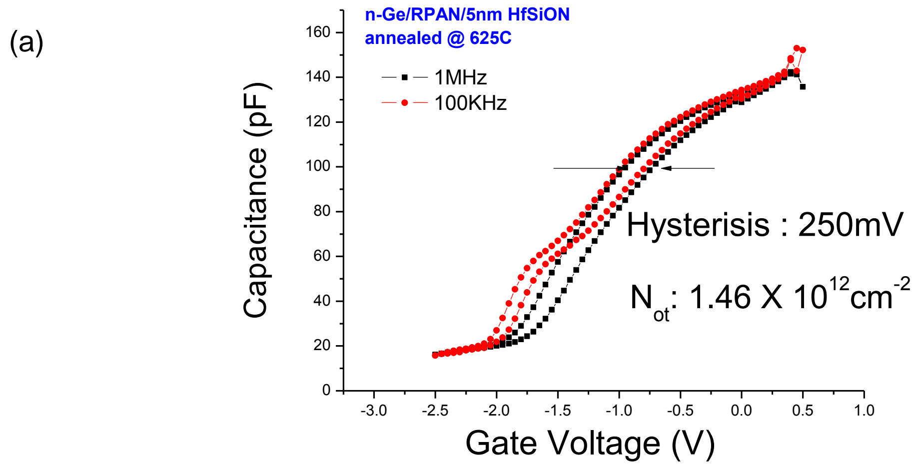


Figure 2.4. (a) the frequency dependence of C-V characteristics of as-deposited HfSiON /nitridation/n-Ge PMOS capacitors (b) Bidirectional of C-V characteristics of as-deposited HfSiON /nitridation/n-Ge PMOS capacitors.

(a)



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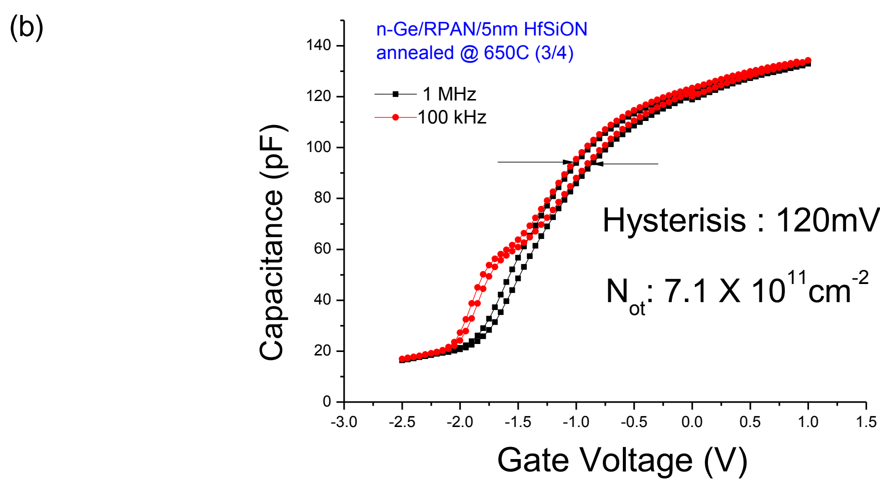


(c)

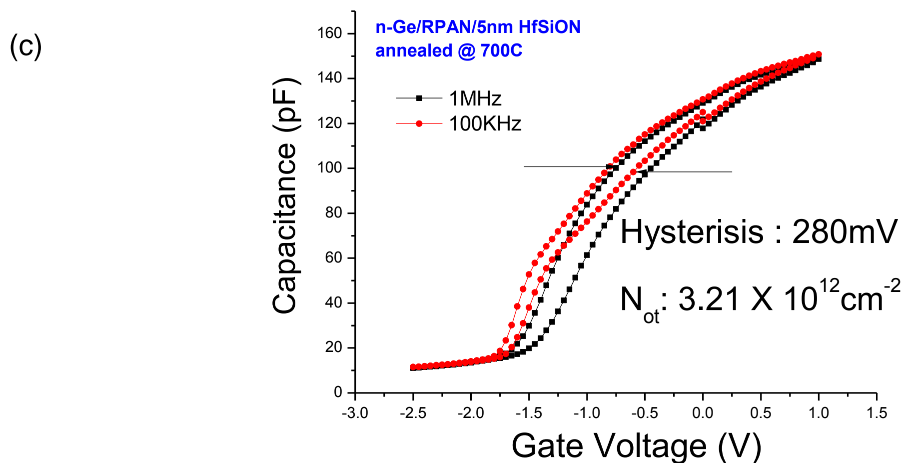
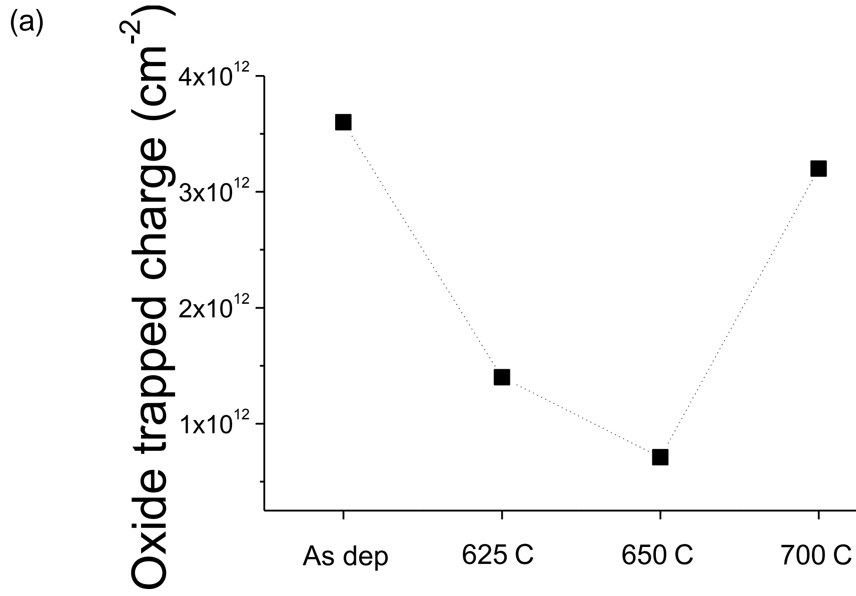


Figure 2.5. (a), (b), and (c) multi frequency C-V characteristics of Al/ HfSiON/nitridation/n-Ge PMOS capacitors as a function of annealing temperatures.

(a)



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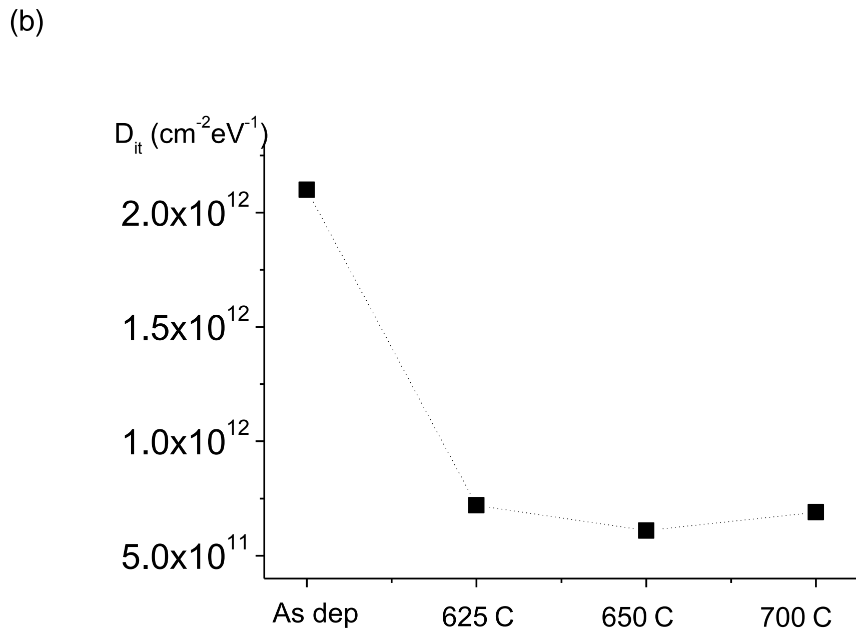

Figure 2.6. (a) the calculated slow trap density as a function of annealing temperature (b) the determined D_{it} of each Ge MOS capacitor as a function of annealing temperature using the conductance technique.

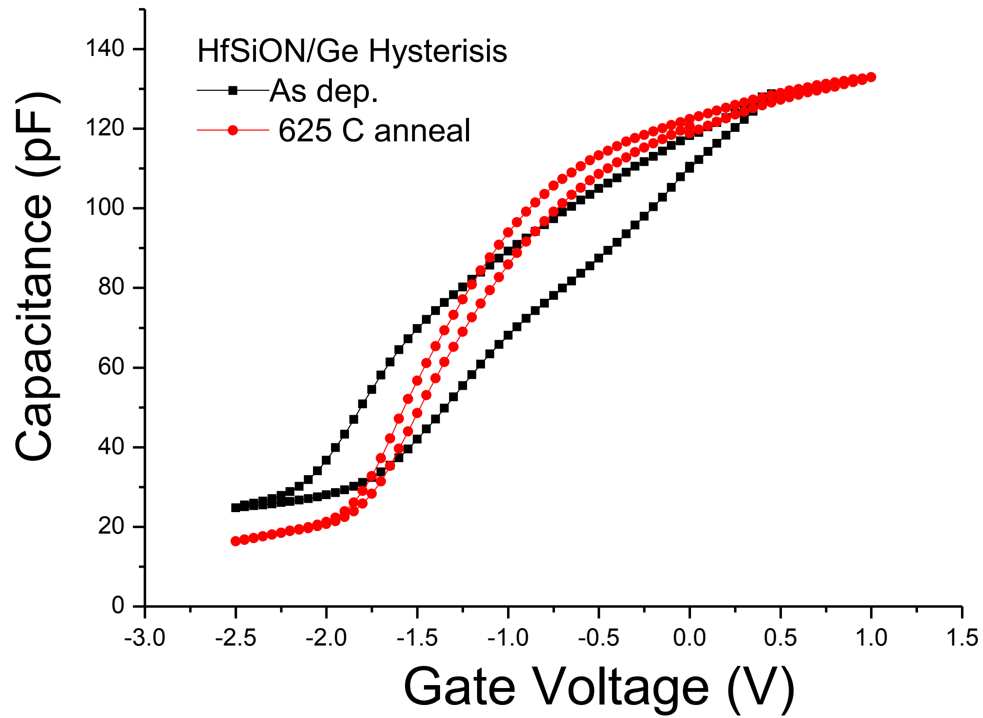

Figure 2.7 1 MHz C-V curves for as-deposited and 650 °C annealed Ge MOS capacitors

Table 2.1. Summary of electrical properties of Al/ HfSiON/nitridation/n-Ge PMOS capacitors as a function of annealing temperatures.

Sample	N_D (cm^{-3})	Hysteresis (V)	*Oxide trapped charge density(cm^{-2})*	*Interface trap density (D_{it}) (eV^{-1} cm^{-2})*
As dep	7.1×10^{17}	0.64	5.1×10^{12}	2.1×10^{12}
625 ℃		0.25	1.4×10^{12}	7.1×10^{11}
650 ℃		0.12	7.1×10^{11}	6.1×10^{11}
700 ℃		0.28	3.2×10^{12}	7.0×10^{11}

3 Investigation of pseudo-ternary HfSiON ($(HfO_2)_3(SiO_2)_3(Si_3N_4)_4$) with surface passivations on Ge

Abstract

The properties of HfSiON on Ge as a function of surface treatment are investigated in this chapter. To investigate the effect of surface passivation treatment on germanium, four types of surface passivation were employed: (1) 1nm of Si + RPAN (15 sec.), (2) 0.6nm of Si + RPAN (50 sec.), (3) 0.6 nm of Si + RPAN (15 sec.), and (4) RPAN (90 sec.). AES using a 3 keV electron beam was performed in the on-line analysis chamber to investigate wet chemical cleaning and the initial stage of formation of a thin “pseudomorphic” silicon layer (an order of 1nm) on the Ge surface. To investigate the chemical structure of the Si passivation layer after HfSiON deposition, high-resolution ex situ X-ray photoelectron spectroscopy (XPS) was performed with 260 and 650 eV soft X-ray excitation to provide some depth resolution. The elemental Si interlayer (Si^{0+} oxidation state, BE ~99.3 eV) is still present after oxide deposition. It is noteworthy that the combination of a pseudomorphic Si layer followed by nitridation yields a high quality passivation layer on Ge. A maximum hysteresis of 16 mV corresponding to a slow trap density of 7 x 10^{10} cm^2, a fixed oxide charge density of 2.2 x 10^{11} cm^2, and a D_{it} of 7 x $10^{11}cm^{-2}$ eV^{-1} were obtained for a Ge MOS capacitor with a pseudomorphic Si passivation layer. The leakage current density for the silicon passivated device was much lower under both accumulation and inversion biases

compared to other passivation approaches. This is closely related to the lower D_{it} level and slow state trap density of the Si passivated device, which suppresses trap assisted tunneling.

3.1 Introduction

Germanium has been spotlighted for an attractive channel material for future metal-oxide-semiconductor (MOS) field-effect transistors because its high intrinsic electron mobility (2X) and hole mobility (4X) as compared to the conventional channel material silicon [1,2]. However, it is difficult to integrate into a MOS fabrication process because GeO_2 has inferior properties such as poor thermal stability and water solubility [3]. One of the most critical issues is to achieve high quality of interface property for a high performance Ge based MOSFET, numerous passivation technologies such as GeO_2, Ge_3N_4 and GeO_xN_y have been widely studied [4-11]. Surface nitridation with NH_3 annealing prior to the high-K dielectric deposition has been demonstrated as a critical step to form high quality gate stack on Ge [12,13]. An alternative surface passivation technique using *in situ* SiH_4 annealing or solid source molecular beam epitaxy (SS-MBE) prior to High-k dielectric deposition was introduced since surface nitridation has a potential for mobility degradation and producing new slow-interface traps deep in the band gap [14,15]. However, both suppression of frequency dispersion in inversion regime at low frequency due to slow state trap density and negligible hysteresis have not been achieved in spite of all the efforts in previous studies on Ge based MOS capacitors.

In this chapter, pseudo-ternary HfSiON ($(HfO_2)_3(SiO_2)_3(Si_3N_4)_4$) with very thin (0.6nm and 1nm) pseudomorphic silicon passivation layer and with surface nitridation on n-type Ge (100) substrates by remote plasma enhanced chemical vapor deposition (RPECVD) are investigated. The initial silicon deposition kinetics and chemical composition of thin silicon layers were determined from analysis of on-line Auger electron spectroscopy (AES) features

associated with Ge and Si. High-resolution ex situ x-ray photoelectron spectroscopy (XPS) analysis using Al K_α radiation source was performed to investigate the chemical structure of the Si passivation layers. Also, the quality of interface and dielectric layers were investigated using fabricated Ge metal-oxide-semiconductor (MOS) capacitors.

3.2 Experimental Procedures

3.2.1 Ex-Situ Wet-chemical Cleaning

As received two-inch Germanium wafers, prior to loading into the UHV environments, were wet-chemically cleaned by modified NH_4OH based cleaning procedure which consists of the following steps:

(1)A rinse in running deionized (DI)-water for 5 min.

(2)A dip in H_2O_2 (6%) for 20 sec.

(3)A dip in methanol for 20 sec.

(4)A dip in NH_4OH (15%) in 30 sec.

(5)A rinse in DI-water for 60 sec.

The process was repeated from step (2) to (5) for two times to remove germanium oxide and contaminations. During the process, Teflon beakers and Teflon tweezers were used for wet chemical cleaning. Within a few minutes after being blown dry by dry nitrogen, the samples were loaded into a multi-chamber system, which provided a separate remote plasma-assisted process and on-line AES measurement [16]. AES using 3 keV electron beam was performed in the on-line analysis chamber to investigate the wet chemical cleaning and initial stage of thin pseudomorphic silicon layer on Ge surface.

3.2.2 Combination of pseudomorphic silicon layer and nitridation on Ge

Prior to deposition of high-k gate dielectrics, very thin (0.6nm and 1nm) pseudomorphic silicon layers were deposited onto n-type Ge (100) substrates at 300 °C by remote plasma enhanced chemical vapor deposition (RPECVD). To optimize pseudomorphic silicon layer deposition, a remote plasma assisted CVD with 2%-SiH_4 in He and He gases for 0 sec, 20 sec, 40 sec, and 60 sec were employed. The gas flow ratio of He and 2%-Si H_4 in He were 200 and 30 sccm respectively. The substrate temperature was 300 ^{o}C, process pressure was 0.2 torr, and plasma power was 30 W at 13.56 MHz. To investigate the initial stages of deposition of the pseudomorphic silicon layer on wet chemically cleaned Ge surface, the AES measurements using 3 keV electron beam was performed following each process step.

After pseudomorphic silicon layer deposition, the layer was exposed to reactive species from a remote N_2/He discharge at 0.3 torr for nitridation to provide chemical passivation to suppress further unwanted reaction between the deposited HfSiON gate dielectrics and the Ge substrates. The processing temperature was 300 ^{o}C, and RF power was 30 W at 13.56 MHz.

3.2.3 Device fabrication and electrical characterization

As shown in Figure 3.1, to investigate the effect of surface passivation treatment, four types of surface passivation were employed: (1) 1nm of Si + RPAN (15 sec.), (2) 0.6nm of Si + RPAN (50 sec.), (3) 0.6 nm of Si + RPAN (15 sec.), and (4) RPAN (90 sec.). After surface passivation treatment, HfSiON (4nm) layers were deposited on films onto n-Ge (100) substrates at 300 °C by remote plasma enhanced chemical vapor deposition (RPECVD).

The Si, Hf source gases, 2% SiH_4 in He, and Hf (IV) t-butoxide respectively, were delivered directly into the substrate region of a remote plasma reactor through two different injectors. An $N_2/N_2O/He$ mixture was subjected to remote plasma excitation at 30 W and 13.56 MHz and was employed to initiate RPECVD process.

For the fabrication of HfSiON MOS devices and electrical characterization studies, n-type Ge (100) with 5 x 10^{17} cm^{-3} to 2x10^{18} cm^{-3} was used in this chapter. The use of heavily doped Ge wafers reduces spreading resistance and thereby minimizes parasitic series resistance. After gate dielectric insulator deposition, a 500 nm Al layer was evaporated and defined by shadow mask. Forming gas anneal (FGA) for 30 minutes in a mixture of 10% H_2 in N_2 at 400°C was used to minimize D_{it}. This step was done before metallization in order to prevent reactions between the Al gate and the dielectric films. Electrical measurements were performed on a Material Development Corporation system. An HP 4284A LCR meter with a frequency range of 1 kHz to 1 MHz was used to perform capacitance-voltage measurements for capacitance dispersion. Current-voltage measurements were done on an HP 4140B voltage source with a pico-ammeter. Voltage-ramp rates were varied from dV/dt = 0.001V/sec to dV/dt = 0.05 V/sec. A slower ramp rate is preferred to reduce the displacement current, ensuring that the current measured is actually tunneling current. All electrical measurements were performed in the dark room and at room temperature.

3.3 Results and Discussion

As shown in Figure.3.2, as received Ge substrates showed native oxide and carbon contamination in AES spectra. After wet chemical clean of Ge substrates, any carbon peaks

(~at 272 eV) were not observed. This feature indicated the wet chemical clean was effective in removing carbon contamination from Ge substrate. However, oxygen Auger peak (~at 510 eV) was still observed, which was possibly due to oxidation after *ex-situ* chemical clean before loading samples into UHV chamber.

Figure 3.3 shows the time evolution of differential AES spectra for the Si layer deposition process of a Ge sample using 2%-SiH_4 in He and He plasma at 300 ^oC with plasma power of 30 W. This AES spectra illustrates from; (a) clean Ge, (b) 20 sec. (c) 40 sec. (d) 60 sec. Si layer deposition on Ge substrate. The intensity of Ge MVV peak (~52 eV) decreased while the intensity of Si LVV (~91 eV) which is mainly associated with Si-Si bonding in the Si layer increased with increasing deposition time. Note that Ge LMM features of sample in Figure 3.3 disappeared after 40 seconds deposition of silicon. These changes in relative intensity of Ge MVV and Si LVV are due to increase of the Si layer thickness wigith time.

Figure 3.4 displays an expanded Si LVV Auger regime from 60 to 130 eV as a function of deposition time. As the deposition proceeds, the intensity of Si LVV gradually increased whereas negligible peak shifts were observed. This suggests that Si-Si bond maintained during thick Si layer deposition and pseudomorphic silicon layer was successfully deposited on Ge surface. .

The kinetics of the pseudomorphic silicon layer process on Ge surface were determined by using AES analysis. Consider a uniform thin silicon layer on Ge substrate. Ge MVV and Si LVV AES intensities are given by [17],

$$I_{Si} = I^{o}{}_{Si} \exp\left(t_{ox} / \lambda_N\right) \tag{3.1}$$

$$I_{Ge} = I^{o}{}_{Ge}\left[1 - \exp\left(t_{ox} / \lambda_{O}\right)\right] \tag{3.2}$$

where, $I^{o}{}_{Ge}$ = Ge MVV Auger electron intensity from the clean Ge substrate,

$I^{o}{}_{Si}$ = Si LVV Auger electron intensity from the thick Si layer,

I_{Ge} = Ge MVV Auger electron intensity from the thin Si layer,

I_{Si} = Si LVV Auger electron intensity from the thin Si layer,

λ_{Ge}= Inelastic mean free path of Ge Auger electron (~52 eV)

Figure 3.5 illustrates three samples: (a) clean Ge substrate, (b) relatively thick Si, and (c) thin Si layer on Ge substrate. In this study, wet chemically cleaned Ge as described in 3.2.1 was used as a clean Ge for $I^{o}{}_{Ge}$, and He and 2%-SiH_4 in He plasma deposited Ge sample (300 ^{o}C, 0.2 torr, 30 W and 1 min) was used as a relatively thick Si layer for $I^{o}{}_{Si}$, respectively. Negative-peak to-background intensities instead of peak-to-peak intensity were used for quantification, because the effects of peak shape changes, associated with changes in the energy loss structure of the matrix, are removed by using the negative-peak-to-background Auger intensity instead of the peak-to-peak intensity [17]. Figure 3.3 shows AES spectra from: (a) clean Ge, (b) 20 sec., (c) 40 sec., and (d) 60 sec. Si layer deposition on Ge substrate. Using Eq. (3.1) and (3.2), we obtain the following equation,

$$t = \lambda_{Ge} \ln\left(1 + \frac{I^{o}{}_{Ge}}{I^{o}{}_{Si}} \times \frac{I_{Si}}{I_{Ge}}\right) \tag{3.3}$$

Using this Auger intensity ratio and Eq. (3.3), we can then estimate a Si layer thickness on the Ge surface.

Figure 3.6 shows the silicon thickness versus the deposition time for the Si layer deposition process. Like a typical deposition process, the thickness of Si layer increased linearly as deposition time increased. A 60 seconds deposition forms approximately 1.6 nm of pseudomorphic Si on the Ge substrate.

To investigate the chemical structure of Si passivation layer, high-resolution ex situ x-ray photoelectron spectroscopy (XPS) analysis using Al Kα radiation source was performed for the HfSiON (2nm)/RPN+Si (1nm)/n-Ge sample.

As shown in Figure 3.7, the depth resolution of measurement is indicated in the Si 2p spectra measured for HfSiON (2nm)/ RPN+Si (1nm)/ n-Ge sample with 260 and 650 eV soft x-ray. We observed distinct Si 2p peaks from both the HfSiON overlayer (Si^{4+} oxidation state, binding energy, BE~102 eV) and the elemental silicon (Si^{0+} oxidation state, BE ~99.3 eV) interlayer in case of 650 eV photon energy which is more sensitive to interfacial layer (See the red line). However, no distinct Si^{0+} (or Si^{1+} and Si^{2+} state) state was observed in case of 260 eV photon energy which is more sensitive to surface of oxide layer (see the black line). A full width at half maximum (FWHM) values, 1.82 for 260 eV and 1.9 eV for 650 eV of Si $2p^{4+}$ were obtained after high-k oxide deposition. It is clear that the elemental silicon interlayer is still present after oxide deposition. However, Hong *et al.* reported that no apparent Si–Si peak at 99.8 eV was observed after Al_2O_3 deposition, indicating that silicon layer deposited by SSMBE was fully oxidized to form SiO_x on Al_2O_3 /4 ML Si/Ge sample [18].

Figure 3.8 exhibits XPS Ge 3d spectra for HfSiON (2nm)/RPN+Si (1nm)/ n-Ge. To clarify the peak position and the contribution of the Hf 5p peak, the Ge 3d peak intensities are normalized by Hf 4f peak intensities. The dotted lines indicate the peak position for GeO

(+1.4 eV shift vs Ge^{0+}), Ge_3N_4 (+2.0 eV), GeO_2 (+3.2 eV), as reported in the literature [19,20]. Ge^{0+} oxidation state (29.2 eV) which is related to Ge bulk was clearly observed. The Hf 5p peak which shifts higher BE by around 3.9 eV was observed at a binding energy of approximately 33 eV. To confirm the origin of Hf peak, SiO_2 with the same surface treatment (1nm Si+nitridation) on Ge sample (SiO_2/RPN+Si(1nm)/n-Ge) was estimated by XPS. As shown in Figure 3.9, negligible GeO_2 peak intensity and presence of various oxidation states (Ge^{2+}, Ge^{3+}, and Ge^{4+}) were observed. The results above indicate the effectiveness or success of pseudomorphic Si passivation step in suppressing subcutaneous oxidation during dielectric deposition. Therefore, the origin of the peak which shifts higher BE (Δ 3.9 eV) from Ge^{0+} was due to Hf 5p even though GeO_2 might be formed at Ge substrate caused by harsh oxidizing environment by PRECVD or air exposure.

The effects of interface treatment on the quality of the interface and the dielectric layer were investigated using as-deposited Ge PMOS capacitors. As shown above (Figure 3.1), these dielectric stacks can be classified into four categories, namely;

(1) Sample1 (SP1): 0.6nm of Si + RPAN (50 sec.),

(2) Sample2 (SP2): 1nm of Si + RPAN (15 sec.),

(3) Sample3 (SP3): 0.6 nm of Si + RPAN (15 sec.),

(4) Sample3 (SN): RPAN (90 sec.)

In order to optimize the intrinsic properties of each surface treatment, as-deposited MOS devices (without anneal) were employed in this chapter. Figure 3.10 shows the frequency dependence of C-V characteristics of Ge PMOS capacitors. The capacitance was measured at various frequencies as a function of gate voltage and the capacitor was swept from

inversion to accumulation at room temperature in the dark room. , As seen in Figure 3.10 (a) and (b), on both SN and SP1 MOS devices, large kinks near the inversion regime and stretch-out which is attributable to high density of interface states could be similarly observed (i.e. interface states respond to lower frequency and generate extra capacitance, thus the CV stretch-out). The kinks near the inversion regime reduce with increasing measurement frequency implying that there exist some "slow" surface states near the valence band (E_v) for n-Ge and the conduction band (E_c) for p-Ge [21]. This phenomenon has been previously observed in ZrO_2/Ge *n*-type MIS and it has been attributed to an increase in minority carrier generation due to diffusion of impurities from the dielectric into the substrate or to the interaction of interface slow states [22]. However, no matter what the nature of the traps is, compared to SN and SP1 devices, significantly reduced interface state densities and minimized minority carrier response are obtained at the HfSiON and Ge interface by 1nm of Si layer and plasma nitridation interface formation (SP2) by remote plasma deposition with 2% SiH_4 /He. As displayed in Figure 3.10 (c), the C-V curve of SP2 device shows no kinks in depletion at all measured frequencies 30 kHz–1 MHz and no stretch-out, which suggests that SP2 gives a lower density of interface states (D_{it}) than does SN and SP1. Interestingly, even the SP1 device has approximately same thickness of interfacial layer (around 1nm), thinner Si layer of SP1 device exhibited large kinks near the inversion regime and stretch out. Previous reports on Ge MOS devices reveal that abnormal inversion regime capacitance in Ge MOS devices is generally considered to originate from a much shorter minority carrier response time and higher minority carrier generation-recombination rate, due to the smaller band gap of Ge. However, in many previous reports

on Ge MOS devices, frequency dispersion in the inversion regime is not unique and seems to depend on process conditions. This fact suggests that the minority carrier generation is caused not only by intrinsic thermal excitation across the Ge band gap but also by another excitation process, such as defect-assisted band tunneling. Therefore, it is clear that the introduction of a silicon passivation layer by RPECVD results in reduced interface state densities and minimized minority carrier generation [23].

However, the SP2 device still exhibits a small frequency dependent flat band voltage shift (~0.2 V), which is usually observed in Ge or GaAs MOS. This is the direct result of interface states. In case of *P*MOS capacitors, this phenomenon is the indication of the weak Fermi-level pinning near the conduction band [24]. At high frequency (1 MHz), the density interface traps in the upper half of band gap results in a positive C-V shift due to filling of acceptorlike interface states with gate voltage is increasing. When the frequency decreases (i.e., 100 kHz to 30 kHz), some of the traps can respond to the gate voltage and contribute to an additional capacitance, giving an illusion that V_{fb} shifts toward the negative direction. V_{fb} , net donor concentration, and EOT extract by NCSU-CVC version 7 were -0.26V, 1.69 x 10^{18} cm^{-3}, and 1.623 nm for SP2 device, respectively. For the direct comparison, Figure 3.11 shows the normalized C-V (C/C_{ox}) at 1 MHz for each MOS capacitors. It is clearly observed that no kinks and very steep C-V curve were achieved on SP2 device. The steep slopes of the C-V curves suggest a rather low concentration of traps localized at the oxide and substrate interface. It is noted that the normalized C-V traces of SP and SP2 gate stacks revealed severe stretch out and the negative V_{fb} shift, due to large amount of positive fixed charge density (N_f). The shift of the flat band voltage from the position for the ideal V_{fb} is

caused by the generation of oxide defects close to the interface region. These are positively charged, as indicated by the negative shift direction [25].

In order to estimate the fixed oxide charge density (N_f), N_f was evaluated by following equation,

$$N_f = \frac{C_{ox}(V_{fb,ideal} - V_{fb})}{qA} \tag{3.4}$$

where work function difference (Φ_{ms}) (or ideal flat band voltage) between Al gate and n-Ge substrate was calculated by following equation,

$$V_{FB,ideal} = \phi_M - (x_n + \frac{E_g}{2} - \phi_F) \tag{3.5}$$

where Φ_m is metal work function, X_n is electron affinity in Ge, E_g is Ge energy band gap, and $\phi_F = \frac{kT}{q} \ln \frac{N_D}{n_i} = 0.254V$

The calculated Ideal flat band voltage ($V_{fb,\ ideal}$) for our devices was around -0.023 V for Al and n-Ge substrate and the calculated N_f values are also given in Table 3.1.

The determined N_f of each Ge MOS capacitor of (i) SN, (ii) SP1, and (iii) SP2 surface treatment was ~1.2 x 10^{12}, ~2.5 x 10^{11}, and ~2.2 x 10^{11} cm^{-2}, respectively.

To estimate hysteresis for devices, the capacitance was measured at 1 MHz as a function of gate voltage and the capacitor was swept from inversion to accumulation and back. As shown in Figure 3.12 (a) and (b), very large hysteresis (around 0.64V for SN and 0.41 V for the SP1 device) were observed at 1 MHz. In addition, this was found across the

entire frequency range (not shown). After scanning from inversion to the accumulation condition, the *C–V* curve shifted along the positive axis during reverse scan as a consequence of electron trapping from the *n*-type Ge substrate injection. However, as shown in Figure 3.12 (c), the retrace on the 1 MHz curve of SP2 sample shows only 16mV of hysteresis indicating that drastically reduce a slow trap density. Around 15 to 16 mV of hysteresis were found across the entire frequency range.

The density of these traps can be estimated by following equation,

$$Q_{ot} = \frac{C_{ox}\Delta V_{hyst}}{qA} \tag{3.6}$$

where ΔV_{hyst} is the magnitude of the hysteresis in the flat band condition.

As graphically shown in Figure 3.13 (a), the determined Q_{ot} of each Ge MOS capacitor of (i) SN, (ii) SP1, and (iii) SP2 surface treatment was ~2 x 10^{12}, ~8 x 10^{11}, and ~7 x 10^{10} cm^{-2}, respectively. Delabie *et al.* reported that around 900 mV of hysteresis was observed on p-Ge/GeO_x /HfO_2 MOS device even though the density of interface states estimated from conductance measurements as a function of frequency was about 3 x10^{11} cm^{-2} eV^{-1} [26]. It is noteworthy that the maximum hysteresis of 16 mV is extremely small for Ge MOS systems suggesting that the combination of a pseudomorphic Si layer with nitridation results in a high quality passivation layer on Ge surface. *G–V* measurements were employed as simple methods to qualitatively evaluate the Ge-passivation interface after the different

passivation treatments for the various gate stacks. Using the conductance technique interface state densities could be extracted using Eq. (3.7) [27].

$$D_{it} = \frac{0.4(G_p / \omega)}{qA} \tag{3.7}$$

where G_p is the peak conductance.

The extracted values of D_{it} are given in Table 3.1 and shown graphically in Figure 3.13 (b). The determined D_{it} of each Ge MOS capacitor of (i) SN, (ii) SP1, and (iii) SP2 surface treatment was ~2.2 x 10^{12}, ~1.1 x 10^{12}, and ~7.1 x 10^{11} $eV^{-1}cm^{-2}$, respectively. These results suggested that the electrical quality of the obtained 1nm of Si and nitridation/Ge interface is excellent, compared with other passivation/Ge interfaces.

The typical gate leakage density as a function of voltage bias for SN and SP2 devices is shown in Figure 3.14 for direct comparison. Through a direct gate voltage bias sweeping, the characteristic leakage phenomena were observed with a symmetric leakage level at both positive and negative bias polarities. Leakage current density level for SN device was much higher under both the gate bias conditions corresponding to the accumulation and inversion mode. This is closely related to the higher D_{it} level and slow state trap density of SN device thus enhanced trap assisted tunneling current of SN sample. There is clear evidence that large hysteresis of SN device is responsible for large amount of electron trapping and kink in the inversion regime due to slow trap density and/or abnormal near inversion regime

capacitance increase (possibly due to generation and recombination through bulk trap level) as described above.

3.4 Summary

In this chapter, the properties of HfSiON on Ge as a function of surface treatments are investigated. AES using a 3 keV electron beam was performed in the on-line analysis chamber to investigate the wet chemical cleaning and the initial stage of thin pseudomorphic silicon layer (an order of 1nm) on the Ge surface. The elemental Si interlayer (Si^{0+} oxidation state, BE ~99.3 eV) is still present after oxide deposition. It is noteworthy that the combination of a pseudomorphic Si layer followed by nitridation yields a high quality passivation layer on Ge. A maximum hysteresis of 16 mV corresponding to a slow trap density of 7 x 10^{10} cm^2, a fixed oxide charge density of 2.2 x 10^{11} cm^2, and a D_{it} of 7 x $10^{11}cm^{-2}$ eV^{-1} were obtained for a Ge MOS capacitor with a pseudomorphic Si passivation layer. The leakage current density for the silicon passivation device was much lower under both accumulation and inversion biases compared to other passivation approaches. This is closely related to the lower D_{it} level and slow state trap density of the Si passivation device, which suppresses trap assisted tunneling.

3.5 References

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Device structure with various surface treatment on n-Ge

1) SN : RPAN/n-Ge

2) SP1 : RPAN(50s)+Si(0.6nm)/n-Ge

3) SP2 : RPAN(15s)+Si(1nm)/n-Ge

4) SP3 : RPAN(15s)+Si(0.6nm)/n-Ge

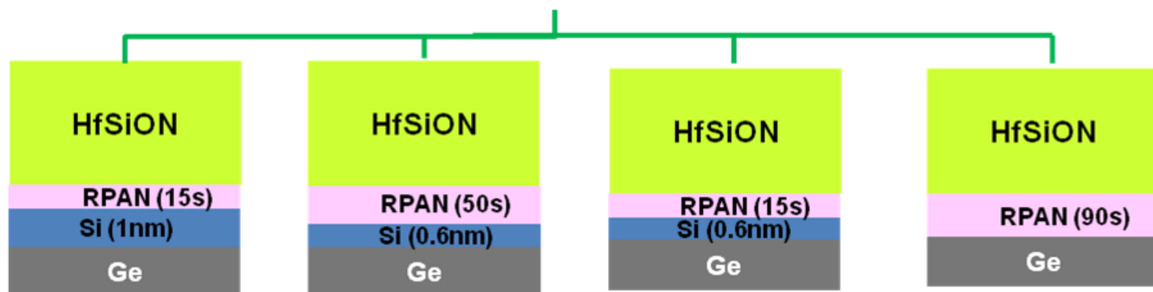


Figure 3.1. The effects of interface treatment on the quality of interface and dielectric layer were investigated using as-deposited Ge PMOS capacitors. These dielectric stacks can be classified into four categories, namely; 1) SP1 : 0.6nm of Si + RPAN (50 sec.), 2) SP2 : 1nm of Si + RPAN (15sec.), 3)SP3 : 0.6 nm of Si + RPAN (15sec.), and 4) SN : RPAN (90 sec.)

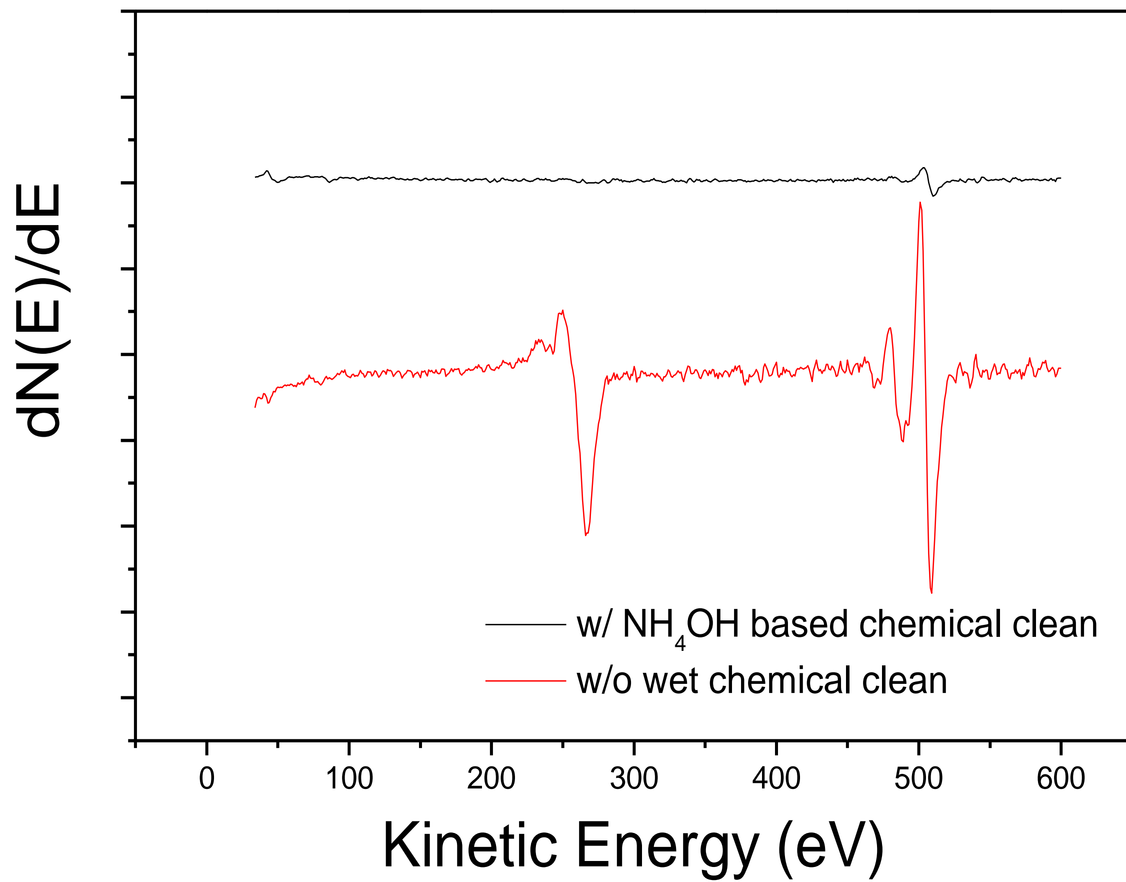


Figure 3.2. Differential AES spectra for the NH4OH based chemical clean of Ge substrate.

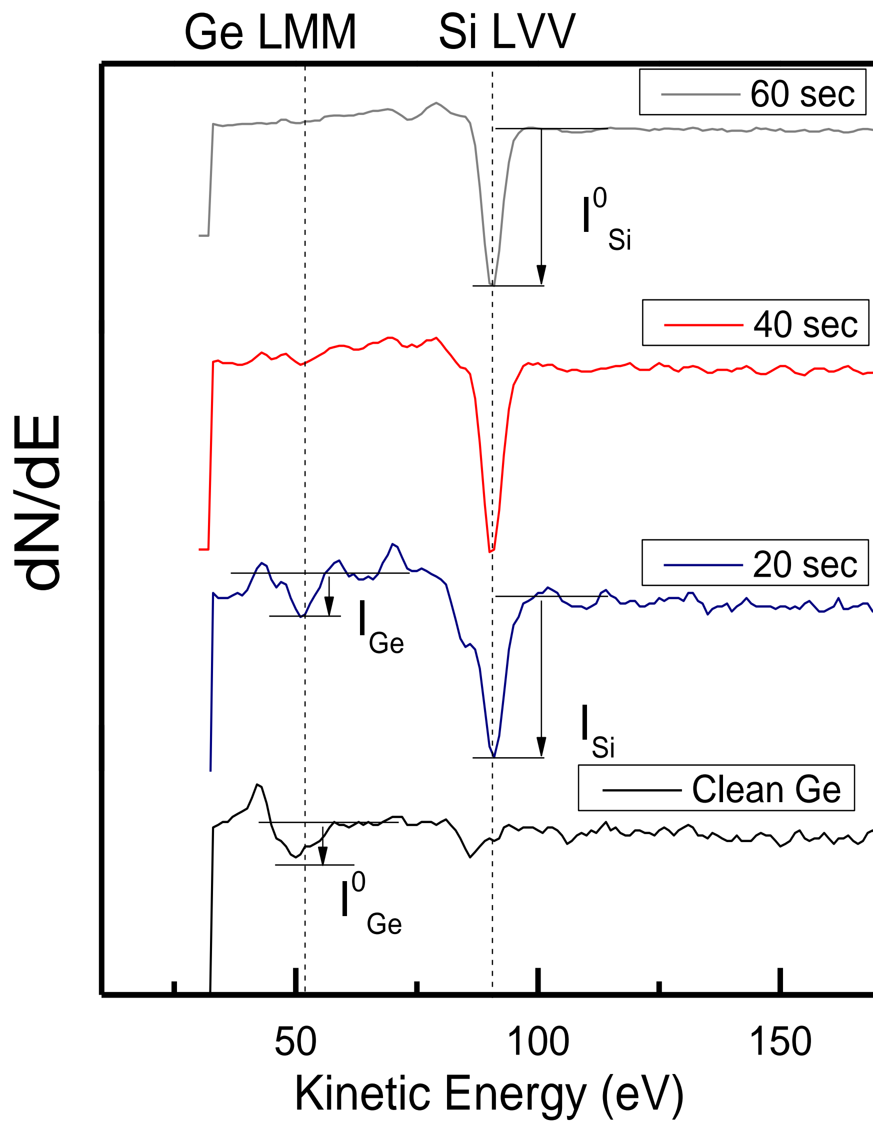


Figure 3.3. The time evolution of differential AES spectra for the Si layer deposition process of Ge sample using 2%-SiH_4 in He and He plasma at 300 ^oC with plasma power of 30 W. This AES spectra illustrates from; clean Ge, 20 sec., 40 sec., and 60 sec. Si layer deposition on Ge substrate.

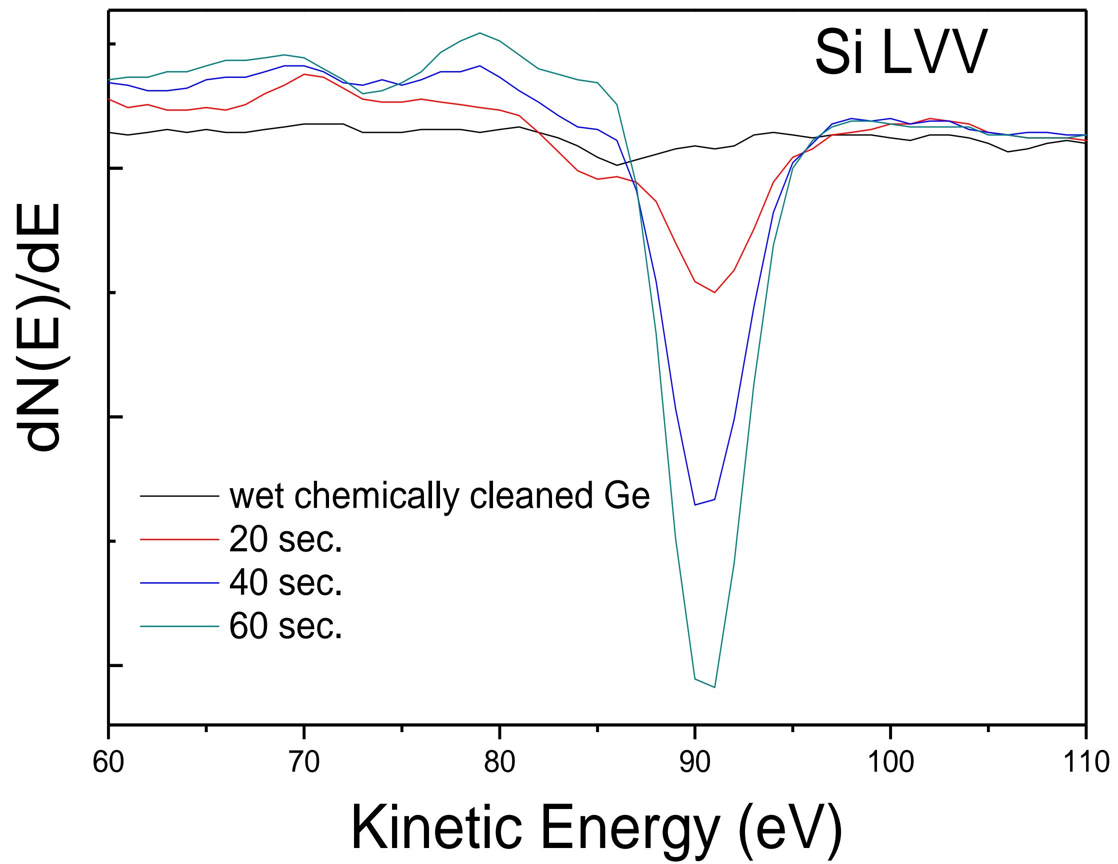


Figure 3.4. An expanded AES sepectra Si LVV Auger regime from 60 to 130 eV as a function of Si layer deposition the process time.

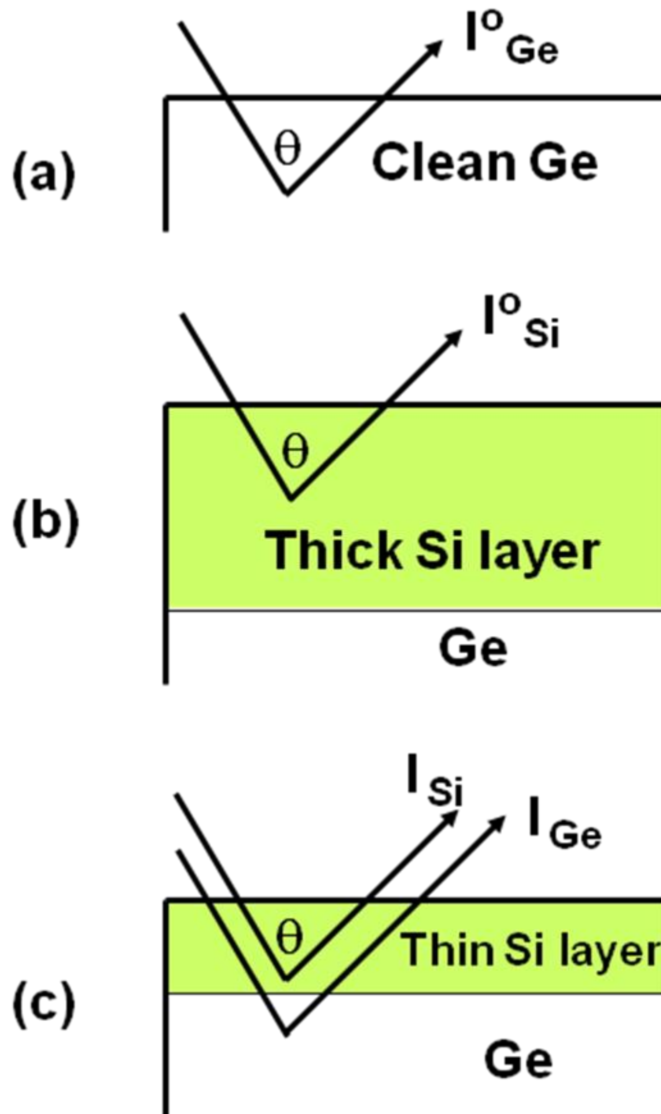


Figure 3.5. Schematic representation of three samples; (a) clean Ge substrate, (b) thick pseudomorphic silicon layer and (c) thin thick pseudomorphic silicon layer on Ge substrate. I^{o}_{Ge} (I_{Ge}) is Ge MVV Auger electron intensity from the clean Ge substrate (or from the Ge substrate with thin silion layer). I^{o}_{si} (I_{si}) is Si LVV Auger electron intensity from the thick Si layer (or from the thin silicon layer).

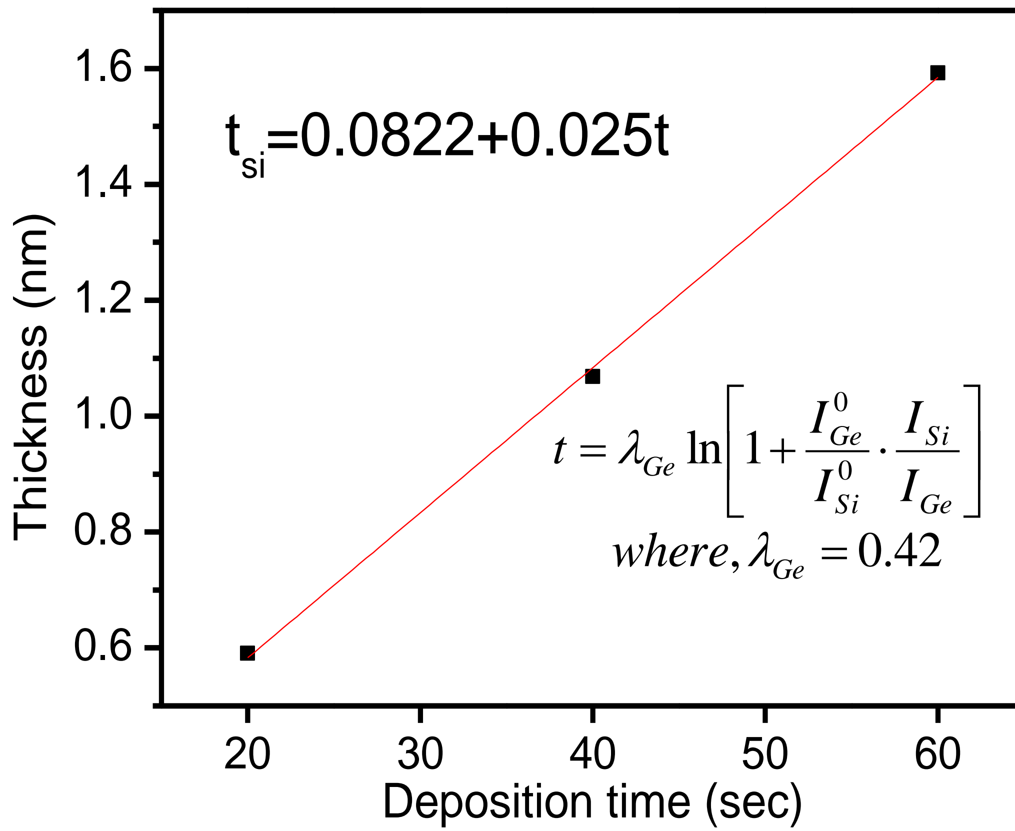


Figure 3.6. The silicon thickness versus the deposition time for the Si layer deposition process on Ge substrate .

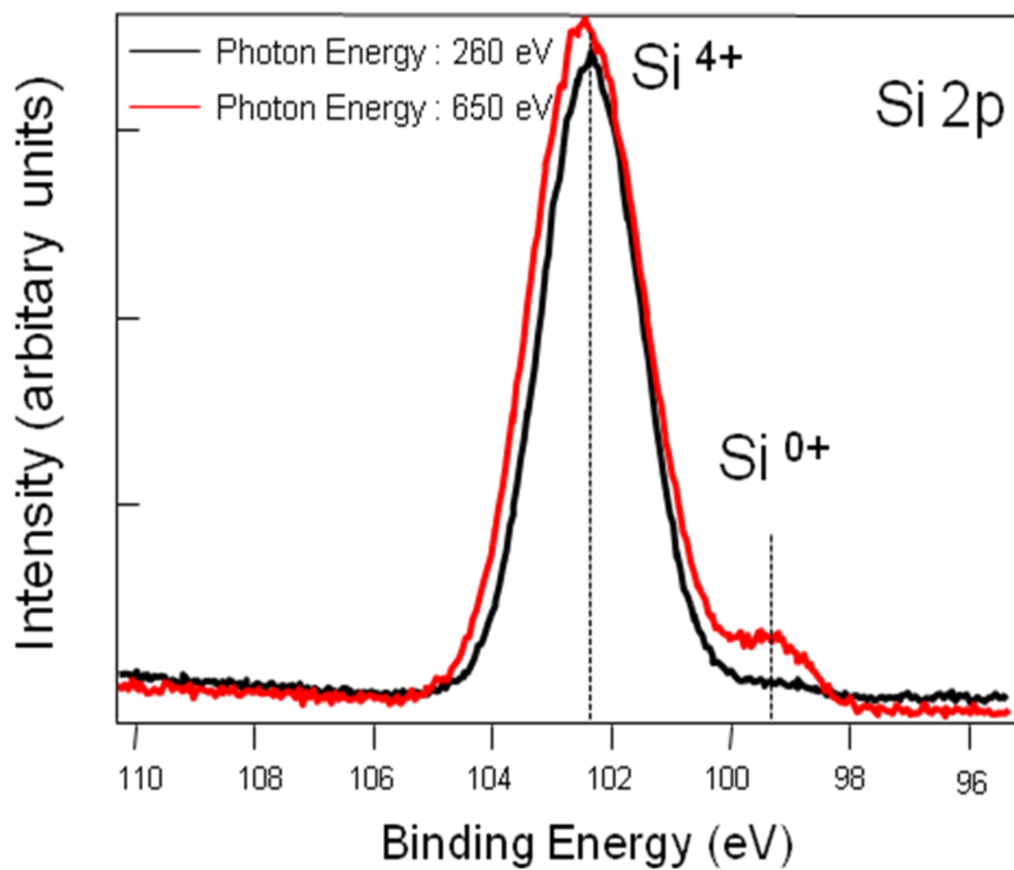


Figure 3.7. The depth resolution of Si 2p spectra for HfSiON (2nm)/ RPN+Si (1nm)/ n-Ge sample with 260 and 650 eV soft x-ray.

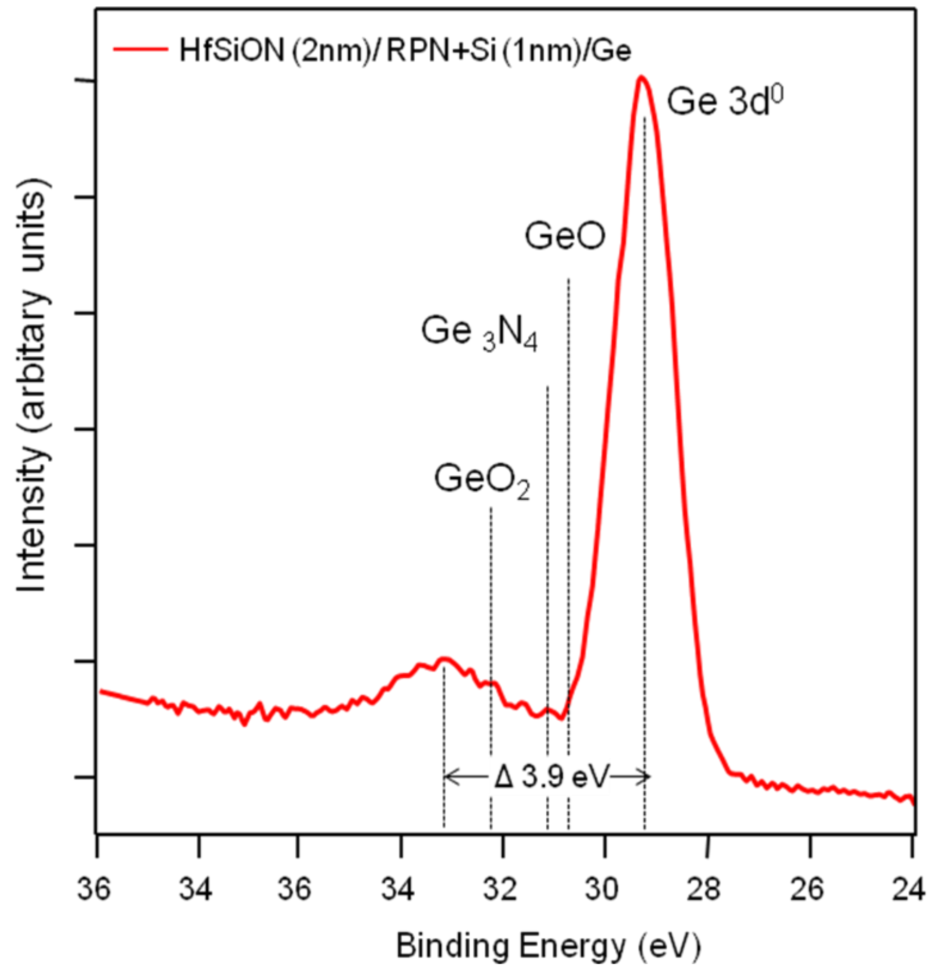


Figure 3.8. XPS Ge 3d spectra for HfSiON (2nm)/RPN+Si (1nm)/ n-Ge. The dotted lines indicate the peak position for GeO (+1.4 eV shift vs Ge^{0+}), Ge3N4 (+2.0 eV), GeO_2 (+3.2 eV), as reported in the literature.

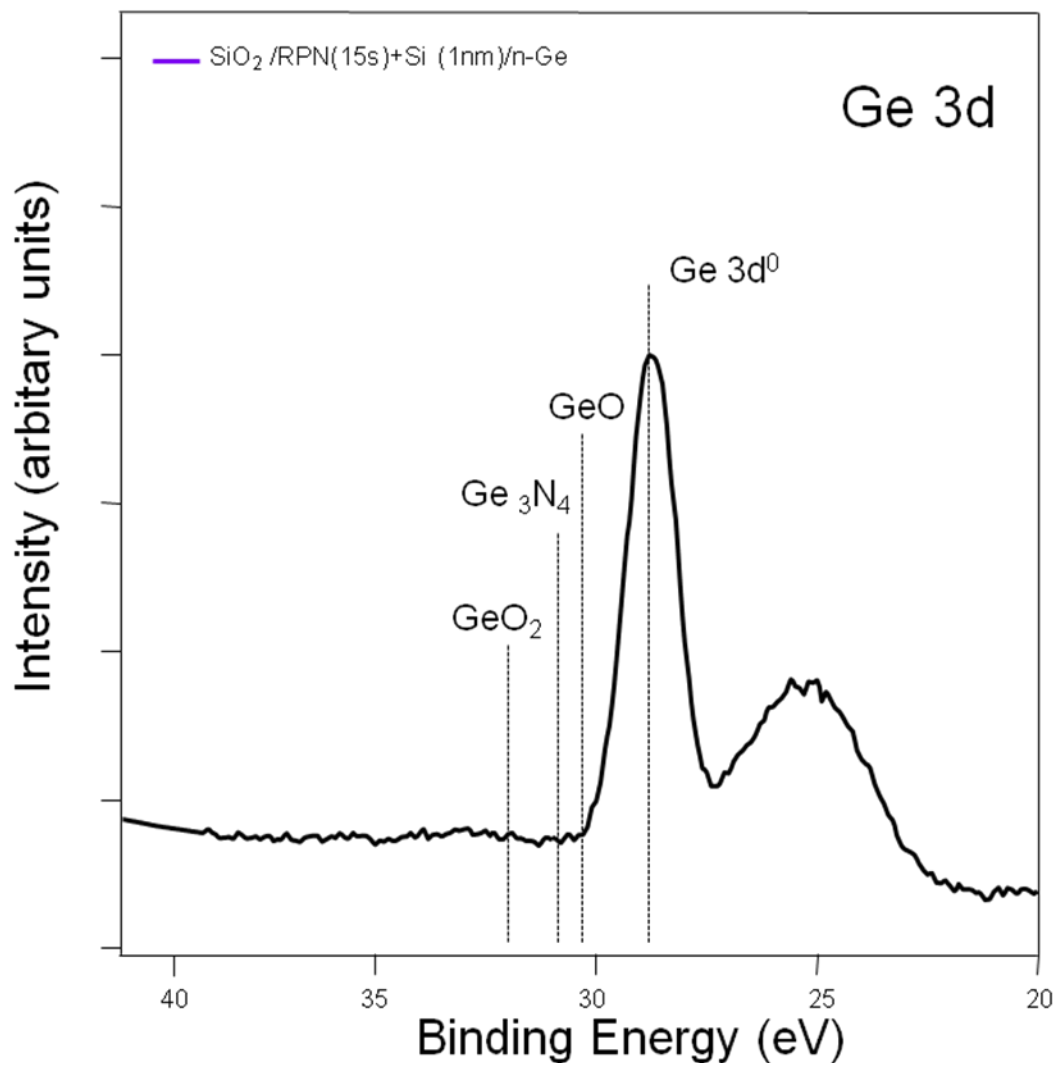
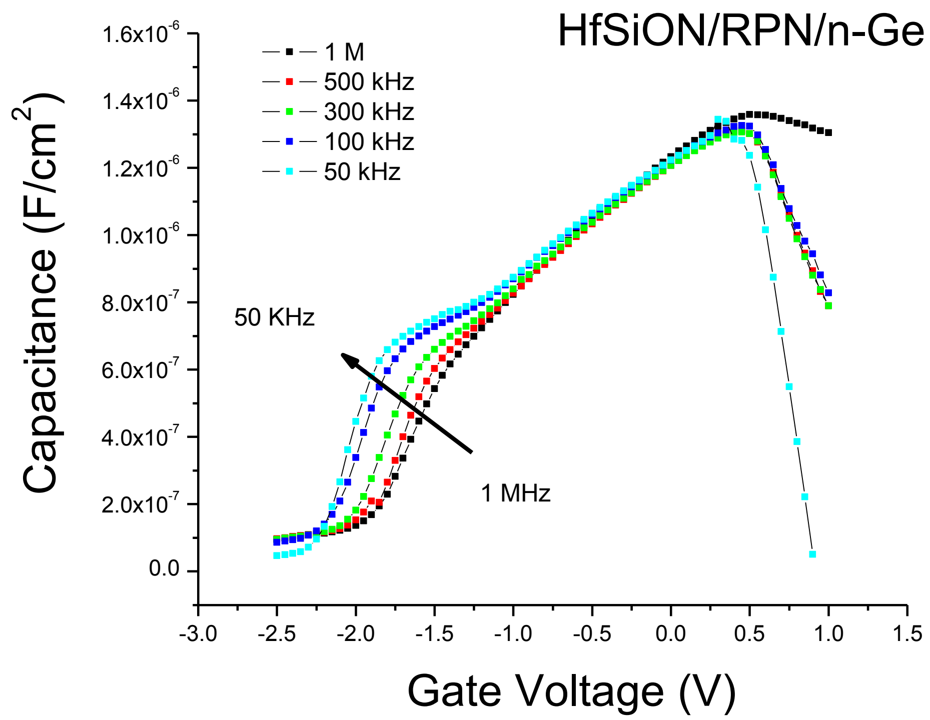


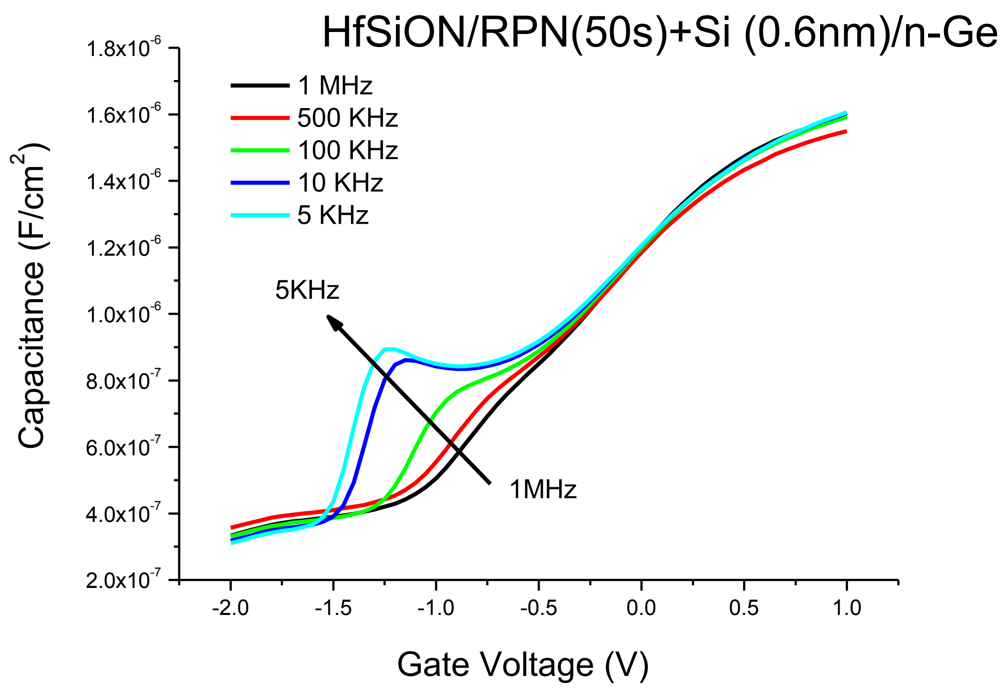
Figure 3.9. Ge 3d spectra for SiO_2/RPN+Si (1nm)/ n-Ge

Figure 3.10. Frequency dependence of C-V characteristics of Ge PMOS capacitors for (a) RPN device, (b) RPN (50s)+si(1nm), and (c) RPN (15s)+Si (1nm) treatment respectively.

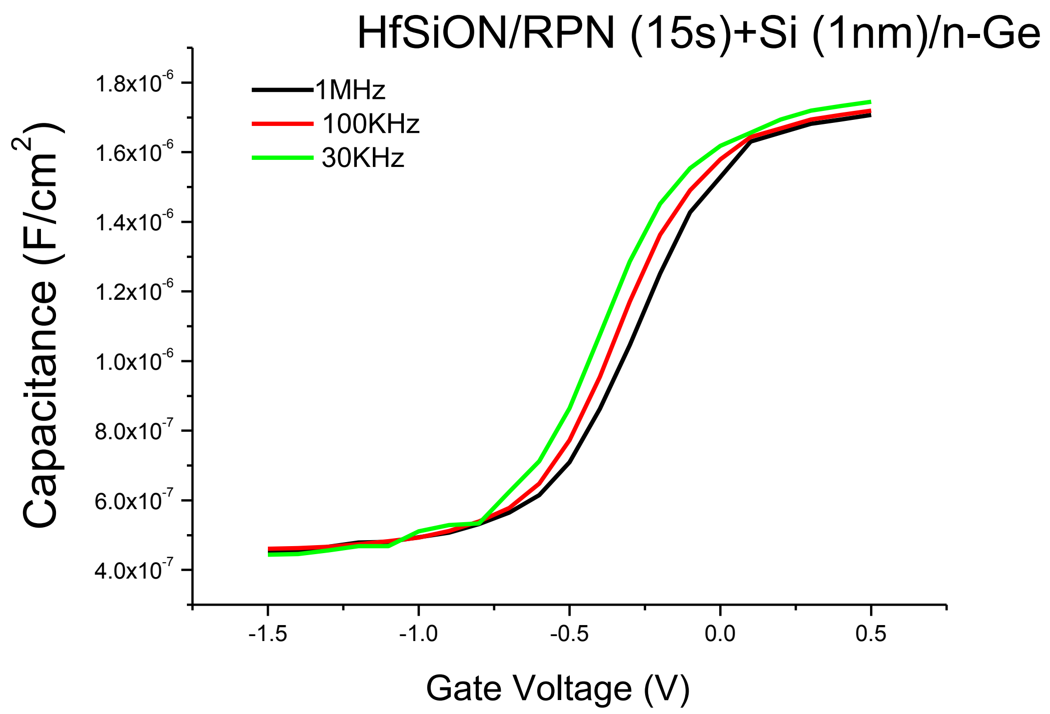
(a)



(b)



(c)



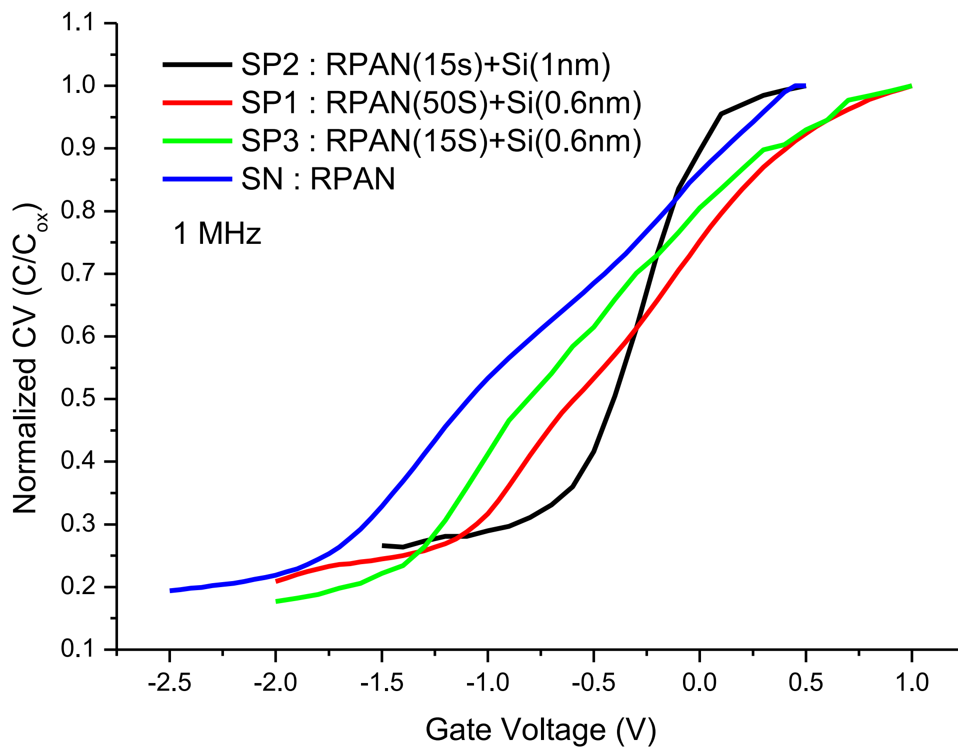
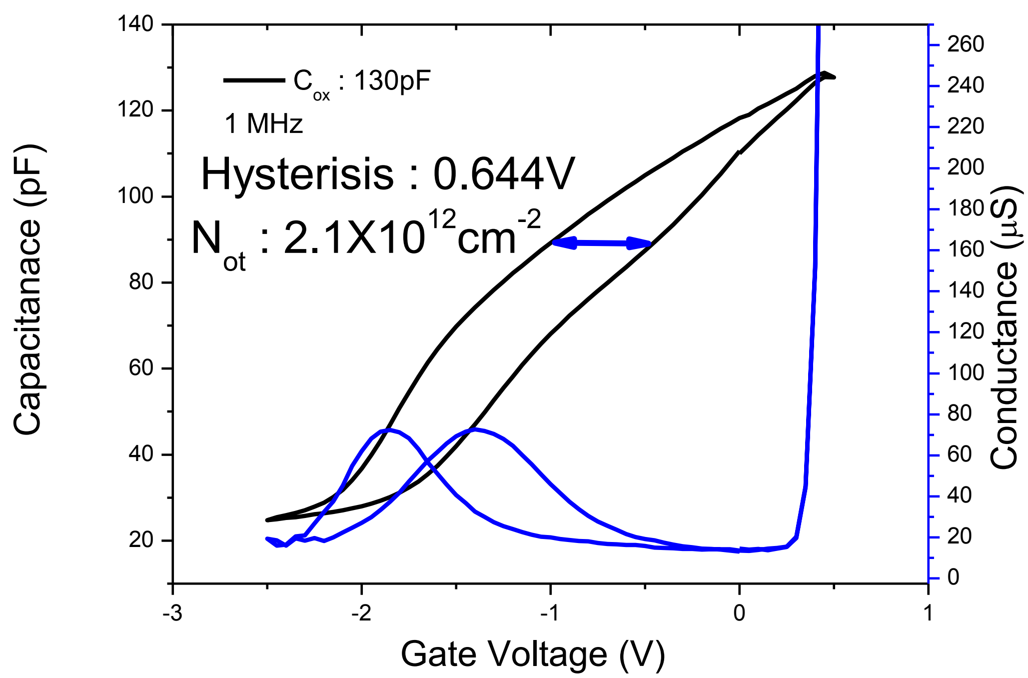


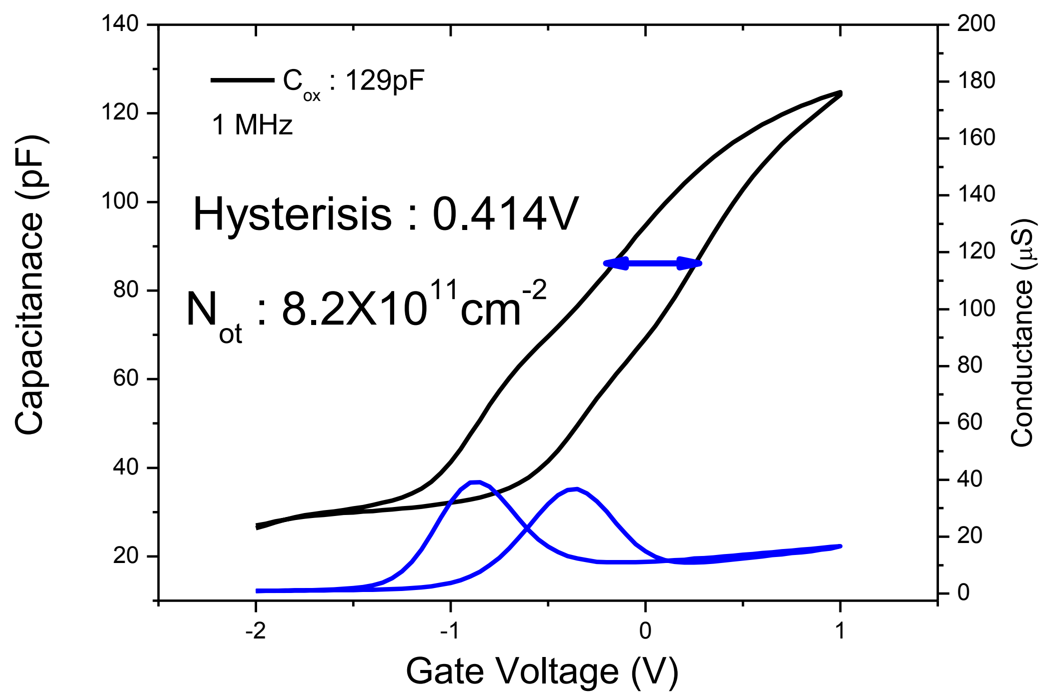
Figure 3.11. Normalized C-V (C/C_{ox}) at 1 MHz for each MOS capacitors

Figure 3.12. Bidirectional C-V characteristics of Ge PMOS capacitors for (a) RPN device, (b) RPN (50s)+Si(1nm), and (c) RPN (15s)+Si (1nm) treatment respectively.

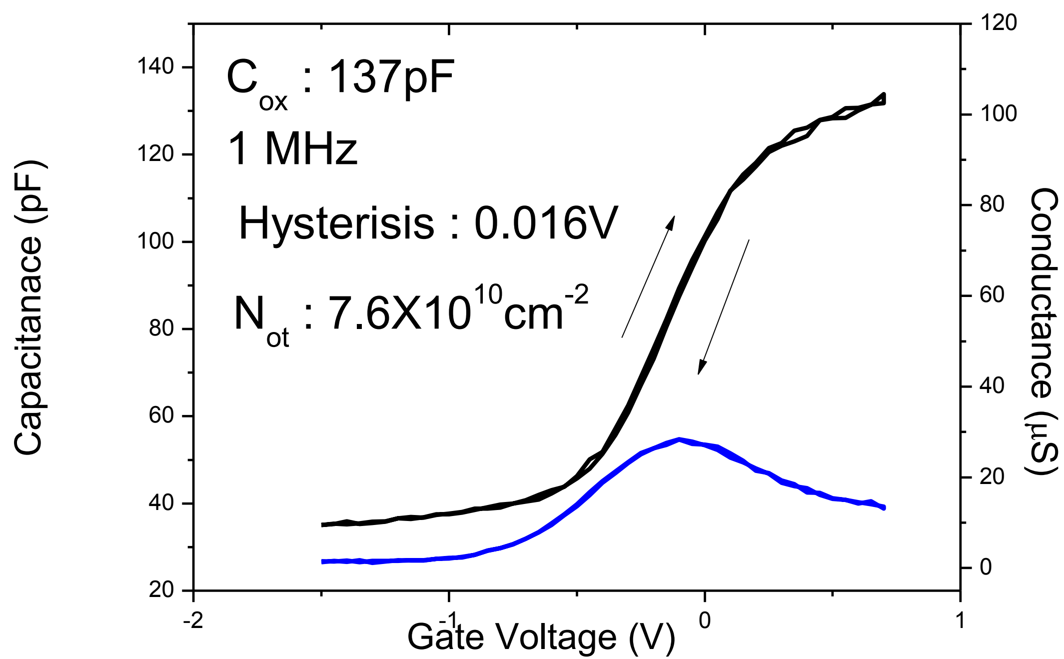
(a)



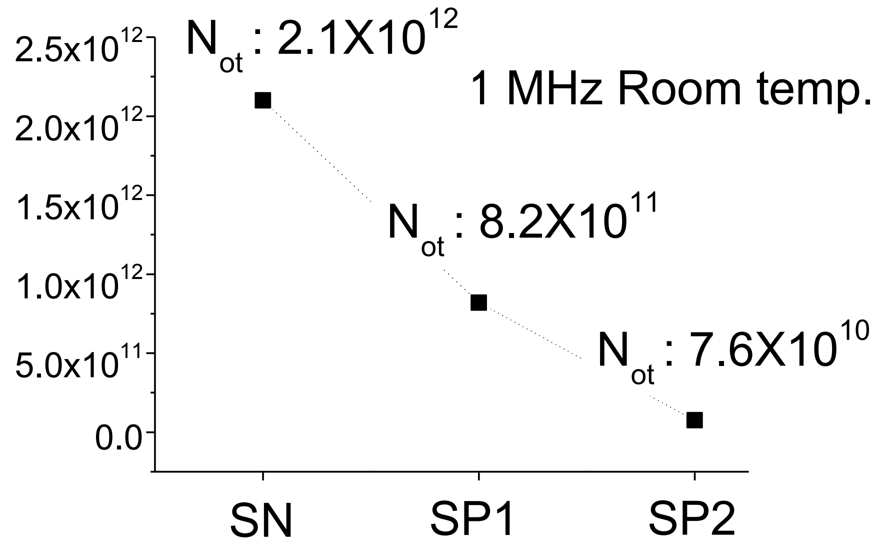
(b)



(c)



(a)



(b)

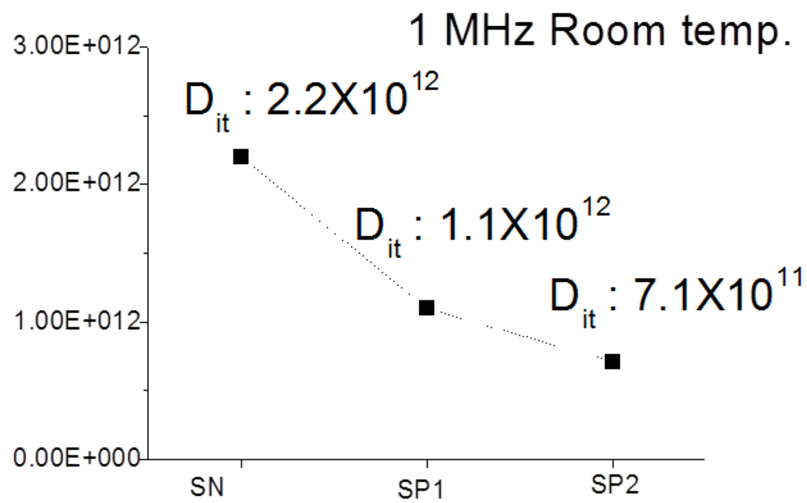


Figure 3.13. (a) Calculated by the hysteresis offset of CV characteristics slow trap density with surface treatment on Ge. (b) Calculated D_{it} by conductance method with surface treatment on Ge.

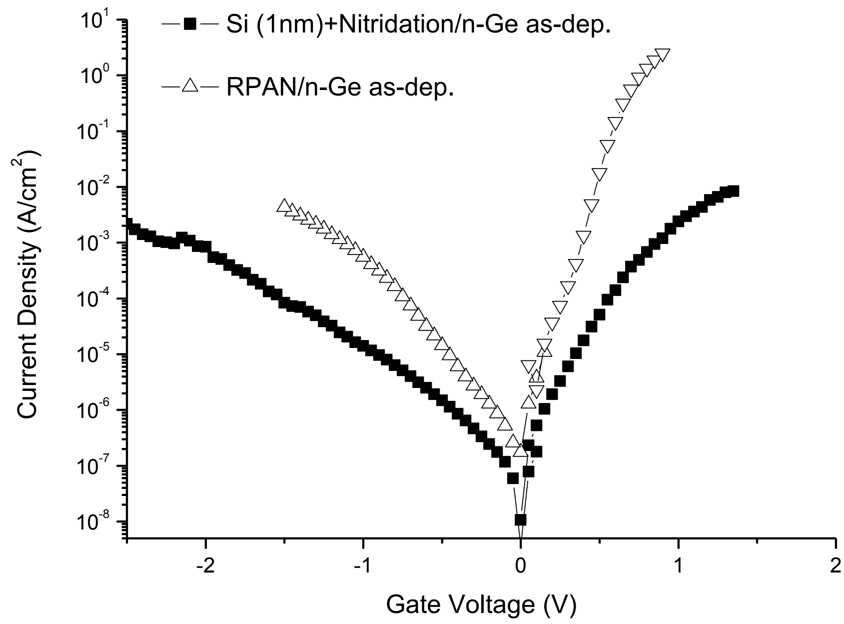


Figure 3.14. Leakage current characteristics of HfSiON Ge PMOS capacitors with RPN and RPN (15s)+Si (1nm) treatment respectively.

Table 3.1. Summary of electrical properties of HfSiON/ Ge MOS capacitors of (i) SN, (ii) SP1, and (iii) SP2 surface.

	EOT (nm)	N_D (cm^{-3})	V_{fb} (V)	Hysteresis (V)	*Oxide trapped charge density(cm^{-2})*	*Interface trap density (D_{it})*
SN	**1.93**	**~1.6X10^18**	**-0.81**	**0.64**	**$2.1X10^{12}$**	**2.2^X10^{12}**
SP1	**1.94**		**-0.21**	**0.41**	**$8.2X10^{11}$**	**1.1^X10^{12}**
SP2	**1.62**		**-0.25**	**0.016**	**$7.6X10^{10}$**	**$7.1X10^{11}$**

4 Investigation of thermal stability of pseudo-ternary HfSiON with combination of pseudomorphic Si layer and nitridation on Ge and investigation of TiO_2 Ge gate stack for the below 1nm of EOT

Abstract

Thermal stability of pseudo-ternary HfSiON with combination of pseudomorphic Si layer and nitridation on Ge with 400, 500, 600, and 700 °C annealed samples as investigated in this chapter. The Si passivation layer is still present even though partial consumption of the Si passivation layer results in SiO_x formation after 700 °C anneal. The peak shift of the Hf 4f spectra during the anneal is small indicating that the effect of anneal for the oxidation state of Hf in the HfSiON layer is beyond the measurement`s detection limit. The C-V curves of all devices show well behaved curves such as minimal stretch out, low slow trap density and no kinks in the depletion region at all measured frequencies (10 kHz–1 MHz) indicating suppression of “slow” surface states near the valence band (E_v) for n-Ge. It is remarkable that no hysteresis was found across the entire frequency range for 600 °C annealed sample indicating that “zero” slow trap density was achieved. Using the DLTS technique, suppression of interface states near E_c by a pseudomorphic Si layer for a HfSiON MOS capacitor was successfully demonstrated. The determined D_{it} near midgap for each capacitors are i)~7 x 10^{11} eV^{-1} cm^{-2} for as-deposited HfSiON, ii) ~3 x 10^{11} eV^{-1} cm^{-2} for 600 ^oC annealed HfSiON, and iii))~7 x 10^{12} eV^{-1} cm^{-2} for deposited HfO_2 respectively. The

possibility of the application of TiO_2 for Ge devices with pseudomorphic Si layers has been successfully demonstrated. The C-V curve of TiO_2 with pseudomorphic Si layers also showed well behaved curves such as no kink in depletion and negligible stretch out. . It is remarkable that extremely low (~5mV) hysteresis corresponding to a slow trap density of 1.13×10^{10} cm^{-2} and a 0.431 nm of EOT were achieved through a pseudomorphic Si layer with nitridation because this passivation yielded large conduction band offset energy (CBOE) and also large valence band offset energy (VBOE) to Ge. Therefore, this passivation layer can provide a pathway for the Titanium based Ge-MOSFETs.

4.1 Introduction

As the scaling of bulk Si CMOS transistors approaches its fundamental limits, innovative device and new materials have been investigated to continue the historic progress in information processing and transmission [1]. One such promising material is Ge due to several of its attractive properties including higher carrier mobility for larger drive current, smaller mobility band gap for supply voltage scaling, and smaller optical band gap to broaden the absorption wavelength spectrum [2]. However, the lack of a sufficiently stable native oxide has prevented the passivation of Ge surfaces. During the last several decades, dielectric materials like GeO_2, Ge_3N_4, and GeO_xN_y, on Ge surface have been widely attempted to achieve high quality interfaces, although only a few of them would likely yield an EOT of less than 10 Å to advance beyond the sub-20 nm regime [3-9].

Inspired by the success of the high quality of pseudomorphic Si layers on Ge substrates, characteristics of ultra thin high-k dielectrics on Ge with pseudomorphic Si layers are investigated in this chapter. In addition, thermal stability of interfacial layer with various rapid thermal annealing (RTA) is investigated. High-resolution ex-situ x-ray photoelectron spectroscopy (XPS) analysis using Al K_α radiation source was performed to investigate the chemical structure of HfSiON/Ge with Si passivation and nitridation samples with RTA. Also, the quality of interface and dielectric layers was investigated using fabricated Ge metal-oxide-semiconductor (MOS) capacitors. Deep level transient spectroscopy (DLTS) was performed to demonstrate the energy distribution of interface traps density for HfSiON MOS capacitors.

TiO_2 has been considered a promising candidate material because the bulk rutile

crystalline phase of TiO_2 exhibiting very high *k* values of ~80. Large leakage current was usually observed for TiO_2 on Ge gate stack due to the "almost zero" conduction band offset energy (CBOE) of TiO_2 with respect to either Ge or Si [2,15,16]. Therefore, interfacial layer (or passivation layer) should be required for the application of TiO_2 as gate dielectric for below 1nm of EOT. In this chapter, the possibility of the application of TiO_2 for Ge device with pseudomorphic Si layer has been investigated.

4.2 Experimental Procedures

As received two-inch n type germanium wafers, prior to load into the UHV environments, were wet-chemically cleaned by modified NH_4OH based cleaning procedure shown in chapter three. Prior to deposit of high-k gate dielectrics, very thin 1nm 'pseudomorphic' silicon layers were deposited onto n-type Ge (100) substrates at 300 °C by remote plasma enhanced chemical vapor deposition (RPECVD) with 2%-SiH_4 in He and He gases for 42 seconds for 1 nm thickness of silicon layer. After pseudomorphic silicon layer deposition, the layer was exposed to reactive species from a remote N_2/He discharge at 0.3 torr for nitridation for 15 seconds to provide chemical passivation to suppress further unwanted reaction between the deposited gate dielectrics and the Ge substrates. The processing temperature was 300 ^oC, and RF power was 30 W at 13.56 MHz. After surface passivation treatment, HfSION (2nm) and TiO_2 (4nm) were deposited on films onto n-Ge (100) substrates at 300 °C by remote plasma enhanced chemical vapor deposition (RPECVD).The Si, Hf, and Ti source gases, 2% SiH_4 in He, Hf (IV) t-butoxide, and Ti (IV) t-butoxide respectively, were delivered directly into the substrate region of a remote plasma reactor

through two different injectors. An $N_2/N_2O/He$ mixture was subjected to remote plasma excitation at 30 W and 13.56 MHz and was employed to initiate RPECVD process. Upon deposition, heat treatment of HfSiON samples was done by rapid thermal annealing (RTA) at 400, 500, 600, and 700 °C respectively.

For the fabrication of HfSiON MOS and TiO_2 MOS devices and electrical characterization studies, a 500 nm Al layer was evaporated and defined by shadow mask. Forming gas anneal (FGA) for 30 minutes in a mixture of 10% H_2 in N2 at 400°C was performed to minimize D_{it}. This step was done before metallization in order to prevent reactions between the Al gate and the dielectric films. Electrical measurements were conducted on a Material Development Corporation system. An HP 4284A LCR meter with a frequency range of 1 kHz to 1 MHz was used to perform capacitance-voltage measurements for capacitance dispersion. Current-voltage measurements were done on an HP 4140B voltage source with a pico-ammeter. Voltage-ramp rates were varied from dV/dt = 0.001V/sec to dV/dt = 0.05 V/sec. A slower ramp rate is preferred to reduce the displacement current, ensuring that the current measured is actually tunneling current. All electrical measurements were performed at room temperature in the dark room.

DLTS measurements were performed on HfSiON MOS devices to demonstrate the distribution of interface trap density. DLTS spectra were obtained on a Rio-Rad 8000 spectroscope. The diodes were -0.4 V reverse biased, and pulsed for 50 ms. To demonstrate the interface states and bulk traps, various pulse voltage from 0 V to 0.2 V were applied to the diodes.

4.3 Results and Discussion

4.3.1 Thermal stability of surface passivation layer

To examine the thermal stability of pseudomorphic Si layers, SXPS with photon energy of 650 eV was performed on HfSiON (2nm)/ RPN+Si (1nm)/ n-Ge with anneal. Figure 4.1 displays Si 2p spectra measured for HfSiON (2nm)/ RPN+Si (1nm)/ n-Ge sample with RTA at 400, 500, 600, and 700 °C respectively. After HfSiON deposition, distinct Si 2p peaks from both the HfSiON overlayer (Si^{4+} oxidation state, binding energy, BE~102.2 eV) and the elemental silicon (Si^{0+} oxidation state , BE ~99.3 eV) interlayer exhibited for as-deposited sample. There were no significant differences of both Si^{4+} oxidation state and Si^{0+} oxidation state for as-the deposited films and 400, 500, and 600 °C anneal samples. Currently, a surface passivation using SiH_4 annealing or deposited by SSMBE prior to high-k deposition has been studied for Ge MOSFETs because surface nitridation is found to create new interface states. Furthermore, it is easily oxidized resulting in the nitride layer containing a high concentration of oxygen, which might degrade the blocking properties and inducing poor interface properties such as thermal stability. However, all of these studies revealed that Si passivation layer was fully oxidized after oxide deposition [10,11]. It is clear that Si passivation on Ge deposited by RPECVD is stable after high-k deposition and has thermal stability at high temperature anneal. Whereas, with increased RTA temperature at 700°C, intensity of Si^{0+} oxidation state slightly decreased and Si^{4+} oxidation state increased due to the partial consumption of the Si passivation layer after 700 °C anneal. However, it is clear that the existence of the Si passivation layer is still present even though partial consumption of the Si passivation layer results in SiO_x formation after 700 °C anneal. Therefore, it is

noteworthy that pseudomorphic Si passivation with nitridation deposited by RPECVD has thermal stability at 700°C anneal and can be an alternative passivation technique for conventional Ge MOSFETs fabrication process.

Figure 4.2 exhibits XPS Ge 3d sepectra for HfSiON (2nm)/RPN+Si (1nm)/ n-Ge with RTA at 400, 500, 600, and 700 °C respectively. To clarify the peak position and the contribution of the Hf 5p peak, the Ge 3d peak intensities are normalized by Hf 4f peak intensities. The dotted line indicates the peak position for GeO_2 (+3.3 eV shift vs. Ge^{0+}), as reported in the literature [12,13]. As shown in chapter two, Ge^{0+} oxidation state (29.3 eV) which is related to Ge bulk and Hf 5p peak (+3.9 eV shift vs Ge^{0+}) were clearly observed for as-deposited sample. As can be expected, we also observed the attenuation of Ge^{0+} oxidation state as annealing temperature increased. In addition, we observed both Hf 5p peak shifted to lower binding energy (around +3.3 eV shift vs. Ge^{0+}) and increased intensity with increased temperature. This indicates 700 °C annealed sample has a much higher concentration of lower binding energy components corresponding to Ge^{4+} oxidation state than does as-deposited 400, 500, and 600 °C samples. The reason is two factors; (i) the oxygen from oxide layer (ii) native oxide due to air exposure before loading into UHV chamber. It can be explained that Ge^{4+} oxidation state sourced from oxidation after wet chemical clean since the existence of elemental Si after deposition and after 700 °C anneal indicates that pseudomorphic Si layer successfully blocks the oxygen during the process.

Figure 4.3 indicates Hf 4f spectra for spectra for HfSiON (2nm)/RPN+Si (1nm)/ n-Ge with RTA at 400, 500, 600, and 700 °C respectively. The peak shift of the Hf 4f spectra during the anneal is small indicating that the effect of anneal for the oxidation state of Hf in the HfSiON

layer is beyond the measurement`s detection limit.

4.3.2 The annealing effects of HfSiON PMOS capacitors with RTA.

Figure 4.4 (a) shows the frequency dependence of C-V characteristics of as-deposited Al/HfSiON(2nm)/RPN+Si(1nm)/n-Ge PMOS capacitors. The capacitance was measured at various frequencies as a function of gate voltage and the capacitor was swept from inversion to accumulation at room temperature in the dark room. The C-V curve of the as-depposited device shows well behaved curves such as no kink in depletion at all measured frequencies (10 kHz–1 MHz) corresponding to the suppression of "slow" surface states near the valence band (E_v) for n-Ge, and minimal stretch out which were similarly observed to 4nm of HfSiON/RPN+Si (1nm)/n-Ge in chapter three. As described in chapter three, calculated ideal flat band voltage ($V_{fb,\ ideal}$) between Al gate and n-Ge substrate (Doping concentration : 7 x 10^{17}-1 x 10^{18} cm^{-3}) is -0.023 V. V_{fb} and N_f values calculated from $V_{fb,\ ideal}$ and EOT extracted by NCSU-CVC version 7 were -0.362V, 4.67 x 10^{11} cm^{-2} and 1.12 nm, respectively. As can be seen, flat band voltage shifts between measurement frequencies (1 MHz-10 kHz) which are the direct result of interface states were observed for around 0.11V. As shown in Figure. 4.4 (b), the retrace on the 1 MHz curve of this device shows 13mV of hysteresis corresponds to slow trap density of 1.76 x 10^{10} cm^{-2}. Around 10 ~13 mV of hysteresis were found across the entire frequency range.

Figure 4.5 (a) shows the frequency dependence of C-V characteristics of 500 °C annealed PMOS capacitors. The C-V curve of annealed device also shows well behaved characteristics such as no kink in depletion and no stretch out. Compared to as-deposited

sample, the positively shift of V_{fb} from ideal V_{fb} was observed indicating that 500 °C anneal reduce the negative fixed charges. N_f values calculated from $V_{fb, ideal}$ was 3.07 x 10^{11} cm^{-2}. As displayed, flat band voltage shifts between measurement frequencies (1 MHz-10 kHz) which are the direct result of interface states decreased 0.098V compared to as-deposited device.

As displayed in Figure 4.5 (b), the retrace on the 1 MHz curve of 500 °C sample shows similar value (12mV) of hysteresis corresponds to slow trap density of 1.50 x 10^{10} cm^{-2}. Around 10 ~12 mV of hysteresis were found across the entire frequency range. 500 °C anneal reduced the negative fixed charge (N_f) and slow trap density as well.

Figure 4.6 (a) shows the frequency dependence of C-V characteristics of 600 °C annealed PMOS capacitors. The C-V curve of 600 °C annealed device also shows well behaved curves such as no kink in depletion and no stretch out. It is remarkable that no hysteresis were found across the entire frequency range. If there are electron trapping from the *n*-type Ge substrate injection, after scanning from inversion to the accumulation condition, the *C–V* curve can be shifted along the positive axis (or clockwise) during reverse scan as a consequence of electron trapping from the *n*-type Ge substrate injection. Therefore, it is clear that “Zero” oxide trap charge (electron trapping) is achieved with 600 °C anneal (Figure 4.6 (b)). As described in chapter two, it displayed similar trend of annealing effects for HfSiON/RPN(90s)/n-Ge case because we achieved minimum hysteresis after 650 °C anneal. In addition, the closest V_{fb} to ideal V_{fb} was shown for this device, indicating that the minimum N_f was obtained with 600 °C anneal. As displayed, minimum flat band voltage shifts between measurement frequencies (1 MHz-10 kHz) were shown for 0.058V compared to other devices. V_{fb} and N_f values calculated from $V_{fb, ideal}$ and EOT extracted by

NCSU-CVC version 7 were -0.101V, 1.22 x 10^{11} cm^{-2} and 0.86 nm at 1 MHz, respectively.

However, after high temperature anneal (700 °C), degraded quality of device was observed in Figure 4.7 (a). Frequency dispersion of C-V characteristics for 700 °C Ge PMOS capacitors increased again and there was small dispersion in accumulation condition in comparison with 600 °C device. Flat band voltage shifts between measurement frequencies (1 MHz-10 kHz) were found for 0.22 V and hysteresis near accumulation regime for around 20 mV as compared to the 600 °C device. In addition, a positive shift of V_{fb} from the ideal V_{fb} was observed compared to other devices, indicating that high temperature anneal produced the negative fixed charges which were effectively located charges at the HfSiON/SiO_x interface. V_{fb} and N_f values calculated from $V_{fb,\ ideal}$ were 0.101 V and -2.0 x 10^{11} cm^{-2}. The C-V hysteresis is shown in Figure 4.7 (b), in which the window of hysteresis varies with different surface potentials (V_G); a 20 mV window near accumulation regime corresponds to slow trap density of 3.02 x 10^{10} cm^{-2} but no apparent window at depletion and inversion. This hysteresis behavior from the accumulation to the inversion supports the hypothesis on the existence of surface states near E_c for p-Ge. More specifically, this C-V performance of the PMOS Ge capacitor is primarily affected by surface states located near the E_c and does not suffer from bulk oxide traps, which normally cause a parallel shift of C-V curves.

For direct comparison, the normalized C-V data at 1 MHz for all devices is shown in Figure 4.8 (a). Minimum stretch out indicating minimum D_{it}, smallest negative shift of V_{fb} from $V_{fb,\ ideal}$ meaning minimum N_f and no hysteresis corresponding to zero slow trap density were achieved for 600 °C device. It is also evident that higher temperature anneal degraded

the interfacial quality such as positive shift of V_{fb} from $V_{fb,\ ideal}$ due to negative fixed charge HfSiON/SiO_x interface, 20mV of hysteresis near accumulation regime corresponding to the existence of surface states near E_c for p-Ge, and relatively stretch out as compared to 600 °C device.

Figure 4.8 (a) and (b) show measured and calculated C-V curved of Ge PMOS capacitors for the as-deposited and 600 °C devices respectively. The determined net donor concentration (N_D), EOT, and threshold voltage (V_{th}) of each Ge MOS capacitor; (i) 5.6 and 7.3 x 10^{18} cm^{-3}, (ii) 1.18 nm and 0.86 nm, and (iii) -0.74 V and -1.07 respectively.

In this section, the results of Deep Level Transient Spectroscopy (DLTS) will be introduced to demonstrate the energy distribution of interface trap density of high-k MOS devices. Figure 4.9 (a) shows the DLTS spectra for as-deposited HfO_2 MOS capacitor for the reference, HfSiON and 600 ^oC annealed HfSiON MOS capacitors. All samples have the same bulk trap at 165 K, of which have 0.28 eV energy level and 7.6 × 10^{-17} cm^{-3} capture cross section. The trap densities of as-deposited HfO_2, as-deposited HfSiON and 600^oC annealed HfSiON MOS capacitors are 5.2 × 10^{17} cm^{-3}, 1.2 × 10^{17} cm^{-3}, and 2.4 × 10^{16} cm^{-3}, respectively.

The identification of the trap can be revealed by the characteristic features by various pulse voltage measurements from 0 to 0.2 V, (Figure 4.10 (a)). The peak position of the deep energy impurity does not shift with pulse voltages, which means it has the discrete energy level regardless of the space charge region. This suggests that the trap at 160 K corresponds to bulk trap, not the interface states. Marten *et al.* reported that DLTS results for Si-passivated HfO_2 germanium MOS-capacitors to demonstrate the interface states. As

clearly shown in Figure 4.10 (b), the peak temperature varies evidently with quiescent voltage, which is an indication of the presence of interface traps and shows the measured response to be due to interface traps and not bulk traps [14].

The amount of the deep energy impurity for as-deposited HfO_2 MOS capacitor is higher than that for as-deposited HfSiON MOS capacitor. Also, in the shallow energy level below 165 K, the DLTS signal of HfO_2 sample is higher than that of the as-deposited HfSiON sample. More specifically, the amount of the trap, which has continuous energy level from 50 to 165 K, of HfO_2 MOS capacitor is larger than that of the as-deposited HfSiON MOS capacitor. These continuous energy level impurities are related to the interface states. Contrary to the bulk trap, these interface states do not exhibit a specific discrete energy level, and its positions change with different space charge regions. Although the interface states are not so apparent due to the effects of the bulk trap, Figure 4.9 clearly shows that the interface states of as-deposited HfSiON at the shallow energy level (in this study, the shallow energy level means near the conduction band edge) are suppressed compared to that of the as- deposited HfO_2. The densities of interface states and bulk trap of HfSiON decreased by the RTA annealing process at 600 ^{o}C as a result of the improvement of the interface quality.

Figure 4.11 shows the energy distribution of interface traps as a function of conduction band offset for as-deposited HfO_2 (for reference), HfSiON and 600 ^{o}C annealed HfSiON MOS capacitors respectively. The D_{it} values of as-deposited HfSiON are more than one order of magnitude and less than that of as-deposited HfO_2 sample. In addition, it is notable that the suppression of conduction band edge interface states were clearly observed for as-

deposited HfSiON and 600 ^{o}C annealed HfSiON MOS capacitors compared to as-deposited HfO_2 MOS capacitor. These results indicate that Si–O and Si–N bonding in noncrystalline Hf-SiON films effectively suppress divacancy defects and Ge incorporation into the films. The determined D_{it} near midgap for each capacitors are i)~7 x 10^{11} eV^{-1} cm^{-2} for as-deposited HfSiON, ii) ~3 x 10^{11} eV^{-1} cm^{-2} for 600 ^{o}C annealed HfSiON, and iii))~7 x 10^{12} eV^{-1} cm^{-2} for deposited HfO_2 respectively. All of electrical properties were summarized in Table 4.1.

The investigation of the suppression of interface state near the (E_c) will be addressed in the next chapter for HfSiON NMOS capacitor.

4.3.3 The possibility of TiO_2 for Ge device for the below 1nm of EOT

In this section, electrical properties of TiO_2 (4nm) on n-Ge with the same passivation layer will be addressed for the application of Ge MOSFETs. As shown in Figure 4.12 (a) shows the frequency dependence of C-V characteristics of as-deposited TiO_2 PMOS capacitors. Like HfSiON Ge PMOS, the C-V curve also showed well behaved curves such as no kink in depletion and negligible stretch out. As displayed, small frequency dispersion between measurement frequencies (1 MHz-100 kHz) which are the direct result of interface states showed 0.025V. As shown in Figure 4.12 (b), the retrace on the 1 MHz curve of device showed extremely low (~5mV) of hysteresis corresponds to slow trap density of 1.13 x 10^{10} cm^{-2}. A negative shift of V_{fb} from ideal V_{fb} is observed indicating that the amount of positive fixed charges is located at the TiO_2 /SiO_x interface. N_f values calculated from $V_{fb, ideal}$ was 5.15 x 10^{11} cm^{-2}. Figure 4.12 (c) shows measured and calculated C-V curves of Ge

PMOS capacitor. The determined V_{fb}, threshold voltage (V_{th}), of device were; (i) -0.255 V, and (ii) -0.944 V, respectively. It is noteworthy that an EOT of 0.431 nm was obtained for the Al/TiO_2 (4nm) /RPN (15s)+Si (1nm) /Ge MOS capacitor extracted from NCSU CVC program.

TiO_2 has been considered a promising candidate material because the bulk rutile crystalline phase of TiO_2 exhibiting very high *k* values of ~80. Large leakage current was usually observed for TiO_2 on Ge gate stack due to the "almost zero" conduction band offset energy (CBOE) of TiO_2 with respect to either Ge or Si. For use as a gate dielectric in MOSFETs, a dielectric should have a CB offset and a VB offset of over 1 eV to achieve low leakage currents due to injection into the bands. Therefore, interfacial layer (or passivation layer) should be required for the application of TiO_2 as gate dielectric [15,16]

Figure 4.13 (a) and (b) display the band alignments for TiO_2/GeO_2/n-Ge and TiO_2/RPN+Si/n-Ge gate stacks using the band gaps and conduction. Figure 4.13 (a) demonstrates that when GeO_2 is used as passivation between Ge and TiO_2, the band gap of that passivation is less than that of the high-K TiO_2 dielectric. This gate stack alignment is qualitatively different than that of SiON passivation where the band gap of the passivation is greater than that of TiO_2 (Figure 4.13 (b)). SiON large conduction band offset energy (CBOE) (3.3 eV) and also large valence band offset energy (VBOE) (4.9 eV) to Ge. Pseudomorphic Si layer with nitridation meets the requirements for the high-*k* gate dielectric with CBOE larger than 1 eV to the semiconductor channel and provides excellent interface quality and thermal stability as well. Qualitatively similar band alignment diagram apply when SiO_2 replaces SiON [2,16]. Therefore, Pseudomorphic Si layer with nitridation could be an alternative passivation technique for the application of TiO_2 for Ge MOSFETs.

4.4 Summary

The thermal stability of pseudo-ternary HfSiON with a combination of pseudomorphic Si layer and nitridation on Ge with 400, 500, 600, and 700 °C annealed samples have been investigated in this chapter. The existence of the Si passivation layer is still present even though partial consumption of the Si passivation layer results in SiO_x formation after the 700 °C anneal. The C-V data of all of devices show well behaved curves such as minimal stretch out, low slow trap density and no kink in depletion at all measured frequencies (10 kHz–1 MHz) indicating suppression of "slow" surface states near the valence band (E_v) for n-Ge. It is remarkable that no hysteresis were found across the entire frequency range for the 600 °C annealed sample indicating that "Zero" slow trap density was achieved. Using the DLTS technique, suppression of interface states near E_c by pseudomorphic Si layer for HfSiON MOS capacitor was successfully demonstrated. The determined D_{it} near midgap for each capacitors are i)~7 x 10^{11} eV^{-1} cm^{-2} for as-deposited HfSiON, ii) ~3 x 10^{11} eV^{-1} cm^{-2} for 600 ^{o}C annealed HfSiON, and iii) ~7 x 10^{12} eV^{-1} cm^{-2} for deposited HfO_2 respectively.

The possibility of the application of TiO_2 for Ge device with pseudomorphic Si layer has been successfully demonstrated. The C-V curve of TiO_2 with pseudomorphic Si layer also showed well behaved curves such as no kink in depletion and negligible stretch out. It is remarkable that extremely low (~5mV) of hysteresis corresponds to slow trap density of 1.13 x 10^{10} cm^{-2} and 0.431 nm of EOT were achieved.

4.5 References

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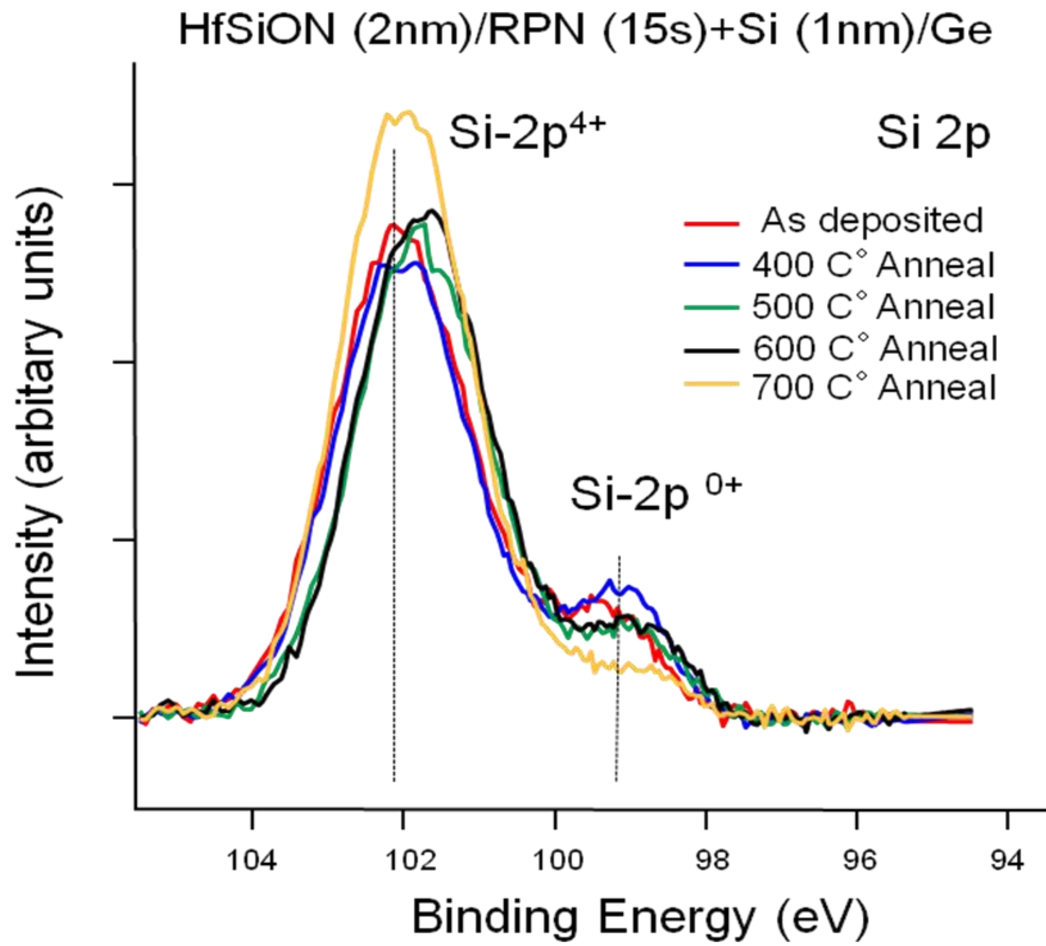


Figure 4.1. Si 2p spectra measured for HfSiON (2nm)/ RPN+Si (1nm)/ n-Ge sample with RTA at 400, 500, 600, and 700 °C respectively.

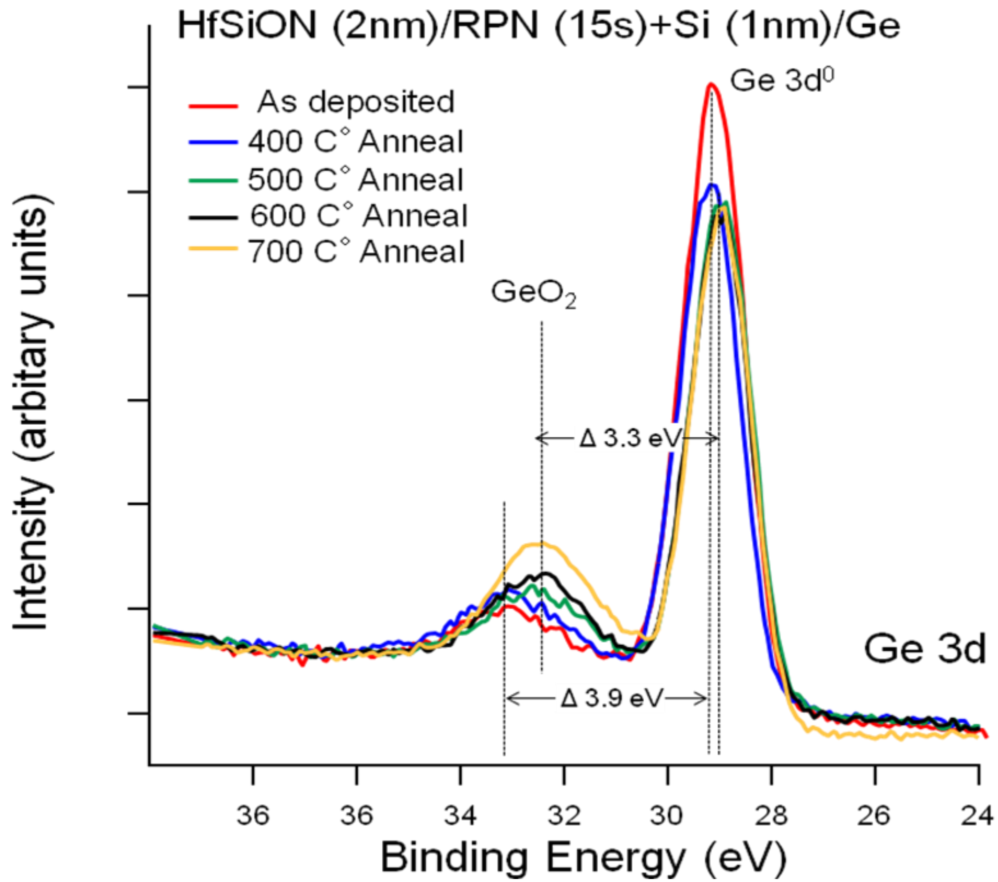


Figure 4.2. XPS Ge 3d spectra for HfSiON (2nm)/RPN+Si (1nm)/ n-Ge with RTA at 400, 500, 600, and 700 °C respectively.

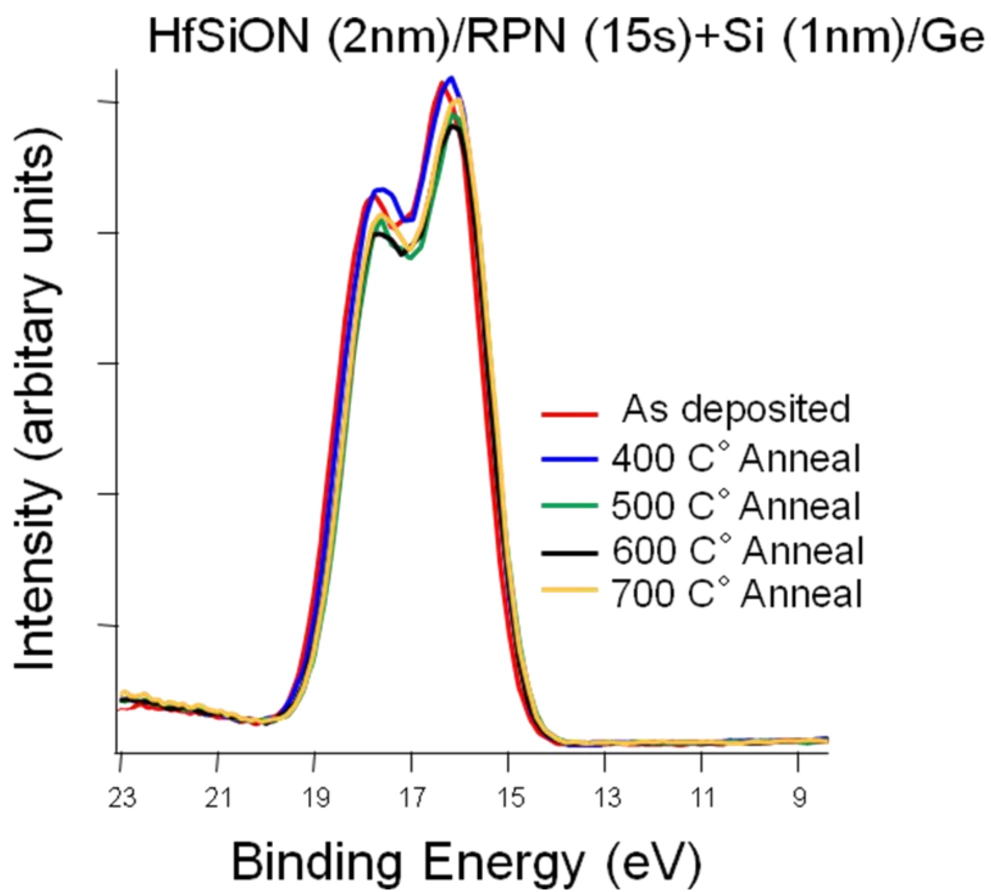
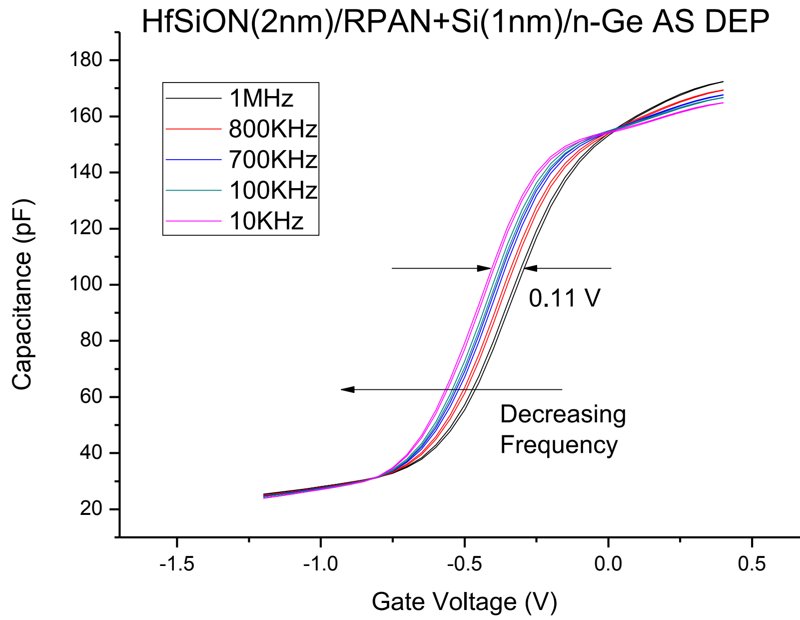


Figure 4.3. Hf 4f spectra for spectra for HfSiON (2nm)/RPN+Si (1nm)/ n-Ge with RTA at 400, 500, 600, and 700 °C respectively.

(a)



(b)

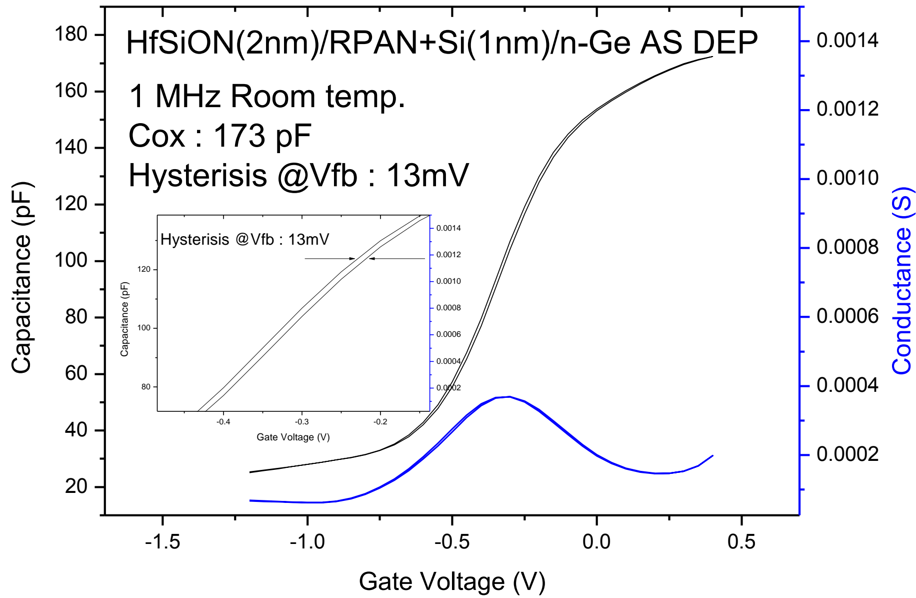
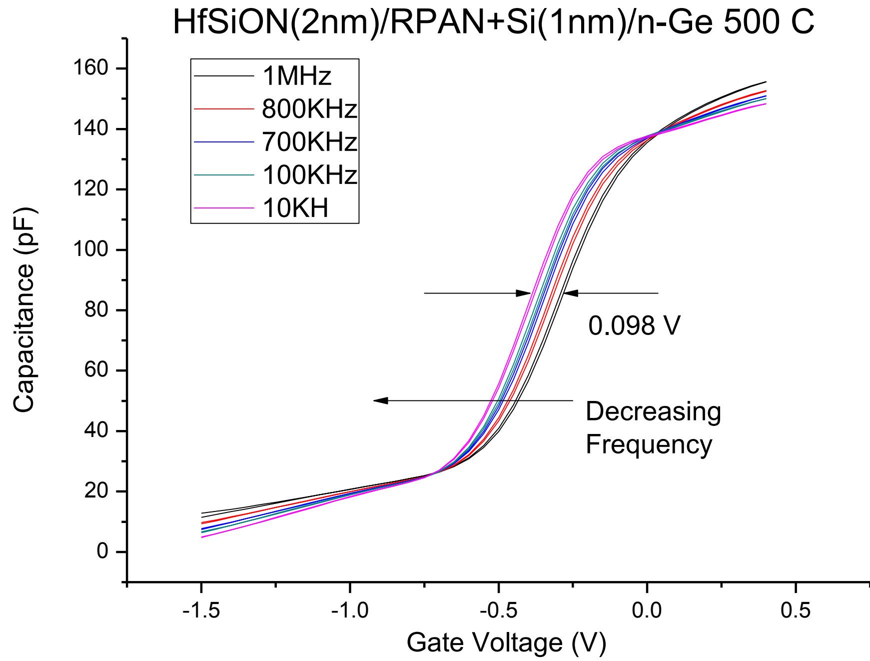


Figure 4.4. (a) the frequency dependence of C-V characteristics of as-deposited Al/HfSiON(2nm)/RPN+Si(1nm)/n-Ge PMOS capacitors. (b) the retrace on the 1 MHz curve of this device shows 13mV of hysteresis corresponds to slow trap density of 1.76 x 10^{10} cm^{-2}. Around 10 ~13 mV of hysteresis were found across the entire frequency range.

(a)



(b)

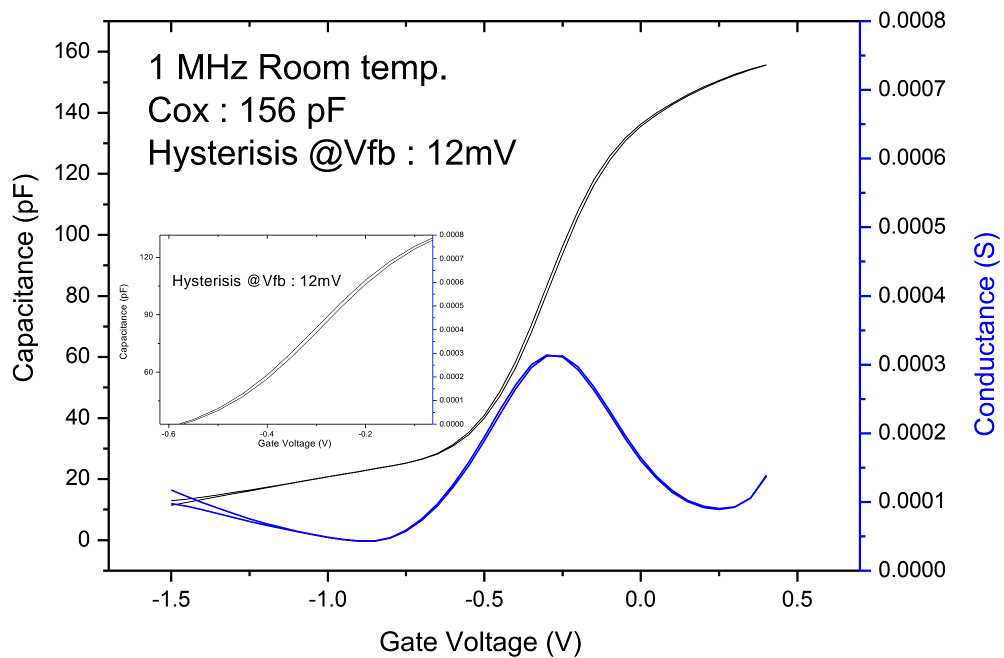
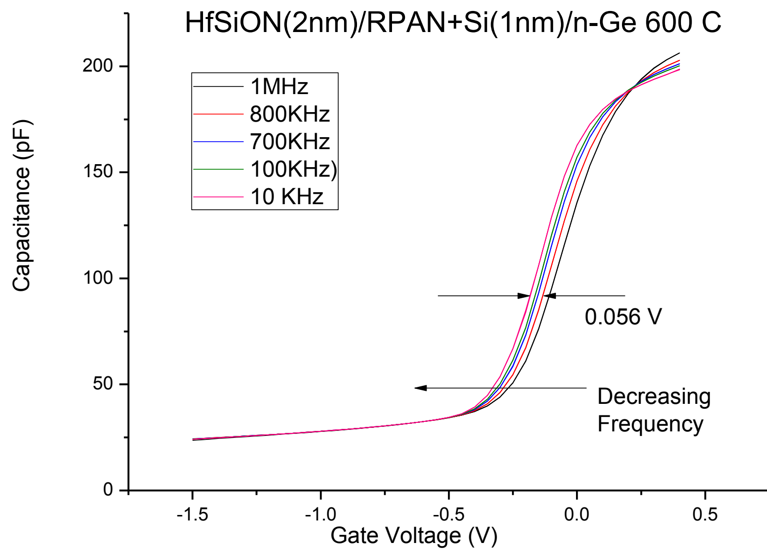


Figure 4.5. (a) the frequency dependence of C-V characteristics of 500 °C annealed PMOS capacitors. (b) the retrace on the 1 MHz curve of 500 °C sample shows similar value (12mV) of hysteresis corresponds to slow trap density of 1.50 x 10^{10} cm^{-2}.

(a)



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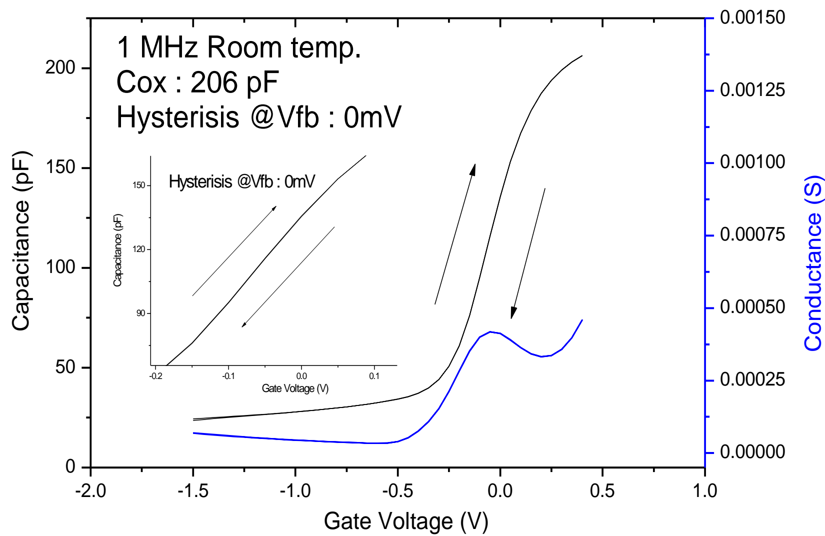


Figure 4.6. (a) the frequency dependence of C-V characteristics of 600 °C annealed PMOS capacitors. (b) the retrace on the 1 MHz curve of 500 °C sample shows “zero” hysteresis at bidirectional C-V. Note that zero hysteresis is found over the entire frequency range.

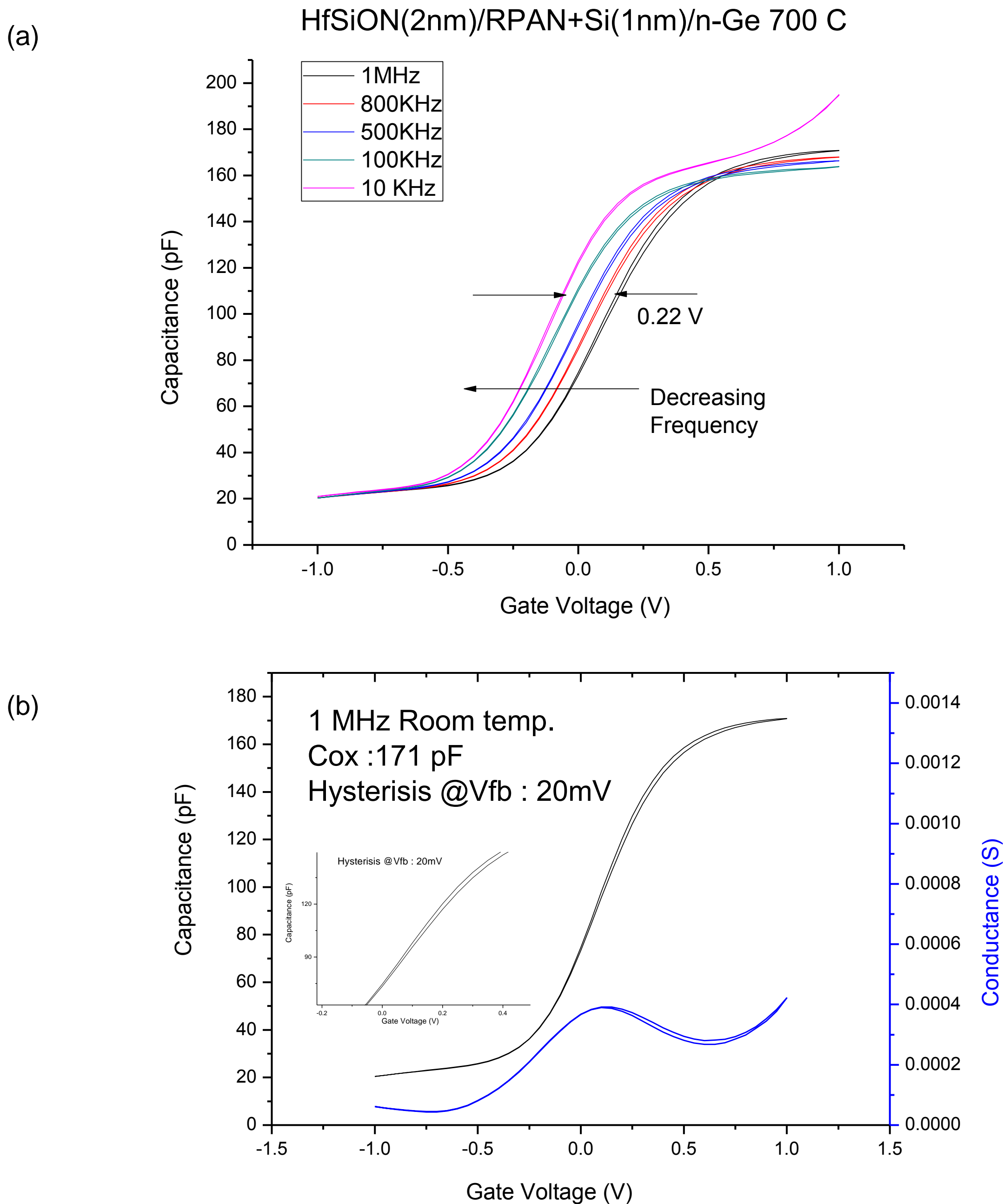
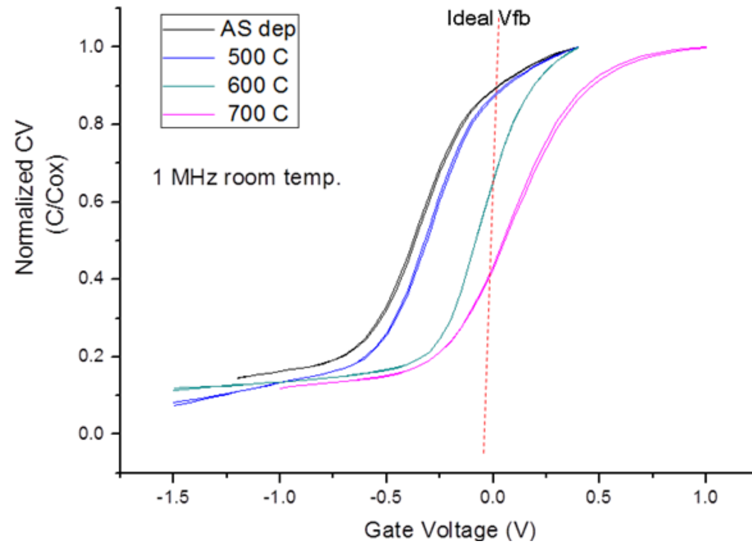
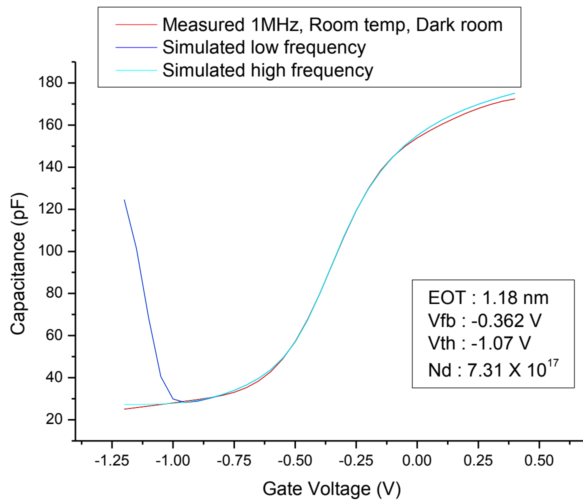


Figure 4.7. (a) Frequency dependence of C-V characteristics of Ge PMOS capacitors was increased and small dispersion in accumulation condition compared to the 600 °C device. (b) the retrace on the 1 MHz curve of 700 °C sample shows 20mV of hysteresis near accumulation regime corresponds to slow trap density of 3.02 x 10^{10} cm^{-2}.

(a)



(b)



(C)

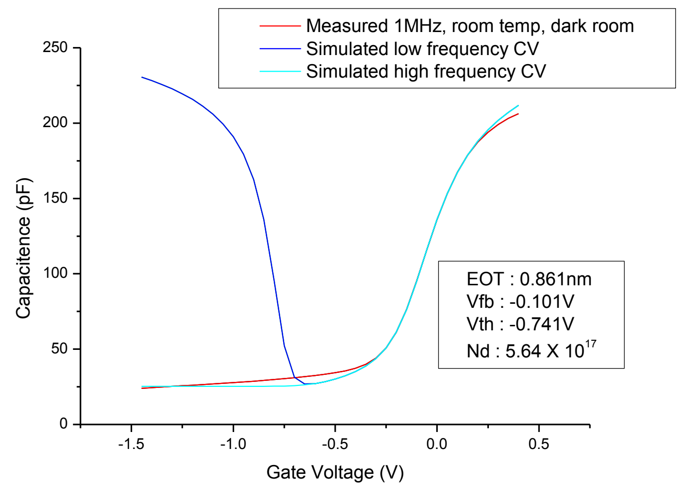


Figure 4.8. (a) normalized C-V at 1 MHz for HfSiON Ge PMOS capacitors. (b) and (c) shows measured and calculated C-V curve of Ge PMOS capacitor for as-deposited and 600 °C devices respectively

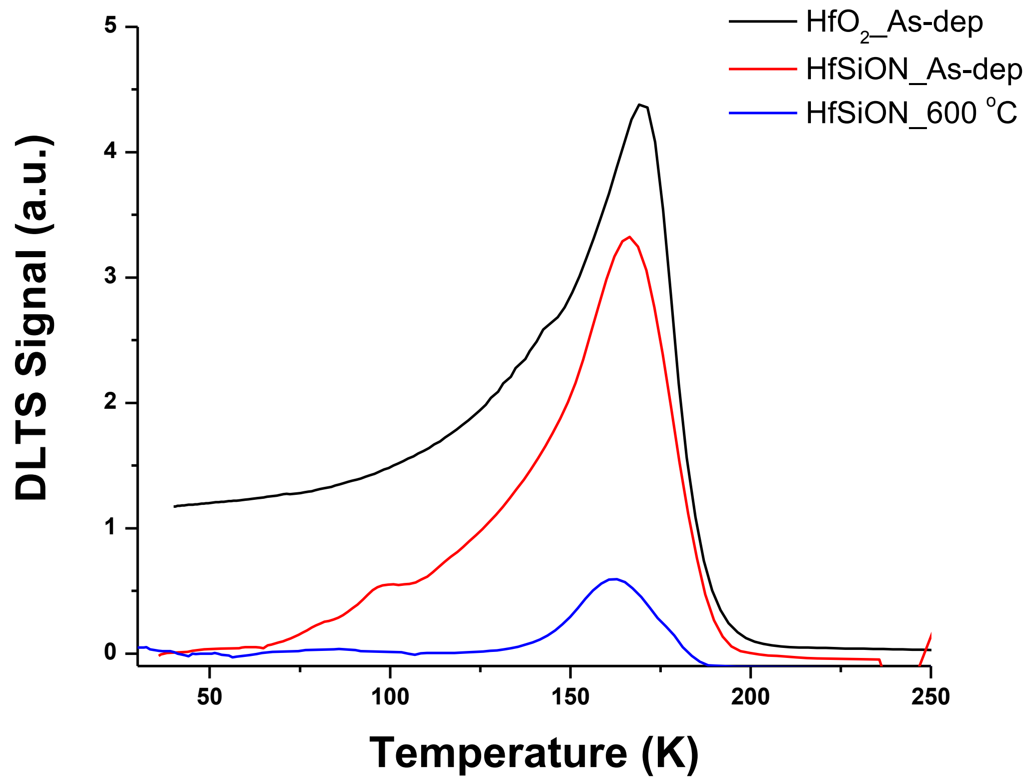
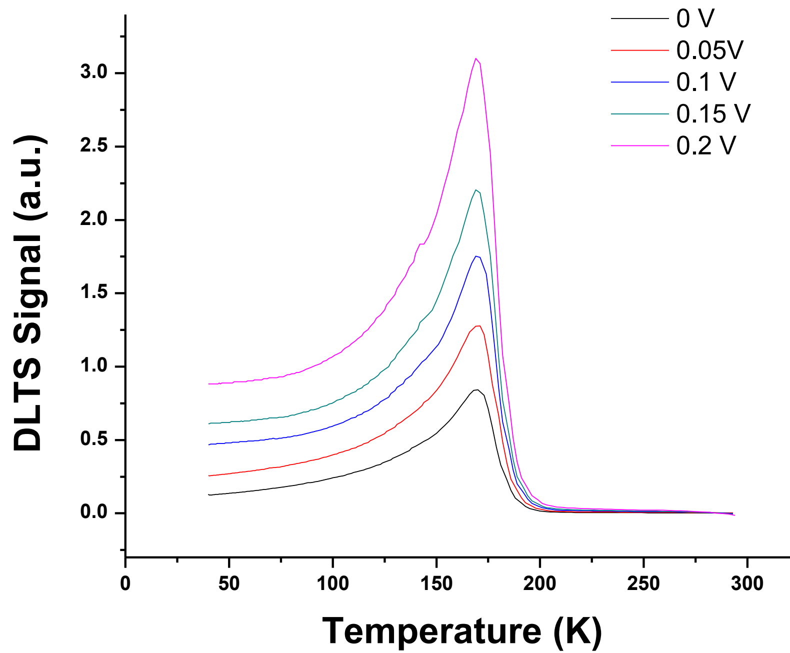


Figure 4.9. DLTS spectra as a function of temperature for as-deposited HfO_2, HfSiON and annealed HfSiON at 600 ^oC. -0.4 V reverse biased, and pulsed for 50 ms.

(a)



(b)

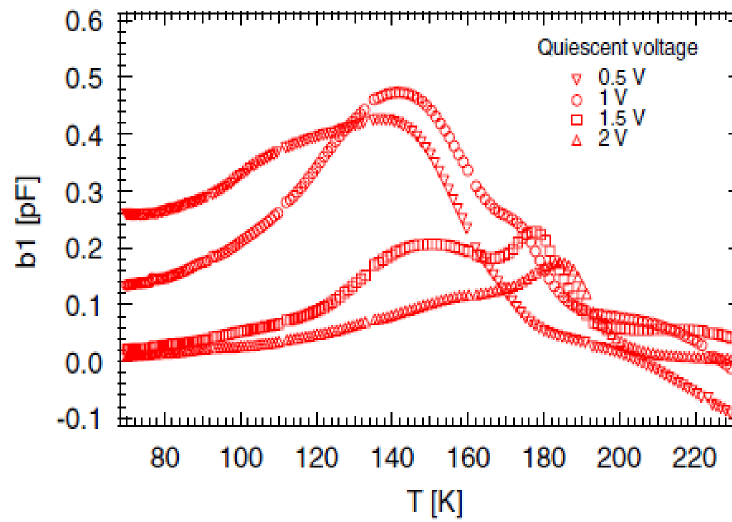


Figure 4.10. (a) DLTS spectra as a function of temperature for as-deposited HfSiON with various pulse voltages from 0 to 0.2 V. -0.4 V, and pulsed for 50 ms. (b) DLTS spectrum for different quiescent voltages indicating the traps to be interface traps.

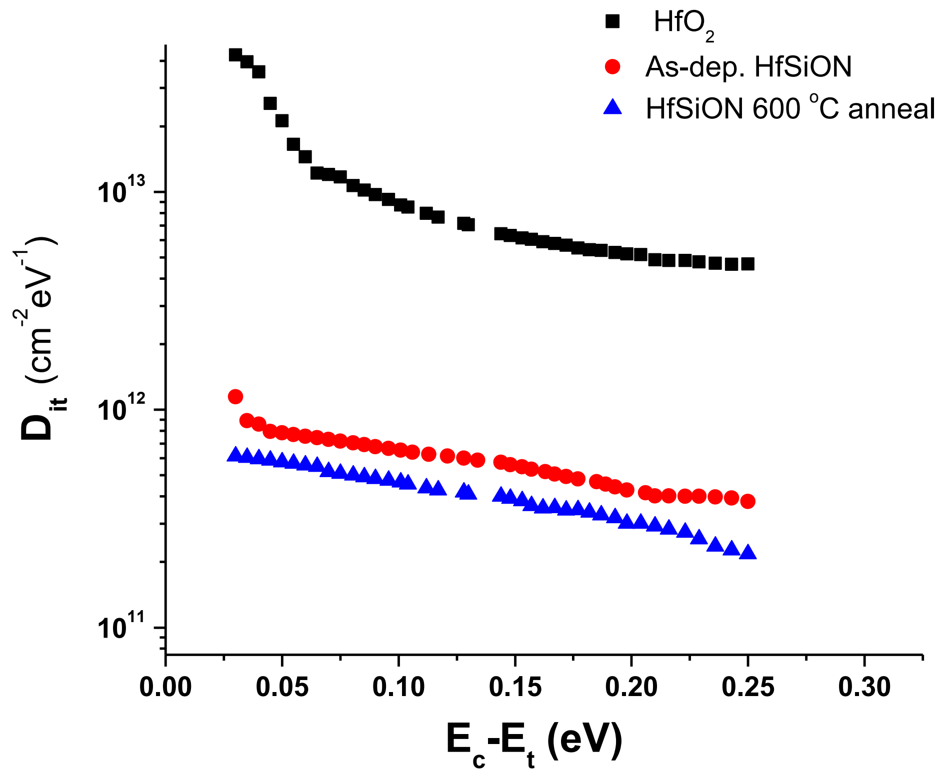


Figure 4.11. the energy distribution of interface traps as a function of conduction band offset for as-deposited HfO_2 (reference), HfSiON and 600 °C annealed HfSiON MOS capacitors.

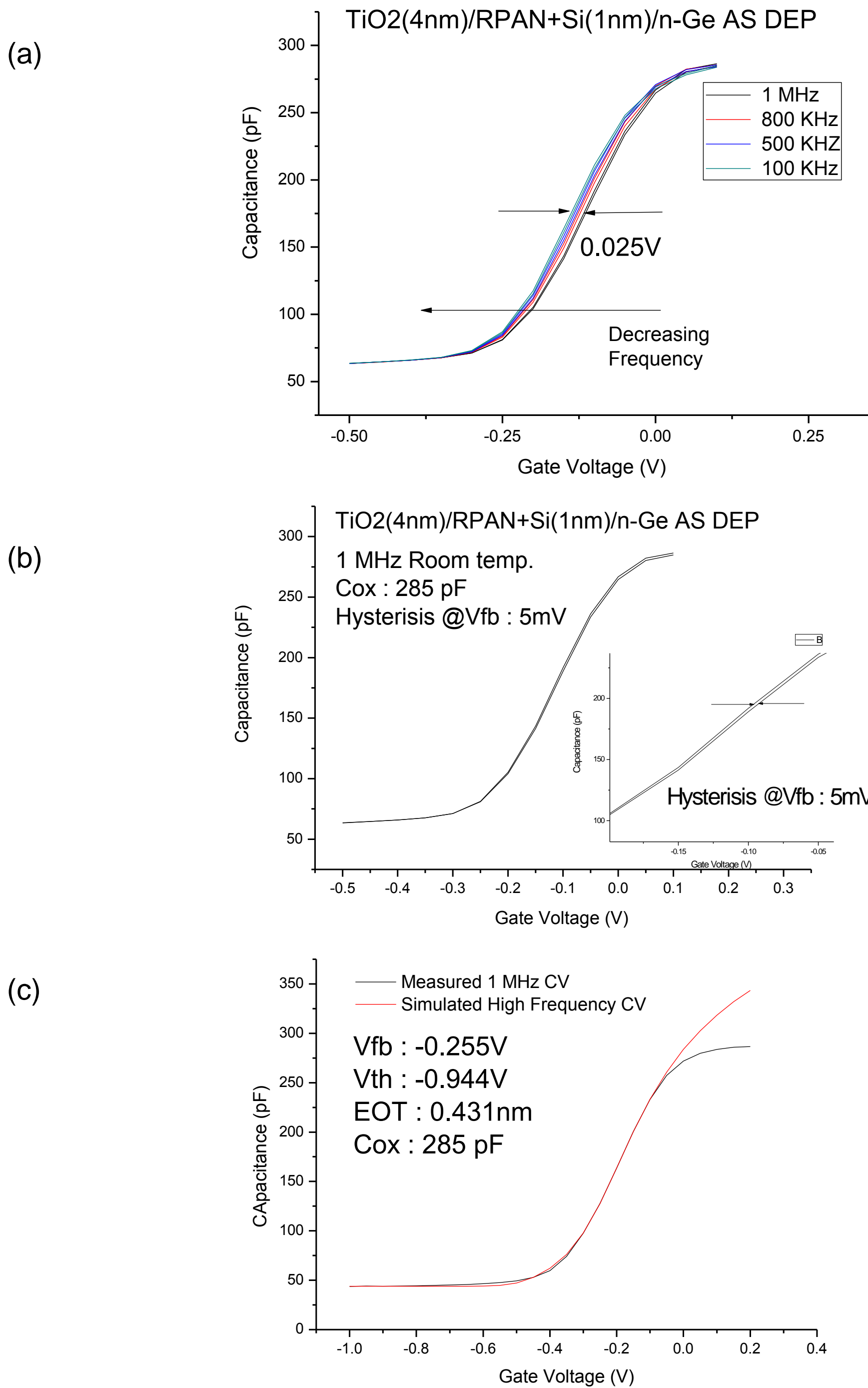
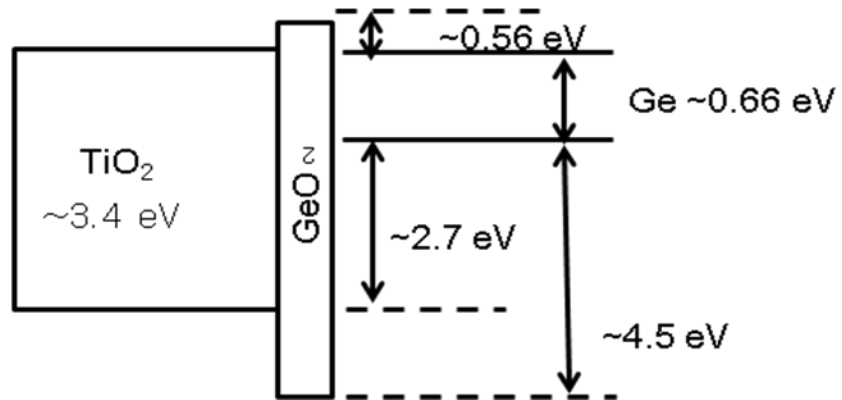


Figure 4.12 (a) the frequency dependence of C-V characteristics of as-deposited TiO_2 PMOS capacitors. (b) the retrace on the 1 MHz curve of device showed extremely low (~5mV) of hysteresis corresponds to slow trap density of 1.13 x 10^{10} cm^{-2}. (c) measured and calculated C-V curve of Ge PMOS capacitor.

(a)



(b)

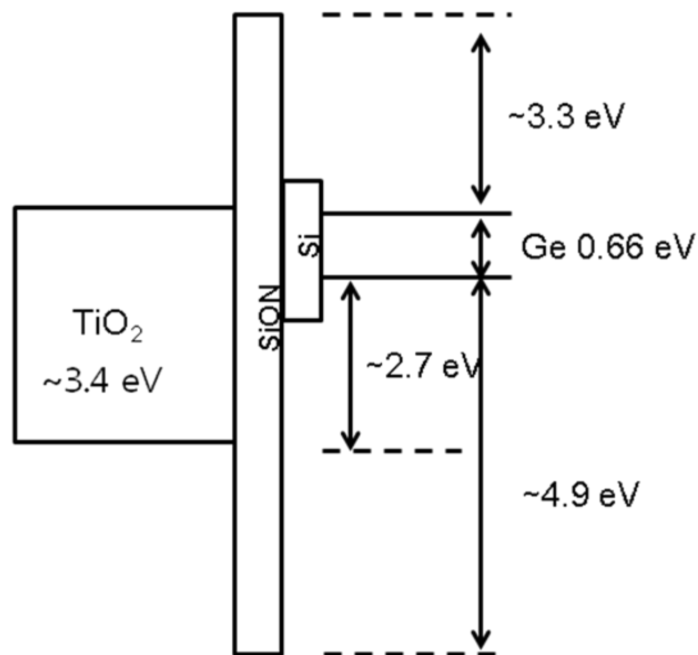


Figure 4.13. (a) and (b) the band alignments for TiO_2/GeO_2/n-Ge and TiO_2/RPN+Si/n-Ge gate stacks.

Table 4.1. Summary of electrical properties of HfSiON PMOS capacitors as a function of annealing temperature.

	EOT *(nm)*	V_{fb} (V)	Doping Density *(cm^{-3})*	Hysteresis (V)	*Oxide trapped charge density(cm^{-2})*	*Interface trap density (D_{it}) ($eV^{-1}cm^{-2}$)*
AS DEP	1.18	-0.36	~5.5 X 10^{17}	0.013	1.76X10^{10}	7X10^{11}
500 ℃	1.30	-0.28		0.012	1.49X10^{10}	5X10^{11}
600 ℃	0.86	-0.10		0	0	3X10^{11}
700 ℃	1.20	0.10		0.020	2.72X10^{10}	1X10^{12}

5 Effect of pseudomorphic Si passivation layer on Ge for HfSiON NMOS device

Abstract

Electrical properties of HfSiON with 1nm pseudomorphic silicon passivation and nitridation and on p-type Ge (100) substrates RPECVD have been investigated to solve critical issues of Ge n-MOSFETs. The suppression of interface states near the conduction band edge (E_c) was obtained by 1nm of pseudomorphic Si for HfiSiON Ge-NMOS device. Calculated N_f value from $V_{fb,\ ideal}$ and slow trap density were -5.15 x 10^{11} cm^{-2} and 5.21 x 10^{10} cm^{-2} respectively. The minimum D_{it} value was found from the observation of the maximum value of G_p / ω peaks at Vg=0.5 V to be 3.2x10^{11} cm^{-2} eV^{-1}. Low leakage current level inversion (substrate injection) supported the suppression of 'slow' surface states near the conduction band (E_c). HfiSiON with 1nm of pseudomorphic Si passivation layer grown by RPECVD can be novel structure to solve the asymmetric electron and hole mobility degradation in Ge device for the high performance Ge n-channel MOSFETs.

5.1 Introduction

Germanium has been spotlighted for an attractive channel material for future metal-oxide-semiconductor (MOS) field-effect transistors because its high intrinsic electron mobility (2X) and hole mobility (4X) as compared to the conventional channel material silicon. However, it is difficult to integrate into a MOS fabrication process because GeO_2 has inferior properties such as poor thermal stability and water solubility. Ge P-channel-MOSFETs with high-k gate dielectrics have been successfully demonstrated recently with enhanced hole mobility [1,2]. However, Ge N-channel MOSFETs have exhibited low mobility and poor drive currents, as reported by numerous research groups [3,4]. For instance, very large hysteresis and abnormal inversion capacitance dispersion for Ge NMOS have been commonly observed in many studies.

In this chapter, to investigate electrical properties of Ge-NMOS, pseudo-ternary HfSiON with 1nm pseudomorphic silicon passivation layer and on p-type Ge (100) substrates by RPECVD has been demonstrated.

5.2 Experimental Procedures

As received two-inch germanium wafers, prior to loading into the UHV environments, were wet-chemically cleaned by modified NH_4OH based cleaning procedure. Prior to deposit of high-k gate dielectrics, very thin 1nm pseudomorphic silicon layers were deposited onto n-type Ge (100) substrates at 300 °C by remote plasma enhanced chemical vapor deposition (RPECVD) with 2%-SiH_4 in He and He gases for 42 seconds for 1 nm thickness silicon layers. After pseudomorphic silicon deposition, the layer was exposed to reactive species

from a remote N_2/He discharge at 0.3 torr for nitridation for 15 seconds to provide chemical passivation to suppress further unwanted reaction between the deposited gate dielectrics and the Ge substrates. After surface passivation, HfSiON (4 nm) layers were deposited on films onto p-Ge (100) substrates at 300 °C by remote plasma enhanced chemical vapor deposition (RPECVD). Metal-oxide-semiconductor (MOS) capacitors were fabricated at the nanofabrication facility at North Carolina State University. The detailed procedure was described in the previous chapter. Electrical measurements were performed on a Material Development Corporation system. An HP 4284A LCR meter with a frequency range of 1 kHz to 1 MHz was used to perform capacitance-voltage measurements for capacitance dispersion.

5.3 Results and Discussion

Figure 5.1 shows the frequency dependence of C-V characteristics of as-deposited Al/HfSiON(2nm)/RPN+Si(1nm)/n-Ge NMOS capacitors. The capacitance was measured at various frequencies (100 kHz to 1 kHz) as a function of gate voltage and the capacitor was swept from inversion to accumulation at room temperature in the dark room. Figure 5.1 displayed small deviation of frequency dispersion in the accumulation region. No kinks were observed in the inversion region at all measured frequencies (100 kHz to 1 kHz) unlike previous studies [5,6]. Kinks are caused by interface traps located at the upper half of the germanium band gap. When the Fermi level crosses the midgap and approaches the upper half of the interface states (inversion), these interface states can lead to a large kink in the C-V curves [6,7]. Therefore, this exceptional result for *p*-type Ge MOS capacitor indicates

that interface states near the conduction band edge (E_c) were effectively suppressed by 1nm of pseudomorphic Si and nitridation deposited by RPECVD. The interface states near E_c have been reported as a major factor to degrade Ge *n*-channel MOSFET performances because it causes weak Fermi level pinning at the conduction band [7].

Previous reports on Ge MOS devices insist that abnormal inversion regime capacitance in Ge MOS devices is generally considered to originate from a much shorter minority carrier response time and higher minority carrier generation-recombination rate, due to the smaller band gap of Ge. However, in many previous reports on Ge MOS devices, frequency dispersion in the inversion regime is not unique and seems to depend on process conditions. This fact suggests that the minority carrier generation is caused not only by intrinsic thermal excitation across the Ge band gap but also by another excitation process, such as defect-assisted band tunneling. For instance, metal impurities diffusing into the near surface of the Ge substrate might create bulk trap levels that permit generation-recombination of minority carriers responsible for the abnormal inversion behavior. Hirayama *et. al.* reported that strong inversion response, like a MIM, at high frequency measurement for $ZrO_2/SiO_2/GeO_2$/p-Ge resulted from penetration of electrons in the depletion region from periphery of MOS capacitor [8]. Therefore, it is apparent that pseudomorphic silicon passivation layer by RPECVD enhances in reduced minimized minority carrier response result from suppressed defect assisted band tunneling.

As can be seen, flat band voltage shifts between measurement frequencies (100 kHz-1 kHz) which are the direct result of interface states were observed for around 0.050V. In addition, positive shift of V_{fb} from ideal V_{fb} was due to the amount of negative fixed charge

density.

In order to estimate the fixed oxide charge density (N_f), work function difference (Φ_{ms}) (or ideal flat band voltage) between Al gate and n-Ge substrate was calculated by following equation,

$$V_{FB,ideal} = \phi_M - (x_n + \frac{E_g}{2} + \phi_F) \quad (5.1)$$

where Φ_m is metal work function, X_n is electron affinity in Ge, E_g is Ge energy band gap, and $\phi_F = \frac{kT}{q} \ln \frac{N_D}{n_i} = 0.0447V$

The calculated Ideal flat band voltage ($V_{fb,\ ideal}$) for our devices was around -0.24 V for Al and p-Ge substrate. The calculated N_f value from $V_{fb,\ ideal}$ was -5.15 x 10^{11} cm^{-2}.

As shown in Figure 5.2, the retrace on the 1 MHz curve of this device shows only around 16mV of hysteresis corresponding to slow trap density of 5.21 x 10^{10} cm^{-2}. About 10 ~16 mV of hysteresis was found across the entire frequency range. It is noted that the 16mV hysteresis of NMOS device revealed negative ΔV_{fb}, which is equivalent to the small amount of positive charge (hole) trapping.

Figure 5.3 displays measured and calculated C-V curves at 100 kHz of a Ge NMOS capacitor. The determined net donor concentration (N_A), EOT, V_{fb} and threshold voltage (V_{th}) of each Ge MOS capacitor; (i) 2.1 x 10^{15} cm^{-3}, (ii) 1.621 nm, (iii) 0.38 V and (iv) 0.51 V respectively. EOT value (1.621nm) is very similar to HfSiON NMOS (1.623 nm) shown in chapter three indicating that uniform removal of the native oxide, stable structure of Si passivation layer and uniform high-k dielectrics growth.

In order to clarify the distribution of D_{it}, conductance method was used in this study. Figure 5.4 (a) shows the parallel conductance loss (G_p/ω) versus measured frequency (ω) curves at selected gate voltages. The peak amplitude $(G_p/\omega)_{max}$ increases with increasing bias. This can be explained by the continuous distribution of interface traps energy levels. The gate voltage was translated into the surface potential using Eq. (5.2) which is the Berglund integral of the quasi-static C-V curve [9].

$$\Psi_S(V_a) = \int_{V_{acc}}^{V_a} [1 - \frac{C(V_a)}{C_{OX}}] dV_a + \Delta \tag{5.2}$$

Assuming negligible series resistance, G_p/ω was obtained from [9]

$$\frac{G_p}{\omega} = \frac{\omega G_m C_{ox}{}^2}{G_m{}^2 + \omega^2 (C_{ox} - C_m)^2} \tag{5.3}$$

where G_m is the measured conductance and C_m is the measured capacitance. From f_D is the universal function as a function of the standard deviation of surface potential ($_s$), D_{it} of sample was calculated from [9].

$$D_{it} = \left(\frac{G_p}{\omega} \right)_{f\ p} \left[q f_D (\sigma_S) A \right]^{-1} \tag{5.4}$$

where f_p is the frequency corresponding to the peak value G_p/ω, q is the magnitude of

electronic charge, and A is the gate electrode area. The determined values of f_D was about 0.387. Figure 5.4 (b) shows energy distribution of D_{it} from the conductance measurements for Ge NMOS. The minimum D_{it} value was found from the observation of the maximum value of G_p / ω peaks at Vg=0.5 V to be 3.2x10^{11} cm^{-2} eV^{-1}. This density of interface states is approaching state-of-the-art Si/SiO_x /HfO_2 /metal gate stacks (typically mid to high 10^{10} cm^{-2} eV^{-1}).

The typical gate leakage density as a function of voltage bias is shown in Figure 5.5. Through a direct gate voltage bias sweeping, low leakage current level inversion (substrate injection) could help to explain the suppression of 'slow' surface states near the conduction band (E_c). To be more specific, a pseudomorphic Si passivation layer effectively suppresses the minority carrier trap (electron) under the positive gate bias (inversion). This observation may help to solve the asymmetric electron and hole mobility degradation in Ge n- and p-channel MOSFETs as demonstrated by previous studies [10,11]. Especially, degradation of n-channel carrier (i.e., electron) mobility due to Coulomb scattering with the filled acceptor states present at a higher D_{it} near the E_C edge would be improved by pseudomorphic Si passivation with nitridation [10].

Leakage current density at V_g-V_{fb}=1 was around 1.25 x 10^{-5} A/cm^{-2}.

5.4 Summary

Electrical properties of Ge-NMOS, pseudo-ternary HfSiON with 1nm pseudomorphic silicon passivation layer and on p-type Ge (100) substrates by remote plasma enhanced chemical vapor deposition (RPECVD) have been investigated. No kinks were observed in

the inversion region at all measured frequencies (100 kHz to 1 kHz) indicating that interface states near the conduction band edge (E_c) were effectively suppressed by 1nm of pseudomorphic Si. Calculated N_f value calculated form $V_{fb, ideal}$ and slow trap density were -5.15 x 10^{11} cm^{-2} and 5.21 x 10^{10} cm^{-2} respectively. The minimum D_{it} value was found from the observation of the maximum value of G_p/ω peaks at Vg=0.5 V to be 3.2x10^{11} cm^{-2} eV^{-1}.

Low leakage current level inversion (substrate injection) supported the suppression of 'slow' surface states near the conduction band (E_c).

5.5 References

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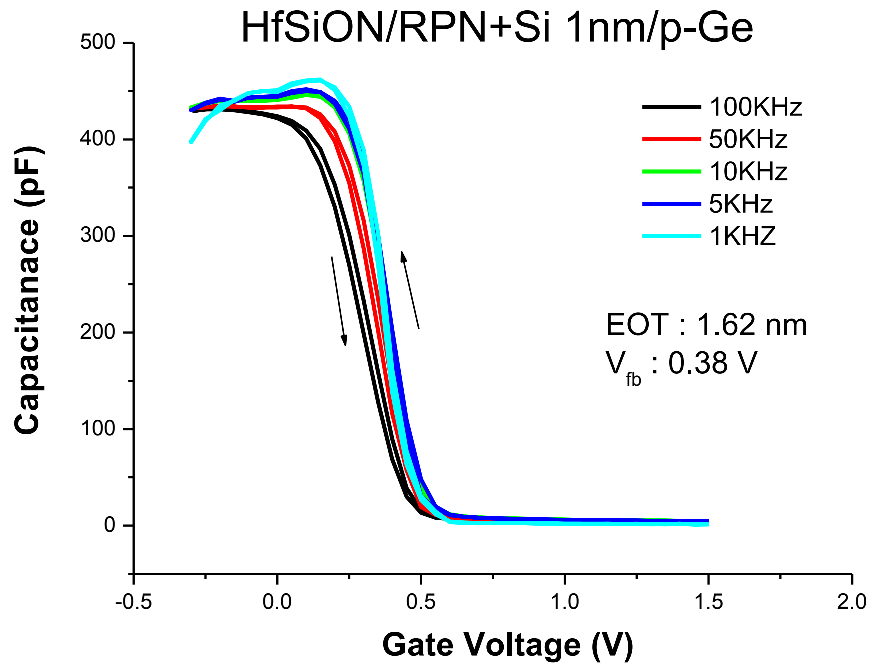


Figure 5.1. Frequency dependence of C-V characteristics of as-deposited Al/HfSiON/RPN+Si(1nm)/p-Ge NMOS capacitors.

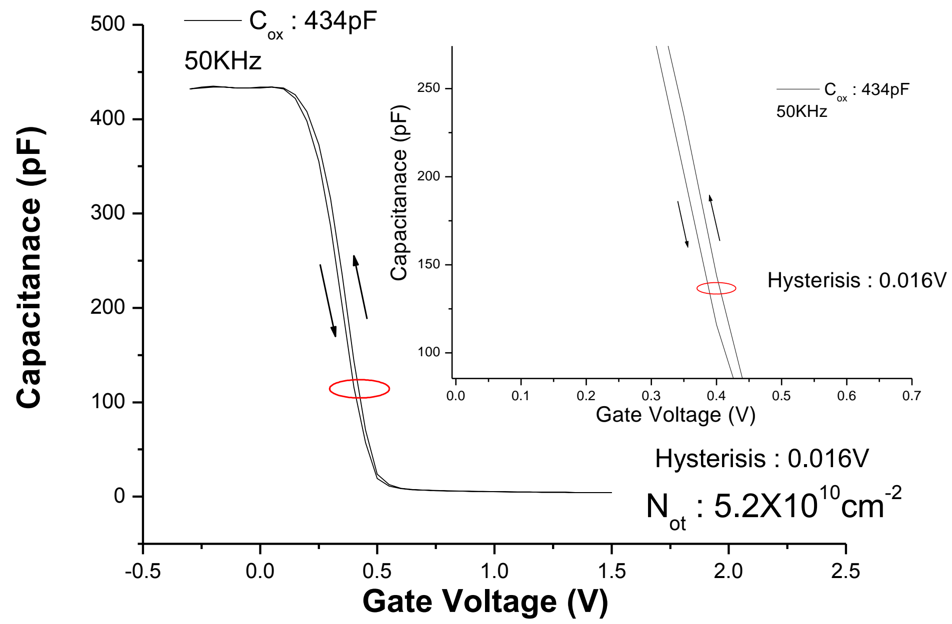


Figure 5.2. Bidirectional C-V characteristics of Al/HfSiON/RPN+Si(1nm)/p-Ge NMOS capacitors.

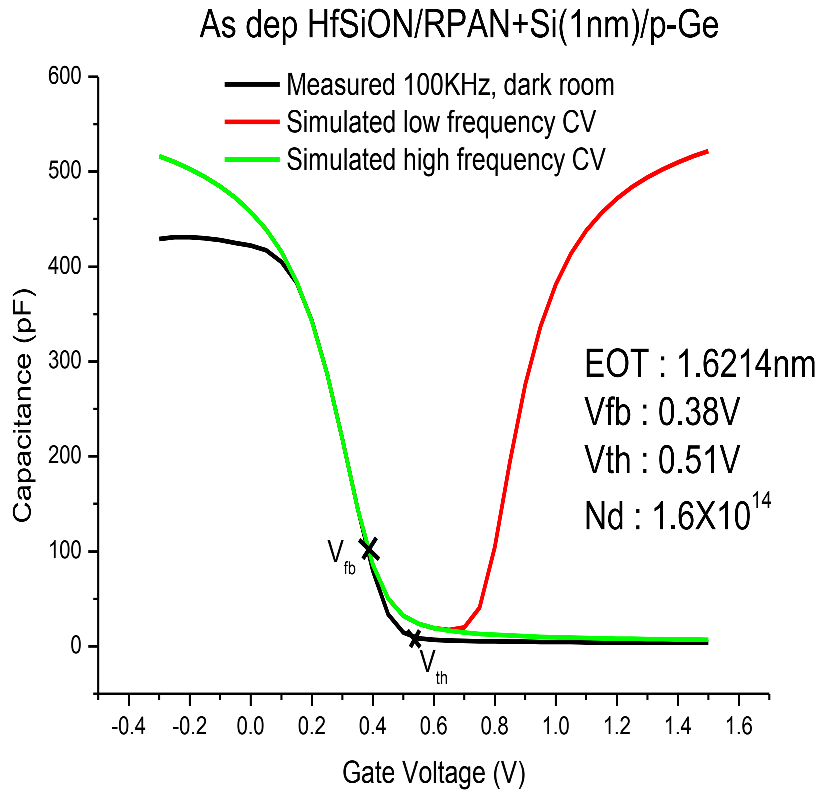
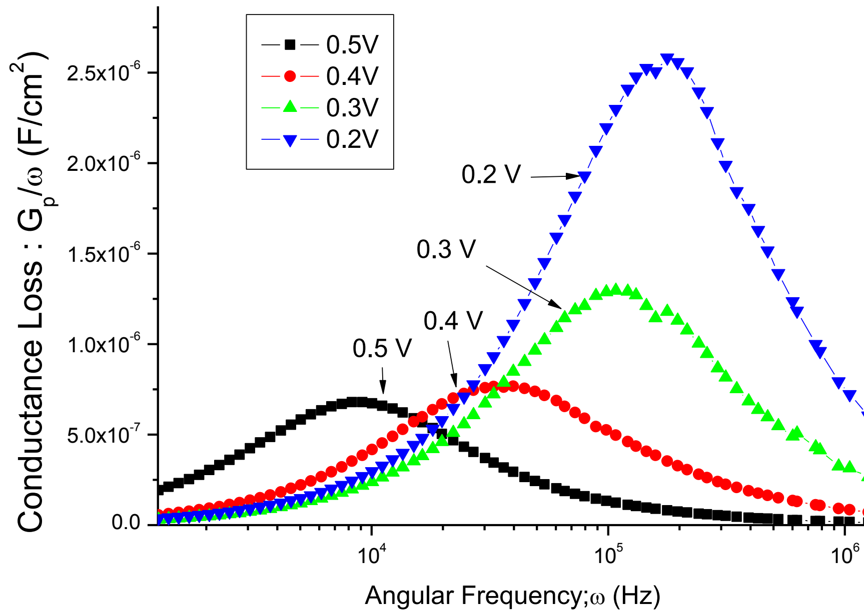


Figure 5.3. Measured and calculated C-V curves of Ge of Al/HfSiON/RPN+Si(1nm)/p-Ge NMOS capacitors.

(a)



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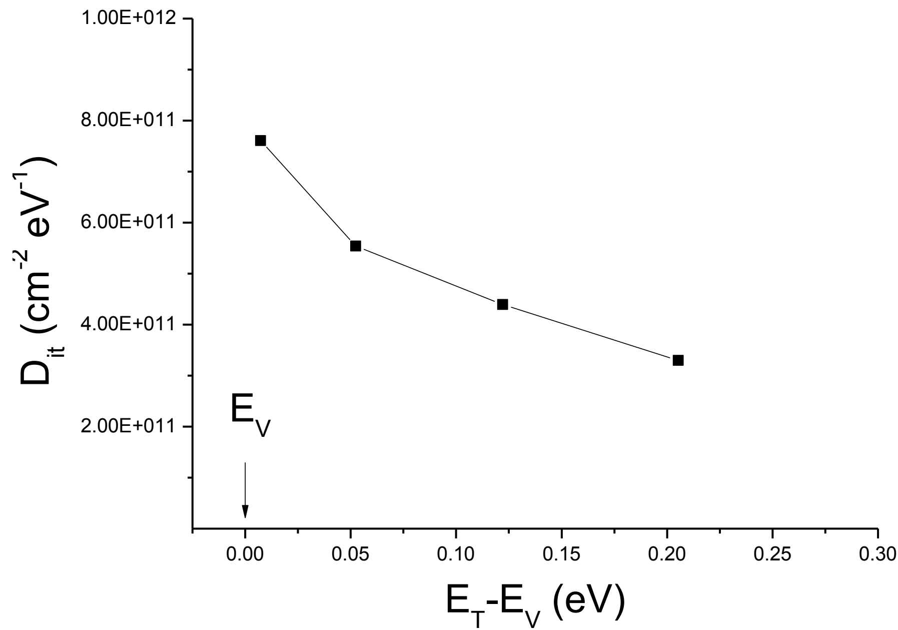

Figure 5.4. (a) the parallel conductance loss (G_p/ω) versus measured frequency (ω) curves at selected gate voltages.

(b) Energy distribution of interface traps in Al/HfSiON/RPN+Si(1nm)/p-Ge NMOS capacitors.

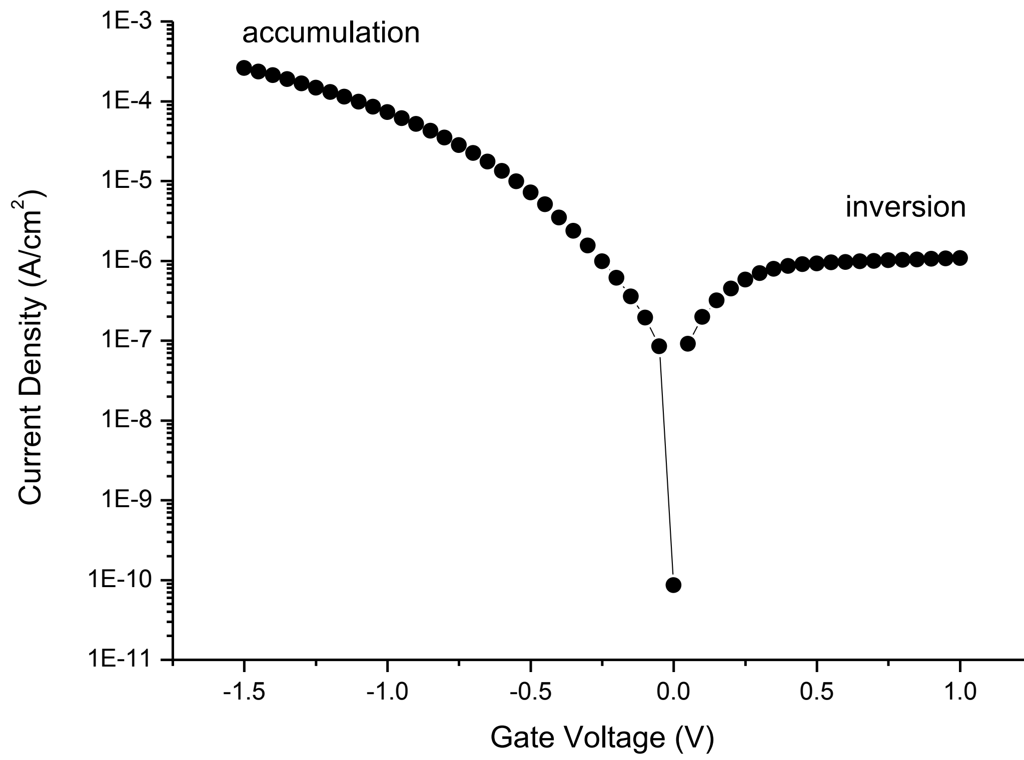

Figure 5.5. Leakage current characteristics of Al/HfSiON/RPN+Si(1nm)/p-Ge NMOS capacitors.

6 Concluding Remarks and Future Work

This dissertation study primarily focused on the investigation of pseudo-ternary Hf Si oxynitrde gate dielectrics and demonstrates the characteristic of pseudomorphic Si layer as an alternative passivation layer on Ge for application of Ge MOSFETs.

The summary of study on intrinsic properties of high-k materials and passivation layer is as following:

HfSiON gate stacks on Si show excellent electrical properties such as negligible frequency dispersion, absence of bumps at any regime, low hysteresis at all measurement frequency and minimal stretch out and very low leakage current level. However, the excellent properties of HfSiON on Si do not transfer to Ge with plasma nitridation. HfSiON Ge-MOS devices show inferior electrical properties such as large hysteresis, severe stretch out, bumps near depletion regime, and severe frequency dispersion due to incorporation of Ge into gate dielectrics. In case of the 650 °C device, improved interface quality is obtained, but D_{it} in the lower half of the band gap still leads to bumps where the sizes are frequency dependent. Therefore, alternative passivation techniques should be explored to improve performance for Ge MOSFETs.

The combination of a pseudomorphic Si layer followed by nitridation using RPECVD has been developed and yields a high quality passivation layer on Ge. HfSiON Ge MOS capacitor with very thin (on the order of 1nm) Si layer with plasma nitridation achieved dramatic improvements such as negligible hysteresis, no kinks at any regime, and minimal stretch out.

This unprecedented result for *n*-type Ge MOS capacitor indicates that interface states near the valence band edge (E_v) were effectively suppressed by 1nm of pseudomorphic Si and nitridation deposited by RPECVD. In addition, it is noteworthy that 1nm of pseudomorphic Si with nitridation by RPECVD has thermal stability at 700 °C anneal because the existence of the Si passivation layer is still present even though partial consumption of the Si passivation layer. This thermally stable passivation layer effectively suppresses Ge interdiffusion into dielectrics and GeO_x or other oxidation states formation during dielectric deposition and further device processing.

Furthermore, dramatic improvements were obtained after 600°C anneal for HfSiON (2nm) Ge PMOS with same passivation. It is remarkable that zero hysteresis corresponding to zero slow trap density and EOT of 0.86 nm were achieved for 600°C annealed HfSiON (2nm) Ge PMOS capacitor.

Suppression of interface states near the conduction band edge (E_c) was also achieved by HfSiON with same passivation p-type Ge MOS device. Therefore, HfSiON with 1nm of pseudomorphic Si with nitridation layer s a novel structure to solve the asymmetric electron and hole mobility of Ge device for high performance Ge n-channel MOSFETs. As a suggestion for future study, more accurate spectroscopic studies for this gate dielectric with regard to the origin of defect states are required. In order to high performance Ge-MOSFET applications, more specific in-situ thermal or H_2 plasma cleaning should be explored to remove the inevitable native germanium oxide formation due to oxidation after ex-situ chemical clean. Other candidate high-k materials such as $TiO_{2,}$ TiSiON, and TiON on Ge should be investigated for the 20nm node Ge MOSFETs.