ABSTRACT

ZHAO, TIEFU. Design and Control of a Cascaded H-Bridge Converter based Solid State Transformer (SST). (Under the direction of Dr. Alex Huang.)

As a result of the recent development of the smart grid system, it is inevitable that the future of power generation and distribution will involve a high degree of distributed resources interconnected to the gird via fully-rated power electronic interface. The interface is required to add functionalities, such as voltage regulation and reactive power compensation, intelligent power management and plug-and-play features for the distribution resources. The motivation for this dissertation is to design a new solid state transformer to replace the most commonly used, 100-year old interface --- distribution transformers.

The purpose of this research has been to design a cascaded H-Bridge converter based Solid State Transformer (SST) and to investigate control methods and the hardware implementation. The SST, including AC/DC rectifier, Dual Active Bridge (DAB) and DC/AC inverter is designed to interface with the single phase 7.2kV distribution system.

First, the switching model, average model and small signal model of the SST are developed. The SST controller is designed based on the small signal model bode plot. The average and switching model simulation are implemented to verify the proposed SST features.

Due to the characteristics of cascaded H-bridge converters, the voltage unbalance can appear on DC buses of different H-bridges. Meanwhile, the power unbalance also becomes unavoidable for the parallel DAB modules. In this dissertation, a new voltage balance controller is proposed to balance the cascaded H-Bridge capacitor voltages. The intrinsic

constraints of the voltage balance control for the cascaded H-Bridge topology are derived. Meanwhile, a new power balance control method is proposed to balance the parallel DAB power in the SST. The proposed balance method is verified by simulations and experiments.

Furthermore, a new feed-forward power ripple control is proposed and a power synchronization method is designed to minimize the DC bus voltage ripple and the required capacitor size. Finally, the SST rectifier hardware prototype is designed and implemented. The SST features and controller are verified by the hardware experiment.

In order to investigate the feasibility of the SST for future substations, a higher power rating and higher voltage substation solid state transformer is designed based on the 10 kV SiC MOSFET and PIN diodes. A novel Zero Voltage Switching (ZVS) operation for a five-level DC/DC converter is proposed to reduce the device switching loss and verified by the simulations.

Design and Control of a Cascaded H-Bridge Converter based
Solid State Transformer (SST)

by
Tiefu Zhao

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DEDICATION

To my dearest wife Yang Sun,

Your love means everything to me.

BIOGRAPHY

Tiefu Zhao received his B.S. and M.S. degrees in Electrical Engineering from Tsinghua University, Beijing, China in 2003 and 2005, respectively. Since 2005, he has been working toward the Ph.D. degree in Electrical Engineering at North Carolina State University under the direction of Dr. Alex Huang.

From 2006 to 2008, he has been a research assistant at the Semiconductor Power Electronics Center (SPEC), North Carolina State University. Since 2008, he has been a research assistant at NSF FREEDM Systems Center, North Carolina State University. His research interests include solid state transformer, renewable energy, smart grid, FACTS and SiC power devices.

Tiefu Zhao is a member of honor society Phi Kappa Phi and a student member of IEEE (Institute of Electrical and Electronics Engineers).

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Finally, I would like to dedicate this thesis to my wife, Yang Sun and my parents, Decai Zhao and Yajun Sun. Their support and love make my Ph. D. study a happy journey.

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Chapter 1. Introduction

1.1. Introduction to distribution transformers

Little more than a hundred years ago, there were no light bulbs, refrigerators, air conditioners, or any of the other electrical marvels that we think of as being so essential today. Today's enormous electric utility industry began in the nineteenth century with the scientific descriptions of electricity and magnetism by giants such as Hans Christian Oersted, Andr´e Marie Amp`ere, and James Clerk Maxwell [1].

Later in the early 1900s, as an alternative to Thomas Edison's DC power system, Westinghouse introduced an AC power system based on a transformer technology that can easily step up or step down AC voltage levels as required for power transmission, distribution, and consumption. The transformer enables the widespread development of today's power systems.

Currently, transformers with a history of 100 years are widely used in electric power distribution conversion systems to perform many functions, such as isolation, voltage transformation, noise decoupling, etc. The distribution transformers are used at almost every site where utility power is delivered. These distribution transformers reduce the voltage to a more usable level, typically 480/277V (for three-phase application) or 208/120V or 240/120V (for single-phase application).

Table 1.1 lists the characteristics of distribution transformers typically used in the United States [2]. There are two primary types of conventional distribution transformer: liquid-immersed and dry-type. The vast majority of distribution transformers on the utility-owned distribution system are liquid-immersed, while those used in commercial and industrial applications are predominantly dry-type.

Table 1.1 Characteristics of distribution transformers typically used in U.S.

Transformer Type	Phase	Primary Voltage (kV)	Secondary Voltage (V)	Capacities (kVA)
Liquid-immersed	1	34.5 and below	600 and below	1–500
Liquid-immersed	3	34.5 and below	600 and below	3–2500
Dry-type	1	34.5 and below	600 and below	15–833
Dry-type	3	34.5 and below	600 and below	15–2500
Dry-type	1and 3	34.5 and below	600 and below	0.25–15

Liquid-immersed transformers typically use oil as both a coolant (removing heat from the core and coil assembly) and a dielectric medium (preventing electrical arcing across the windings). Liquid-immersed transformers are typically used only outdoors because of concerns over oil spills or fire if the oil temperature reaches the flash-point level. Dry-type transformers are air-cooled, fire-resistant devices that do not use oil or other liquid insulating/cooling media. Due to the physics of their construction (including the ability of these units to transfer heat), dry-type units have higher losses than liquid-immersed units and are larger than liquid-immersed units for the same voltage and/or kVA capacity. However, dry-type transformers are an important part of the transformer market because they offer safety, environmental, and application advantages for industrial and commercial customers.

1.2. Motivations of solid state transformers

The positive attributes of conventional distribution transformers, well documented for years, include low cost, high reliability, and high efficiency. However, these conventional copper-and-iron based transformers possess many undesirable drawbacks. These drawbacks include large size and weight, voltage drop under load, power quality susceptibility, sensitivity to harmonics, environmental concerns when leaks of mineral oil occur, and no DC output or energy-storage capacity.

Due to their bulky iron cores and heavy copper windings, conventional transformers are by far one of the heaviest components in an electrical distribution system. The size and weight of the transformer is primarily a function of the saturation flux density of the core material and maximum allowable core and winding temperature rise [1]. The saturation flux density is inversely proportional to frequency, and hence increasing the frequency allows higher utilization of the steel magnetic core and reduction in transformer size. However, because the operating frequency of commercial power is ordinarily fixed (60 Hz in the U.S.), the volume and the weight of the distribution transformer cannot be reduced below its definite values. Moreover, with the increased cost in basic materials such as copper and laminated steel, the SST, which uses much less copper, is potentially attractive. This is even more important to the higher power SST because today's 2.7 MVA transformer weighs more than six tons and uses a large amount of copper and steel. As shown in Figure 1.1, the estimated core size significantly decreases as the frequency increases [3]. Our study indicates that a 3X size and weight reduction is possible with 20kHz high voltage SiC power devices.

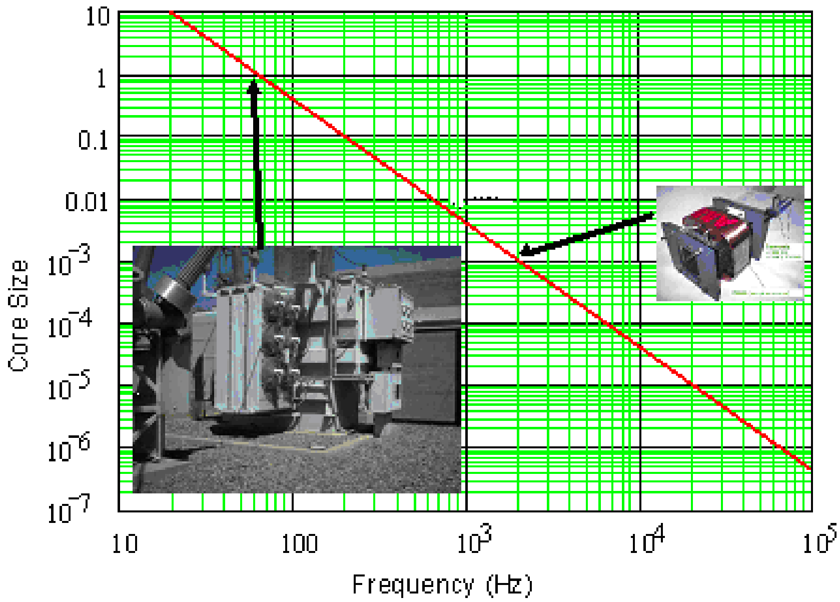


Figure 1.1 Transformer core size and frequency relationship

The output of the conventional transformers can be easily interrupted because of a disturbance at the input. When a voltage sag occurs on the grid side, the output voltage is affected inevitably. Meanwhile, when the output load has harmonic distortions or faults, the conventional transformer reflects them back to the input side. This becomes an increasing power quality concern in today's power system.

While some major improvements have occurred in transformer technology from time to time, other developments in the areas of core, winding, insulation, and dielectric liquids have provided only incremental improvements in transformer technology.

As the development of the smart grid infrastructure and the increase of the penetration of distributed generations, there is a strong desire to have intelligent transformers which can enhance the power quality performance, reduce transformer size and eliminate oil, increase the functionality, and provide the capability to actively manage the power and allow for easy connection of the distribution resources. The solid state transformer is a revolutionary power electronics device which will bring a quantum leap in iron-and-copper distribution transformer technology and better facilitate the future smart grid infrastructure.

1.3. Literature review --- State-of-the-Art of solid state transformer topologies

The idea of a “solid-state transformer” has been discussed since 1970 [4]. The initial purpose of solid-state transformers is to convert AC to AC for step-up or step-down with a function the same as that of a conventional transformer.

In 1970, W. McMurray form G.E. first introduced a high frequency link AC/AC converter, which became the basis for the solid state transformer based on direct AC/AC converter [5].

In 1980, Navy researchers proposed a power-electronic transformer that consisted of an AC/AC buck converter shown in Figure 1.2 to reduce the input voltage to a lower one [6]. This was followed in 1995 by a similar Electrical Power Research Institute (EPRI) sponsored effort [7]. Both of these efforts yielded working prototypes, but they operated at power and primary voltage levels that were orders of magnitude below utility distribution levels. The drawbacks of this approach also include the use of series tied devices, lack of magnetic isolation, inability to correct load power factor, and inability to prevent load harmonics from propagating into the primary-voltage system.

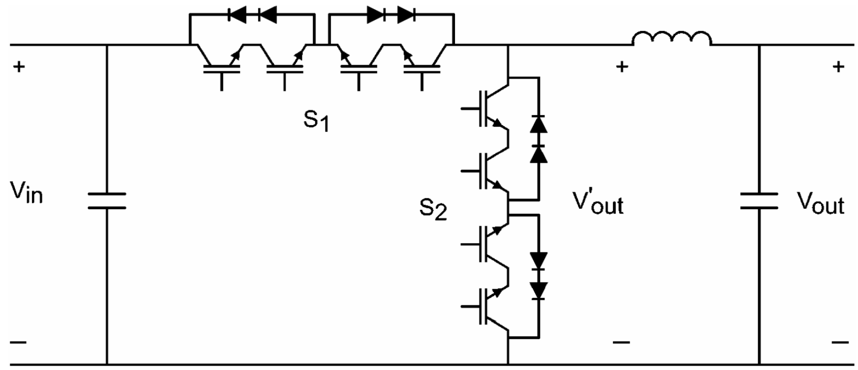


Figure 1.2 AC/AC Buck Converter

In 1996, Koosuke Harada proposed a new "intelligent transformer" [8], which significantly reduce the size of transformers by performing high frequency link. Various functions, such as constant voltage and constant power are realized by phase control. The paper also discussed the implementation of the concept on a 200V 3kVA unit operating at 15 kHz. The overall efficiency was reported to be about 80% and is viewed as a major disadvantage.

The earlier research on solid state transformers is limited by the power device and high voltage high power converter technologies of the time. Therefore, although various designs are proposed, none of them finally comes into practice; especially very little progress on distribution level transformers (above 10kV). By the 1990s, significant progress has been achieved in distribution system solid state transformers [9][10][11][12].

A high-power AC/AC conversion has been proposed by Moonshik Kang and Enjeti from Texas A&M University [9][13]. For that topology, shown in Figure 1.3, the incoming AC waveform is modulated by a power-electronic converter to a high-frequency square wave and passed through a small high-frequency transformer. This scheme has the benefit of reducing the transformer size and weight and the stress factor is more reasonable, but it does not provide any benefits in terms of control or power-factor improvement.

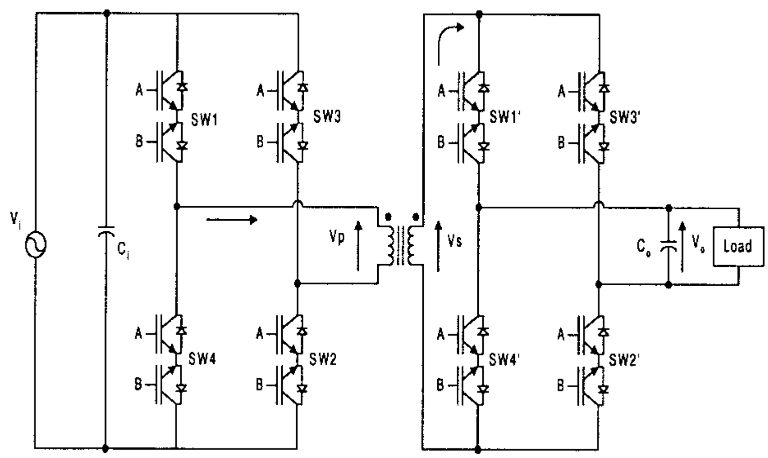


Figure 1.3 High frequency AC link converter

In 1999, a new structure of SST was introduced by Sudhoff shown in Figure 1.4 [4]. This topology contains three cascaded converters which are power factor controller, isolated DC/DC converter and voltage source inverter. The traditional 60 Hz transformer is replaced by a high frequency transformer plus solid state devices, which is the key to achieve size and weight reduction. These converters are used for programming input current waveform, electrical isolation and output voltage regulation, respectively. In this topology, to operate properly at medium voltage levels, the series to parallel connection of converters has been used. The number of series converters depends on voltage levels and the type of semiconductors.

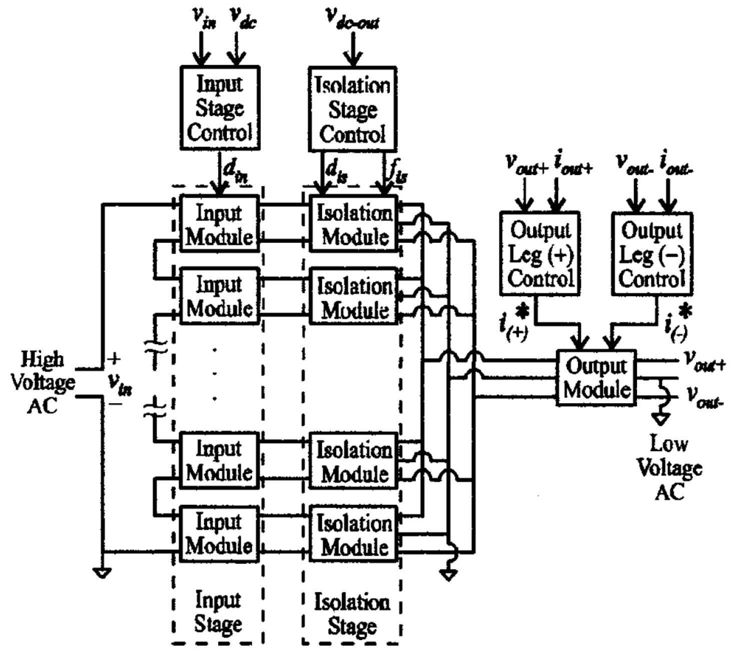


Figure 1.4 Three-stage solid state transformer.

Electrical Power Research Institute (EPRI) has been researching the Intelligent Universal Transformer (IUT) since 2002 [2][14][15][16]. The IUT topology is shown in Figure 1.5. It is proposed to replace conventional distribution transformers with the multilevel power electronic systems. An intelligent and controllable system can provide multiple transformer functions, such as voltage transformation, voltage regulation, non-standard customer voltages (DC or 400 Hz AC), voltage sag correction, power factor control, and distribution system status monitoring to facilitate automation.

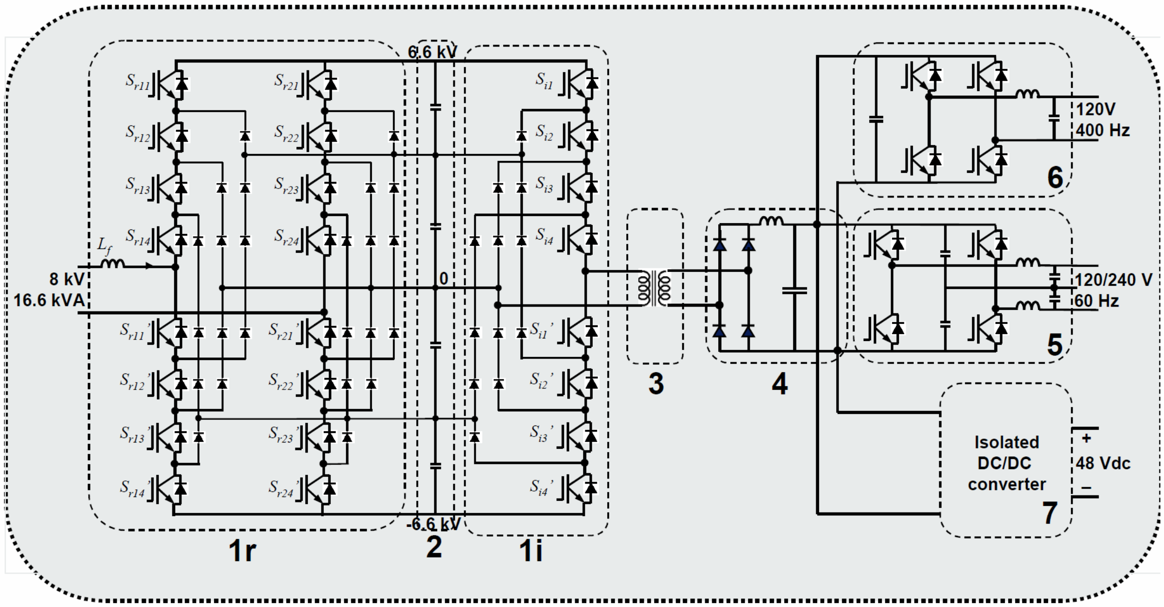


Figure 1.5 EPRI Intelligent transformer topology

The advancement and availability of high-voltage semiconductor devices have shed light on viable solid state based transformers for distribution systems. There are two possible approaches for realizing the goal of a solid state transformer. The hybrid design is based on using a conventional transformer and integration of power electronics systems on the secondary side of the transformer [17][18]. The all-solid-state designs, on the other hand, provide a fundamentally different and more complete approach in transformer design by using some form of power electronics (on the primary as well as the secondary side) as the interface with the utility AC system.

The most practical solutions are the solid state transformers proposed by Sudhoff from Purdue University and the intelligent transformer proposed by EPRI. Purdue has implemented a 7.2kV to 240/120V distribution transformer prototype, however no update has been found after 2002. Silicon Power is working with EPRI on the intelligent transformer with a different topology. All the previous designs are all focused on the replacement of the distribution transformer with additional functionalities, so none of them has bidirectional power flow capability and there is no proposed infrastructure to connect today's distribution resources. In the next section, a solid state transformer is proposed to facilitate the smart grid infrastructure.

1.4. SST development with Silicon and SiC devices

Although silicon power devices have served the power electronics industry well for more than five decades, silicon based technology is reaching its physical limits for power handling and switching frequency capability. The high-voltage silicon power devices have achieved a very large power handling capability by increasing current handling to more than 1,500A per device, however their voltage capability is typically below 6.5kV, and their frequency capability is normally below 1 kHz. Moreover, these silicon power devices normally cannot be used at temperatures higher than 125°C in power electronic systems.

With the rapid development of the wide-bandgap SiC material, SiC devices become the most promising post-silicon alternatives because of its superior properties, e.g., ten times higher breakdown electric field, higher thermal conductivity and much lower intrinsic carrier concentration [19][20][21][22][23]. The SiC device is a viable option even at high voltages while still maintaining a high switching speed. Therefore, it is possible to apply high frequency PWM converters in electric power transmission and distribution applications that are traditionally not feasible with slower silicon bipolar devices [24][25][26][27]. Enabled by high voltage SiC device, the substation solid-state transformer (SST) with high frequency power electronics converter is becoming practical to replace the conventional transformers.

1.4.1. *Solid State Transformer based on Silicon devices*

The most commonly used power electronic converter topology is the two-level converters. A two-level converter based SST system diagram is shown in Figure 1.6. Even using the highest available power rating 6.5kV IGBTs, a two-level converter based SST can only interface with 2.4kV AC voltage. In order to apply the silicon based SST to a distribution voltage level 7.2kV/12kV, multi-level converter topology is inevitable [19] [28] [29][30][31]. The cascaded H-Bridge multi-level converter based SST system is shown in Figure 1.7.

By using commercially available low voltage low current devices and components, a standardized, integrated and modularized solid state transformer can be designed. A modular SST example is presented for single phase 12kV 60Hz AC, power rating 5kW, output 120V 60Hz AC. The high voltage DC bus of each modular converter can be designed as 400V, low voltage DC bus 200V. To establish an equivalent 18kV DC bus, 45 converter cells are in series at the input (shown in Figure 1.8). Meanwhile, to share the high output current, all the converter cells are paralleled at the output. The high voltage side current is less than 0.42A. The low voltage side current is less than 5kW/120V/45=0.93A. So 600V 1A devices could be selected to construct the low voltage H-Bridges. The advantages of modular SST is that only low voltage H-Bridges are needed for the entire SST, and the system is easy to upgrade by adding on new modular SST cells.

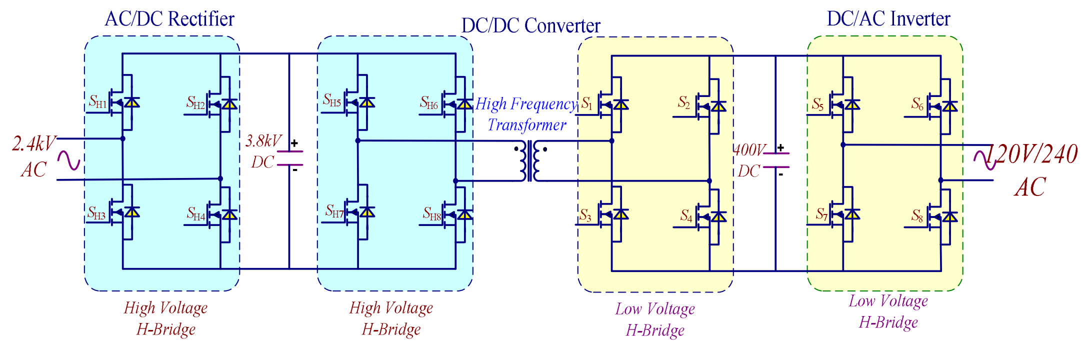


Figure 1.6 SST based on two-level converters

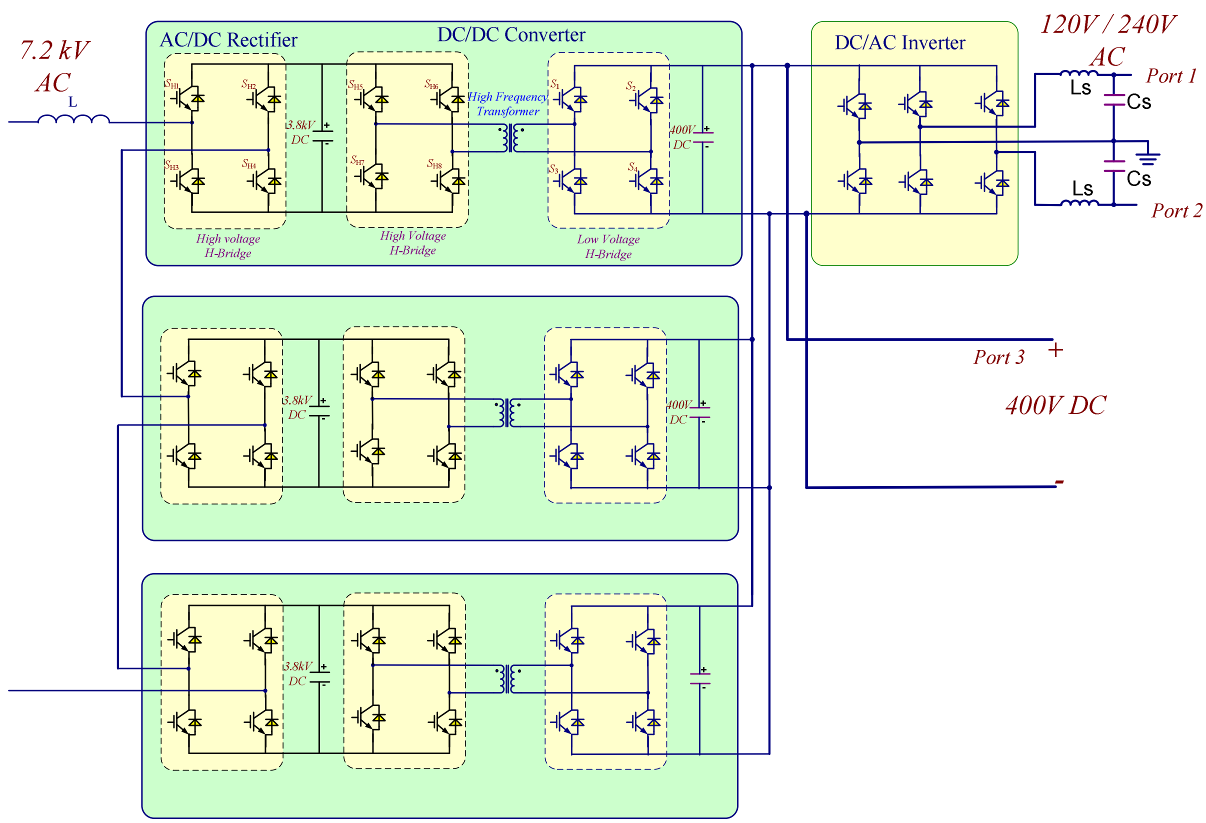


Figure 1.7 Topology of multi-level converter SST

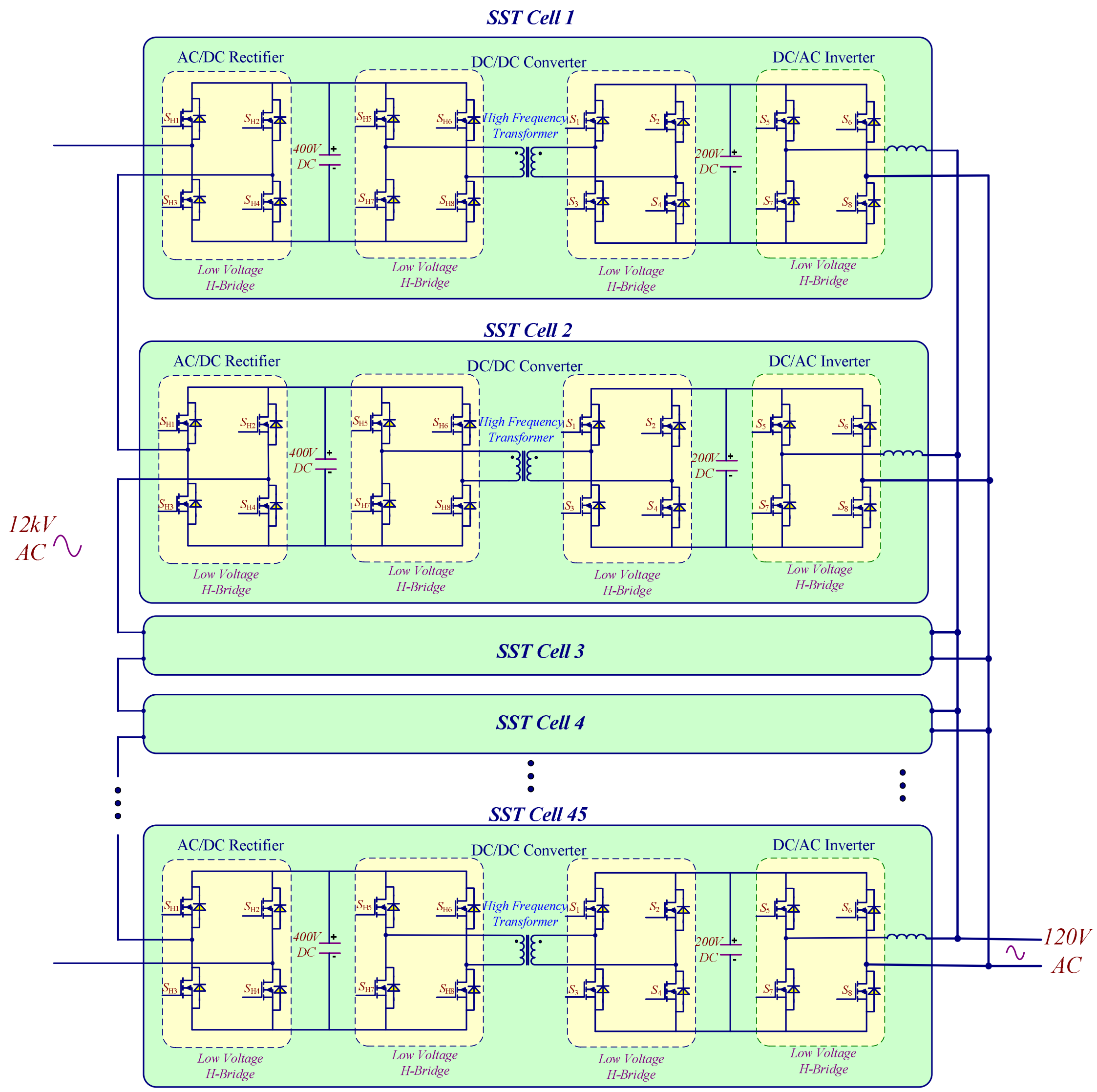


Figure 1.8 Modular solid state transformer with low voltage silicon devices

1.4.2. *Solid State Transformer based on SiC devices*

Enabled by high voltage SiC device, solid-state transformer (SST) is endowed with new opportunities to simplify the complicated topology due to the silicon device limitation. 10 kV SiC MOSFET and PIN or JBS diodes are currently being developed by a number of organizations. With 20kV or 10kV SiC device, the SST only needs two-level or three-level converters to sustain the distribution level voltage (12kV).

For the same system requirement as the modular SST in Figure 1.8 (single phase 7.2kV 60Hz AC, power rating 5kW, output 120V 60Hz AC), the followings are two solutions with SiC high voltage devices.

Solution 1: Two level converter, SST based on 15kV SiC IGBT

The high voltage H-Bridges are designed with 15kV SiC IGBT in Figure 1.9. Due to the high voltage devices, a typical two-level H-Bridge converter is enough to sustain the high input voltage. The high voltage DC bus is 12kV, and low voltage DC bus is 400V. The actual device currents are depending on the control and modulation method. However, the RMS current could be estimated as less than 0.42A.

In the low voltage stage, the RMS current of each device is less than 5kW/120V=42A. So 600V 50A silicon devices with proper heatsink could be used for the low voltage H-Bridges.

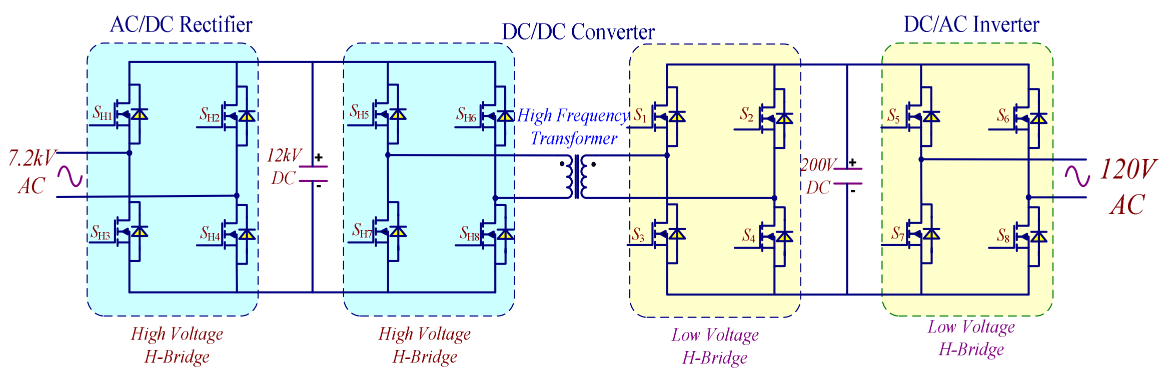


Figure 1.9 SST based on 15kV SiC IGBT

Solution 2: Three level converter, SST based on 10kV SiC MOSFET

With 10kV SiC MOSFET, a three-level neutral point clamped H-Bridge converter can be applied in high voltage stage. As shown in Figure 1.10. The high voltage DC bus is 18kV (each capacitor voltage 9kV), low voltage DC bus is 200V. The device RMS current in high voltage side is less than 0.42A. The low voltage side is the same as in solution 1.

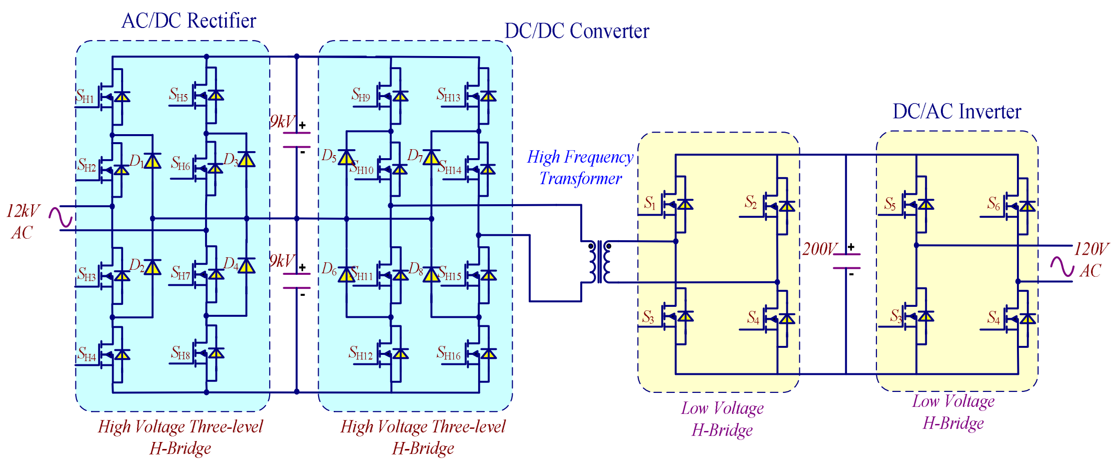


Figure 1.10 SST based on 10kV SiC MOSFET

The high voltage SiC devices make the simple two-level and three-level converter topology possible for the SST in 7.2kV distribution level. Similar to the modular SST, the higher voltage level 69kV can also be interfaced by SiC multi-level converters based SST. As the most promising postsilicon device, the SiC device can break the silicon theoretical limits because of the superior properties of SiC material, which enables simple SST topology and higher SST voltage.

1.5. Research background

The Future Renewable Electric Energy Delivery and Management (FREEDM) Systems proposes a smart-grid paradigm shift to prepare the U.S. to take advantage of advances in renewable energy for a secure and sustainable future. In the electric configuration of the FREEDM system shown in Figure 1.11, low voltage (120V), residential class Distributed Renewable Energy Resource (DRER), Distributed Energy Storage Device (DESD), and loads are connected to the distribution bus (12kV) through a revolutionary, highly efficient power electronics based Intelligent Energy Management (IEM) subsystem. Each IEM consists of a Solid State Transformer (SST) and its intelligent controller. The IEM will have bi-directional energy flow control capability allowing it to provide key plug-and-play features and isolate the system from faults on the user side. An Intelligent Fault Management (IFM) subsystem will be used to isolate potential faults in the 12 kV primary distribution grid. The IEMs and IFMs will communicate with each other via a Reliable and Secured Communication (RSC) network. The brain of the FREEDM system will be provided by the Distributed Grid Intelligence (DGI) software embedded in each IEM and IFM. Most energy storage requirements are provided by DESDs (which can be Plug-in Hybrid Vehicles - PHEVs), but an additional energy storage device may be considered necessary to satisfy the global need. The FREEDM system will be connected to the traditional grid through a higher power IEM. Industry users requiring 480V three-phase power will be connected to the FREEDM system through a medium power IEM.

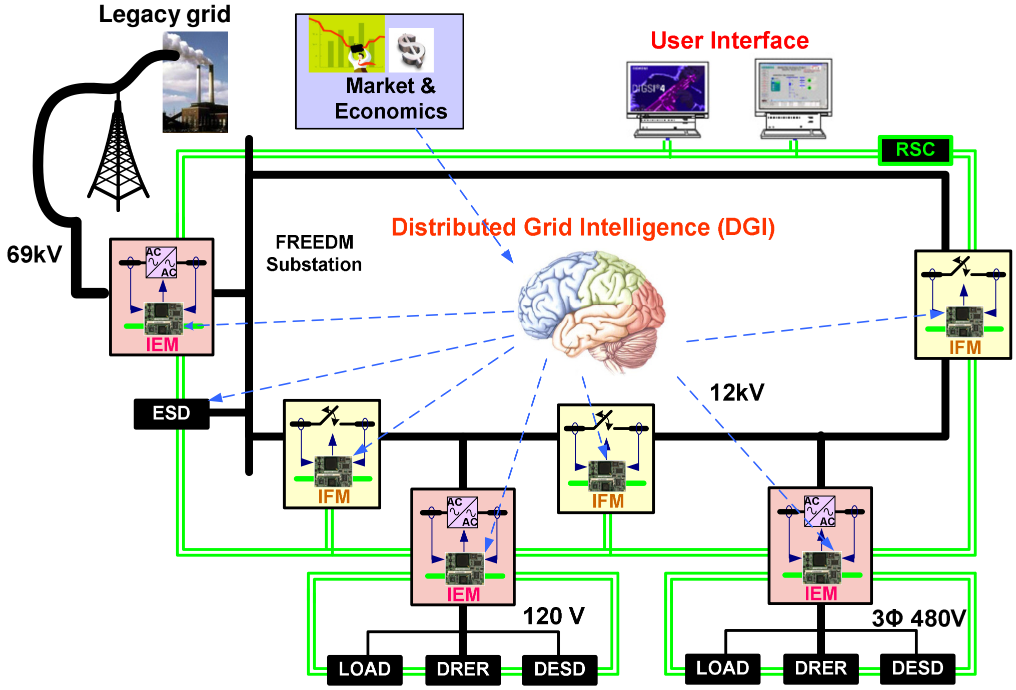


Figure 1.11 FREEDM Systems Diagram (IEM: Intelligent Energy Management, IFM: Intelligent Fault Management, DRER: Distributed Renewable Energy Resource, DESD: Distributed Energy Storage Device)

The proposed solid state transformer in the IEM is used to enable active management of DRER, DESD and loads, rather than a 60 Hz traditional transformer. The four-quadrant power flow control provided by the SST allows the plug-and-play of distributed generation and also allows for the addition of storages and loads to the grid with no adverse effects on nearby users. The SST will provide power quality improvement to residential users and industry customers. The FREEDM system understands the value of different types of energy and maximizes green energy utilization, which improves the energy efficiency of the total system.

The concept of the "solid-state transformer" has been discussed since 1970. However, the earlier research on solid state transformers is limited by the high voltage power device technologies of the time. Therefore, none of the SST designs ultimately comes into practice; in particular very little progress was made on the distribution level (above 10kV) transformer.

With advanced wide-band gap semiconductor devices such as 10kV SiC MOSFET, a much higher frequency (10 kHz instead of 60Hz) can be used to reduce the transformer size and weight, making the SST a valid option to replace the conventional transformers at the distribution voltage levels. Moreover, with the increased cost in basic materials such as copper and laminated steel, the SST, which uses much less copper, is potentially attractive. The Gen-I SST is still based on the 6.5kV silicon IGBT device, so a multilevel converter is needed to interface with the 7.2kV distribution level voltage. The FREEDM system center will use revolutionary post-silicon (HV SiC) power devices, 15kV SiC IGBT and 15kV SiC DMOSFET, to construct a compact, highly efficient, and robust Gen-II SST to demonstrate the FREEDM system.

1.6. Cascaded H-Bridge Converter based Solid State Transformer

The proposed 20kVA cascaded H-Bridge multilevel converter based solid state transformer directly interfaces with 12kV distribution voltage level. The solid state transformer consists of a cascaded multilevel AC/DC rectifier, Dual Active Bridge (DAB) converters with high frequency transformers and a DC/AC inverter.

The Solid State Transformer (SST) is the interface device between the distribution system and the electricity consumers in future smart grid systems. In the electric configuration of the smart grid system shown in Figure 1.12, low voltage (120V), residential class

Distributed Renewable Energy Resource (DRER), Distributed Energy Storage Device (DESD), and loads are connected to the distribution bus (12kV) through a solid state transformer. The solid state transformer is used to enable active management of DRER, DESD and loads, rather than a 60Hz conventional transformer. The SST has the features of instantaneous voltage regulation, voltage sag compensation, fault isolation, power factor correction, harmonic isolation and DC output. The SST has a 400V DC port that will facilitate more efficient connection of certain classes of DRERs and DESDs. Acting very much like an energy router, each SST has bi-directional energy flow control capability allowing it to control active and reactive power flow and to manage the fault currents on both the low voltage and high voltage sides. Its large control bandwidth provides the plug-and-play feature for distributed resources to rapidly identify and respond to changes in the system.

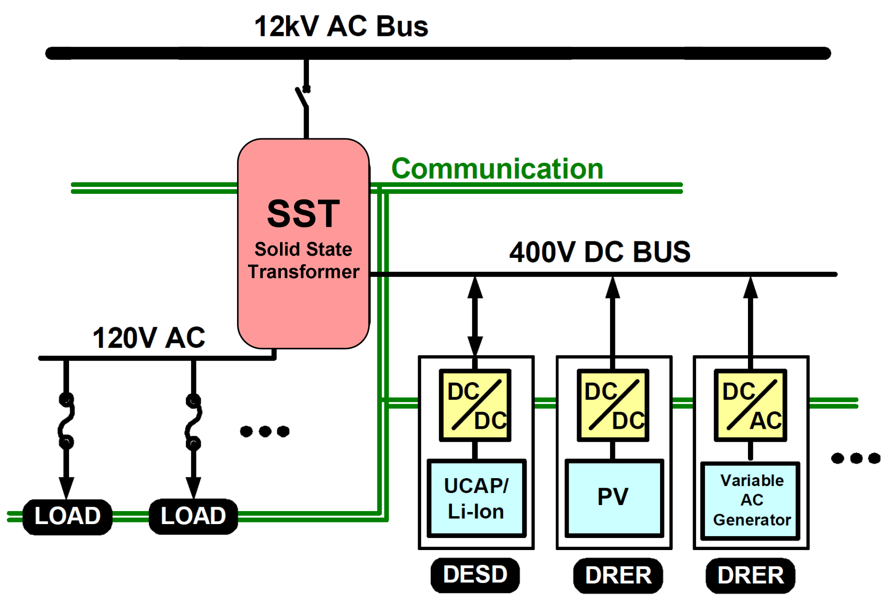


Figure 1.12 SST at one residential home (SST: Solid State Transformer, DRER: Distributed Renewable Energy Resource, DESD: Distributed Energy Storage Device)

With incorporation of the solid-state technology into the distribution transformer, many new features can be realized through power electronics control and dc bus energy storage [2][14].

1) Voltage sag compensation. When the input source voltage drops for a short period, the SST can compensate for the deficit and maintain constant output voltage. The total period of compensation, as a function of the amount of energy storage, can be adapted to the specific need of the customer.
2) Outage compensation. Similar to voltage sag compensation, the SST can provide full voltage compensation for the period needed by the built-in energy storage.
3) Instantaneous voltage regulation. If the input source voltage fluctuates due to power system transient or other load effects, the SST will maintain constant output voltage because it has the energy buffer.
4) Fault isolation. The SST can act as a circuit breaker to isolate the power grid from load fault and vice versa.
5) Power factor correction (and reactive power compensation). The SST can maintain a unity power factor within its power rating. The SST can also generate or absorb reactive power as required by the system.
6) Harmonic isolation. Nonlinear loads produce harmonic-distorted current that tends to propagate back to the primary side of the transformer. The SST will maintain a clean input current with a unity power factor.

7) DC output. In addition to the 120/240V AC voltage, the SST has 400V DC output, which allows easier connection to distributed energies.

8) Metering or advanced distribution automation. The SST has advanced monitoring capabilities including instantaneous voltage, current, power factor, harmonic percentage, kWh and fault current or voltage information as well.

9) Environmental benefit. Unlike the conventional liquid immersed transformer, the solid state transformer is an oil-free transformer and friendly to environment.

The comparisons of the reviewed solid state transformer topologies are summarized in Table 1.2.

Table 1.2 Comparisons of SST topologies

	Conventional transformer	**AC/AC converter design**	**ABB design**	**EPRI design**	**FREEDM SST**
Eliminating oil	×	√	√	√	√
Reducing weight and size	×	√	√	√	√
Reactive power compensation (Power factor correction)	×	×	√	√	√
Voltage sag compensation	×	√	√	√	√
Voltage regulation	**Limited, slow**	√	√	√	√
Outage compensation	×	×	√	√	√

Table 1.3 Continued

	Conventional transformer	AC/AC converter design	ABB design	EPRI design	FREEDM SST
Harmonic isolation	×	√	√	√	√
DC output	×	×	×	√	√
Energy storage option	×	×	√	√	√
Fault isolation (current limit)	×	√	√	√	√
Bidirectional power flow	√	√	×	×	√

× No such benefit; √ Has the benefit.

1.7. Contributions

The major contributions of this dissertation are as follow:

1) Proposed a cascaded multilevel H-Bridge converter based SST, including AC/DC rectifier, Dual Active Bridge (DAB) and DC/AC inverter for interfacing with the single phase 7.2kV distribution system.
2) Designed and developed the SST modeling and control. The SST features are verified by the average model and switching model.
3) Proposed a new voltage balance controller to balance the cascaded H-Bridge capacitor voltages. Derived the general constraints of the unbalance power for the

cascaded H-Bridge topology. The proposed method and analysis are verified by simulations and experiments.

4) Proposed a new power balance control method to balance the parallel DAB power in the SST. The proposed method is verified by simulations.
5) Proposed a new feed-forward power ripple control to minimize the DC bus voltage ripple and the capacitor size in the SST. The proposed method together with the power synchronization method is verified by simulations.
6) Designed and implemented a SST rectifier hardware prototype. The SST features and controller are verified by the experiment.
7) Designed a high power rating (270kVA) and high voltage (13.6kV) substation solid state transformer based on the 10 kV SiC MOSFET and PIN diodes. Proposed a novel ZVS operation for five-level DC/DC converter to reduce the device switching loss.

1.8. Outline

Chapter 1 introduces the development of distribution transformers, the motivation of the solid state transformer. The state-of-the-art topologies and solutions of SST are reviewed and compared. Then the proposed cascaded H-Bridge converter based solid state transformer is presented and the research background FREEDM system is introduced.

In Chapter 2, the modeling of the SST, including the rectifier, dual active bridge and inverter stage are developed. Based on the small signal model and bode plot, the dq axis vector controller is designed. The SST average model is developed to enable the dynamic system level simulation. Then the average and switching model simulation including unbalanced load, voltage sag, regenerative mode and short circuit fault are presented to verify the proposed controller.

In Chapter 3, a novel voltage control strategy is proposed to balance the rectifier capacitor voltages. Due to the intrinsic constraints of the cascaded H-Bridge circuit, the unbalance power range of each H-Bridge is limited. The power unbalance constraints of the cascaded H-Bridge rectifier are derived. Furthermore, a power balance control is proposed to balance the real power through the DAB parallel modules. The SST switching model simulation demonstrates the proposed voltage and power balance controller. The 20kW SST scaled down prototype experiment is implemented and verifies the effectiveness of the proposed voltage controller.

Chapter 4 proposes a feed-forward ripple power control method for the DAB stage and designs a power synchronization method for the inverter stage. The proposed methods are based on the power synchronization of input and output, including the rectifier, DAB and the inverter stage. The simulation results verify the proposed controller and the required capacitance can be reduced effectively.

In Chapter 5, a hardware prototype of the cascaded H-Bridge rectifier in the solid state transformer is implemented. The detailed hardware design and the model based controller are presented in details. The steady state performance, reactive power control, load unbalance and dynamic load change, power unbalance limit, input voltage sag and swell, the rectifier operation state machine, voltage loop notch filter are all verified by the experiments. The experiments illustrate the performance of the designed controller.

In Chapter 6, a 270 kVA substation solid state transformer using 10kV SiC Power MOSFET and JBS diodes has been proposed. A novel ZVS five-level DC-DC converter and its ZVS soft-switching operation are proposed. The proposed ZVS method significantly reduces the turn-on loss of the MOSFETs and improves the overall efficiency. The closed loop controller of the substation solid state transformer system is designed. The simulation results verify the functionality and feasibility of the rectifier and DC/DC converter stage. Furthermore, based on the device characteristics from physics simulation, the devices losses are calculated to verify the system feasibility.

Chapter 2. Design, Modeling and Control of a Cascaded H-Bridge Converter based Solid State Transformer

2.1. SST System Design

This section details the design of the SST system and components. The solid-state transformer consists of an AC/DC rectifier, a DC/DC converter with a high frequency transformer and a DC/AC inverter. The traditional 60 Hz transformer is replaced by a high frequency transformer plus solid state devices, which is the key to achieve size and weight reduction.

The basic configuration of a proposed 20kVA SST interfaced to 12kV distribution voltage with center-tapped 120V single-phase output is shown in Figure 2.1. The SST is rated as single phase input voltage 60 Hz, 7.2kV, output voltage 60 Hz, 240/120V, 1 phase/3 wires. The SST consists of a high voltage high frequency AC/DC rectifier that converts 60Hz, 7.2kV AC to three cascaded 3.8 kV DC bus, three high voltage high frequency DC-DC converters that convert 3.8 kV to 400V DC bus and a voltage source inverter (VSI) that inverts 400V DC to 60 Hz, 240/120V, 1 phase/3 wires. In order to use 6.5kV IGBT devices to interact with 7.2kV AC voltage, the rectifier stage is designed with three H-bridges cascaded to have a 7-level voltage waveform and reduce the voltage stress. The DAB stage uses a high frequency transformer with 3.8kV/400V turns ratio to step down the voltage. The regulated 400V DC voltage is a unique output of the SST, which allows easier connections of some renewable energies and energy storages. The output of the DC/AC inverter will connect to the residential houses and provide 120/240V AC voltages.

The switching devices in high voltage H-bridge and low voltage H-bridges shown are 6.5kV IGBT and 600V IGBT respectively. The switching frequency of the HV-IGBT devices is 1 kHz, because the device current is very low which results in low switching losses [32]. The 20 kVA SST unit is envisioned as a building block of IEM (shown in Figure 1.11) and also for construction of a larger rated three-phase 100kVA SST. Figure 2.2 shows a preliminary hardware implementation of the proposed 20kVA SST [33].

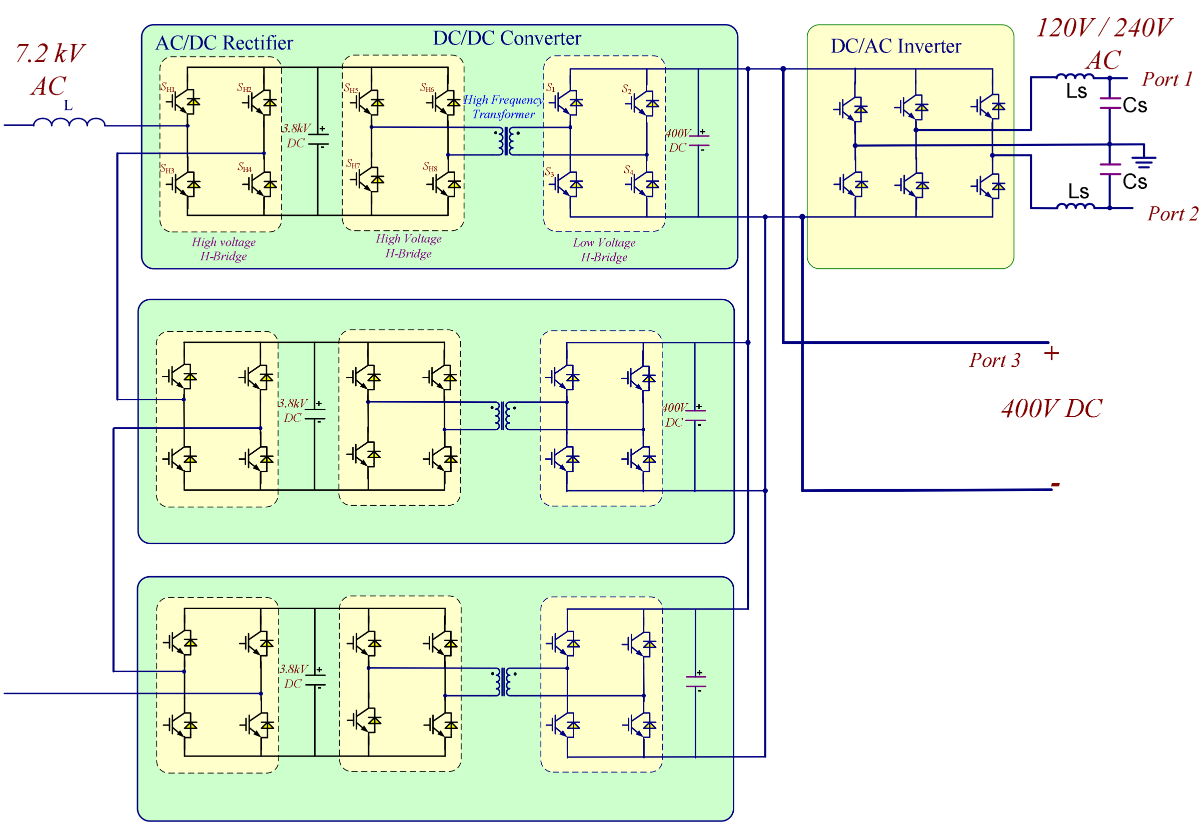


Figure 2.1 Topology of Solid State Transformer

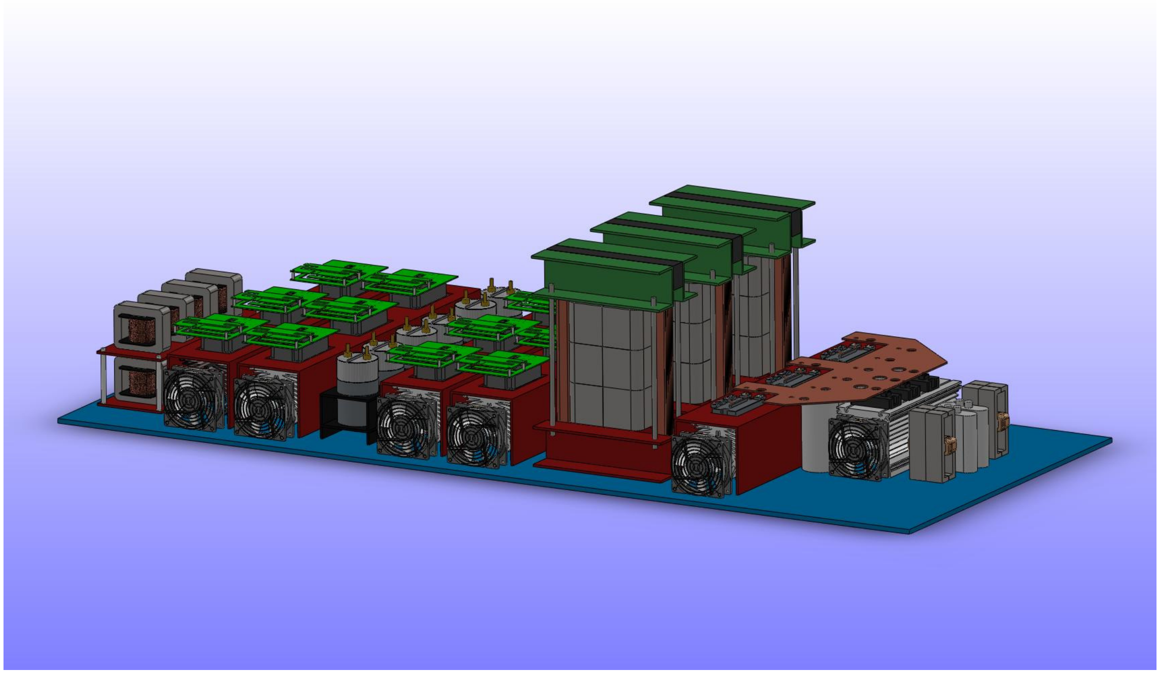


Figure 2.2 3D drawing of 20kW Solid State Transformer

2.1.1. *DC bus voltage*

The rectifier DC bus voltage is required to be higher than the input AC peak voltage to guarantee the DC bus regulation and the input current control. With modulation index M limited to 0.9, the dc bus voltage should be:

$$V_{dc} = \sqrt{2}V_{ac} / M \tag{2.1}$$

Where $V_{ac} = 7.2kV, M = 0.9$, then $V_{dc}=11.4kV$ with each H-Bridge DC bus voltage 3.8kV.

A higher DC bus voltage allows a voltage margin for better input current waveform shaping and more reactive power flow control margin. However, in order to have enough voltage margins for 6.5kV device, the DC bus voltage cannot be designed higher.

2.1.2. *DC link capacitance*

The size of the DC bus capacitor depends on the magnitude of ripple voltage and capacitor current. Generally, the capacitor charge, energy storage and system stability need to be considered to select the DC link capacitors.

When the filter current is positive, the capacitor is charged. When the filter current is negative, the capacitor is discharged. The charging frequency is twice the line frequency. Assume that the charging time is the same as discharging time and a 10% voltage ripple is allowed for the DC bus.

$$I_{a-rms}\Delta t = C_d \Delta V_{dc} \tag{2.2}$$

$\Delta t = \frac{1}{2} * \frac{1}{120} s, \Delta V_{dc} = 10\% V_{dc} = 380V, I_a = 2.8A$

So, V_{dc}=3.8kV for each H-Bridge.

Unlike the three phase converter system, the DC bus voltage in single phase H-bridge always contains 120Hz low frequency ripple, because the single phase power itself is a 120Hz variable according to the equation $P = V\sin(\omega t) * I\sin(\omega t)$. This requires a much larger capacitance to limit the DC voltage ripples within the allowable range compared to the three phase system. A power ripple control method is proposed in Chapter 4 to minimize the required capacitance in the SST.

From the energy point of view, only extreme cases are considered for simplicity. Assume in one switching cycle the rectifier input power is zero while the inverter output power reaches maximum and vice versus. The relationship between the capacitance and the voltage dip is given by equation (2.3) [34].

$$C = \frac{P_{\max}}{\left(V_{dc}\Delta U \pm \frac{1}{2}\Delta U^2\right) f_{sw}} \tag{2.3}$$

$P_{\max} = 20*2/3kW, \Delta V_{dc} = 10\% V_{dc} = 380V, f_{sw} = 1kHz$

Where P_{max} is instantaneous maximum power.

System stability also needs to be considered to determine the capacitance. The rectifier and the inverter are two cascaded subsystems. In order to avoid interaction between the two systems the output impedance of the rectifier should be lower than the input impedance of the inverter [35]. Then the constraint for DC link capacitance is given by

$$20\lg\left(\frac{V_{dc}^{\ 2}}{P_{out}}\right) - 20\lg\left(\frac{1}{2\pi f_{BW} C}\right) \geq Z_m \tag{2.4}$$

Based on the above criteria, the designed capacitance for the high voltage DC bus is C_d=30uF.

2.1.3. *Input AC Inductor*

The input AC inductor is a key component to interface with the high voltage AC. The input AC inductor selection is determined based on the maximum power transfer, AC current harmonics, current ripple and inrush current.

In order to guarantee the rated power can be transferred through the rectifier, the inductance is required to meet the vector equation (2.5).

$$MV_{dc} > \sqrt{Vp^2 + (\omega L I_p)^2} \tag{2.5}$$

Where M is the modulation index (maximum value 1), V_p is the peak AC voltage, I_p is the peak AC current, ω is the angular speed and L is the inductance.

Another consideration is the input current harmonic requirement. The input current THD can be obtained with spectrum analysis results under a given switching frequency. The input current THD is given by equation (2.6).

$$THD = \frac{\sqrt{\sum \left(\frac{u_i}{\omega_i L} \right)^2}}{I_1} \tag{2.6}$$

where u_i is the amplitude of the harmonic voltage with order i, ω_i is the harmonic frequency, L is the harmonic inductor and I_1 is the fundamental current.

The current ripple also needs to be considered when determining the input inductance. The input current ripple should be suppressed to a reasonable level to guarantee control feasibility and the proper operation of the switching device. The current ripple will vary as the main input voltage varies over a fundamental cycle. Here we discuss only the point when the fundamental phase current reaches the peak value as it is useful to determine the maximum current for inductor design.

Assume the inductor current change could be ignored in one switching cycle (volt-second equals zero). The peak current ripple is shown in equation (2.7).

$$\frac{di_a}{dt} = \left| \frac{v_{in} - V_{dc}}{L_f} \right| \tag{2.7}$$

$$L_f = D_m \frac{|V_m - V_{dc}|}{2 f_{sw} \Delta i_a} \tag{2.8}$$

So the inductance can be calculate as L=0.23H.

During the inrush period, the rectifier works like a diode bridge, the peak current should be constrained due to the limit of the semiconductor device. The relationship between the peak inrush current I_{peak} and the passive parameters is given by

$$\frac{1}{2} L i_{peak}{}^2 = \frac{1}{2} C (V_{line} - V_{initial})^2 \tag{2.9}$$

2.2. SST Modeling and Control

As shown in Figure 2.3, the model development process begins with the SST switching model. By averaging the switching state, the SST average mode is obtained. The average model is linearized at a steady state point and the small signal model is derived. Based on the linear small signal mode, the key open-loop transfer functions of the control parameters to state variables such as SST currents and DC capacitor voltages can be obtained. The feedback control is designed and evaluated based on the derived transfer functions [36][37][38][39]. The loop gains are then modified to achieve as much stability as possible, while the dynamic response is not sacrificed. The proposed control technique is validated by both computer simulation and experiments.

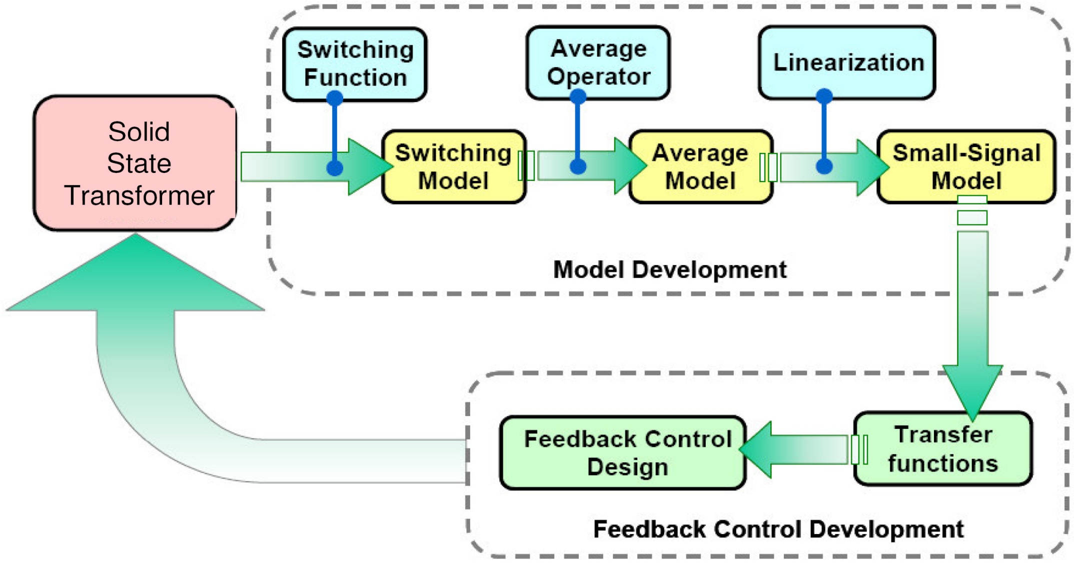


Figure 2.3 Controller development for solid state transformer

2.2.1. *Modeling and control of rectifier stage*

2.2.1.1. **Rectifier switching and average model**

The rectifier converts the single phase 7.8kV AC voltage to three DC output while maintaining unity power factor at the input side. The rectifier consists of three cascaded H-bridges with each reference DC bus 3.8kV. The basic topology of an H-bridge converter is shown in Figure 2.4. The top and bottom switch in each pole must be switched on and off complimentary. Therefore, the top switch can therefore be used to represent the switching status of its phase leg. Three possible output-voltage levels of the H-bridge converter and their corresponding switch combinations are illustrated in Table 2.1. “0” represents that the switch is on and “1” represents that the switch is off.

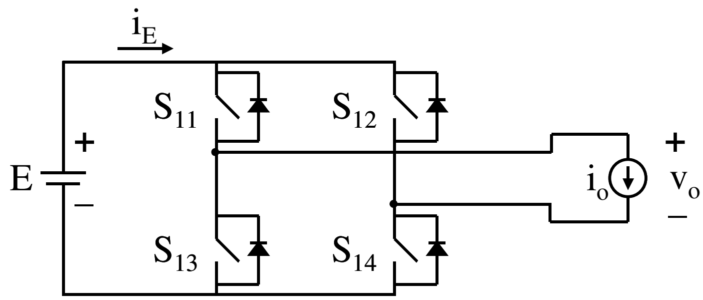


Figure 2.4 Basic structure of a H-Bridge converter

Table 2.1 H-bridge Converter Switching Combinations

S_{11}	S_{12}	v_o	i_E
0	0	0	0
1	0	E	i_o
0	1	-E	$-i_o$
1	1	0	0

The relationship between the DC bus voltage and the output voltage, the capacitor current and the output current are derived in equations (2.10) and (2.11).

$$v_o = (S_{11} - S_{12})E \tag{2.10}$$

$$i_E = (S_{11} - S_{12})i_o \tag{2.11}$$

Redefine $S_1 = S_{11} - S_{12}$, thus, $v_o = S_1 \cdot E$ and $i_E = S_1 \cdot i_o$

The switching model of the H-bridge converter can be represented as shown in Figure 2.5. In the same way, the cascaded H-Bridge rectifier can be represented by the switching model in Figure 2.6.

$$v_i = S_i \cdot E_i \tag{2.12}$$

$i_{Ei} = S_i \cdot i_o$, for $i = 0 \ldots N$.

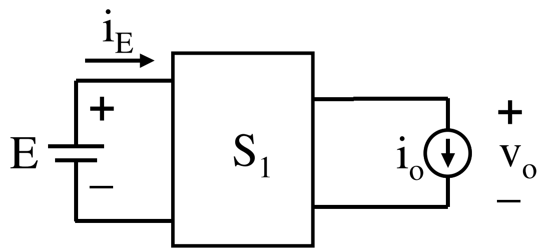


Figure 2.5 Switching model of H-Bridge converter

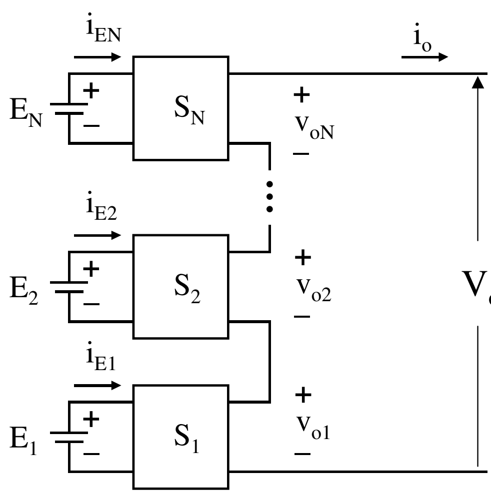


Figure 2.6 Switching model of a *2N+1* level cascaded converter

For a complex power electronic system simulation as SST, the switching model requires very short time steps and results in a long simulation time. Therefore, the average model of SST is indispensable for the dynamic system level simulation, because it allows much faster simulation and reduces memory requirement when compared to the detailed switching models.

Furthermore, the large signal average model is the basis of developing the small signal model and designing the controller parameters.

Applying an average operator to the switching model

$$\overline{X}(t) = \frac{1}{T}\int_{t-T}^{t} x(\tau)d\tau \tag{2.13}$$

The switching duty cycle:

$$d_i = \overline{S}_i(t) = \frac{1}{T}\int_{t-T}^{t} S_i(\tau)d\tau \tag{2.14}$$

Average of quadratic terms:

$$v_i = S_i \cdot E_i \tag{2.15}$$

$$\overline{V}_i = \frac{1}{T}\int_{t-T}^{t} (S_i(\tau)\cdot E_i(\tau))d\tau \tag{2.16}$$

In one switching cycle, $E_i(\tau)$ is assumed to be constant.Thus,

$$\overline{V}_i = \frac{1}{T}\int_{t-T}^{t} S_i(\tau)d\tau \cdot E_i = d_i E_i \tag{2.17}$$

Therefore,

$$\overline{v}_{ai} = d_{ai} \cdot E_{ai} \tag{2.18}$$

$$\overline{i}_{Eai} = d_{ai} \cdot i_a \tag{2.19}$$

$$\overline{v}_{an} = \sum_{i=0}^{N}\left(d_{ai} \cdot E_{ai}\right) \tag{2.20}$$

To simplify the average model, the following assumptions are made. All DC voltage sources are equal, i.e. $E_{ai} = E_{bi} = E_{ci}$, for $i = 0...N$. All duty circle of each are equal, i.e. $d_{ai} = d_a$, $d_{bi} = d_b$, $d_{ci} = d_c$, $i = 0\ldots N$.

Based on the rectifier circuit analysis [40], the average differential equations of the rectifier are:

$$\frac{di_a}{dt} = \frac{3E}{L_s} d_a - \frac{V_{pcca}}{L_s} - \frac{R_s}{L_s} i_a \tag{2.21}$$

$$\frac{dE}{dt} = -\frac{E}{R_L C} - \frac{d_a i_a}{C} \tag{2.22}$$

Where, i_a is the input current, V_{pcca} is the average input voltage, R_s is the input line resistance, R_L is the equivalent output impedance of the rectifier stage, L_s is the input inductor, E is the DC bus voltage, C is the DC capacitor, d_a is the rectifier PWM duty cycle. Based on the circuit equations, the average model equivalent circuit is derived in Figure 2.7.

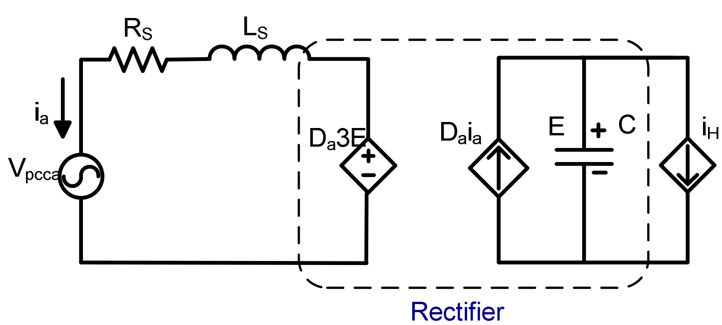


Figure 2.7 Rectifier average model

The single phase d-q vector control is used in the rectifier control. First an imaginary phase M which is 90 degree lagging the original phase A is hypothesized.

$$\frac{di_m}{dt} = \frac{3E}{L_s} d_m - \frac{V_{pccm}}{L_s} - \frac{R_s}{L_s} i_m \tag{2.23}$$

$$\frac{dE_m}{dt} = -\frac{E_m}{R_L C} - \frac{d_m i_m}{C} \tag{2.24}$$

Neglect the 120Hz voltage ripple on DC capacitor, then E_m=E (small ripple approximation). Rewrite above equations:

$$\frac{d\vec{i}_{am}}{dt} = \frac{3E}{L_s} \vec{d}_{am} - \frac{\vec{V}_{pccam}}{L_s} - \frac{R_s}{L_s} \vec{i}_{am} \tag{2.25}$$

$$\frac{dE}{dt} = -\frac{E}{R_L C} - \frac{\vec{d}_{am}{}^T \vec{i}_{am}}{2C} \tag{2.26}$$

Where, $\vec{i}_{am} = \begin{bmatrix} i_a \\ i_m \end{bmatrix}$, $\vec{d}_{am} = \begin{bmatrix} d_a \\ d_m \end{bmatrix}$, $\vec{V}_{pccam} = \begin{bmatrix} V_{pcca} \\ V_{pccm} \end{bmatrix}$.

Then the single phase d-q transformation is applied to the differential equations (2.25) and (2.26), then the differential equations in d-q coordinates are derived.

The single phase d-q transformation [41]:

$$[x]_{dq} = [T] \cdot [x]_{am} \tag{2.27}$$

Where, $T = \begin{bmatrix} \sin(\theta) & -\cos(\theta) \\ \cos(\theta) & \sin(\theta) \end{bmatrix}$, $\theta = 2\pi ft$, f is line frequency.

Multiply the d-q axis equations on both sides by single phase d-q transformation matrix, then equations of the single phase H-bridge rectifier are then derived as equation (2.28) and (2.29). The average model of cascaded H-Bridge converter in d-a axis is shown in Figure 2.8.

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \frac{3E}{L_s}\begin{bmatrix} d_d \\ d_q \end{bmatrix} - \frac{1}{L_s}\begin{bmatrix} v_{pccd} \\ v_{pccq} \end{bmatrix} - \begin{bmatrix} \frac{R_s}{L_s} & -\omega \\ \omega & \frac{R_s}{L_s} \end{bmatrix}\begin{bmatrix} i_d \\ i_q \end{bmatrix} \tag{2.28}$$

$$\frac{dE}{dt} = -\frac{E}{R_L C} - \frac{1}{2C}\begin{bmatrix} d_d \\ d_q \end{bmatrix}^T \begin{bmatrix} i_d \\ i_q \end{bmatrix} \tag{2.29}$$

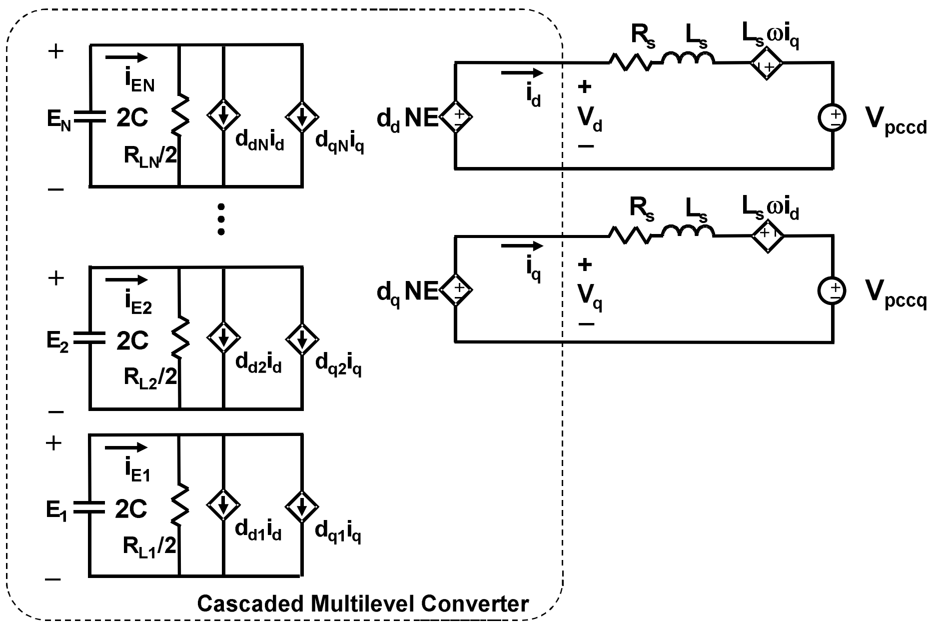


Figure 2.8 Average model of cascaded H-Bridge converter

The small signal model can be derived by liberalizing the equation at a steady state point. The small signal model of cascaded H-Bridge converter in d-q axis is shown in Figure 2.9.

$$\frac{d}{dt}\begin{bmatrix}\tilde{i}_d \\ \tilde{i}_q\end{bmatrix} = \frac{3E}{L_s}\begin{bmatrix}\tilde{d}_d \\ \tilde{d}_q\end{bmatrix} + \frac{3\tilde{E}}{L_s}\begin{bmatrix}D_d \\ D_q\end{bmatrix} - \frac{1}{L_s}\begin{bmatrix}\tilde{v}_{pccd} \\ \tilde{v}_{pccq}\end{bmatrix} - \begin{bmatrix}\frac{R_s}{L_s} & -\omega \\ \omega & \frac{R_s}{L_s}\end{bmatrix}\begin{bmatrix}\tilde{i}_d \\ \tilde{i}_q\end{bmatrix} \tag{2.30}$$

$$\frac{d\tilde{E}}{dt} = -\frac{\tilde{E}}{R_L C} - \frac{1}{2C}\begin{bmatrix}D_d \\ D_q\end{bmatrix}^T \begin{bmatrix}\tilde{i}_d \\ \tilde{i}_q\end{bmatrix} - \frac{1}{2C}\begin{bmatrix}I_d \\ I_q\end{bmatrix}^T \begin{bmatrix}\tilde{d}_d \\ \tilde{d}_q\end{bmatrix} \tag{2.31}$$

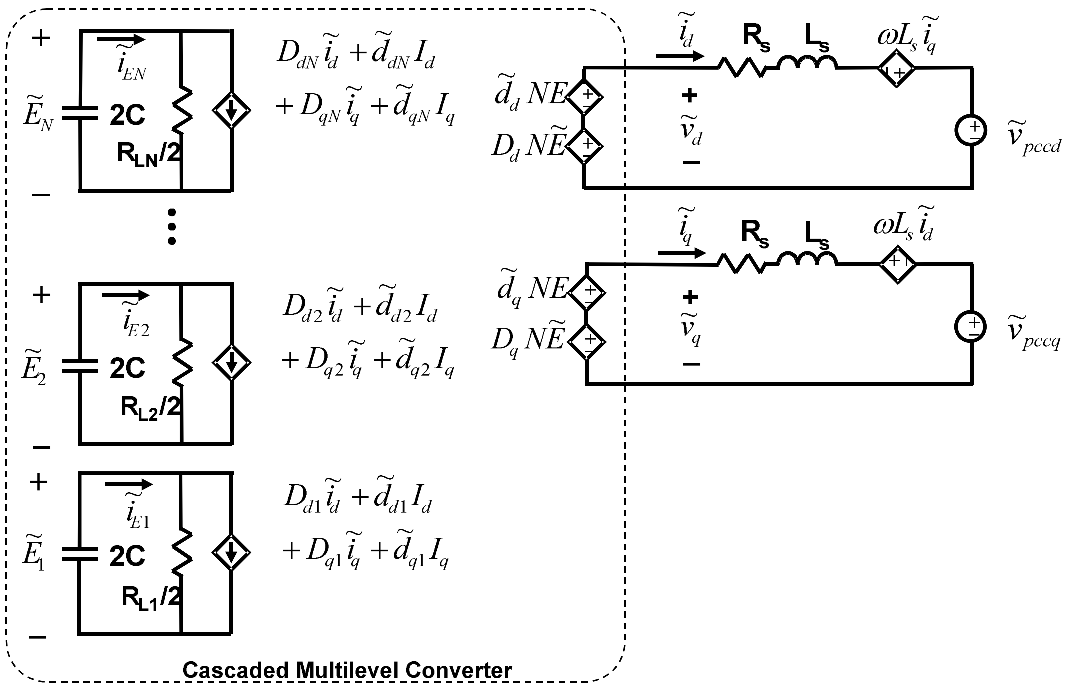


Figure 2.9 Small signal model of cascaded H-Bridge converter in d-q axis

The state space functions are given by equation (2.32).

$$\frac{d}{dt}\begin{bmatrix}\tilde{i}_d\\ \tilde{i}_q\\ \tilde{E}\end{bmatrix}=\begin{bmatrix}-\frac{R_s}{L_s} & \omega & \frac{3D_d}{L_s}\\ -\omega & -\frac{R_s}{L_s} & \frac{3D_q}{L_s}\\ -\frac{D_d}{2C} & -\frac{D_q}{2C} & -\frac{1}{R_L C}\end{bmatrix}\begin{bmatrix}\tilde{i}_d\\ \tilde{i}_q\\ \tilde{E}\end{bmatrix}+\begin{bmatrix}\frac{3E}{L_s} & 0\\ 0 & \frac{3E}{L_s}\\ -\frac{I_d}{2C} & -\frac{I_q}{2C}\end{bmatrix}\begin{bmatrix}\tilde{d}_d\\ \tilde{d}_q\end{bmatrix}+\begin{bmatrix}-\frac{1}{L_s} & 0\\ 0 & -\frac{1}{L_s}\\ 0 & 0\end{bmatrix}\begin{bmatrix}\tilde{v}_{pccd}\\ \tilde{v}_{pccq}\end{bmatrix} \quad (2.32)$$

2.2.1.2. **Rectifier d-q vector control**

With the chosen PLL, the voltage vector is aligned with the direction of the d-axis during steady state. The grid voltage component in the d-direction is equal to its peak value and the q-component of the grid voltage is equal to zero. Thus, the d-component of the current vector (parallel to the grid voltage vector in steady state) becomes the active current component and the q-component of the current vector becomes the reactive current component [29][38][42]. The decoupled d-q vector controller for each H-bridge is shown in Figure 2.10. The three SPWM carriers for the cascaded H-bridge are phase shifted so that the rectifier has seven voltage levels to reduce voltage stress and harmonics [43].

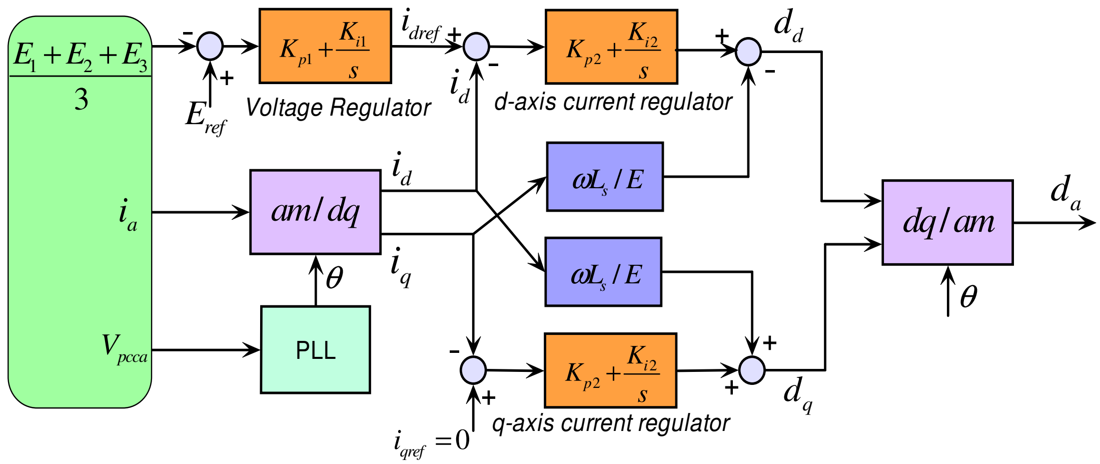


Figure 2.10 d-q decoupled controller of rectifier

With the decoupled d-q control, the equation of V_d and V_q are as follows.

$$V_d = (i_{dref} - i_d)(K_{p1} + \frac{K_{i1}}{s}) - \omega L i_q + V_{pccd} \tag{2.33}$$

$$V_q = (i_{qref} - i_q)(K_{p1} + \frac{K_{i1}}{s}) + \omega L i_d + V_{pccd} \tag{2.34}$$

Substitute the V_d and V_q in the state space function with above equations.

$$p\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} -\frac{(K_{p1}+\frac{K_{i1}}{s}+R_s)}{L_s} & 0 \\ 0 & -\frac{(K_{p1}+\frac{K_{i1}}{s}+R_s)}{L_s} \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} + \frac{(K_{p1}+\frac{K_{i1}}{s})}{L_s} \begin{bmatrix} i_{dref} \\ i_{qref} \end{bmatrix} \tag{2.35}$$

With the decoupled d-q vector control, the d and q loops are decoupled and the d-q current loops are symmetric. Therefore the d-axis loop is considered here and the control block is shown in Figure 2.11.

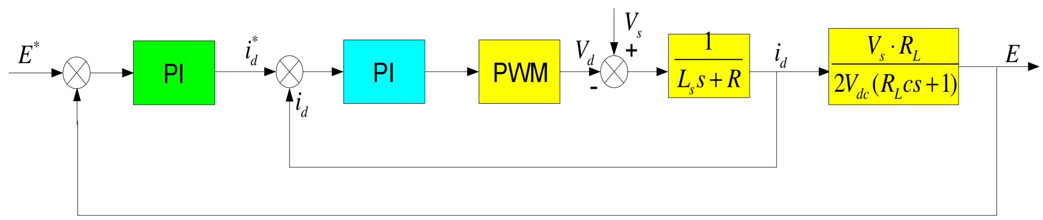
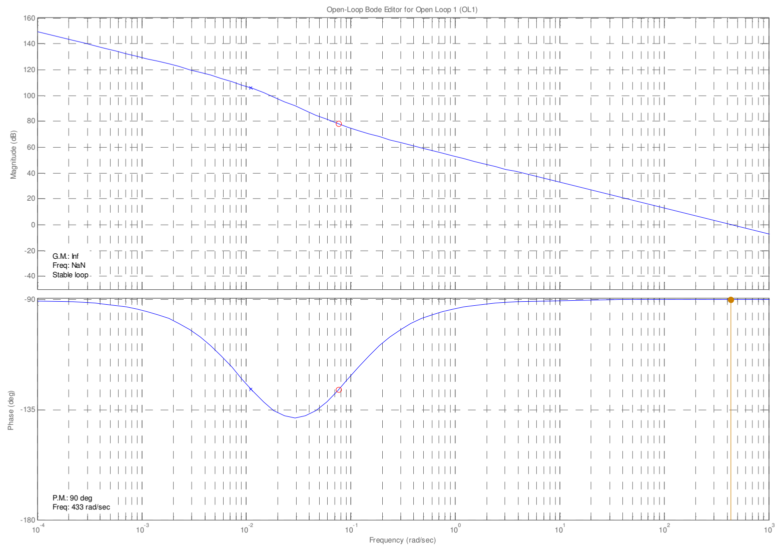


Figure 2.11 Control block of d-axis loop

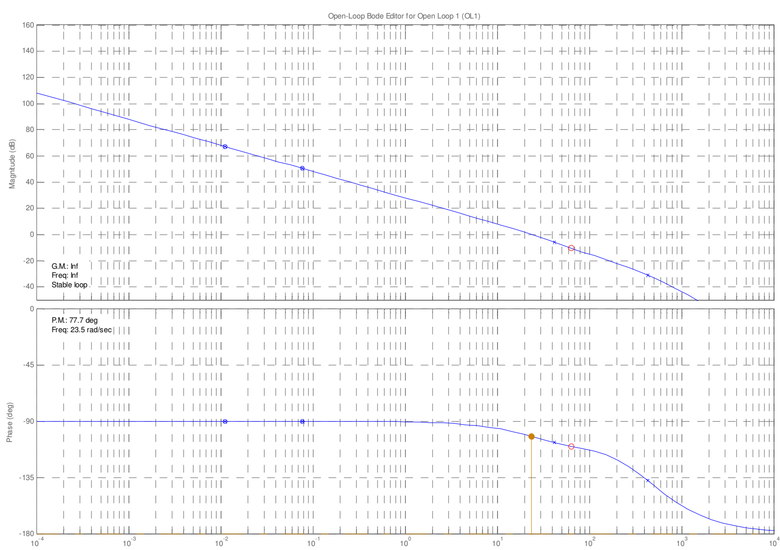
The two PI regulators in d-axis loop are designed based on the bode plot. As shown in Figure 2.12, the cutoff frequency of the d-axis current loop and the voltage loop are 70Hz and 4Hz respectively. The SST with the proposed controller is simulated to verify the controller design.

2.2.2. *Modeling and control of Dual Active Bridge (DAB)*

As shown in Figure 2.13, the dual active bridge consists of a high voltage H-Bridge, a high frequency transformer and a low voltage H-bridge. The rectifier controls the high voltage DC link voltage and the input current to be sinusoidal from the AC input. The low voltage DC link is regulated by the DAB converter. The typical transformer voltage and current waveforms are illustrated in Figure 2.14. The dual active bridge topology offers zero voltage switching for all the switches, relatively low voltage stress for the switches, low passive component ratings and complete symmetry of configuration that allows seamless control for bidirectional power flow [44].



(a)



(b)

Figure 2.12 Bode plot of d-axis current (a) and voltage loop (b) of rectifier

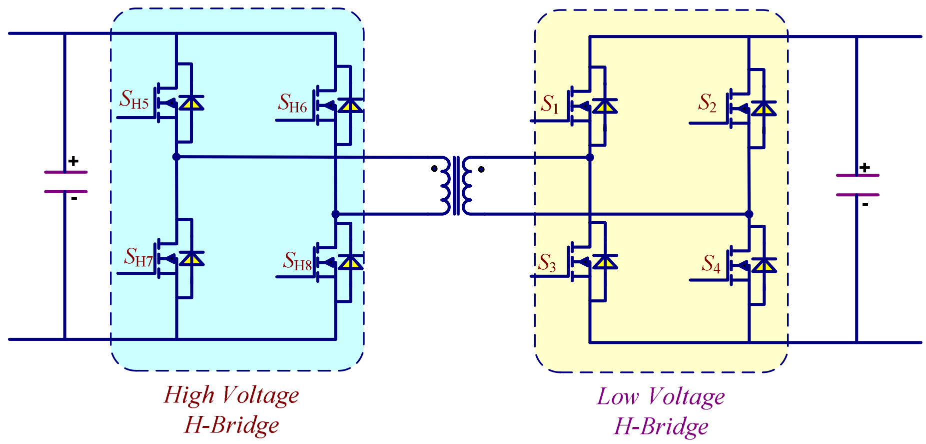


Figure 2.13 Dual active bridge circuit

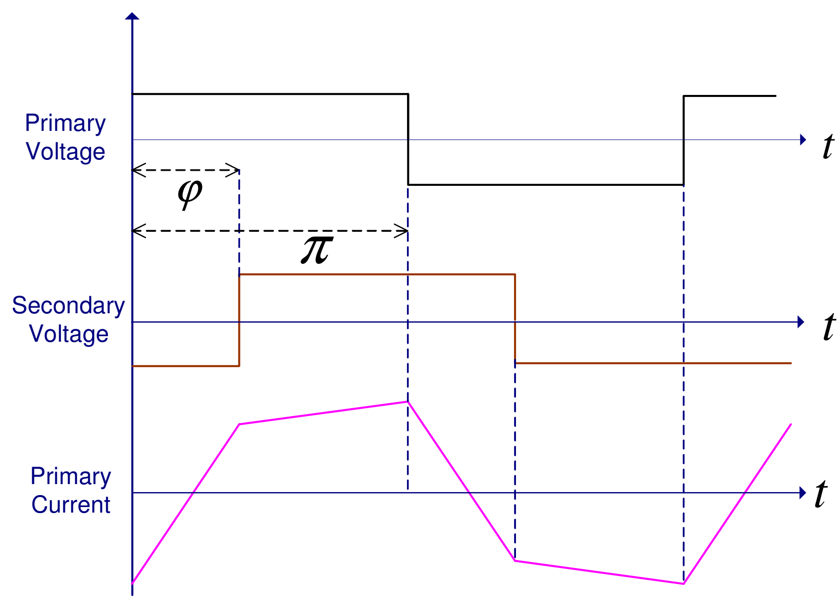


Figure 2.14 DAB voltage and current waveforms

The real power flows from the bridge with leading phase angle to the bridge with lagging phase angle, the amount of power transferred being controlled by the phase angle difference and the magnitudes of the dc voltages at the two ends as given by [45].

$$P_o = \frac{V_{dc} V_{dc\_link}}{2Lf} d_{dc}\left(1 - d_{dc}\right) \tag{2.36}$$

Where, V_{dc} is input dc voltage, f is switching frequency, L is leakage inductance, V_{dc_link} is dc link voltage referred to input side and d_{dc} is ratio of time delay between the two bridges to one-half of switching period.

From the power flow equation, and using graphical techniques on the inductor waveform over half a switching period it can be shown that the average dc link current over half a cycle is given by the equation. The average model of the DAB stage is developed as in Figure 2.15.

$$I_d\left(avg\right) = \frac{V_{dc} T_s}{2L} d_{dc}\left(1 - d_{dc}\right)$$

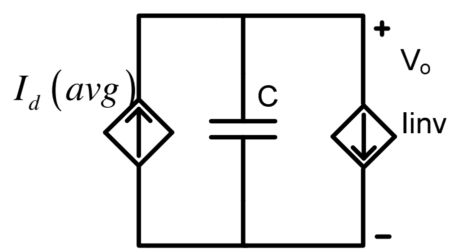


Figure 2.15 DAB average model

For the DAB converter, the phase shift control is used to regulate the low voltage DC voltage to the reference 400V under different load conditions. The DAB controller is shown in Figure 2.16. First the difference between the low voltage DC voltage V_{dc} and the reference voltage is compared. Then the phase shift angle is adjusted by the PI controller to regulate V_{dc} according to this voltage error.

The transfer function is derived and the PI regulator is designed based on the bode plot. With $G(s) = 0.34*(1+0.034s)/s$, the cutoff frequency of the control loop is 143Hz as shown in Figure 2.17.

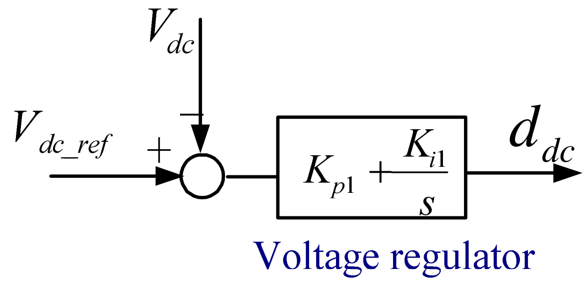


Figure 2.16 Phase shift controller of DAB

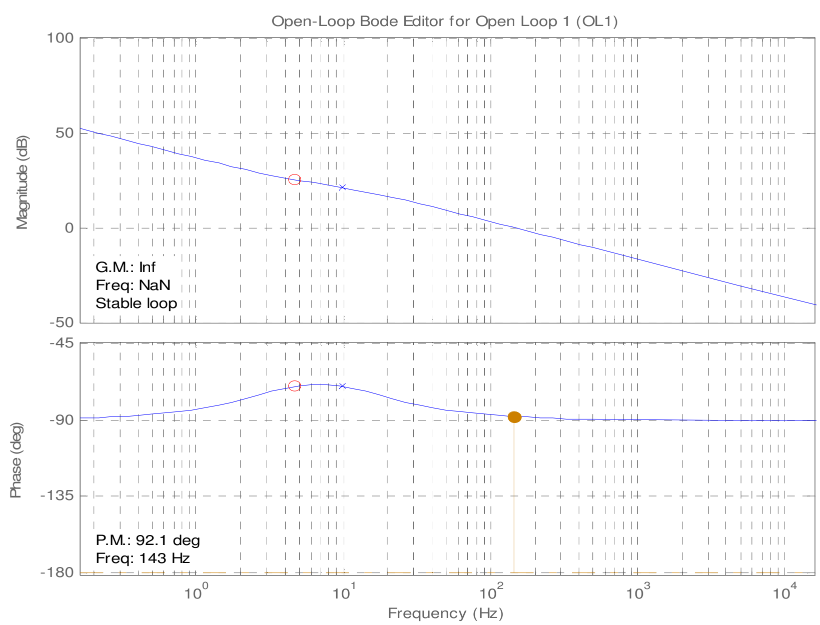


Figure 2.17 Bode plot of DAB control loop

2.2.3. *Modeling of Inverter stage*

The DC/AC inverter converts the 400V DC to 240/120V AC, 1 phase/3 wires. The topology is shown in Figure 2.18 and the average model of DC/AC inverter is shown in Figure 2.19. The inverter consists of six switches with three phase legs. The neutral point is connected to the third phase leg and the other two phase legs in the four-switch inverter are controlled by Sinusoidal Pulse Width Modulation (SPWM). The two sinusoidal control references have a 180 phase difference and the same amplitude. The third phase leg in the six-switch inverter usually is controlled to produce a square waveform to serve as the neutral phase and at same time achieve the maximum utilization of the DC bus voltage [46][47][48].

In the inverter stage, the DC link voltage is regulated by the DAB converter while the PWM AC inverter controls the magnitude of the output side AC voltage. The inverter controller has an inner current loop and an outer voltage loop. The controller diagram is shown in Figure 2.20, and both voltage and current regulators are PI regulators. The D_{inv1} and D_{inv2} are the duty cycles of two output port voltages in the average model.

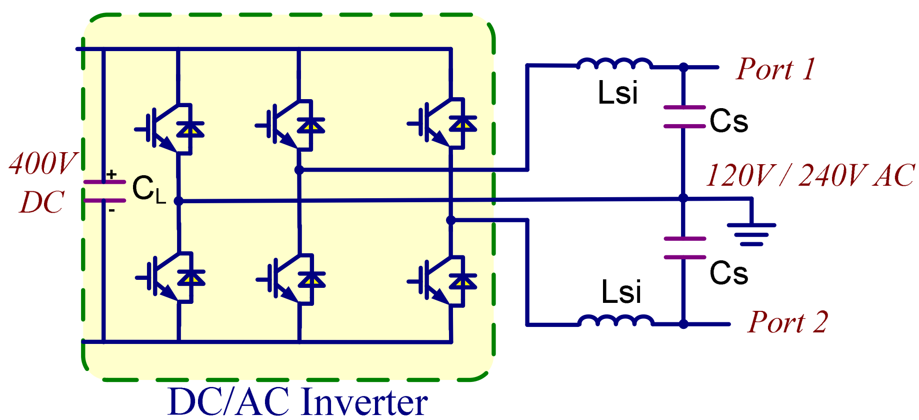


Figure 2.18 Topology of DC/AC inverter

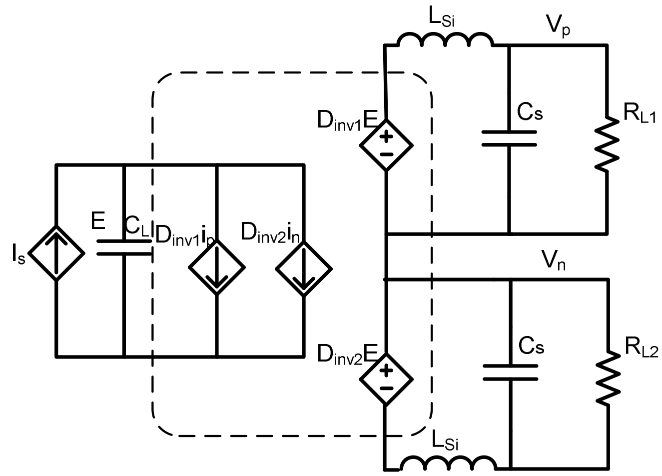


Figure 2.19 Average model of DC/AC inverter

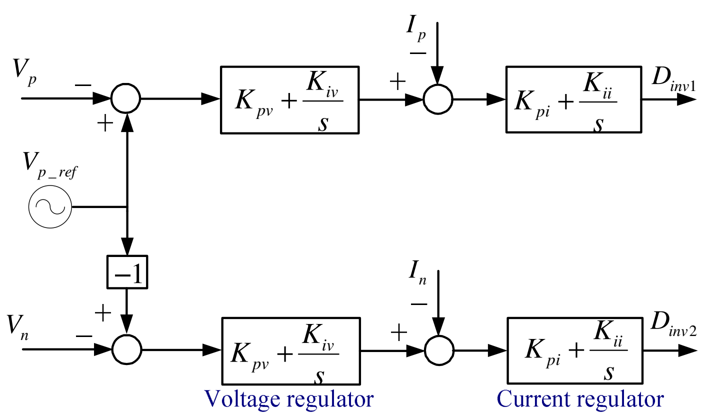


Figure 2.20 Controller for DC/AC inverter

2.3. Average Model Verification and Limitation

The developed SST average model is verified by comparing the simulation results with the detailed switching model. In the SST switching model, the IGBT devices are represented by the switch model in Matlab/Simulink. The control scheme and the controller parameters are identical with the average model. The modulation scheme used for the switching model is

SPWM. The triangle carriers for the cascaded H-bridge are phase shifted so that the rectifier has seven voltage levels to reduce the voltage stress and harmonics.

The simulations are implemented with the same circuit and control parameters. The comparisons of the average model with the switching model are shown in Figure 2.21 and Figure 2.22, the voltages and currents on the AC side of the seven-level rectifier are well matched.

Figure 2.23 and Figure 2.24 illustrate the average model and switching model simulation under voltage sag condition. The dynamic response of the two models also match with each other. This validates the developed average model to be used for dynamic system level simulation study of the FREEDM system.

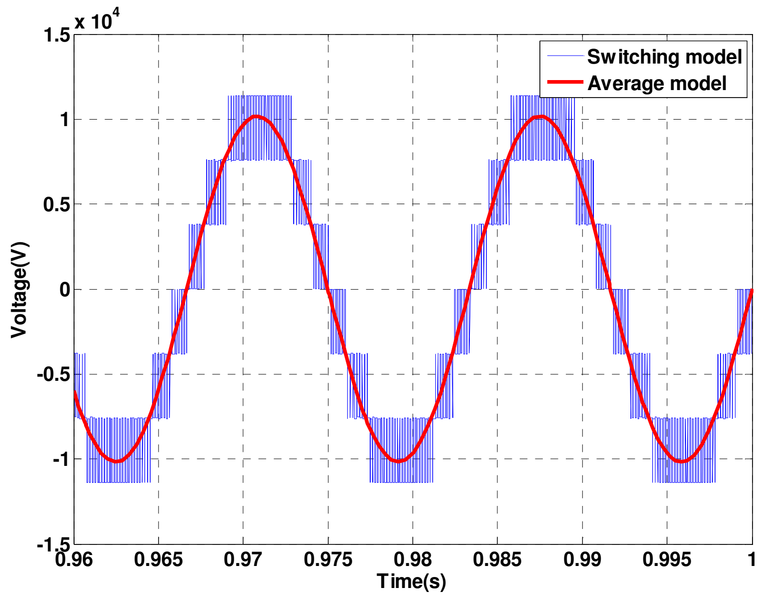


Figure 2.21 Input AC voltage of switching model and average model

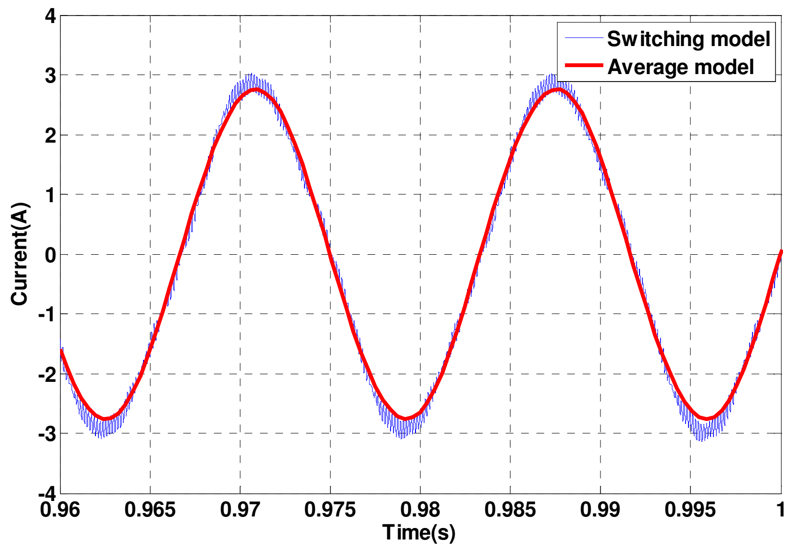


Figure 2.22 Input AC current of switching model and average model

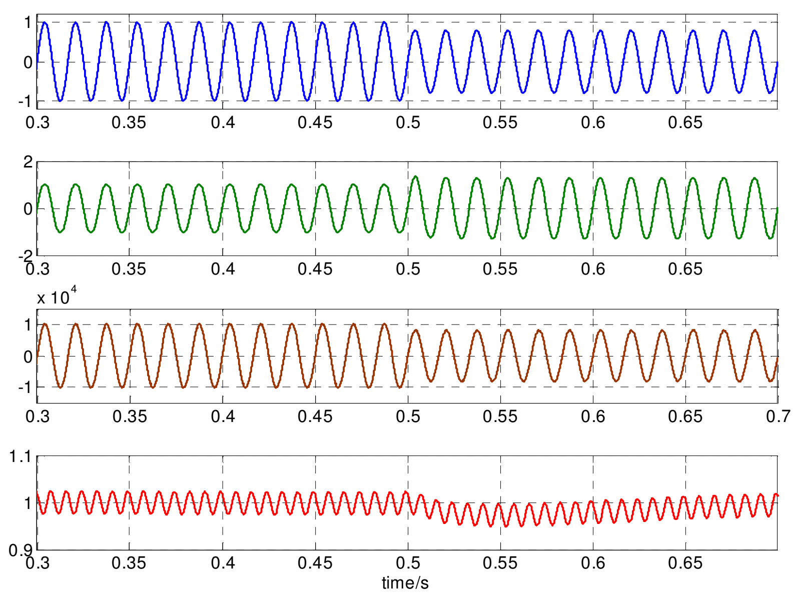


Figure 2.23 Average model simulation of 20% voltage sag

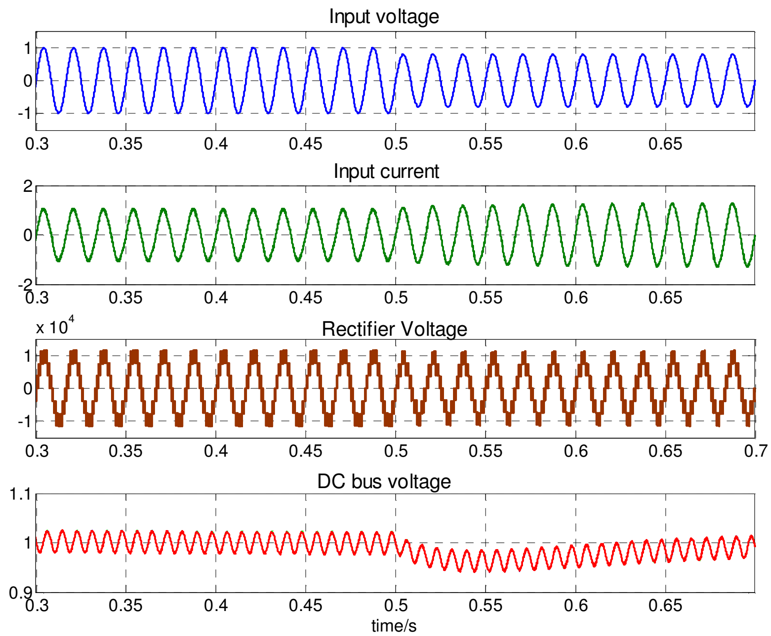


Figure 2.24 Switching model simulation of 20% voltage sag

The SST average model averages the voltage and current in each switching cycle. The modeling process involves approximations to neglect the switching frequency components. The limitations of the average model are:

1) The SST average model does not model the SST diode charging. The detailed switching mode simulation should be used in SST start up, shut down or other operation state machine changes that involve diode charging.

2) The average model can only be used for the system simulation where the PWM switching is applied to the SST system. When the simulation involves non-PWM switching control, the SST switching model should be used.

3) The simulation results of the SST average model only represent the average voltage or current response in each switching cycle. The model can not be used to investigate the harmonics components of the SST system.

2.4. Average Model Simulation

In order to verify the SST controller and the developed average model, simulations in Matlab/Simulink are carried out under conditions of load change, regeneration (with DRER or DESD connected at the SST output), and input voltage sag. The SST parameters are shown in Table 2.2. Figure 2.25 is the SST simulation system block.

Table 2.2 SST Average Model Simulation Parameters

Input AC voltage	7.2kV
Power rating	20kVA
Line inductance Ls	230mH
High voltage DC capacitor	30uF
High voltage DC reference	3.8kV
Low voltage DC capacitor	2mF
Low voltage DC reference	400V
Transformer leakage inductance	165mH
Switching frequency for rectifier	1kHz
Switching frequency for DAB	3kHz
Rectifier control parameters (P, I)	0.3, 12
DAB control parameters (P, I)	1.5e-3, 0.2

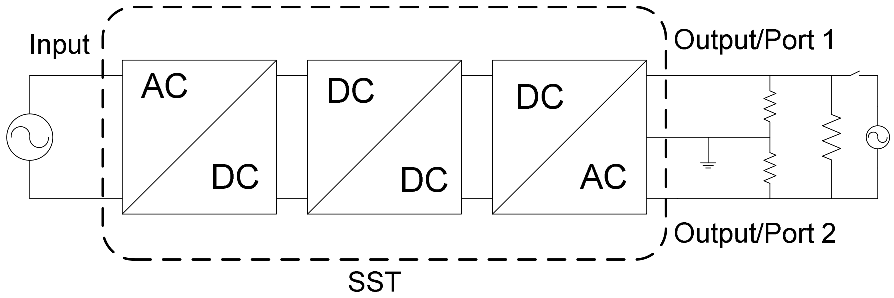


Figure 2.25 SST Simulation System

2.4.1. *Load change*

In this simulation, the step change load and unbalanced load conditions are taken into account. Figure 2.26 shows SST input and output power under load change. The active load power of port 1 is changed from 6kW to 9kW at 1.0s, and is changed back from 9kW to 6kW at 1.2s. The reactive load power of port 1 is changed from 0kVar to 5kVar at 1.0s, and then changed back from 5kVar to 0kVar at 1.2s. The power transferred at port 2 remains 6kW under both of these load change conditions. It can be seen from the simulation that only active power is being transferred by SST, while there is no input reactive power.

Figure 2.27 shows the DC voltage under load change. From the simulation one can see that the high DC bus voltage can be regulated at 3800V and the low DC bus voltage can be regulated at 400V under different load conditions.

Figure 2.28 shows the voltage and current of SST. The input current is in phase with the source voltage, which results in a unity power factor. The RMS output voltage remains 120V under different load conditions.

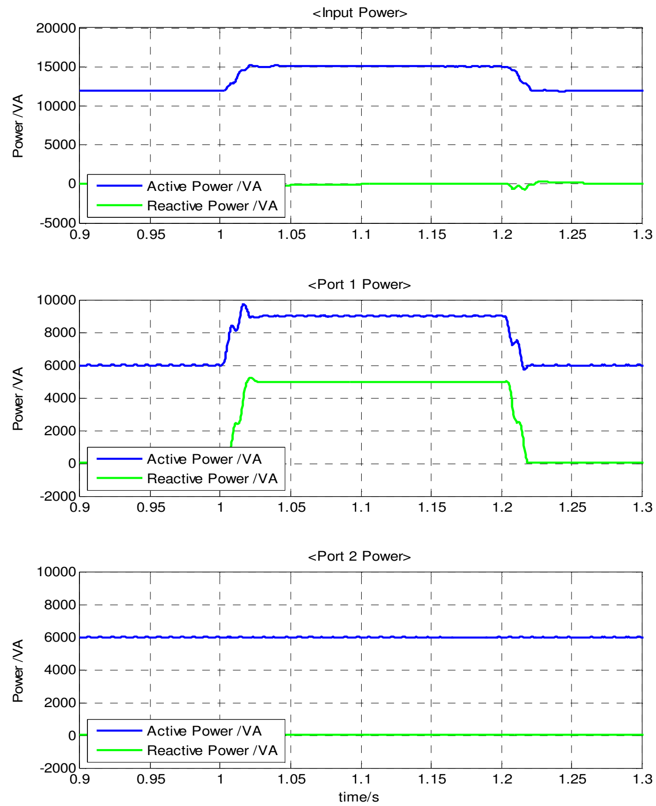


Figure 2.26 SST input and output power under load change

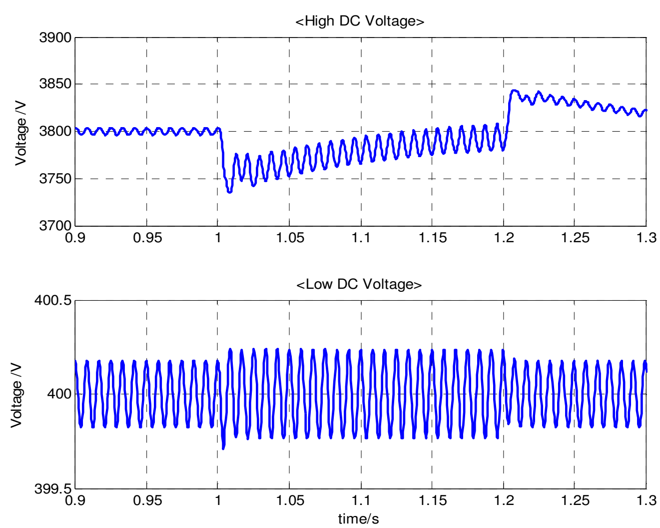


Figure 2.27 DC voltage response under load change

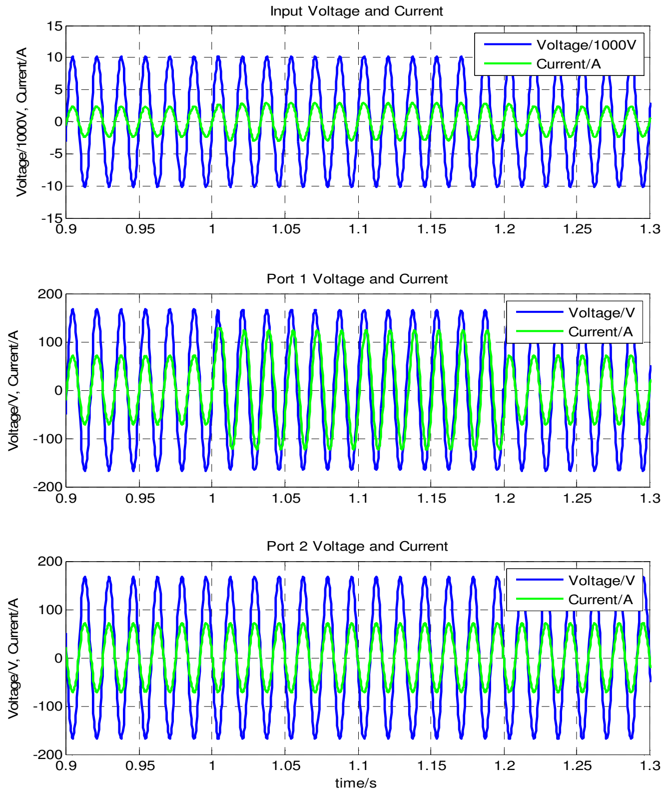


Figure 2.28 SST voltage and current under load change

2.4.2. *Regenerative mode*

In regenerative mode simulation, a distributed energy source is connected to SST, so the SST is sending power back to grid. Figure 2.29 and Figure 2.30 show the response under regenerative mode. As shown in Figure 2.29, 10kW active power is injected to both SST output ports at 2.0s and switched off at 2.2s. Thus, load power of both output ports are changed from 6kW to -4kW at 2.0s, then changed back from -4kW to 6kW at 2.2s. It can be seen from Figure 2.30 that DC Voltage can be regulated at reference voltage in the regenerative mode and the regenerative power is sent back to the grid.

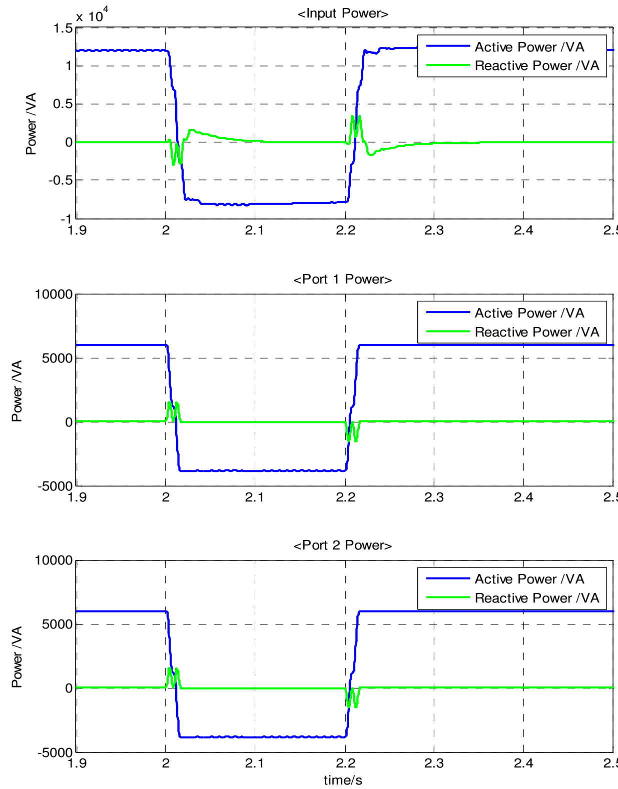


Figure 2.29 SST power under regenerative mode

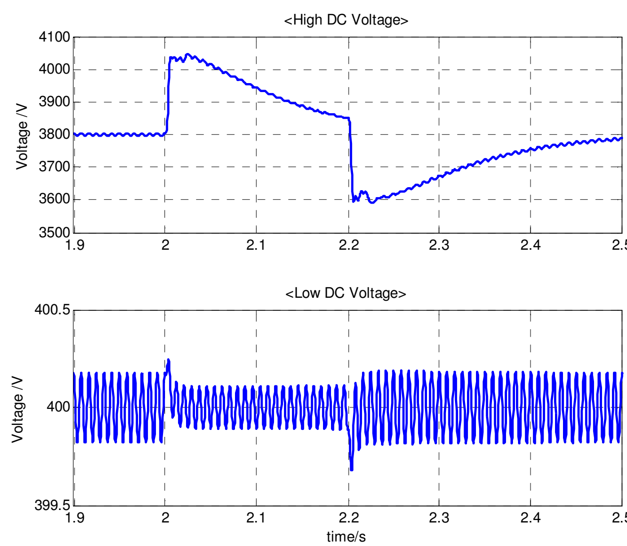


Figure 2.30 DC voltage response under regenerative mode

2.4.3. *Voltage sag*

One of the most important features of the SST is the voltage sag or swell ride through capability. The voltage sag or swell can be compensated by the rectifier stage and will not affect the load side voltage. The maximum input current determines how much a voltage sag the SST can compensate, and the maximum input voltage determines how much a voltage swell the SST can support. Furthermore, when the voltage sag is so large that the SST cannot continuously sustain the compensation, the DC bus capacitance (or energy storage) will determine how many cycles the SST can compensate before the system shut down. The SST design can be flexible enough to accommodate specific requirements.

Figure 2.31 and Figure 2.32 demonstrate the SST response under input AC voltage sag. In this simulation, the magnitude of input voltage changes from 100% to 80% at 3.0s, and then changes back from 80% to 100% at 3.2s. During the voltage sag, the high voltage DC bus varies a little around 3.8kV, but the low voltage DC bus can be stabilized at 400V, the output voltage is not affected by the input voltage sag, and the input current still maintains a unity power factor.

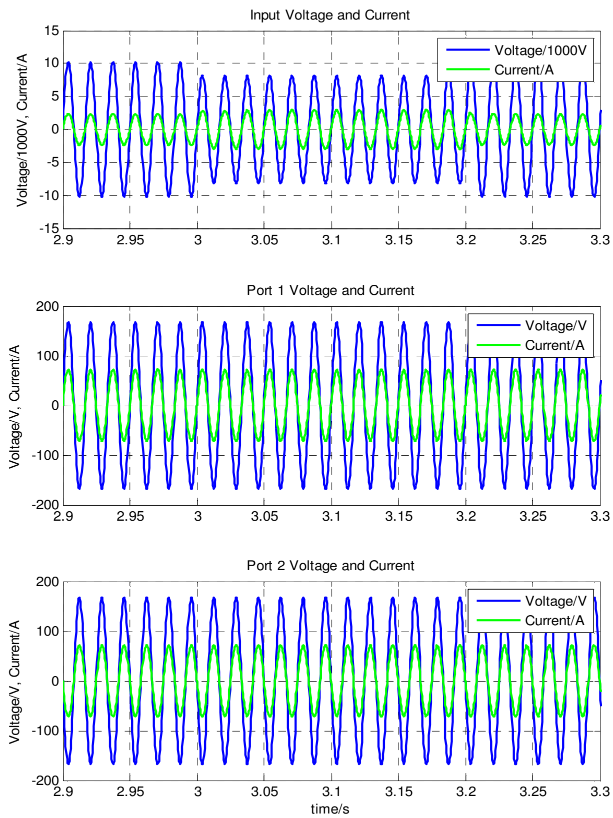


Figure 2.31 SST response under input AC voltage sag

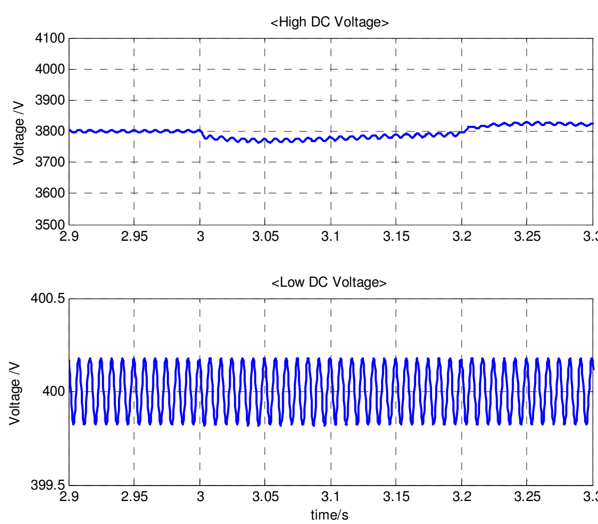


Figure 2.32 DC voltage response under input AC voltage sag

The above system simulation results illustrate that the SST is susceptible to neither source nor load side disturbances. The voltage sag ride-through characteristic decouples the load from input AC voltage sags and greatly enhances the load side power quality.

2.4.4. *Short circuit fault*

The SST protection scheme for the output short circuit is, the SST will stay online but limit the load current to 2 times of the rated current. Then some of the electronic equipment loads are not affected and still able to operate under a lower voltage. After the circuit breaker (or fuse) trip the fault, the SST will again output rated voltage.

In the simulation, the output port A short circuit occurs at 3.5s, lasts for 100ms, then the fault is cleared at 3.6s. The output port B remains normal 10kW load constantly.

Figure 2.33 is the SST Input voltage and current. The input current decreases during short circuit fault due to the lower power transfer. Figure 2.34 and Figure 2.35 demonstrate the output voltage and current of port A and port B, respectively. The output current of port A is limited during the short circuit fault with the SST remaining on line. As soon as the short circuit fault is cleared, the output voltage recovers to rated value. As shown in Figure 2.35, there is no significant affect to Port B during Port A short circuit.

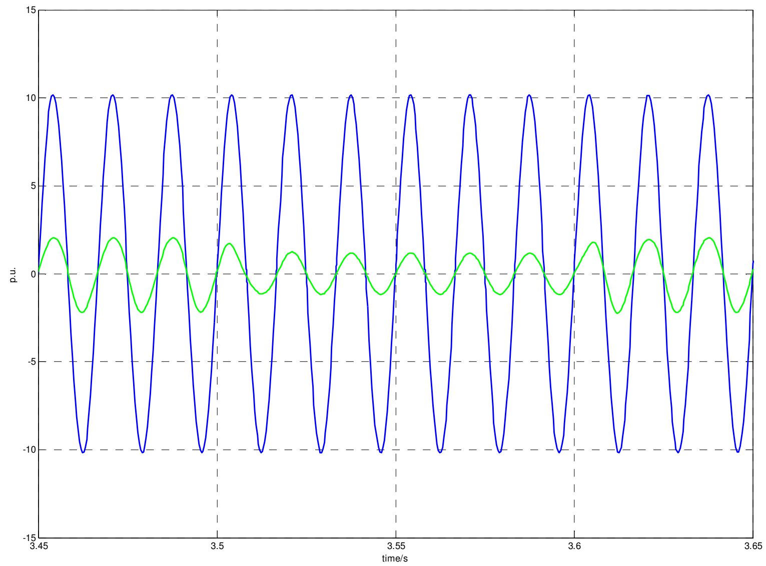


Figure 2.33 SST Input voltage and current

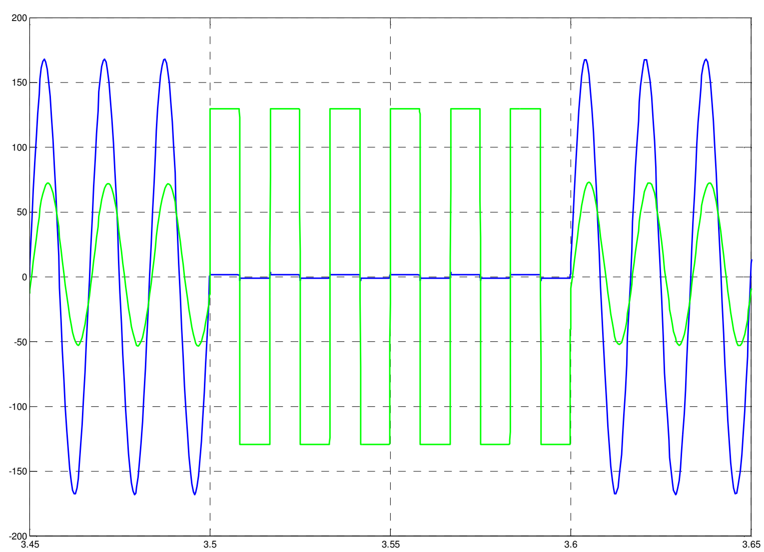


Figure 2.34 Port A output voltage and current

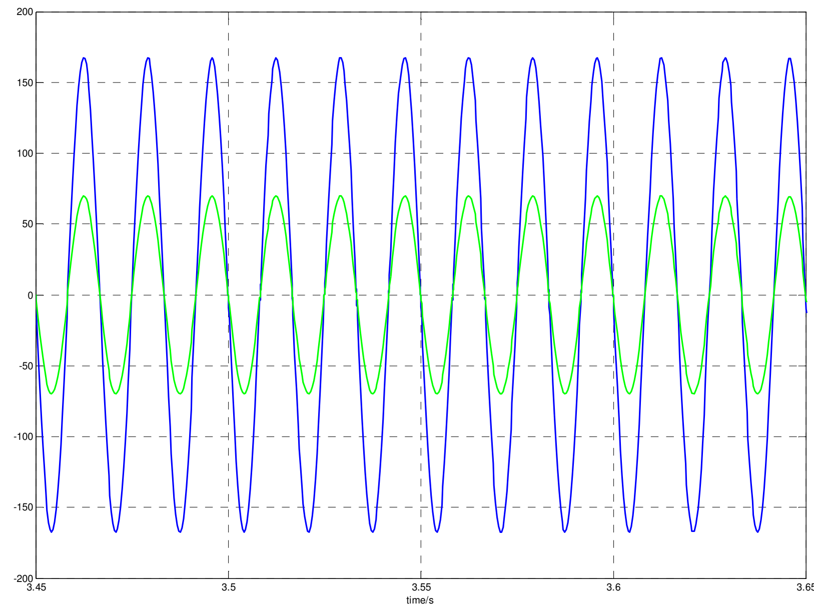


Figure 2.35 Port B output voltage and current

2.5. Switching Model Simulation

The switching model of the solid state transformer is implemented in Matlab/Simulink to verify the SST control algorithm. The steady state simulation, reactive power control, dynamic load change and voltage sag simulations are carried out with the switching model.

2.5.1. *Steady state simulation*

In the steady state simulation, the SST system parameters are shown in Table 2.2. The input of the SST is 7.2kV AC, and the output is connected to a 20kW load. The SST voltage base value is $7.2\sqrt{2}kV$, current base value 4A. Figure 2.36 shows the SST input voltage, input current and rectifier PWM voltage. Figure 2.37 shows the high voltage DC bus. Figure

2.38 is the DAB primary voltage, secondary voltage, primary current, secondary current. Figure 2.39 is the low voltage DC bus. Figure 2.40 shows the SST inverter stage steady state output voltages.

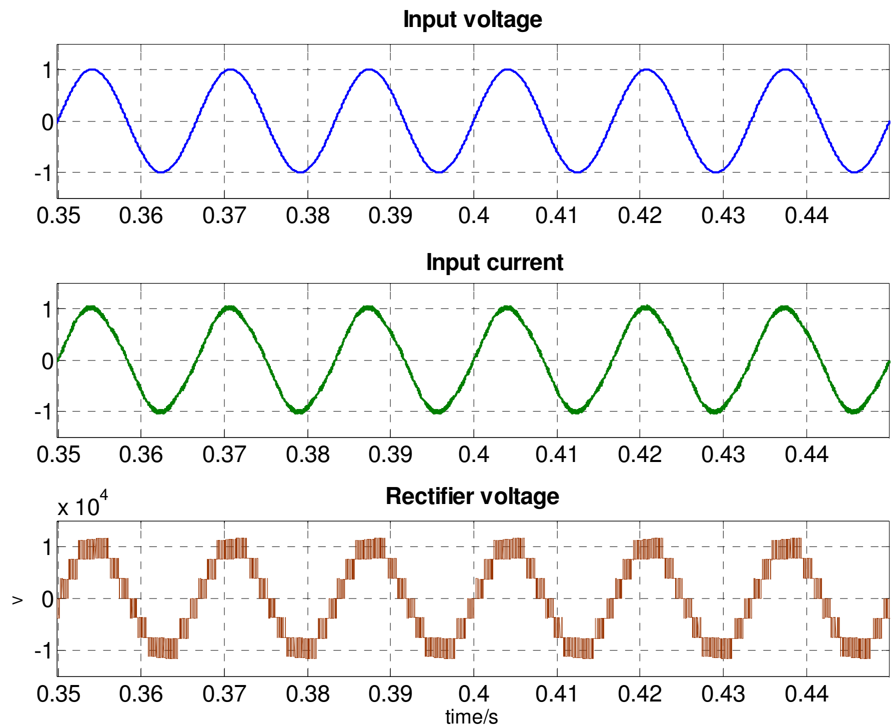


Figure 2.36 SST rectifier stage steady state simulation (SST input voltage, input current and rectifier PWM voltage, pu)

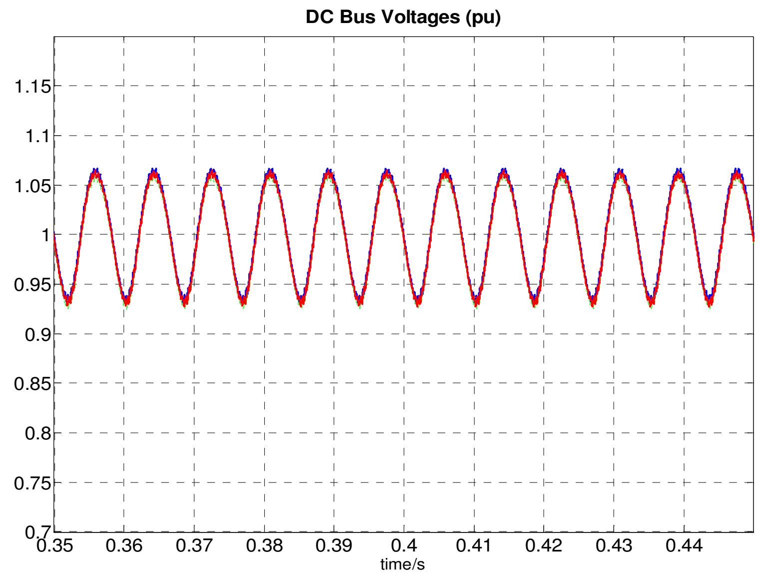


Figure 2.37 SST rectifier stage steady state simulation (High voltage DC bus, pu.)

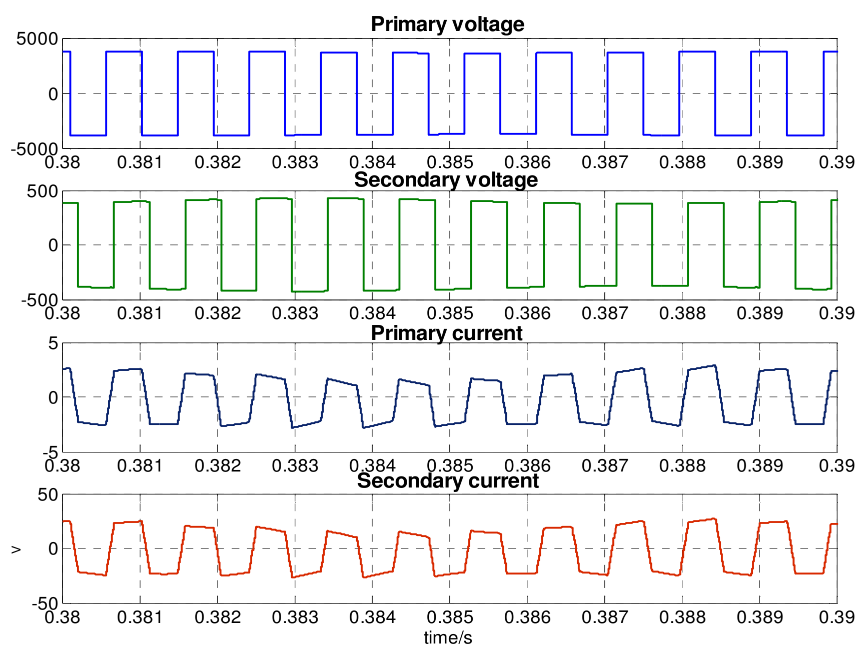


Figure 2.38 SST DAB stage steady state simulation (DAB primary voltage, secondary voltage, primary current, secondary current)

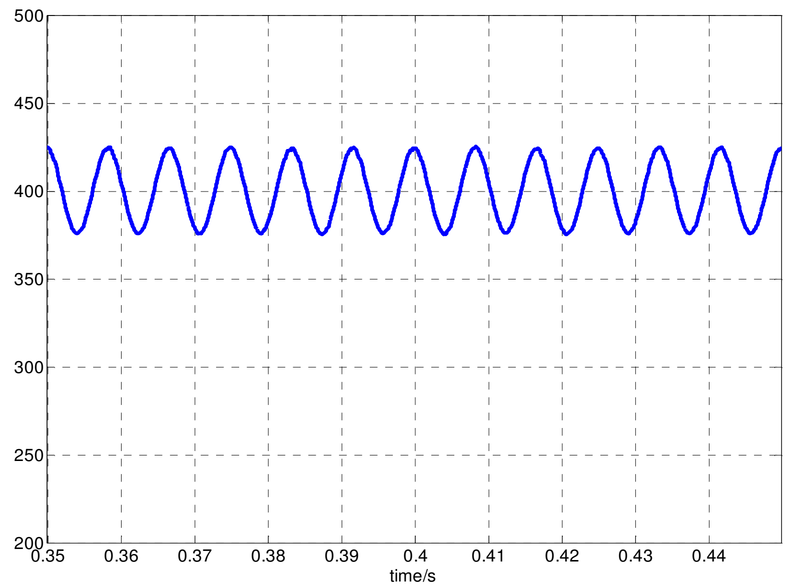


Figure 2.39 SST DAB stage steady state simulation (low voltage DC bus)

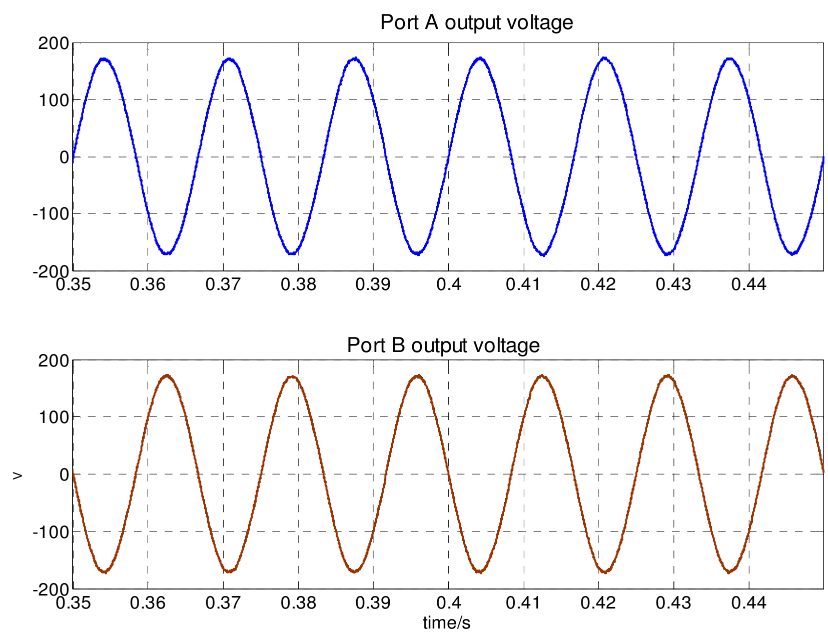


Figure 2.40 SST inverter stage steady state simulation (output voltages)

2.5.2. *Reactive power compensation*

The SST rectifier stage not only converts the input AC to regulated DC voltages, but also has reactive power compensation capabilities. Depending on the reactive power reference in the SST controller, the SST can generate or absorb the rated reactive power to the power grid. This fast and controllable local reactive power compensation is beneficial to support the system voltage, reduce the transmission line loss and enhance the power system stability. The reactive power control is verified in two cases. In both cases, the SST operates in reactive and capacitive mode, respectively.

Figure 2.41 shows the simulation of the SST input voltage and current in the capacitive mode with Iq=0.2 pu. The input current is leading the input voltage, so the SST is generating reactive power to the input. Figure 2.42 is the SST input voltage and current in the inductive mode (Iq =-0.2 pu). The input current is lagging the input voltage, so the SST is absorbing reactive power from the input AC.

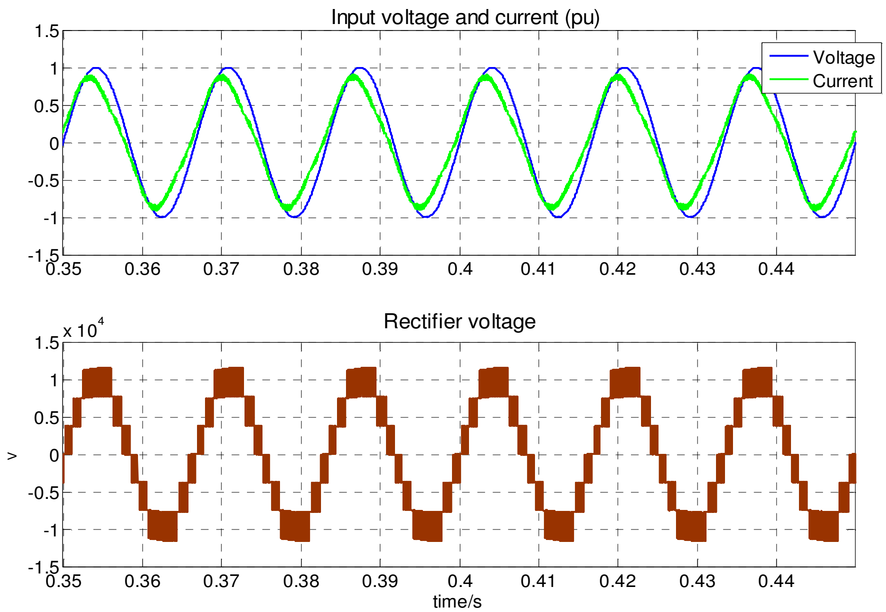


Figure 2.41 SST capacitive mode simulation

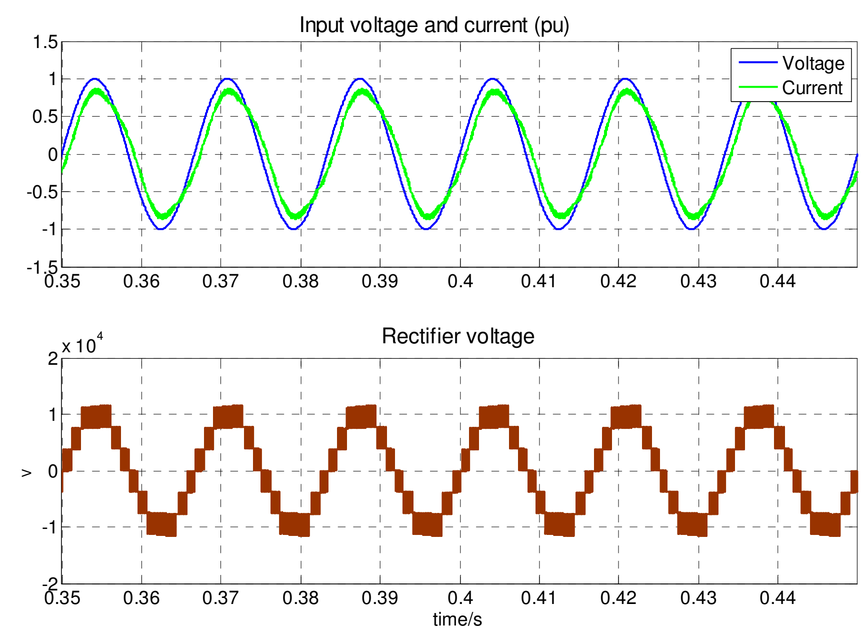


Figure 2.42 SST inductive mode simulation

2.5.3. *Dynamic load change*

In the dynamic load change simulation, the SST output load, shown in Figure 2.43, changed from 4kW (20%) to 20kW (100%) at 0.5s and from 20kW (100%) to 4kW at 0.9s (20%). The DC bus voltages have a transit time about 5 cycles, then settle down to the reference voltage. Figure 2.44 and Figure 2.45 are the simulation of the load change. The input current decreases as the load power is reduced. The low voltage and high voltage DC bus have a transient time of 5 cycles and then recovers to the reference.

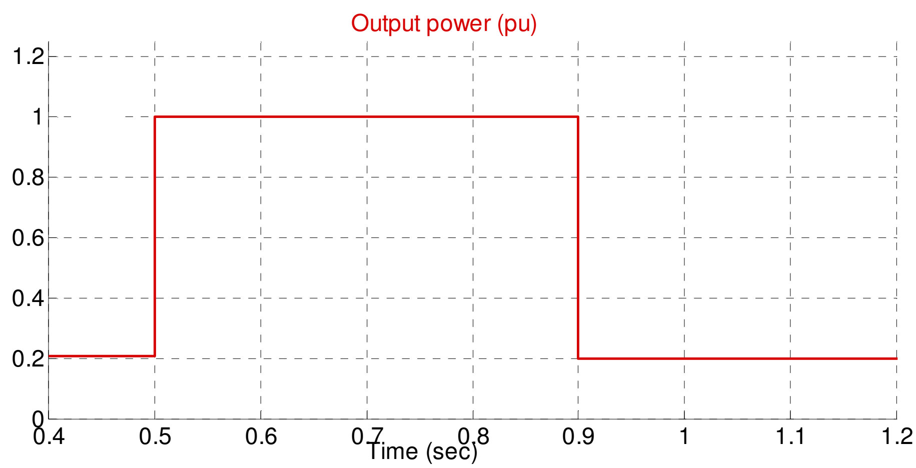


Figure 2.43 SST output load change

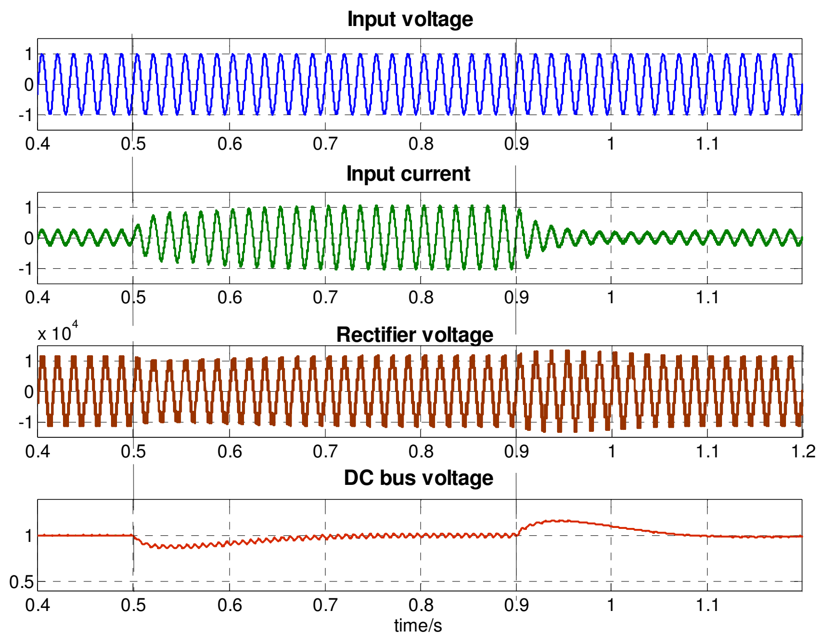


Figure 2.44 SST load change simulation

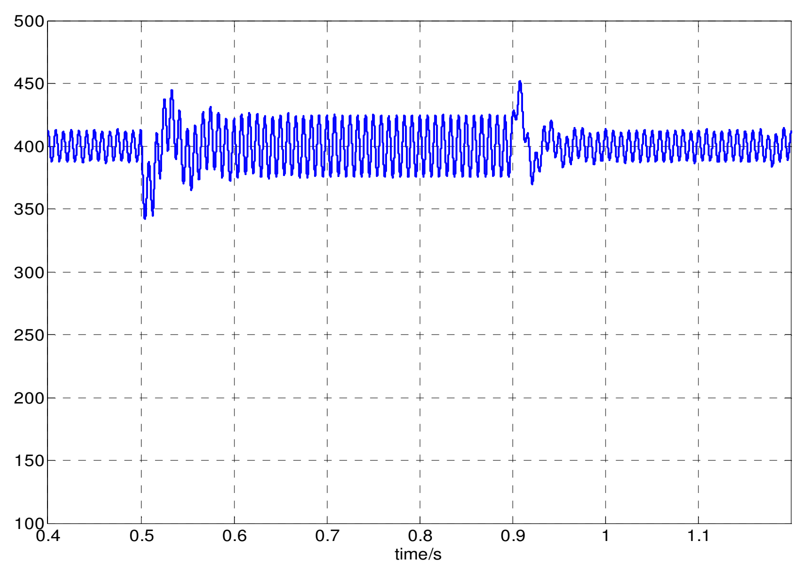


Figure 2.45 SST load change simulation (low DC bus votlage)

2.5.4. *Voltage sag simulation*

In the voltage sag simulation, as shown in Figure 2.46, the magnitude of input voltage changes from 100% to 80% at 0.5s, and then changes back from 80% to 110% at 0.9s. Figure 2.47 demonstrates the SST response under input AC voltage sag. During the voltage sag, the high voltage DC bus varies slightly around 3.8kV, but the low voltage DC bus can be stabilized at 400V, the output voltage is not affected by the input voltage sag, and the input current still maintains a unity power factor.

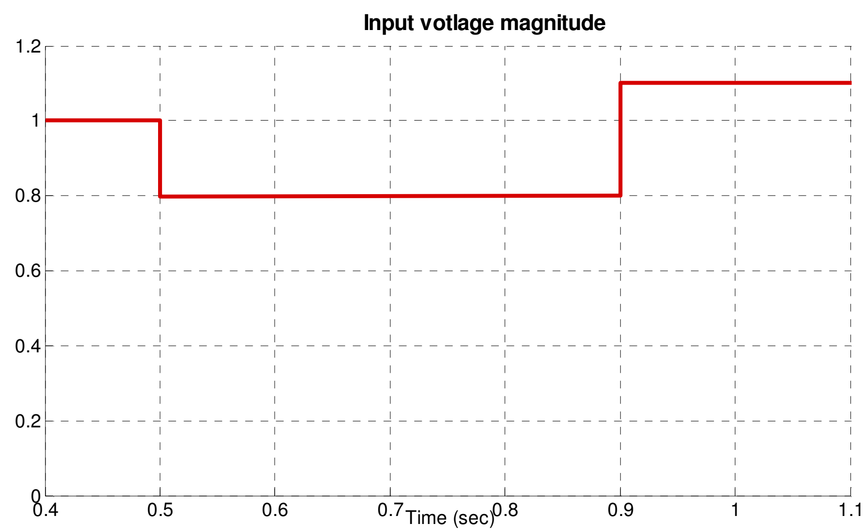


Figure 2.46 SST input voltage magnitude (pu)

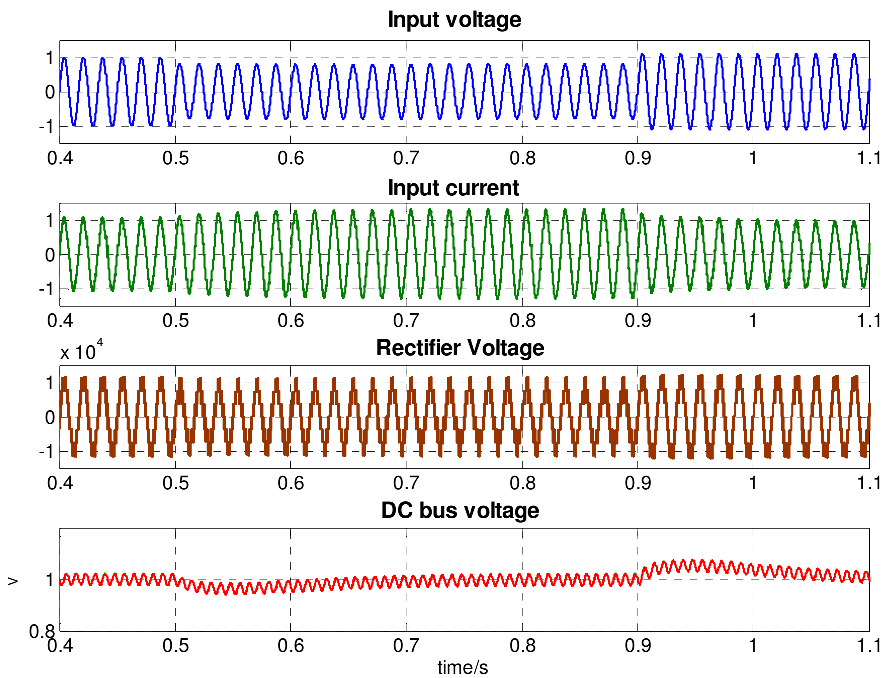


Figure 2.47 SST voltage sag simulation

2.6. Summary

In this chapter, a 20 kVA cascaded H-bridge converter based solid state transformer is proposed to interface with 7.2kV distribution voltage. The SST system design, including the circuit configuration, the selection of the DC bus voltage, DC link capacitance and input AC Inductor are analyzed. The single phase d-q vector controller for the rectifier stage and the phase shift controller for the Dual Active Bridge (DAB) stage are both designed and analyzed. The average model of the SST, including AC/DC rectifier, DAB and the DC/AC inverter stage are developed, with the aim to enable dynamic system level simulation studies of the FREEDM distribution system. The detailed switching level SST simulation is also implemented in Matalb/Simulink. The average model is verified by comparing the simulations with the detailed switching model. Based on the proposed control strategy, the dynamic system level SST simulation with both the average model and switching model is performed under the conditions of steady state, load change and voltage sag. The simulation results verify the control scheme and demonstrate the functionalities and advantages of the SST.

Chapter 3. Voltage and Power Balance Control

The rectifier stage of the Solid State Transformer (SST) consists of a seven level cascaded H-Bridge converter. One of the main disadvantages of the cascaded H-bridge converter is the voltage unbalance that could appear on the DC side of different H-bridges (E_1, E_2, and E_3, shown in Figure 3.1) due to the device loss mismatching and H-Bridge real power differences [49][50][51][52][53]. The unbalance issue becomes worse when the SST operates at no-load or light-load condition, because a small power difference is a significant percentage of the real power and will result in a large voltage unbalance. The unbalanced voltage will cause the capacitor or device over-voltage in the H-Bridge and trigger the system over-voltage protection.

The DAB stage consists of three DAB modules in parallel. The power unbalance (P_1, P_2 and P_3, shown in Figure 3.1) can be caused by the transformer parameter mismatching (such as leakage inductance or turns ratio) and DC bus voltage differences. The power unbalance may cause device over-current issue.

In the SST, three H-Bridge modules are in series to support the 7.2kV distribution voltage at the rectifier state. Therefore, the power balancing between the modules is indispensable to prevent the SST from overvoltage or overcurrent caused by the unbalance power transfer.

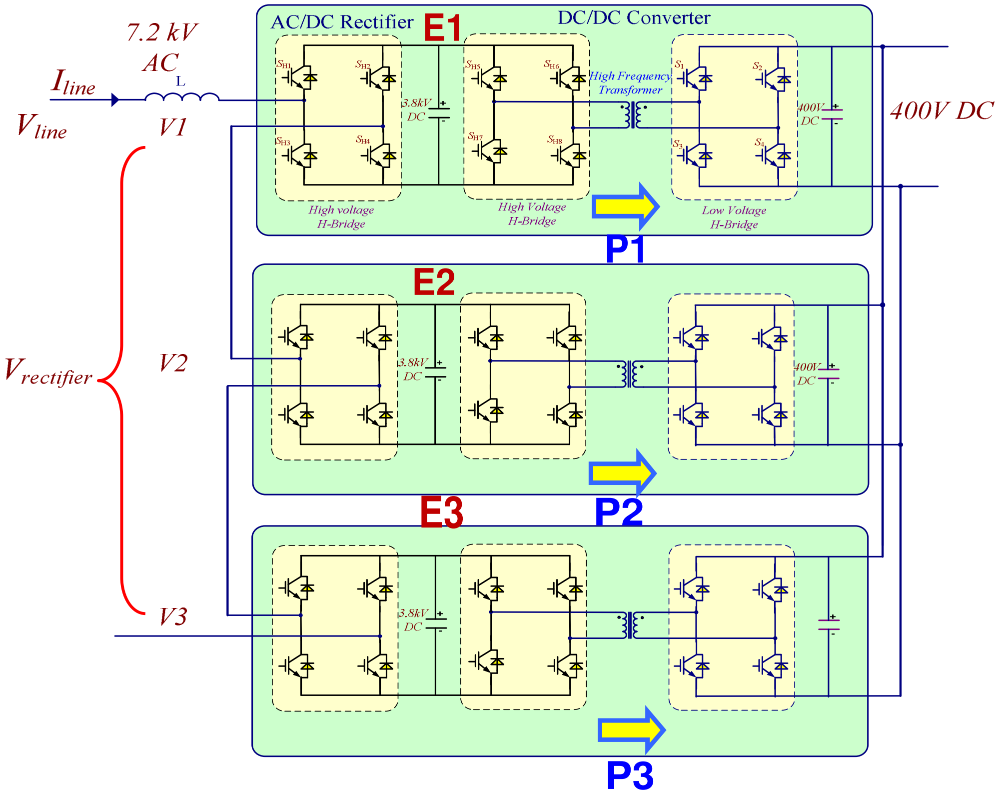


Figure 3.1 Voltage and power unbalance in SST

3.1. Review of voltage and power balance control methods

To avoid the voltage unbalances, an adequate control technique of the cascaded H-bridge converter-based SST must regulate the active power that is individually controlled by each H-bridge. Meanwhile, it should be guaranteed that the reactive power that is delivered by all H-bridges is equally distributed [54]. Relevant research focuses mainly on the unbalance issues in STATCOM or drive applications and no power control method has been mentioned.

In reference [49][50][51], several cascaded H-bridge multilevel converter applications are presented. The low frequency PWM modulation techniques for STATCOM are presented.

The DC bus voltage is balanced by using different switching patterns to charge and discharge each H-Bridge capacitor, but the reactive power is not controlled. Reference [55] presents an individual voltage balancing strategy to balance the DC bus voltage with PWM modulation. The method maintains the delivered reactive power equally distributed among all H-Bridges. However, the method is based on the STATCOM application and no power unbalance constraints are mentioned in the paper. Reference [56] presents a method that ensures the DC bus voltages converge to the reference value when the loads have different power. The method results in different switching frequencies for the H-Bridges and a complicated controller implementation. Reference [57][58] present different PWM modulation methods to balance the DC bus voltages, however the balance range and power control are not included.

Different from the STATCOM and drive application, the SST requires a high frequency modulation and both real and reactive power control. Furthermore, due to the intrinsic constraint of the cascaded rectifier topology, the voltage balance control is limited and the power balance control is required.

3.2. SST voltage balance control

The single phase *d-q* vector controller for the rectifier stage regulates the total DC bus voltage and controls the reactive power. Based on the single phase *d-q* control, a voltage balance control method is proposed to solve the voltage unbalance on the DC voltages of different H-bridges. The voltage balance control basically adjusts the modulation signal d_{a1}, d_{a2}, d_{a3} individually to achieve different real power of the H-Bridges. In Figure 3.2, the d_d

and d_q are calculated according to the single phase d-q vector control. Figure 3.3 is the voltage balance controller. The individual DC bus voltages of the first two H-Bridges, E_1 and E_2 are compared with the DC bus voltage reference E_{ref} to generate d-axis compensation Δd_{d1} and Δd_{d2} by a PI regulator. Then Δd_{d1} and Δd_{d2} are added to the original d_d. Therefore, d_{d1} for the first H-Bridge and d_{d2} for the second H-Bridge are adjusted so that the real power of each H-Bridge can be changed. The real power of the H-Bridge with a lower (or higher) DC bus voltage is increased (or decreased) to eliminate the voltage unbalance. For the third H-Bridge, $\Delta d_{d3} = -\Delta d_{d1} - \Delta d_{d2}$, so the total DC bus voltage regulation is not affected. Meanwhile, the q-axis current references are still independent form the d-axis, which means the reactive power can be controlled independently.

In order to verify the proposed voltage control, the switching model simulation of the 20kVA SST is implemented in Matlab/Simulink. The SST simulation system parameters are shown in Table 3.1.

In the simulation, the real power P_1, P_2 and P_3 of the three H-Bridges are controlled by connecting different resistor to the DC buses, E_1, E_2, and E_3. Before 0.83s, the three H-Bridge have the same amount of real power, P_1=P_2=P_3=1.0pu (20kW/3). Then at 0.83s, P_3 are decreased to 0.8pu, P_1=P_2=1.0pu, P_3=0.8pu.

Two different cases are simulated. Figure 3.4 shows the three DC bus voltages without balance control. The three H-Bridge DC bus voltages become unbalanced after the power change. The H-bridge which transfers more power has the highest DC bus voltage. Figure 3.5

shows the three DC bus voltages with balance control. With the voltage balance controller, the three DC bus voltages are equally regulated in the steady state.

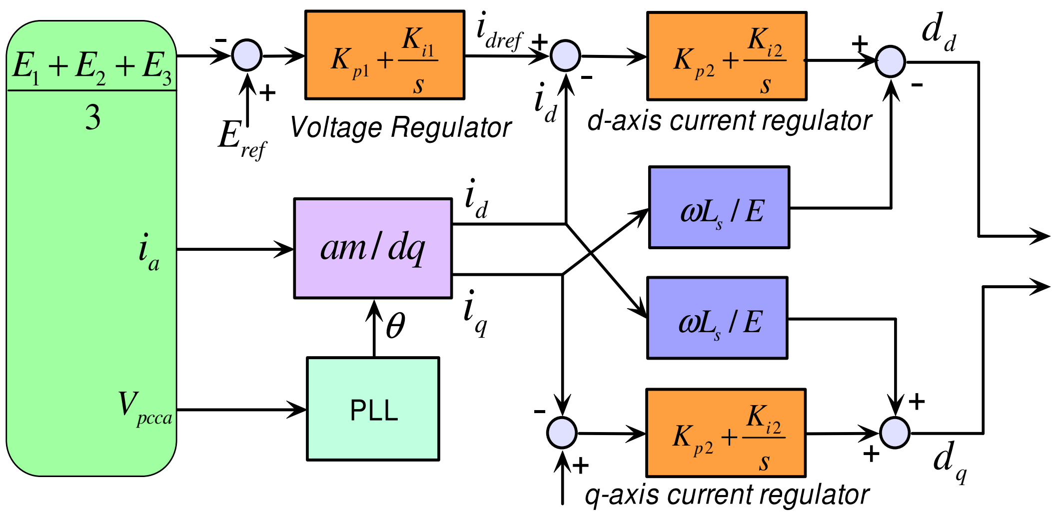


Figure 3.2 Rectifier single phase d-q vector controller

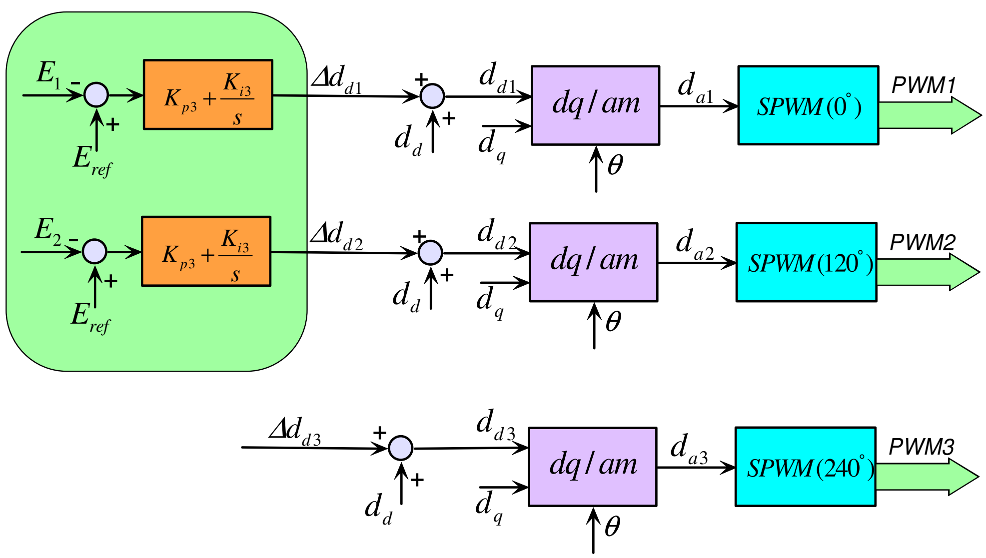


Figure 3.3 Voltage balance control based on single phase d-q vector

Table 3.1 SST Simulation Parameters

Input AC voltage	7.2kV
Power rating	20kVA
Line inductance Ls	230mH
High voltage DC Capacitor	30uF
High voltage DC reference	3.8kV
Low voltage DC Capacitor	2mF
Low voltage DC reference	400V
Transformer leakage inductance	165mH
Switching frequency	1kHz

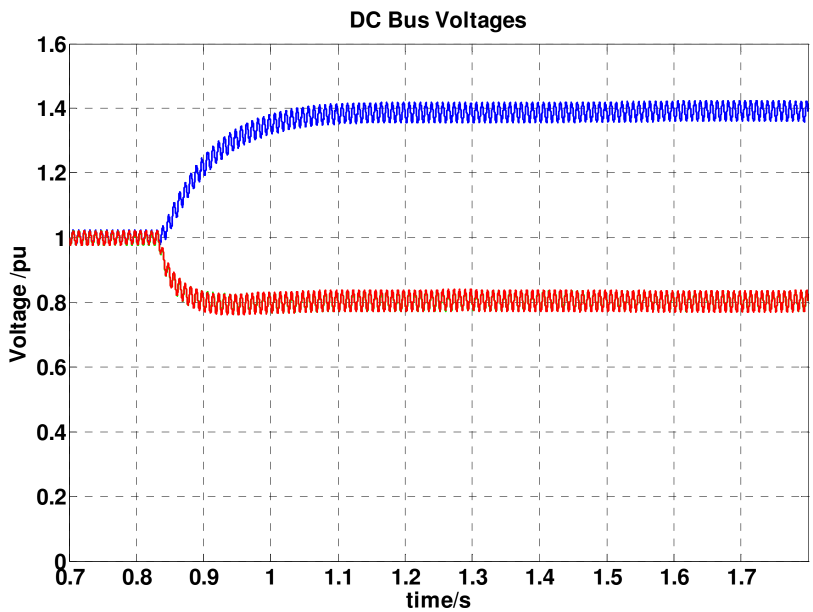


Figure 3.4 DC bus voltages without voltage balance control

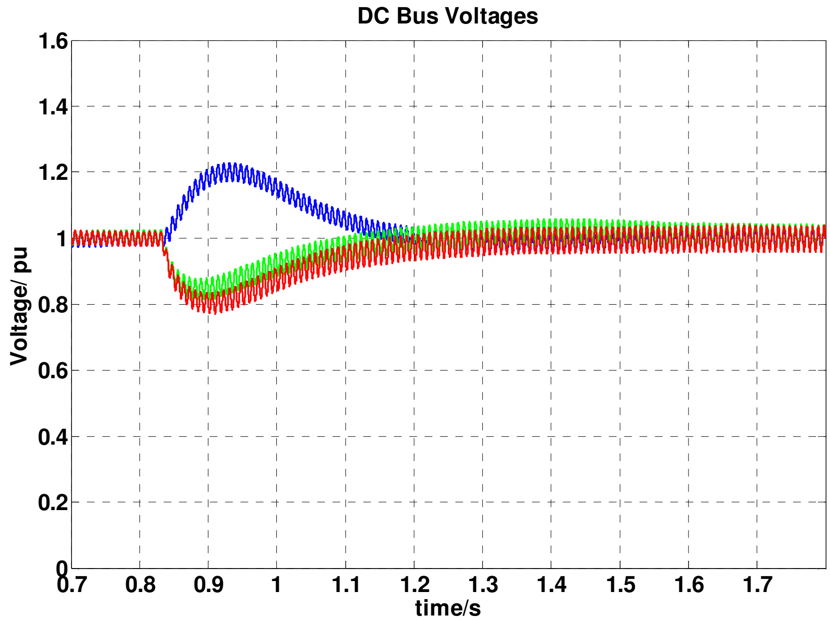


Figure 3.5 DC bus voltages with voltage balance control

3.3. Voltage balance constraints

The proposed the voltage controller can maintain the balanced DC bus voltage when the real power is different for each H-Bridge. However, due to the intrinsic constraints of the cascaded H-Bridge circuit, in order to maintain the DC bus balanced, the real power unbalance range of the H-Bridges is limited. This limitation is determined by the input AC voltage, DC bus voltage reference and the input inductance. As shown in Figure 3.6, the constraints of the voltage vectors are given by equation (3.1)-(3.2).

$$V_1 + V_2 + V_3 = V_{line} - j\omega L I_{line} \tag{3.1}$$

$$V_1 = (d_1 + jq_1)E, V_2 = (d_2 + jq_2)E, V_3 = (d_3 + jq_3)E \tag{3.2}$$

Where, V_n is the N H-Bridge voltage vector, V_{line} is the input voltage vector, I_{line} is the input real power vector, L is the input inductor, d_n and q_n are the d-axis and q-axis duty cycle generated by the controller, and E is the DC bus reference voltage of each H-Bridge.

Rearrange the equation (3.1) and (3.2),

$$d_1 + d_2 + d_3 = \frac{V_{line}}{E}, q_1 + q_2 + q_3 = \frac{-j\omega L I_{line}}{E} \tag{3.3}$$

The real power of each H-Bridge is calculated as:

$$P_1 = I_{line} d_1 E, P_2 = I_{line} d_2 E, P_3 = I_{line} d_3 E \tag{3.4}$$

Then, d_1 is derived as:

$$d_1 = \frac{P_1}{P_{in}} \frac{V_{line}}{E} \tag{3.5}$$

Without loss of generality, assume $d_1 \geq d_2 \geq d_3$, the reactive power is equally distributed and ${d_1}^2 + {q_1}^2 < 1$ (no over-modulation).

So $d_1 \leq \sqrt{1 - (\frac{\omega L I_{line}}{3E})^2}$, then the maximum power P_1 should meet the equation (3.6).

$$\frac{P_1}{\sum_1^N P_n} \leq \frac{E}{V_{line}} \sqrt{1 - (\frac{\omega L I_{line}}{NE})^2} \tag{3.6}$$

Where, N is the number of H-Bridges.

In order to balance the DC bus voltages, the real power of each H-Bridge has to be within the range in equation (3.6). In other words, if the power unbalance is too large, the H-Bridge will not be able to maintain the balanced DC bus voltage. For the designed SST system, the maximum power unbalance happens when the maximum power $P_1 = 37\% P_{in}$. Figure 3.7

shows the simulation of DC bus voltages at maximum power unbalance condition. The DC bus voltage inevitably becomes unbalanced if the equation (3.6) is not satisfied.

When the SST is under light load condition, the power unbalance becomes much more severe because the device loss and transformer parameter mismatch account for a significant percentage of the total power, the power balance equation (3.6) cannot be assured. Therefore, a power balance control is needed to regulate the H-Bridge real power.

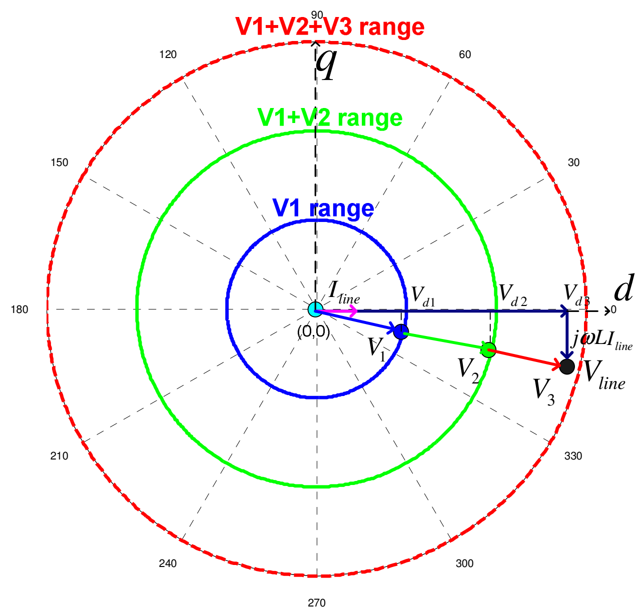


Figure 3.6 Rectifier voltage vector constraints

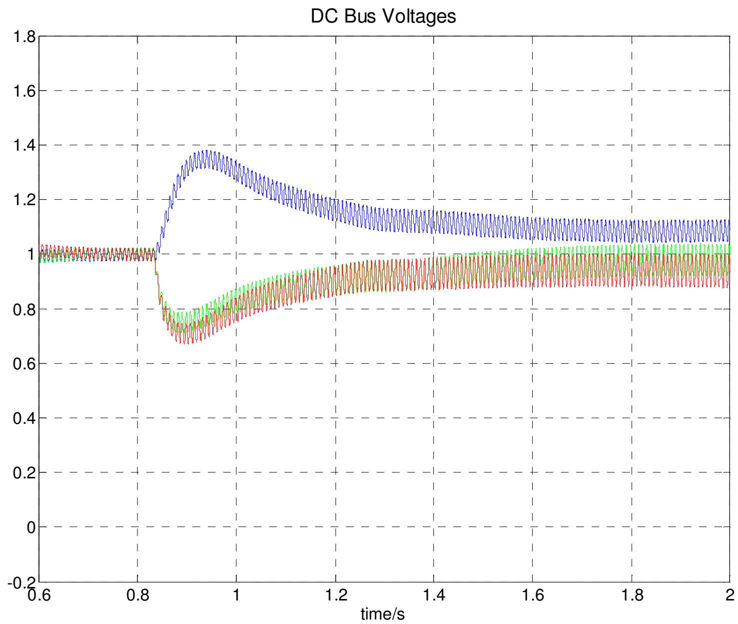


Figure 3.7 DC bus voltages at maximum power unbalance

3.4. SST power balance control

Due to the parameter variation of the high frequency transformers, such as leakage inductance and turns ratio, the three DAB currents can be different, which results in a power unbalance of the three DAB modules. A power balance control method is proposed to regulate the real power transferring through the DAB parallel modules. As shown in Figure 3.8, the voltage regulator compares the low voltage DC voltage V_{dcL} with the reference V_{dcL_ref} and generates the power references P_{ref} for the three DAB modules. Then the power regulator compares the calculated average power of each DAB module with P_{ref} and generates the phase shift angles φ_1, φ_2, φ_3 for the three DAB modules. Figure 3.9 shows how the average power calculator calculates the average power in each switching cycle (3 kHz). In the calculation, $P = \int_0^{\pi} V_{dcH} i_p dt$, the primary DC voltage V_{dcH} can be considered constant in a switching cycle. So the power calculation involves only the summation of current, which is easily implemented in DSP.

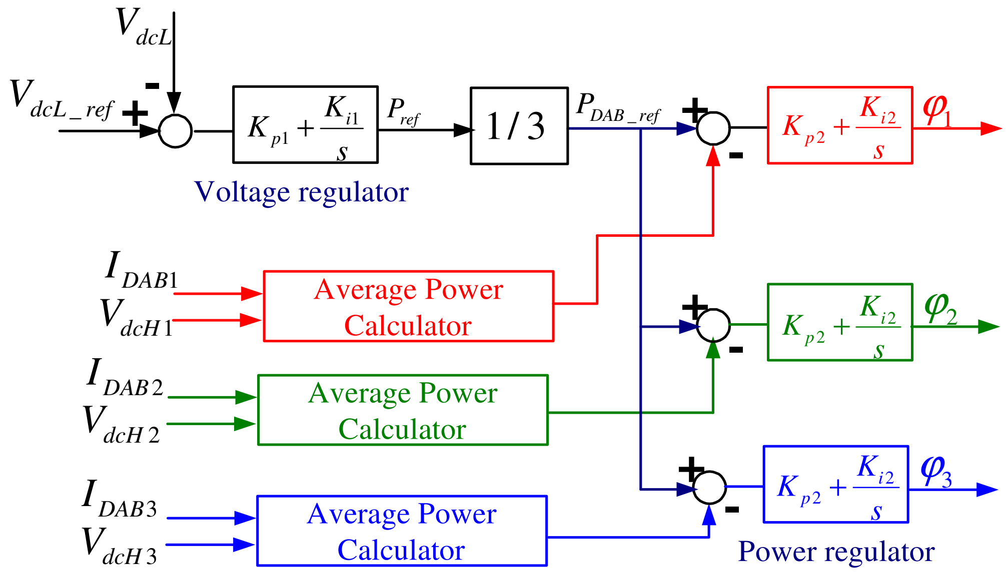


Figure 3.8 Power balance controller

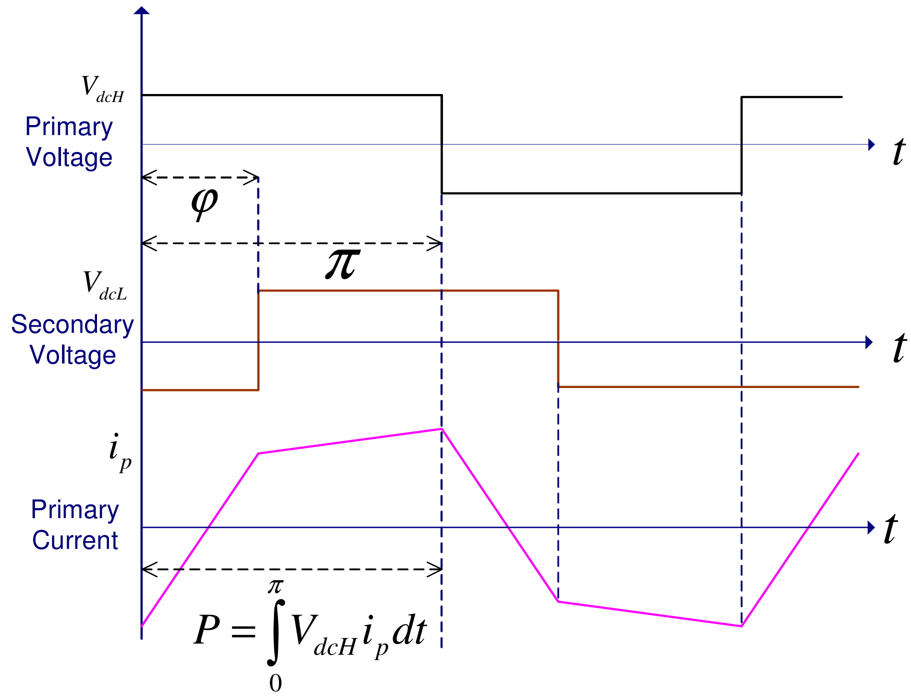


Figure 3.9 DAB average power calculation

The switching model simulation is implemented to verify the proposed power balance control. In the simulation, different leakage inductance values are set for the three transformers: 165mH, 165mH, 115mH (30% variation). Figure 3.10 and Figure 3.12 are the DAB primary currents and power without power balance control. The DAB module with smaller leakage inductance has large current and transfers more power. Figure 3.11 and Figure 3.13 illustrate the DAB primary currents and power with power balance control. The power transferring through each DAB module is balanced.

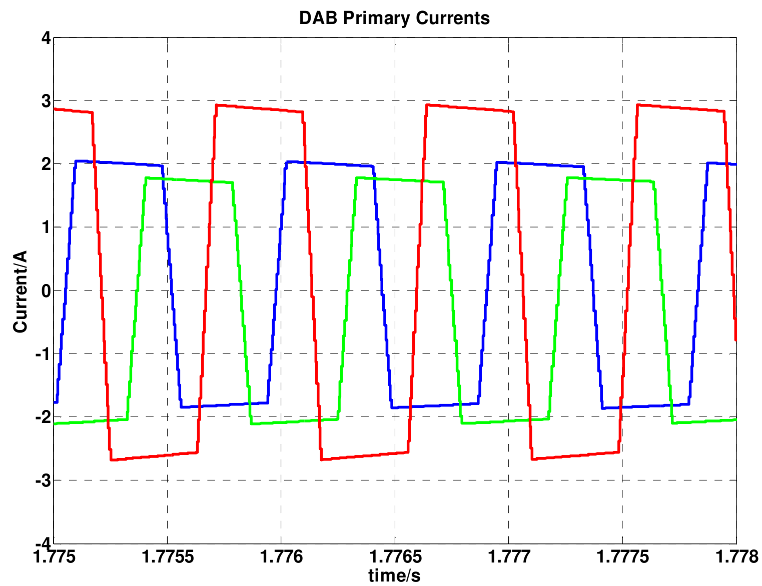


Figure 3.10 DAB current without power balance control

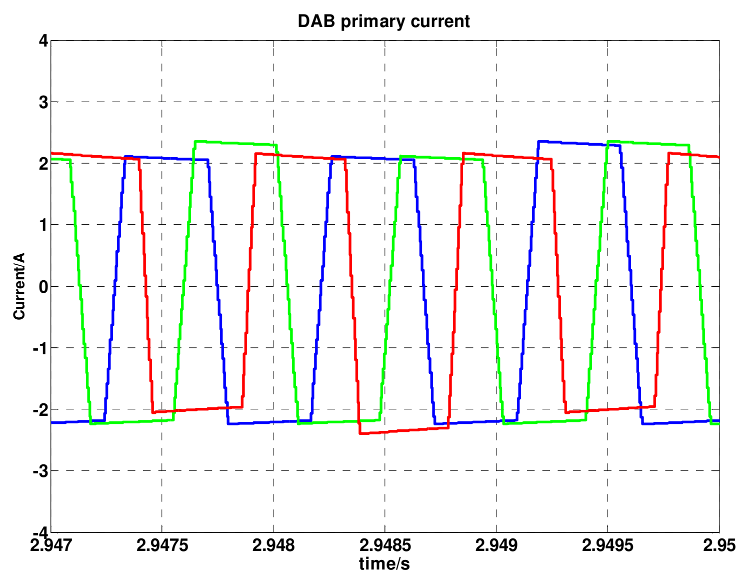


Figure 3.11 DAB current with power balance control

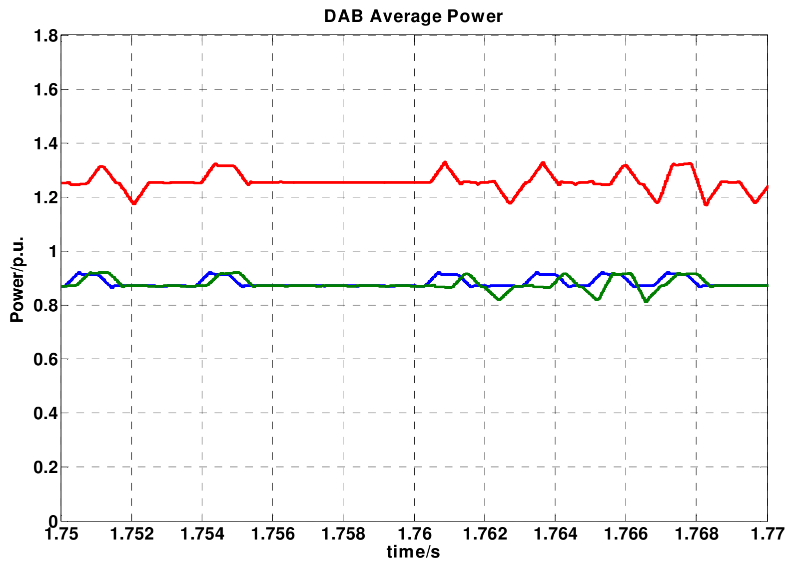


Figure 3.12 DAB power without power balance control

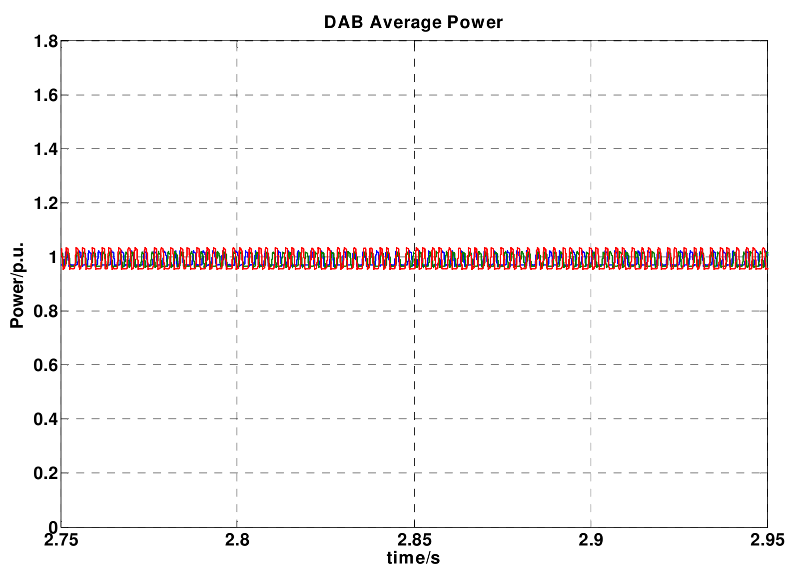


Figure 3.13 DAB power with power balance control

3.5. Experiment verification

To develop the SST controller and verify the proposed strategy, a scale-down SST prototype is implemented. The SST module prototype is designed as single phase input voltage 60Hz, 240V, and DC output 400V. The prototype consists of an cascaded H-Bridge AC/DC rectifier that converts 60Hz, 240V AC to 400V DC bus, a DC/DC converter that convert 400V to 400V DC bus with 1:1 high frequency transformer. The SST module output will connect to a DC/AC inverter that converts 400V DC to 120/240V AC. The prototype is implemented by using 600V 75A Intelligent Power Modules (IPM). The SST control algorithm is programmed in DSP TMS320F28335. Figure 3.14 is the SST rectifier stage diagram. The SST hardware prototype is introduced in detail in Chapter 5.

In order to verify the voltage balance controller, the load resistors connected to the DC bus are dynamically changed to create the real power differences. In this experiment, the DC bus voltage reference is 50V and the reactive power reference is zero, the load resistor R3 changes from 32Ω to 46Ω and R1 and R2 maintain as 32Ω. Figure 3.15 shows three DC bus voltages without the voltage balance control. The three DC bus voltages are all regulated at 50V when the loads are the same. However after the load change, the DC bus voltages become 56V, 56V and 43V (25% voltage unbalance) respectively. The H-Bridge with the larger load resister has a higher DC bus voltage. Figure 3.16 shows the three DC bus voltages with the voltage balance control. The balance controller regulates the DC bus voltage when there is a load change. The DC bus voltages have a transit time of about 4 cycles, then settle down to the same voltage. The experiment verifies the effectiveness of the voltage balance controller.

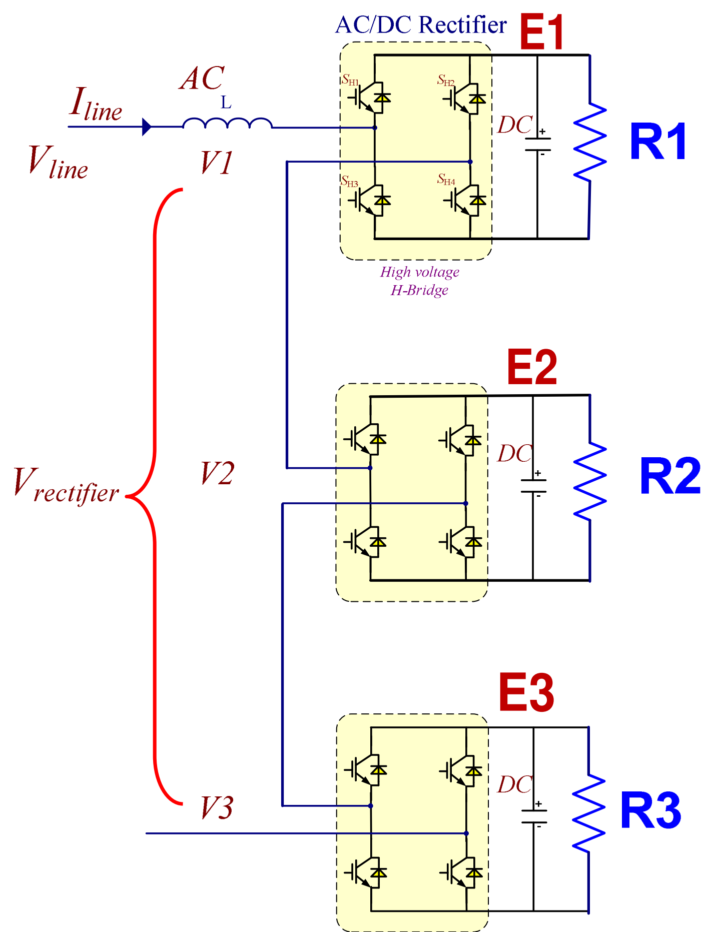


Figure 3.14 SST rectifier stage topology

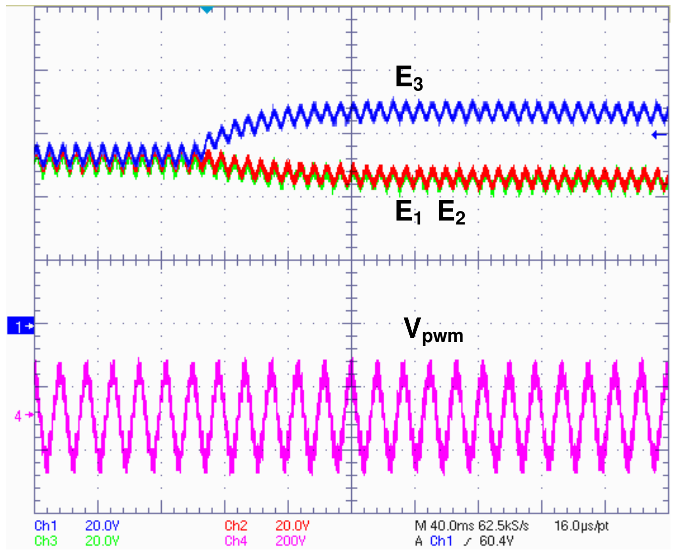


Figure 3.15 DC bus voltages without balance control (Ch1, DC bus voltage of H-Bridge #1 E_1, 20V/div; Ch2, DC bus voltage of H-Bridge #2 E_2, 20V/div; Ch3, DC bus voltage of H-Bridge #3 E_3, 20V/div; Ch4, rectifier PWM voltage V_{pwm}, 200V/div)

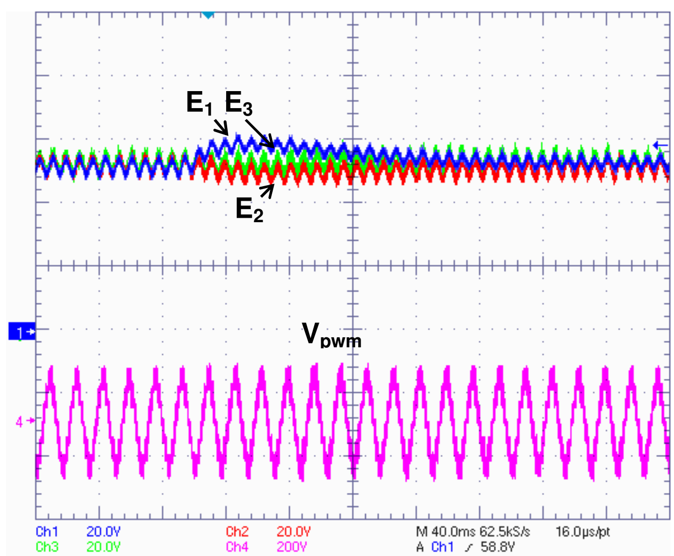


Figure 3.16 DC bus voltages with balance control (Ch1, DC bus voltage of H-Bridge #1 E_1, 20V/div; Ch2, DC bus voltage of H-Bridge #2 E_2, 20V/div; Ch3, DC bus voltage of H-Bridge #3 E_3, 20V/div; Ch4, rectifier PWM voltage V_{pwm}, 200V/div)

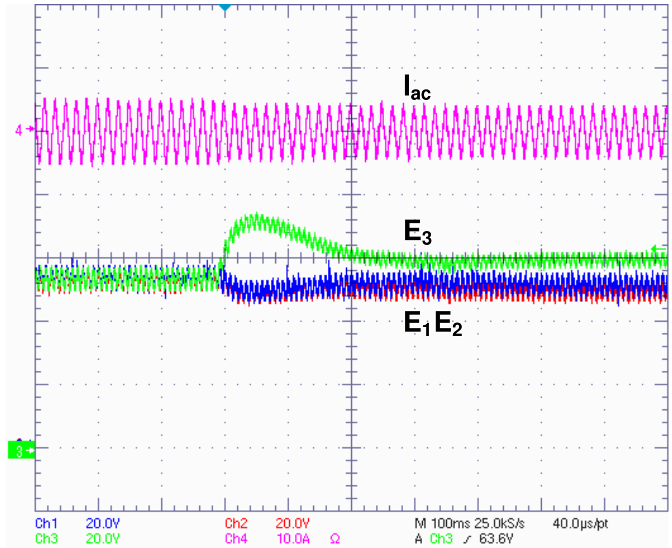


Figure 3.17 Power unbalance limit test, R3 changes from 32Ω to 65Ω (Ch1, DC bus voltage of H-Bridge #1 E_1, 20V/div; Ch2, DC bus voltage of H-Bridge #2 E_2, 20V/div; Ch3, DC bus voltage of H-Bridge #3 E_3, 20V/div; Ch4, input current I_{ac}, 10A/div)

According to equation (16), the maximum power unbalance happens when the load resistor R_3 is 65Ω and $R_1=R_2=32$Ω. Figure 3.17 demonstrates the DC bus voltages when R_3 changes from 32Ω to 65Ω. The power unbalance does not meet the equation (3.6) and the DC bus voltage will inevitably become unbalanced. Therefore, the proposed power controller is indispensable for the SST application.

3.6. Summary

In this chapter, a novel voltage control strategy is proposed to balance the rectifier capacitor voltages. Based on the single phase vector control, the voltage balance control adjusts the modulation signal individually to achieve different H-Bridge real power needed for the voltage balance. However, due to the intrinsic constraints of the cascaded H-Bridge circuit, the unbalance power range of each H-Bridge is limited. The power unbalance constraints of the cascaded H-Bridge rectifier are derived as equation (3.6). Furthermore, a power balance control is proposed to balance the real power through the DAB parallel modules. The power balance controller calculates the average power in each switching cycle and regulates the power of the each DAB module individually. The SST switching model simulation demonstrates the proposed voltage and power balance controller. The 20kW SST scale-down prototype experiment is implemented and verifies the effectiveness of the proposed voltage controller.

Chapter 4. SST Power Ripple Control

The proposed solid state transformer (SST) is an interface between the single phase high voltage 7.2kV AC and low voltage 120V AC. The SST has three 3.8kV high voltage DC buses and a 400V low voltage DC bus. Unlike the three phase converter system, the DC bus voltage in single phase H-bridge always contains 120Hz low frequency ripple, because the single phase input power itself varies at 120Hz frequency according to the equation (4.1).

$$P = V\sin(2\pi ft) * I\sin(2\pi ft - \phi) \tag{4.1}$$

Where, V and I are the input voltage and current, f=60Hz, and ϕ is the input power factor angle. This requires a much larger capacitance to limit the DC voltage ripples within the allowable range comparing to the three phase system.

A major motivation of this chapter is therefore to develop a feed-forward power synchronization technique to reduce the required DC filter capacitance as well as the 120Hz voltage ripple for high voltage and low voltage DC bus. The references [59][60][61] all focus on the ripple reduction method for the single phase back-to-back system, none of them can be directly applied to the SST. The proposed method in this Chapter is based on the power synchronization of input and output, including the rectifier, dual active bridge (DAB) and the inverter stage.

4.1. SST power flow analysis

Figure 4.1 shows the power flow of each stage in the SST, PA is the power through the rectifier, PB is the power through DAB stage and PC is the power through DC output and inverter stage.

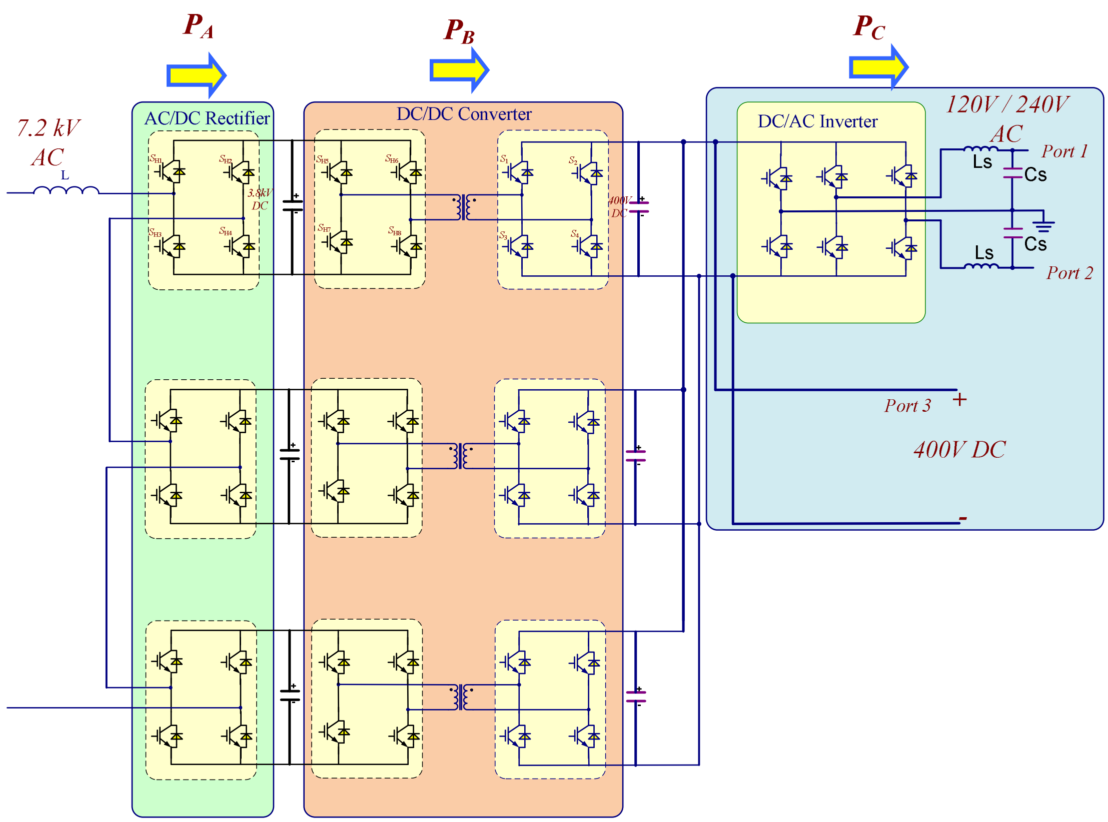


Figure 4.1 Power flow between the SST three stages

Neglecting the converter power losses, the DC link capacitor power can be written as:

$$p_{c1}(t) = p_A - p_B = V_{c1}C_1\frac{dV_{c1}}{dt} = V_{in}\sin(2\pi ft) * I_{in}\sin(2\pi ft - \phi) - p_B \qquad (4.2)$$

$$p_{c2}(t) = p_b - p_c = V_{c2}C_2\frac{dV_{c2}}{dt} \qquad (4.3)$$

Where C_1 is the high voltage capacitor, V_{c1} is the high DC link voltage, C_2 is the low voltage capacitor, V_{c2} is the low DC link voltage, V_{in} and I_{in} are the input voltage and current respectively, and ϕ is the input power factor angle.

The average power P_A, P_B and P_C in a 60Hz cycle are the same at steady state according to capacitor charge balance theory. It is the power ripple differences between P_A, P_B and P_C that determine the voltage ripple and the required capacitance of each DC bus.

Figure 4.2 shows the simulation of the input voltage, input current and rectifier power P_A, DAB power P_B. As the input voltage and current are both 60Hz AC variables, the rectifier power P_A contains 120Hz ripple. By contrast, the DAB power is a DC without much ripple. The mismatch between P_A and P_B results in the capacitor power ripple and 10% voltage ripple of the high voltage DC bus as shown in Figure 4.3.

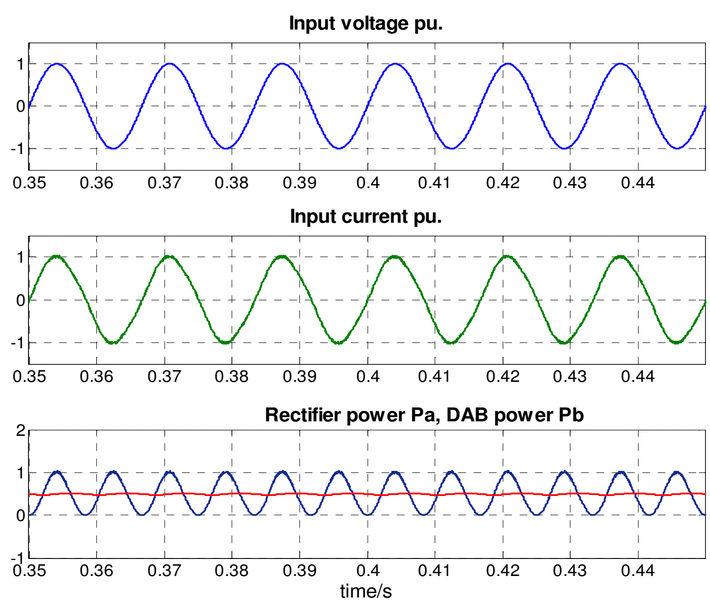


Figure 4.2 SST simulation (input voltage, current and rectifier power P_A, DAB power P_B)

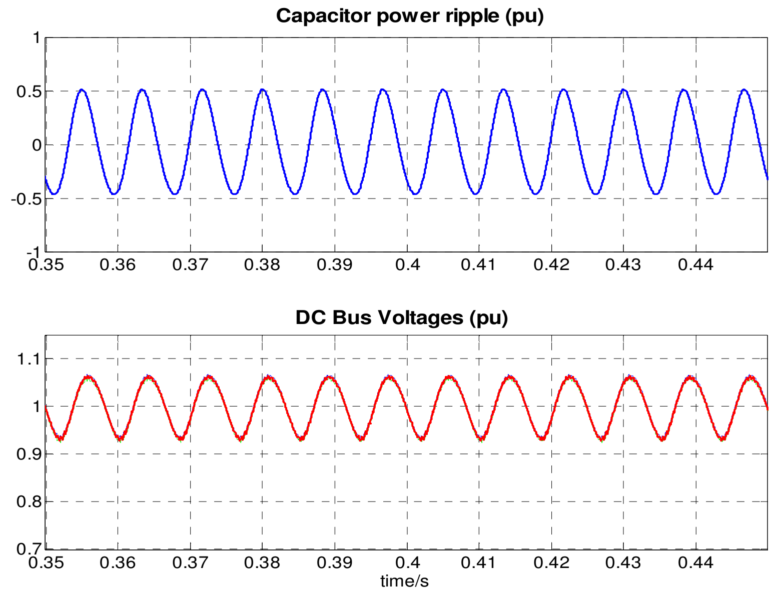


Figure 4.3 SST simulation (capacitor power ripple, DC bus voltages)

4.2. DAB feed-forward power ripple control

The proposed DAB feed-forward power control block is shown in Figure 4.4. The DAB Feed-forward power ripple is calculated as

$$P(t) = V_a I_a - \frac{1}{T}\int_0^T V_a I_a dt, T = 1/60s \quad (4.4)$$

Where, V_a and I_a are the input voltage and the real power current, and ϕ is the input power factor angle. The input voltage and current are already measured for the single phase d-q vector controller, so there is no additional measurement for the power control. The ripple power is calculated in the DSP and added to the DAB power control reference. The voltage regulator in the DAB controller generates the required "DC" reference power, and then the ripple power is added to match the input power ripple. The DAB power control loop is designed with a bandwidth of 300Hz to have a good track of the 120Hz ripple power. The DAB voltage regulator output ripple and the control bandwidth both affect the ripple matching performance. It should also be noticed that the proposed power ripple control is designed to reduce the voltage ripple caused by the real power mismatch between the rectifier and DAB. The reactive power can also be matched, but this will require a higher DAB peak current, so the DC capacitor is still designed based on the voltage ripple caused by the reactive power.

Figure 4.5 shows the DAB average power (averaged in each switch cycle 1000Hz) without feed-forward power control. Figure 4.6 shows the DAB average power with feed-forward power control. Figure 4.7 and Figure 4.8 illustrate the high DC bus voltages without and with feed-forward power control, respectively. The simulations verify that the feed-forward control reduces the voltage ripple from 10% to 2%. In other words, the capacitance can be reduced to 20% to meet the same voltage ripple requirement.

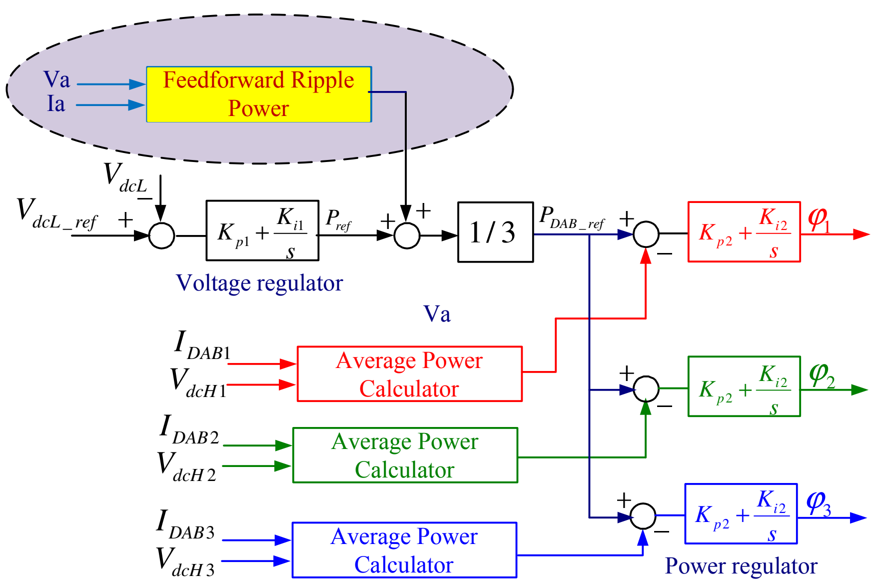


Figure 4.4 Feed-forward ripple power controller

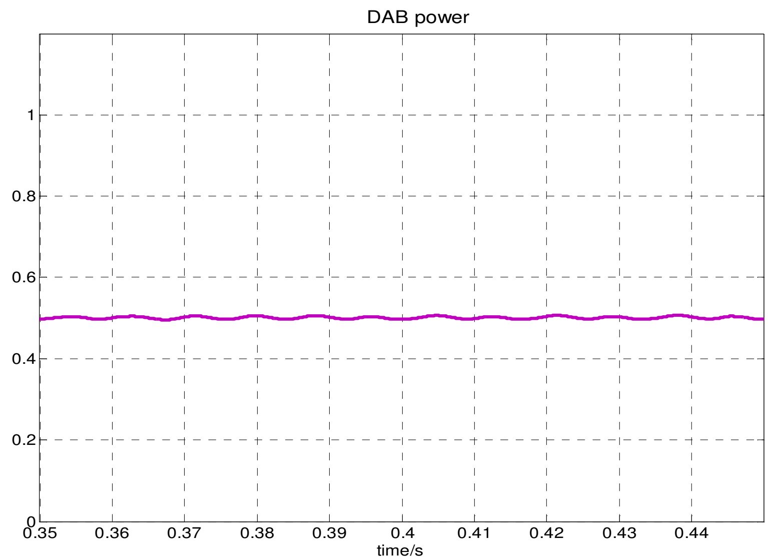


Figure 4.5 DAB average power without feed-forward power control

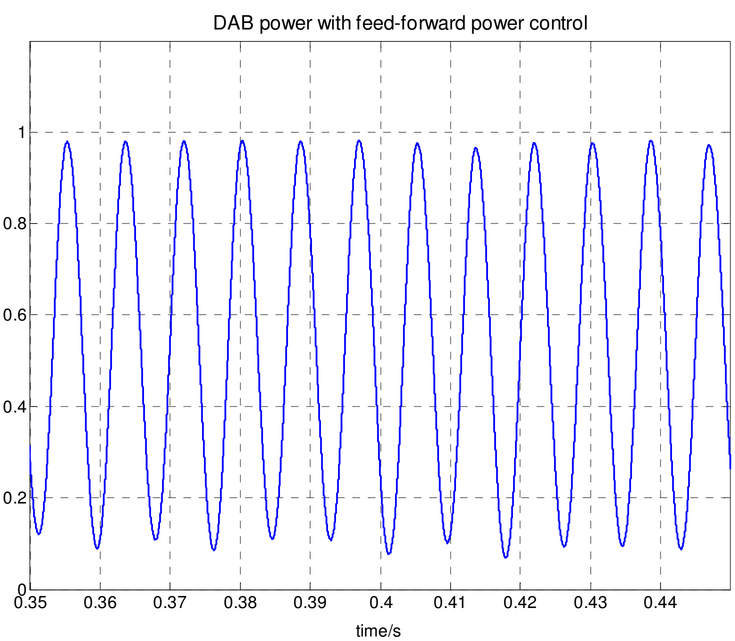


Figure 4.6 DAB average power with feed-forward power control

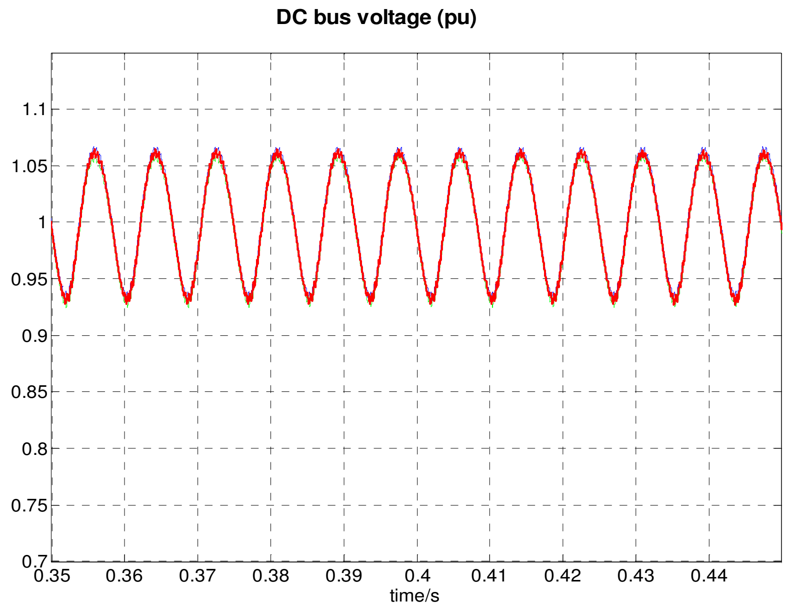


Figure 4.7 High DC bus voltage without feed-forward power control

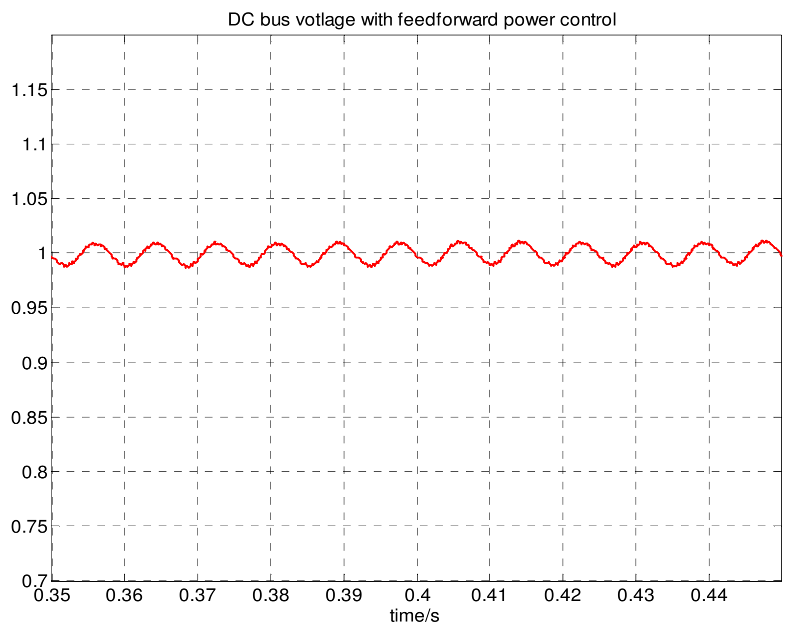


Figure 4.8 High DC bus voltage with feed-forward power control

4.3. Inverter power synchronization control

The 20kVA SST output is designed as an interface between the residential and the distribution system. The residential application has various load types, including linear and nonlinear, reactive power and capacitive power. Without loss of generality, the inverter power synchronization control aims to synchronize the input power with the fundamental component of the output power [59][60][61]. The capacitor still needs to take all the ripple power caused by the harmonic current, but the power synchronization control is able to minimize the ripple power due to the load fundamental current.

In the previous inverter controller, the output 60Hz AC voltage has a random phase angle. The power synchronization control utilizes the output phase angle to synchronize the output fundamental power with the input power. By outputting a proper phase angle, the capacitor voltage ripple can be reduced, therefore the required capacitance can be minimized as well.

In order to calculate the optimum voltage phase angle, first the input and output power are calculated in equation (4.5) and (4.6), respectively.

$$P_1 = V_1 \sin(\omega t) * I_1 \sin(\omega t) = \frac{V_1 I_1}{2}(1 - \cos(2\omega t)) \quad (4.5)$$

$$P_3 = V_3 \sin(\omega t + \beta) * I_3 \sin(\omega t + \beta - \phi) = \frac{V_3 I_3}{2}(\cos(\phi) - \cos(2\omega t + 2\beta - \phi)) \quad (4.6)$$

Where, V_1 and I_1 are the input voltage and the real power current, V_3 and I_3 are the output voltage and the current, β is the angle of the output voltage with respect to the input voltage, ϕ is the lagging angle of the fundamental load current with respect to the output voltage.

In steady state, according to the law of conservation of energy,

$$\int_0^T P_1 dt = \int_0^T P_3 dt \tag{4.7}$$

So the DC component of equation (4.5) and (4.6) are equal. $V_1 I_1 = V_3 I_3 \cos(\varphi)$. The capacitor power ripple can be derived as equation (4.8).

$$P_c = P_1 - P_3 = \frac{V_1 I_1}{2}\cos(2\omega t) - \frac{V_3 I_3}{2}\cos(2\omega t + 2\beta - \phi) \tag{4.8}$$

The equation (4.9) is the ripple energy of the DC capacitor.

$$E_{c2} = \int_0^{T/2} |P_{c2}| = \int_0^{T/2} |P_B - P_c| = \left| \frac{V_1 I_1}{2}\cos(2\omega t) - \frac{V_3 I_3}{2}\cos(2\omega t + 2\beta - \phi) \right| \tag{4.9}$$

The minimum voltage ripple is achieved when the equation (4.9) reaches its minimum at $\beta = \dfrac{\varphi}{2}$.

The inverter power synchronization control is shown in Figure 4.9. First the PLL block calculates the phase angle φ of the fundamental load current. Then the output voltage phase angle is set at $\beta = \dfrac{\varphi}{2}$.

Figure 4.10 and Figure 4.11 show the SST inverter simulation without power synchronization control. Since the output voltage angle is random, it is assumed the input power and output power are out of phase. With the selected capacitance, the voltage ripple is around 10%. Figure 4.12 and Figure 4.13 are the SST inverter simulation using the power synchronization control. By controlling the output voltage angle, the output power is synchronized with the input power, therefore the capacitor power ripple is greatly reduced, and the DC bus voltage ripple is only 2%.

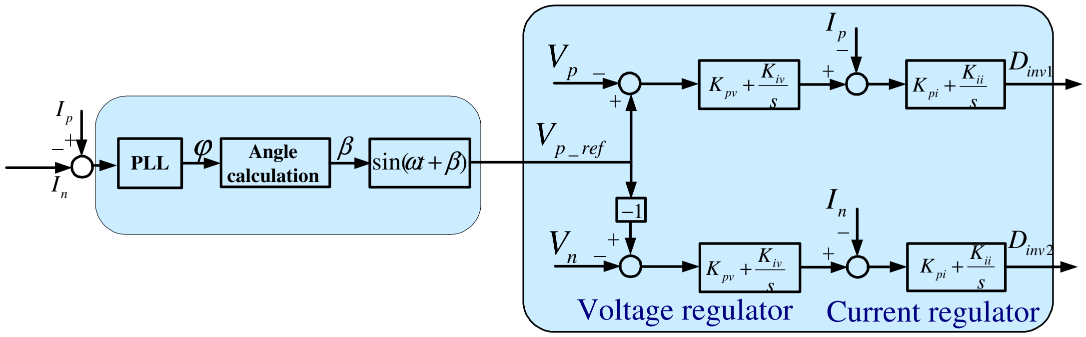


Figure 4.9 SST inverter power synchronization control

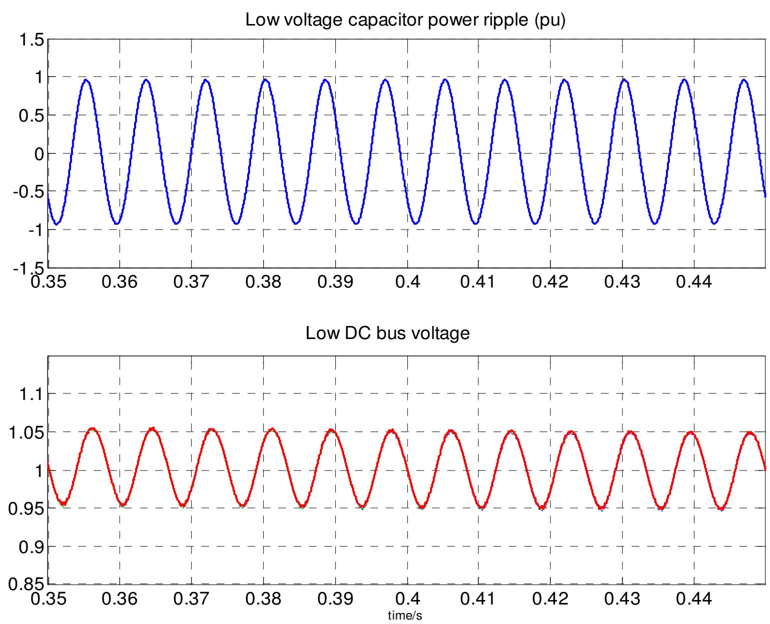


Figure 4.10 SST inverter simulation without power synchronization control

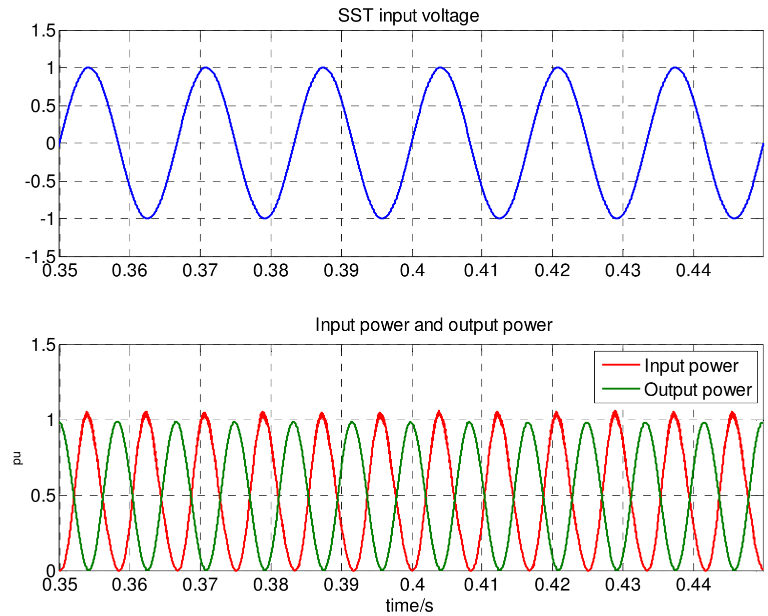


Figure 4.11 SST inverter simulation without power synchronization control

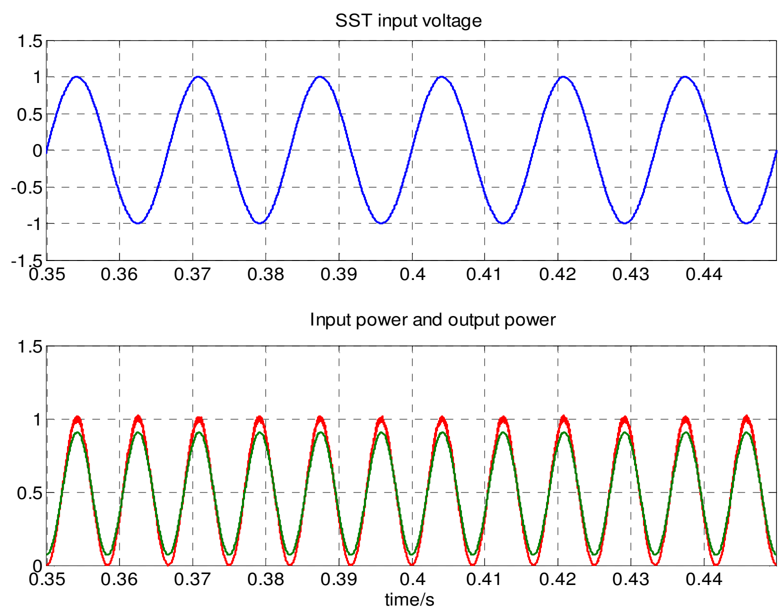


Figure 4.12 SST inverter simulation with power synchronization control

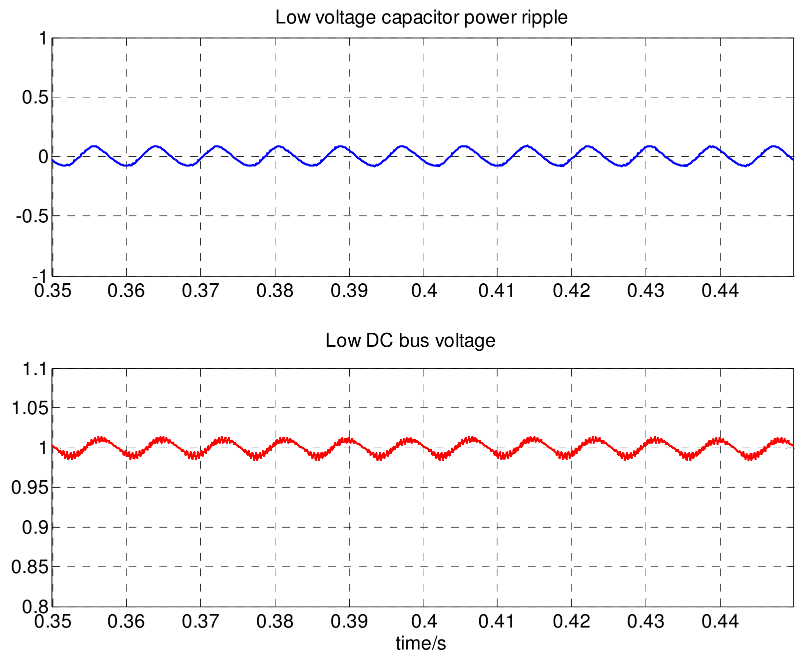


Figure 4.13 SST inverter simulation with power synchronization control

4.4. Summary

In this chapter, the power flow of the SST three stages is analyzed. A feed-forward power ripple control method is proposed for the DAB stage to reduce the high voltage DC bus ripple and the required capacitance. A power synchronization method is designed for the inverter stage to determine the output voltage angle and minimize the voltage ripple for the low voltage DC bus. The proposed methods are based on the power synchronization of input and output, including the rectifier, dual active bridge (DAB) and the inverter stage. The simulation results verify the proposed controller and the required capacitance can be reduced to 20% of the normally designed value.

Chapter 5. SST Hardware Development and Experiments

5.1. SST Rectifier Stage Hardware Design

In order to verify the proposed SST functionalities and the controller scheme, a low voltage solid state transformer prototype is designed. The SST prototype is designed as single phase input voltage 60Hz, 240V, and DC output 400V, AC output 60Hz, 120/240V. The prototype consists of a cascaded H-Bridge AC/DC rectifier that converts 60Hz, 240V AC to 400V DC bus, a DC/DC converter that convert 400V to 400V DC bus with 1:1 high frequency transformer. The SST module output will connect to a DC/AC inverter that converts 400V DC to 120/240V AC.

This chapter focuses on the implementation and experiment of the rectifier stage prototype. The prototype is implemented by using 600V 75A Intelligent Power Modules (IPM) PM75CLA060. The IPM has built-in control circuits which provide optimum gate drive and protection for the IGBT and free-wheel diode. Figure 5.1 and Figure 5.2 are the SST rectifier stage topology and the prototype photo respectively. The system parameters are shown in Table 5.1.

The SST single phase vector control and the voltage balance control are shown in Figure 5.3 and Figure 5.4. The details are presented in Chapter 3. The controller is programmed in floating point DSP TMS320F28335 with a model based program method. The model based programming uses Matlab Target Support Package to deploy code generated from

Matlab/Simulink for real-time execution on microcontrollers and DSPs without writing low-level drivers and run-time code.

The single phase d-q vector control is implemented in the DSP controller by using a model based program. The clock of TMS320F28335 is set to 100MHz, the switching frequency and the ADC sampling rate is 10kHz. The sampled phase *A* voltage is delayed by 1/4 cycle (1/4*10kHz/60Hz sampling points) to synthesize the orthogonal imaginary phase *M* for the single phase *dq* transformation.

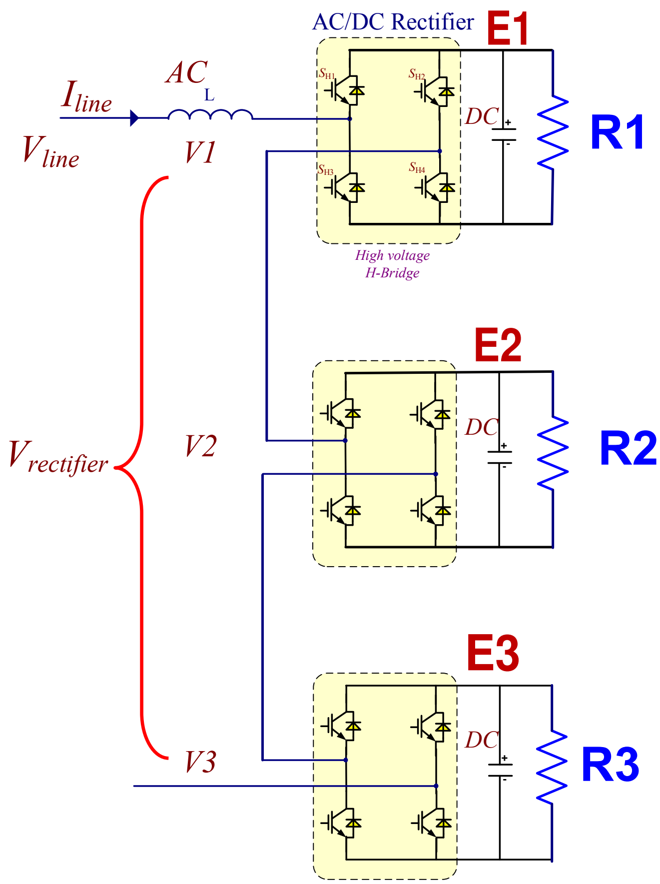


Figure 5.1 SST rectifier stage topology

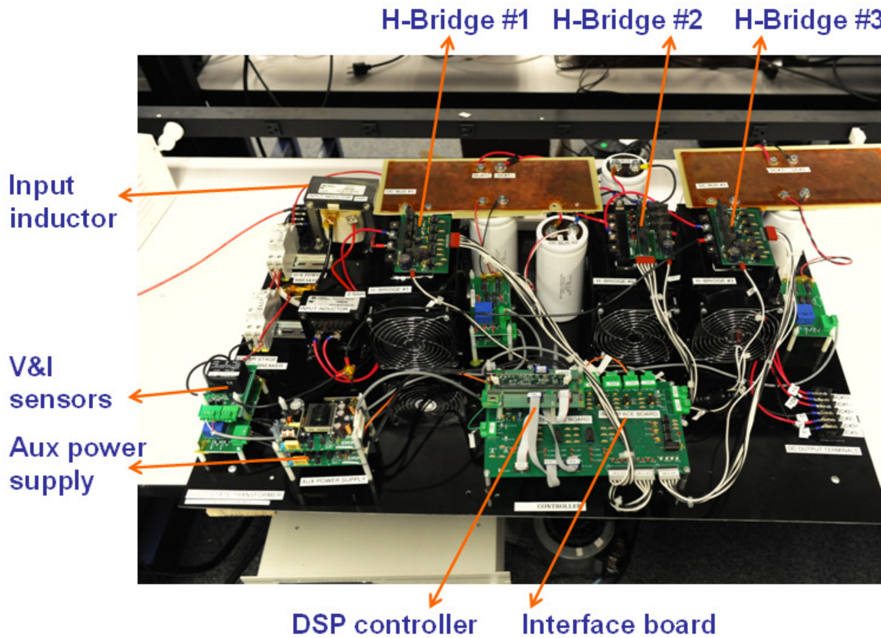


Figure 5.2 SST rectifeir prototype

Table 5.1 SST Prototype Parameters

Input inductance	3.5mH
DC Capacitor	900uF
DC voltage reference	400V
Switching frequency	10kHz
Input AC source	Chroma model 61703 power supply (0-240V)
Intelligent Power Modules (IPM)	PM75CLA060

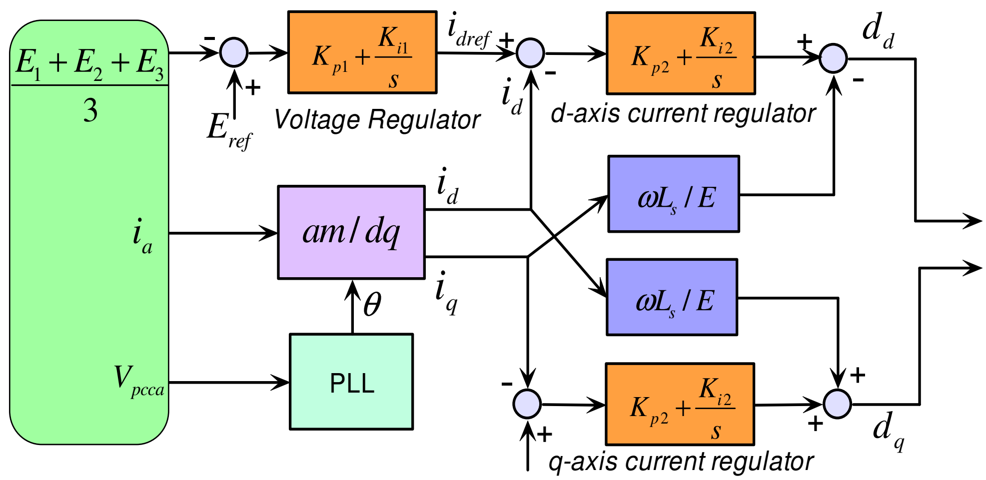


Figure 5.3 Rectifier single phase d-q vector controller

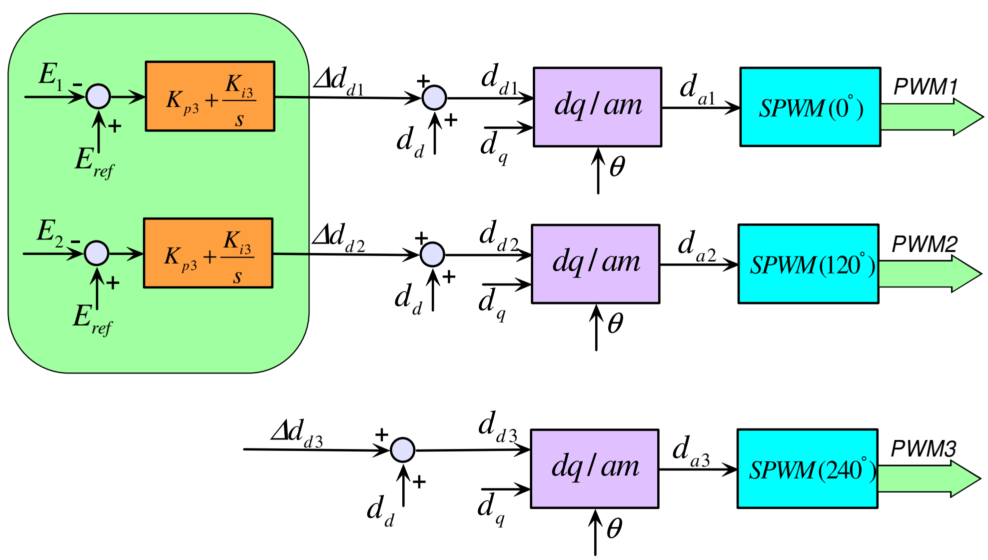


Figure 5.4 Voltage balance control based on single phase d-q vector

5.2. SST Experiments

5.2.1. *Steady state test*

In the steady state test, the DC bus voltage reference is 50V for each H-Bridge and the reactive power reference is zero. The input voltage is 240V 60Hz AC voltage, and the three DC outputs are loaded with resistors $R_1 = R_2 = R_3 = 32\Omega$.

Figure 5.5 illustrates the filtered PLL output angle with respect to the input AC voltage. The PLL output angle (0-2π) is modulated by a 10kHz triangle carrier and output to a DSP I/O. The high frequency I/O output is filtered by a low pass analog filter. The filter bandwidth (2kHz) limits high frequency components of the PLL angle signal and results in a slow decrease from 2π to 0. The recovered phase signal is in phase with the input AC voltage, which ensures the accuracy of the d-q transformation.

Figure 5.6 demonstrates the steady state experiment results of the SST rectifier stage with single phase d-q vector controller. Similar to the simulation, the rectifier generates a 7-level voltage waveform to regulate the DC bus and the input current. The DC bus voltage is regulated to the reference 450V total (150V each) and the input current is in phase with the input voltage. Figure 5.7 is the online total power quality analysis result, which shows the input current harmonics at different harmonic orders. A 99.6% input power factor is achieved and the total current THD is 4.32%. The steady state test verifies the SST features of power factor control and DC bus regulation.

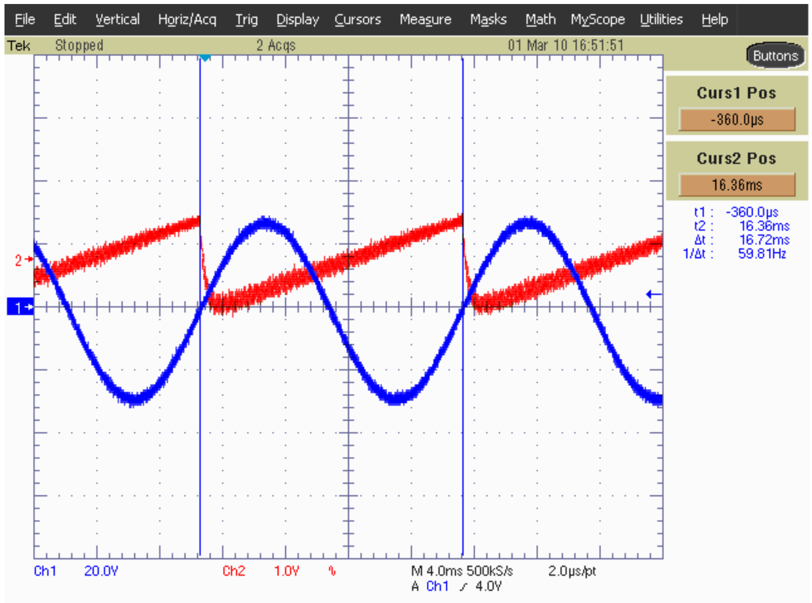


Figure 5.5 PLL test results (Ch1, input AC voltage, 20V/div; Ch2, PLL output angle, 1V/div)

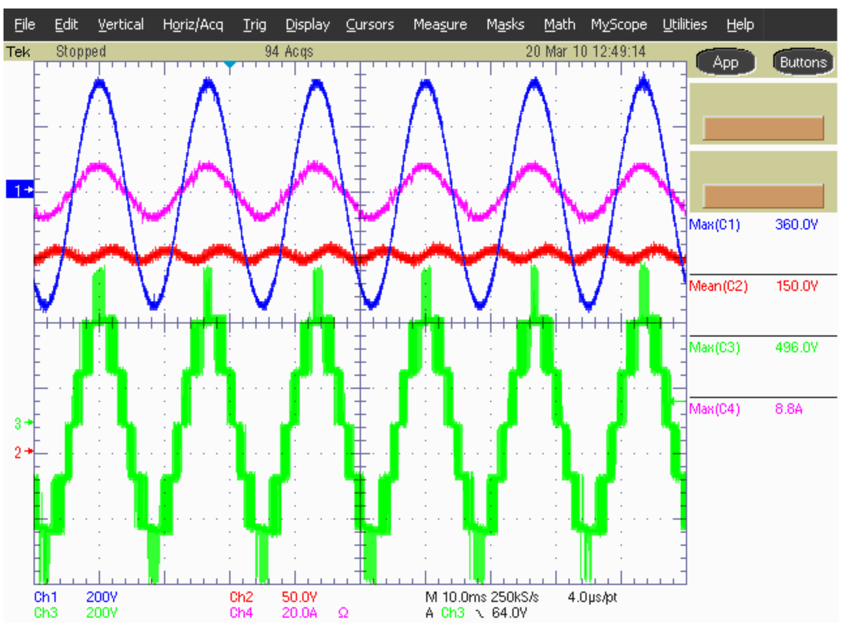


Figure 5.6 Experiment results of SST rectifier stage (Ch1, input AC voltage, 100V/div; Ch2, DC bus voltage of H-Bridge #2, 20V/div; Ch3, rectifier PWM voltage, 100V/div; Ch4, input current, 10A/div)

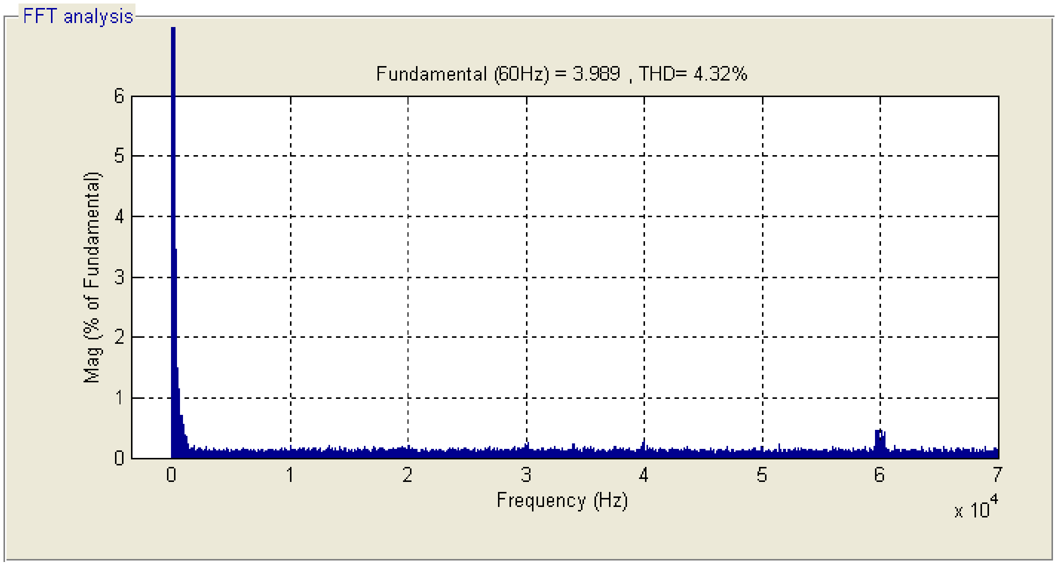


Figure 5.7 Input AC current harmonic analysis

5.2.2. *Reactive power control*

The SST rectifier stage not only converts the input AC to regulated DC voltages, but also has reactive power compensation capabilities. Depending on the reactive power reference in the SST controller, the SST can generate or absorb the rated reactive power to the power grid. This fast and controllable local reactive power compensation is beneficial to support the system voltage, reduce the transmission line loss and enhance the power system stability. The reactive power control is verified in two cases. In the two cases, the SST operates in reactive and capacitive mode, respectively.

1) Test condition 1: total DC bus reference $E=150V$, reactive power reference i_q = -0.2pu (reactive mode, $I_{base}=10A$). Resistor load $R_1=R_2= R_3=32\Omega$.

As shown in Figure 5.8, the input current is lagging the input voltage, so the SST is absorbing reactive power from the input AC. This is useful when the power system has more capacitive power loads, for example the transmission line light load condition. The SST will absorb reactive power to reduce the transmission line voltage swell due to the capacitive load.

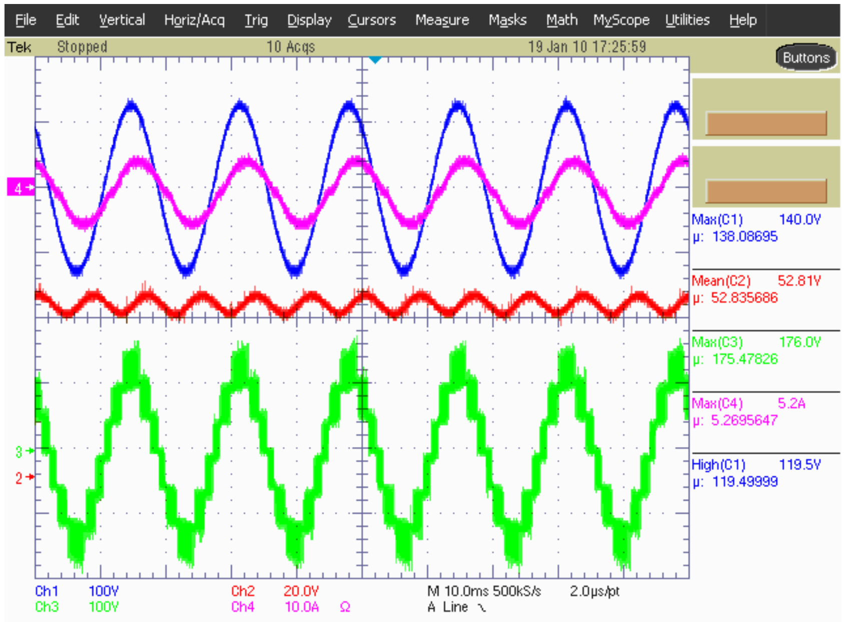


Figure 5.8 SST reactive mode (Ch1, input AC voltage, 100V/div; Ch2, DC bus voltage, 20V/div; Ch3, rectifier PWM voltage, 100V/div; Ch4, input current, 10A/div)

2) Test condition 2: Total DC bus reference E=150V, reactive power reference iq = 0.2pu (capacitive mode, Ibase=10A). Resistor load R1=R2=R3=32Ω.

As shown in Figure 5.9, the input current is leading the input voltage, so the SST is generating reactive power to the input. These two experiments verify the SST reactive power compensations. The reactive power reference can be generated by the higher level smart grid system and downloaded to the SST DSP controller.

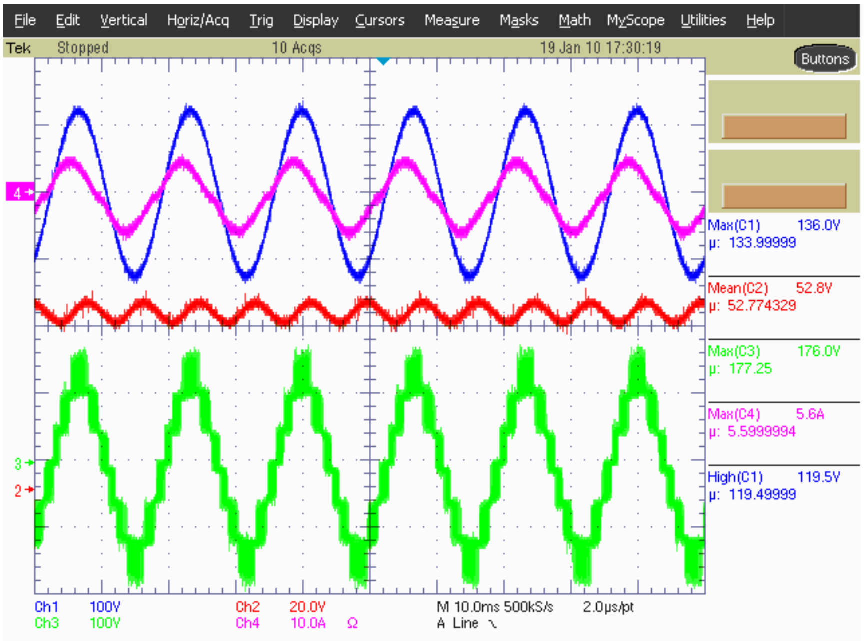


Figure 5.9 SST capacitive mode (Ch1, input AC voltage, 100V/div; Ch2, DC bus voltage, 20V/div; Ch3, rectifier PWM voltage, 100V/div; Ch4, input current, 10A/div)

5.2.3. *Load unbalance and dynamic load change test*

One of the main disadvantages of the cascaded H-bridge converter is the voltage unbalance that could appear on the DC side of different H-bridges due to the device loss mismatching and H-Bridge real power differences. The unbalanced voltage will cause the capacitor or device over-voltage in the H-Bridge and trigger the system over-voltage protection. Therefore, a novel voltage control strategy is proposed to balance the rectifier capacitor voltages in Chapter 3. The load unbalance test is to create a load unbalance condition and find out the existing voltage unbalance problem. The dynamic load change test is to verify the performance of the proposed unbalance controller.

The load unbalance test conditions are: total DC bus reference $E=150V$, reactive power reference $i_q=0$. The load resistors are different. Resistor load $R_1=R_2=32\Omega$; $R_3=26\Omega$. (20% load power unbalance).

Figure 5.10 shows three steady state DC bus voltages without voltage balance control. The average DC bus voltages are 56V, 56V and 43V respectively (25%.voltage unbalance). The H-Bridge with the larger load resister has a higher DC bus voltage. The DC bus is unbalanced due to the load unbalance. Figure 5.11 shows three steady state DC bus voltages with voltage balance control. The DC bus voltages are equally distributed regardless of the unbalance load.

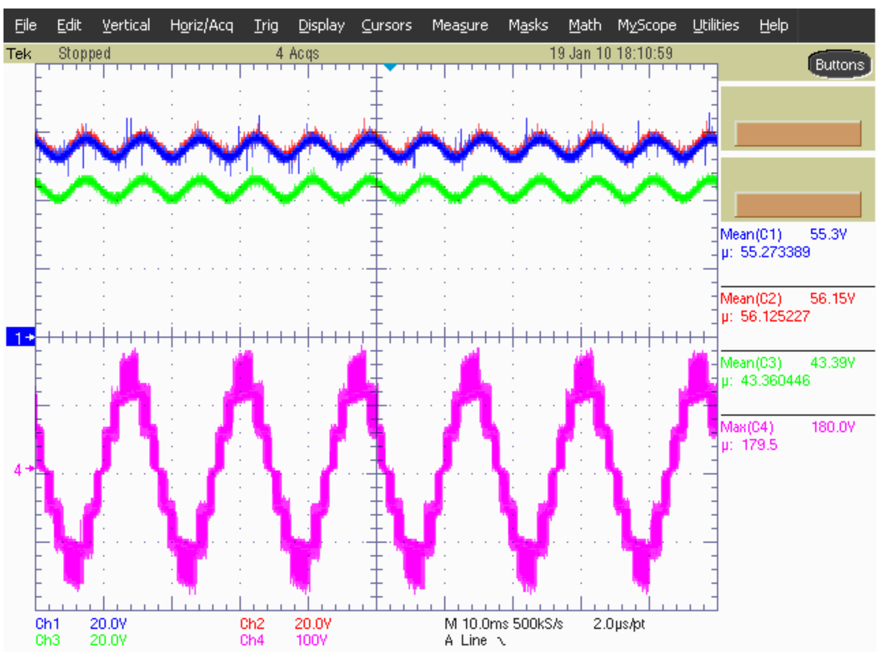


Figure 5.10 H-Bridge DC bus voltages (Ch1, DC bus voltage of H-Bridge #1, 20V /div; Ch2, DC bus voltage of H-Bridge #2, 20V /div; Ch3, 20V /div; DC bus voltage of H-Bridge #3, 20V /div; Ch4, rectifier PWM voltage, 100V/div)

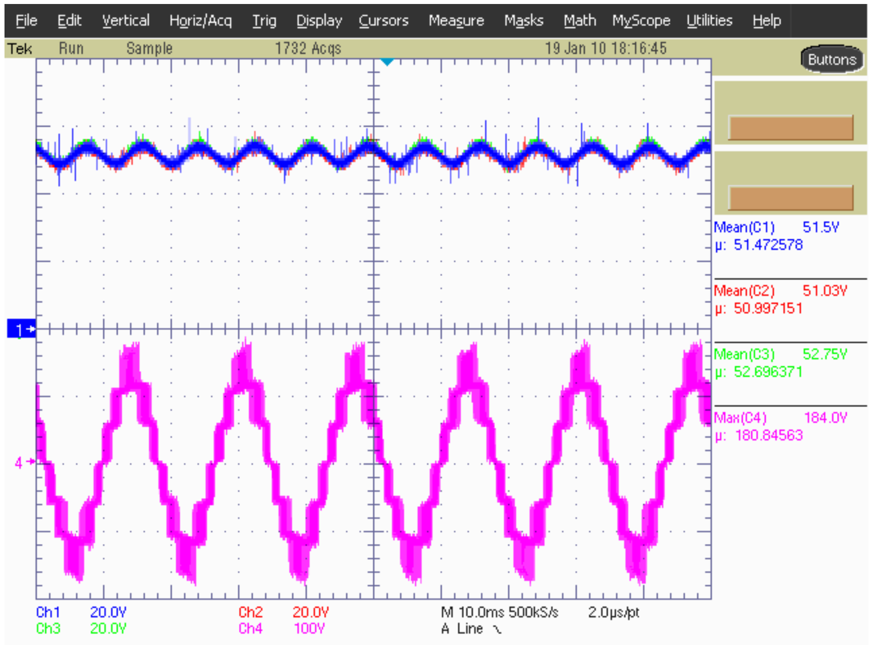


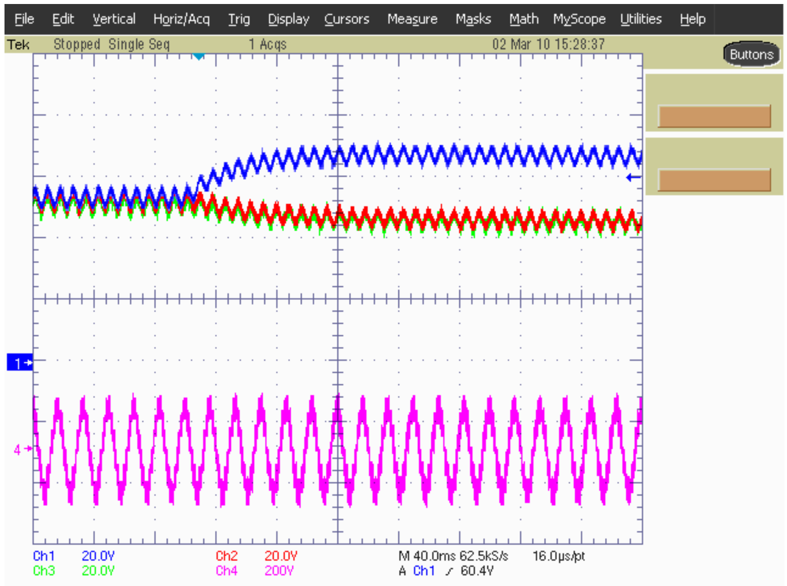
Figure 5.11 H-Bridge DC bus voltages (Ch1, DC bus voltage of H-Bridge #1, 20V/div; Ch2, DC bus voltage of H-Bridge #2; Ch3, 20V /div; DC bus voltage of H-Bridge #3, 20V /div; Ch4, rectifier PWM voltage, 100V/div)

In the dynamic load test, the load resistors connected to the DC bus are dynamically changed to create the real power differences. The load resistor R_3 has a step increase from 32Ω to 46Ω (80% load decrease) in the first test and a step decrease from 32Ω to 20Ω (80% load increase) in the second test. R_1 and R_2 are maintained as 32Ω all the time.

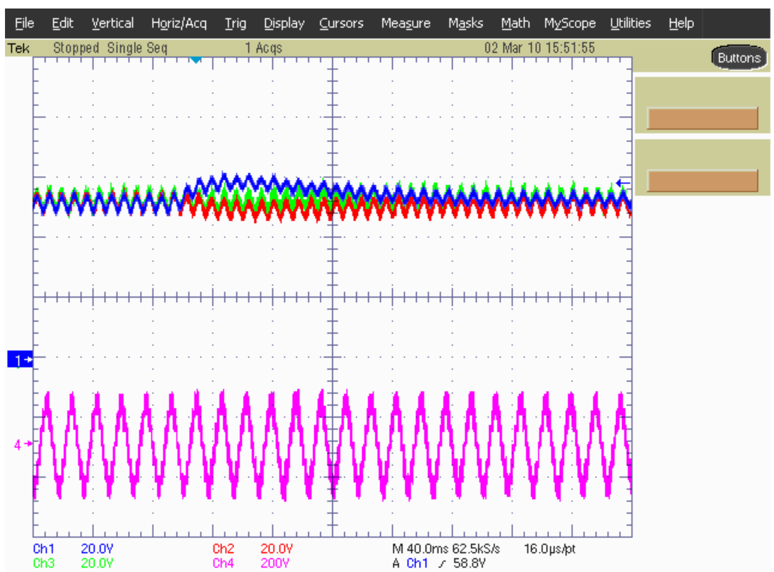
Figure 5.12 shows the test results with R_3 step change from 32Ω to 46Ω. Figure 5.12 (a) shows three DC bus voltages without the voltage balance control. The three DC bus voltages are all regulated at 50V when the loads are the same. However after the load step change, the DC bus voltages become 56V, 56V and 43V (25%.voltage unbalance) respectively. The H-Bridge with the larger load resister has a higher DC bus voltage. Figure 5.12 (b) shows the three DC bus voltages with the voltage balance control. The balance controller regulates the

DC bus voltage when the load change occurs. The DC bus voltages have a transit time of about 4 cycles, then settle down to the same voltage. Similarly, Figure 5.13 demonstrates the DC bus voltages at 80% load increase. The experiment verifies the effectiveness of the voltage balance controller.

1) Dynamic load test condition 1: total DC bus reference E=150V, reactive power reference i_q=0, resistor load R_1 =R_2=32Ω; R_3 step change from 32Ω -46Ω.
2) Dynamic load test condition 2: total DC bus reference E=150V, reactive power reference i_q=0, resistor load R_1 =R_2=32Ω; R_3 step change from 32Ω-20Ω.

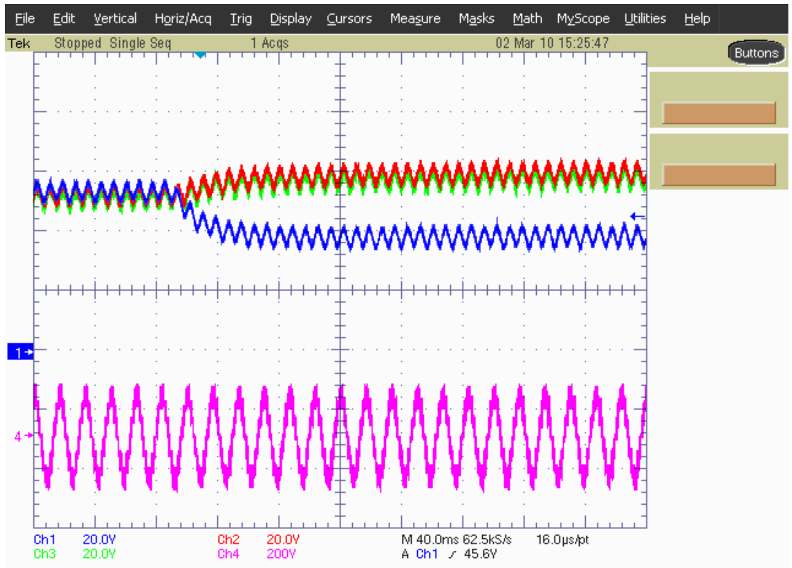


(a) Without Voltage balance control

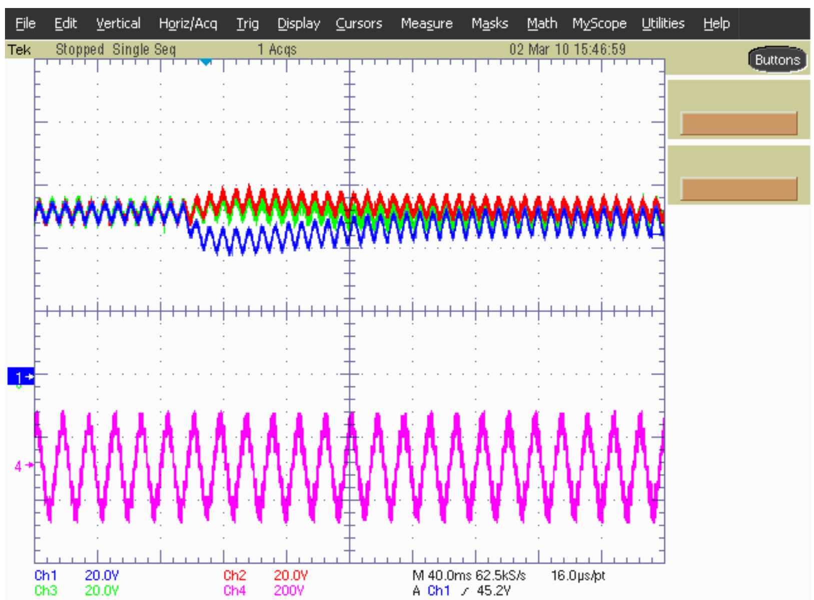


(b) With voltage balance control

Figure 5.12 H-Bridge DC bus voltages, R_3 step change from 32Ω -46Ω (Ch1, DC bus voltage of H-Bridge #3, 20V/div; Ch2, DC bus voltage of H-Bridge #1; Ch3, 20V/div; DC bus voltage of H-Bridge #2, 20V/div; Ch4, rectifier PWM voltage, 200V/div)



(a) Without Voltage balance control



(b) With voltage balance control

Figure 5.13 H-Bridge DC bus voltages, R_3 step change from 32Ω -20Ω (Ch1, DC bus voltage of H-Bridge #3, 20V/div; Ch2, DC bus voltage of H-Bridge #1; Ch3, 20V/div; DC bus voltage of H-Bridge #2, 20V/div; Ch4, rectifier PWM voltage, 200V/div)

5.2.4. *Power unbalance limit*

Due to the intrinsic constraints of the cascaded H-Bridge circuit, the real power unbalance range of the H-Bridges is limited in order to maintain the DC bus balanced. This limitation is determined by the input AC voltage, DC bus voltage reference and the input inductance as derived in equation (3.16) in Chapter 3.

$$\frac{P_1}{P_{in}} \leq \frac{E}{V_{line}}\sqrt{1-(\frac{\omega L I_{line}}{3E})^2} \tag{5.1}$$

In the prototype, $E=50V$, $V_{line}=125V$, $L=3.5mH$, $I_{line}=8A$. By solving the equation (3. 16), the maximum power unbalance happens when the load resistor R_3 is 65Ω and $R_1=R_2=32\Omega$. Figure 5.14 shows the DC bus voltages when R_3 step increases from 32Ω to 65Ω. The load power does not meet the unbalance equation (5.1), the DC bus voltage will inevitably become unbalanced. The experiment results verify the unbalance limit analysis of the cascaded rectifier.

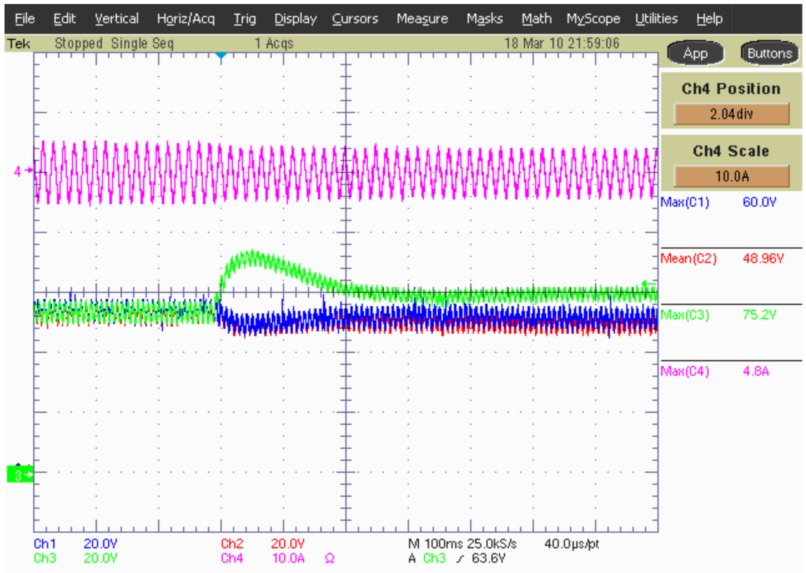


Figure 5.14 H-Bridge DC bus voltages, R_3 step increases from 32Ω to 65Ω (Ch1, DC bus voltage of H-Bridge #1, 20V/div; Ch2, DC bus voltage of H-Bridge #2; Ch3, DC bus voltage of H-Bridge #3, 20V/div; Ch4, rectifier PWM voltage, 200V/div)

5.2.5. *Input voltage sag and swell*

One of the most important features of the SST is the voltage sag or swell ride through capability. The voltage sag or swell can be compensated by the rectifier stage and will not affect the load side voltage. The maximum input current determines how much of a voltage sag the SST can compensate, and the maximum input voltage determines how much a voltage swell the SST can support. Furthermore, when the voltage sag is so large that the SST cannot continuously sustain the compensation, the DC bus capacitance (or energy storage) will determine how many cycles the SST can compensate before the system shut down.

The voltage sag and swell test is implemented to verify the designed SST rectifier controller and analyze the sag and swell compensation capability.

1) Voltage swell test condition: Total DC bus reference E=150V, reactive power reference i_q=0. Resistor load R_1= R_2= R_3=32Ω; The input voltage increases from 105V to 135V. (30% voltage swell)

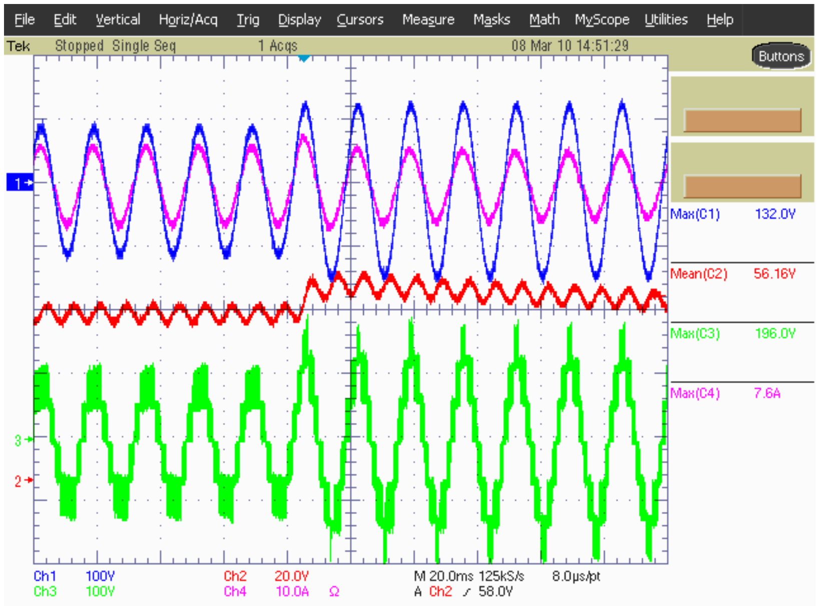


Figure 5.15 Voltage swell test (Ch1, input AC voltage, 100V/div; Ch2, DC bus voltage of H-Bridge #2, 20V/div; Ch3, rectifier PWM voltage, 100V/div; Ch4, input current, 10A/div)

As shown in Figure 5.15, the input AC voltage increases from 105V to 132V, the input current drops when voltage increases because the SST rectifier closed-loop control tries to put the same amount of power into the DC bus. The DC bus voltage has a maximum overshoot 8V (16% of the normal voltage) and takes about 6 cycles transient time to recover back to normal.

2) Voltage sag test condition: Total DC bus reference $E=150V$, reactive power reference i_q=0. Resistor load R_1= R_2= R_3=32Ω; The input voltage decreases from 135V to 105V. (23% voltage sag)

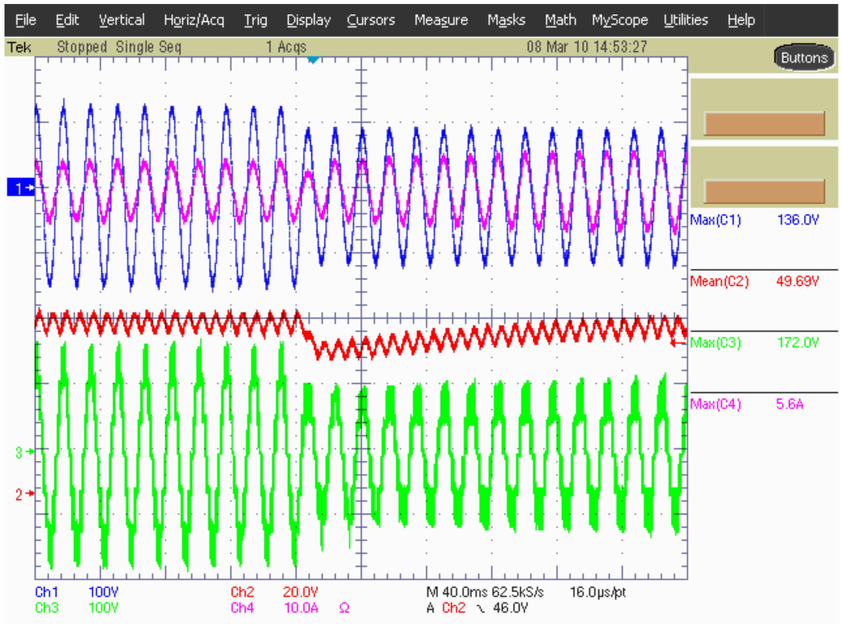


Figure 5.16 Voltage sag test (Ch1, input AC voltage, 100V/div; Ch2, DC bus voltage of H-Bridge #2, 20V/div; Ch3, rectifier PWM voltage, 100V/div; Ch4, input current, 10A/div)

As shown in Figure 5.16, the input AC voltage has a 23% voltage sag from 135V to 105V, the input current increases to maintain the same input power. The DC bus voltage decreases when the voltage sag happens, and then recovers back to normal. The overshoot voltage of the DC bus voltage is 9V (14% of the normal voltage) and the transient time is 8 cycles. The overshoot voltage and the transient time are related to the voltage loop controller design. In the experiment, the voltage control loop bandwidth is 10Hz (limited by the 60Hz low pass filter), so a faster voltage loop will result in a shorter transient time. The experiment results verify the controller design and the voltage sag and swell compensation of the SST.

5.2.6. *Operation state machine*

The rectifier operation state machine is an indispensable operation sequence for a real SST implementation. The sate machine is designed to determine the state change between the start up, steady state operation and system shut down.

As shown in Figure 5.17, the rectifier state machine includes four operation modes.

1) Diode charge mode. The DSP controller starts and sends "off" commands to all the IGBT devices. The rectifier is working as a diode rectifier and charges the DC bus voltage to the peak input AC voltage.
2) Soft start mode. The controller detects that the DC bus voltage reaches a point higher than the minimum start up voltage and sustains it for 100ms. The voltage reference is ramped up to the rated DC bus value in 400ms and the DSP controller starts sending out PWM signals. The DC bus voltage is controlled to increase gradually to avoid a start up overcurrent.
3) PWM boost mode. The DC bus voltage reference reaches its rated value. The rectifier enters a normal operation mode.
4) Protection mode. The protection mode is triggered when there is an input over voltage, input over current, DC bus under voltage, DC bus overvalue or system over temperature. The DSP controller blocks all the PWM and turns off all the IGBTs, so the rectifier goes back to diode charge mode. Additional contactors may be required to fully disconnect the SST from the power system.

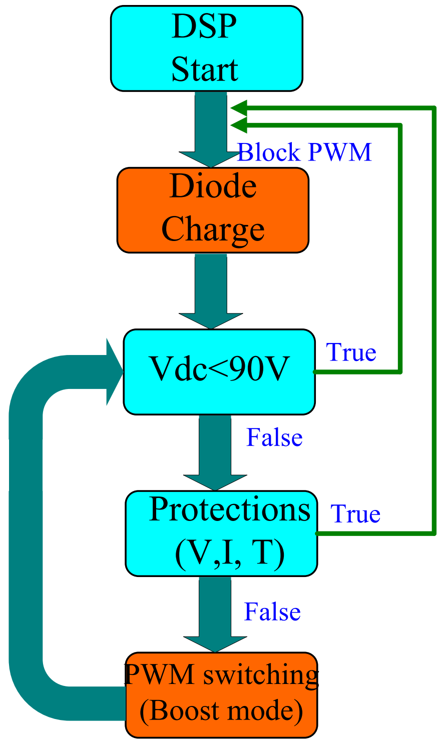


Figure 5.17 SST Rectifier state machine block

The conditions of the rectifier state machine tests are: total DC bus reference E=150V, reactive power reference i_q=0; resistor load R_1=R_2=R_3=32Ω, input voltage step change from 0 to 240V; diode charge time 100ms, then the DC bus voltage is ramped to the reference (soft start) in 400ms, after that the rectifier works in PWM boost mode. The operation sequence waveform is shown in Figure 5.18.

First the DSP starts and enters the diode charge to a stable DC voltage. Figure 5.19 shows a zoom-in waveform of the diode charge mode. After 100ms when the DC bus voltage Vdc>90V, the rectifier enters soft start mode and the DSP starts the PWM gating signals to ramp up the DC voltage. Figure 5.20 shows a zoom in waveform of the transition from diode charge mode to soft start mode. Then after 400ms, the DC bus voltage is boosted up to the rated reference value 150V, the rectifier enters normal operation, PWM boost mode. When Vdc<90V or any voltage, current or temperature protection happens, the DSP blocks all the PWM signals and the system goes back to diode charge mode. Figure 5.21 shows a zoom in waveform of transition from the PWM boost mode to protection mode.

The start up current is limited due to the controller soft start scheme; however the diode charge inrush current still needs careful analysis. The diode charge inrush current cannot be reduced by the controller and is determined by the input voltage, input inductor and DC capacitor. Therefore an additional current limiter may be required to reduce the inrush current to an allowable level.

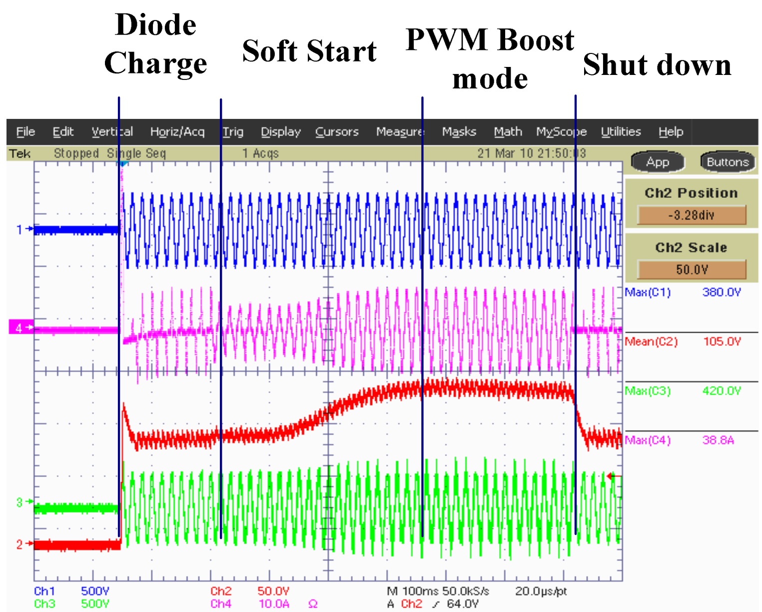


Figure 5.18 Rectifier operation state machine test (Ch1, input AC voltage, 100V/div; Ch2, DC bus voltage of H-Bridge #2, 20V/div; Ch3, rectifier PWM voltage, 200V/div; Ch4, input current, 10A/div)

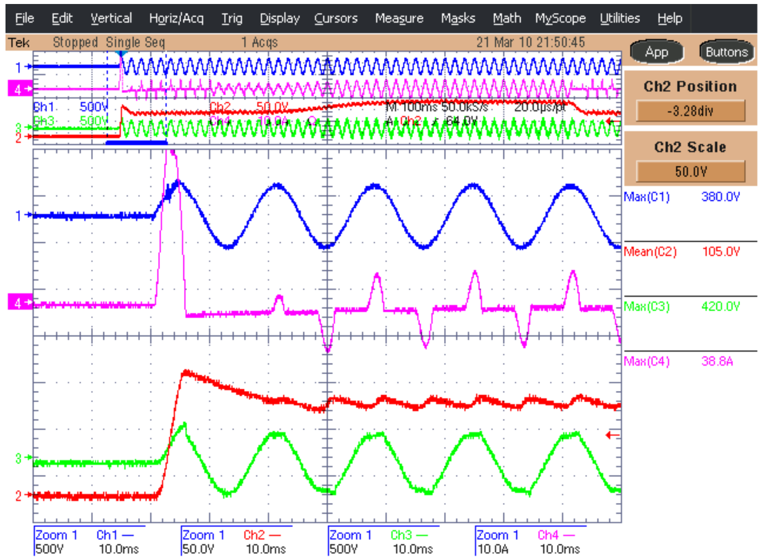


Figure 5.19 Rectifier state machine test: diode charge starts
(Ch1, input AC voltage, 100V/div; Ch2, DC bus voltage of H-Bridge #2, 20V/div; Ch3, rectifier PWM voltage, 200V/div; Ch4, input current, 10A/div)

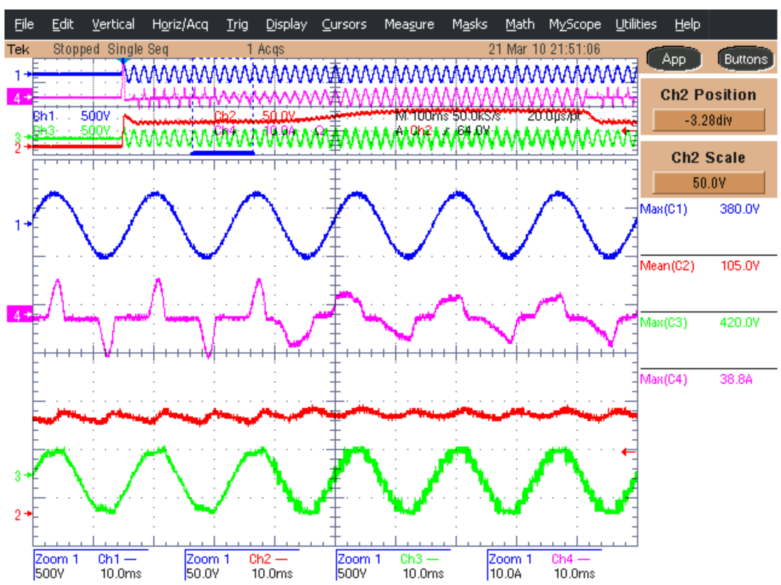


Figure 5.20 Rectifier state machine test: diode charge mode to soft start mode
(Ch1, input AC voltage, 100V/div; Ch2, DC bus voltage of H-Bridge #2, 20V/div; Ch3, rectifier PWM voltage, 200V/div; Ch4, input current, 10A/div)

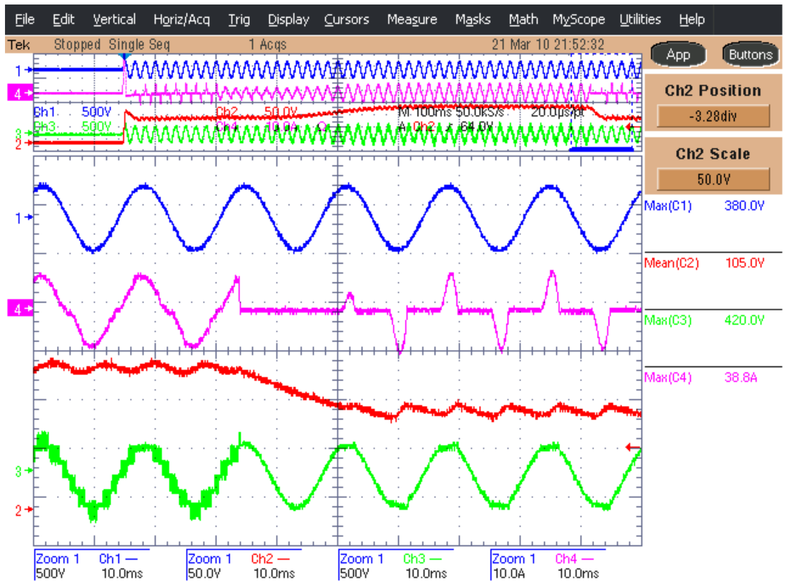


Figure 5.21 Rectifier state machine test: PWM boost mode to protection mode (Ch1, input AC voltage, 100V/div; Ch2, DC bus voltage of H-Bridge #2, 20V/div; Ch3, rectifier PWM voltage, 200V/div; Ch4, input current, 10A/div)

5.2.7. *Voltage loop notch filter*

The input power of a single phase rectifier inevitably contains a second harmonic, this results in a second harmonic ripple on the DC bus voltage. Since the voltage controller generates the d-axis reference current, a second harmonic in the voltage will result in a third harmonic component in the AC current reference. Therefore, a low pass filter in the voltage control loop is necessary to eliminate the second order harmonics and avoid the third harmonic in the AC current. However, the low pass filter not only filters out the second harmonic but also slows the dynamic response of the rectifier controller [62].

In order to solve the above problem, a notch filter is proposed in this section. Comparative studies between the low-pass filter and notch filter are implemented experimentally. The notch filter can alleviate the second harmonic signal in the DC voltage signal remarkably, so it will depress the third harmonic component in the AC current reference, and it will maintain the AC side input current of the PWM rectifier with less harmonic and higher power factor. Because the notch filter doesn't affect other band signals; it will accelerate the dynamic response of the whole system.

Figure 5.23 show the dynamic load change test with the low pass filter and notch filter, respectively. The test conditions are: total DC bus reference *E=150V*, reactive power reference i_q=0, resistor load $R_1=R_2=32\Omega$; R_3 step change from 32Ω-46Ω (80% power decrease).

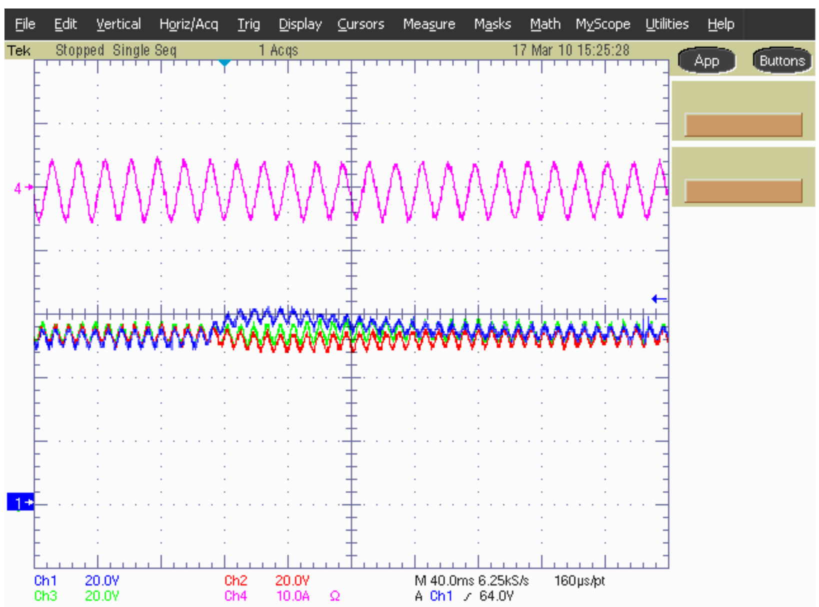


Figure 5.22 H-Bridge DC bus voltages, voltage controller with low pass filter, R_3 step change from 32Ω to 46Ω (Ch1, DC bus voltage of H-Bridge #3, 20V/div; Ch2, DC bus voltage of H-Bridge #1; Ch3, 20V/div; DC bus voltage of H-Bridge #2, 20V/div; Ch4, rectifier PWM voltage, 200V/div)

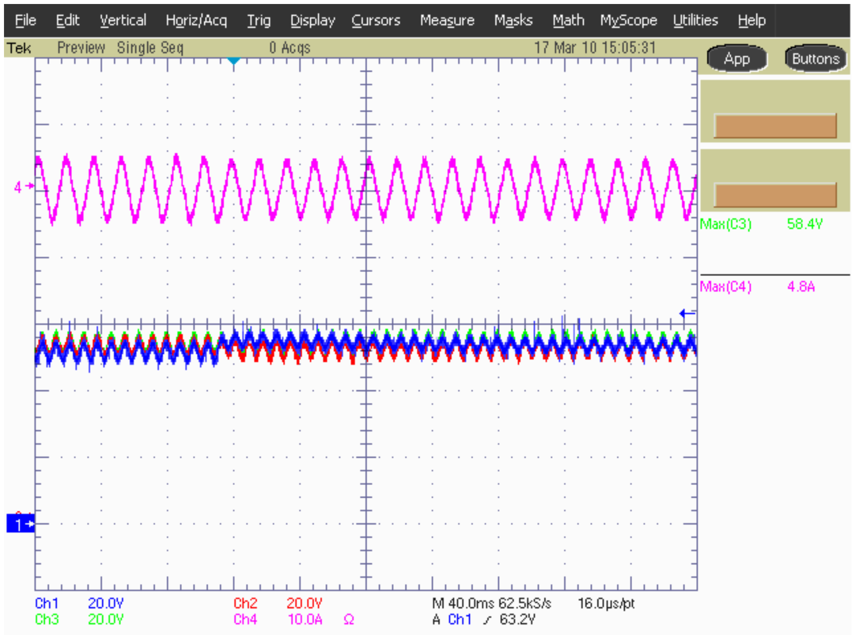


Figure 5.23 H-Bridge DC bus voltages, voltage controller with 120Hz notch filter, R_3 step change from 32Ω to 46Ω (Ch1, DC bus voltage of H-Bridge #3, 20V/div; Ch2, DC bus voltage of H-Bridge #1; Ch3, 20V/div; DC bus voltage of H-Bridge #2, 20V/div; Ch4, rectifier PWM voltage, 200V/div)

Comparing to Figure 5.22, the DC bus voltage in Figure 5.23 has less overshoot and recovers faster. The experiment verifies that the notch filter is effective in accelerating the dynamic response of the rectifier system.

5.3. Summary

In this Chapter, a 20kW cascaded H-Bridge rectifier of the solid state transformer is implemented with 600V IPMs. The single phase d-q vector control and voltage balance controller presented in Chapter 3 are programmed in DSP TMS320F28335. The detailed hardware design and the model based controller are presented in detail. The steady state performance, reactive power control, load unbalance and dynamic load change, power unbalance limit are all verified by the experiments. Moreover, the input voltage sag and swell test illustrates the voltage sag compensation capability. Then the rectifier operation state machine, including an analysis of the diode charge and the soft startup is designed and verified by experiments. Finally, a voltage loop notch filter is designed to improve the dynamic response of the rectifier voltage loop. The experiments verify the performance of the designed controller.

Chapter 6. Higher Voltage and Higher Rating Substation Solid State Transformer (SST) based on 10 kV SiC Power Devices

In the previous chapters, a distribution level solid state transformer based on the silicon devices is proposed and investigated. In Chapter 6, a higher power rating and higher voltage substation solid state transformer is designed based on the 10kV SiC power devices.

The main purpose of substation solid state transformer is to convert AC to AC for step-up or step-down with a function same as a conventional substation transformer. The substation solid-state transformer consists of an AC/DC rectifier, a DC/DC converter, a high frequency transformer and a DC/AC inverter [63]. The traditional 60 Hz transformer is replaced by a high frequency transformer plus solid state devices, which is the key to achieve size and weight reduction.

The substation solid state transformer has several advantages over traditional substation transformers. Unlike the conventional 60Hz transformer, whose power factor depends on the load, the AC/DC rectifier stage of SST acts as a front-end power factor correction device, which enables the unity power factor for the power grid. Besides, the substation SST is not susceptible to voltage sag or swell in the power system because there is a DC link between the AC/DC rectifier and DC/AC inverter. The DC bus voltage can be kept almost constant regardless of system voltage change. Furthermore, due to the energy stored in the DC link capacitors, the SST is capable of sustaining the output power for a few cycles even in the case of power outage. Meanwhile, the SST automatically operates like a circuit breaker or current limiter because it can limit the current through proper control of the DC/AC converter, or it can trip based on standard I^2t curve if the DC/AC converter is designed with proper capacity. These advantages are much less understood by the electric power companies hence significant research is needed to demonstrate these capability and advantages at a meaningful power level.

The basic configuration of a proposed 270 kVA substation SST is shown in Figure 6.1, which consists of a high voltage high frequency AC/DC rectifier that converts 60Hz, 13.8 kV AC to 24 kV DC bus, a high voltage high frequency DC-DC converter that converts 24 kV to 750V DC bus and a voltage source inverter (VSI) that inverts 750V DC to 60 Hz, 480V AC. The 270 kVA substation SST unit is envisioned as a building block for construction a much larger 2.7 MVA SST.

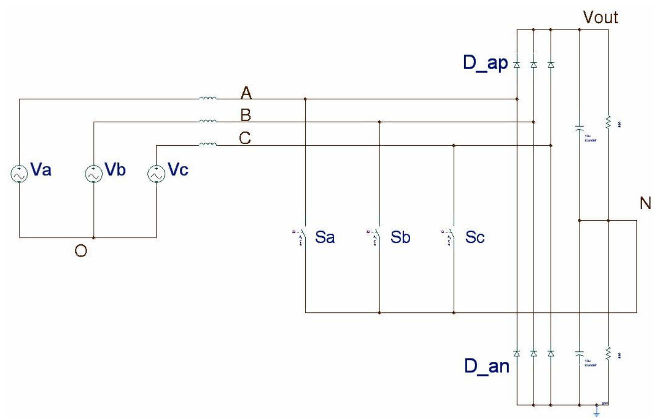
In this chapter, simulation study of the rectifier and the DC/DC converter are performed to demonstrate the functionality and feasibility of the substation SST. In order to realize the high frequency rectifier and DC/DC converter with bus voltage as high as 24 kV, high voltage power devices with low conduction and switching losses are needed. 10 kV SiC MOSFET and PIN or JBS diodes are currently being developed by a number of organizations [21][22][26]. Based on the device characteristics obtained from physics model simulation, the conduction losses and switching losses are analyzed for the devices of the rectifier and the DC-DC converter as well. A Zero Voltage Switching (ZVS) five-level DC/DC converter is proposed to eliminate the MOSFET turn-on loss. The circuit simulation in Saber verifies the working principle and the performance of the proposed ZVS operation. The closed loop controller of the substation solid state transformer system is designed. Simulation results verify the control scheme and the functionalities of the SST.

Figure 6.1 Basic configuration of substation solid state transformer

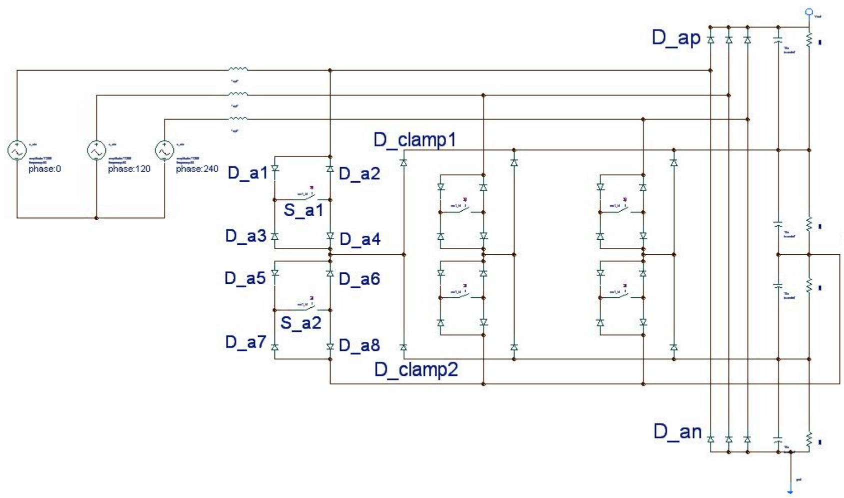
6.1. Simulation and loss analysis of rectifier

One of the significant superiorities of the substation SST over traditional transformers is that the power factor is no longer dependent on the load characteristic but can be maintained at unity power factor. The rectifier converts the three-phase AC voltage into a DC output while maintaining good power factor at the input side.

The Vienna rectifier has been proposed in references [64][65]. The circuit diagram is shown in Figure 6.2(a) with S_a, S_b and S_c being gate-controlled two-directional switches. The voltage stress for S_a, S_b and S_c is only half of the total output voltage. In order to use 10kV SiC MOSFET in SST, the 24kV DC bus is divided into five levels. A modified five level Vienna Rectifier is shown in Figure 6.2(b).



(a)



(b)

Figure 6.2 Circuit Diagram of Basic Vienna Rectifier (a) and Circuit Diagram of Five-level Vienna Rectifier (b).

Simulation circuit has been implemented in Saber and one-cycle control [66] is used for the five-level Vienna Rectifier. Figure 6.3 shows the simulation waveform of the output voltage and the input phase voltage and phase current. The input voltage and current are in phase, which results in a unity power factor.

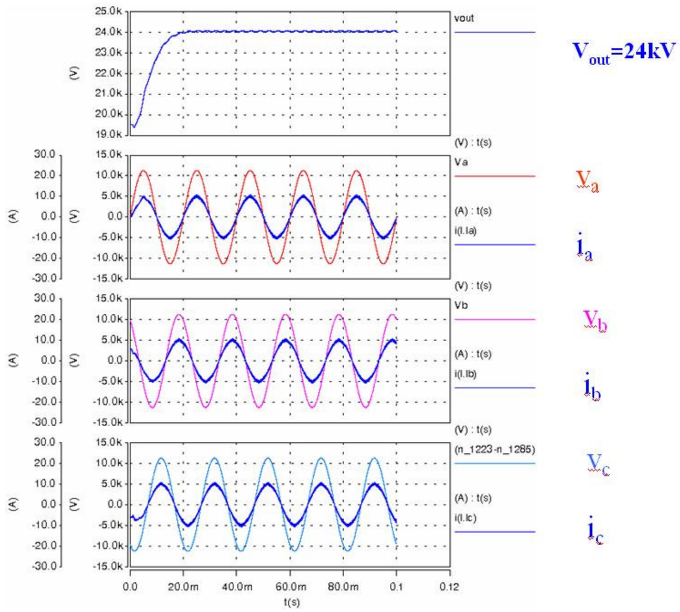


Figure 6.3 Simulation results of Five-level Vienna Rectifier

The conduction losses and switching losses of the 10kV SiC MOSFETs and 10kV PiN diodes are extracted based on device simulations performed on devices with similar structure as those being manufactured by Cree Inc. The calculation is based on the following conditions: V_{IN}=60Hz, 13.8kV AC, V_{DC}=24kV, P_{OUT}=270kW, f_{sw}=20kHz, MOSFET die area = 4mm*4mm and Diode die area = 4mm*4mm. The simulated 10 kV SiC DiMOSFET forward I-V curve and switching loss vs. load current are shown in Figure 6.4 and Figure 6.5 [67]. The calculated loss results are listed in Table 6.1.

As can be seen from the Table 6.1, except the switching loss of the MOSFET, all other losses are low and easy to handle. The MOSFET switching losses could be further reduced if more MOSFETs are parallel, or the switching frequency is lower. The simulation results and loss calculation shows the Vienna rectifier is a good option for the rectifier stage of solid state transformer.

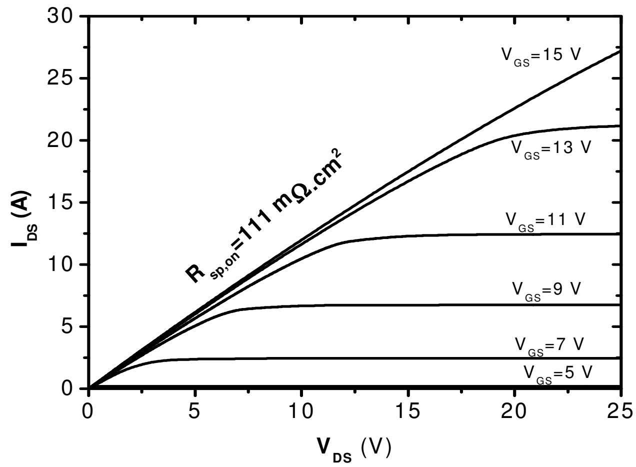


Figure 6.4 Simulated forward I-V curve of 10 kV SiC MOSFET

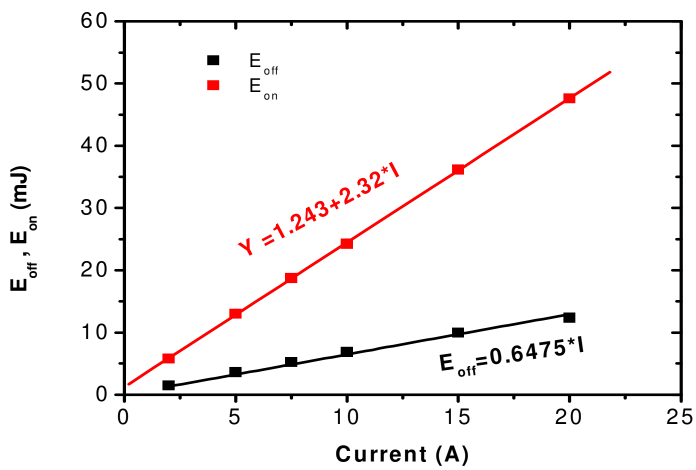


Figure 6.5 Switching loss of SiC MOSFET vs. load current.

Table 6.1 Loss analysis of Five-level Vienna Rectifier

	Conduction Loss	Switching Loss	Total Loss
S_a1 or S_a2	17.9W	681.7W	699.6W
D_ap or D_an*	13.9W*4	29.9W*4	43.8W*4
D_a1 to D_a8	4.9W	29.9W	34.8W

* (each has four PiN diodes in series to sustain 24kV)

6.2. ZVS operation of five-level DC/DC converter

After the 13.8kV AC voltage is rectified to a 24kV five-level DC output, the DC/DC converter and high frequency transformer are needed to step down the voltage to 750V DC. Then the voltage source inverter serves as the final stage to invert 750V DC to 60 Hz, 480V AC.

In order to realize the high frequency DC/DC converter with input voltage as high as 24 kV, high voltage power devices with low conduction and switching losses are needed. Although these SiC devices achieve improved characteristics when compared with their silicon counterpart, there are still significant power losses in the devices when they are hard-switched at high voltage, high current and high frequency. Figure 6.5 shows the turn-on and turn-off loss of the simulated 10 kV SiC DiMOSFET switching loss vs. load current. The turn-on loss is significantly higher than turn-off loss due to large reverse recovery current caused by the 10 kV PIN diode. Therefore, a significant loss reduction will be achieved if the MOSFET turn-on loss can be reduced or eliminated.

In this section, a novel Zero Voltage Switching (ZVS) five-level DC/DC converter is proposed to eliminate the MOSFET turn-on loss. The circuit diagram and the gating signals are shown in Figure 6.6and Figure 6.7, respectively. Likewise, five levels are chosen in order to support a high input voltage of 24 kV using 10 kV SiC MOSFET. The difference between the proposed structure and the basic neutral-point-clamped (NPC) multilevel converter is the inclusion of three flying capacitors Cs1, Cs2 and Cs3. These additional capacitors enable the operation of ZVS for the main switches with phase shift control [68][69][70].

The five-level DC/DC converter is operated in eleven stages by phase shifting switch S1-S8 as shown in Figure 6.7. For instance, during [t0-t1], switches S5, S6, S7 and S8 are ON, and the input power is delivered to the output. During [t1-t2], S8 is turned off, so the voltage across S8 rises to the voltage of C4 (6kV). Meanwhile the voltage across S1 must decrease to 0 due to the clamping effect of C1-C4 and Cs3. Then S1 could be turned on after its voltage reduces to 0, so the ZVS turn-on of S1 is achieved. The other switches S2, S3, S6-S8 are turned on and off in the same manner, however S4 and S5 are a little different.

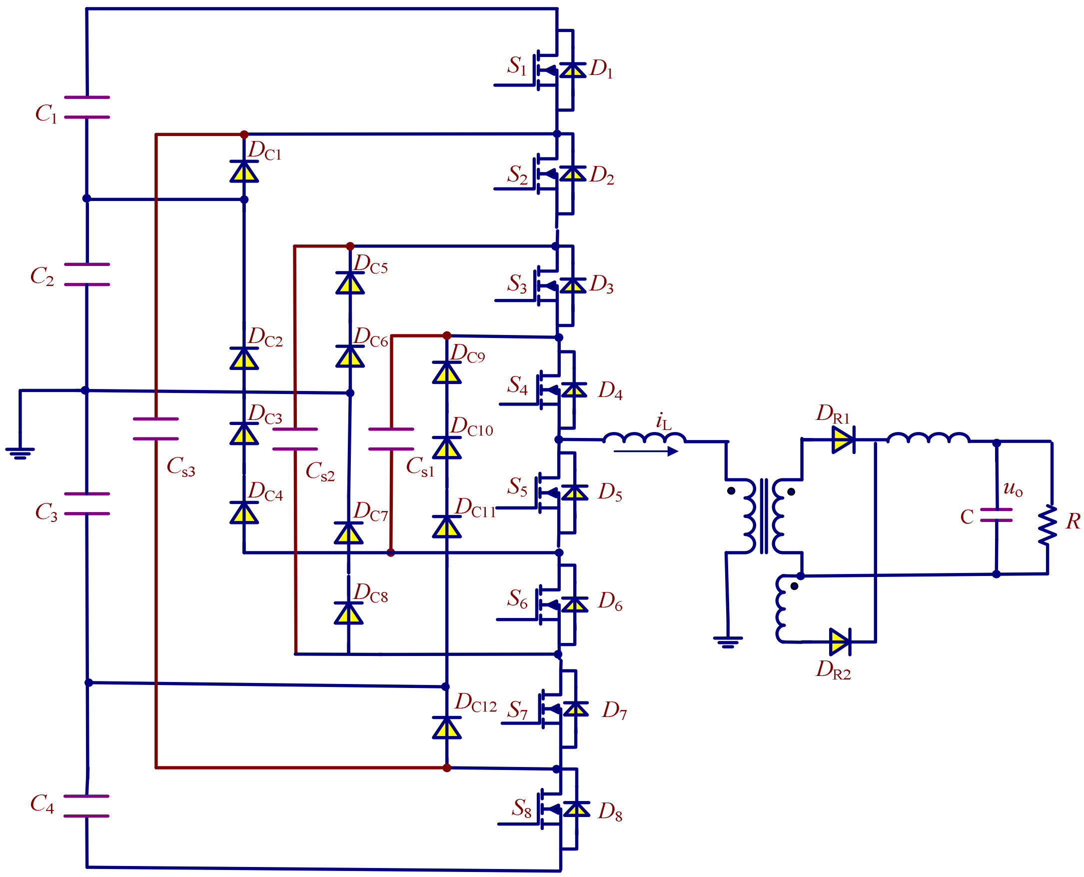


Figure 6.6 Circuit Diagram of Five-level DC/DC converter

The detailed operation principle can be described in the 10 time intervals as shown in Figure 6.7. It is assumed that the circuit works in steady state. The voltage across each of the four input capacitors, C1 to C4, is 6kV. So the total input voltage is 24kV. The voltage across the three flying capacitors, Cs1, Cs2 and Cs3, are 6kV, 12kV and 18kV, respectively. Also, the phase shift between S1, S2, S3 and S4 is assumed to be equal, so is the phase shift between S8, S7, S6 and S5.

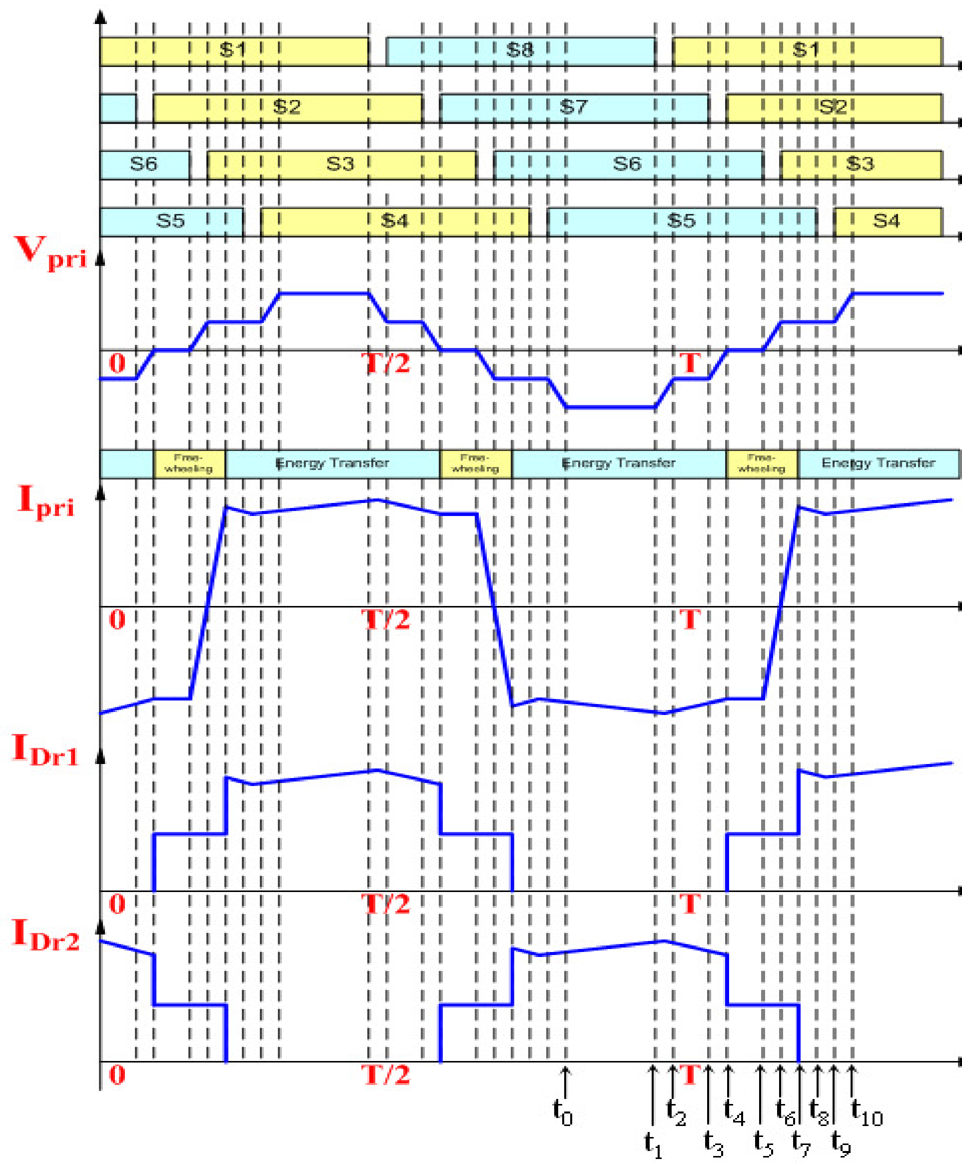


Figure 6.7 Five-level DC/DC converter: Gate signal timing scheme and waveforms (The top four rows are the gate signals for the eight MOSFETs, Vpri is the voltage of the node between S4 and S5 with respect to the ground, Ipri is the primary current of the transformer, and IDr1 and IDr2 are the current flowing through the two secondary diodes, respectively.)

[t0-t1]: During this stage, switches S5, S6, S7 and S8 conduct, and the input power is delivered to the output.

[t1-t2]: The gate signal for S8 goes to 0 and turns off S8, and the drain voltage of S8 rises to 6kV. In the meantime the drain voltage of S1 must decrease to 0 due to the clamping effect of C1-C4 and Cs3. The gate turn-on signal is applied to S1 after its drain voltage reduces to 0, so that the ZVS turn-on for S1 is realized.

[t2-t3]: The primary current goes through the clamping diode Dc12 and C3 after S8 is turned off.

[t3-t4]: The gate signal for S7 goes to 0 and turns off S7, and the drain voltage of S7 rises to 6kV. In the mean time the drain voltage of S2 has to decrease to 0 due to the clamping effect of Cs2 and Cs3. The gate turn-on signal is applied to S2 after its drain voltage reduces to 0, so that the ZVS turn-on for S2 is realized.

[t4-t5]: The primary current goes through the clamping diodes Dc7 and Dc8 after S7 is turned off.

[t5-t6]: The gate signal for S6 goes to 0 and turns off S6, and the drain voltage of S6 rises to 6kV (if the transformer primary current is large enough). In the mean time the drain voltage of S3 has to decrease to 0 due to the clamping effect of Cs1 and Cs2. The gate turn-on signal is applied to S3 after its drain voltage reduces to 0, so that the ZVS turn-on for S3 is realized. It should be pointed out that the drain voltage change for S3 and S6 are accomplished by the energy stored in the resonant inductor. So the primary current in this time interval is not equal to the load current reflected to the primary side, which is the case for S1/S8 and S2/S7. So the resonant inductor needs to be large enough so that its stored energy can complete the voltage change for S3 and S6.

[t6-t7]: Assuming the transformer primary current is still negative, the resonant inductor is discharged by a 6kV DC voltage. The primary current has two possible paths to flow. One is (ground, primary winding, resonant inductor, S5, Cs1, D3, D2, D1, C1, C2, ground), and the other path is (ground, primary winding, resonant inductor, S5, Dc4, Dc3, Dc2, C2, ground).

[t7-t8]: The gate signal of S5 turns to 0. It is assumed the transformer primary current is still negative. The remaining energy in the resonant inductor will charge the drain voltage of S5 to 6kV if the energy stored in the leakage inductance is enough. In the mean time the drain voltage of S4 has to decrease to 0 due to the clamping effect of Cs1.

[t8-t9]: The gate signal of S4 goes to high. The primary current is changed to positive direction and rises rapidly to the reflected load current.

[t9-t10]: After the S4/S5 switching, the primary current now goes through S1, S2, S3 and S4. The input power is delivered to the output. This stage will end when S1 is turned off, and a similar process will happen again.

To verify the working principle and performance of the proposed converter and demonstrate the viability of 10kV SiC power devices for operation at 20 kHz, the five-level converter is simulated using Saber circuit simulator. A SPICE model for the SiC MOSFET and the level one model for the PIN diode are developed and implemented in Saber. The main simulation parameters are V_{in}=24kV, V_{out}=750V, P_{out}=270kW, f_{sw}=20kHz, phase shift=1.5-4us, dead time=1us, turns ratio = 24:2:2 and L_r=130uH.

Figure 6.8 shows the ZVS operation of the switches. During turn-on time, $V_{DS(s1)}$ falls down before $I_{d(s1)}$ rises up, so the turn on for S_1/S_8 is ZVS. Likewise, the waveforms verify the

ZVS operation for S_2/S_7 and S_3/S_6. However, $V_{DS(s4)}$ falls down after $I_{d(s4)}$ rises up, so it is a hard turn-on for S_4/S_5. But if the value of the resonant inductor is increased, it is possible to realize soft switching for S_4 and S_5 as well because more energy is stored in the resonant inductor. So the proposed phase shift pattern for five-level DC/DC converter ensures six switches S1-S3, S6-S8 operating with ZVS turn-on, whereas the middle two switches S4, S5 may lose ZVS under light load condition.

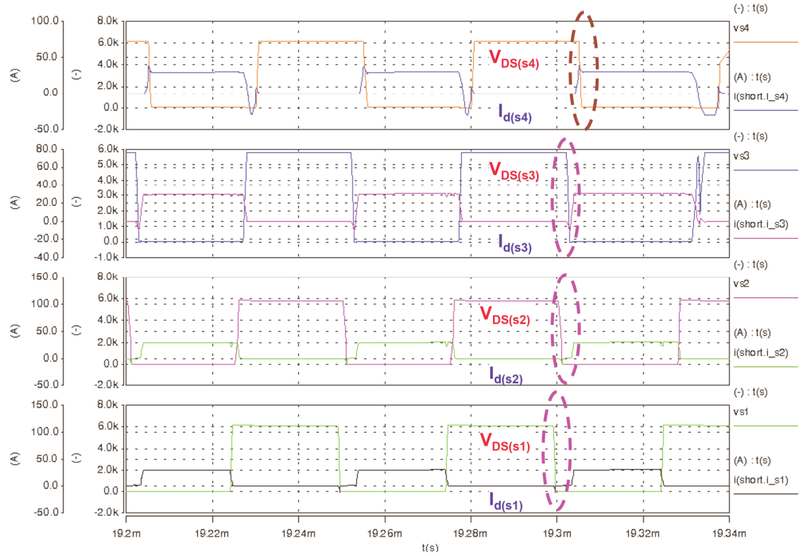


Figure 6.8 Simulation waveforms showing ZVS operation (Time scale = 20us/div) (From top down, voltage and current for Switch S4, S3, S2 and S1 respectively)

Table 6.2 shows the conduction and switching losses of the MOSFETs with hard switching at an output power of 270 kW.

Table 6.3 summarizes the losses of the MOSFETs with ZVS operation. Due to the ZVS turn-on of most switches, the losses in the SiC MOSFET and diodes are significantly reduced compared to hard-switched converters. The major losses are the turn-on loss of switch S4 and S5, while the other MOSFETs and diodes losses are much less significant. Comparing to the hard switching loss, the switching loss with ZVS operation is reduced by 75%. Therefore, the losses are still low enough that conventional thermal management (water, air) can be used to cool the 10 kV SiC MOSFET/diode module.

Table 6.2 Calculated MOSFET losses without ZVS operation

Power loss for each MOSFET S1-S8 (Unit: W) Hard Switching			
Conduction	Turn on	Turn off	Total loss
288	1200	8.6	**1497**

Table 6.3 Calculated MOSFET losses with ZVS operation

Power loss for the MOSFETs at 100% load (Unit: W)				
	Conduction	**Turn on**	**Turn off**	**Total loss**
S_1 or S_8	253	0	8.6	261.6
S_2 or S_7	277	0	8.6	285.6
S_3 or S_6	288	0	8.6	296.6
S_4 or S_5	250	**1200**	8.6	**1459**

6.3. Closed loop simulation of five-level Vienna rectifier and DC/DC converter

To verify the functionality of the system, the closed loop control for both Vienna Rectifier and DC/DC converter are designed respectively. The control block is shown in Figure 6.9.

In five-level Vienna Rectifier, one-cycle control [66] is employed. The closed loop controller is to regulate the output DC bus voltage (24kV) and maintain the unity power factor at the input.

For the five-level DC/DC converter, the phase shift control is used to regulate the output DC voltage under different output load conditions. First the difference between the output voltage V_{DC} and the reference voltage is compared. Then the phase shift angle is adjusted to regulate the output voltage according to this voltage error.

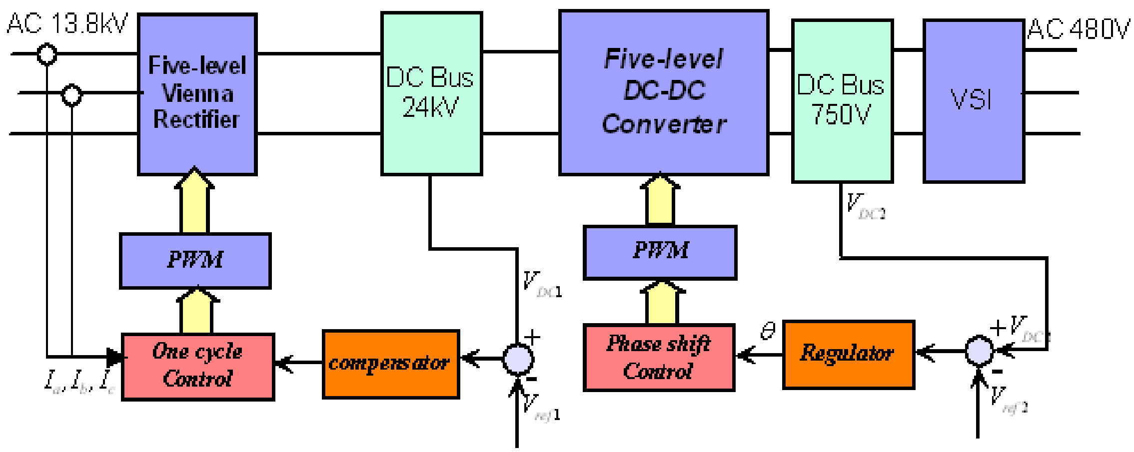


Figure 6.9 Control block of the DC/DC converter

Figure 6.10 is the closed loop simulation result taken into account different load conditions. The load is changing from 100% (P_{out}=270kW) to 150% at 20ms, then from 150% to 100% at 25ms, from 100% to 30% at 30ms. It can be seen from the simulation waveforms that the output voltage can be regulated at 750V at different load conditions by adjusting the phase shift.

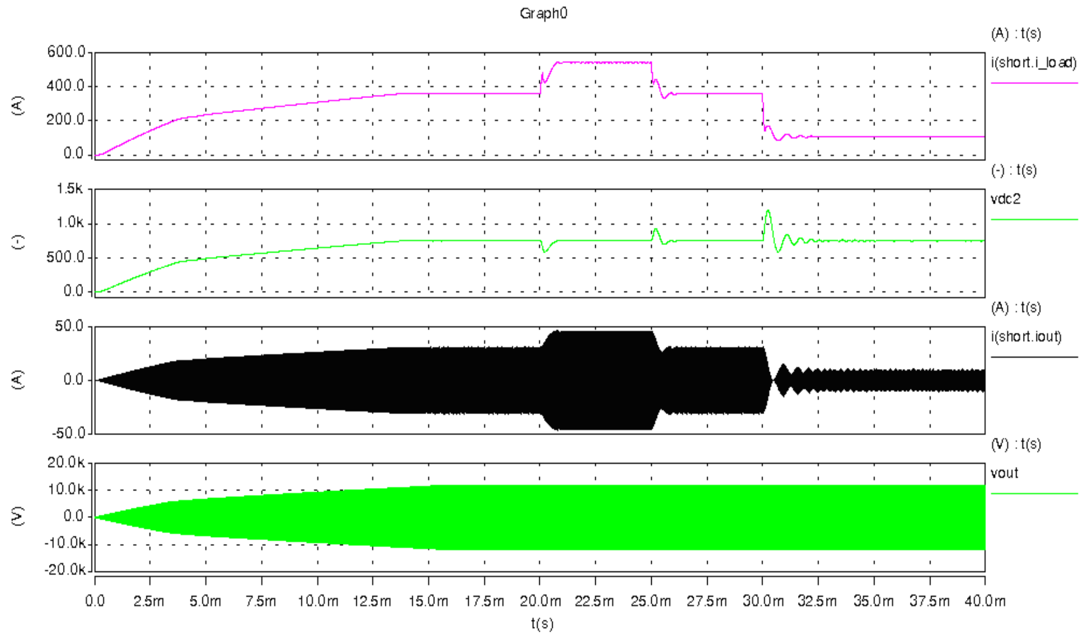


Figure 6.10 Five-level converter closed loop simulation under different output load conditions (Top trace: load current, 200A/div; second top trace: load voltage, 500V/div; third top trace: transformer primary current: 50A/div; bottom trace: the voltage of the node between S4 and S5, 10kV/div). (Time scale=2.5ms/div)

Figure 6.11 shows the simulation results with the disturbance of single phase voltage sag. The magnitude of input phase A voltage changes from 100% in the 1st cycle to 80% in the 2nd and 3rd cycles. Phase B and C voltages are normal. During the voltage sag, the rectifier output voltage varies a little around 24kV, but the five-level converter output can be stabilized at 750V and the input current still maintains a good power factor.

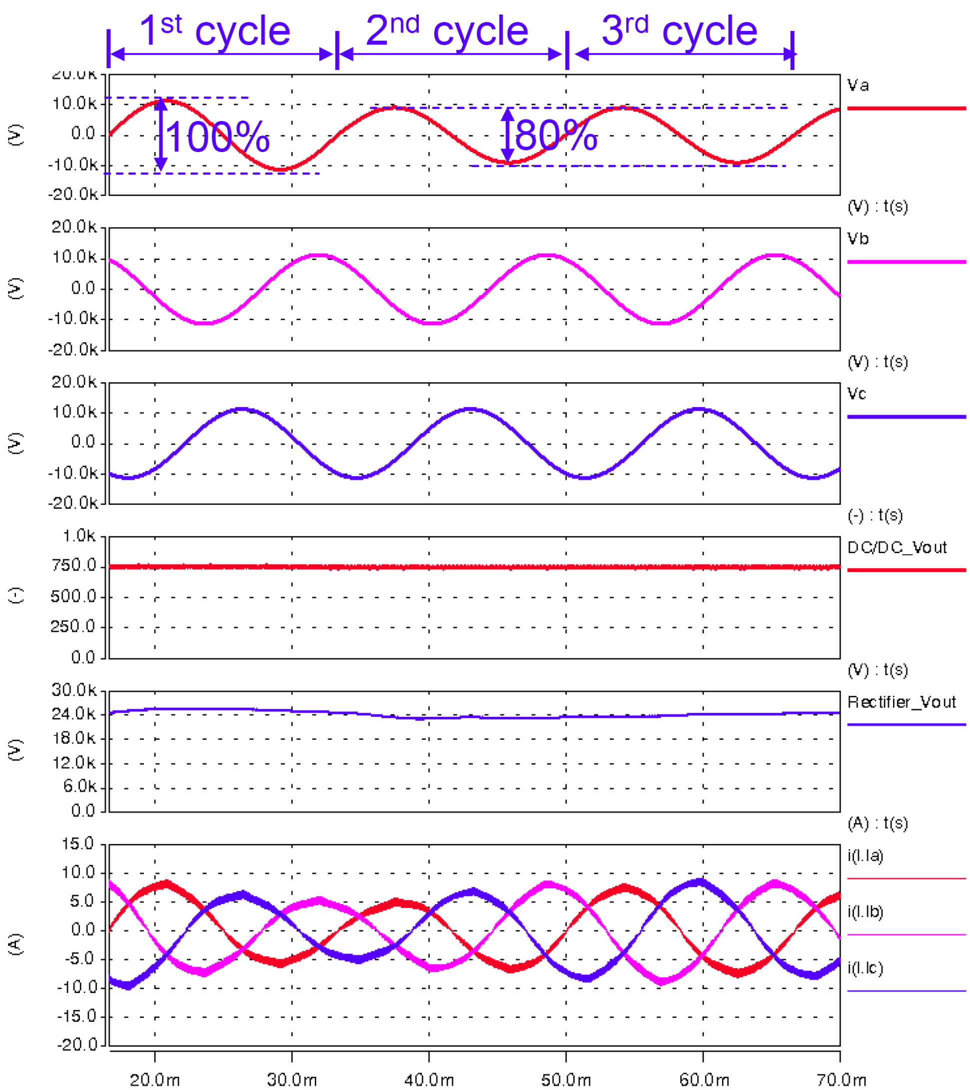


Figure 6.11 Closed loop simulation under input voltage sag (Top trace: Input phase A voltage, 10kV/div; second top trace: Input phase B voltage, 10kV/div; third top trace: Input phase C voltage, 10kV/div; fourth top trace: Five-level DC/DC converter output voltage, 250V/div; fifth top trace: Viennia rectifier output voltage, 6kV/div; bottom trace: three phase input current, 5A/div). (Time scale=10ms/div)

The simulation results illustrate that the solid state transformer is not susceptible to both source and load disturbance. The voltage sag ride-through characteristic protects load from input voltage sags and greatly enhances the power quality.

6.4. Summary

In this chapter, a 270 kVA substation solid state transformer using 10kV SiC Power MOSFET and JBS diodes has been proposed. Vienna rectifier is employed in the rectifier stage, which enables the substation SST a unity power factor. A novel ZVS five-level DC-DC converter is proposed. By employing a phase shift control, the five-level DC-DC converter allows ZVS soft-switching operation for most of the main devices. This significantly reduces the turn-on loss of the MOSFETs and improves the overall efficiency. The ZVS operation is verified by the circuit simulation in Saber. Meanwhile, the closed loop controller of the substation solid state transformer system is designed. The simulation results verify the functionality and feasibility of the rectifier and DC/DC converter stage. Furthermore, based on the device characteristics from physics simulation, the devices losses are calculated. The losses are low enough that conventional thermal management (water, air) can be used to cool the 10kV SiC MOSFET/diode module. The above simulation results and loss analysis justify that the 10kV SiC power device is a valid option for the future substation solid state transformers.

Chapter 7. Conclusions

This dissertation proposes a cascaded multilevel H-Bridge converter based SST, including AC/DC rectifier, Dual Active Bridge (DAB) and DC/AC inverter stage for interfacing with the single phase 7.2kV distribution system.

The switching model, average model and small signal model of the SST, including the rectifier, dual active bridge and inverter stage are developed. Based on the small signal model and bode plot, the dq axis vector controller is designed. The average and switching model simulation including unbalanced load, voltage sag, regenerative mode and short circuit fault are presented and verified the proposed controller.

In order to solve the voltage unbalance problem of the cascaded H-Bridges, a novel voltage control strategy is proposed based on the single phase d-q vector controller. However, due to the intrinsic constraints of the cascaded H-Bridge circuit, the unbalance power range of each H-Bridge is limited. The power unbalance constraints of the cascaded H-Bridge rectifier are derived. Furthermore, a power balance control is proposed to balance the real power of the DAB parallel modules. The SST switching model simulation and the hardware prototype experiment demonstrate the effectiveness of the proposed voltage balance controller.

In order to minimize the DC bus voltage ripple and required capacitor size, a feed-forward ripple power control method for the DAB stage is proposed and a power synchronization method for the inverter stage are designed. The proposed methods are based on the power synchronization of input and output, including the rectifier, DAB and the inverter stage. The simulation results verify the proposed controller and the required capacitance can be reduced effectively.

Moreover, a hardware prototype of the cascaded H-Bridge rectifier in the solid state transformer is implemented. The detailed hardware design and the model based controller are presented in details. The steady state performance, reactive power control, load unbalance and dynamic load change, power unbalance limit, input voltage sag and swell, rectifier operation state machine, voltage loop notch filter are all verified by the experiments. The experiments illustrate the design feasibility and the performance of the controller.

Finally, a 270 kVA substation solid state transformer using 10kV SiC Power MOSFET and JBS diodes has been proposed. A novel ZVS five-level DC-DC converter and its ZVS soft-switching operation are proposed. This significantly reduces the turn-on loss of the MOSFETs and improves the overall efficiency. The closed loop controller of the substation solid state transformer system is designed. The simulation results verify the functionality and feasibility of the rectifier and DC/DC converter stage. Furthermore, based on the device characteristics from physics simulation, the devices losses are calculated to verify the system feasibility.

The future work of this research includes:

1) System level SST control strategy. The proposed SST will be part of the Intelligent Energy Management (IEM) in the FREEDM system. The system level control needs to address how to control the SST to optimize the FREEDM system power

management. This includes multiple SST communications and coordination, multiple SST power sharing, SST response to system fault.

2) SST protections. The SST needs to work well with the traditional power grid. However, the protection of the traditional power system is much slower than the power electronics response time. The SST protection needs to be fast enough to protect to power electronics system, but also compliant with the traditional system protection, such as relay protection and re-closing. The control of SST islanding mode also needs to be further investigated.
3) SST high voltage high frequency hardware implementation. The high voltage rectifier converter, high frequency transformer, high voltage power device packaging, thermal management are all challenging issues in the SST hardware implementation and need further investigation.

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