US007015533B2

(12) **United States Patent**
Basceri et al.

(10) **Patent No.: US 7,015,533 B2**
(45) **Date of Patent: Mar. 21, 2006**

(54) **CAPACITOR CONSTRUCTIONS, SEMICONDUCTOR CONSTRUCTIONS, AND METHODS OF FORMING ELECTRICAL CONTACTS AND SEMICONDUCTOR CONSTRUCTIONS**

(75) Inventors: **Cem Basceri**, Boise, ID (US); **Garo J. Derderian**, Boise, ID (US)

(73) Assignee: **Micron Technology, Inc.**, Boise, ID (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/917,894**

(22) Filed: **Aug. 13, 2004**

(65) **Prior Publication Data**

US 2005/0020026 A1 Jan. 27, 2005

Related U.S. Application Data

(62) Division of application No. 10/389,659, filed on Mar. 13, 2003, which is a division of application No. 10/094,581, filed on Mar. 6, 2002, now Pat. No. 6,900,106.

(51) **Int. Cl.**
H01L 27/108 (2006.01)

(52) **U.S. Cl.** **257/311**; 257/295; 257/304; 257/305; 257/310; 438/253; 438/256; 438/396; 438/399

(58) **Field of Classification Search** 438/244, 438/253–256, 387, 391, 396–399; 257/304, 257/311

See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,371,701	A	12/1994	Lee et al.	
5,565,708	A	10/1996	Ohsaki et al.	
5,837,591	A	11/1998	Shimada et al.	
5,950,092	A	9/1999	Figura et al.	
6,001,420	A *	12/1999	Mosely et al.	427/258
6,017,144	A	1/2000	Guo et al.	
6,026,882	A	2/2000	Taukamoto	
6,093,615	A *	7/2000	Schuele et al.	438/396
6,096,595	A *	8/2000	Huang	438/238
6,174,781	B1	1/2001	Dai et al.	
6,248,640	B1	6/2001	Nam	

(Continued)

OTHER PUBLICATIONS

Wolf et al., "Silicon Processing for the VLSI Era vol. 1: Process Technology", Lattice Press, 1986, pp. 160-175.

Primary Examiner—Tom Thomas
Assistant Examiner—José R. Diaz
(74) *Attorney, Agent, or Firm*—Wells St. John, P.S.

(57) **ABSTRACT**

The invention includes a method of forming a semiconductor construction. A semiconductor substrate is provided, and a conductive node is formed to be supported by the semiconductor substrate. A first conductive material is formed over the conductive node and shaped as a container. The container has an opening extending therein and an upper surface proximate the opening. The container opening is at least partially filled with an insulative material. A second conductive material is formed over the at least partially filled container opening and physically against the upper surface of the container. The invention also includes semiconductor structures.

15 Claims, 6 Drawing Sheets